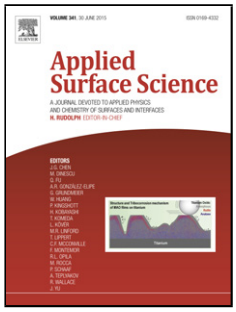

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A study of Selenium nanoparticles as Charge Storage Element for Flexible semi-transparent memory Devices

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Abstract

Flexible Semi-Transparent electronic memory would be useful in coming years for integrated flexible transparent electronic devices. However, attaining such flexibility and semi-transparency leads to the boundaries in material composition. Thus, impeding processing speed and device performance. In this work, we present the use of inorganic stable selenium nanoparticles (Se-NPs) as a storage element and hydrogenated amorphous carbon (a-C:H) as an insulating layer in two terminal non-volatile physically flexible and semi-transparent capacitive memory devices (2T-NMDs). Furthermore, a-C:H films can be deposited at very low temperature (< 40˚C) on a variety of substrates (including many kinds of plastic substrates) by an industrial technique called Plasma Enhanced Chemical Vapour Deposition (PECVD) which is available in many existing fabrication labs. Self-assembled Se-NPs has several unique features including deposition at room temperature by simple vacuum thermal evaporation process without the need for further optimisation. This facilitates the fabrication of memory on a flexible substrate. Moreover, the memory behavior of the Se-NPs was found to be more distinct than those of the semiconductor and metal nanostructures due to higher work function compared to the commonly used semiconductor and metal species. The memory behavior was observed from the hysteresis of current-voltage (I-V) measurements while the two distinguishable electrical conductivity states ("0" and "1") were studied by current-time (I-t) measurements.

Keywords: Amorphous carbon; Selenium Nanoparticles; Flexible memory; two terminal flash memory.

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Introduction

A flash memory is the most famous kind of non-volatile memory. It is ideal for a myriad kind of electronic applications, for instance, laptop computers, digital cameras, mobile phones, etc. Thus, it has been widely used and shows significant role in the electronic market [1]. However, there are still some challenges including the fact that scaling down the thickness of dielectric tunneling gate in flash is essentially challenging while maintaining the memory reliability and data retention [2], and the write and erase voltages are still too high. As a result, memory-cell structures using nanostructures as the charge storage elements have gained much attention. It is also a promising candidate to replace existing flash memory in the near future as it requires less power and can operate at higher speeds [3]. Furthermore, the use of a floating gate consisting of distributed nanostructures (nanoparticles, nano-spherical, nanocrystals) removes the problem such as leakage of charges encountered in the conventional flash memory. It also allows the use of thinner dielectric tunneling gate and, so, the write and erase voltages will be smaller and have better data retention and endurance [4].

The flexible transparent electronic memory device is required for most of the flexible electronic applications. The main advantage of this kind of memory is fabrication cost which is dramatically lower than the cost of existing technologies. Several kinds of flexible memory devices are based on the use of organic materials [5], [6]. But, the stability of organic based memory devices is still challenging. This work demonstrates the use of all inorganic layers for the fabrication of flexible memory as two terminal capacitive memory, whereas the conventional flash memory consists of three terminals and inflexible.

Most research significantly investigated in the fabrication of semiconductor nanocrystals (such as Si and Ge) to use as charge storage medium in memory cell structures [2], [7], and metal nanocrystals such as Ag, Au, Pt, W, Ni, and Al [1]. In general, metal nanocrystal memory has more advantages such as a varied range of available work functions. The work function plays a vital role in the effective memory [8], where the material with higher work function is preferred because it offers small barrier for programming process and large barrier for data retention [1]. Hence, Pt and Au are used in conventional memory devices, but they are very expensive. Thus, material to be used should not be expensive and high work function is more desirable for instance Se. The work function of Se (5.11ev)[9] is higher than work function of many metal materials including Ag (4.33ev), Au(5.1ev), W(4.55ev), Ni (4.96ev), TiN (2.92ev) and Al (4.24ev) [1].

In addition, selenium, as a non-metal, demonstrates remarkable photoelectrical property that has been successfully exploited/proposed for solar cells, rectifiers, signal emitting devices, transmitting devices, xerography and photographic exposure meters [10] related applications. Recently, Se-NPs have been attracting more consideration due to their excellent unique structural and electronic properties that facilitate its use in memory devices. Amongst several fabrication techniques, Se-NPs can be deposited by a simple technique, low-cost vacuum thermal evaporation process at room temperature without the need for further treatment on a variety of substrates (including flexible transparent plastic). In this work, the flexible semi-transparent non-volatile memory device is inexpensively fabricated at very low temperature using stable inorganic layers (Se-NPs as storage medium and a-C:H as a dielectric layer).

Experiment details:

A reference device (without Se-NPs) and two terminal memory devices (with SeNPs evaporated at 0.1nm/s for 10 and 50sec) were fabricated (as shown in Fig-1) by thermal evaporation (with base pressure 1×10^{-7} mBar vacuum, and at <32˚C as shown in Fig-2 (a-1) of the bottom contact electrodes (four Aluminium (Al) tracks: 100 nm thick, 1 mm wide and 22 mm long) onto a plastic substrate (Lexan 8010 sheet is transparent polycarbonate film), then a 13.56 MHz RF PECVD was used to deposit 35nm a-C:H dielectric layer film as a blocking layer at very low temperature (< 40˚C as shown in Fig-2 (b)). The a-C:H film was deposited at very low temperature using argon (Ar) and methane (CH_4) gasses at a chamber pressure of 100 mTorr, radio frequency (RF) power of 100W, -80Vdc self-bias. Following this, Self-assembled Se-NPs was deposited at room temperature as shown in Fig-2(a (2)). In this work, Se was evaporated in the thermal evaporator for 10sec and 50sec at 0.1nm/s, respectively. From hereon, we refer these samples as SeNPs-10sec and SeNPs-50sec. Scanning electronic microscope (SEM) was used to gather information about the size of Se-NPs. Subsequently, another dielectric film of a-C:H (8 nm thin layer) was deposited on top of the selenium nanoparticles that act as a tunneling layer with the same growth conditions as described for the a-C:H blocking layer. Finally, the top Al electrodes were evaporated in a perpendicular direction to the bottom contacts as shown in Fig-1.

Selenium nanoparticles:

Morphology of self-assembled nanoparticles evaporated at the rate of 0.1nm/sec for 10sec and 50sec at room temperature is shown in Fig-3 and Fig-4, respectively. To gather more information about Se-NPs from Fig-3 and Fig-4, IMAGE-J and SmartTiff softwares are utilised

to perform particle analysis. Procedure for particle analysis included smoothening, varying brightness and contrast, bandpass filter, threshold, watershed and particle analysis for obtaining the desired parameters. Circularity for measuring particles was set between 0.0 to 0.95. However, Scanning Electron Microscope used in this work (Carl-Zeiss Evo 15) could resolve particles with a diameter of 40nm and above. We do not have data for nanoparticles with a diameter below 40nm.

It is clear from SEM images that diameters of self-assembled Se-NPs are between 40nm to 130nm that are formed during 10sec deposition and 80nm to 160nm that are formed during the 50sec deposition process. The histogram in Fig-5 shows that the majority of nanoparticles has diameter <80nm and >120nm at deposition time 10sec and 50 sec, respectively, However, when an electron is tunnelled and stored in nanoparticle, the nanoparticle potential energy is increased as a result of the electrostatic charging energy $e^2/2C$, where 'e' is elementary charge ($1.60217662 \times 10^{-19}$ coulombs) and C is the nanoparticles capacitance, which relies on nanoparticle size [11]. Hence, 2T-NMDs were fabricated and tested with two samples (SeNPs-50sec and SeNPs-10sec), to understand the effect of particle diameter that has the ability to serve as a better non-volatile memory device.

Principle of the device operation

The working mechanism of 2T-NMDs depends on the charging of storage medium (Se-NPs), where the probability of charge injection/tunnelling through the top a-C:H layer (tunnelling layer) is high when a positive voltage is applied. The thickness of tunnelling layer (8nm) is thinner than the blocking layer (35nm) as depicted in Fig-6. As a result, the direct tunneling phenomenon is expected in this memory.

The model explained below (in Fig-7, Fig-8, Fig-9, Fig-10 and Fig-11) is used to describe the generation of the internal electric field and its utilisation of bistability in electrical conductivity. The memory effect will only exist when an external electric field is applied. Thus, there is no tunnelling or storage of charges in Se-NPs when V=0, as shown in Fig-7. However, when a positive external field (E_0) is applied across the memory device ($V_{write} > 0$) the tunnelling phenomena will dominate and the charges tunnel through the dielectric tunnelling layer (a-C:H

film) and stored in Se-NPs as depicted in Fig-8. In this case V_{write} = +5V and measured current value I = +5nA at point (1). This process is called programming of memory.

Subsequently, when E_0 was removed, the created negative internal electric field (E_i) remains, due to stored charges within the Se-NPs. Therefore, during the read operation, when small positive external field (E_0) is applied (V_{read} =0.5V < V_{write}) a dramatic drop in the current is observed, as the net electric field is more than applied electric field, as shown in Fig-9, as a consequence, the measured current is negative (I = -2 nA) at point (2) and represents the low conductivity (state '0') of a memory bit.

Nevertheless, during the erasing operation, the charges will tunnel back from the storage medium when the negative external field is applied across the memory (V_{erase} = - V_{write} = -5V), as shown at point (3) in Fig-10. In this case, the internal field (E_i) is completely removed.

Again the read operation is performed after the erase operation has completed. For which a small positive external field is applied (V_{read} =0.5V < V_{write}) and a significant increase in the current is observed at point (4) (high conductivity, state '1') compared to point (2) (low conductivity, state '0') as there is no internal electric field (E_i) as shown in Fig-11.

To conclude this working mechanism of 2T-NMDs, the Se-NPs facilitate storage of charges, which generates an internal electric field (E_i) inside the memory. I-V hysteresis and electrical bistability rely on the direction of the external field (E_o) which can either match or oppose the internal field (E_i). This model is used to describe the generation of the internal electric field and the realisation of the bistability, which is a key parameter for the proposed 2T-NDMs.

Results and Discussion

I-V measurements were carried out on three different types of devices. A reference device (Fig-1(a)), 2T-NMDs containing (SeNPs-50sec) (Fig-1(b)) and 2T-NMDs containing (SeNPs-

10sec) (Fig-1(c)) were used to investigate the ability of Se-NPs to store electrons as the storage elements in the memory device.

The voltage was swept from -5V to +5V on the devices as shown in Fig- 12. The arrows indicate the direction of the sweep. However, the 2T-NMDs containing SeNPs-10sec shows a large hysteresis compared to another device (Fig- 12 (3)). This is attributed to the ability of the of smaller diameter Se-NPs to serve as a storage medium which is also confirmed by measured hysteresis in an I-V curve that reflects in the electrical behaviour of the charges stored in Se-NPs. However, the 2T-NMDs containing SeNPs-50sec shows memory behaviour but it has its share of disadvantages. Such a device increases in the area, which not consistent with the direction of shrinking the memory applications. Moreover, it was not able to store more charges (Area of hysteresis as shown in Fig- 12 (2)) compare to the memory containing SeNPs-10sec. This is attributed to the quantum confinement, which becomes significant when the nanoparticle size shrinks to the range of 1-100nm. Due to discrete energy levels in the conduction band of nanoparticles and shifts in the energy levels to higher states is observed compared to large sized particles or bulk material [12].

The most important factor of any memory device is the lifetime that it can retain the information (charges) [13], [14]. Therefore, the charge retention measurements are performed to monitor the two conduction states, ‘0’ and ‘1’, over a certain time (1000 seconds). Fig-13 illustrates the retention time characteristics of the reference device without Se-NPs and 2T-NMDs containing SeNPs-10sec on plastic substrates. For switching to the low state ‘0’, the high positive voltage (Vwrite= +5V) is applied to both devices, followed by a lesser positive voltage (Vread = +0.5V). Thereafter, the low state ‘0’ has turned to the high state ‘1’ by applying the high negative voltage (Verase = -5V) and then +0.5V as a read voltage. Moreover, it is very clear from Fig-13(A) that the conductivity states collapsed in the device without Se-NPs. However, a distinct difference (about 21 pA) was retained by the both conductivity states (see Fig-13(B)).

Currently, research is being conducted on improving the retention time for both conductivity states by using bilayers of Se-NPs instead of single-layer as the storage elements in the 2T-NMDs device.

Conclusion:

In brief, the fabrication and characterisation of 2T-NMDs containing Se-NPs on the flexible substrate were presented in this work. We have demonstrated that Se-NPs act as a good medium for charge storage. Current-voltage measurements were performed for 2T-NMDs structures and evidence of the charge being stored in Se-NPs is discussed, this is reflected from hysteresis loops obtained from I-V measurements. The structure fabricated in this work is a semi-transparent flexible non-volatile capacitive memory device. This work suggests that diameter of Se-NPs is a key parameter in the storage of charges and their retention. The hysteresis in I-V measurements revels that Se-NPs (memory containing SeNPs-10sec) with many smaller diameter nanoparticles can store more charges and prove to be a stable memory device. Moreover, the two conductivity states (On and Off) remain distinguishable for a certain period, as shown in the data retention characteristics. This research provides the first proof of concept for storing charges in a non-metal semiconductor selenium as charge storage element in two-terminal memory devices.

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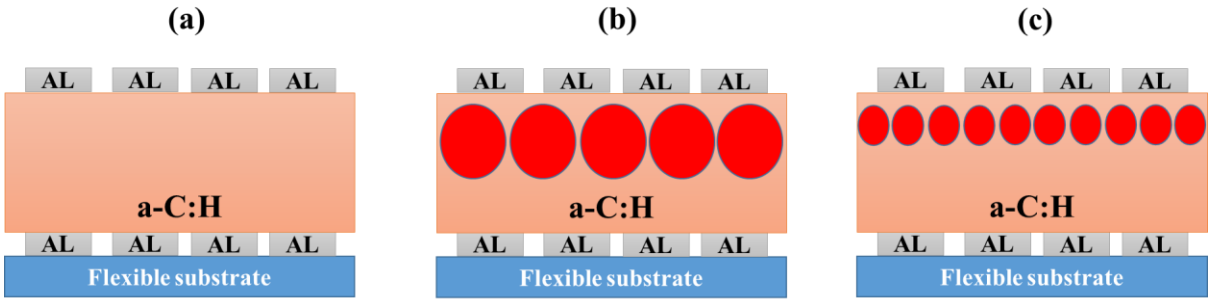

Fig-1: (a) Schematic of the proposed reference device (Al/a-C:H / a-C:H /Al), (b) Schematic of proposed 2T-NMDs (Al/a-C:H /SeNPs-50sec / a-C:H /Al) and (c) Schematic of proposed 2T-NMDs (Al/a-C:H /SeNPs-10sec / a-C:H /Al). The entire memory cell is fabricated on plastic substrate.

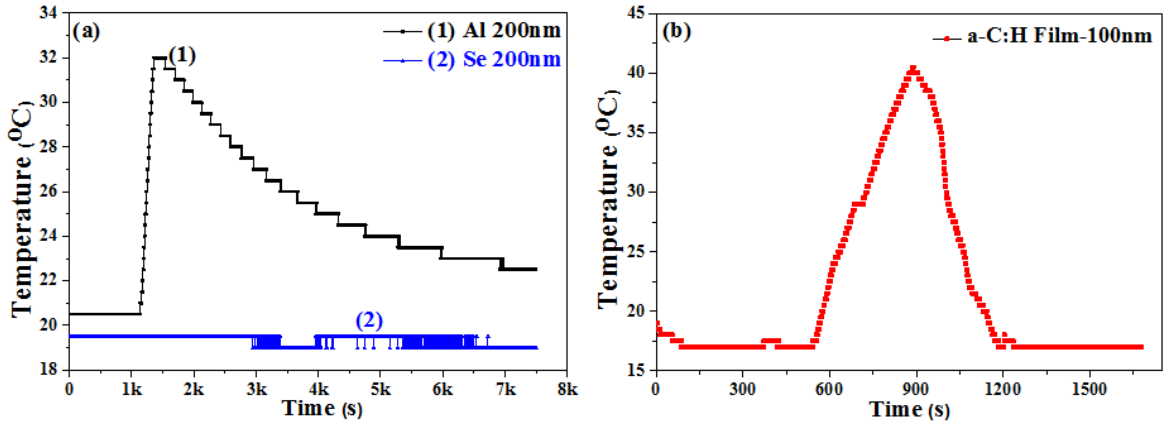

Fig-2: Measured temperature of substrates at with samples were placed in a thermal evaporator and PECVD during the deposition process, (a) evaporation of (1) Al and (2) Se-nanoparticles, (b) deposition of a-C:H film.

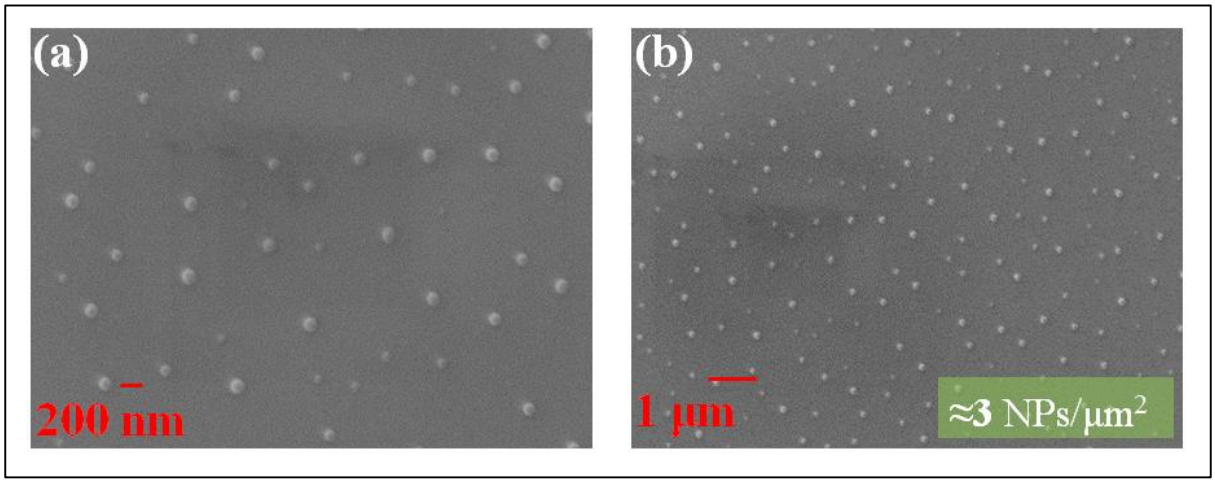

Fig-3: Se-NPs evaporated for 10 Sec at 0.1nm/s: (a) shows small and less number of particles and (b) shows the number of Se-NPs is 23 per/µm^2. The area covered by Se-NPs on the substrate is 18.43%.

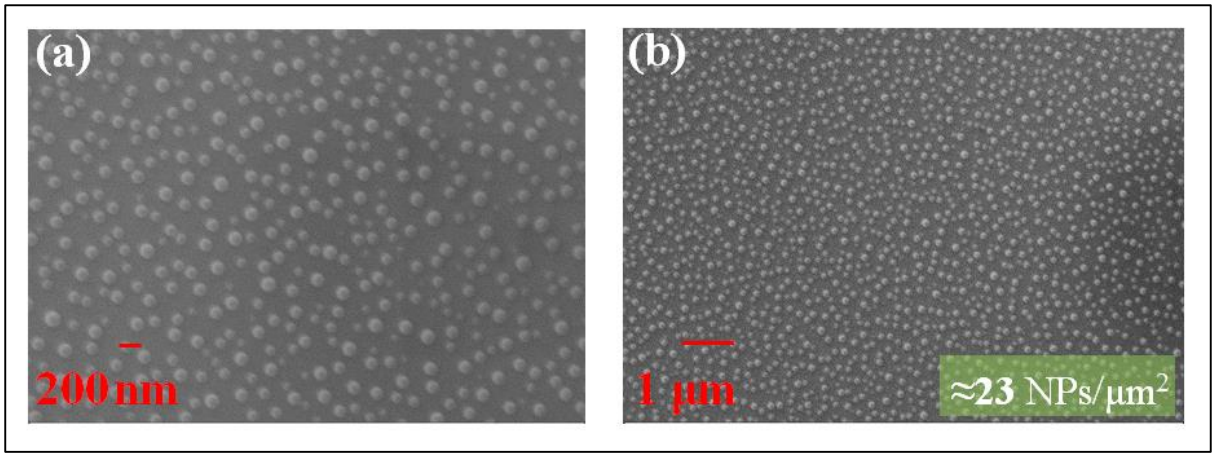

Fig-4: Se-NPs evaporated for 50 Sec at 0.1nm/s, (a) shows many and large numbers of particles and (b) shows the morphology and measured density of Se-NPs (23 per/µm^2). The area covered by Se-NPs on the substrate is 21.62%.

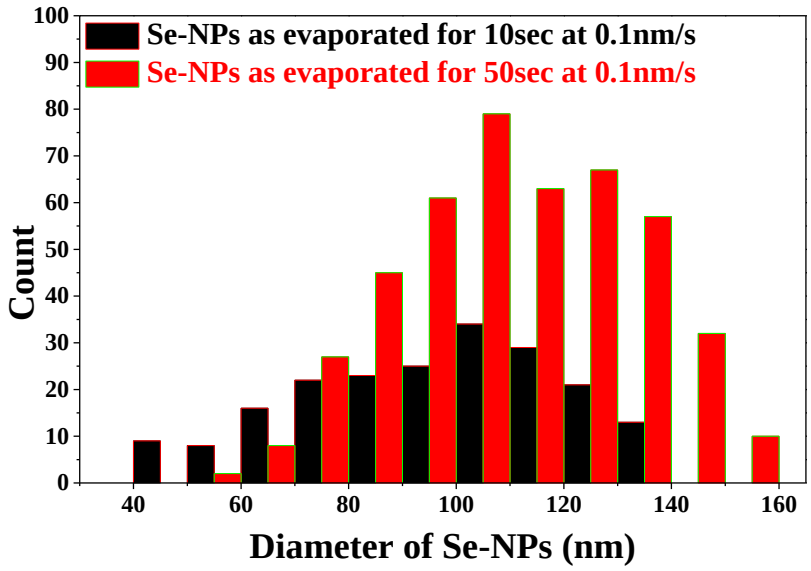

Fig-5: Histogram of Se-NPs evaporated at 0.1nm/s for 10 and 50sec durations.

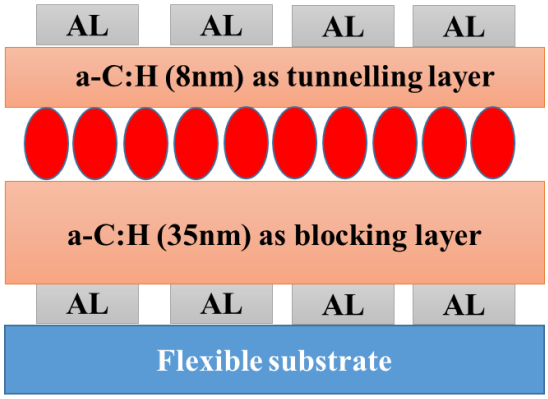

Fig-6: The proposed working mechanism (direct tunnelling) of the 2T-NMDs memory cell with Se-NPs sandwiched between two a-C:H layers as charge storage elements.

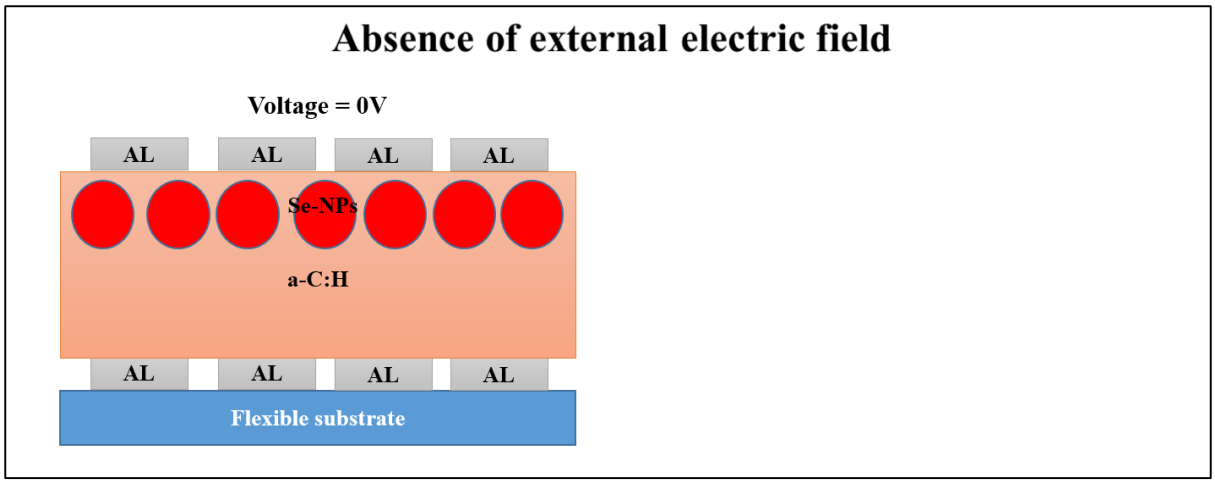

Fig-7: Schematic showing different layers of 2T-NDMs.

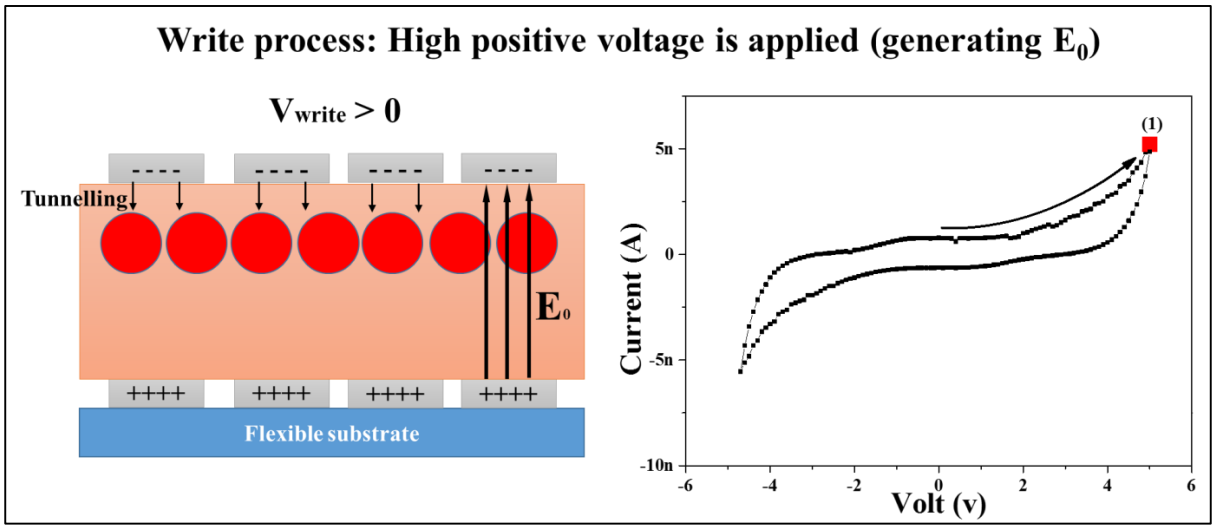

Fig-8: Working mechanism of 2T-NMDs during 'write process' and measured I-V characteristics show point (1) in hysteresis curve.

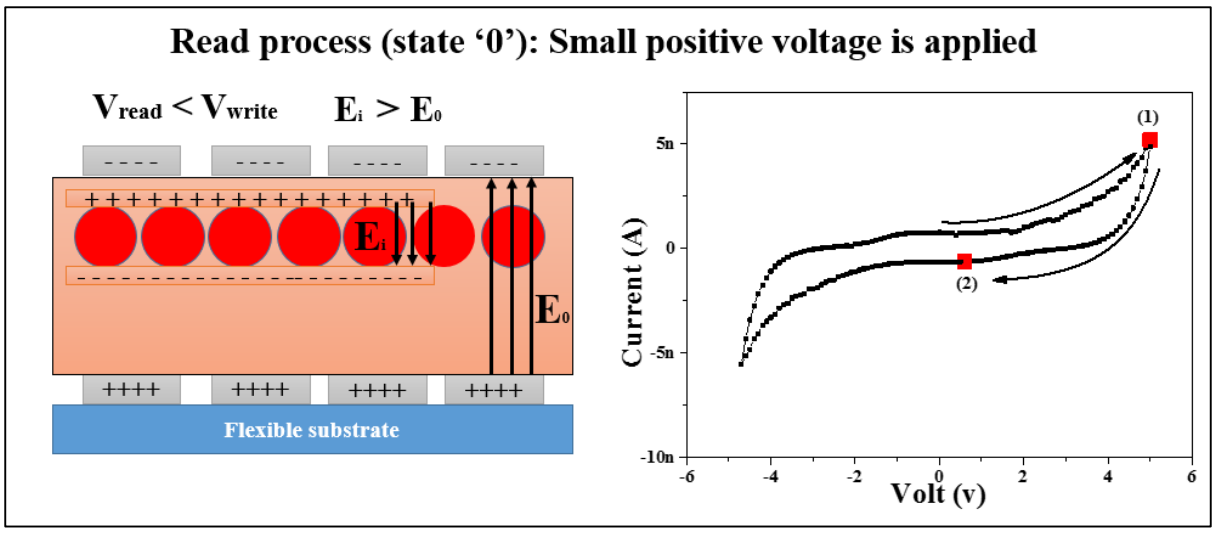

Fig-9: Working mechanism of 2T-NMDs during 'Read process (state '0')' and measured I-V characteristics show point (2) in hysteresis curve as low conductivity state.

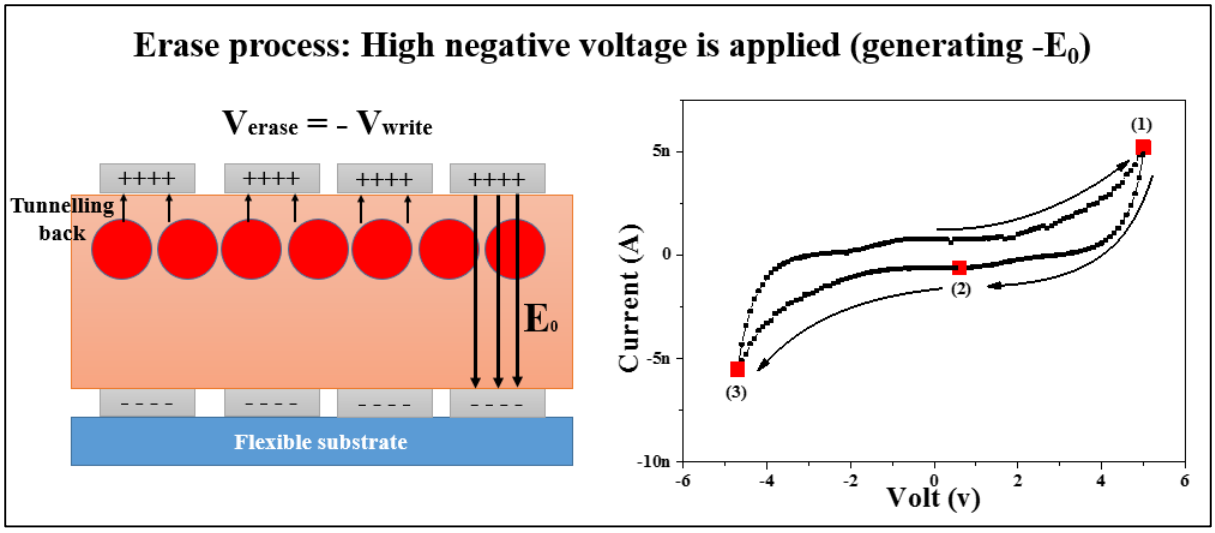

Fig-10:Working mechanism of 2T-NMDs during 'Erase process' and measured I-V characteristics show point (3) in hysteresis curve.

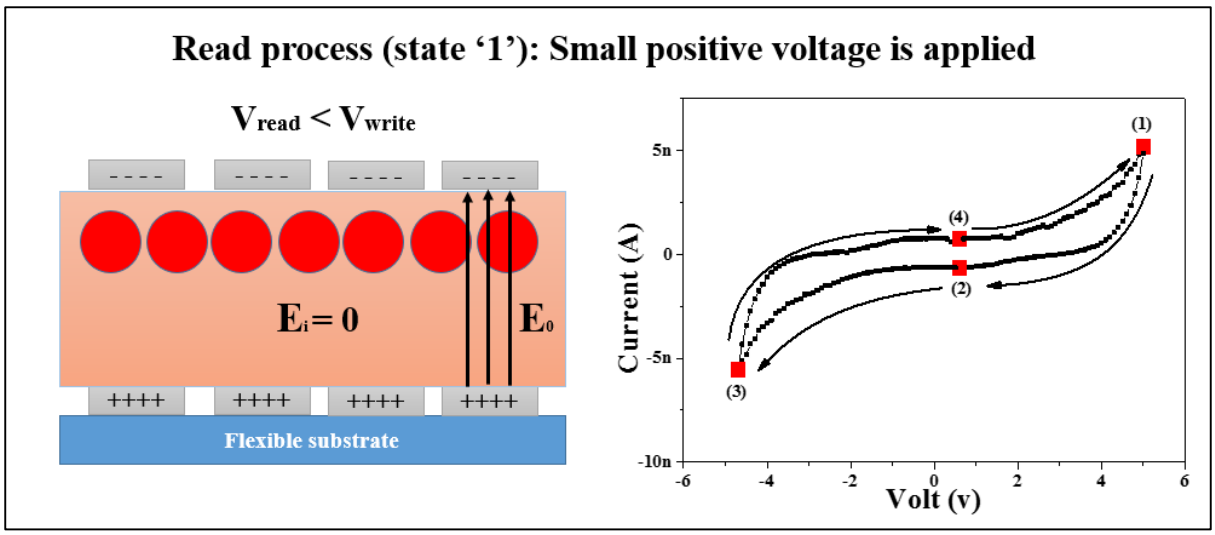

Fig-11: Working mechanism of 2T-NMDs during 'Read process (state '1')' and measured I-V characteristics show point (4) in hysteresis curve as high conductivity state '1'.

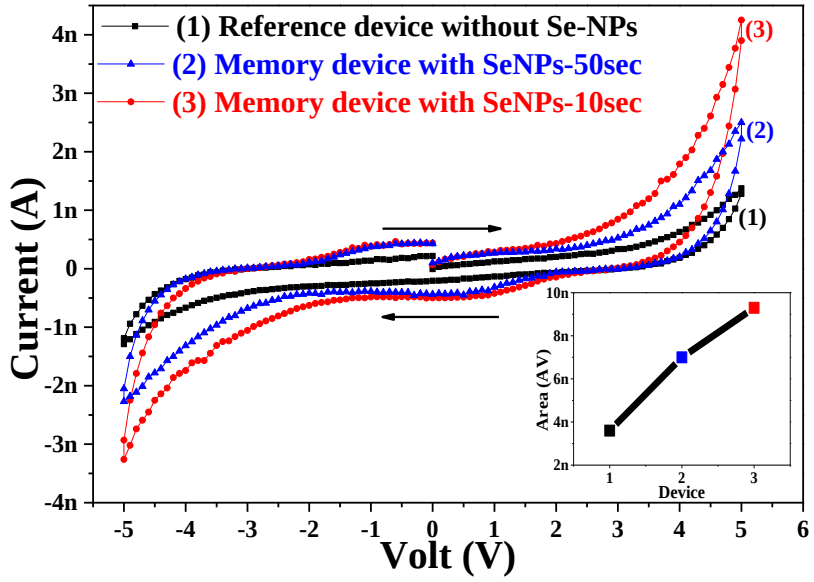

Fig- 12: I-V characteristics of reference device without Se-NPs (loop (1)), and 2T-NMDs with SeNPs-50sec (loop (2)) and 2T-NMDs with Se-NPs-10sec (loop (3)) on Flexible substrates. The inset shows the change in the area surrounded by the hysteresis loops Vs scan voltage, the maximum value of the area is observed for a memory containing SeNPs-10sec. The trend in the graph also suggests the charge storage in 2T-NMDs is relying on the size of nanoparticles.

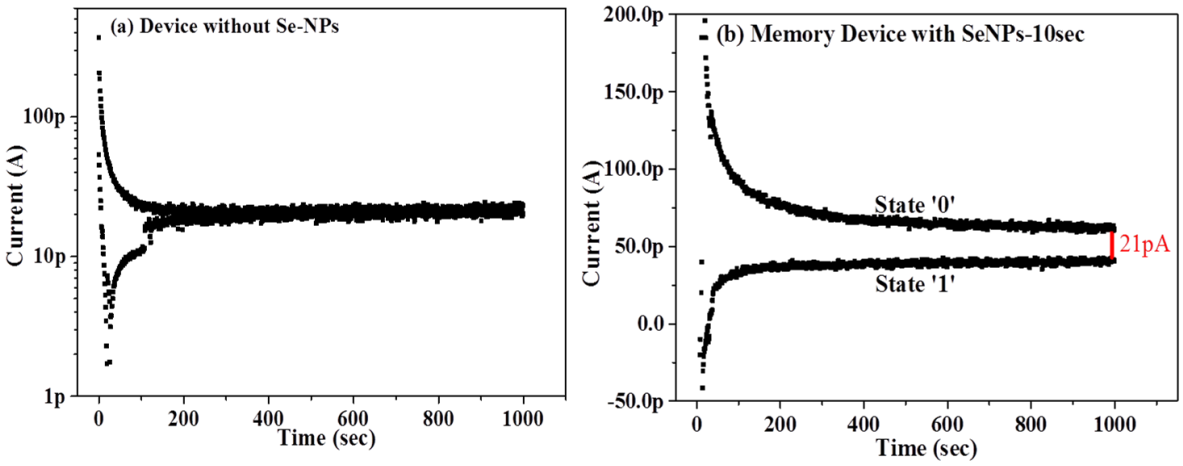

Fig-13: Graph of current Vs time to describe and understand charge retention of both conduction states, '0' and '1' in 2T-NMDs. (a) the two states collapse for the reference device without Se-NPs, and (b) the two states remain distinguishable around 21pA for 2T-NDMs containing SeNPs-10sec.