An Investigation of the Performance and Stability of Zinc Oxide Thin-film Transistors and the Role of High-k Dielectrics

PhD Thesis

De Montfort University

Ngwashi Divine Khan

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Author's Declaration

This thesis contains results of research undertaken by the author between January 2007 and June 2010 in the Emerging Technologies Research Centre (EMTERC), De Montfort University Leicester UK, under the initial supervision of Prof. M. M. De Souza and Dr. Luther Ngwendson and subsequently under the supervision of Dr. R. B. M. Cross and Dr. S. Paul.

This research is entirely my own original work and contains nothing done in collaboration except where explicit acknowledgement is given.

This work has not been submitted in whole or in part for any other degree or diploma.

Permission is granted to consult or copy the information contained herein for the purposes of private study but not for publication.

Ngwashi Divine Khan

Leicester, June 2010.

"Those who wish to succeed must ask the right preliminary Questions."

... Aristotle.

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Notations

Units

It is common in this field to use *the centimetre, the gram and the second* (C.G.S) units rather than the more conventional S.I. units. For compatibility with other published data, C.G.S units have therefore been adopted throughout this thesis.

References

References in the text are given in square brackets and the reader is directed to the list of relevant literature at the back of this thesis. The numerical value of each reference is determined by the order in which it appears in the text. Numerical values in curly brackets that are preceded by the symbol § direct the reader to sections of this dissertation. Numbers in round brackets refer to equations and reactions listed in the text.

Abbreviations

All abbreviations used in the text are written out in full at first occurrence, followed by the relevant abbreviation in round brackets.

Keywords

Reactive sputtering, Zinc oxide (ZnO), Thin film Transistor (TFT), Performance, Stability, High-k dielectrics, Metal-organic chemical vapour deposition (MOCVD), Vienna ab initio simulation package (VASP), Oxygen adsorption.

Abstract

Transparent oxide semiconducting films have continued to receive considerable attention, from a fundamental and application-based point of view, primarily because of their useful fundamental properties. Of particular interest is zinc oxide (ZnO), an n-type semiconductor that exhibits excellent optical, electrical, catalytic and gas-sensing properties, and has many applications in various fields. In this work, thin film transistor (TFT) arrays based on ZnO have been prepared by reactive radio frequency (RF) magnetron sputtering. Prior to the TFT fabrication, ZnO layers were sputtered on to glass and silicon substrates, and the deposition parameters optimised for electrical resistivities suitable for TFT applications. The sputtering process was carried out at room temperature with no intentional heating. The aim of this work is to prepare ZnO thin films with stable semiconducting electrical properties to be used as the active channel in TFTs; and to understand the role of intrinsic point defects in device performance and stability. The effect of oxygen (O_2) adsorption on TFT device characteristics is also investigated.

The structural quality of the material (defect type and concentration), electrical and optical properties (transmission/absorption) of semiconductor materials are usually closely correlated. Using the Vienna ab-initio simulation package (VASP), it is predicted that O_2 adsorption may influence film transport properties only within a few atomic layers beneath the adsorption site. These findings were exploited to deposit thin films that are relatively stable in atmospheric ambient with improved TFT applications. TFTs incorporating the optimised layer were fabricated and demonstrated very

impressive performance metrics, with effective channel mobilities as high as 30 $cm^2/V^{-1}s^{-1}$, on-off current ratios of 10^7 and sub-threshold slopes of 0.9 – 3.2 V/dec. These were found to be dependent on film thickness (~15 – 60 nm) and the underlying dielectric (silicon dioxide (SiO_2), gadolinium oxide (Gd_2O_3), yttrium oxide (Y_2O_3) and hafnium oxide (HfO_2)).

In this work, prior to sputtering the ZnO layer (using a ZnO target of 99.999 % purity), the sputtering chamber was evacuated to a base pressure ~4 x 10^{-6} Torr. Oxygen (O_2) and argon (Ar) gas (with O_2/Ar ratio of varying proportions) were then pumped into the chamber and the deposition process optimised by varying the RF power between 25 and 500 W and the O_2/Ar ratio between 0.010 to 0.375. A two-level factorial design technique was implemented to test specific parameter combinations (i.e. RF power and O_2/Ar ratio) and then statistical analysis was utilised to map out the responses.

The ZnO films were sputtered on glass and silicon substrates for transparency and resistivity measurements, and TFT fabrication respectively. For TFT device fabrication, ZnO films were deposited onto thermally-grown silicon dioxide (SiO_2) or a high-k dielectric layer (HfO_2, Gd_2O_3 and Y_2O_3) deposited by a metal-organic chemical deposition (MOCVD) process.

Also, by using ab initio simulation as implemented in the "Vienna ab initio simulation package (VASP)", the role of oxygen adsorption on the electrical stability of ZnO thin film is also investigated. The results indicate that O_2 adsorption on ZnO layers could modify both the electronic density of states in the vicinity of the Fermi level and the band gap of the film. This study is complemented by studying the effects of low

temperature annealing in air on the properties of ZnO films. It is speculated that O_2 adsorption/desorption at low temperatures (150 – 350 ^{0}C) induces variations in the electrical resistance, band gap and Urbach energy of the film, consistent with the trends predicted from DFT results.

Peer Reviewed Published Work and Conference Presentations

1. D.K. Ngwashi, R. B. M. Cross S. Paul, A. P. Milanov and A. Devi, "*High Performance ZnO Thin Film Transistors Using Novel High-k Dielectrics* ", Mat. Res. Soc. Symp., Fall Meeting (**2010**) (Submitted).

2. D. K. Ngwashi and R. B. M. Cross, '*'Ab initio investigation of oxygen adsorption on the stability of carbon nanotube field effect transistors (CNTFETs)*'', (**2010**) 150 (5 - 6) 258 – 261 Solid State Communications.

3. A. P. Milanov, T. Toader, H. Parala, D. Barreca, A. Gasparotto, C. Bock, H.-W. Becker, D. K. Ngwashi, R. Cross, S. Paul, U. Kunze, R. A. Fischer, A. Devi, *Lanthanide Oxide Thin Films by Metalorganic Chemical Vapour Deposition Employing Volatile Guanidinate Precursors, Chem. Mater.* **2009**, *21*, 5443

4. A. P. Milanov, T. Thiede, M. Hellwig, H. Parala, C. Bock, H.-W. Becker, D. K. Ngwashi, R. B. M. Cross, S. Paul, U. Kunze, R. A. Fischer, A. Devi, *Rare-earth based oxide and nitride thin films employing volatile homoleptic guanidinate precursors*, *ECS Transactions* (**2009**), *25*, 143

5. Divine Ngwashi, R. B. M. Cross and S. Paul, "*Electrically air-stable ZnO thin film produced by reactive RF magnetron sputtering for thin film transistors applications*", Mat. Res. Soc. Symp., Fall Meeting (**2009**) 1201- H05 - 32.

6. M. M. De Souza and R. B. M. Cross, D. Ngwashi, S. Jejurikar and K. P. Adhi "*Performance and Stability of ZnO TFTs with SiO_2, SiN and AlN Insulators*'', orally presented at *Mat. Res. Soc. Symp., Fall meeting* (**2007**).

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Chapter - 1

Introduction

"The best way to have a good idea is to have lots of ideas."

... Linus Pauling

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) are currently the most commercially used TFTs in large area electronics applications such as active matrix liquid crystal displays (AMLCDs) and other flat panel display (FPD) applications. However, the low effective mobility (~1 $cm^2V^{-1}s^{-1}$) and the high photo-induced instability in a-Si:H TFTs [1] remain key issues limiting their applicability. Poly-silicon TFTs, which have higher mobility and less photo-induced related instability, were first developed by using conventional integrated circuit (IC) processes (that require high temperatures) , using poly-silicon deposited by low pressure chemical vapour deposition (LPCVD) at temperatures as high as 900 - 1000°C. Although modified processes are constantly being investigated by different researchers for low temperature applications [2-7], the challenge for realising near-room temperature large area electronics remains. As a consequence of this, wide bandgap semiconducting oxides (including zinc oxide (ZnO)) are currently being investigated intensively for TFT applications.

There has been a growing interest in using ZnO as a new material for TFT applications the world over within the last decade [8, 9], leading to drastic improvements in ZnO TFT performance and the general understanding of ZnO thin films. Figure 1.1 demonstrates a flat panel display (FPD) screen driven by a ZnO TFT matrix [8].

Figure 1.1 - A 1.46´´ ZnO TFT driven LCD with improved picture and defect quality, demonstration from [8].

Transparent ZnO TFTs were first demonstrated in 2003 via the works of Nomura, Masuda, Hoffman, and Carcia [10-13]. Following this demonstration, considerable advances in the scientific understanding of the properties of ZnO thin films and their technological applications have been made. ZnO TFTs are already seen as a potential alternative to the currently-used a-Si:H TFT as a select transistor for active matrix liquid crystal display (AMLCDs) technology (a select transistor is used to choose a pixel so that information can be supplied to that pixel); This is due to their

high optical transparency in the visible region, high effective channel mobility (~12 $cm^2V^{-1}s^{-1}$, compared to < 1 $cm^2V^{-1}s^{-1}$ for a-Si:H produced under similar conditions [14]) and the possibility of low (room) temperature processing compared to temperatures of ~250 - 350 ^{0}C required for a-Si:H.

The high mobility observed in ZnO TFTs has been ascribed to the fact that ZnO is an ionic semiconductor and usually occurs in a polycrystalline form (the effect of localised states on charge carriers is thus small) [15, 16]. Martins et al. found that structural order has minimal effect on the mobility in such materials, as almost all induced charges remain delocalised and would participate in conduction [17]. They even reported a higher mobility in indium-doped amorphous ZnO TFT than in polycrystalline ZnO TFTs produced under similar conditions [17].

Some of the physical properties of ZnO that makes it particularly attractive for electronic devices are summarised in table 1.1, (extracted from a review on ZnO by Pearton [18]).

Table 1.1 - Properties of wurtzite ZnO [18].

Lattice parameters at 300 K	
a	0.32495 nm
c	0.52069 nm
c/a	1.602 (ideal hexagonal structure shows 1.633)
u	0.345
Density (gcm^{-3})	5.606
Stable phase at 300 K	Wurtzite
Melting point (^{0}C)	1975
Static dielectric constant	8.656
Refractive index	2.008
Energy gap	~ 3.4 eV, direct
Intrinsic carrier	concentration : max n-type doping ~ 10^{20} cm^{-3}; max p-type doping ~ 10^{17} cm^{-3}
Exciton binding energy	60 meV, sufficiently larger than thermal energy at room temperature (~26 meV).
Electron effective mass	0.24
Electron Hall mobility at 300 K for lightly doped n-type ZnO	200 cm^2V^{-1} s^{-1}
Hole effective mass	0.59
Hole Hall mobility at 300 K for lightly doped p-type ZnO	5–50 cm^2V^{-1} s^{-1}

One of the main benefits of ZnO is that good quality films can be deposited at/near room temperature. In addition, ZnO has a wide bandgap (~ 3.4 eV), high transparency to visible light and TFTs utilising ZnO as a channel material have demonstrated high channel mobilities compared to that of conventional a-Si:H and organic based TFTs [11, 13], which have also been seen as an attractive alternative. Furthermore, ZnO is more resistant to radiation damage compared to other common semiconductor materials, such as, silicon (Si), gallium nitride (GaN), cadmium sulphite

(CdS), and gallium arsenide (GaAs) [19] due to its strong ionic properties. ZnO TFTs, therefore, offer a way to overcome the mobility issue with improved device stability to light using low temperature processes. These transistors have also been found to exhibit high channel electron mobility, which would lead to higher drive currents and faster device operating speeds (required for high frequency applications and as driving transistors in light emitting diode displays) [20-24].

Carrier mobility in ZnO channel layers deposited at/near room temperatures has often been found to increase with post-deposition treatments such as post-thermal annealing. This has been attributed to increases in the film crystallites size and a reduction in grain boundary density. In this work, different dielectric layers have been investigated in part as an alternative method for tuning carrier transport via different ZnO/dielectric interfaces and the fact that growth of ZnO films is influenced by the underlying dielectric. It is also hoped that by integrating high-k dielectrics into the fabrication process, low operational input voltages may be achieved with two main consequences: 1) the gate field at the ZnO/dielectric interface will be reduced, and 2) the electric field-induced gate leakage current will be reduced. The fact that high-k dielectrics result in TFTs with low gate fields at the ZnO/dielectric interface offers a means to modulate instability issues resulting from prolonged gate bias stressing. This has been investigated in detail in chapter 6 and 7.

Layers of ZnO thin films can be deposited by a number of different methods such as: atomic layer deposition (ALD), chemical vapour deposition (CVD), molecular beam epitaxy (MBE), pulse laser deposition (PLD), electrophoretic deposition (EPD), and RF (or direct current (DC)) sputtering [13, 25-29]. One of the most commonly-used and effective methods, that has produced excellent films (dense and

crystallographically-oriented) at temperatures close to room temperature, is the RF magnetron sputtering technique. This is partly due to the simplicity of the RF magnetron sputtering technique, easy parameter control and film reproducibility together with the fact that films can be sputtered over large areas on a variety of substrate materials. Sputtered ZnO films have been used as transparent conducting electrodes in photo-voltaic applications, organic light emitting diodes (OLEDs), active channels in TFTs, resistive elements in heated mirrors and glasses, smart windows and as chemical/biological or gas sensors [20, 30-36].

The main disadvantage associated with the sputtering process is the stringent requirement of high-vacuum equipment. In addition, inert gases used in the sputtering system are often trapped in the growing film as impurities. Also, it is difficult to prevent target material diffusion into pre-existing substrate layers and underneath shadow masks.

Irrespective of the deposition process, ZnO growth suffers from asymmetric doping; p-type ZnO films have been difficult to obtain, whereas n-type films are easily produced. However, with a few reports of p-type films emerging (although most of them still suffer from instability and repeatability issues), it may be possible for all-ZnO light emitting diodes (LEDs) to be realised in the future [37, 38].

1.1 Objectives and Methodology

Despite the fact that n-type ZnO can be produced with relative ease, its use in TFT device applications is often hindered by a large concentration of background electrons and the electrical instability of ZnO films in ambient environments. Although

near room temperature processes have been reported to have produced TFT devices with enhanced performance over that of a-Si:H produced under similar conditions, reliability and instability have remained challenging issues [39-41]. In particular, the electrical properties of ZnO degrade greatly with time in oxidising environments including ambient air [39, 42-47]. One solution to this has been the use of suitable passivation layers [48]. However, this extra additional layer not only increases the production cost but can also reduce the film transparency.

It is hoped that suitable optimisation of the ZnO layer deposition parameters together with a post-ageing step in an oxygen environment could directly address these issues and produce electrically air-stable ZnO layers. All ZnO thin films studied in this work were post-treated with oxygen (0.2 mTorr) for one hour immediately after sputtering prior to breaking the vacuum in order to minimise the dependence of electrical properties of films on exposure to air.

The results of x-ray diffraction (XRD) investigations reveal that all films sputtered were predominantly c-axis oriented. The effect of oxygen (O_2) adsorption on the (0001) ZnO surface was then studied in order to understand the contribution of O_2 on the electrical properties of the films. This was achieved theoretically using the Vienna ab initio simulation package (VASP). An experimental approach was also performed by studying the influence of O_2 desorption on the film properties via low temperature (150 – 350 ^{0}C) annealing in air.

In this work, the main interest in the study of ZnO thin films, in part, is to increase understanding of the effects of intrinsic point defects, such as oxygen vacancies and zinc interstitials, on the electrical properties of ZnO films. This is achieved via the

modulation of the O_2 flow rate in the reactive sputtering system. By studying the electrical and optical properties of the deposited films, the effects of oxygen vacancies and/or zinc interstitials could be observed. This understanding is then exploited as a means of defect control to tune, characterise and fabricate high performance, and electrically-stable ZnO TFTs. Furthermore, an attempt is made to integrate high-k dielectrics into ZnO TFT structures with an aim to produce ZnO TFTs with improved performance as a result of an increased coupling of the gate capacitance with the active channel charge; this enhances the density of charge induced in the channel. In addition, high-k dielectrics integration is also investigated for ZnO TFT gate bias stability. SiO_2 (control dielectric) is also used and studies relating to the performance and stability related issues of TFTs incorporating different gate insulators are compared and discussed.

1.2 Thesis Structure

The thesis is organised as follows:

- Chapter 2 gives an insight into the electronic and crystal structure of ZnO and oxide semiconductors in general. The doping mechanism and the role of defects on the performance of oxide semiconductor-based electronic devices are presented.

- Chapter 3 presents a brief description of some of the commonly-used techniques for depositing and characterising thin films. A description of film deposition by

sputtering, which is the technique used to deposited ZnO semiconducting films used in this work, is also presented.

- Chapter 4 describes the effects of oxygen vacancies and/or O_2 adsorption on the (001) ZnO surface on its electronic properties using computer simulations. In these studies, the density functional theory (DFT) as implemented in VASP was used. The results presented are further demonstrated experimentally by studying the effects of O_2 desorption on the electrical properties of ZnO films. O_2 adsorption on ZnO surface is then exploited throughout this work as a means to improve film stability in air.

- Chapter 5 presents high-k dielectrics and their role in microelectronics field effect devices. The results of the ZnO thin film optimisation for TFT applications are also presented.

- Chapter 6 presents the TFT structure, fabrication and characterisation processes used to produce the ZnO TFT test devices used in this work. The ZnO thin film is optimised for thickness and performance using TFT structures incorporating SiO_2. The optimised film thickness is then used for performance and bias stress stability studies across different high-k dielectrics.

- Chapter 7 presents and discusses the results of ZnO TFT performance and gate bias stress instability, while chapter 8 concludes the thesis and proposes future work for continuation of the research.

Chapter – 2

The Structure and Electronic Properties of Zinc Oxide

An overview of ZnO and its applications

2.1 Introduction

ZnO occurs naturally as the mineral zincite. However, most ZnO used commercially is synthetically produced. ZnO is widely used as an additive in a variety of applications including ceramics, plastics, cement, glasses, lubricants, paints, pigments, and ointments. Recently, due to its semiconducting properties, ZnO has been very attractive to researchers as an emerging material for electronics applications. In this chapter, a brief review of the structural and electronic properties of ZnO thin films relevant to its microelectronics applications is presented.

From the theory of crystalline solids, the periodicity of atomic nuclei in solids leads to the separation of the energy levels into bands. An introduction of defects and/or impurities in the crystalline network results in symmetry breakdown and consequently different band structures that would give rise to different electrical and/or optical properties. The purpose of this chapter is to summarise the generally-accepted model for the structure of polycrystalline ZnO (a group II-VI semiconductor), the role of native point defects (mainly zinc interstitials and oxygen vacancies), and hydrogen impurities, and to review the general electronic properties of ZnO thin films. Furthermore, the

density of states (DOS) and the role of defects on the electronic transport in ionic oxide semiconductors are discussed.

2.2 The Structure and Electronic Properties of ZnO

The most stable structure of ZnO is the hexagonal wurtzite (figure 2.1) (C_{6v} point group symmetry with a = 3.2476 Å and c = 5.3033 Å), with c-axis orientation predominantly observed in ZnO films synthesised by a number of different processes [49-52]. The zinc (Zn) atoms are tetrahedrally co-ordinated to four oxygen (O) atoms, with the O anions occupying the octahedral sites. Unlike amorphous semiconductors, such as a-Si:H, ZnO thin films are generally n-type polycrystalline ionic oxide semiconductors [53].

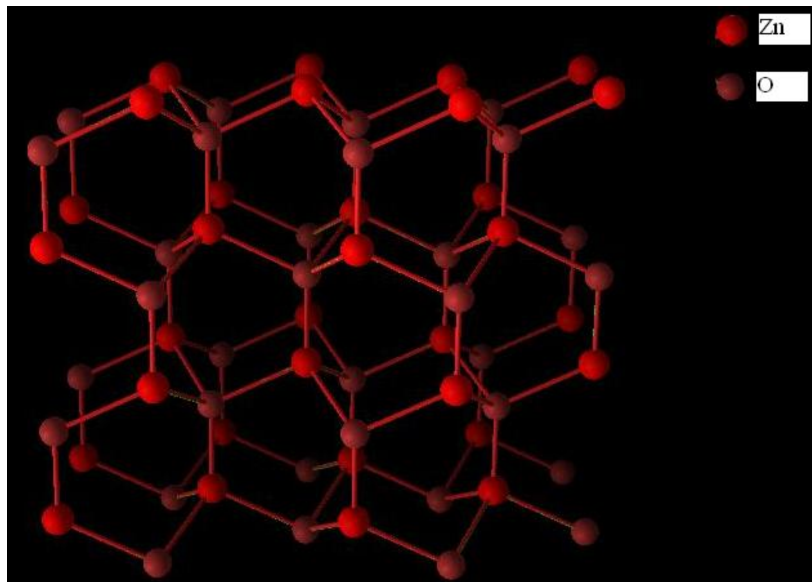


Figure 2.1 - Hexagonal wurtzite structure of bulk ZnO

The dominating n-type character in ZnO has often been attributed to the presence of intrinsic native defects (O vacancies (V_O) and/or Zn interstitials (Zn_i)). However, there is still a great deal of controversy over which of these two defects is the dominant cause of the n-type character [54]. Some researchers have suggested that V_O are deep-level states [55-58] and are therefore not likely to be the dominant cause of n-doping in un-intentionally-doped ZnO films. Hydrogen is usually considered the main cause of n-type doping in undoped ZnO films [59-62]. In this thesis, it is observed that the n-type doping in ZnO is influenced by V_O and hydrogen (chapters 4 and 7).

The strong ionicity in ZnO imposes higher ordering as every ion is surrounded by ions of opposite polarity. ZnO therefore exhibits a pronounced metallic s-like conduction band (CB) minimum and a valence band (VB) maximum of O2p states [63]. The CB minimum is mainly localised on the 4s Zn-states and its energy is independent of the interaction between the metal 4s states and the O2p states and only depends on the metal-metal second neighbour distance. Heavy metal cations with overlapping orbitals ensure that charge carriers remain delocalised, so that any disorder may only pose a second order effect on the carrier mobility [17]. Thus, the introduction of any disorder in ZnO has a negligible effect on the carrier transport.

The lack of localized states close to the CB edge in ionic oxides allows the Fermi level to move well into the bottom of the CB; thus, degenerate doping is possible to attain (as in figure 2.2 left), where the arrows (figure 2.2 right) indicate the existence of states at the band edges in amorphous materials. This has the effect of pinning the Fermi level around the band edges. Degenerate doping is an important requirement for applications where ZnO is used as a transparent conducting electrode. Furthermore, due

to the high transparency of ionic oxide semiconductors, '*light-induced defect state creation instability*', a common problem in a-Si:H [64-70], is expected to be relatively small in ionic oxides.

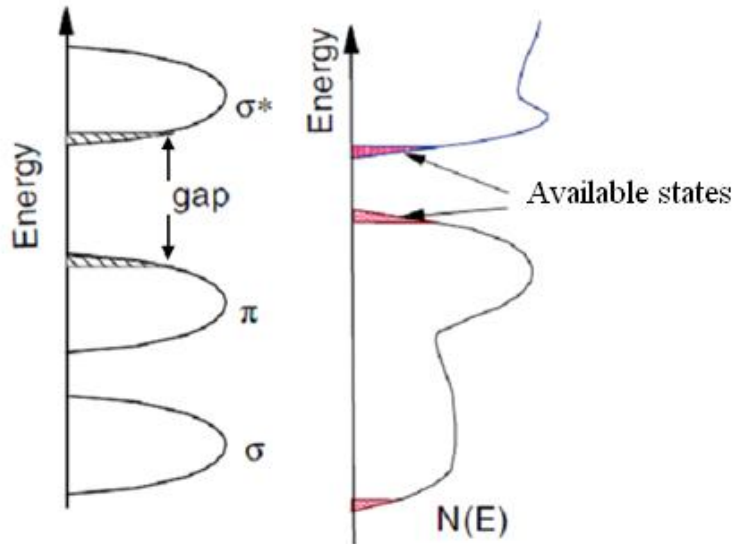


Figure 2.2 - Density of states of a disordered ionic oxide (left), and the density of states of amorphous silicon (right) [71].

2.2.1 The Role of Defects on the Electronic Properties of ZnO

The n-type character of as-grown ZnO has often been attributed to V_O and Zn_i within the ZnO network. The reactions for creating excess electron carriers can be expressed as in equation (2.1); for V_O and Zn_i respectively.

– ……………………...…………………………..….... (2.1a)

– …………………………………….………...….. (2.1b)

The Zn_i occurs as a shallow donor (~25 – 30 meV) while the V_O is a relatively deep level donor [72, 73] and is likely to be the dominant compensator in p-type ZnO [74]. However, the formation energy of Zn_i has been reported to be high and so it is not expected to be the dominant cause of the background donor concentrations ($10^{15} – 10^{16}$ cm^{-3}) often observed in as-grown, undoped ZnO [74]. It is therefore predicted that Zn_i is likely to occur mainly in the form of complexes that involve low formation energies. On the other hand, Zn-deficient films with reduced Zn_i also favour the formation of Zn vacancies (V_{Zn}); which has been reported to be an important compensating acceptor dopant in n-type ZnO [55, 75, 76]. These controversies make it difficult to draw a definitive conclusion as to whether intrinsic point defects are the dominant contributor to the n-type character in undoped ZnO grown using a number of different techniques including: sol-gel, MOCVD, spray pyrolysis, sputtering, PLD, thermal evaporation, and spin-coating [31, 49-52, 77-81]. However, due to the low formation energy of V_O (in the 2+ state) compared to Zn_i [76, 82], they are assumed in this thesis to be influential in the observed n-type conduction in the sputtered ZnO films studied. As a consequence of the controversies associated to Zn_i, V_{Zn} or V_O in ZnO thin films, the need for optimising the deposition process in order to improve on the electronic properties becomes important.

2.2.2 Surface Roughness and Microstructure of ZnO thin Films

The electrical, optical and structural properties of ZnO thin films produced by a number of different techniques have been found to show a strong dependence on thickness [83-87]. The film crystallites sizes generally increase with film thickness. Furthermore, the deposition temperature and/or post-deposition annealing also influence

the crystallite size. As a consequence, the ZnO surface gets rougher and the concentration of grain boundaries in the film decrease with thickness. This is of relevance as carrier transport in ZnO is strongly influenced by charge trapping at the grain boundaries [88-92].

2.3 Thermal and Electrical Stability of ZnO

The most common II-VI semiconducting materials are ZnO, beryllium oxide (BeO), magnesium oxide (MgO), and cadmium oxide (CdO). Thermodynamically the ZnO and BeO materials crystallise in the wurtzite structure, while the MgO and CdO materials crystallise in a rocksalt structure. Thermodynamically, the wurtzite phase is the most stable ZnO phase at room temperatures, while the zincblende occurs as a metastable phase [93, 94]. The wurtzite phase has a very strong iconicity while the zincblende is more covalent with greater crystal symmetry. The conversion of zincblende phase domains to wurtzite and vice versa can be viewed as potentially possible [95]. Owing to the high structural symmetry of the zincblende phase, its carrier mobility is expected to be superior to that of the wurtzite phase with an experimental bandgap difference in the range 60 – 100 meV [93].

2.3.1 Influence of O_2 Adsorption at (0001) ZnO on Film Electrical Stability

The polar surfaces (0001) and ( ) (figure 2.1) of c-axis oriented ZnO are very reactive and unstable in oxidising environments [96, 97]. This results in the

electrical, structural and optical properties of ZnO films being strongly dependent on ageing in air and post-deposition procedures such as plasma and oxygen treatment and/or post-deposition annealing. The reactive surfaces make ZnO films electrically unstable in ambient atmosphere. As a result of this, electronic devices incorporating ZnO top layers often require the use of a suitable surface passivation technique [98]. There has been evidence that O_2 adsorption at the V_O site on the ZnO polar surfaces is the main cause of electrical instability in an ambient environment [97-104]. As such, there have been many reports from different researchers on the potential use of ZnO as an O_2 sensor [100, 105-110]. As a consequence, the main cause of instability of ZnO thin films in air and as suggested in this work has been attributed to O_2 adsorption on the film surfaces and/or at the grain boundary interfaces. The effect of this phenomenon on the electrical characteristics of TFT/material will be described in more detail in chapter 4.

2.4 Optical Properties of ZnO

The large optical bandgap (~3.4 eV) of ZnO makes ZnO thin films highly transparent to visible light (400 – 700 nm). Defects that affect film electrical properties such V_O, Zn_i and hydrogen incorporation are reported to also affect film transparency [111-115]. It is the deviation from stoichiometry as a result of the presence of these intrinsic native point defects that makes ZnO semiconducting.

The refractive index of thin films is often found to be closely related to the film density [116]. The relationship between the refractive index (n_f) and the corresponding packing fraction (P) of the film is given by (2.2);

— ———— ……………………………………………………….…………. (2.2)

where n_f and n_b are the refractive indices of the film and bulk ZnO material, and $_f$ and $_b$ are the densities of the film and bulk respectively.

The refractive index of single crystalline ZnO is ~2.008. Equation (2.2) suggests that denser films have higher refractive indices, and . Also, n is related to the film dielectric constant ε through equation (2.3).

…………………………………………………………………………… (2.3)

Ng et al [117] have found that the mobility of n-type GaN, another wide bandgap semiconductor, is dominated by dislocation scattering mobility (μ_{disl}), and could be described by;

—

———— ……………………………………………………….…. (2.4)

where, — is the Debye screening length, d the distance between acceptor centres, f the occupancy rate of the acceptor centres and N_{disl} is the concentration of dislocations. Thus, , so that the mobility of denser films are expected to show negligible dependence on dislocation scattering. As ZnO is generally deposited in the polycrystalline form, it often contains a large concentration of grain boundaries and other forms of dislocations. Films with high refractive indices, which are expected to give better mobility, also possess smooth surfaces as a consequence of their high

density and would produce better interfaces, which are all important conditions for TFT performance.

2.5 Doping in Oxide Semiconductors

Doping in semiconductors is often achieved by introducing a foreign atom into the semiconductor host material. For n-type semiconductors, delocalised electrons in the CB are majority charge carriers, whereas holes in the VB are majority carriers in p-type semiconductors. In metal-oxide semiconductors, e.g. ZnO, the presence of native point defects (V_O and/or metal interstitials) induce un-intentional n-type doping. Shallow donors (their energies lie in the upper half of the bandgap) and acceptors (their energies lie in the lower half of the bandgap) have much smaller ionisation energies compared to the bandgap energy of the host; hence, they greatly influence the electrical transport properties.

The resistivity of ZnO thin films has been reported to depend strongly on carrier concentration [118]. Many reports have also suggested other factors affecting the electrical properties of ZnO thin films, such as thickness, impurity distribution, grain size and grain boundaries; all of which have strong dependence on growth conditions [84, 85, 87, 119-127]. Therefore, the conductivity of films can be a measure of deviation from stoichiometry.

Recently, it has been demonstrated that hydrogen is a shallow level (~ 25 – 40 meV) donor [128-132] in ZnO, and so hydrogen can be considered as one of the dominant contributors to room temperature n-type conduction in ZnO [133-136]. Hydrogen incorporation in ZnO has also been suggested to improve electrical stability

in ZnO thin films, and improved performance in ZnO TFTs has been attributed to the passivation of interface states by hydrogen [23, 137-141]. In addition, background hydrogen from the underlying dielectric has been reported in a-Si:H layers deposited by PECVD [141, 142], and has been shown to be a useful route for improving performance in a-Si:H TFTs.

As a consequence of native point defects resulting from deviations from stoichiometry, as-deposited ZnO layers are normally intrinsically n-doped. In applications requiring degenerately doped ZnO layers, such as in transparent conducting electrodes, extrinsic doping becomes useful. In order to extrinsically dope ZnO n-type, Zn- or O-atoms are usually substituted with an atom that has one valence electron more than the atom it replaces. Thus, group III elements are potential shallow donors on Zn cations sites according to equation (2.5);

…………………………………………………………………….. (2.5)

D^0 and D^+ are the neutral and ionized donors, respectively and e is the electronic charge.

Recent reports have demonstrated that boron (B)-, aluminium (Al)-, gallium (Ga)-, indium (In)-, and fluorine (F)-doped ZnO films can be achieved [31, 51, 122, 143, 144], exhibiting both low resistivity and high transparency in the visible region. The high transmission in the visible region is often ascribed to the Burstein-Moss effects that arise as a consequence of degenerate doping, and so offers a means for modulating the optical bandgap [51, 77, 79, 80, 143, 144]:- a vital property of transparent electrodes. Once degenerate doping has been achieved, excess doping does

not move the Fermi level any further and only contributes to mobility degradation via impurity and grain boundary scattering (as excess metallic ions segregate into the grain boundaries and are not activated) [78]. It has been predicted that ionised impurity scattering is the major limitation to degenerate doping in oxide semiconductors, limiting the carrier concentration to below 2.0 x 10^{21} cm^{-3} [145, 146].

There has been much discussion concerning the difficulty involved in achieving p-type doping in ZnO [147, 148]. This is highly-desirable for the fabrication of light emitting diodes (LEDs) and complementary metal oxide semiconductor (CMOS) devices. From the discussion above, it could be expected that the substitution of a Zn cation site with group I elements (lithium (Li), sodium (Na), potassium (K), silver (Ag), and copper (Cu)) should result in the creation of acceptor states that would induce p-type conductivity [38, 149, 150] (equation 2.6).

……………………………………………………………………….. (2.6)

A^0 and A^- are the neutral and ionized acceptors, respectively, and h is the elementary charge of the hole.

This has however been difficult to achieve due to the large density of background compensating states and partly due to the fact that the acceptor states obtained by Zn-site substitution are usually deep levels at room temperature (with activation energies of a few hundred meV, much greater than k_BT at room temperature). In addition, excess impurity atoms occupying the interstitial sites will act as donors, compensating part of the acceptors and also inducing more disorder. As a consequence of these issues, attempts have been made to achieve p-type conductivity via substitution with group V

elements (N, P, As, and Sb) at the O-anion sites [147, 151]. Many reports indicate that this may be the only route to achieving p-type conductivity (although the carrier concentration is limited to less than 10^{18}), and N has been most promising in this regard (this maybe due to its close atomic radius to that of the O-atom) [38, 81, 152-156].

2.5.1 Thermal Activation Energy in ZnO Thin Films

It is known that to activate the electrical conductivity in n-type semiconductors, the donor levels must be ionised with at least a minimum energy equal to the energy difference $E_C - E_D$, where E_C represents the conduction band minimum and E_D the donor levels. ZnO generally contains deeper levels (traps), E_t, below the conduction band minimum: Major et al. [157] found that the electrical conductivity of such levels depends on the free carrier concentration, n, in the conduction band as in equation (2.7).

—— ………………………………………………………………... (2.7)

where, N_C is a function of doping level, the density of states in the conduction band, trap density and the grain size. If the temperature-activated mobility is not the dominant process [158], equation (2.7) can be used to calculate the activation energy. In this work, the activation energy was extracted from the semilog plot of the film electrical conductivity as a function of the measurement temperature T (figure 2.3). It is assumed here that the conductivity will follow the same relation as the carrier concentration (2.7).

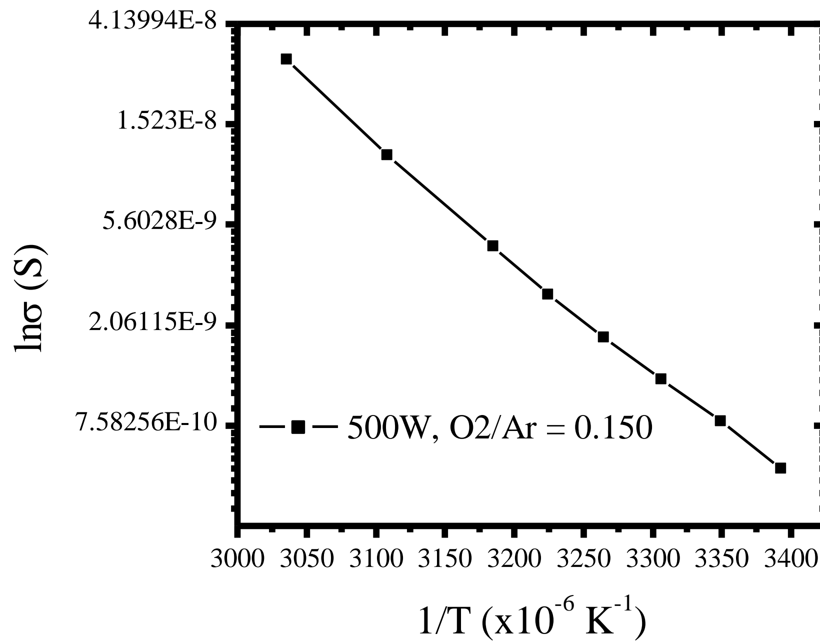


Figure 2.3 - Typical plot of the dependence of film resistivity on measurement temperature.

2.6 Summary

In this chapter, the structure of ZnO and the role of defects on the electrical properties of ZnO films is briefly discussed. The correlation between electronic properties and the optical properties is also examined. The role of intrinsic point defects on the electronic properties of ZnO is discussed. Extrinsic doping and the difficulty associated in achieving p-type conductivity in ZnO is also presented. In addition, the influence of atmospheric oxygen adsorption on the electrical stability of ZnO is highlighted.

Chapter – 3

Thin Films Preparation and Characterisation Techniques

3.1 Introduction

Thin films used in the semiconductor industry are deposited by a variety of techniques. In this chapter, the deposition techniques usually employed to deposit ZnO thin films and other films commonly used for microelectronics device fabrication (as in this thesis) are briefly presented, together with the electrical and physical characterisation techniques used. As the drive to reduce production costs and the desire to develop flexible, large-area electronics continues, the need for integrating cheap substrates (such as plastics) in the device fabrication process cannot be over emphasised. The low melting temperatures of plastics places a restraint on the device processing temperature. In the following sections, {§3.2 – 3.3}, some of the commonly-used thin-film deposition processes are discussed, with particular emphasis on the sputtering process as it has been used to deposit the ZnO semiconductor used in this work. The rest of the chapter is devoted to the physical and electrical characterisation techniques used to characterise the films used in this thesis.

3.2 Thermal Oxide

SiO_2 is one of the most commonly-used materials as a gate dielectric in field effect transistors (FETs). For these applications the oxide must fulfil the following

requirements: good structural integrity (stoichiometric and low defect levels), high dielectric strength, homogeneous thickness and low state density at the SiO_2/semiconductor interface.

The growth of SiO_2 by the thermal process often produces high-quality SiO_2 dielectrics. Thermally-grown oxide has higher integrity, better uniformity and dielectric strength, and is less defective as compared to oxides obtained using other methods such as CVD. High quality thermal oxide has a refractive index of about 1.462 (at a wavelength of 632 nm) and the process requires high temperatures (800 – 1200 ^{0}C) [159], and can be performed in one of two ways: - a *wet* or *dry* growth method in a furnace.

The wet method uses oxygen and hydrogen as precursors that have been mixed and heated to the required temperature in a separate furnace, and is frequently used to grow oxides that are much thicker than 100 nm. The O_2 reacts with H_2 in the wet process to form H_2O (g). Due to the strong dipole moment in the H_2O molecule, its diffusion rate in SiO_2 is enhanced over that of O_2.

The dry method uses only pure oxygen for the SiO_2 growth and denser films are obtained as the growth rate is slower, and often suitable for thinner films of ~100 nm in thickness or less (a consequence of the low diffusion rate of O_2 in SiO_2). During thermal oxide growth, oxygen diffuses through the native SiO_2 layer and the growth process occurs at the Si/SiO_2 interface via the reaction (3.1), so that it grows from bottom-up as shown by figure 3.1.

.... (3.1)

However, it has been reported that for the growth of very thin SiO_2, silicon transport from the underlying Si substrate to the O_2/SiO_2 interface becomes an important process [160, 161].

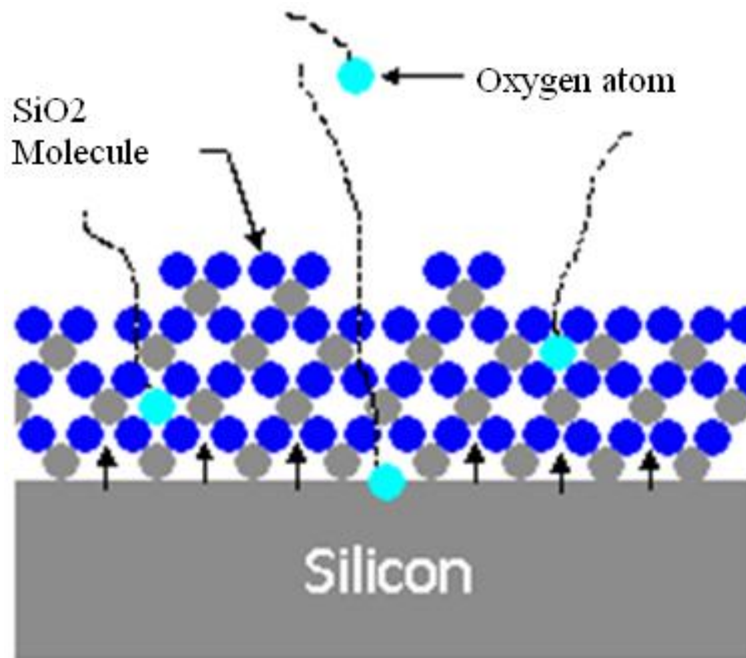


Figure 3.1 - A schematic of thermal oxide growth process, modified from [159].

In this work, the dry thermal growth method has been employed (mainly due to the fact that only 100 nm films were required and partly because the use of H_2 in a wet process would impose stringent storage requirements due to the explosive nature of H_2).

3.3 Chemical Vapour Deposition (CVD)

The chemical vapour deposition (CVD) technique uses gas phase sources to form thin films by chemical reactions on the substrate surface. When the source gases

are introduced into the reaction chamber, they diffuse to the substrate surface where the thin film is formed by a chemical reaction between the various gas atoms and the substrate. Some commonly used CVD techniques for thin film deposition include; plasma-enhanced chemical vapour deposition (PECVD) and metal-organic chemical vapour deposition (MOCVD). In the next sub-section {§ 3.3.1}, a brief discussion is presented on MOCVD as this has been used to deposit the high-k dielectrics studied in this work.

3.3.1 Metal-Organic Chemical Vapour Deposition (MOCVD)

The MOCVD process is a frequently-used technique utilised to deposit high-quality films (including ZnO) in the semiconductor industry [162-165]. This technique is similar to other CVD techniques, with the exception that the source gases are obtained from metal-organic precursors (figure 3.2). In this work, this technique has been used to deposit the high-k dielectric films (hafnium oxide (HfO_2), gadolinium oxide (Gd_2O_3) and yttrium oxide (Y_2O_3)) [166-169] used for the fabrication of ZnO TFT test structures. This has been in part to investigate how high-k dielectrics can be integrated in future ZnO TFTs and because the MOCVD technique, although not directly used in this work in the same way, is also compatible with large-area deposition, and has already been successfully employed to deposit ZnO films (at temperatures between 250 ^{0}C and 450 ^{0}C) [170-175]. Thus, the same deposition technique could be used for the deposition of both the insulator and the channel material in future ZnO TFT technology; it also offers an alternative route to investigating the integration of high-k dielectrics into oxide electronics. Although the MOCVD process

has been successfully used to produce ZnO TFTs with encouraging characteristics at relative low temperatures (200 – 450 ^{0}C) [171, 176], the sputtering process however, remains the deposition process of choice in this work due to its compatibility with room temperature deposition.

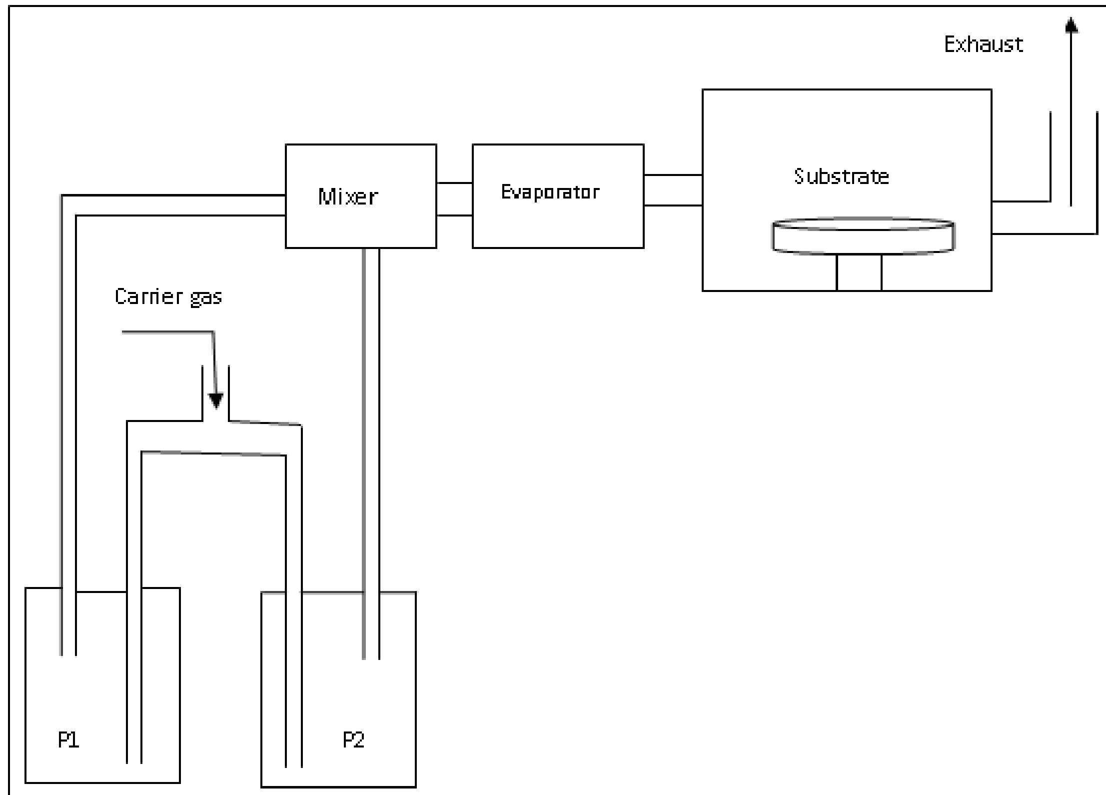


Figure 3.2 - Schematic diagram of a general scheme of metal-organic chemical vapour deposition (MOCVD) system; P1 and P2 are metal-organic based precursors and the carrier gas is usually nitrogen.

3.3.2 Physical Vapour Deposition (PVD).

The PVD technique involves the physical removal of atoms or molecules from the surface of a source material and the subsequent deposition of a solid material onto a

substrate. The physical removal of the materials is commonly-achieved through one of the following methods:

- *Evaporative deposition*: the material to be deposited is heated until a high vapour pressure is reached by an electrically resistive heating element. The thermal evaporation process is briefly discussed in the following sub-section {§ 3.3.3}.
- *Electron/ion beam evaporation*: the material to be deposited is heated until a high vapour pressure is reached by electron/ion bombardment in a "high" vacuum.
- *Sputter deposition*: a glow discharge (plasma) usually localised around the "target" by a series of magnets (as in a magnetron sputtering process) bombards the material, removing some of the target surface atoms away as a vapour {§ 3.3.4}.
- *Pulsed laser deposition*: a high power laser ablates material from the target surface into a vapour.

The atoms or molecules eroded are then transported through low pressure (to enhance their mean free path) onto the substrate surface where condensation takes place and the film is formed. Some commonly-used PVD techniques that have been employed to deposit ZnO on large-area substrates include: thermal evaporation [177-180], sputtering [181-191], electron beam evaporation (EBE) [192-198] and ion beam evaporation (IBE) [199, 200]. The main disadvantage of all PVD techniques is the stringent requirement of a vacuum system.

3.3.3 Thermal Evaporation

Thermal evaporation is achieved by electrically vapourising the solid source material in a high-vacuum environment using a heating element (usually tungsten (W) wire) where the vapour is allowed to condense on the substrate surface. The main drawback to this technique is the fact that it is not suitable for materials with very high melting points (resulting in *vapourisation* problems), and the possibility of cross-contamination from the heating filament or the crucible in which the source material is vapourised. The high melting point of ZnO ceramic (~1975 ^{0}C) means this technique is not suitable for ZnO deposition. In this work, all aluminium contacts used were thermally evaporated.

3.3.4 Sputtering

If a solid or liquid at any temperature is subjected to bombardment by suitably high energy particles (usually ions), it is possible for individual surface atoms to acquire enough energy via collision processes to escape. This means of causing ejection of atoms from a surface is known as '*sputtering*'. The incident ions lose their energy mainly by momentum transfer as they come to rest within the solid target. Thus, sputtering also leads to ion implantation into the lattice. In this process, the ions displace atoms within the sample, introducing some disorder and impurities. The incident projectiles need not be ions; as neutral beam bombardment causes sputtering also, but ions are frequently used due to their high yield (i.e. average number of atoms sputtered per incident primary ion; this, however, depends on the sample or target

material, its crystallographic orientation, and the nature, energy and incidence angle of the primary ions).

In this work, the ZnO thin films used have been produced by sputtering. For this reason, an extended introduction of the sputtering technique is presented in the remaining part of this section.

The sputtering technique often produces dense and crystallographically oriented films with good uniformity over large areas [201-208]. It is the easy parameter control coupled with the high deposition rate (although strongly dependent on parameter), that renders sputtering an attractive technique in semiconductor manufacturing where large-area deposition and/or mass production is desired. Furthermore, the 'spitting' issues suffered by high melting point materials in the thermal evaporation process are not encountered in sputtering.

The main disadvantages of sputtering deposition are: 1) the need for high vacuum equipment that increases production cost and 2) the introduction of defects by energetic particles as they are sputtered onto the pre-existing film. The latter becomes a serious issue especially when short source-to-target distances are used.

During the sputtering process, high energy particles (usually inert gas ions e.g. argon (Ar) ions as used in this work) are used to remove the surface atoms from a source material (called the '*target*'). In order to improve the mean free path of the sputtered atoms, purity and control of the sputtered atoms, sputtering is performed in a high-vacuum environment with a controlled injection of argon gas with a pressure between 0.1 mTorr and 10 mTorr [209]; this is sufficient to support the plasma (a mixture of ionised gas and electrons) between the two high-voltage electrodes (the

cathode and anode) in the chamber (as in a direct current (DC) sputtering process). In the case of RF sputtering, when the RF generator is turned on, an alternating electric field is created. In the first phase of the alternating voltage supply, the substrate is biased at a higher potential compared to the target which is at ground potential; any electrons in the chamber (present due to background radiation or due to electron emission from the target surface as a result of the large potential difference between the electrodes), are accelerated away from the target, towards the substrate electrode (which is at a higher potential, figure 3.3), colliding with the argon gas atoms on their way. The energy gained by the atoms from the collision causes excitation/ionisation, producing positive argon ions and additional electrons.

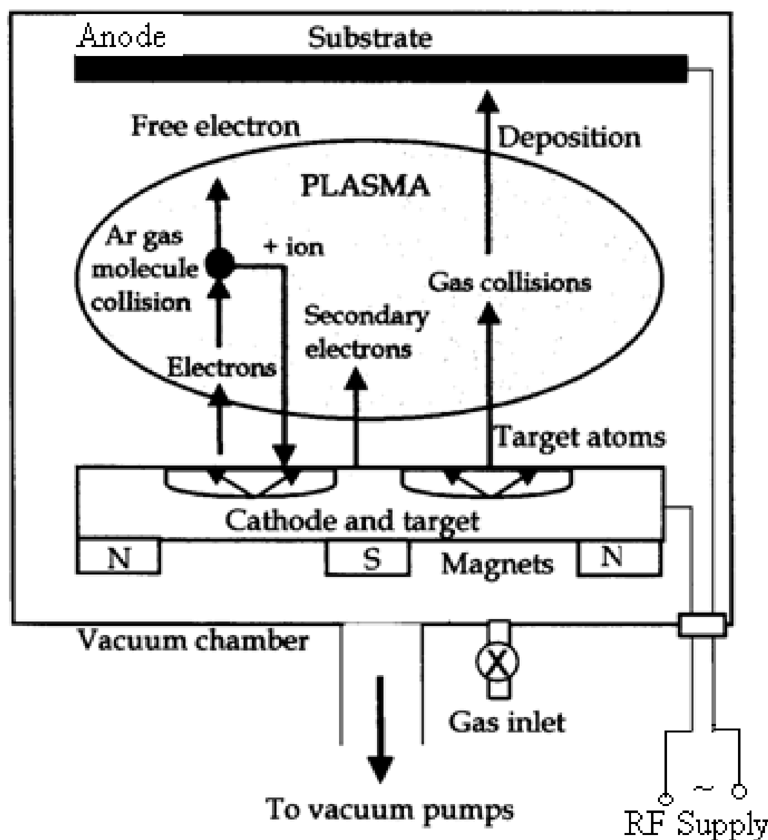


Figure 3.3 - RF Magnetron Sputtering process, modified from [209].

The excited atoms quickly decay back to their ground state by photon emission, resulting in the formation of a *glow discharge*. The positive Ar ions generated by gas ionisation are attracted towards the target where they collide with the target surface, knocking off material particles and generating electrons, (sputtering), while the secondary electrons generated in the process are again accelerated towards the substrate. This leads to more collisions and ionisation, hence the plasma is sustained. The impinging ion can either bounces-back, implants itself into the target, be adsorbed on the target surface or remove target surface ions. As the ions accumulate on the target surface, the target potential increases resulting to self-biasing, which hamper the further acceleration of ions towards the target. This is often a serious issue when an insulating target is used. The use of an RF supply (typically 13.56 MHz), however does not allow the heavy ions (ions only respond to an average electric field in the chamber) enough time to build up as a result of the quick potential reversal (and their large mass). This is because during the second phase of the RF supply when the target is at a higher potential relative to the substrate, no deposition takes place, but gas ions now move away from the target, hence minimising self-biasing (accumulation of ions on the target) which is a serious issue in DC sputtering of insulators (and semiconductors). As a consequence, RF Sputtering is a widely used deposition process, used to deposit films of both conducting and non-conducting materials of high quality [121, 210-215]. Sputtering yield is usually improved by use of magnetic fields, and this is referred to as *'magnetron sputtering'*.

- The magnetic field from the magnets beneath the target (figure 3.3) increases the path of the electrons in the plasma (as electrons perpendicular to magnetic field line follow an orbital path) and thus improves gas ionisation yield as the electron

collides with many more gas atoms. In addition, the magnetic fields trap electrons in the vicinity of the target; keeping electrons away from the substrate and hence reducing substrate heating and film damage by energetic electrons and also reducing the sputtering of atoms from the walls of the chamber, that could potentially contaminate the film.

- AC current in the RF range (13.56 MHz) applied to the target helps prevent charge accumulation on the target surface and enables the deposition of insulating films.
- Non-inert gases can also be introduced in the reaction chamber where they are ionised and made available for reaction at the substrate surface for film formation. This gives rise to the '*reactive sputtering'* process. Deposition parameter optimisation, and in particular the use of reactive sputtering, has been found to produce ZnO films with good thermal stability [94, 216]. If the target material is a good conductor, self-biasing can be neglected (even in DC sputtering) as the impacting ions are quickly redistributed and conducted away from the surface. In such a process, it is possible to use direct current (DC) sputtering, however, RF sputtering has been found to produce films of superior quality [211, 215]. In order to prevent the shorting of the conducting target to ground through the RF matching network, a blocking capacitor is often used.
- The main drawback in the use of magnetron sputtering is the fact that the target typically erodes in a *'racetrack'* fashion. This type of erosion produces a large amount of waste.

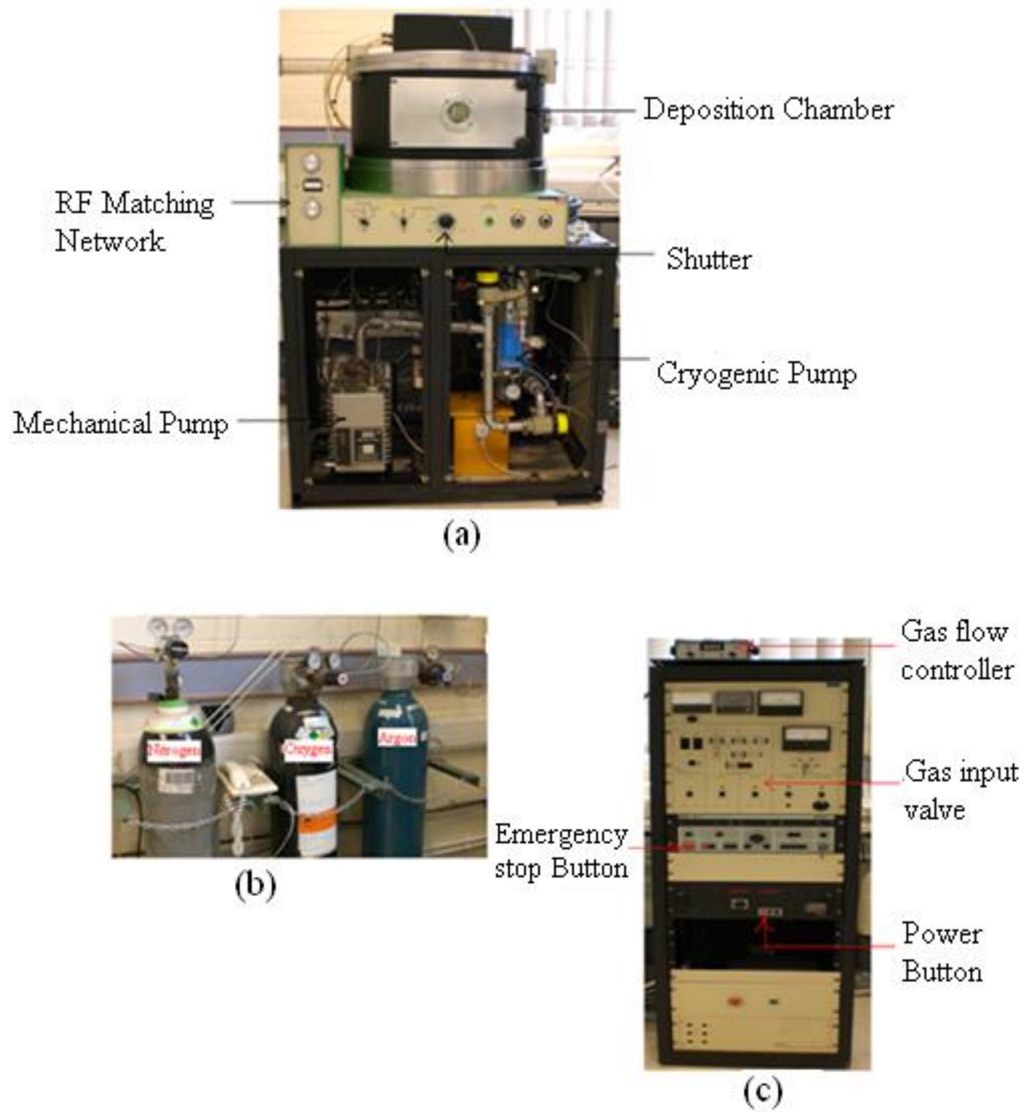


Figure 3.4 - Photograph of: a) Sputtering system, b) Gases used in this work (N_2, O_2, and Ar) and c) the electronic control rack.

3.3.4.1 Plasma Composition in a Sputtering System

For a reactive RF sputtering, as employed in this work, the introduction of O_2 into the reaction chamber results in a complex ion distribution. In order to initiate the sputtering process, a large negative potential difference is often required between the

target and the substrate electrodes, causing electron emission from the target surface. The ejected electrons accelerate through the potential, ionising gas atoms in the chamber through collision. Positive ions are accelerated towards the low potential (usually at ground potential) which is located behind the target. When these positive ions strike the target (ZnO), ionised particles, neutral particles (O- and Zn-atoms), secondary electrons and photons are emitted. The neutral atoms migrate to the substrate surface to form the film while the secondary electrons are used to generate more positive ions through increased ionisation and to keep the plasma running. A fraction of the O_2 gas in the chamber is also dissociated and ionised while some remains in molecular form. In this work, it is assumed that some of the oxygen atoms gain momentum from the Ar atoms to react with the molecular O_2 forming ozone O_3, which can also be ionised and form different complexes. Thus, the plasma is expected to be composed of O, O_2, O_3, Zn, secondary electrons and all the possible ionisation states. It is also suggested that the processes in equation (3.2) are likely to control the plasma composition for low RF power sputtering processes.

……………………………….………........……... (3.2a)

………………………..……………………......…….. (3.2b)

3.4 Post-deposition Oxygen (O_2) Treatment.

O_2 treatment of oxide semiconductors (and ZnO in particular) usually results in increased resistivity [46, 217-220]. This is usually attributed to the filling of oxygen vacancies at the surface of ZnO films or at the grain boundaries. This modulation of

film electrical properties is likely to have a strong influence on the threshold voltage (V_T) and the turn-on voltage (V_{On}) of oxide based TFTs. In addition, O_2 adsorption has been suggested to influence both structural and optical properties of ZnO thin-films [221].

In this work, as-deposited ZnO films were treated with O_2 at room temperature by exposing the films in an O_2 environment (0.2 mTorr) for one hour immediately after sputtering without breaking the vacuum. It is expected that the electrical properties of such films would be more stable in air as they will have less dependence on atmospheric O_2. The effects of O_2 adsorption on ZnO (0001) surface has been modelled and discussed in detail via density functional theory (DFT) in chapter 4.

3.4.1 Post-deposition Annealing

Post-deposition annealing is often employed to modulate the properties of semiconducting oxide thin films (including ZnO). For example, post-deposition annealing of ZnO in an inert ambient often increases the conductivity [222-227]. This is often attributed to the creation of oxygen vacancies in these oxides, as oxygen diffuses out of the films as a result of the annealing. ZnO thin films produced by a number of different methods have been reported to exhibit a strong re-crystallisation with post-deposition annealing at temperatures around 600 ^{0}C [224, 228-230]. For TFTs, post-deposition annealing of the channel layer may also influence the device performance as a result of the modulations of the active layer's electrical properties. The effects of low temperature post-deposition annealing on film properties and hence the device performance will be presented in chapter 4.

Post-deposition annealing of ZnO films studied in this work was achieved using a furnace (Carbolite) in air, in an effort to understand the influence of O_2 desorption from the ZnO surface and/or at the grain boundary interfaces {§ 4.8}.

3.5 Thin Film Characterisation Techniques

Thin films are often characterised using a number of different physical characterisation techniques. The techniques used in this thesis are briefly presented in this section {§ 3.5} under two main headings: - physical and electrical characterisations.

3.5.1 Physical Characterisation

3.5.1.1 Film Thickness Measurement by Ellipsometry

Ellipsometry is a simple, accurate, non-destructive and non-invasive measurement technique, frequently used for the determination of the refractive index (n) and thickness of thin films. Film thicknesses in this work were measured by an AutoEL-III ellipsometer equipped with a 633.2 nm helium-neon (HeNe) laser at an incident angle of 70^0. The evaluation of ellipsometry data depends on the (intensity-independent) ratios ( ) of the amplitudes and phases of the reflected and incident polarised light, and as such it is important that the material to be studied is non-absorbing at the laser wavelength. The thickness measurements were complemented by results obtained from surface profilometry using a Tencor Alpha Step 200 profilometer (vertical resolution of ±0.5 nm), in order to determine the correct order of measurement. For the surface profilometry measurements, a probe or stylus contacts the surface of the sample and

records height variations as it scans the surface. The height variations are converted into electrical signals that are used to generate a topographical map of the sample surface. These latter measurements required the creation of a sharp edge between the substrate and the film. In this work, the sharp edge was achieved using lift-up photo lithography on a section of film that had been patterned using photo-resist prior to the film deposition.

3.5.1.2 Structure Determination by X-Ray Diffraction (XRD)

Atoms of a pure solid are arranged in a regular periodic pattern called 'a *lattice'*. The inter-atomic distance and interaction of atoms in any crystalline lattice is unique and results in a unique X-ray diffraction (XRD) pattern to identify its crystal structure. When X-ray radiation with a wavelength, λ, is incident onto a crystal, a diffraction peak occurs if the Bragg criterion (3.3) for constructive interference is satisfied (the sharpness of this peak is a measure of the degree of ordering in the crystal):

.... (3.3)

where d is the inter-plane separation of the lattice, n = 0, 1, 2, ... is the interference order and θ is the angle of incidence as shown in figure 3.5. In this work, a Siemens/Bruker D5000 diffractometer equipped with a copper target (CuKα) was used to generate the incident X-rays of wavelength = 0.1540562 nm for the diffraction measurement. All films were deposited on lightly-doped p-type silicon substrates. From the XRD pattern, the average crystallite size τ could be calculated using the Scherrer's formula (3.4);

——— .... (3.4)

Where is the full width at half maximum (FWHM) of the peak of interest at 2θ (in radians), κ = 0.9, is the shape factor of the average crystallite and θ is the Bragg angle (figure 3.5).

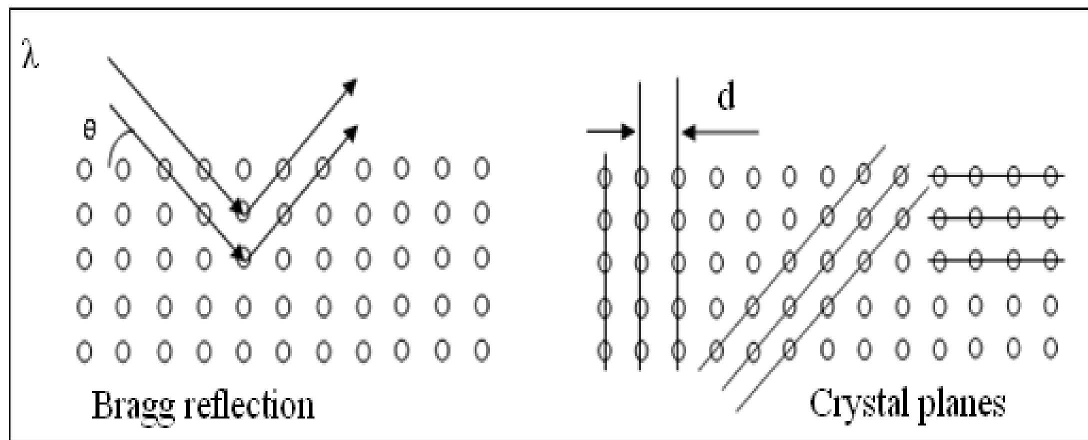


Figure 3.5 - Illustration of Bragg reflection and Crystal planes

3.5.1.2.1 Crystal Structure of Sputtered ZnO

ZnO films deposited by magnetron sputtering have been reported to possess varying degrees of crystallinity and are predominantly c-axis oriented, i.e. their preferred growth direction is normal to the substrate surface. As expected, our films deposited by reactive RF magnetron sputtering are also predominantly c-axis oriented and the crystallinity and film orientation are affected by the ratio of O_2/Ar (figure 3.6) [231]. For the purpose of TFT applications, film growth along other crystallographic

planes would be important, as it could lead to reduced grain boundary density along the channel leading to improved charge percolation in the channel region.

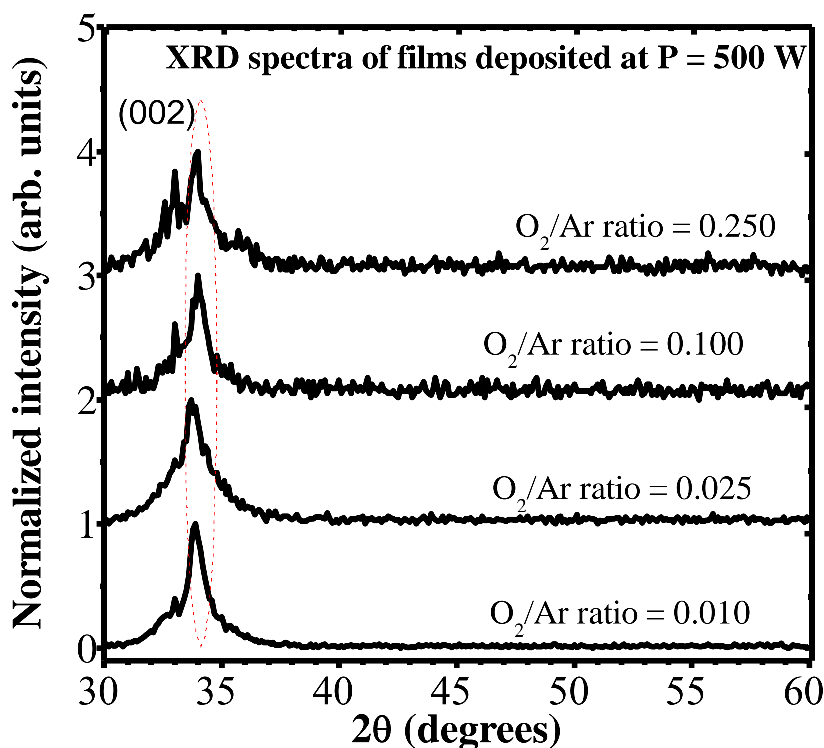


Figure 3.6 – X-ray diffraction (XRD) of a reactive magnetron sputtered ZnO films.

3.5.1.3 Surface Morphology by Atomic Force Microscopy

The Atomic force microscopy (AFM) is a very high-resolution technique (resolution down to approximately 1 nm or less). Hence, the AFM is also a very useful tool for manipulating matter at the nanoscale. An atomic force microscope (AFMc) consists of a cantilever with a sharp tip (*probe*) at its end that is used to scan the sample surface. When the tip is brought into proximity with a sample surface, the interaction of forces between the atoms of the tip and the surface atoms of the sample lead to a

deflection of the cantilever. The deflection force varies across the sample surface as it is scanned depending on the gap between the tip and the sample surface. Typically, the deflection is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes (position sensitive detectors (PSDs)). Two scanning modes are commonly used in AFM measurements; the contact mode and the non-contact mode. In the contact mode, the tip is in a physical contact with the sample surface and operating in the region where the resultant interaction (U) between the tip and the sample is in the repulsive regime (figure 3.7). The main disadvantage of the contact mode is the possibility of damaging the sample surface and degrading the tip as the cantilever drags across the surface.

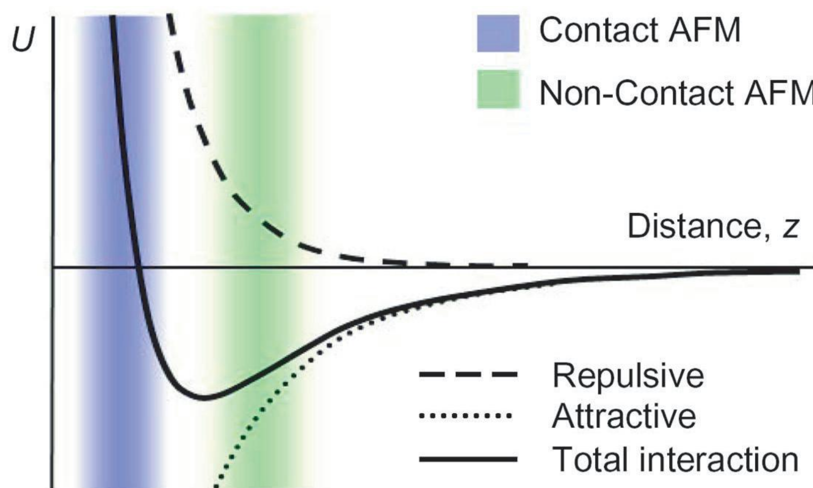


Figure 3.7 - Interaction between AFM tip and sample surface versus separation.

In this work, the non-contact mode has been used throughout. The non-contact mode operates in the region where the resultant interaction is dominated by attractive forces (figure 3.7). If the tip is scanned at a constant height, there would be a risk that

the tip may collide with the surface causing damage to both the tip and the material in question; hence, in most equipment (including the Park XE-100 system used in this work) a feedback mechanism is employed to adjust the tip-to-sample surface distance to maintain a constant force between the tip and the sample. Traditionally, the sample is mounted on a piezoelectric tube that can move the sample in the *z*-direction for maintaining a constant force, and the *x* and *y* directions for scanning the sample. The resulting surface profile of the area *s bounded by x and y* represents the topography of the sample. In this work, the AFM was used to analyse the surface morphology (surface roughness and to predict trends in grain boundaries) of the sputtered ZnO films. Figure 3.8 shows a typical AFM image of a sputtered ZnO film deposited in this work.

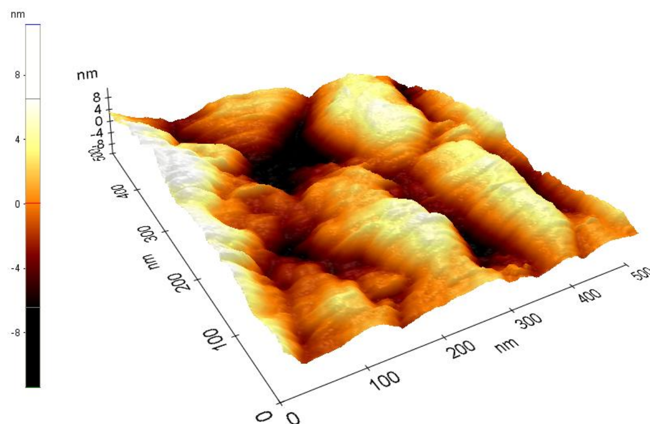


Figure 3.8 - Typical AFM image of a 40 nm thick ZnO film sputtered on a layer of HfO_2, deposited by MOCVD.

3.5.1.4 UV-Vis Absorption Spectroscopy

Ultra-violet to visible (UV-Vis) spectroscopy has been employed for the determination of optical transmittance measurements of all films used in this work and

from this extraction of bandgap data. A UNICAM-UV/VIS (UV 2) single beam spectrometer was used within a scanning range of 200 – 900 nm. Films studied were either deposited on corning 7059 glass or soda lime glass slides due to their high transparency in the ZnO band edge region. A pristine substrate of the same type was always used for baseline correction prior to measurement. The relationship between transmitted intensity (I_t) and incidence intensity (I_0) to a thin film of thickness (d) has been assumed to follow the Beer-Lambert relation (3.5);

……………………………………………………………......…… (3.5)

where α is the absorption coefficient of the film. The transmittance − can be directly measured and thus, for a film of known thickness, the absorption coefficient can be calculated from the transmission data.

The absorption coefficient is also related to the optical bandgap via Tauc's relation (3.6) [232]. Photons with frequencies greater than the resonance frequency of the film are strongly absorbed by electrons which are excited across the bandgap into the conduction band. For transition between parabolic valence and conduction bands (in this work we assumed these bands to be so);

…………………………………………....……..…. (3.6)

where h is Planck's constant, υ is the photon frequency and E_g is the bandgap of the film, and n is a real number. For a direct bandgap material like ZnO, the index n = ½ and for indirect bandgap material such as silicon for example, n = 2.

3.5.1.4.1 Localised states and Urbach tails in ZnO

The film absorption coefficient as a function of photon energy in the near band edge region is usually calculated using equation (3.7). The empirical parameter E_u, often referred to as the '*Urbach tails*' has the dimensions of energy and is frequently used to determine the film quality (measures the degree of disorder in amorphous semiconductors) [233]. E_u is usually used to describe the width of the localized states in the bandgap (but not their positions). Pankove has shown that the value of E_u is related to the impurity concentration [234]. However, Redfield has shown that all defects (point, line, and planar defects) lead to local electric fields that cause band tailing. Thus, the Urbach energy can be considered a parameter that includes all possible defects [235, 236].

— …………………………......………………………...…........…… (3.7)

In this work, the Urbach tail is used as a parameter for assessing the amount of disorder in ZnO films.

3.5.2 Electrical Characterisation of films

This section presents the electrical characterisation techniques used for characterising the different dielectrics and ZnO thin films used in this work.

3.5.2.1 Resistivity

The electrical resistivity, , of a material depends on it free-carrier concentration, n, and its carrier mobility, μ, as in equation (3.8), with units of Ohm-cm (Ωcm).

— .... (3.8)

where, q is the carrier's elemental charge. The reciprocal of the resistivity is the conductivity σ of the material. In TFTs, the carrier mobility in the active channel is strongly influenced by the channel discontinuity at the insulator/semiconductor interface. The effective mobility μ_{eff} in this case is obtained from contributions due to lattice scattering , impurity scattering and grain boundaries scattering according to Mathiessen's addition rule (3.9) [49];

— — — — .... (3.9)

Mobility in ZnO films is often dominated by grain boundary mobility, especially in films with smaller crystallites where huge densities of grain boundaries are often observed. The grain boundaries therefore indirectly affect ZnO film resistivity.

Thin film resistivity can be measured using a number of different techniques; which include: the transmission line method (TLM), Van der Pauw, two- and four-point probe methods. In this work, the TLM was used due to its simplicity and non-dependence on geometric factors.

3.5.2.1.1 Transmission Line Method (TLM)

The multi-contact two-terminal transmission line method (TLM) [237] is a widely-used technique to measure the electrical resistivity , and contact resistance R_c at metal-semiconductor junctions. For a film on a non-conducting substrate (e.g. glass) with thickness t, the length Z of the metal electrode and the varying inter-electrode separation (L) as in figure 3.9, the total electrical resistance R_T can be expressed by equation (3.10).

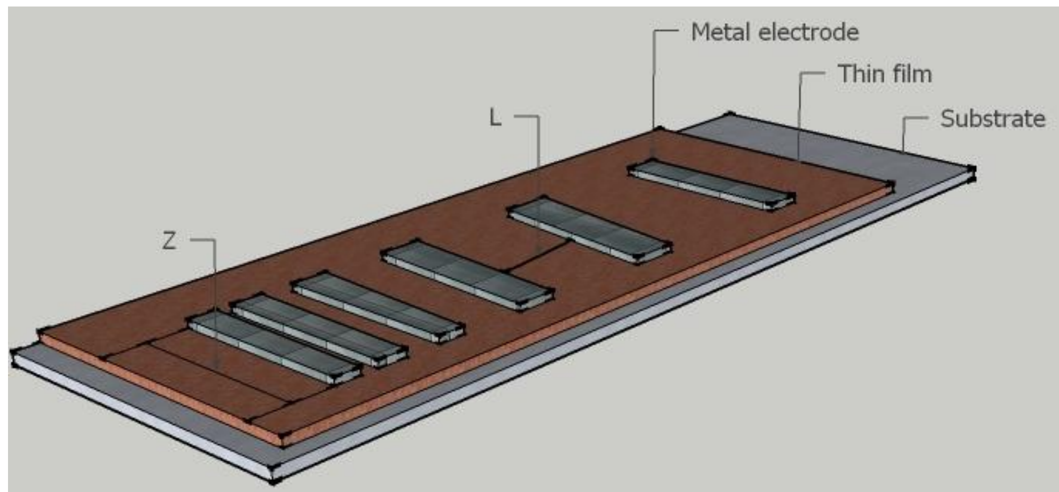


Figure 3.9 – A typical sample prepared for transmission line method (TLM) measurement of resistivity.

— ………………………………………..……….......………. (3.10)

In this work, the total resistance R_T of the films was calculated as the slope of the current-voltage (IV) data obtained using an HP4140B pico ammeter, controlled remotely by a Visual Engineering Environment (VEE) program. A plot of R_T versus L

results in a straight line graph whose slope is —. The intercept on the ordinate (R_T-axis) corresponds to $2R_c$. A typical room temperature R_T-L plot of a ZnO film deposited in this work is shown in figure 3.10.

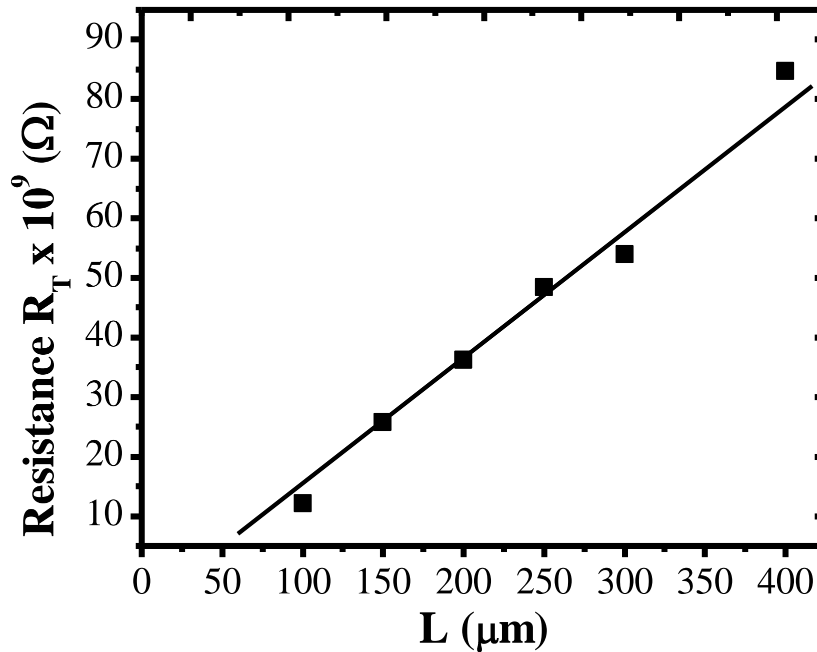


Figure 3.10 - A typical RT-L plot of a ZnO film on glass substrate used to extract the electrical resistivity.

3.5.2.2 A Metal-Insulator-Semiconductor (MIS) Structure

Figure 3.11 shows a typical structure of a MIS capacitor. A ramping of the gate voltage through a complete cycle provides a means of estimating the dielectric traps/interface charges via any hysteresis that may be observed. The density of interface traps and fixed charges can be obtained by comparing the measured capacitance versus voltage (C-V) curve to the theoretical characteristics. A translation of the C-V curve

along the voltage axis is a measure of the total insulator charge, while the interface states density is proportional to the degree of ‘stretch-out’ in the characteristics by comparing the measured experimental capacitance with the theoretical capacitance [238]. In this work, MIS structures (figure 3.11) were produced on a p-type silicon substrate and wherever the interface (insulator/substrate) trap density is estimated, the Terman method [238] is employed. However, the interface traps at the ZnO/insulator interface is estimated from a ZnO TFT bottom-gated test structure using the method described in chapter 6 {§ 6.2}.

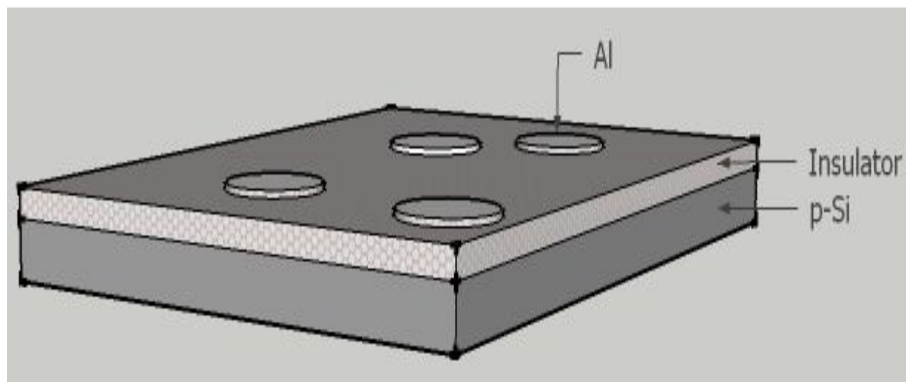


Figure 3.11 – A typical MIS structure

3.5.2.2.1 Extraction of Dielectric Constant

In this work, the dielectric constant was measured by fabricating MIS capacitors using the dielectric material of interest on (100)-silicon and calculating the dielectric constant (κ) from the measured capacitance. Due to the frequency dispersion of the capacitance observed in most of the high-k dielectric films, the true capacitance C was extracted from two different capacitance values $C_1^{'}$ and $C_2^{'}$ measured at frequencies of

f_1 = 100 KHz and f_2 = 1 MHz respectively using equation (3.11) as proposed by Yang and Hu [239].

________________ .... (3.11)

Where C, is the true capacitance of the dielectric layer, and $D_1^{'}$ and $D_2^{'}$ are the dissipations measured at the frequencies f_1 and f_2 respectively. A typical C-V characteristic of a MIS structure incorporating a high-k dielectric (Gd_2O_3) deposited by MOCVD on p-type silicon used in this work is shown in figure 3.12.

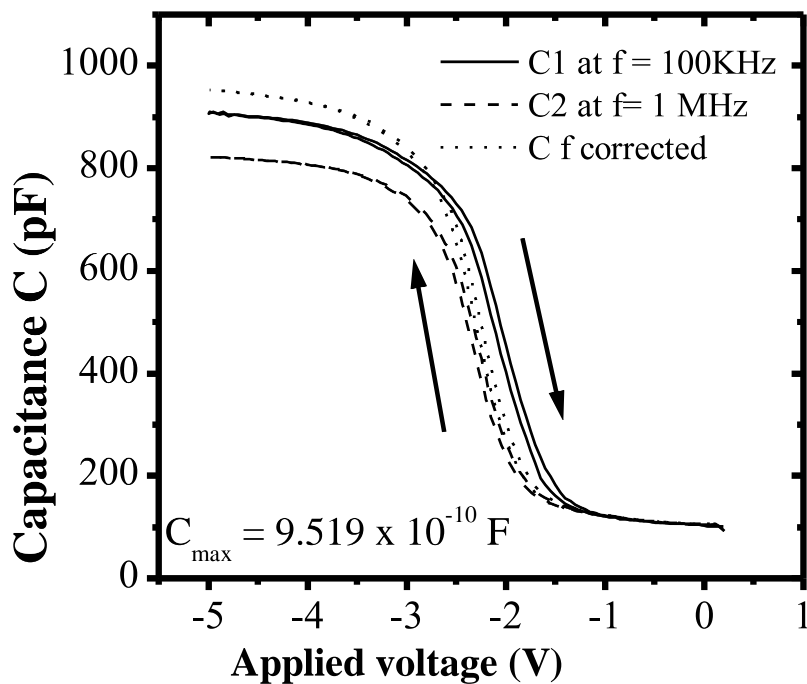


Figure 3.12 - A typical C-V characteristic of a MIS structure incorporating Gd_2O_3 deposited by MOCVD.

The area, A, of the aluminium (Al) electrodes in the MIS structure was defined by the dimension of the shadow mask (A = 0.0079 cm^2). The thickness d of the dielectric material was obtained by ellipsometry measurement, and the measured capacitance of the device in accumulation was used to calculate the dielectric constant κ of the dielectric material by substituting in (3.12). Prior to the deposition of the dielectric material, aluminium was deposited at the back of p-type silicon substrate and annealed at ~490 ^{0}C in a nitrogen environment to ensure an ohmic contact was obtained between the silicon substrate and the back electrode.

— …………………………………........…………………………….….… (3.12)

Table 3.1 shows the dielectric constants of some of the high-k dielectrics deposited by MOCVD and thermally grown SiO_2 produced in this work.

Table 3.1 - Typical parameters of dielectric materials used in this work.

Material	**Sample ID**	**Dielectric Constant (κ)**	**Leakage current density J (A/cm^2) at a field of 0.2 MV/cm**
Gd_2O_3	APMCVD04	9.6	3.2×10^{-9}
Y_2O_3	APMCVD05	10.1	1.2×10^{-9}
HfO_2	APMCVD05	7.9	8.8×10^{-10}
SiO_2	SiO_2-Batch 2	3.1	9.6×10^{-9}

3.5.2.2.2 Dielectric Strength

The maximum electric field (usually in $MVcm^{-1}$) that can be applied across an insulating material before breakdown occurs is referred to as the '*dielectric strength*'. In this work, the breakdown was considered at the gate voltage where the current just begins to increase exponentially with voltage.

Breakdown is usually limited by either thermally or electrically activated processes. However, at low temperatures, including room temperature, breakdown is dominated by electrical activation. The dielectric strength provides a means of evaluating the integrity of an insulator. The critical breakdown field (dielectic strength) has been reported to be proportional to the radius of the intrinsic-point defect cluster and the density of ionised impurities in them [240-242]. *'Soft breakdown'* is often associated with large defects clusters or a high density of ionised impurities, while *'hard breakdown'* is associated with materials of low defect density [243, 244]. In order to minimise the effects of surface resistivity that results from thickness differences on the properties of the material and thickness dependence issues, the dielectric strength was compared for materials of approximately the same thickness (~100 nm as for SiO_2 and for the high-k dielectrics). The dielectric strengths were measured by applying a negative (for p-type MIS) or positive bias (for n-type MIS) on the aluminium gate electrode until breakdown was observed (this was determined by the gate voltage at which the leakage current reached 100 pA, due to the fact that at leakage currents beyond this value the C-V characteristics began showing significant gate leakage), and an exponential increase in current is observed thereafter. Care was taken to ensure that all breakdown measurements were performed after all required measurements have been

performed, as breakdown once reached may result in irreversible damage of the dielectric material. Figure 3.13 shows a typical IV plot used for dielectric strength extraction.

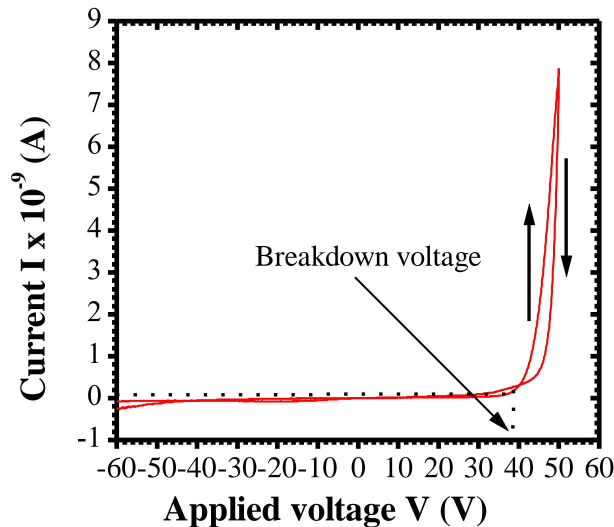


Figure 3.13 - A typical IV plot used for the extraction of dielectric strength of MIS structure incorporating thermally grown SiO_2.

3.6 Summary

In this chapter, the different thin film preparation and characterisation techniques relevant to the work presented in this thesis have been discussed. A number of PVD and CVD techniques have been discussed briefly and compared with sputtering deposition, which has been extensively-used in this work. Electrical and physical characterisation (UV-Vis spectroscopy, XRD spectroscopy, C-V and IV) techniques used for both insulating films and insulator/semiconductor junction characterisation is briefly presented.

Chapter - 4

The Influence of Oxygen Adsorption at a (0001) ZnO Surface

4.1 Introduction

There has been an increasing need for novel materials in electronic applications both for research and industry as a result of the performance limitations imposed on silicon-based devices such a-Si:H TFTs. A large number of materials are being considered, with many such materials having little or no existing data [245]. This has made materials modelling using computing resources invaluable; and first principles (ab initio) methods using density functional theory (DFT) has been one such technique for understanding materials where little or no experimental results are available.

Ab initio methods are based on quantum mechanical concepts of inter-atomic interactions, and unlike semi-empirical techniques, do not require recourse to experimental data, except the basic elementary entities such as the electronic charge. However, DFT usually requires high computational cost and time. In an attempt to solve this problem, DFT simulations are usually performed for fixed ions and therefore produce results that best describe ground state energy (0 K processes). Thus, the band structure and hence the density of states (DOS), generated by DFT only describe accurately the filled bands, so that the bandgap is usually underestimated by up to 50 % [246, 247]. Nevertheless, intuitive information is still obtained from trends observed in DFT calculations, especially for future technologies, and can offer a cost effective route to the investigation of new materials.

In this chapter, the influence of O_2 adsorption on the electronic properties of ZnO (0001) surface is examined via DFT as implemented in the '*Vienna Ab-initio Simulation Package (VASP)*'. The surface modification and the identification of preferred adsorption sites are also investigated. These effects are further elucidated experimentally by low temperature (150 – 350 ^{0}C) annealing of ZnO layers in air to understand the effects of O_2 adsorption/desorption at the ZnO surface and/or grain boundaries. The role of O_2 adsorption on the electrical stability of ZnO thin films is then discussed.

4.2 Density Functional Theory (DFT) as Implemented in the '*Vienna Ab initio Simulation Package*' *(VASP).*

VASP is a software package for performing quantum-mechanical molecular dynamics simulations using DFT with pseudo-potentials and a plane wave basis set [248-251]. For a many-particle system in the absence of an external influence, the total Hamiltonian is given by;

..(4.1)

VASP is based on the Born-Oppenheimer approximation of the total Hamiltonian. In this approximation, the nuclei are treated as classical particles with a heavy mass M_i, while electrons are considered as quantum mechanical particles with a much smaller mass m_e. The nuclei are then considered to be stationary relative to electrons, as $M_i >> m_e$. Therefore, the first term in equation (4.1) has a negligible contribution to the total

Hamiltonian while the last term only provides a constant external potential, V_{ext}, to the sea of electrons [252]. The Hamiltonian in (4.1) is now of the form;

.... (4.2)

and are the kinetic and potential energy operators of the electron respectively.

From Hohenberg-Kohn theorem [252, 253], *the ground state electronic density is an invertible functional of the ground state energy.* This means that if ψ is the normalised wave function of the entire many-particle-system then;

.... (4.3)

where E_0 is the ground state energy of the system. The minimum of equation (4.3) is E_0 and this occurs only when ψ is the ground state eigen-function of the system.

In order to calculate this ground state density functional, VASP uses the pseudo-potential method. From this, the ground state wave function of the system can then be determined and hence all other properties that will thoroughly characterise the many-electron system in the ground state.

4.3 Single-electron Approximation

Sham and Kohn [252] reduced the complex many-particle problem of (4.1) into a set of non-interacting single-particle Schrödinger equations that can be solved easily compared to the normal many-particle system Schrödinger-equation. For a system of

non-interacting particles with wave function of each ith particle represented by , the single-particle equations are of the form;

.... (4.4)

.... (4.5)

where is the exchange-correlation (potential experienced by a single electron due to the effect of the other electrons in the system) energy functional, is the Hartree-Fock potential (potential of a system of non-interacting electrons), (potential created by the fixed ions on a singly non-interacting electron-system) functional operator and is the total kinetic energy functional for the non-interacting electron gas.

The efficiency of the calculation lies in an efficient diagonalisation technique of the Sham-Kohn Hamiltonian , and on the dimension of the plane wave basis set used, upon which the accuracy of the result relies [248, 249].

Car and Parrinello [248, 254] introduced an efficient way of calculating the action of the Sham-Kohn Hamiltonian onto the electronic wave functions. They used the fact that the local potential part of the Hamiltonian is diagonal in real space and that the kinetic energy part of the Hamiltonian is diagonal in reciprocal (momentum) space. Therefore, if we consider a plane wave function $\psi(\vec{r})$ in real space, the local potential operator and the kinetic energy operator —— , then the single-particle Schrödinger equation can be re-written as the sum of equations (4.6) and (4.7) below. This shows that the kinetic energy operator and the local potential operators are diagonal in the reciprocal and real space respectively.

—— —— ....…………………………….……………... (4.6)

.... (4.7)

where is the Fourier transform of the wave function in reciprocal space and $< V_{loc} >$ is the eigenvalue of the local potential. Hence, time is usually gained by transforming the wave functions from real space to reciprocal space and vice versa using fast Fourier transforms (FFT). The non-local part is also easily evaluated using the pseudo-potential technique.

4.4 Pseudo Potential Method

In order to reduce the cost in computational resources associated with an infinite set of wave vectors that will describe the system more accurately, the pseudo potential approach is usually used. Having used the Born-Oppenheimer approximation in the calculations, this means that the inner atomic shells have little contribution. However, given that they are all made up of paired-electrons, they do not contribute to conduction but help in screening the valence electrons from the influence of the nuclear field. Close to the nucleus the wave function varies very rapidly, requiring the superposition of too many wave functions to accurately describe the potential in this region. However, this region has little effect on the electronic transport properties. Hence, in order to improve on computational time, a set of slowly varying pseudo-potentials is introduced at the neighbourhood of the nuclei in such a way that they remain continuous with the external and exact potential of the system at the boundary. The dimension of the basis set is

determined by the maximum K-vector $K_{\max}$ of a single-particle wave function that will generate a wave function close enough to the external wave function describing the slowly varying region in the valence shell. $K_{\max}$, is usually specified using cut-off energy E_{cut} as in equation (4.8).

$$E_{cut} = \frac{\hbar^2 K_{\max}^2}{2m_e} \quad \ldots\ldots\ldots (4.8)$$

where, m_e is the electronic mass and $\hbar$ is the reduced Planck's constant.

In this thesis, E_{cut} = 400 eV has been used throughout to model the ZnO ionic potential. This is much greater than the maximum energy (270 eV) of the pseudo-potential file used in the simulation and leads to improved accuracy.

4.5 Material Modelling

This section presents the techniques often used in VASP to simulate different material geometric structures as used in this thesis. The supercell method, which is frequently used in material simulation for investigating bulk, interfaces and surface properties is discussed in {§ 4.5.1}.

4.5.1 The Supercell Method

The supercell method is based on the periodic boundary conditions, which are intrinsic properties of solids. In a pure crystalline material, the periodic boundaries allow for a piece of the material to be extended infinitely in all directions [255]. This allows for bulk properties to be modelled accurately. In order to study surfaces and

interfaces in VASP, the slab method is often used. For a supercell that generates the entire lattice, when a defect is modelled, the position of the defect in the supercell is immaterial due to the periodicity exhibited by the supercell. The images of the defect will appear in the repeated supercells, and the defect's interaction with its periodic image affects the simulation results. It is therefore important that supercells used are large enough to minimise the influence of image interactions. Defects that give rise to delocalised states for example, have wave functions that will spread over large areas, and the size of the supercell required to accurately model such defects would be considerable.

In this work, $2 \times 1 \times 2$ ZnO supercells were used for modelling the ZnO bulk and surfaces. Slabs with a vacuum of 25 Å in the z-direction were used to model the effects of oxygen adsorption on the (0001) surface. In order to mimic the contributions from oxygen vacancies, an oxygen vacancy was created close to the surface and near the oxygen adsorption site (figure 4.1). The adsorbed O_2 was placed with its principal axis perpendicular to the adsorption surface, with the nearest O-atom at a distance of 2.073 Å (obtained by performing initial optimisation runs using a smaller supercell) from the surface prior to relaxation. Three adsorption sites have been investigated; 1) the O_2 molecule is placed directly above the surface Zn-atom close to the vacancy (T-site), 2) the O_2 molecule is placed directly above the centre of the ZnO surface hexagon (H-site) and 3 the O_2 molecule is placed directly above the midpoint of the ZnO surface bond close to the vacancy.

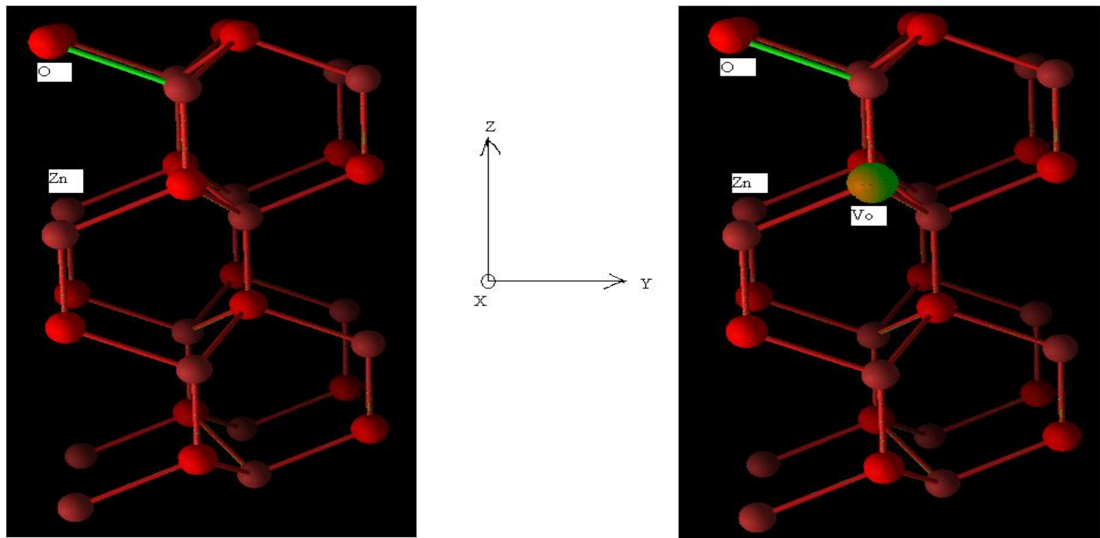


Figure 4.1 - A 2 × 1 × 2 crystallographic unit cell of: a clean ZnO (left) and ZnO layer with an oxygen vacancy (Vo) close to the upper (0001) surface (right).

4.5.2 Modelling Surfaces

In order to model surfaces in the supercell, the slab method is used. In this approach, a large vacuum (containing zero atoms) is added above one of the boundaries of the supercell, giving rise to the surface to be studied. As the entire supercell remains periodic in all directions, this vacuum will repeat between supercells and as such should be large enough to minimise the interaction of the supercell and its image. This generates a slab of material that extends infinitely in the other two directions.

4.5.3 Convergence Criterion

Since it is important to ensure that the vacuum separating repeating slabs is enough to minimise the interaction between the upper surface of one slab and the lower

surface of the repeated slab above it, the dimension of the supercell in this direction may become too large. By increasing the vacuum size, the number of plane waves required will also increase. This will greatly increase the computational cost. Also, the slab should be reasonably thick, so that the effect of discontinuity at the surface does not affect the inner layers which are supposed to reproduce bulk properties. By comparing the electrostatic potentials of the slab to that of the bulk supercell relaxed with the same parameters, the bulk potential should show negligible off-set with that of the innermost layers of a slab that is thick enough to be used.

4.6 Extraction of Binding Energy

The binding energy (E_b) of a system of molecules is the energy required to bind a collection of interacting molecules together. For a system of N interacting molecules, the binding energy is defined as in equation (4.9).

………………………………………………… (4.9)

where is the total energy of the interacting molecular system and is the sum of the total energies of the individual molecules X_i. The binding energy so defined is negative for an exothermic (favourable) interaction, and positive for an endothermic (unstable) interaction.

4.7 Oxygen Adsorption on (0001) ZnO Surface

The effects of oxygen adsorption on the ZnO surface, and at the crystallite interfaces of a ZnO film on conductivity, have been investigated. O_2 adsorption as

suggested here is a suitable pre-treatment technique that could be used to achieve more stoichiometric and stable films [100, 256]. Khranovskyy et al. reported that oxygen adsorption at a ZnO surface and/or at the grain boundaries was predominantly a diffusion process with an oxygen diffusion coefficient in undoped ZnO between $8.3 \times 10^{-16} - 4.3 \times 10^{-14}$ cm^2 s^{-1} [100].

Using VASP, we show that O_2 adsorption on the (0001) ZnO surface remains a favourable reaction irrespective of the adsorption site (binding energy table 4.1). In all three configurations that we studied, the nearest ZnO surface distance to the nearest O-atom is from the Zn-atom. These adsorption distances were calculated to be 2.06, 2.07, and 2.23 Å for the T-site, B-site and H-site respectively. Comparing these adsorption distances with the binding energies of the corresponding adsorption sites, it is suggested that the T-site is the most likely adsorption site.

Table 4.1 - The bandgap, total energy and binding energy of the different O_2 adsorption sites on (0001) ZnO surface

Configuration	**Bandgap**	**Total Energy**	**Binding energy of O_2**
O_2 adsorbates	---	-7.760	---
Pristine ZnO	1.359	-140.300	---
Pristine ZnO with	1.883	-132.823	---
B-site	0.916	-141.741	-1.158
H-site	0.938	-141.740	-1.157
T-site	0.956	-142.888	-2.305

4.7.1 Electronic Band Structure and Density of States

The presence of a V_O near the ZnO surface gives rise to an up-shift in the Fermi level as seen from both the electronic band structure and DOS (figures 4.2 and 4.3).

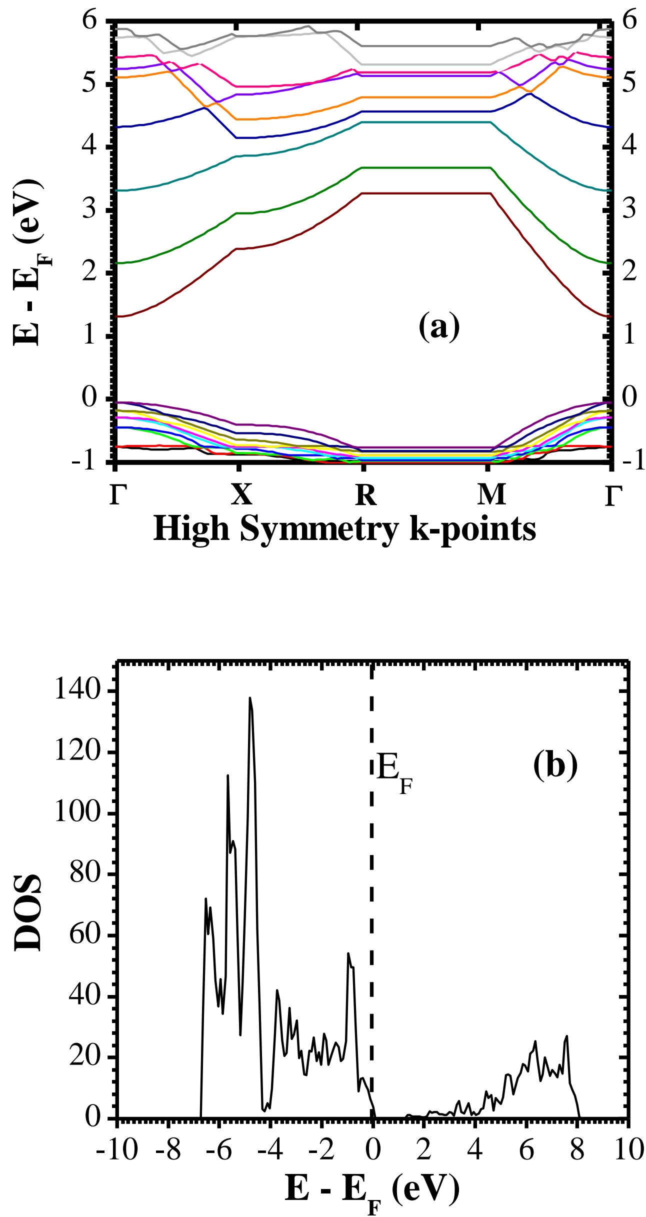


Figure 4.2 – a) The electronic band structure and b) the electronic density of states (DOS) of a defect free ZnO layer.

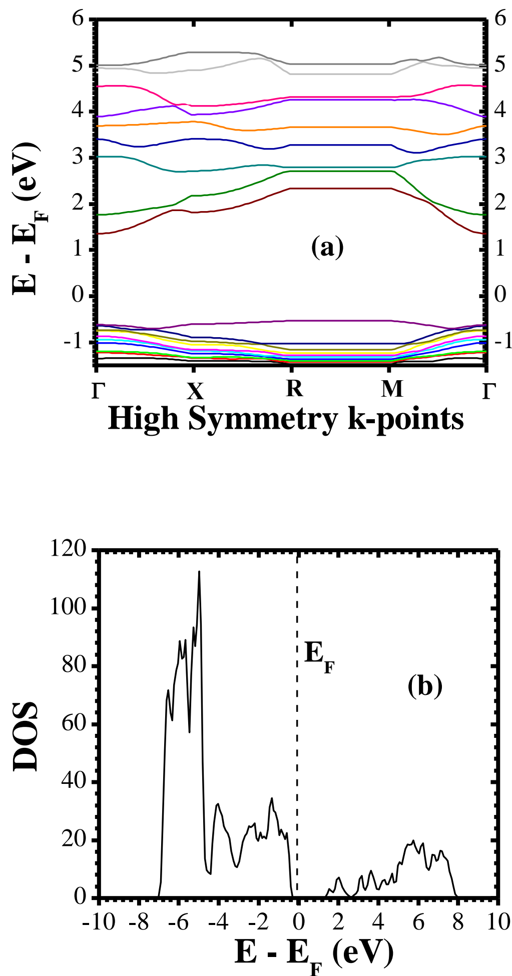
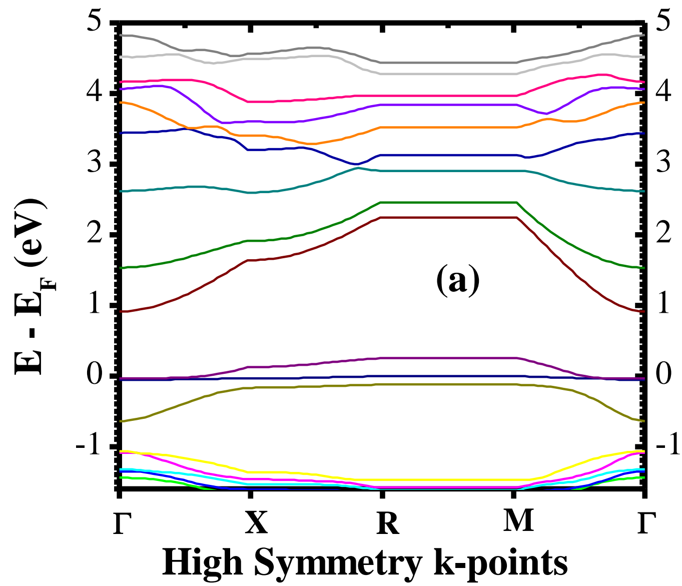


Figure 4.3 – a) The band structure and b) the DOS of ZnO with an oxygen vacancy close to the (0001) surface (the zero of the energy scale corresponds to the Fermi energy E_F).

The V_O also results in an enhancement of the bandgap, and so is likely to improve film transparency (figure 4.2a and 4.3a).

O_2 adsorption at the surface of c-axis oriented ZnO has been reported to have a modulating effect on the ZnO layer conductivity [256]. In the sub-section {§ 4.7.1}, the effects of O_2 adsorption on the electronic band structure and density of states of ZnO is

examined. Analysis of band structure and density of states of the system reveals that an introduction of a V_O near the ZnO (0001) surface enhances the bandgap by about 39 % (it is worth noting that DFT only accurately describe ground state properties and has been known to underestimate band gap, hence, only the trends in band gap results are useful). Furthermore, O_2 adsorption at the different adsorption sites (T-, H- and B-sites) decreases the bandgap by about 49, 50 and 51 % for the T-site, H-site and B-site respectively with a corresponding increase in the O-O bond length in the O_2 adsorbates of 13, 19 and 20 %. Therefore, the O_2 molecule is more likely to remain un-dissociated at the T-site. In all three adsorption sites, a sharp peak is introduced in the electronic density of states (DOS), centred at the Fermi level (figures 4.4 – 4.6). Due to the fact that O_2 adsorption enhances the bandgap and partly because ZnO is a wide bandgap material, most of the states created following an O_2 adsorption are likely to be deep level, having a negligible influence on the electronic properties of delocalised carriers.



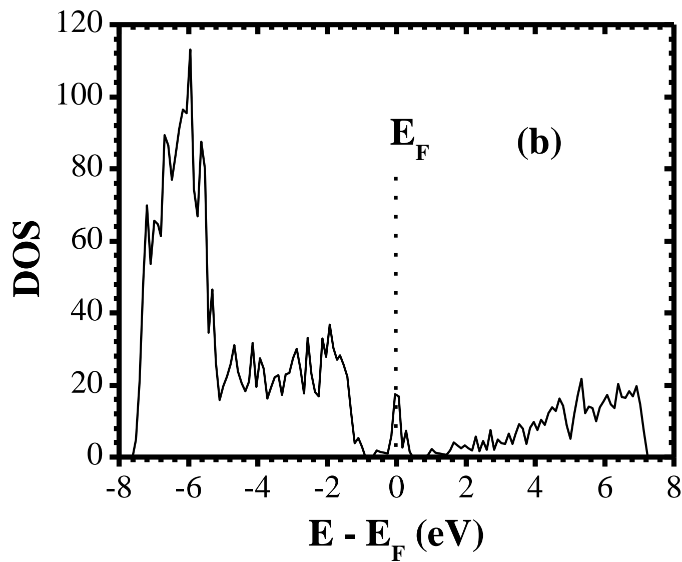
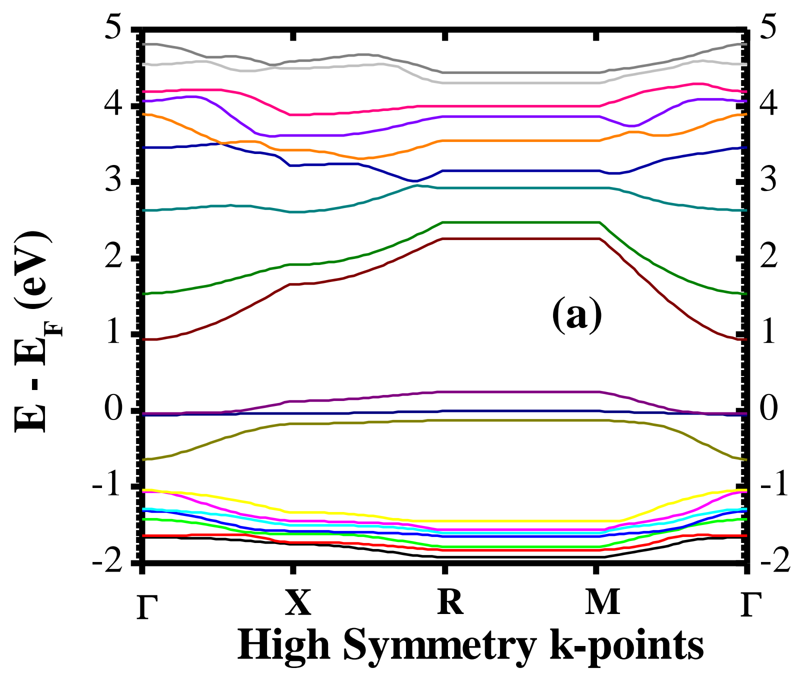


Figure 4.4 – a) Band structure and b) DOS of ZnO with O_2 adsorbed at B-site on (0001) surface near the Vo.



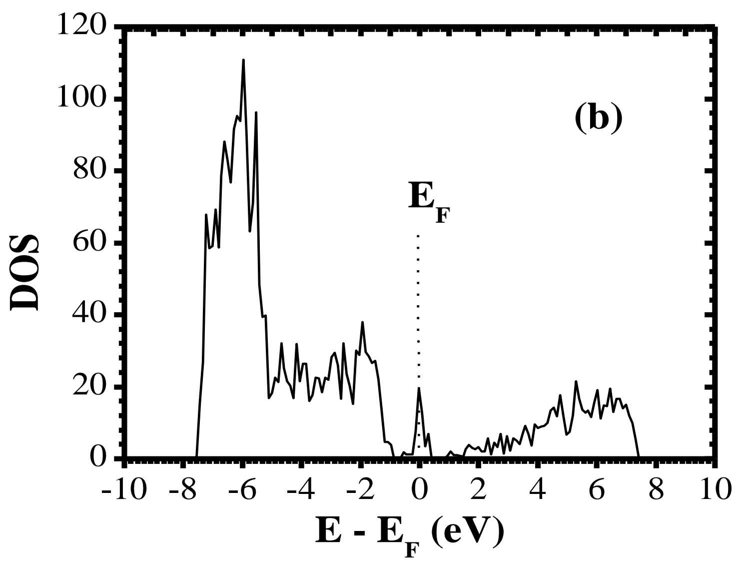


Figure 4.5 - a) Band structure and b) DOS of ZnO with O_2 adsorbed at H-site on (0001) surface near the Vo.

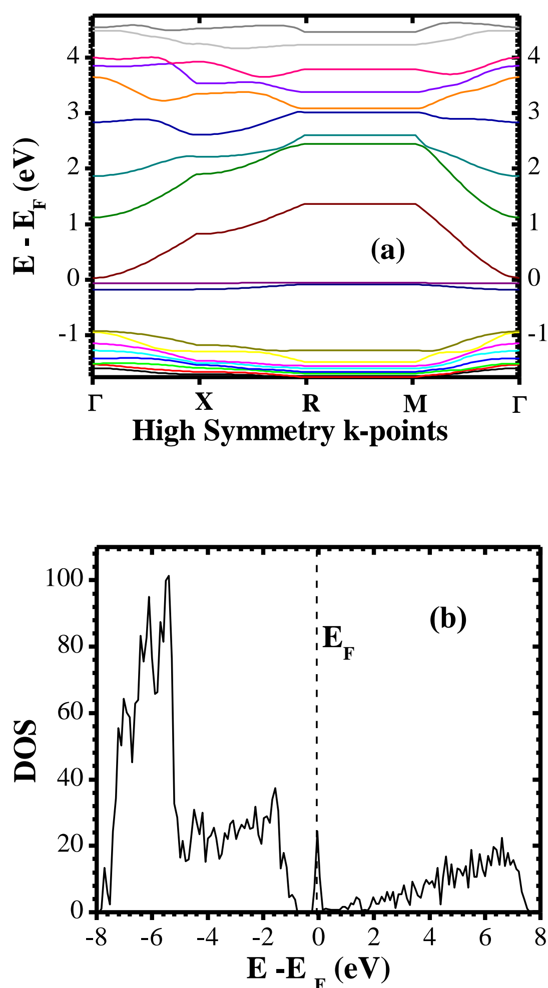


Figure 4.6 - a) Band structure and b) DOS of ZnO with O_2 adsorbed at T-site on (0001) surface near the Vo.

4.7.2 Electron Localisation Function (ELF)

The ELF of the (0001) ZnO surface (with and without V_O) is presented in figure 4.7. In VASP, the ELF is evaluated by measuring the relative probability of locating an electron close to another of the same spin (as proposed by Becke and Edgecombe [257]) and often used to describe chemical bonding in terms of localised electrons [257, 258].

As observed in figure 4.7, the presence of a V_O close to the ZnO surface modifies both the surface bonding and the surface structure leading to different surface reconstructions.

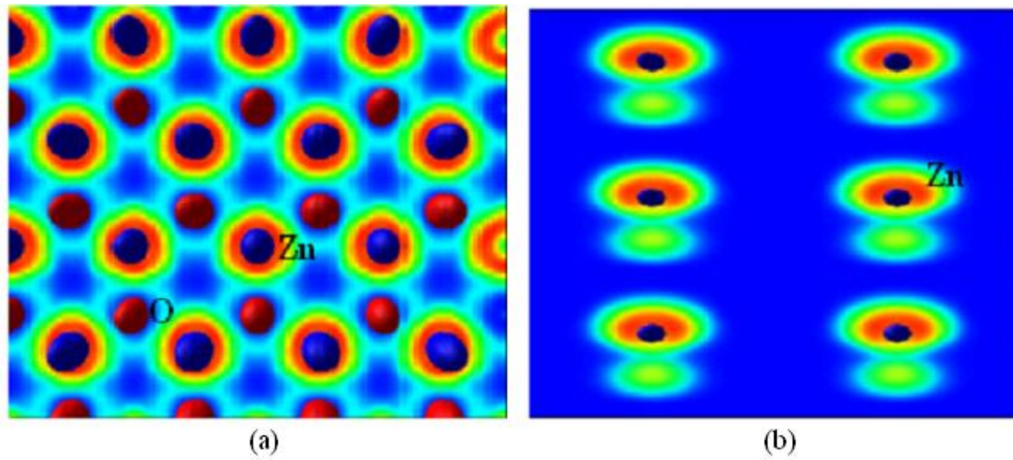


Figure 4.7 – The electron localisation function (ELF) of a (0001) surface of (a) defect free ZnO and (b) ZnO with an oxygen vacancy close to the surface.

In a pure ZnO bulk, the underlying O-atoms are moved to the Zn-terminating (0001) surface forming a hexagonal arrangement of alternating Zn- and O-atoms. The presence of a V_O close to the (0001) surface leads an increased separation between the Zn-terminating surface and the underlying O-terminated layer so that the surface is predominantly made of Zn atoms (figure 4.7 b). Since the T-site adsorption is found to be the preferred adsorption site, the presence of V_O also enhances O_2 adsorption and as a consequence modulates the electronic properties of the film.

4.8 The Effect of Low Temperature Annealing and Oxygen Desorption at (0001) ZnO Surface

O_2 adsorption and thermal/photo-desorption of O_2 from the ZnO surface and/or grain boundary interfaces have been reported to have a strong modulating effect on the its conductivity [219, 259-262]. Changes in electrical conductivity following low temperature (~ 400 ^{0}C) thermal treatment have been ascribed to O_2 desorption at the film surface; while a further decrease in electrical conductivity following higher temperature treatment has been associated to the desorption of O_2 at both the film surface and the grain boundary interfaces [219].

In this work, films that have been pre-treated in vacuum with oxygen were annealed at temperatures ranging from 150 – 350 ^{0}C. The pre-treatment was achieved by treating as-deposited ZnO films with oxygen (0.2 mTorr at room temperature) without breaking the vacuum for one hour. All the films studied were sputtered-deposited on different corning (2875-25) glass substrates at the same time in order to minimise the effects of parameter variations. The films were then annealed at different temperatures in air and their electrical resistances (R) compared with that of the un-annealed film for different channel lengths (L). The non-linear variation of electrical properties of polycrystalline ZnO films with channel length is often attributed to the heterogeneous distribution of crystallites and/or grain boundaries [90, 263-265].

4.8.1 Electrical Conductivity

The electrical properties of aluminium-doped ZnO (ZnO:Al) films have been reported to improve with rapid temperature annealing (RTA) as a result of defects activation in the grain boundaries and surface desorption of O_2 [219, 256, 266-269]. Moreover, oxygen adsorption has been found to play a significant role in modulating ZnO film resistivity [100]. In addition, ZnO TFTs have been reported to suffer from threshold voltage instability as a result of changes to the surface properties due to exposure to an ambient environment [39].

In this work, the electrical resistivity of films is seen to depend on annealing temperature (figure 4.8).

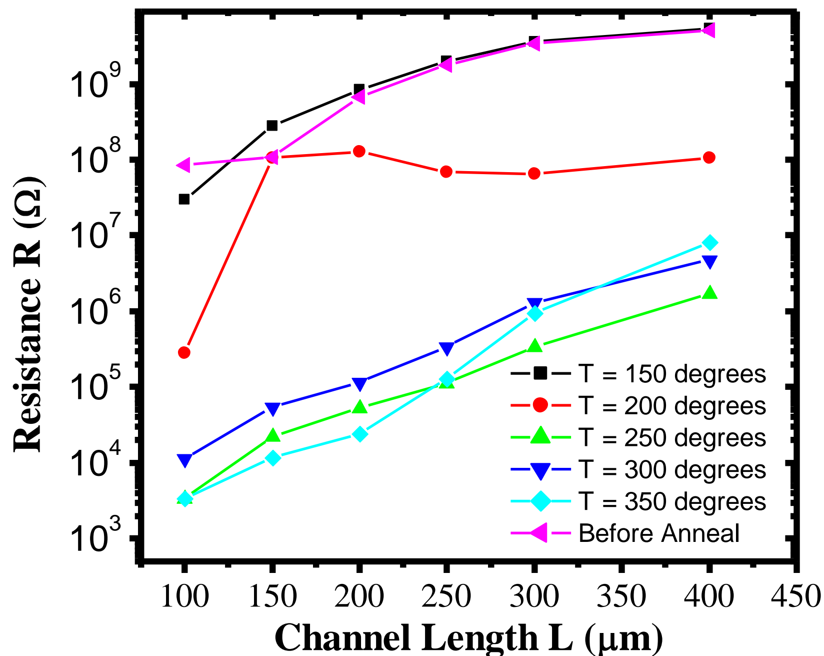


Figure 4.8 – The relationship between resistance R and channel length L parameterised by the annealing temperature T.

Under low temperature annealing (150, 200 ^{0}C) in air, the film resistance is almost unchanged. At higher temperatures (250 - 350 ^{0}C), a sharp decrease in resistance of upto four orders in magnitude is observed. This could be associated to O_2 desorption at the surface and/or at the grain boundaries, resulting to the creation of additional V_O in the film. The greater linearity of the dependence of R on L, in the films annealed at higher temperatures further confirms the possible desorption of O_2 at the grain boundary interfaces.

4.8.1.1 Electrically Air-stable ZnO Thin Films

The electrical stability of ZnO TFTs in atmospheric ambient [270] is one of the major issues that is required to be addressed if they are to compete with conventional amorphous silicon TFTs. By treating the (0001) surface of ZnO thin films with O_2 in a vacuum, an optimal O_2/Ar ratio of 0.01 at an RF power of 500 W was found. The optimal film has a resistivity of ~ 2.4×10^5 Ωcm, with negligible variation in electrical and optical properties in air for over 18 months. This is an indication that TFTs fabricated with such films are likely to be stable in air.

In addition to improving film electrical stability, O_2 adsorption may also provide a new route to ZnO surface passivation. This is an indication that treatment of ZnO (0001) surface with O_2 can be used as an ageing technique to reduce the variability of film electrical properties in air. Furthermore, this may even eliminate the use of a passivation layer.

In this work, ZnO thin films produced by RF sputtering have been pre-treated with O_2, and optimised films were shown to be stable in air (figure 4.9). The details of

this study are provided in the proceedings of the Material Science Society (MRS) Fall 2009 [271].

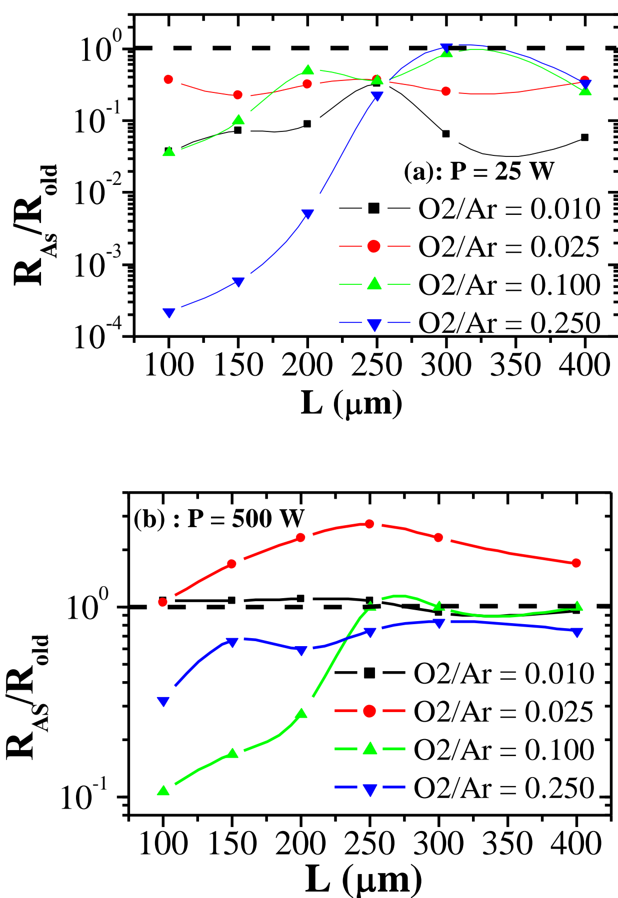


Figure 4.9 - Normalised resistance as a function of ZnO channel length L of the film after 18 months exposure in air. R_{AS} and R_{old} are the resistances of the as-grown film and of the same film after 18 months respectively, produced at (a): 25 and (b): 500 W RF power

4.8.2 Optical Properties

The optical bandgap, E_g, (as shown in figure 4.10) is unaffected by low temperature annealing up to temperatures of 150 ^{0}C with a small increase in the Urbach

tail states, E_u, of ~ 2 meV after 150 ^{0}C annealing. The energy changes ΔE_g and ΔE_u in figure 4.10 are defined as $\Delta E_g = E_{g2} - E_{g1}$ and $\Delta E_u = E_{u1} - E_{u2}$, where the subscripts 1 and 2 represent conditions before and after annealing respectively. It is observed that, for annealing temperatures < ~ 200 ^{0}C, E_g and E_u are affected. Within the temperature range of 200 – 350 ^{0}C, the change in Urbach tail states ΔE_u is observed to be between 25 – 31 meV. The decrease in E_u at annealing temperatures over 200 ^{0}C suggests a decrease in structural disorder with annealing and correlates the decreased resistance in figure 4.10. This is likely to be dominated by O_2 desorption at the grain boundaries. The decrease in E_u, together with the linear R-L relation observed above, suggests that O_2 adsorption at ZnO grain boundaries is likely to increase disorder.

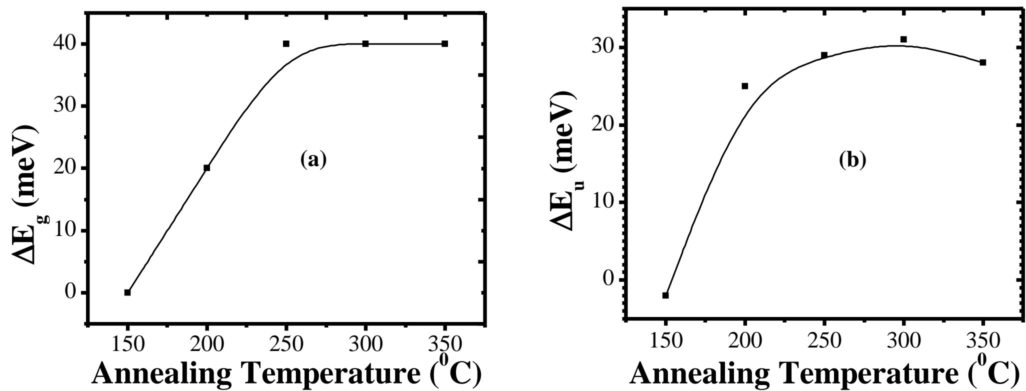


Figure 4.10 – The variation of: a) change in bandgap ΔE_g and b) change in Urbach energy ΔE_u with annealing temperature.

4.9 Summary

In this chapter, the effect of intrinsic point defects (oxygen vacancies in particular) on the electronic properties of ZnO thin films has been investigated by a

DFT technique. The influence of adsorbed O_2 on ZnO thin films is also investigated and proposed here as a suitable ageing technique that could be used to improve film electrical stability in atmospheric air. In addition, low temperature (150 – 350 ^{0}C) annealing in air has been used as a complementary method to study the effect of oxygen desorption from ZnO, possibly at the exposed top surface or at the grain boundary interfaces. As a consequence of the studies carried out in this chapter, it has been possible to fabricate high performance ZnO TFTs with O_2 treated ZnO layers (chapters 6 and 7).

Chapter – 5

The Optimisation of ZnO Films for TFT Applications

5.1 Introduction

TFTs are commonly used in Active Matrix Liquid Crystal Displays (AMLCDs) as select transistors. AMLCD technology is widely used in applications such as mobile phones, notebook personal computers, desktop monitors and high definition televisions. Also, TFTs are becoming increasingly used in light-emitting-diode (LED) display technology both as select and drive transistors. The drive transistors supply current to the LEDs, and it is therefore important that they are fairly stable during their operation, as any degradation in the current will result in reduced light intensity from the LED and hence affect the corresponding pixel quality.

In this chapter, the roles of the structural properties (interfaces and device configuration) of the TFT that are likely to influence both performance and/or electrical stability are discussed. Furthermore, the integration of high-k dielectrics (hafnium oxide (HfO_2), Gadolinium oxide (Gd_2O_3) and Yttrium oxide (Y_2O_3)) deposited by MOCVD into ZnO TFTs is also discussed as they are integrated in ZnO TFTs used in this work. The rest of the chapter is devoted to the optimisation of the deposition parameters of ZnO semiconducting films, tailored to achieve electrically stable semiconducting properties.

5.2 Metal/Semiconductor Junction

The metal/semiconductor interface in semiconductor devices often results in the formation of a contact resistance (Schottky barrier (SB)) due to the depletion of the semiconductor side of the junction. Figure 5.1(b) and (c) show the energy band diagrams of a SB. The energies Wm and W_s are the work functions of the metal and semiconductor respectively, referenced from the vacuum level. In general, $W_m > W_s$, so that as soon as the contact is established between the two materials, (figure 5.2 b), electrons begin to flow from the semiconductor into the metal until equilibrium is reached (figure 5.2 c). The transient flow of carriers depletes the semiconductor surface region of electrons, leading to a downward bending of bands into the semiconductor. The amount of band bending is a function of the doping density in the semiconductor and can be used to control the depletion width and hence the barrier thickness, which determines the carrier tunnelling probability across the barrier [272].

Contact resistances (R_c) affect device performances through potential drops across the contact decreasing charge injection. R_c is often minimised in devices by heavy doping of the semiconductor at the near interface region, which decreases the depletion layer, enhancing the carrier tunnelling probability (leading to Ohmic contacts at the interface). For a semiconductor with doping density N; $R_c \alpha \exp(-N^{1/2})$ [273], so that R_c is very sensitive to the doping concentration.

Typical SB and Ohmic contact current-voltage characteristics are shown in figure 5.1a. In this work, Ohmic contacts of aluminium on silicon were achieved by 30 minutes annealing of 100 nm layer of aluminium at 950 ^{0}C in nitrogen.

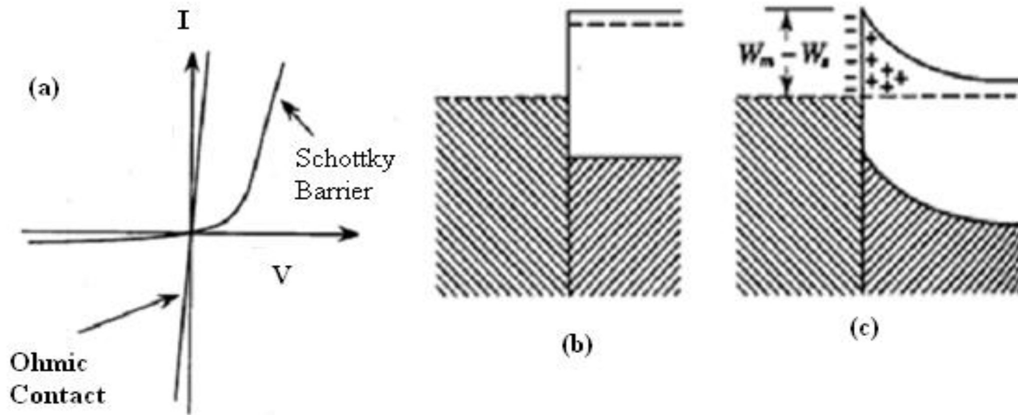


Figure 5.1 - (a) shows the current-voltage characteristics of a SB diode and an Ohmic contact, (b) energy band diagram of a metal/semiconductor juction device and (c) energy diagram of a metal/semiconductor after equlibrium is established (Modified from [272, 274]).

5.2.1 Contact Resistance and Drain Leakage

SBs formed at the metal/semiconductor junction have been one of the most important issues often found to degrade the performance of microelectronics devices. For proper in/out flow of current, ohmic contacts are essential. Ohmic contacts present minimal and negligibly-small contact resistance. A common technique often used to minimise SB in TFTs is to degenerately-dope the semiconductor close to the junction so that the SB formed is negligible compared to the resistance of the active channel material. As a consequence of this, the device characteristics are mainly determined by the active channel region.

O_2 adsorption on the (0001) ZnO surface increases back surface resistance (R_S) [275]. Furthermore, the adsorption leads to a surface reconstruction that modifies both

the electronic band structure and the surface electrostatic potential of the film (this has been examined in {§ 4.6}). This has been used in this thesis as a means to control the effects of contact resistance on the performance of TFTs, while assuming that the bulk properties of the film remain unaffected. As such, the contact resistance (R_c) becomes negligible compared to the channel resistance (R_{ch}). This is illustrated by equation (5.1) that has been defined as follows: if R_b is the bulk resistance of the film, the effective sheet resistance of a two-layer structure on an insulating substrate can be approximated by two resistors in parallel:

.... **(5.1)**

Furthermore, the drain leakage current due to the formation of conducting channels at the ZnO back channel surface is also expected to be improved considerably, leading to an enhanced overall performance. Any treatment that increases the surface resistance R_s, so that $R_s >> R_b$, does not affect the overall resistance of the channel, as $R_{ch} \longrightarrow R_b$. A similar technique has been employed recently by use of a double-layer passivation technique on amorphous-gallium-indium-zinc oxide (Ga_2O_3-In_2O_3-ZnO) TFT back channel, or by N_2O plasma treatment of the ZnO TFT back surface [276, 277].

5.2.2 Metal-Insulator-Semiconductor Field Effect Transistor

The structure of an *n-channel*, enhancement mode metal-insulator-semiconductor field effect transistor (MISFET), also called metal-oxide-semiconductor field effect transistor (MOSFET), as SiO_2 is the insulator of choice commonly used in

microelectronic devices is illustrated in figure 5.2. It is a three-terminal device and consists of a *p-type crystalline silicon* semiconductor substrate into which two degenerately doped n^+-type regions, used as the source (S) and drain (D), are diffused or implanted. In this section, the n-channel MISFET shall be discussed. A similar argument can be applied for a p-channel MISFET device. The gate contact (usually a metal or a degenerately doped poly-silicon) is separated from the semiconductor surface by a thin insulating layer of thickness d_{ins}. No current flows from drain to source without the formation of a conducting channel between them, since the drain-substrate-source combination comprises of two oppositely directed p-n junctions in series along the conducting channel (figure 5.2).

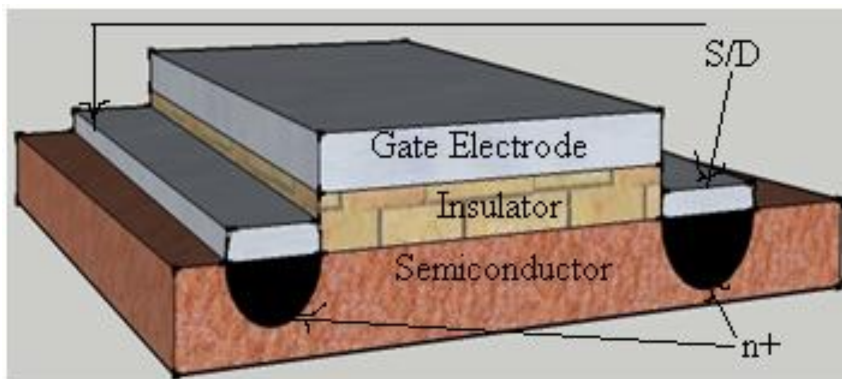


Figure 5.2 - Schematic of a MISFET structure.

When a positive voltage (V_{gs}) is applied to the substrate, negative charges are induced in the semiconductor at the insulator/semiconductor interface with the formation of a depletion region and a sheet (length L and width W; L is the S-D separation while W is the width of the gate electrode) of delocalised electrons in the semiconductor near the interface. These induced electrons form the conducting channel of the MISFET device.

The application of a drain-source voltage (V_{ds}), causes the electrons to move along the channel from the source to the drain giving rise to a drain-source current (I_{ds}). The electron mobility in the channel is greatly affected by interface scattering resulting in an effective mobility (μ_{eff}) that is less than the bulk mobility. The channel conductivity is modulated by the gate voltage through the capacitive coupling of the gate voltage with the gate insulator. Changes in gate voltage lead to changes in the induced charge density at the channel. For any given gate voltage, there exists a drain voltage (V_{sat}) for which the current reaches a steady state.

One of the most important figures of merit in MISFETs is the threshold voltage (V_T), which is the *minimum gate voltage required to induce a uniform channel*. For an n-channel device, the gate voltage must be more positive than V_T before a uniform conducting channel is induced. In the ideal case, when $V_{gs} = V_{ds} = 0$ V, the energy bands in both the insulator and the semiconductor are flat and the Fermi level is continuous at the interface (flat-band condition) and the threshold voltage in this case is the minimum voltage required to produce inversion. In a normal MISFET however, the effects of insulator fixed charge (Q_f), mobile charge (Q_m), interface states charge (Q_{it}) and the metal-insulator work function difference (Φ_{ms}) must be taken into account. As a result of these charges, some band bending at the interface already exists at $V_{gs} = 0$. Therefore, to achieve threshold, V_{gs} must be large enough to first re-instate the flat-band condition (V_{FB}), and accommodate the charge in the depletion region before inducing an inverted channel at the interface. TFT electrical characterisation is often achieved by using the well-established MISFET equations. Equations 5.2 to 5.5 show some of the most useful results governing the output current (I_{ds}) of MISFET devices.

In the linear regime ($V_{ds} << (V_{gs} - V_T)$)

– ………………………………………………… (5.2)

And in the saturation regime ($V_{ds} \geq V_{sat} \approx V_{ds} \geq (V_{gs} - V_T)$)

– ………………………………………………… (5.3)

Where C_{ins} is the capacitance per unit area of the insulator layer,

………………………………………..……….. (5.4)

………………………………………………... (5.5)

And ε_s, $\varphi_{B,}$ q and N_A are the semiconductor dielectric constant, band bending energy, elemental charge and acceptor charge density respectively.

5.3 Thin-film Transistor Structure and Operation

TFTs are often categorised into four main structural types: (a) the staggered, (b) the coplanar, (c) the inverted-staggered and (d) the Inverted-coplanar (these are shown schematically in figure 5.3). This nomenclature is based on the structural arrangement of the semiconductor, the insulating layer and the relative positions of S/D electrodes used for the fabrication. The staggered TFT structures have source-drain contacts on the opposite side of the semiconductor with respect to the gate electrode, while the coplanar structures have all three electrodes on the same side of the semiconductor.

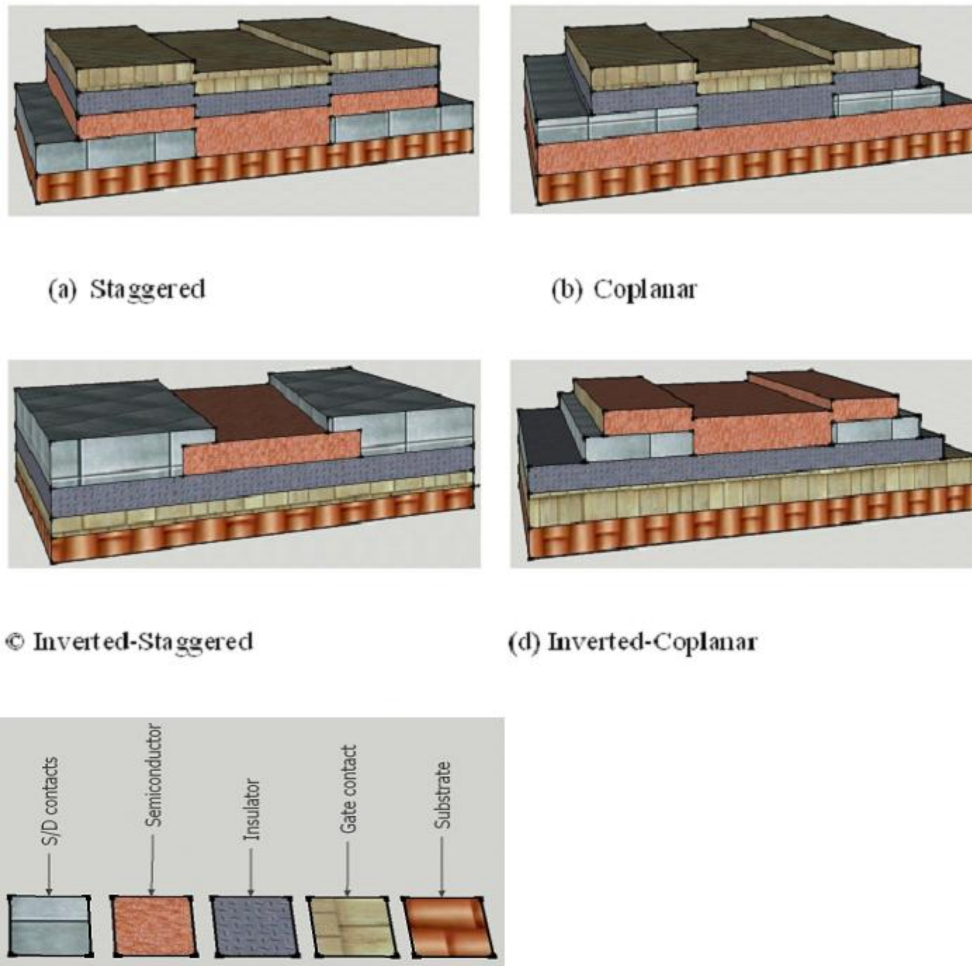


Figure 5.3 - Common TFT configurations

In this work, the inverted-staggered structure is used with an n^+-silicon substrate as a bottom gate due to its fabrication simplicity. Where a different structure and/or substrate (or gate electrode) is used, it is clearly stated. Aluminium (Al) has been reported to make good ohmic contacts on ZnO [278-282]. Figure 5.4 shows a typical IV characteristic of a ZnO film sputtered onto a glass substrate with Al electrodes of varying inter-electrode separations (L) produced in this work. The IV characteristic is linear and symmetrical, a clear demonstration that Al makes a viable ohmic contact with

the ZnO films deposited in this work. Thus, Al was used throughout this thesis as the source/drain electrodes of the ZnO TFT test devices.

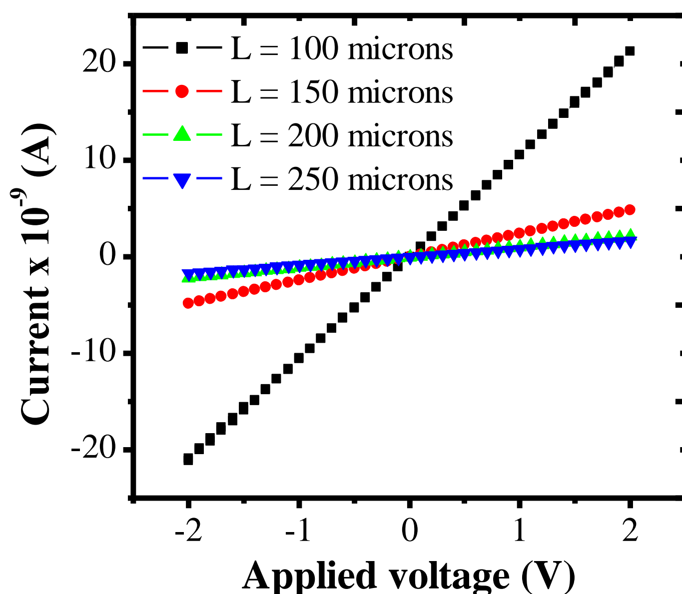


Figure 5.4 – Typical IV characteristics of ZnO films with aluminium contacts produced in this work, exhibiting Ohmic behaviour.

Ohmic contacts allow both holes and electrons to be injected equally at the source/drain contacts, increasing drain current leakage in TFTs. Degenerately doping the layer underneath the source/drain contacts n^+-type (or p^+-type), improves the transport of one of the carrier types, while causing a blocking effect on the other carrier type. As a consequence of this blockage, the TFT off-state current is improved and hence the on-off ratio is also improved. For the sake of simplicity and the fact that the aim of this work was to demonstrate performance/stability from the material point of view and not processing technique, this latter processing step was ignored in this work.

In the fabrication of the bottom-gated ZnO-TFT structure mentioned above, the insulator layer and the semiconductor (ZnO) are deposited consecutively onto the gate electrode. Aluminium source/drain electrodes are then patterned onto the ZnO layer using shadow masks (the complete step-by-step fabrication process can be found in appendix A). The finished TFT leaves the top surface of the ZnO active channel exposed to atmospheric ambient. Although ZnO has been reported to suffer from electrical instability in air, in this work we have tried to improve electrical stability via the optimisation of deposition parameters and post-oxygen treatment of the exposed surface in vacuum with the aim of eliminating the need for a surface passivation step.

In this work, the discussion of TFT operation is centred on n-channel TFTs; a similar discussion can be applied to p-channel TFTs. Figure 5.5 shows the energy band diagrams as viewed through the gate of an n-channel, accumulation-mode TFT [283]. The equilibrium band diagram shown in Fig. 5.5a assumes an ideal situation, where there is no charge in the semiconductor before the application of a gate bias and indicates that the semiconductor layer is slightly n-type. This gives rise to the flat band condition. If $V_{gs} < 0$, the gate repels mobile electrons and pushes them deeper into the semiconductor, leaving a depletion region near the interface. The positive space charge region near the semiconductor-insulator interface is consistent with the charge neutrality relationship such that the depletion charge in the semiconductor equals the charge accumulated on the gate electrode. The applied voltage is dropped across the dielectric and semiconductor layers, resulting in upward band-bending in the insulator and the semiconductor (near the interface). As the magnitude of the negative gate bias is increased, the depletion region moves further into the semiconductor. On the other hand, for $V_{gs} > 0$ V, electrons are attracted towards the interface, creating an

accumulation layer (leading to the formation of a conducting channel) near the interface. The associated energy band diagram exhibits downward band-bending in the insulator and the semiconductor (near the interface), as shown in Fig. 5.5b. Increasing the gate bias modulates the conductivity of the surface layer as shown by the greater band bending.

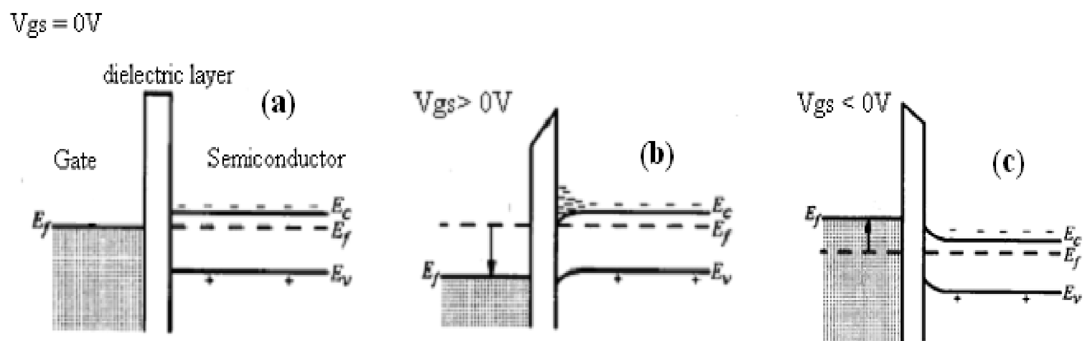


Figure 5.5 - The energy band diagrams for (a) equilibrium, (b) accumulation and (c) depletion conditions.

Once the channel formation has been established, the application of a positive voltage on the drain attracts electrons towards the drain electrode leading to current I_{ds} flowing from drain to source.

5.4 Optimisation of the ZnO Semiconductor for TFTs

The electrical resistivity of ZnO thin films measured using the TLM described in {§ 3.5} was used as the primary optimisation parameter. The ZnO thin films were sputtered under varying deposition conditions of RF power and O_2/Ar ratio (measured

as the ratio of O_2 flow rate to that of the Ar flow into the sputtering chamber). In order to reduce the variations in film properties as a result of differences in thickness, films investigated were sputtered to approximately the same thickness (~ 150 nm). Thin film electrical resistivity ($_f$) is known to depend on the film dimensions as in equation (5.6) [284]. Furthermore, ZnO thin film thickness has been found to influence ZnO TFT performance parameters such as mobility, threshold voltage and turn-on voltage [285, 286].

– – ………………..…..…………....…….. (5.6a)

– – – ……………………..……..…...……….. (5.6b)

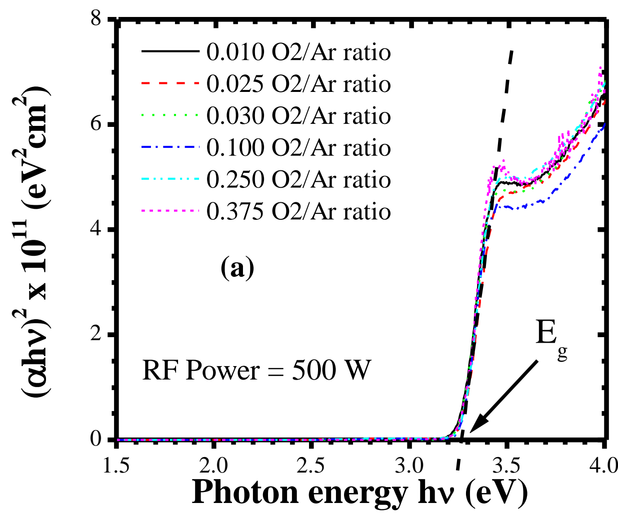
The parameters d and l are the film thickness and length (inter-electrode separation) respectively.

5.4.1 Optimisation of ZnO Thin Films

In this thesis, ZnO films are deposited on to either n^+-silicon or glass substrates by reactive RF magnetron sputtering. Ar and O_2 were used as the sputtering gases. The flow rates of the gases were varied between 8 – 20 Sccm and 0.2 – 3 Sccm for Ar and O_2 respectively. The sputtering source used was an 8 inch diameter ZnO target with 99.999% purity (Kurt J. Lesker) at a substrate distance of ~6 cm. The RF power was varied between 25 – 500 W and the chamber was always pumped down to a base pressure below 4.0 x 10^{-6} Torr prior to the deposition. The sputtering system used and some of its peripheral devices is depicted in Figure 3.4 of {§ 3.3.4}.

5.4.2 Parameter Variation

The flow of O_2 into the sputtering chamber was varied from 0.2 to 8 Sccm while that of Ar was varied from 8 to 20 Sccm. The resolution of the mass flow controllers (MFCs) used was 0.1 Sccm. The optimisation was completed via a full two-level factorial design while varying the RF power between 25 and 500 W involving three factors (RF power, and O_2 and Ar flow rates). Figures 5.6 – 5.9 show the variation of film electrical resistivity and optical transparency with sputtering parameters. The transmission data of the ZnO films sputtered in this work showed that the effect of O_2/Ar variation on the bandgap of the films was less than 15 meV (figure 5.6).



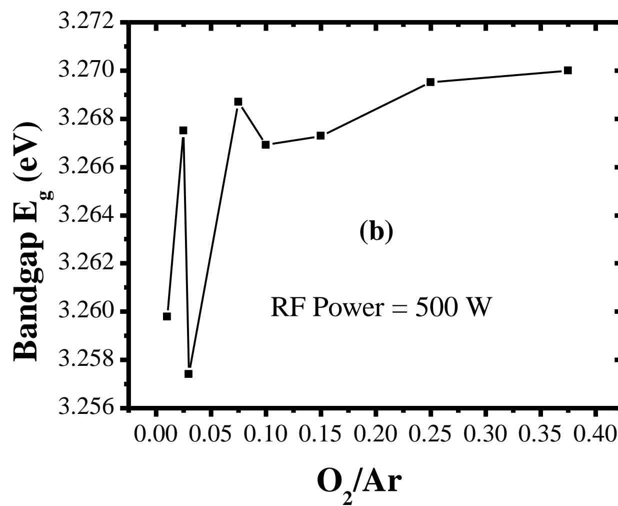


Figure 5.6 - The dependence of: a) absorption coefficient and b) optical bandgap of sputtered ZnO thin films on the O_2/Ar ratio for an RF power of 500 W.

The contour plots (figures 5.7 and 5.8) show the dependence of ZnO film resistivity and averaged transmission in the visible regime (400 – 700 nm) on deposition parameters. It is observed that both the film resistivity and averaged transmission

generally increase as the O_2/Ar ratio increases. Increased resistivity in ZnO is often ascribed to an increase in the grain boundaries (reduction in grain size), or a consequence of a reduction in the intrinsic point defects (Zn_i or V_O) [287, 288]. Moreover, as the transparency also improves with O_2/Ar, it is possible to speculate that the crystallinity of the films will also improve with O_2/Ar ratio.

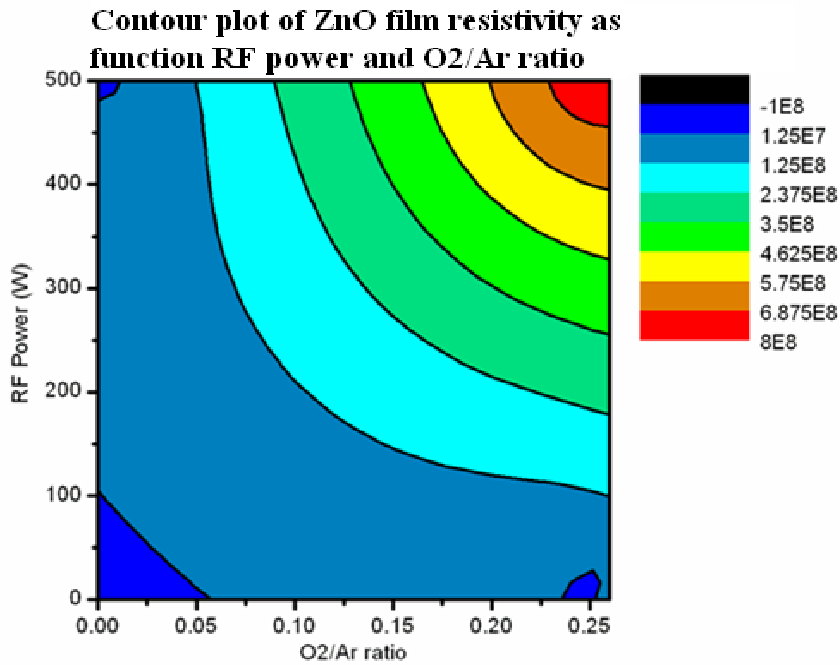


Figure 5.7 – Contour plot of film resistivity as a function of sputtering parameters.

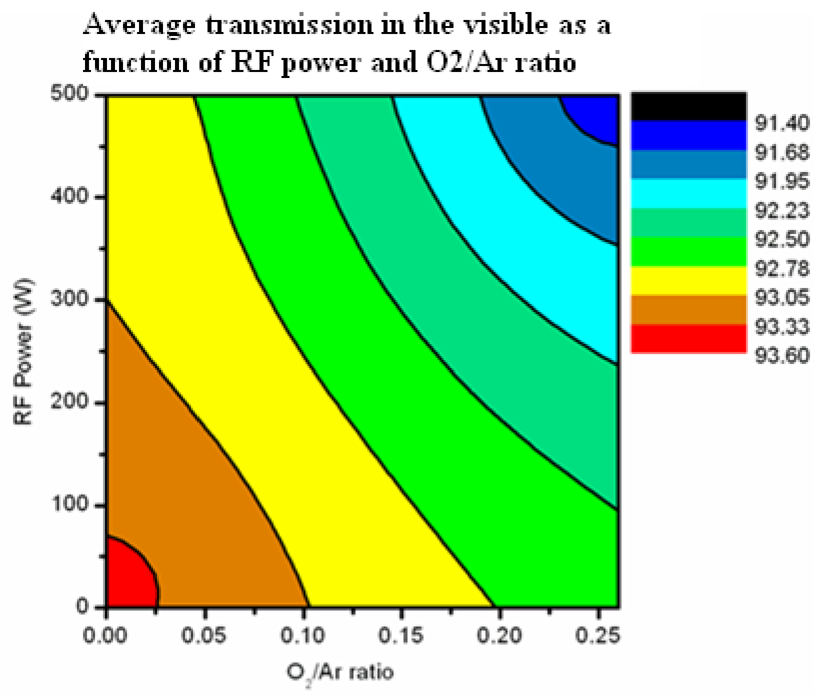


Figure 5.8 – Contour plot of ZnO film transparency as a function of sputtering parameters.

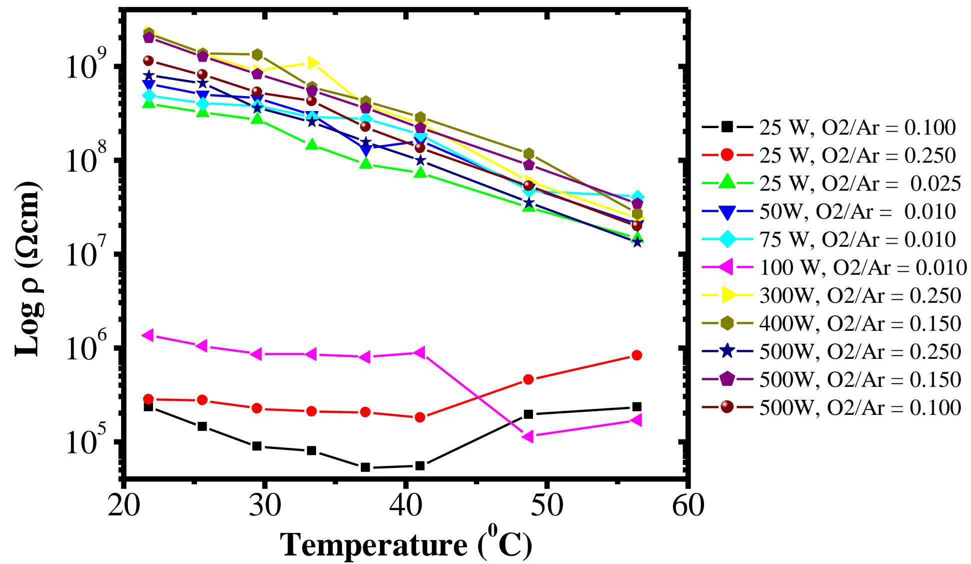


Figure 5.9 – The dependence of ZnO film resistivity on measurement temperature and sputtering parameters.

The electrical conduction mechanism in ZnO at temperatures above 200 K including room temperature, has been reported to be dominated by temperature activation and by thermal emission (activation energy (E_A) in the range of 150 - 650 meV) [289, 290]. The dependence of electrical resistivity on temperature (295 – 330 K) is studied in this work as shown in figure 5.9. The Arrhenius plots of the electrical resistivity of most of the films are linear on a semilog plot, an indication that the activation energy is dominated by a single defect type with an exponential distribution of shallow levels within the temperature range studied. The activation energy of these films varies between 30 – 50 meV as shown on table 5.1, similar to those observed by Litton [291]. High O_2/Ar ratio produces films with deeper levels. The films that follow an Arrhenius plot with a linear relationship also exhibit high resistivity. High resistivity ZnO films are often nearer to stoichiometry, less defective and highly transparent [288].

High power (such as 500 W) deposition of ZnO in the bottom-gate TFT configuration, as used in this work, is detrimental to the underlying dielectric layer, and could result in a possible increase in gate leakage current across the gate insulator. However, for films deposited at low power (such as 25 W), although minimal damage is expected on the dielectric surface, the Arrhenius plots of the film resistivity do not follow logarithmic relationships. Some of the films even exhibit resistivity increases with temperature. In such films, electrical transport is likely to be dominated by phonon scattering. However, as the film resistivity also depends on the O_2/Ar ratio, the film produced at a power of 25 W and an O_2/Ar = 0.2/8 is seen to be a possible compromise as it shows a linear Arrhenius plot parallel to those of films deposited at high RF power (500 W) and also exhibiting a high resistivity (suggesting that it is likely to have a low defect density). The packing fraction of all the films exhibiting a linear Arrhenius relationship is more than 0.9 (table 5.1), clear indication of high density.

Table 5.1 – The Activation energy, refractive index and packing fraction of films that show a linear Arrhenius relation on a semilog scale.

RF power (W)	**O_2/Ar ratio**	**E_A (meV)**	**Refractive index**	**Packing Fraction**
25	0.025	37	1.992	0.989
50	0.010	38	1.954	0.964
75	0.010	30	1.968	0.973
300	0.250	50	1.963	0.970
400	0.150	46	1.965	0.971
500	0.025	45	1.970	0.975
500	0.150	44	1.952	0.962
500	0.100	44	1.931	0.948

5.5 Electrical Characterisation of TFTs

5.5.1 The thin film Transistor Structure

Figure 5.10 shows the TFT configuration used in this thesis for TFT fabrication. In this inverted staggered structure, a highly doped n^+-silicon was used as bottom gate.

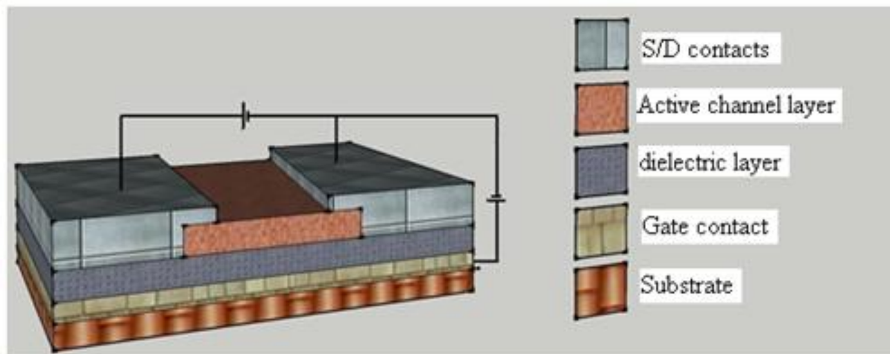


Figure 5.10 – The Conventional Bottom Gate Inverted-Staggered TFT structure

5.5.2 High-k dielectrics

This section elucidates the properties of high-k dielectric materials and why their integration into ZnO TFT fabrication can be a useful route to improve performance with reduced bias stress instability issues. In this work, the following high-k dielectrics have been investigated: hafnium oxide (HfO_2), Gadolinium oxide (Gd_2O_3) and Yttrium oxide (Y_2O_3).

5.5.2.1 Motivation for High-k Dielectrics in ZnO TFTs

Materials whose dielectric constant is greater than that of the traditional silicon dioxide (SiO_2) are known as '*high-k dielectric materials*'. In recent years, researchers have focused on high-k dielectric materials as an alternative to SiO_2 in highly-scaled electronic devices [292-296]. From equation (5.7) below, it is clear that high-k materials will provide the same capacitance as SiO_2, but with a larger thickness, which will reduce gate leakage current in highly-scaled semiconductor devices.

……………………….......………...………………………. (5.7)

where C_{0x}, k_{ox}, t_{ox} are SiO_2 capacitance per unit area, relative dielectric constant and dielectric layer thickness respectively. $C_{high\text{-}k}$, $k_{high\text{-}k}$, $t_{high\text{-}k}$ are the corresponding parameters for a high-k material and ε_0 is the vacuum permittivity.

The equivalent oxide thickness (EOT) is calculated using the two equations in (5.7), for $C_{ox} = C_{high\text{-}k}$. The relationship between the dielectric constant of the high-k and SiO_2 is usually expressed in terms of the EOT, as shown by equation (5.8). The EOT is the thickness of a pure SiO_2 layer that will provide the same gate capacitance as the high-k layer.

$$EOT = \left(\frac{k_{ox}}{k_{high-k}} \right) t_{high-k} \quad \text{(5.8)}$$

One of the major drawbacks of the ZnO TFT is the large threshold and hence large operating voltage in comparison to a-Si:H TFTs [297-300]. Furthermore, ZnO

TFTs also suffer from threshold voltage instability issues resulting from prolonged gate bias stress [41]. To reduce the operating voltage of the transistor, one must increase the coupling of the gate electric field to the channel layer. This can be done by either reducing the gate dielectric thickness or by using a gate dielectric material with higher dielectric permittivity (high-k gate dielectric) [301]. Both solutions strive to increase the gate capacitance; however, high-k materials present a more promising solution since a thicker high-k layer maybe used to produce an equivalent capacitance that would have otherwise require a very thin and leaky SiO_2 layer. Another benefit associated to high-k integration in TFTs is the fact that by using a thicker dielectric layer, this would lead to a reduced gate field at the interface and consequently reduce the effect of gate bias stressing on the threshold voltage. The use of thicker high-k dielectric layers also reduces gate leakage current without compromising the induced interface charge density. Furthermore, the large capacitance that results from high-k dielectric layers also means a higher carrier density can be accumulated at the ZnO/dielectric interface, even at small gate voltages; this would greatly reduce the operating voltages and thus reducing even further the effect of gate bias electrical stressing that could be a consequence of prolonged operation.

High-k dielectric films used in this work (HfO_2, Gd_2O_3 and Y_2O_3) were deposited by MOCVD [166, 302] (at a temperature of 400 ^{0}C) and supplied through collaboration with Prof. Anjana Devi and Andrian P. Milanov of the Inorganic Materials Group, Ruhr-University Germany.

5.6 Summary

In this chapter, the structure and electrical characterisation of different thin film interfaces have been discussed. The main operational features of TFTs have been briefly discussed and the different TFT configurations commonly used are presented. The integration of different high-k dielectrics in ZnO TFTs has been investigated and proposed as an alternative route to reducing electrical instability in ZnO TFTs under prolonged electrical stress bias. In addition, the ZnO optimisation process and ZnO TFT device fabrication have been presented.

Chapter - 6

Fabrication and Electrical Characterisation of ZnO TFTs

6.1 Introduction

This chapter is devoted to describing the electrical measurement system and the procedure used to assess ZnO TFT static performance and stability. The main figures of merit include: the threshold voltage (V_T), the turn-on voltage (V_{on}), the sub-threshold slope (S) and the effective mobility (μ_{eff}). The technique used to identify and quantify the gate bias stress related instability mechanism is also discussed. ZnO TFTs using an engineered dielectric layer have been reported to improve electrical stability at low operating voltages [303]. As high-k dielectrics result in enhanced gate capacitance and hence an increased concentration of the induced channel charge, they are a suitable choice for low voltage applications. They therefore offer an alternative route to improve electrical stability in ZnO TFTs.

6.2 Electrical Characterisation of TFTs

6.2.1 Transfer Characteristics

From the bottom-gate TFT structure {§ 5.5} considered in this work, when $V_{gs} > 0$ V, the energy bands in the ZnO semiconducting channel layer bend downwards at the ZnO/dielectric interface drawing electrons into the channel region from the source and

drain contacts. An application of a bias at the drain electrode, results in a flow of current I_{ds} from the drain to the source.

The transistor transfer characteristics (I_{ds}-V_{gs}) provide a means to quantitatively measure the performance of the TFT device. Figure 6.1 shows a typical transfer characteristic of a ZnO/Gd_2O_3 TFT operating in the linear regime. Many performance parameters of TFTs are extracted from I_{ds}-V_{gs} relations by modifying the traditional MOSFET equations of {§ 5.2}. These parameters include amongst others: the inverse sub-threshold slope S, the turn on voltage V_{On}, the threshold voltage V_T, the drain current On-Off ratio I_{On-Off}, and the effective channel mobility μ_{eff}.

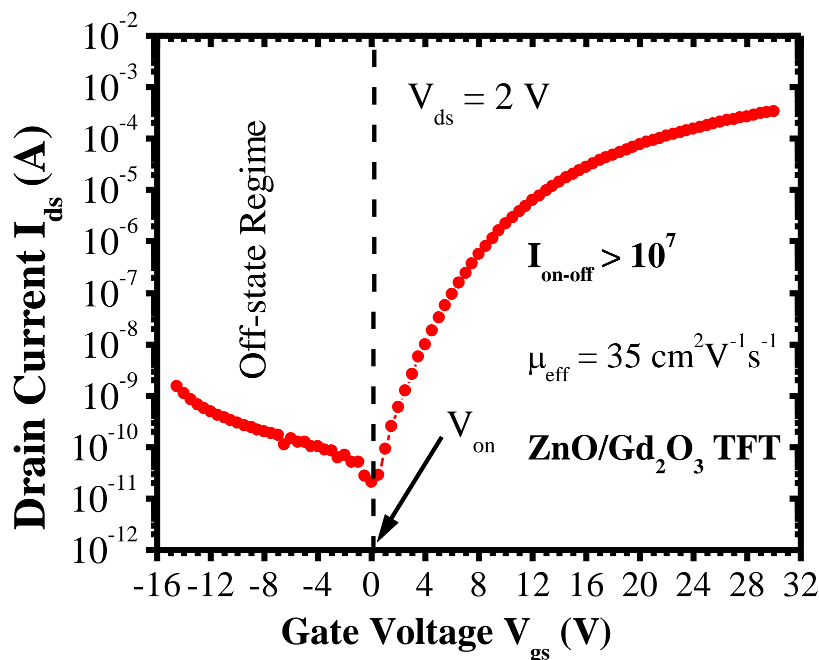


Figure 6.1 – Transfer characteristic of a typical ZnO/Gd_2O_3 TFT fabricated in this work.

6.2.2 The Inverse Subthreshold Slope, On-Off Current Ratio and Turn-on Voltage

The subthreshold (S), On-Off ratio (I_{On-Off}) and turn-on voltage (V_{on}) are extracted from the semilog plot I_{ds}-V_{gs} plot as follows [304]:

…………………………..…..………. (6.1)

where T is the ambient temperature, q is the elemental electronic charge, C_{ins} is the insulator capacitance and C_{dm} is the depletion capacitance. Since the depletion capacitance is in parallel with the interface capacitance, S also provides information on the density of interface traps N_{ss}. This can be estimated by [141, 304];

……………………………………...…………… (6.2)

S is thus a useful quantity that provides information on how fast a device turns on. It is typically between 70-100 mV/dec for an ideal MOSFET [304]. A subthreshold of 210 mV/dec has been reported for a good quality ZnO TFT on silicon nitride (SiN) dielectric [305]. In this work, equation (6.2) is used to characterise the ZnO interface on different dielectrics in the TFT structure.

The I_{On-Off} current is the ratio of the On-current to the Off-current and is a useful parameter for switching applications and a useful figure of merit for performance assessment, as it is directly affected by insulator leakage via the reduction of carrier density in the channel.

V_{On} is extracted as the gate voltage at which the drain current just begins to increase monotonically with increasing gate voltage, and corresponds to the minimum current on a semilog plot. This parameter is related to the amount of background charge in the semiconductor (delocalised charge that exists in the semiconductor prior to depletion) and to the threshold voltage.

6.2.3 The Effective Channel Mobility and the Threshold Voltage

The effective channel mobility (μ_{eff}) and threshold (V_T) of TFTs are often extracted using modified equations of the well-known metal-insulator-semiconductor field effect transistor (MISFET) {§ 5.5}. The μ_{eff} is the average mobility experienced by a charge carrier in the device active channel, taking into account all possible scattering mechanisms (phonon, ionized impurity, interface, and grain boundary scattering) according to Mathiessen's rule as in {§ 3.5}.

μ_{eff}, therefore, provides a means to measure current drive, and the switching rate of a FET and so it is often considered a very important figure of merit for device performance assessment. Several methods are often used to extract the effective channel mobility using the MISFET drain current equations. The μ_{eff} is obtained using the linear (sub-threshold) region of the I_{ds}-V_{gs} relation while the saturated mobility μ_{sat} is obtained from the I_{ds}-V_{gs} relation in the saturation regime (equation 5.2 - 5.3). In this work, all μ_{eff} values reported have been evaluated from the linear regime. Figure 6.2 shows a typical I_{ds}-V_{gs} plot of a ZnO/Gd_2O_3 TFT operating in the linear regime.

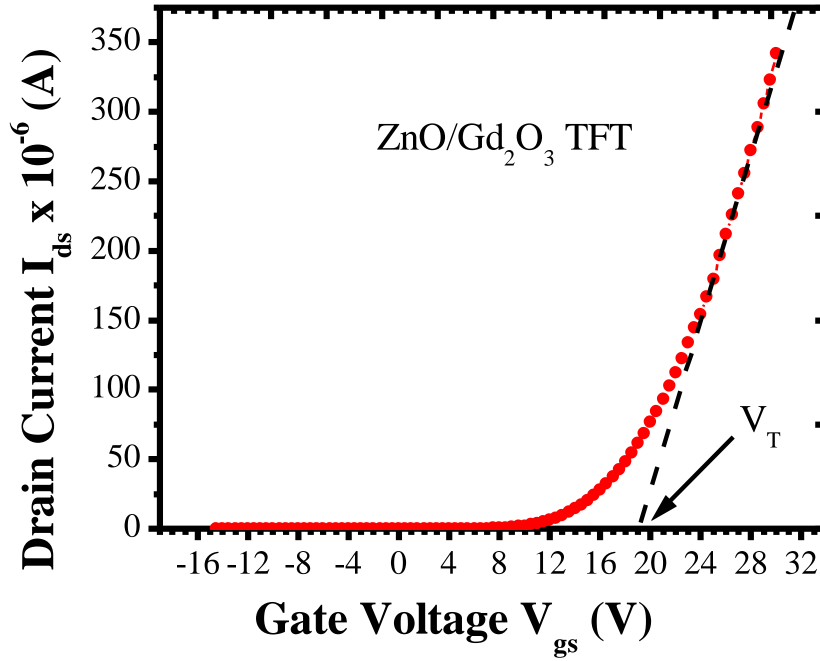


Figure 6.2 – Transfer characteristic of a Typical ZnO/Gd2O3 TFT, illustrating the extraction of threshold voltage.

6.2.4 The Time Dependence of $\Delta\mu_{eff}$, ΔV_T, ΔV_{on}, S, and $I_{On\text{-}Off}$ on Gate Bias Stressing.

Following the fabrication of a TFT, an initial transfer characteristic was measured using a fast voltage ramp (2 V/s). The TFT was then gate bias stressed for a maximum period of 10^4 s at room temperature (~300 K). During the gate bias stressing, both the drain and source were grounded and an equivalent bias voltage of ±10 V on 100 nm of SiO_2 (i.e. E_s = 1 M/cm, similar to the stress field values used by Kattamis et al. [306]) was applied to the gate electrode and the source-drain current was sampled at intervals of t = 10^1, 10^2, 10^3, 10^4 s. The positive and negative bias stress assessments

were performed on different TFT devices to avoid the effects of damage or changes in TFT properties after a given stress test has been carried out. The threshold voltage and turn-on voltage shifts, induced as a consequence of the gate bias stress, caused variations in the source-drain current. By extracting the μ_{eff}, V_T, V_{on}, S and $I_{On\text{-}Off}$ ratio at time t, and comparing with their corresponding values extracted from the initial device transfer characteristics prior to bias stress application, the dependence of these parameters on time under the specified gate bias stress condition is obtained.

6.2.5 Output Characteristics

The output characteristics (I_{ds}-V_{ds}) are often used to extract qualitative information about the TFT characteristics. Current saturation is an indication that the active channel semiconductor layer can be fully depleted of charge carriers with the bias voltage at which saturation is observed. Thus, they provide a means of quantitatively estimating the doping level of the active channel layer. Furthermore, in the low voltage regime, the I_{ds}-V_{ds} relation is expected to be linear, following Ohms' law. A significant deviation from linearity (current crowding at the origin) is an indication of poor electrical contacts (non-Ohmic contacts) at the source/drain regions. Figure 6.3 shows a series of output characteristics for a typical ZnO/Gd_2O_3 TFT investigated in this work.

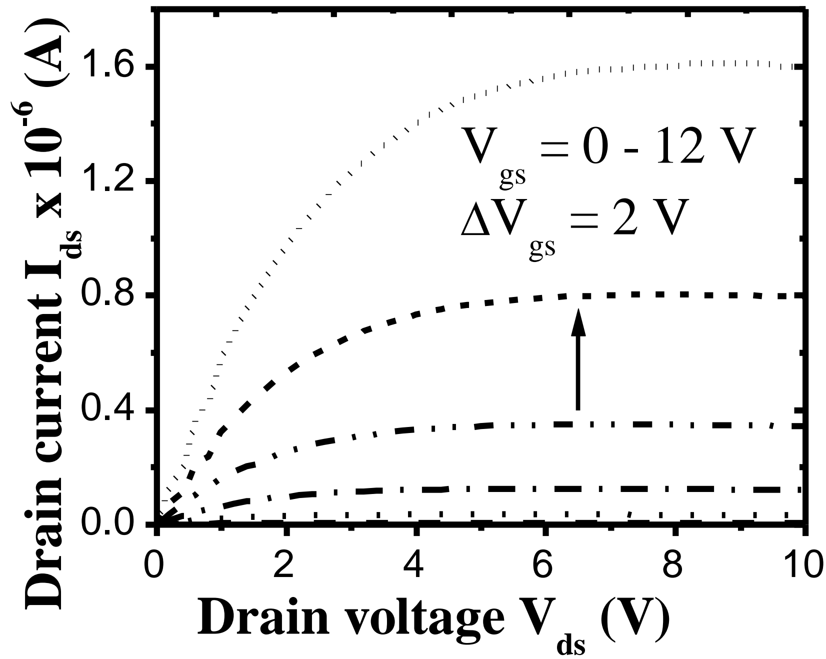


Figure 6.3 – Output characteristics for a typical ZnO/Gd_2O_3 TFT fabricated in this work.

6.3 ZnO TFT Fabrication

The ZnO TFTs fabricated in this work were bottom-gate inverted staggered devices. This structure was selected because of its fabrication simplicity and the fact that the processing temperature of the underlying dielectric is much higher than that used to sputter the ZnO channel layer. All devices were fabricated on degenerately doped n^+-type, 0.025 Ωcm, <100>, 4′′ crystalline silicon (c-Si) wafers, which served both as the substrate for the gate dielectric (thermally grown or by MOCVD) and as a distributed gate contact for all the devices, leading to a simplified fabrication process. The electrical contact to the c-Si gate was made via a piece of aluminium foil which was attached by silver paste.

In this work, as only one ZnO TFT device was tested at any one time, the ZnO channel layer was deposited un-patterned (distributed semiconductor layer for all the devices) on the dielectric layer over the whole c-Si wafer. This again greatly reduced the processing steps. Aluminium source/drain electrodes were then deposited by thermal evaporation patterned using shadow masks to complete the ZnO TFT fabrication process. Figure 6.4 shows a 3D diagram of a completed ZnO TFT device. All devices investigated had a channel length (L) of 100 µm and channel width (W) of 1000 µm leading to a W/L ratio of 10:1.

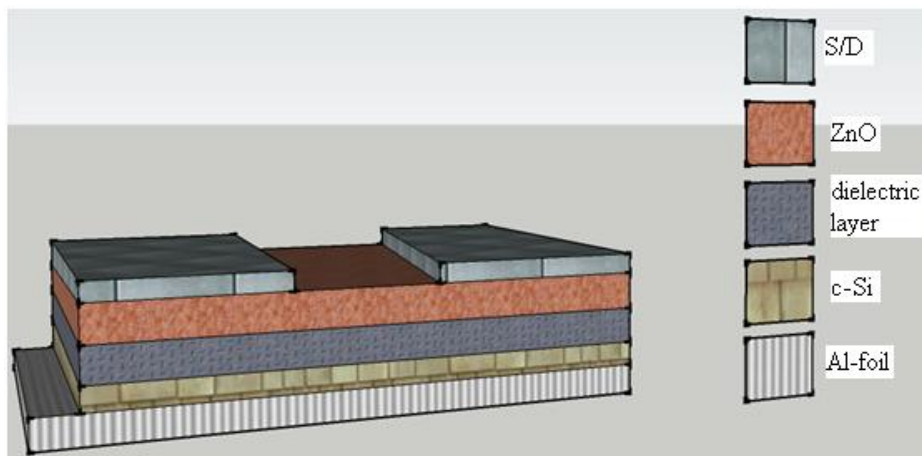


Figure 6.4 - Bottom gate ZnO TFT Test Structure.

Apart from the simplicity in fabrication offered by the above structure, it also allows for the S/D contacts to be deposited immediately after the ZnO has been deposited, reducing the level of ZnO surface contamination. In addition, no lithographic steps or chemicals are involved, and so the possibility of contamination to the ZnO layer during processing could be reduced. The area of the S/D electrodes as defined by the shadow mask was 4 mm^2. The large overlap of the distributed gate with S/D regions

increases the parasitic capacitance of the device. This may greatly reduce the S/D series resistance [307] and in some cases can improve the On-current. For active matrix switching applications, envisaged for LCDs and other switching applications, the large parasitic capacitance may slow down the TFT switching speed, affecting its operation. However, for this work, the TFT structure used here was adequate for the performance and stability assessment set out in the thesis objectives.

6.4 ZnO TFT Electrical Measurement Setup

The electrical measurement setup used to determine the static characteristics and gate bias stress stability of the ZnO TFTs and dielectric integrity is shown in figure 6.5. The measurements were controlled remotely via a VEE program (written by the author), with defined input parameters. For TFT static measurements, the output voltages (V_A and V_B) of the HP4140B are connected to the gate (G) and drain (D), and the source/drain current (I_{ds}) is measured. Controllable voltage ramps were supplied to G or D to measure the transfer and output characteristics respectively. For bias stress measurements, the gate is biased to the required stress voltage, while the drain is grounded for a given stress time; at the end of which, the stress bias is turned off and an appropriate drain voltage (V_{ds} = 2 V) is set and the transfer characteristics measured. Prior to any measurements, a gate leakage assessment was performed to ensure that the current is not dominated by gate leakage currents (L_g) across the dielectric and ensure that the dielectric is of device quality standard. This was performed by electrically connecting the S/D together; grounding them and applying a 30 V (the maximum gate voltage reached during the TFT electrical assessment) at the gate and only devices with

$L_g \leq$ 100pA were used for further assessment. The electrical measurement process was performed in an electrically grounded, light-tight probe station equipped with tungsten tip microprobes.

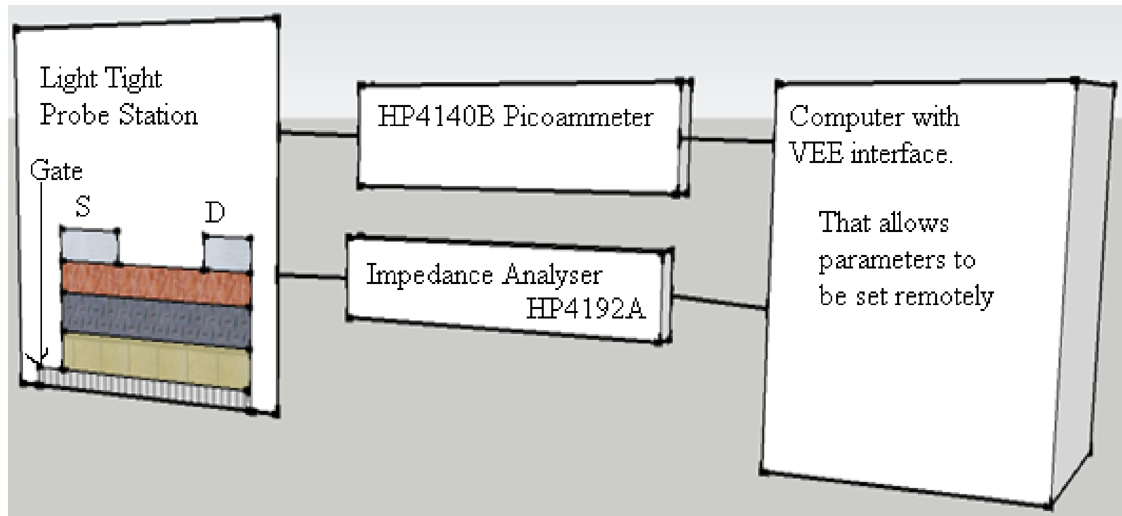


Figure 6.5 - TFT and gate dielectric layer electrical measurement setup

6.5 ZnO Channel Thickness Optimisation for TFT Performance

The S/D series resistance in FET devices is often determined as a sum of the source contact resistance (R_S), the drain contact resistance (R_D) and the channel resistance (R_{ch}). As a consequence of the S/D contact resistance, current crowding at the source in the vicinity of the channel gives rise to the spreading resistance (R_{sp}). A first order approximation of R_{sp} is often given by the analytical expression (6.3);

—— — .... (6.3)

where W is the channel width, the source-drain resistivity, x_j the junction depth, x_{ch} the channel thickness and is a scaling factor [159, 308]. In physical terms this means both the doping concentration and the channel thickness can be used to modulate R_{sp} and hence the device performance. ZnO channel thickness has already been reported to be a useful parameter for modulating performance and off-state leakage currents in TFTs [309, 310]. For TFT applications, the channel thickness is related to off-state leakage current ($I_{ds\text{-}off}$) when $V_{gs} = 0V$, according to equation (6.4).

— ……………………………………………..………..…….. (6.4)

where is the electrical conductivity of the film, and all other parameters are as previously defined.

In this work, the ZnO channel thickness was optimised using a SiO_2 dielectric for performance and gate bias stress stability. The main figures of merit used for this optimisation process were μ_{eff}, V_T and V_{on}. The $I_{On\text{-}Off}$ {§ 6.2} is greatly influenced by the $I_{ds\text{-}off}$ of the TFT, which is an important performance parameter, especially when the TFT is used for switching applications. Therefore, according to equation (6.4), there is a need to optimise the thickness (d) of the ZnO channel in order to reduce the off-state leakage current. The ZnO thicknesses investigated in this work were between (20 – 60 nm) and deposited by reactive magnetron RF sputtering.

6.6 Bias Stress Instability in TFTs

The tracking of threshold voltage shifts in TFTs under prolonged application of gate bias has been greatly used to study instability in a-Si:H TFTs. Mobile ions, such as Na^+ [311, 312] or OH^-, H^+ water related ions [313, 314], induce a positive threshold shift (ΔV_T) with a negative stress bias, and a negative shift with a positive stress bias, with no change in sub-threshold slope or sheet conductance. Charge trapping at high gate bias in the dielectric [315, 316] has been reported to induce a positive ΔV_T with a positive gate bias stress and a negative shift with a negative gate bias stress, while the sub-threshold slope (S) remains unchanged. Bias stress related state creation in the bandgap of a-Si:H is also reported to induce instability in a-Si:H TFTs [317, 318]. In this case, a positive ΔV_T is observed for n-type silicon and a negative shift for p-type. States created in the upper half of the bandgap induce an increase in S in n-Si TFTs, whereas states created in the lower half of the bandgap in p-Si TFTs also increase S [319-322], and the ΔV_T follows a logarithmic power law with time. States creation instability has also been suggested in ZnO TFTs [323]. The different charge trapping mechanisms at or near the interface of ZnO TFT is illustrated in the energy band diagram of figure 6.6.

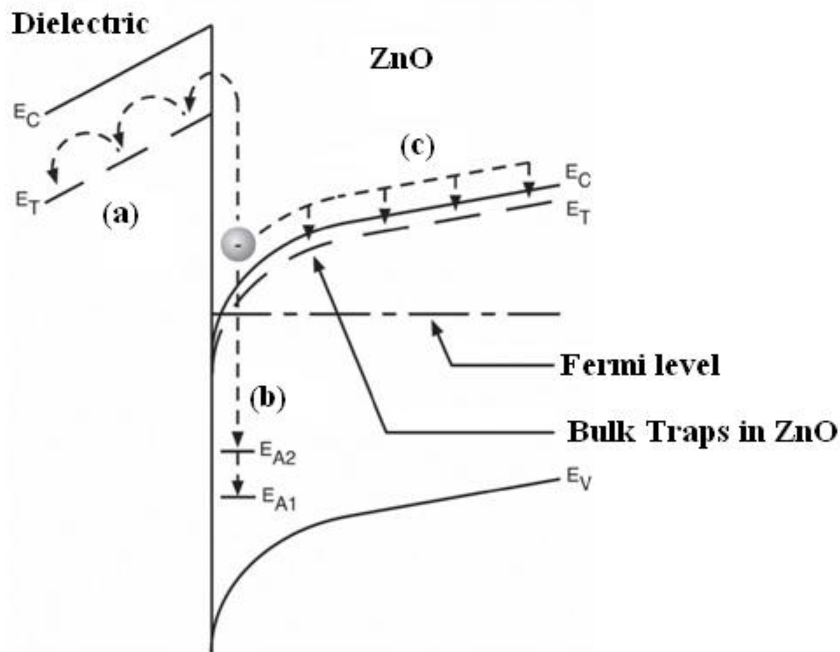


Figure 6.6 - Energy band diagram of a ZnO TFT, illustrating three instability mechanisms: (a) Electron injection and trapping within the gate dielectric, (b) deep state creation for the explicit case of V_{Zn} and (c) electron trapping within the ZnO active channel layer (modified from [319]).

In a-Si:H TFTs, insulator charge trapping induced by gate bias stress, requires that the equivalent surface field E_s at the insulator/semiconductor interface is about 1 MV/cm [321]. In this work, E_s was defined as in equation (6.5), so that the influence of the interface field resulting from dielectric layers with different thicknesses and dielectric constant could be compared.

——— …………………………………………………………………………… (6.5)

d_{ins} is the dielectric layer thickness, V_{gs} the TFT gate bias, and ε_{SiO2} and ε_{ins} are the dielectric constants of SiO_2 and gate insulators respectively. In this work, the gate bias stress voltage (V_{gs}) has been scaled to generate E_s= 1 MV/cm, irrespective of the dielectric constant. This ensures that the same quantity of charge is induced at the semiconductor/insulator interface during the stress period.

6.7 Summary

In this chapter, the TFT structure used in this thesis is presented and some of the important figures of merit commonly used for TFT electrical characterisation are also discussed. The dependence of ZnO TFT performance and electrical instability, and the role of the gate insulator on bias stress instability are also described.

Chapter - 7

Results and Discussion on the Performance and Stability of ZnO TFT

7.1 Introduction

In this chapter, ZnO TFT performance and gate bias stress electrical instability is discussed. The performance and stability of ZnO TFTs incorporating different dielectrics, including high-k dielectrics (Gd_2O_3, HfO_2 and Y_2O_3) produced by MOCVD are discussed and compared with SiO_2-based ZnO TFTs. In addition, the ZnO TFTs are optimised for performance with respect to the ZnO layer thickness.

7.2 Experimental Optimisation of ZnO Layer Thickness for TFT Performance

The structural, optical and electronic properties of ZnO layers are strongly influenced by the layer thickness [83-87]. As result of this, the ZnO active channel of the ZnO TFT test device was optimised for thickness and performance.

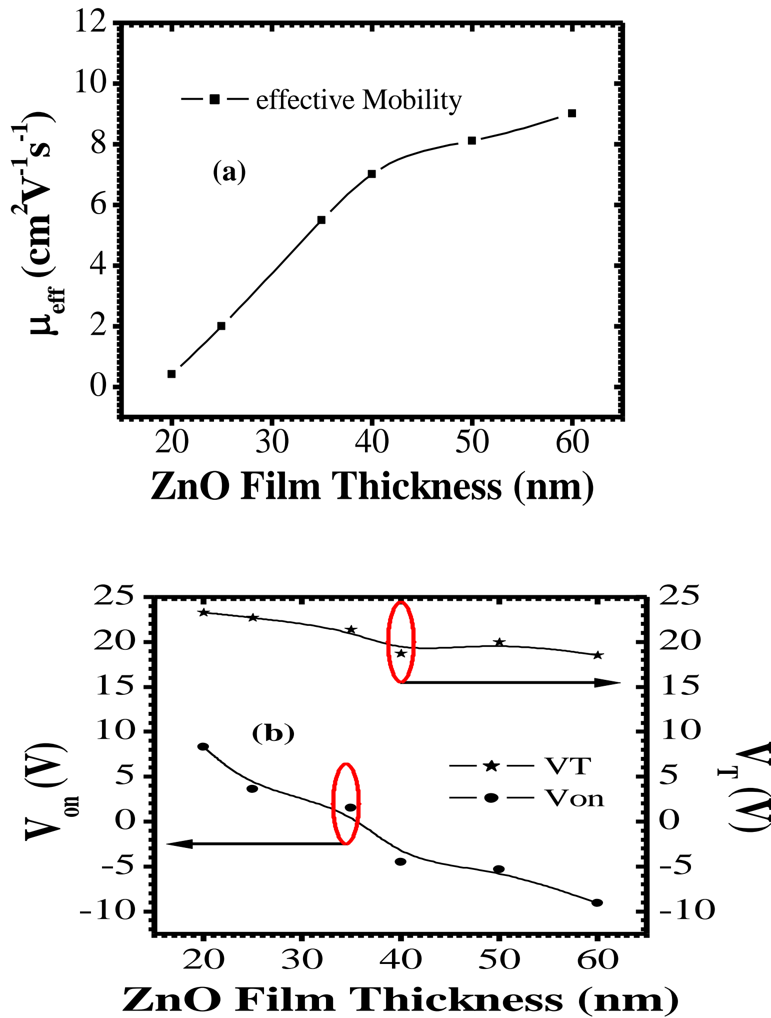


Figure 7.1 – Dependence of ZnO TFT: a) channel mobility and b) threshold/turn-on voltage shifts, on ZnO layer thickness.

Figure 7.1 shows the variation of V_{On}, V_T and μ_{eff} with thickness for ZnO TFT incorporating SiO_2 dielectric. Using a temperature of 950 ^{0}C, 100 nm thick films of SiO_2 with a refractive index of 1.457 were thermally grown on n^+-silicon (serving as a bottom gate). The growth rate was found to be 1.32 nm/min and a dielectric strength of ~ 8.25 MV/cm (measured when a leakage current of 100 pA was reached) with a

dielectric constant of 3.3. It is observed that the effective channel mobility increases monotonically with channel thickness (figure 7.1a). Similar to observations reported for un-doped ZnO and other ZnO derivatives, a-Si:H and other semiconductor TFTs, V_T and V_{on} decrease with increasing channel thickness [84, 85, 87, 120-126, 324, 325]. For films used in this work, both V_{On} and V_T also decreased with ZnO layer thickness. After 40nm, the decrease in V_T becomes negligible (figure 7.1b). One possible cause may be that the crystallinity and grain sizes are improved [286, 326-328]. This results in the reduction of grain boundary scattering, and hence the carrier mobility increases. As a consequence of improvements in the film crystallinity, the voids and defects in the films are reduced leading to the release of trapped or bound carriers [329]. Thus, the carrier concentration increases and is manifested as variations in V_{On} (or V_T). In addition V_{on} varies much more than V_T and so has been considered a more sensitive parameter for electrical instability assessment.

7.2.1 Performance and Gate Bias Stress Instability Assessment

7.2.1.1 ZnO TFTs Incorporating SiO_2 Dielectric

It is observed that an application of a gate bias stress on the ZnO/SiO_2 TFTs, results in variations in μ_{eff}, V_T and $V_{on.}$ An application of a positive gate bias stress moves the characteristic curve to the right whereas a negative gate bias shifts the curve to the left (figure 7.2).

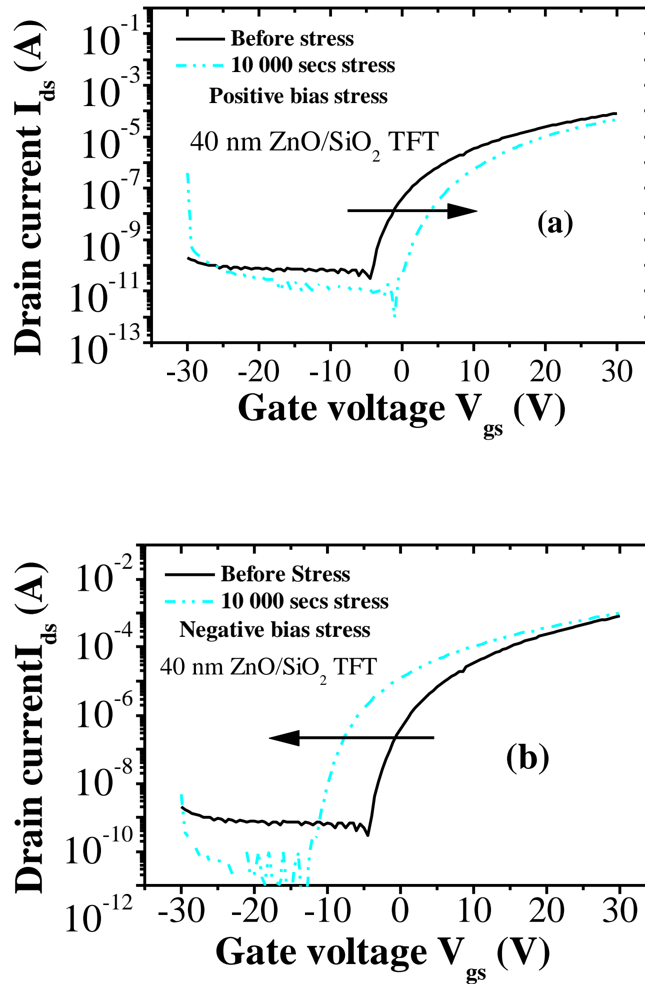


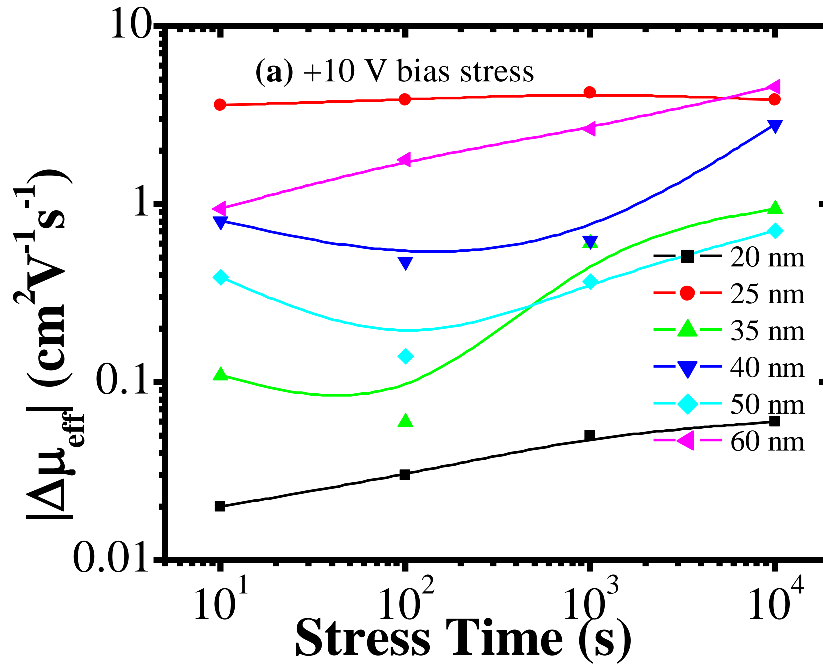
Figure 7.2 – Typical instability in ZnO TFT incorporating SiO_2: (a) positive gate bias stress (b) negative gate bias stress.

The shifts ΔV_T and ΔV_{On} following a positive gate bias stress are shown in figures 7.3 and 7.4 for stresses up to a maximum time of 10^4s. The shift in V_{On} following a negative bias stress is generally greater than that following a positive bias stress and also found to vary with ZnO layer thickness (see appendix B). The parameters ΔV_T and ΔV_{On} used here are defined as in equations (7.1).

………………………………………………………….. (7.1a)

………………………………………………………….. (7.1a)

$V_T(t)$ and $V_{on}(t)$ are the threshold and turn-on voltages of the TFT after a stress bias time t. The values of the parameters prior to an application of a stress bias correspond to t = 0. Figures 7.3 and 7.4 show the results of gate bias stress (positive bias stress) instability obtained in this work. It is observed that both performance and stability are dependent on ZnO thickness. In addition, the variation of S with stress time is generally weak but again shows a clear dependence on ZnO layer thickness (figure 7.4b).



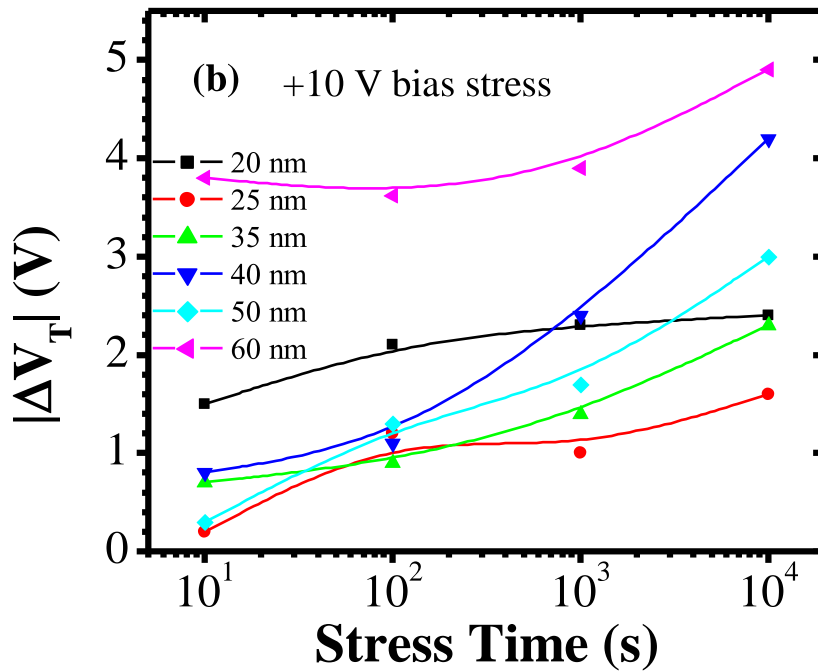
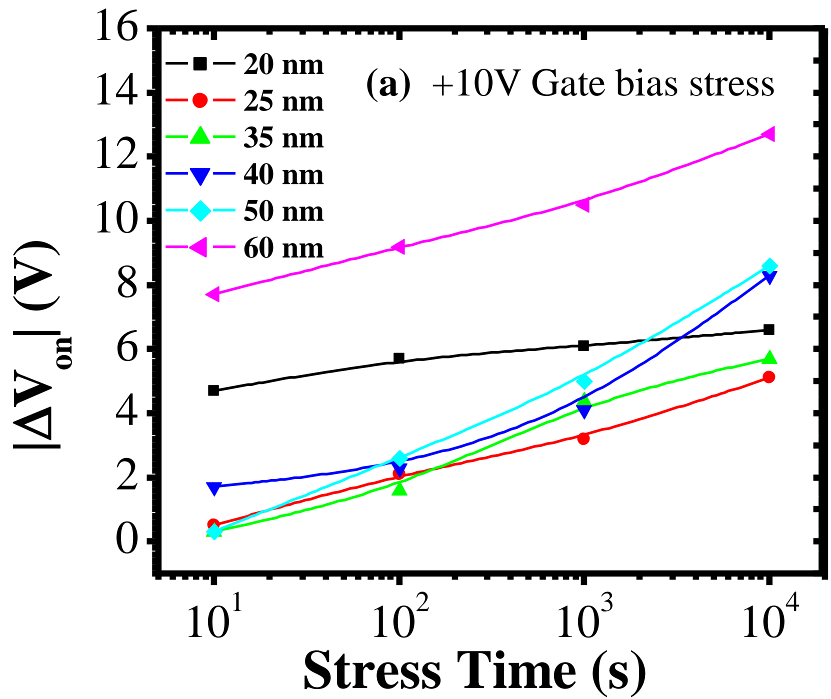


Figure 7.3 - Variations in (a) effective mobility, (b) threshold voltage, parameterised for different ZnO thicknesses (20 – 60 nm).



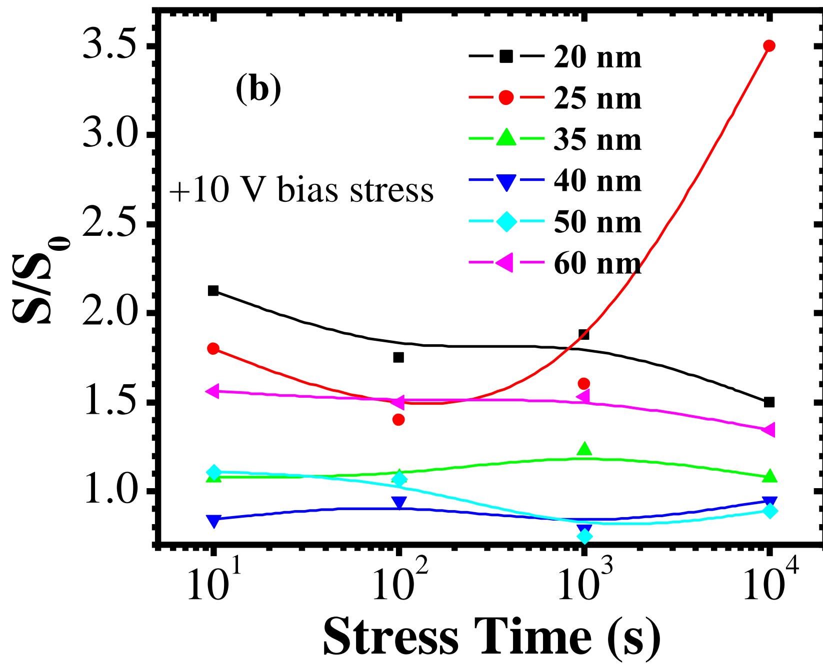


Figure 7.4 - Variations in (a) turn-on voltage and (b) sub-threshold slope; parameterised for different ZnO thicknesses (20 – 60 nm).

Following the ZnO layer thickness optimisation for performance and gate bias stress instability, a thickness of 40 nm was considered the most appropriate and is used throughout in this thesis for ZnO TFT fabrication. This is because; the film with 40 nm demonstrates the best stability in terms of S and V_{On} (figure 7.4) while exhibiting only a weak variation ($\Delta\mu_{eff}$) with prolonged stress bias (figure 7.3 a) compare to 50 and 60 nm thick ZnO layers.

7.3 Performance Assessment on High-k Dielectrics

Figure 7.5 shows the results of the normalised sheet conductance (G) versus induced charge (Q_{ind}) at the interface of ZnO TFTs incorporating different dielectrics. G is calculated from the transfer characteristics as in equation (7.2), and provides a means of comparing the induced charge in TFTs incorporating different dielectrics.

——— .... (7.2a)

—— .... (7.2b)

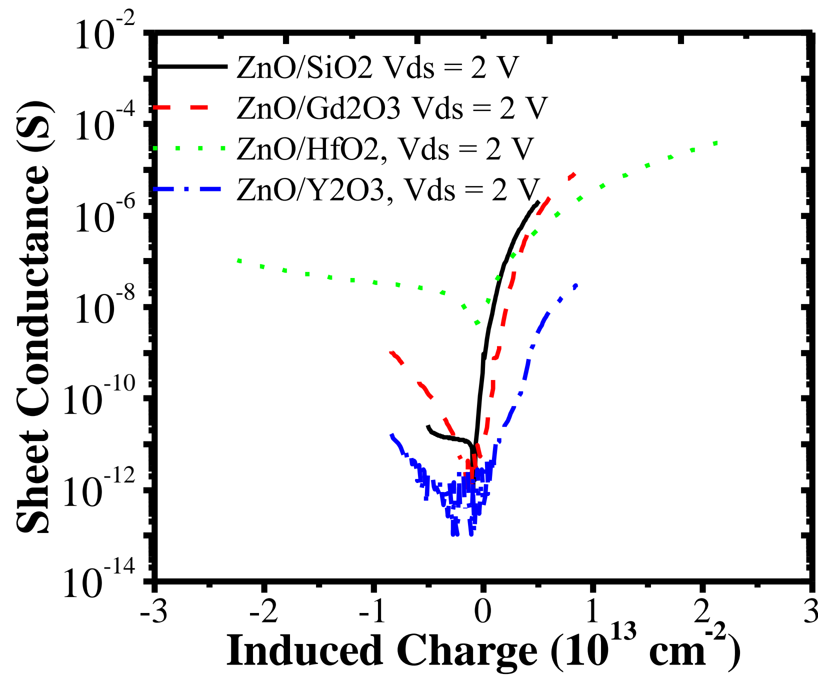


Figure 7.5 - Normalised gate transfer characteristics for ZnO-TFTs using SiO_2, Gd_2O_3, HfO_2, and Y_2O_3 as the gate insulator material.

Comparing the performance parameters of ZnO TFTs (table 7.1) across different dielectrics, HfO_2 and Gd_2O_3 are found to have much superior performance (with respect to μ_{eff}) relative to SiO_2. Also, comparing the interfacial properties with those of ZnO TFTs incorporating thermally grown SiO_2 and other high-k dielectrics [41, 330], the density of interface traps is between $10^{12} – 10^{14}$ cm^{-2}.

Table 7.1- Performance parameters of ZnO TFTs incorporating different dielectrics.

	μ_{eff} ($cm^2V^{-1}.s^{-1}$)	V_T	V_{on}	I_{On-Off}	S	N_{ss} (cm^{-2})
ZnO/Gd₂O₃	33.50	19.8	-4.7	8.3×10^7	2.4	1.1×10^{13}
ZnO/Y₂O₃	0.07	20.6	-0.3	1.0×10^4	2.7	1.3×10^{13}
ZnO/HfO₂	31.18	17.0	-1.4	1.1×10^4	0.63	7.2×10^{12}
ZnO/SiO₂	7.0	18.7	-4.5	1.6×10^6	0.9	2.4×10^{12}

HfO_2-based ZnO TFTs, however, were found to exhibit lower on-off ratios. The decrease in On-Off ratio observed in ZnO/HfO_2 TFTs, as a result of high off-state currents together with anti-clockwise hysteresis observed in the transfer characteristics, could be due to the desorption of hydrogen in the underlying HfO_2 films which diffuses into the ZnO layer above it. Hydrogen incorporation at the interface and in the ZnO active channel layer grain boundary interfaces has been reported to enhance both performance and off-state leakage current in ZnO TFTs [23, 137-140]. However, as hydrogen is a shallow donor in ZnO, excess hydrogen may lead to degradations in off-state leakage current as a result of increased channel conductivity. This suggestion is also supported by the weak saturation observed in the transistor output characteristics of these devices (Appendix B), an indication of greater doping. The improved mobility, carrier concentration, and conductivity by hydrogen here suggested, is in agreement with the work of Jae-Min et al. [140].

Furthermore, the density of interface states in ZnO/HfO_2 TFTs is also lower, suggesting the possibility of hydrogen diffusion from the underlying dielectric layer may have occurred, resulting to the passivation of the interface, so that the high

mobility observed can be partly due to reduced interface scattering. Also, anti-clockwise hysteresis in both the *off-state* and *on-state* current regimes suggest that field-dependent electron-hole pair generation is likely to be another dominant mechanism in ZnO films deposited on HfO_2; and hence the off-state leakage in these films is likely to have contributions from hole conduction that increases ambipolar characteristics.

In general, all the high-k dielectrics have higher densities of interface traps (about 10^{13} cm^{-2}, about one order higher than for SiO_2). The marked difference in the TFT performance across different dielectrics is an indication that the lattice mismatch at the interface may not be the only cause of the performance variation in this case as N_{ss} is approximately of the same order in all the high-k dielectrics (table 7.1). However, Y_2O_3 TFTs present the lowest effective mobility and drain current, even though the induced charge is superior to that of the SiO_2 and approximately the same as for Gd_2O_3 based TFTs (figure 7.4). The interface trap density is also the highest in Y_2O_3 TFTs, thus, interface scattering (lattice mismatch) could be a contributor to the performance degradations in these transistors.

The large variation of performance parameters also suggests that the films either crystallise in different orientations or that the crystallite sizes are affected differently by the underlying dielectric during growth as reported earlier [8, 137, 176]. Indeed, ZnO thin films in this work also crystallise differently on different dielectrics (figure 7.6).

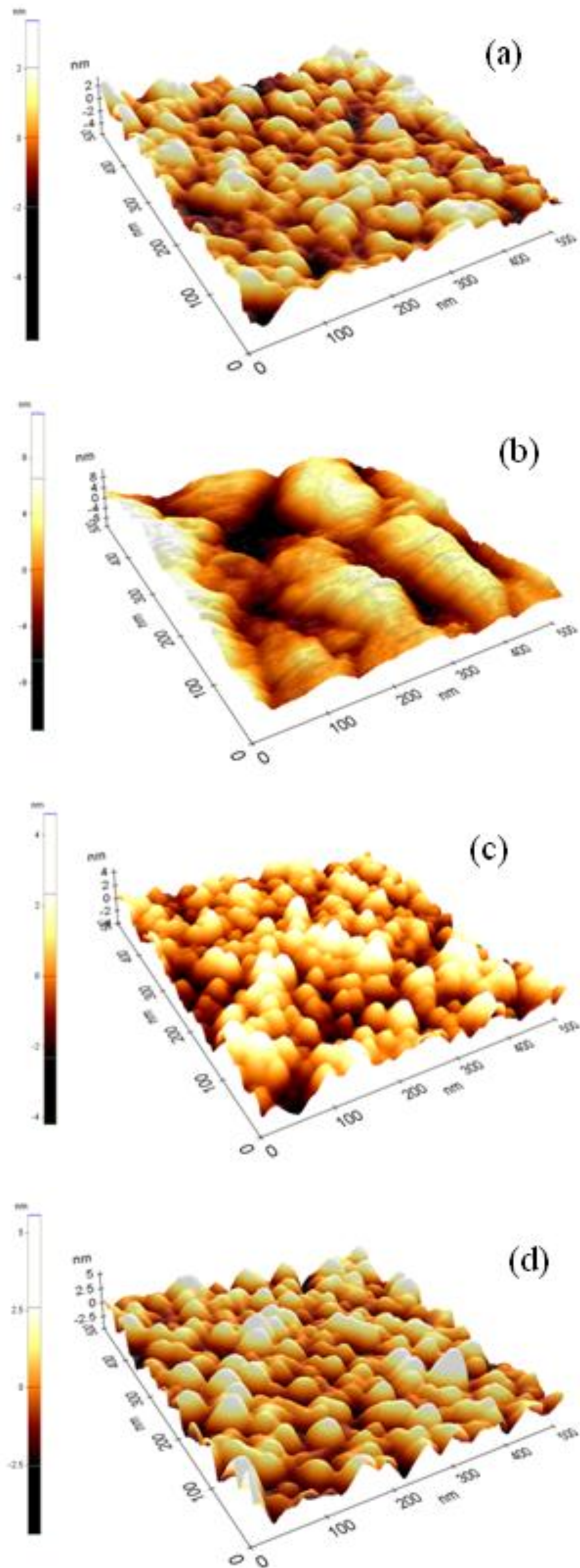


Figure 7.6 – AFM images of sputtered ZnO thin films on different dielectrics: (a) Gd_2O_3, (b) HfO_2, (c) Y_2O_3 and (d) SiO_2

The AFM images show that ZnO films deposited on HfO_2 have the largest grains and show grains shapes that are significantly different (appear as elongated ridges) from those of ZnO deposited on the other dielectric layers (which are more circular in shape). Both these properties will greatly affect the density of grain boundaries in the active channel layer (assuming that the size of the grains at the interface is proportional to that of the top surface grains), resulting in improved charge percolation and hence improved effective mobility.

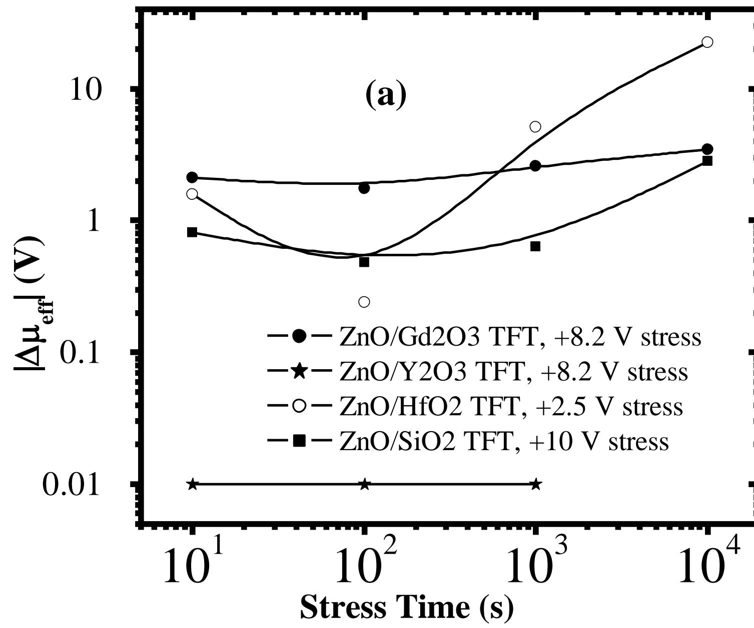
As a consequence of the larger grain sizes, the ZnO/HfO_2 interface is likely to be rougher. On the other hand, ZnO films deposited on Gd_2O_3 have smaller grains similar to that of ZnO on SiO_2, an indication that both the surface roughness and the concentration of grain boundaries are likely to have a strong influence on ZnO/Gd_2O_3 TFT performance. Furthermore, ZnO TFTs incorporating Y_2O_3 insulating layers showed the poorest performance. In addition, the Y_2O_3/ZnO interface is rougher than that of ZnO on SiO_2 and Gd_2O_3. Therefore the poor performance of ZnO TFT incorporating Y_2O_3 can be ascribed to the poor interfacial characteristics. Therefore, charge scattering at grain the boundaries at/or near the interface is likely to be the dominant factor contributing to the poor performance.

Table 7.2 - Surface roughness of a 40 nm thick ZnO thin film sputtered on different dielectric layers.

Dielectric material	Gd_2O_3	HfO_2	Y_2O_3	SiO_2
Surface roughness (nm)	0.763	3.230	1.367	0.953

7.3.1 Gate Bias Stress Instability Assessment of ZnO TFTs Incorporating High-k Dielectrics

Bias stress-related instability in a-Si:H TFTs as discussed in {§ 6.6} is either as a result of charge trapping at the insulator/semiconductor interface, charge injection into the insulator, or as a result of state creation in the semiconductor. State creation is reported to be the dominant cause of instability in a-Si:H TFTs at low fields (< 1MV/cm). As high-k dielectrics offer an enhanced gate capacitance coupling with the induced interface charge, the influence of charge trapping at the insulator/semiconductor interface and charge injection into the insulator on carrier transport in the active channel is likely to be minimised in TFTs incorporating high-k dielectrics due to the possibility of low operational voltages. Therefore instability issues related to performance e.g. $\Delta\mu_{eff}$ is likely to have a stronger dependence on state creation in the semiconductor. Figures 7.7 - 7.10 show the variation of some important parameters (μ_{eff}, V_T, V_{on} and $I_{On\text{-}Off}$ ratio), for positive and negative gate bias stresses respectively as a function of stress time for different dielectrics.



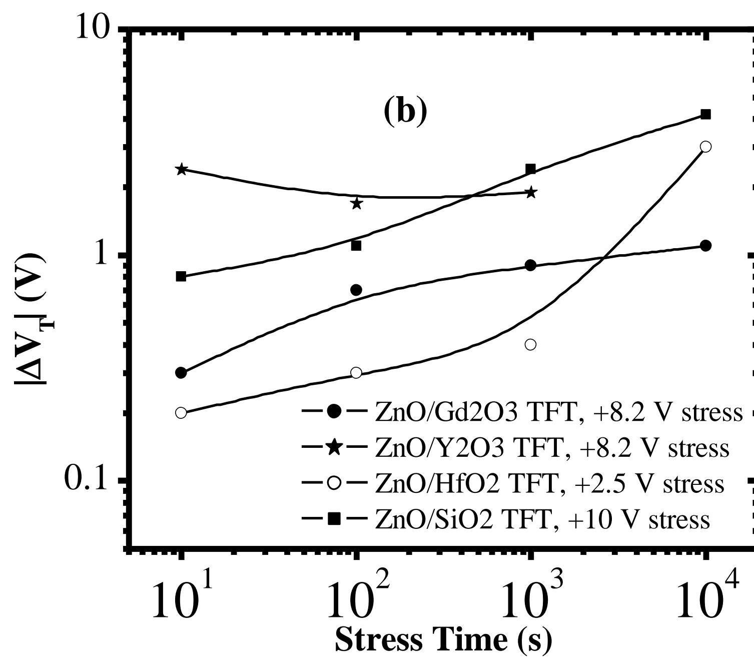
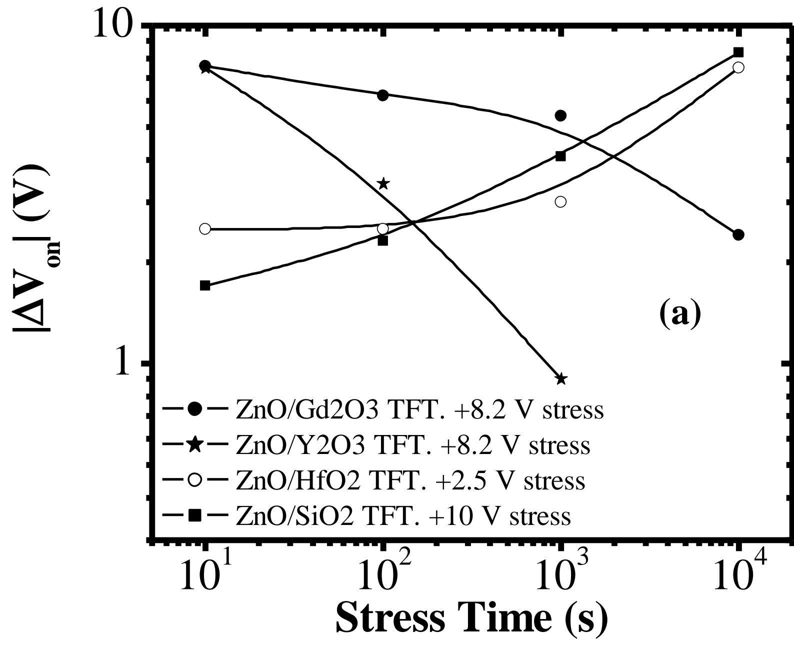


Figure 7.7 - Variations of: (a) effective mobility and (b) threshold voltage of ZnO TFTs incorporating different high-k dielectrics under positive gate bias stress for up 10^4 s, referenced to SiO_2.



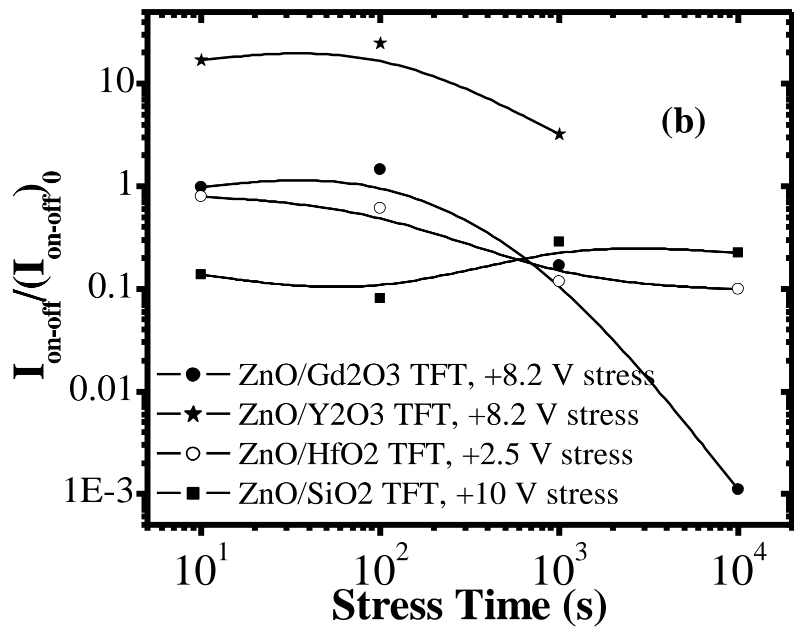


Figure 7.8 – Variations of: (a) turn-on voltage and (b) On-Off ratio of ZnO TFTs based on different high-k dielectrics under positive gate bias stress for up 10^4 s, referenced to SiO_2.

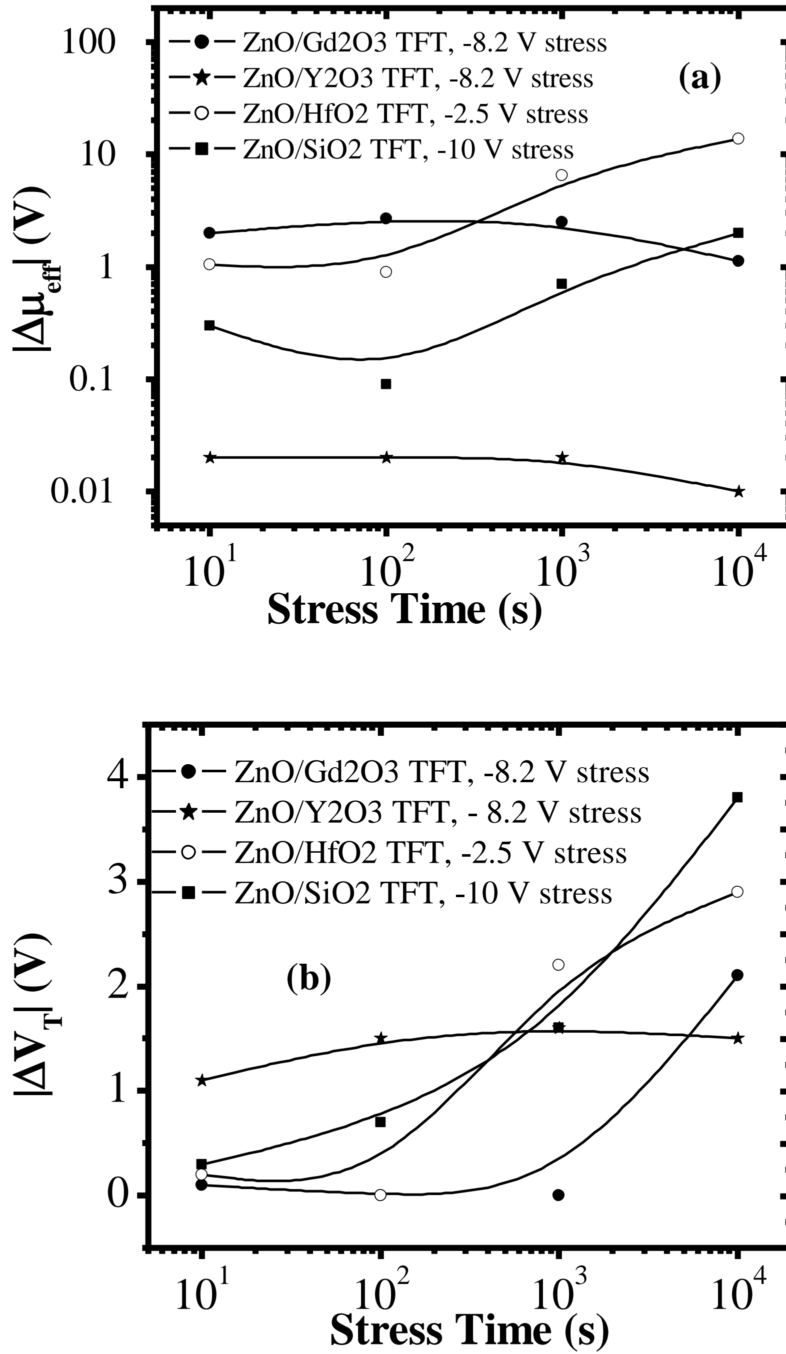
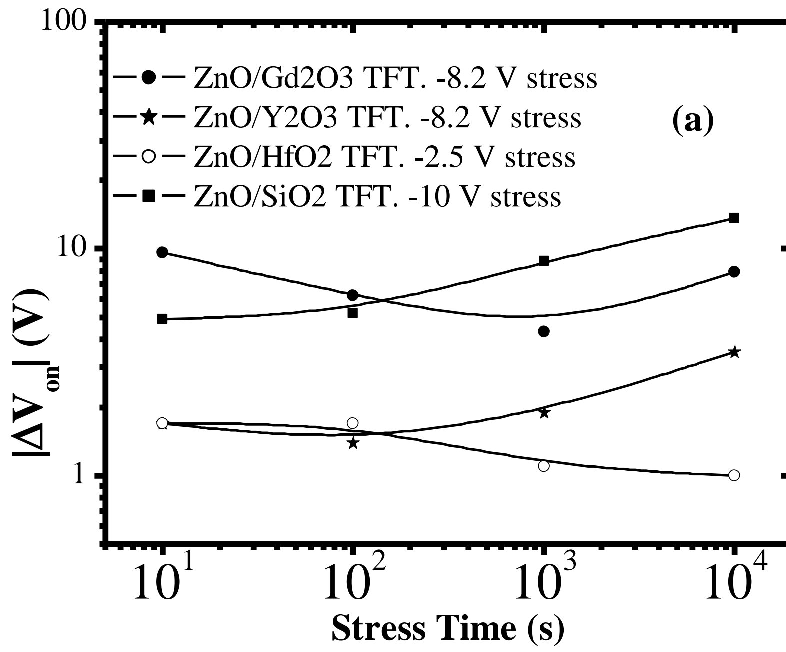


Figure 7.9 - Variations of: (a) effective mobility and (b) threshold voltage of ZnO TFTs incorporating different high-k dielectrics under negative gate bias stress for up 10^4 s, referenced to SiO_2



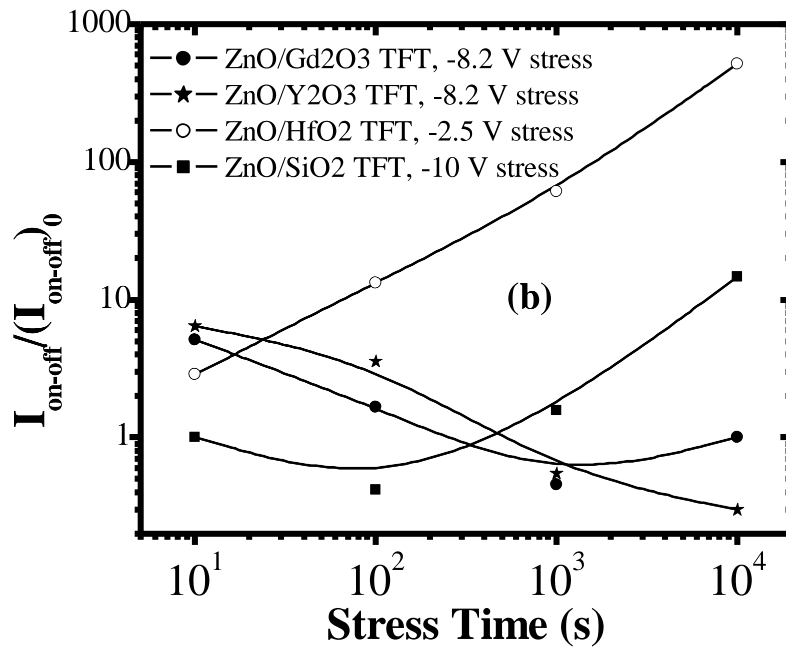


Figure 7.10 - Variations of: (a) turn-on voltage and (b) on-off ratio of ZnO TFTs incorporating different high-k dielectrics under negative gate bias stress for up 10^4 s, referenced to SiO_2

As observed in figures 7.7 - 7.10, an application of a stress bias on to the different TFT structures for a short period (10 s) already induces instability in μ_{eff}, V_T, V_{On} and $I_{On\text{-}Off}$. Further bias stressing on these structures however, demonstrate that TFTs incorporating Gd_2O_3 and Y_2O_3 have very stable characteristics. The ZnO/Y_2O_3 TFT even demonstrates stability in μ_{eff} that is superior to that of a ZnO/SiO_2 TFT. Comparing the variations in V_{On} with bias stress time for the different TFTs, ZnO/HfO_2 TFTs show better stability following a negative bias stress. However, the stability in $I_{On\text{-}Off}$ is worst in these TFTs (figure 7.10 b) due increase in off-state current.

Figures 7.2, 7.6 and 7.7 show that the instability exhibited under negative bias stress is generally greater than for positive bias stress. In addition, it is observed that the characteristic curves of all the TFTs relax to their original shape following a positive or negative bias stress after about 3 – 6 hours on their own after the stress bias is removed. However, relaxation following a negative stress bias was slower than that following a positive bias stress. This asymmetry suggests that the instability was not limited to charge trapping at the interface alone, and state creation in the ZnO bulk could not be ruled out. Moreover, since negative bias stress results in greater instability, one could speculate that, for a good device quality insulator, instability may be limited to charge trapping at/near the interface and state creation in the ZnO semiconductor. In addition, figures 7.9 and 7.10 show that the dependence of ΔV_T and ΔV_{On} with bias stress time is more linear with time (on a log scale). This further confirms the assertion that state creation instability could be an issue in ZnO TFTs.

With the exception of the ZnO/HfO_2 TFT devices, clockwise hysteresis was observed in the transfer characteristic of all devices incorporating other insulators. This

together with the unidirectional parallel shift in the transfer characteristics following either a negative or positive bias stress was consistent with trapped charge screening of the applied electric field [319], modulating the V_T of the devices.

7.4 Summary

In this chapter, ZnO TFTs have been electrically characterised for performance and gate bias stress instability. TFTs incorporating both SiO_2 and high-k dielectrics have been characterised and compared. The characteristics have also been discussed against the ZnO film physical properties deduced from AFM analysis. The role of hydrogen incorporation on the performance of ZnO TFTs is also suggested. The exceptionally improved performance (with respect to μ_{eff}) of ZnO TFTs incorporating the HfO_2 insulator (in comparison to SiO_2) is potentially related to an improved interface as a consequence of H_2 passivation, and in part as a result of enhanced channel conductance, which may be a consequence of H_2 diffusion into the active channel layer. The high channel mobility in TFTs incorporating Gd_2O_3 may be ascribed in part to improvements in ZnO crystallite sizes and on the excellent interface (smooth). Y_2O_3 based ZnO TFTs' poor performance have also been discussed.

Chapter - 8

Conclusions and Suggestions for Future Work

It has been demonstrated in this thesis that thin films of device quality ZnO, suitable for low temperature TFT applications can be deposited by a reactive RF magnetron sputtering process. Moreover, high-k dielectrics (Gd_2O_3, HfO_2 and Y_2O_3) deposited by MOCVD have been incorporated into ZnO TFTs with useful performance metrics (e.g. μ_{eff} > 33 $cm^2V^{-1}s^{-1}$ and $I_{On\text{-}Off}$ > 10^7). In addition, using the different dielectric materials, AFM images reveal that, ZnO growth is substrate dependent, and hence film properties would be influenced by the underlying dielectric layer, and could be a major contributing factor behind the performance and stability variations observed.

The ZnO films used have been optimised for performance and bias stress stability, via deposition parameters and post-deposition treatment with oxygen. The post-deposition oxygen-treatment is found to be a vital approach to solving electrical instability issues related to O_2 diffusion from the surrounding ambient into the ZnO films and the adsorption of O_2 on the top surfaces. It is suggested that treating ZnO films with O_2 can precipitate ageing in the films, so that the effects of O_2 from the surrounding air on the electrical properties can be neglected. Using VASP, the effects of O_2 adsorption on the (0001) ZnO surface and its consequences on the film electronic properties has been investigated and found to be a plausible cause of the modulation of surface properties. In addition, it is suggested that O_2 adsorption at (0001) ZnO surfaces could affect both the bandgap and film transparency.

Using the optimised (for performance, stability and thickness) ZnO film, that has been O_2 treated, the integration of high-k dielectrics into ZnO TFTs is investigated, and it is hoped that high-k dielectric materials can provide a useful route to achieve stable TFTs. The performance and stability assessment of ZnO TFTs using different dielectric materials is performed and compared to their SiO_2 counterparts. ZnO films are found to grow differently on different dielectrics and this modulates both the performance and bias stress stability. This demonstrates that performance and stability in ZnO TFTs could also be optimised via a suitable choice of the dielectric layer. In addition, the overall impressive performance characteristics of ZnO TFTs incorporating Gd_2O_3 suggests that high-k dielectrics integration presents a viable route to solving both performance and instability issues in such TFTs.

8.1 Future Work

The aim of this thesis has been to investigate the performance and stability of ZnO TFTs produced using a sputtering process at near room temperature. Despite achieving ZnO TFTs with impressive performance using different high-k dielectrics, these dielectrics were deposited at temperatures (400 – 950 ^{0}C) much higher than room temperature. It is envisaged that low temperature-produced semiconductors could be integrated in the roll-able or flexible LCDs of the future. Therefore, it would be important to investigate further the performance, stability and reliability of ZnO TFTs incorporating dielectric layers that are compatible with near-room temperature processes.

It has also been assumed in this thesis that the variation of the electrical properties of ZnO thin films in air is dominated by O_2 adsorption. Although O_2 post-deposition treatment has produced stable films, it is recommended that the study be extended to other gases and the possibility of using a specified gas mixture for an optimum post-deposition treatment. In addition, it would be vital to investigate on whether the O_2 post-treatment is actually limited to the top surface, and as such gain a better understanding on the extent to which the O_2 diffuses into the ZnO layer and its possible effect on the grain boundaries in the bulk.

Appendix A - Substrate Cleaning and Device fabrication

I) Glass

(1) 30 minutes ultrasonic in 5 % Decon-90 in 18 MΩ De-ionised (D.I.) water solution.

(2) 2 minutes ultrasonic rise in 18 MΩ D.I. water. (Repeat 5 times).

(3) 15 minutes ultrasonic in acetone (Fisher Electronics grade).

(4) 15 minutes ultrasonic in isopropyl alcohol (Fisher Electronics grade).

(5) 2 minutes ultrasonic rise in 18 MΩ D.I. water. Repeat 5 times.

(6) Spin dry (3000 rpm) under nitrogen for 30 seconds.

(7) 1 hour drying baking in air at 150 ^{0}C.

II) Silicon wafers

(1) 10 minutes 'bomb' clean (i.e. 50 % sulphuric acid and 50 % hydrogen peroxide (H_2O_2)). The mixture is obtained by slowly adding the H_2O_2 onto the acid.

(2) 2 minutes ultrasonic rise in 18 MΩ D.I. water. Repeat 5 times.

(3) 3o minutes dip into buffered hydrofluoric acid (HF) (Fisher electronic grade), H_2O: HF = 10:1 mixture.

(4) 2 minutes ultrasonic rise in 18 MΩ D.I. water. Repeat 5 times.

(5) Spin dry (3000 rpm) under nitrogen for 30 seconds.

(6) 15 minutes sift baking in air, at 100 ^{0}C.

III) Silicon wafers Process flow for the ZnO TFT Fabrication

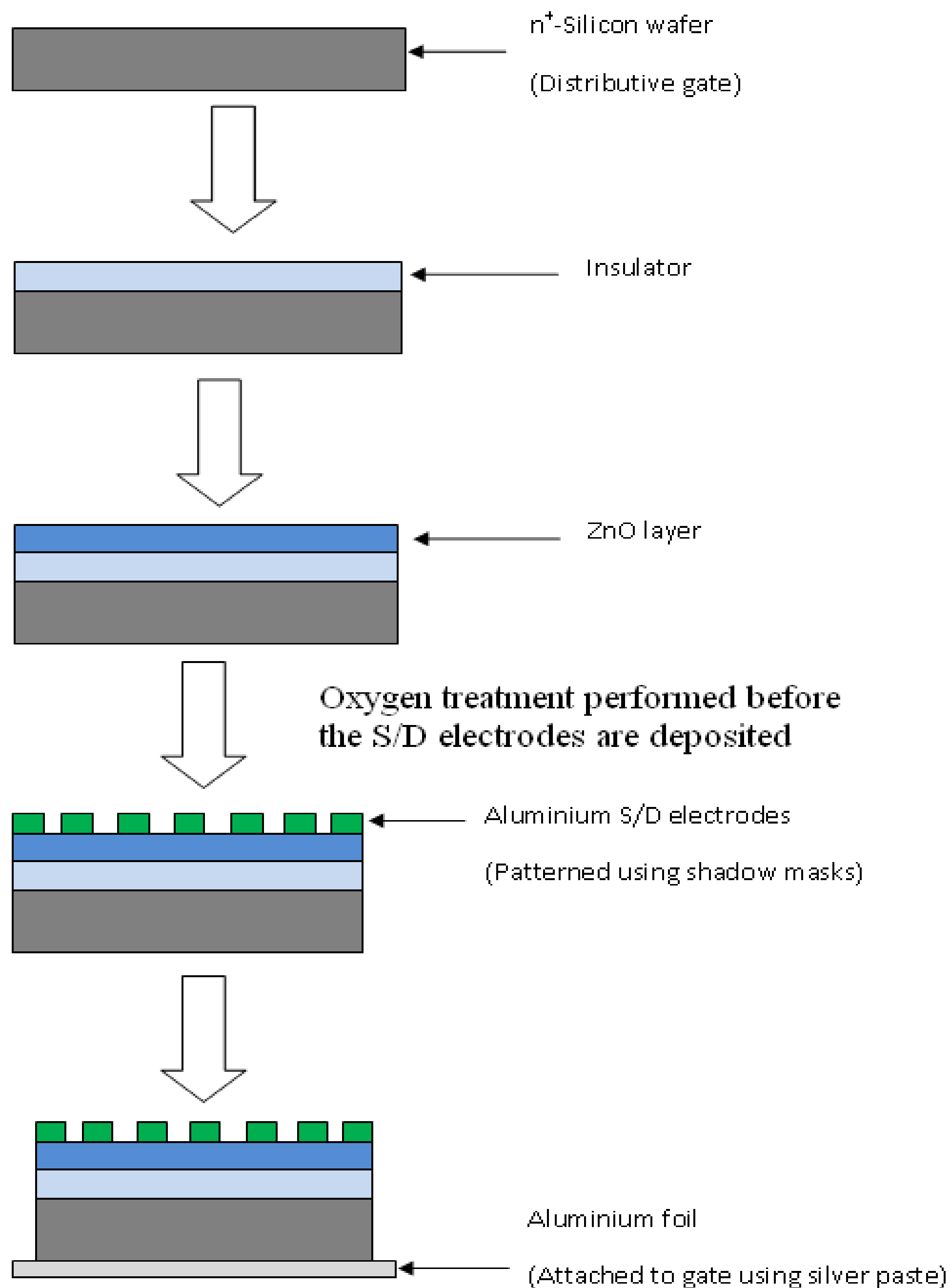


Figure 8.1 – ZnO TFT Fabrication process

Appendix B - Supplementary Results

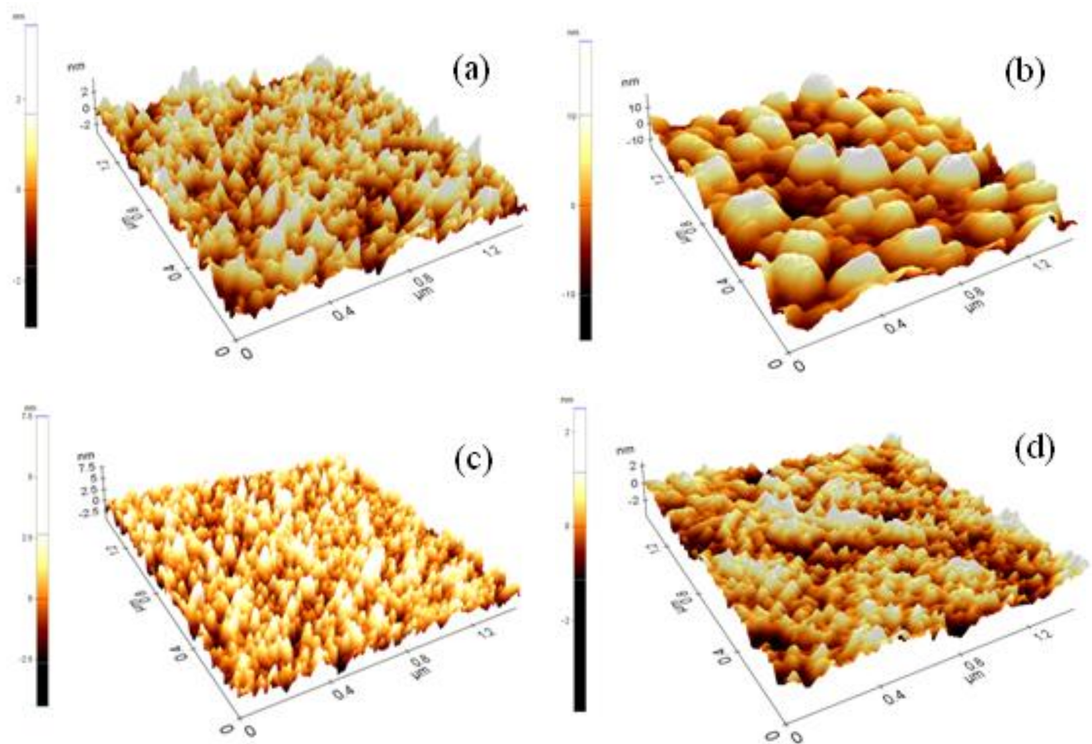


Figure 8.2 – Typical large scan (1.5 μm) AFM images of dielectrics used: (a) Gd_2O_3, (b) HfO_2, (c) Y_2O_3 and (d) SiO_2.

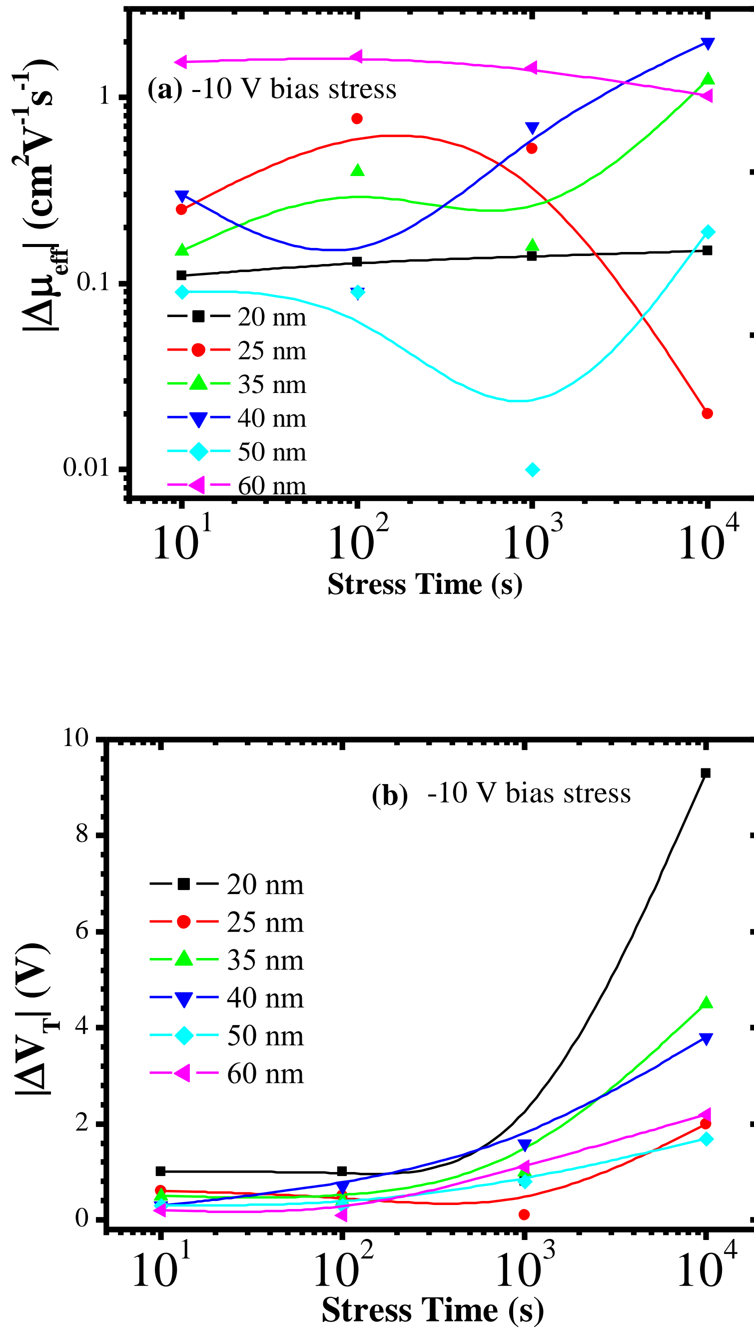


Figure 8.3 - Figure 8.2 - Variation of: a) change in effective channel mobility ($\Delta\mu_{eff}$) and b) change in threshold (ΔVT) with ZnO thickness, following a negative gate bias stress.

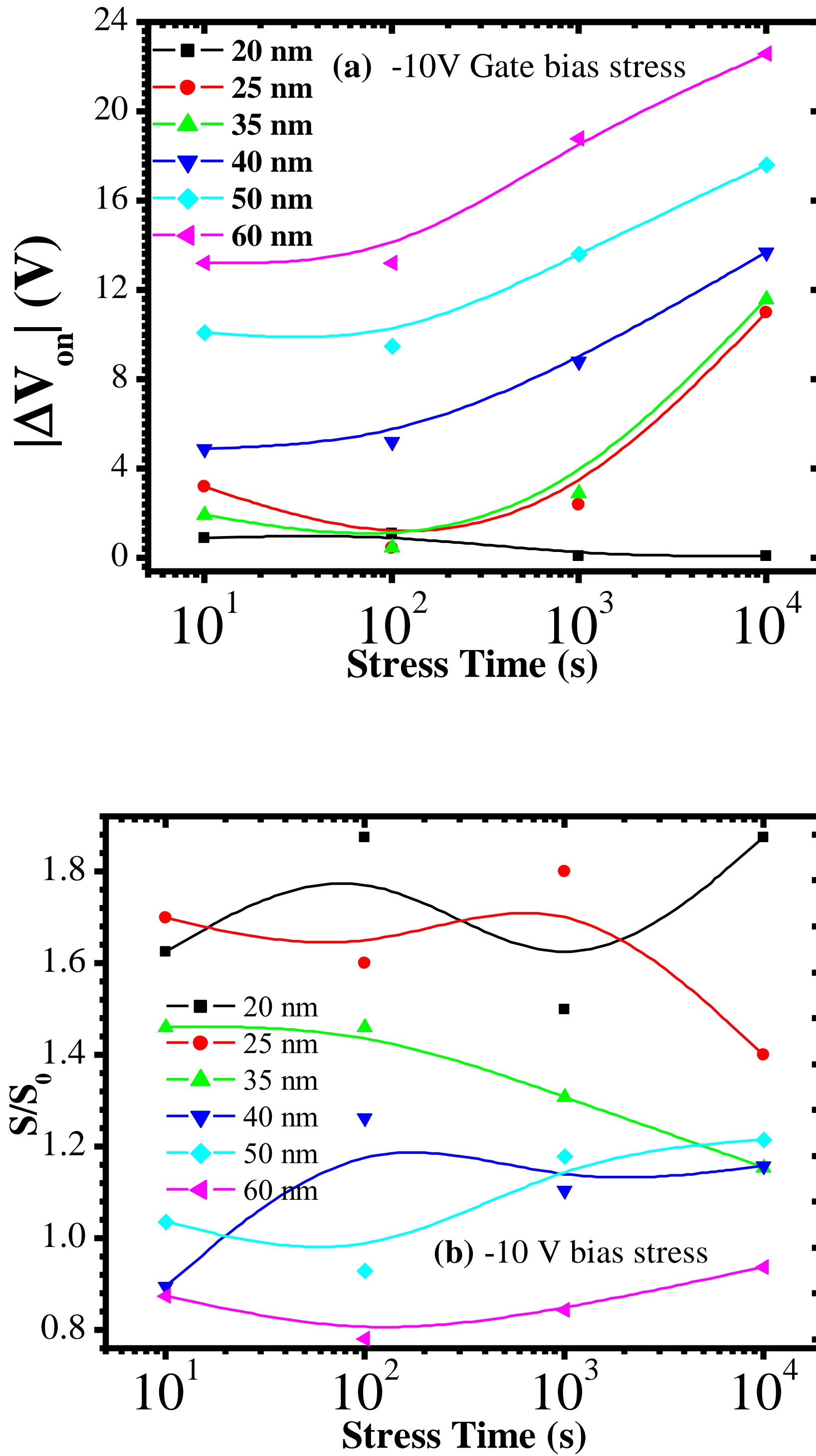


Figure 8.4 - Variation of: a) change in turn-on voltage (ΔV_{On}) and b) normalised threshold slope (S/S_0) with ZnO thickness, following a negative gate bias stress.

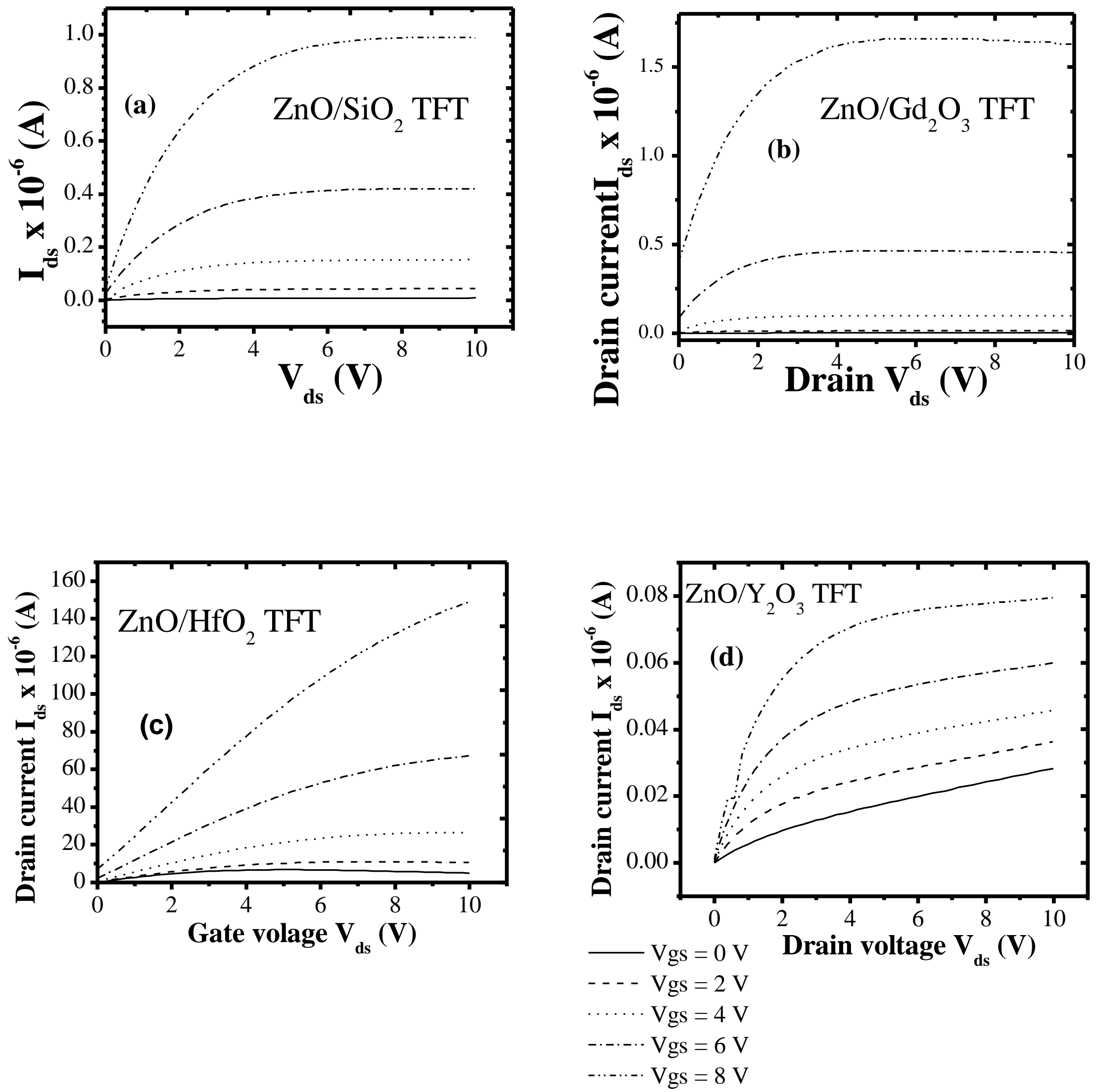


Figure 8.5 – ZnO TFT output characteristics incorporating layers: (a) SiO_2, (b) Gd_2O_3, (c) HfO_2 and (d) Y_2O_3 insulators.

Appendix C – List of Acronyms

AFM .... Atomic Force Microscopy

AFMc .... Atomic Force Microscope

ALD .... Atomic Layer Deposition

AMLCD .... Active Matrix Liquid Crystal Display

E_b .... Binding Energy

C.G.S .... The Centimetre, the Gram and the Second

CB .... Conduction Band

CMOS .... Complementary Metal Oxide Semiconductor

CV .... Capacitance-Voltage

CVD .... Chemical Vapour Deposition

DC .... Direct Current

DFT .... Density Functional Theory

DOS .... Density of States

ELF .... Electron Localisation Function

EOT .... Equivalent Oxide Thickness

EPD .... Electrophoretic Deposition

FET .... Field Effect Transistor

FPD .... Flat Panel Display

FWHM .... Full Width at Half Maximum

HeNe .... Helium-Neon

IC .... Integrated circuit

IV .... Current-Voltage

LED .... Light Emitting Diode

LPCVD .... Low Pressure Chemical Vapour Deposition

MBE .... Molecular Beam Epitaxy

MFC .... Mass Flow Controllers

MIS .... Metal-Insulator-Semiconductor

MISFET .... Metal-Insulator-Semiconductor Field Effect Transistor

MOCVD .... Metal-Organic Chemical Vapour Deposition

MOSFET .... Metal-Oxide-Semiconductor Field Effect Transistor

MRS .... Material Science Society

OLED .... Organic Light Emitting Diode

PECVD .... Plasma-Enhanced Chemical Vapour Deposition

PLD .... Pulse Laser Deposition

PSD .... Position Sensitive Detector

PVD .... Physical Vapour Deposition

RF .... Radio Frequency

RTA .... Rapid Temperature Annealing

SB .... Schottky Barrier

TFT .... Thin Film Transistor

TLM .... Transmission Line Method

UV-Vis .... Ultra-Violet-Visible

VASP .... Vienna Ab initio Simulation Package

VEE .... Visual Engineering Environment

VB .... Valence Band

XRD .... X-Ray Diffraction

ZnO .... Zinc Oxide

Appendix D – Physical Constants

Name	Symbol	Value	Units
Boltzmann Constant	k	1.380650×10^{-5}	J k^{-1}
Elementary Charge	q	1.602176×10^{-19}	C
Permittivity of Free	ε_0	8.854188×10^{-14}	F cm^{-1}
Planck Constant	h	6.626069×10^{-34}	J s
Reduced Planck Constant	$\hbar$	1.054572×10^{-34}	J s

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