Bistability and Electrical Characterisation of Two Terminal Non-Volatile Polymer Memory Devices.

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Author's declaration

I declare that the work in this thesis is in accordance with the regulations of De Montfort University. No part of this thesis has been submitted for any other degree or qualification at De Montfort University, or any other academic institution. Permission to copy or use whole or part of the work contained herein must be solicited except for the purpose of private study or academic purposes in which case the author must be explicitly acknowledged. The work contained in this thesis is as a result of my own effort unless stated otherwise.

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Abstract

Polymer blended with nanoparticle and ferroelectric materials in two terminal memory devices has potential for electronic memory devices that may offer increased storage capacity and performance. Towards understanding the memory performance of a combination of an organic polymer with a ferroelectric or unpolarised material, this research is concerned with testing the memory programming and capacitance of these materials using two-terminal memory device structures. This research contributes to previous investigation into the internal working mechanisms of polymer memory devices and increases understanding and verifies the principles of these mechanisms through testing previously untested materials in different material compositions.

This study makes a novel contribution by testing the electrical bistability of new materials; specifically, nickel oxide, barium titanate and methylammonium lead bromide and considers their properties which include nanoparticles, ferroelectric, perovskite structures and organic-inorganic composition. Due to their material properties which have different implications for internal switching and memory storage. Nanoparticles have a greater band gap between the valence band and conduction band compare to bulk material which be exploited for memory storage and ferroelectric properties and perovskite materials have non-volatile properties suitable for switching mechanisms. Specific attributes of memory function which include charging mechanism, device programming, capacitance and charge retention were tested for different material compositions which included, blend and layered with a PVAc polymer, and as a bulk material with a single crystal structure using MIM memory devices and MIS device structures. The results showed that nickel oxide was the most effective material as a blend with the polymer for memory performance, this was followed by barium titanate, however, methylammonium

lead bromide performed poorly with polymer but showed promise as a single crystal structure. The results also showed that an increase in concentration of the tested material in a blend composition resulted in a corresponding increase in memory function, and that blend compositions were much more effective than layered compositions.

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Chapter 1 Overview of Research

1.1 Introduction

There has been a rapid increase in the study of organic materials and polymers for electronic memory devices. Such devices exhibit two electrical conductance states, namely; “high” and “low”, when an external voltage is applied [1] [2] and therefore, such electronic memory devices may find their use in many applications such as Computers, Radio Frequency Identification (RFID), Smart labels and packaging, Electronic Books, and Papers. To encourage the commercial application of organic memory devices, further studies are required to understand the working mechanisms of such devices. In this study, three different materials in different material composition and device structures are used to test the electrical bistability mechanism proposed by Paul (2007). For each device, electrical characterisation is investigated for the different memory functions, and to further understand the physical process of electrical bistability in such devices.

There has been an increase in the demand for faster and more efficient memory devices. The efficiency of these memory devices is measured using speed of performance and storage capacity. Two-terminal resistive switching memory devices are increasingly receiving attention [3]. They are comprised of an active material sandwiched between two electrodes. Polymers are used as the insulator in such devices, however, the memory capability is also achieved by the active material such as nanoparticles and nanostructures which trap and retain charge as part of memory function. Resistive switching has been

observed in these types of devices, a mechanism that is considered and verified in this study.

The essential ability to retain electric charge and to achieve an electrical bistability through the creation of an internal electric field within a nano-composite, result in two terminal non-volatile memory devices (2TNVM) is an ability that has been established in a principle by Paul (2007) [4]. This study scrutinises this principle proposed by Paul (2007) in a polymer composite; a polymer in combination with nanoparticle, and organic/inorganic ferroelectric materials. The choice of materials was nickel oxide (NiO), barium titanate ($BaTiO_3$) and methylammonium lead bromide ($MAPbBr_3$). These materials have not been tested before, particularly in terms of different material compositions and structures, but importantly were chosen for testing because of their differentiated internal properties resulting in different internal structures that create polarisation and bistability, suitable for memory devices.

The electrical bistability that is achieved within these devices is verified in light of the principles presented by Paul (2007) [4] . Verification of these principles is part of understanding what happens in terms of internal mechanisms for each of the tested materials, specifically, the internal switching mechanisms that give rise to electrical bistability which is a requirement for memory capability. It is important to note, however, that it is not the main intention of the study to verify these principles, rather it is to test and understand the internal mechanisms of devices using the tested materials against the proposed principle of the workings of these mechanisms.

It is important to understand that the need to verify the principles comes from the fact that in reference to testing nanoparticles there are a number of experimental differences that make it difficult to make a conclusion about a mechanism possibly responsible for the switching behaviour [5]. Specifically, the differences relate to different devices, differences in electrical testing and different manufacturing procedures [5]. Therefore, towards further verification of the principles established by Paul (2007) there is a need to test nanoparticles of different materials, different device structures and different material compositions.

In light of the above idea, the principles cannot be attributed to every single case, and the only way to approve the mechanism for these numerous possible cases is extensive experimentation that includes different variety of device structures, materials and manufacturing techniques, as well as different experimentation in terms of the attributes of memory. Therefore, a contribution of the present study is that it verifies the internal switching mechanisms for different materials, different material compositions, including blended, layered and bulk, at different concentrations and thicknesses respectively, different manufacturing techniques, different device structures, both Metal-Insulator-Metal (MIM) and Metal-Insulator-Semiconductor (MIS), as two-terminal devices and different tests for different attributes of memory including charging mechanism, memory device programming, capacitance and charge retention and durability. Therefore, this study contributes, for a number of different variables which include different materials, material compositions, specifically, various concentrations of the active material combined with the polymer, and different layered thicknesses of the active material in layered structures towards further verification of Paul's (2007) principles through filling

some of the gaps in the research. Furthermore, studies involving the bistability of polymer / nanoparticle devices are often limited in the number of variables they address, for example, only MIM or MIS structures investigating certain attributes of memory, or only blend or layered compositions. The present study contributes further by considering blend and layered compositions, MIM and MIS structures to investigate different attributes of memory, and different materials.

Therefore, the main aim of this research is to identify the optimal combination of material constitution and fabrication method for electrical bistability in two terminal memory devices. This is to be achieved together with understanding and verifying the working mechanism(s) of two terminal electronic memory devices.

1.2 Aims and Objectives

The study aimed to identify the optimal combination of material constitution and fabrication method for electrical bistability in memory devices. Furthermore, the study set out to verify the principles of the electric-dipole based memory model (Paul, 2007) for understanding and determining electric bistability for different materials, material compositions and fabrication methods. In order to achieve these aims the study investigated electrical bistability of different combinations of material constitutions and fabrication methods, elucidated the memory behaviour from physical and electrical investigations which include testing memory and electrical characterisation using MIM and MIS structures, and considered the results in consideration of the principles of internal switching mechanisms established by Paul (2007).

1.3 Contributions of study

The contributions of the study include the following:

- Establishing memory behaviour of NiO, $BaTiO_3$ and $MAPbBr_3$ combined with a PVAc polymer at different material compositions and as a layered structure with PVAc.
- Measuring the memory effect and electrical bistability of a new material composition, namely; $CH_3NH_3PbBr_3$ Perovskite with PVAc polymer and $CH_3NH_3PbBr_3$ as a single crystal structure.
- Verifying the established principles of internal switching mechanisms established by Paul (2007).

1.4 Thesis Organisation

The thesis is divided into seven chapters. Chapter 2 is concerned with an overview of memory devices. Chapter 3 deals with the two terminal NVM devices and Charge Transport Mechanisms. The experimental methodology used in this work is described in Chapter 4, while the results and discussion are presented in Chapter 5, 6 and 7. A summary of the major outcomes from this study and suggestions for future works are presented in chapter 8.

1.5 Thesis Outcomes

This study addresses some of the gaps in the research through testing different materials that have different properties using different material compositions as well as considering all of the functions of memory. For NiO the results showed that generally an increase in

the concentration of the material and an increase in the thickness of the layers lead to an increase in hysteresis, the same was true for charge endurance. However, NiO as a layered was less effective for charge endurance. The resulting hysteresis was evidence of the achievement of electrical bistability which proved the viability of these materials for rewritable memory devices and verified the internal switching mechanisms proposed by Paul (2007).

For Barium titanate ($BaTiO_3$) there was also an increase in I-V hysteresis corresponding to an increase concentration, although the overall effect was less than NiO, and an increase in concentration also lead to an increase in charge endurance. Moreover, $BaTiO_3$ was found to be more effective as a layered composition than NiO as a layered composition, this was found to be true for charging mechanism, memory device programming and charge.

Both these materials were tested as nanoparticles, however, the third tested material, $MAPbBr_3$, was not a nanoparticle material and was found to be less effective than the other two materials for memory device programming. There was an increase in charge endurance corresponding to increase in concentration.

$MAPbBr_3$ was also tested as a crystal structure to test the crystalline properties that were otherwise removed as part of the process of combining the material with the polymer. This was conducted to determine if it is the ferroelectrical properties of $MAPbBr_3$ that was responsible for charge trapping. The results showed bistability in the device and switching between two resistive states during programming and the device also exhibited data retention properties over time.

1.6 Work Published And/or Presented at Conference

Published Work

- D.C. Prime, Z. Al Halafi, M.A Green, I Salaorua and S. Paul, ‘‘Electrical Conductivity Bistability in Nano-Composite’’, ECS Transactions, 223rd ECS Meeting in Toronto, Ontario, Canada (May 12-16, 2013), 53 (4) 141-148 (2013)
- Z. Alhalafi, and S.Paul, ‘‘Switching in Polymer Memory Devices based on Polymer and Nanoparticles Admixture’’, Advances in Science and Technology, CIMTEC the 6th Forum on New Materials, Italy, Vol. 95 (June 2014) pp 107-112.
- Salaoru, S.Alotaibi , Z. Al Halafi and S. Paul, ‘‘Creating Electrical Bistability Using Nano-bits – Application in 2-Terminal Memory Devices’’, MRS Advances, 2017 Materials Research Society, DOI: 10.1557/adv.2016.677 (Open Access article), (2017).

Conference Presentations

- ‘‘Understanding the bistability of emerging two terminal resistive and polymer memory device’’, Z.Alhalafi and S.Paul, Saudi Student Conferences (7th SSC),1-2 of February 2014, Edinburg , the UK.
- ‘‘Switching in Polymer Memory Devices based on Polymer and Nanoparticles Admixture’’,Z.Alhalafi and S.Paul, 6th Forum on New Materials, CIMTEC 2014,15-19June 2014), Montecatini Terme, Italy.
- ‘‘Organic Ferroelectric Non- volatile Memory Devices - Exploiting Ferroelectricity in Two-Terminal Memory Devices’’, Z.Alhalafi and S.Paul , CCESEN-2015, 14-19 October 2015, Kemer-Antalya ,TURKEY.

Chapter 2 Overview of Memory Devices

2.1 Introduction

This chapter will provide an overview of memory devices, which will include a definition and types of electronic memories. Moreover, there is an explanation of the characteristics of a memory cell through reviewing access time, number of cycles and retention time.

In information technology (IT) and devices such as mobile phones, computer laptops and iPhones, there is a requirement for some form of data storage of information or memory. Primary storage, which is mainly comprised of semiconductor memory, is used in computers and other digital electronic devices [6], [7]. Semiconductor memory is comprised of volatile and non-volatile memory and is organised into memory cells that store 1 bit each. Currently, there are emerging memory devices which are more effective in the storage of data as a result of technological advancement and the emergence of new technologies.

The origins of these devices can be traced back to the 1940s where the first programmable digital computers used thousands of octal base radio vacuum tubes. Acoustic delay line memory was later developed by Presper Eckert using glass tubes filled with mercury and plugged with quartz crystal [8]. In 1946, two alternatives to the delay line memory were developed referred to as the William tube and Solectron tube which utilised electron beams in glass for storage purposes. The first random access computer memory was later invented by Fred Williams and it had a larger memory capacity for storing thousands of

bits as compared to the selectron tube which could only store 256 bits, however, it was weak and sensitive to environmental disturbances [9] . A magnetic core memory was developed in the late 1940s by Ann Wang, Jan Rajchman and Jay Forrester which could recall memory even after power loss. This type of memory was used until the late 1960s when the transistor-based memory was developed. Technological advancements led to the development of very large memory computers which led to development of Random Access Memory (RAM) [10]. IBM is one of the companies that utilised modern technology to develop memory devices that were more effective.

Currently, technological advancement has led to the development of volatile and non-volatile memory, the former is computer memory which needs power in order to store the information, whilst the latter does not require power to store information [11]. Currently, there are about 13 types of non-volatile emerging memories being investigated. As a result of different types of emerging memory devices, comparisons have to be made in order to select the most suitable and various factors have to be considered such as maturity, read latency, write latency, endurance and energy [12]. Additionally, in terms of characteristics of device memory, factors such as memory cell, cycle endurance, and memory speed and retention time have to be considered [13].

2.2 Types of Memory

The two well-known types of memory device are volatile and non-volatile memory. Two examples of volatile memory include the static and the dynamic random-access memories (SRAM and DRAM) and they require power to maintain the stored information [14] and

if the power supply is switched off, or interrupted, the data is usually lost immediately. However, this research is concerned with non-volatile memory. Non-volatile memory such a s magnetised disks operates even in the absence of a power supply and is commonly referred to as Read Only Memory (ROM). Storage capacity of memory devices is defined in terms of bytes. Non-volatile memories can be further divided into Read Only memory (ROM) which include the Electrically Programmable ROM (EPROM) and the write-once read-many times (WORM); hybrid

non-volatile includes Electrically Erasable Programmable ROM (EEPROM), Ferroelectric RAM and flash memory [15]. Types of volatile and non-volatile memories are illustrated in figure 2.1 below.

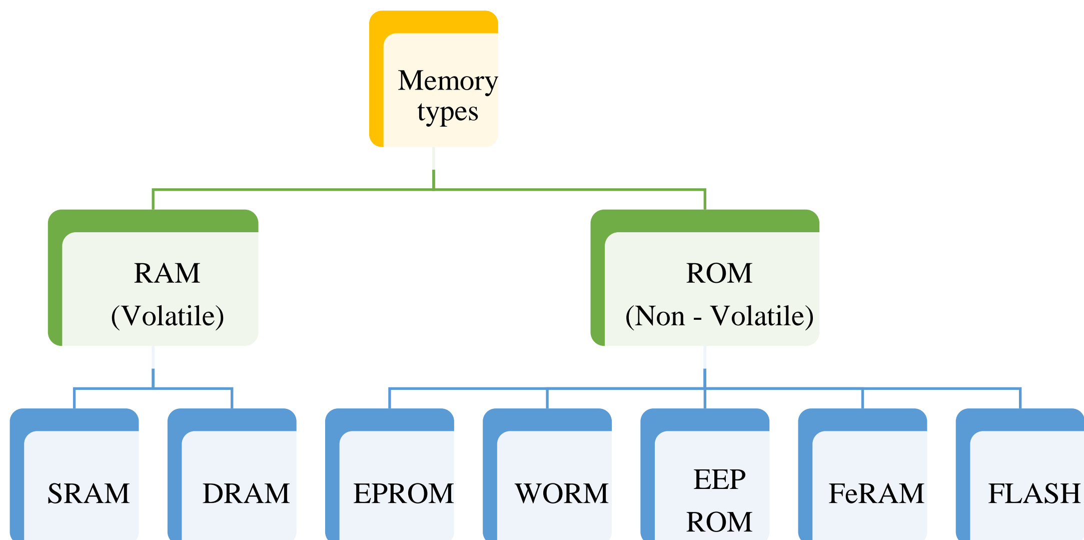


Figure 2.1 Classification of Electronic Memory.

2.2.1 Non-volatile memories (ROM-Hybrid)

There has been a surge in research for new generation storage devices which has been driven by an increasing demand for non-volatile memory cells [16]. Non-volatile memory refers to all types of solid states memory that do not require the contents of the memory to be periodically refreshed. This type of memory includes the Read Only Memory Hybrid. Non-volatile memory devices can retrieve information even after the power is turned off and back on again [17]. In most cases, non-volatile memory is employed as a secondary storage or a long term persistent storage. Moreover, these types of memories are mainly factory programmable and are mainly used for large volume products that do not require updates after it has been manufactured.

Much research is taking place to develop high speed non-volatile memory which includes WORM, EEPROM, EPROM, FeRAM and flash. Each type of non-volatile memory has its advantages as well as disadvantages, although flash memory is one of the common non-volatile memories that dominate the market [18]. Latency, cost as well as the capacity are important factors that have to be considered during the selection of non-volatile memories. Scalability as well as the issues of power consumption are also important considerations when selecting the non-volatile memory.

Write Once Read Many (WORM) is a data storage device in which information cannot be modified once it has been written. However, it is capable of storing data on a permanent basis and data can be read from this type of device repeatedly [14]. This type of storage device is important in ensuring that the data cannot be tampered with after writing [19]. This emerging technological device is important in ensuring that the data can be read

unlimited times once it has been written. WORM memory devices are often used to store databases, archival data, and other uses whereby there is a need for long-term reliability [14]. This type of memory device was developed after the invention of CD-R and DVD-R which are common WORM devices [20]. As a result of the technological advancements, there has been a renewed interest in the WORM devices. This includes the organic WORM components such as PEDOT: PSS. Other includes polymers such as PVK and PCz [21]. This is mainly because the organic WORM devices can be used as memory element for the low powered RFID.

Erasable Programmable Read Only Memory (EPROM) is a non-volatile memory chip that has the ability of retaining data when the power supply has been switched off. EPROM comprises floating gate transistors in an array formation that have been programmed by electronic devices that supply high voltage power. The data stored in EPROM can be erased once it has been programmed through exposing it to strong ultraviolet light source [22]. A single effect field transistor is part of the device and it is at the storage location. A surrounding layer of oxide is used for insulating the floating gate electrode which has no connection with other parts of the integrated circuit [23].

Flash memory is a non-volatile memory medium first developed in the early 1980s. With flash memory, the data stored can be reprogrammed or erased electrically [24]. Therefore, flash memory is non-volatile and rewritable [14]. NAND and NOR are the two commonly used types of flash memory, NOR allows bytes to be written to an erased location, and NAND allows for writing in blocks that are smaller as compared to the device. USB flash drives as well as memory cards and solid state drives utilize NAND. Flash memory is,

however, facing some challenges which include the ability to endure only a small number of write cycles within a specific block, although it does have a fast-read access time in comparison to dynamic RAM [25]. Other qualities of flash memory include high durability, mechanical shock resistance, ability to withstand high pressure, immersion in water and temperature. The flash memory has an advantage over some of the memory devices in terms of writing a large amount of data. The flash memory is suitable for mass storage device like the memory card since it is similar to the secondary data storage devices [26]. Common uses for flash memory include portable electronic systems such as digital cameras and PDAs [14].

Electronic Erasable Programmable Read Only Memory (EEPROM) is a non-volatile memory that is used for the storage of small amounts of data and allows for the erasing and reprogramming of individual bytes. This emerging memory device is organised in an array of floating gate transistor [27]. The modern EEPROM allows for multi-byte page operations which are an improvement from the past where it was limited to single byte operations. The life for reprogramming and erasing which was common in the past has been enhanced to millions of operations. Unlike some of the non-volatile memories, this memory device can be reprogrammed while the computer is still in use [28].

FeRAM is one of the emerging technology devices that are replacing EEPROM [29]. It is a non-volatile memory device that utilises a combination of the fast read and writes access for the DRAM cells which are comprised of transistors and capacitor structure. The dielectric state of the capacitor is usually sensed through the transistors and the ferroelectric state which has to be activated. The polarisation properties of the

ferroelectric substances are mainly used in the memory device. Lead Zirconate titanate is commonly used for the development of the memory device [30]. Currently FeRAM is considered as the most commonly use non-volatile memory device for personal computers. FeRAM maintains data even where there is no power supply, achieved through the use of ferroelectric material instead of the commonly used dielectric material situated between the two plates of a capacitor and the application of an electric field usually leads to the polarisation of the ferroelectric material. The main limitation of FeRAM is a destructive read cycle [31], however, it has the potential of enduring a high number of cycles even when operating with a very low power supply.

These types of memory devices are also used widely in small consumer devices which includes personal digital assistants and smart cards. Currently, this memory is much quicker than the flash memory and it will replace other non-volatile memories such as EEPROM [32]. It is also set to become a major component in wireless products of the future. In terms of power consumption, FeRAM only requires power during the process of reading or writing a cell. The performance of this memory device is based on the movement of atoms when exposed to an external field, and this process is extremely fast and contributes to the high speed of the device. However, reliability of the device is an issue due to the problem of imprint and fatigue resulting from minimum voltage during the writing process [32].

2.3 Memory Devices Structures

Generally, from a structural perspective there are three main types of non-volatile memory device, these are transistor-type, capacitor-type and resistor-type [16]. With their respective ability to amplify electronic signals, to store charge, and to produce electric currents, electronic memory devices can be made from transistors, capacitors and resistors [33]. The present research is concerned with capacitor- and resistor type memory devices which are described below.

2.3.1 Capacitor-Type

Capacitors can store charges between two parallel plate electrodes upon application of an electric field. According to the amount of charge stored within the cell, the bit level (either "0" or "1") may be encoded accordingly. When the medium found between the two electrodes is only dielectric, the stored charge will eventually be lost [34]. Thus, DRAM using a dielectric capacitor is volatile memory, which means that any information stored in DRAM will eventually fade except in the case where the capacitor charge is periodically refreshed. However, if the medium is ferroelectric, permanent electric polarisation can be maintained and a longer retention time is possible. A ferroelectric material is capable of maintaining permanent electric polarisation which can be switched between the two stable states using an externally applied electric field. Therefore, memory that is based on ferroelectric capacitors is non-volatile [35]. FeRAM does not need to be periodically refreshed and it still keeps the data even in the event of a power failure. Organic and polymeric ferroelectric materials can also be used in DRAM and FeRAM applications [36], [37]. There are a number of different FeRAM structures, which

include 1T1C (T – transistor and C – capacitor), [38] 2T2C [39] and 1T2C [40]. The simplest DRAM and FeRAM cells have similar structures, both utilizing 1T1C as the building components.

2.3.2 Resistor-Type

Devices that include switchable resistive materials are resistive random-access memory (RRAM) or resistor-type memory. In contrast to transistor and capacitor memory devices, a specific cell structure is not needed for resistor-type memory and does not require integration with complementary metal-oxide-semiconductor (CMOS) technology because data is stored differently using electrical conductivity states (ON and OFF) and bistability is achieved through the properties of the material which can include phase change and charge transfer [33]. This type of structure, which has an active layer which is sandwiched between two electrodes, means that a three-dimensional stacking structure can be fabricated to achieve high-density data storage [16]. Resistor type memory devices store data in a different form, such as, according to different electrical conductivity states, i.e. ON and OFF states. For two-terminal resistive memory it is the electrical bistability that defines data storage and access [16]. In fact, it is the structural simplicity of resistive memory devices that allows the synthesis of materials for resistive devices [16]. Electrical bistability is usually a result of changes in the intrinsic properties of the material, for example phase change, charge transfer, conformation change and reduction–oxidation (redox) reaction, all as a response to a voltage or electric field [41].

Resistive electronic memory usually has a basic structure with an organic/polymer film located between two electrodes placed on a substrate (glass, silicon wafer, plastic or metal foil). The configuration of the top and bottom electrodes is either symmetric or asymmetric, whereby aluminium, gold, copper, p-doped or n-doped silicon are used. The basic configuration of a memory device used for testing is shown in Figure 2.2 a. The individual memory cells are integrated into the cross-bar (two-dimensional) memory array (Figure 2.2b), and further stacked into three-dimensional data storage devices (Figure 2.2 c). Each cell in the 2D memory array or 3D stacked device can be identified by its unique Cartesian coordinates. Due to the two terminal simple structures and the nanoscale active organic/polymer thin film, high data storage density can be realised in organic/polymer memory [42].

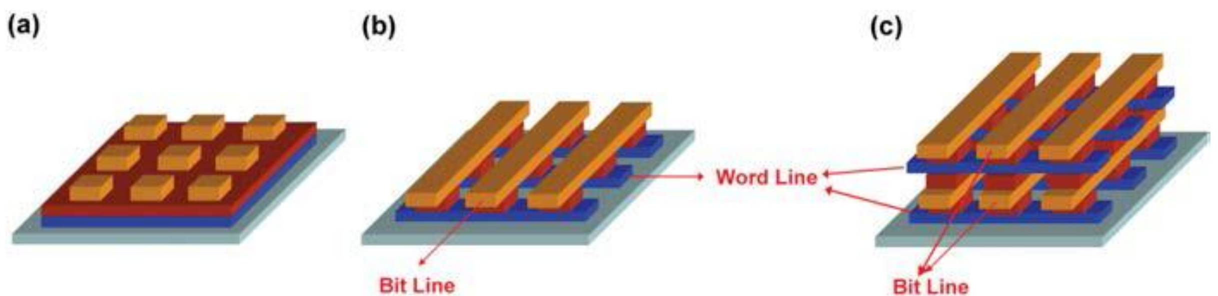


Figure 2.2 Schematic diagram of (a) a 3 × 3 polymer memory device, (b) a 3 (word line) × 3 (bit line) cross-point memory array, and (c) a 3 (layer) × 3 (word line) × 3 (bit line) stacked memory device9 [33].

Resistor-type memory is based on the change of the electrical conductivity of materials according to the applied voltage the most widely reported mechanisms include filament

conduction, charge transfer effects, space charges and traps, and conformational changes[42].

2.3.2.1 Space Charges and Traps

The intrinsic electrical conductivity of polymer and organic materials is much lower compared to metals. When the electrode–film contact is ohmic, charge carriers are easily injected into the organic thin film from the electrode and accumulated near the interface to form a build-up of space charge. The electrostatic repulsion between the individual charges can screen the applied electric field and further limit the injection of charge into the film [43]. Consequently, hysteresis of the current–voltage (I–V) characteristics is observed. Space charges found in materials may be the result of a number of different sources which include electrode injection of charge carriers, accumulation of mobile ions at the interface between electrode and organic film, and ionized dopants found at interfacial depletion areas.

Capacitance–voltage (C–V) characteristics can also show hysteresis arising from space charges [44]. The hysteric behaviour, either in I–V or C–V characteristics, can be employed to make data storage devices. A device may be programmed through applying a voltage pulse to write a state, the device current is then read using a small probe voltage. When traps are present either in the bulk of the material or at the interface regions, the charge carrier mobility will be significantly reduced. Adsorbed oxygen molecules in organic films [45] intra-molecular donor–acceptor structures [46] and semiconductor or metal nanoparticles [47] can act as charge trapping centres. As greater numbers of charge carriers are injected with increasing voltage, the traps in the organic thin film are

gradually filled [45]. When all of the traps are eventually filled, the injected charge carriers will no longer be affected by the fully filled traps, thus, electrons injected from the electrode exceed the equilibrium concentration, and therefore, will dominate the conduction as seen in space charge limited conduction (SCLC). A sudden increase in the current can be seen, and the transition between OFF to ON states is linked to the occupancy level of the charge traps. The current is restricted due to the re-excitation (de-trapping) of the trapped carriers in the trap-filled state [48]. Both space charges and traps are important in the electronic processes and switching behaviour of organic electronic devices [49].

2.4 Bistability

Resistive random-access memory is based on the idea of resistive switching and has its origins in a sudden change in resistance which offers a bistable state [50]. Data storage and access are the result of the electrical bistability which is the high resistance 'ON' state and low resistance 'OFF' state [16].

The bistable bipolar switching that has been revealed by loops or hysteresis of the I–V curve has the potential use of the phenomenon of bistable switching in memory devices [51] and bistability with a non-volatile hysteresis has been used in organic memory elements [52]. The specific mechanism works whereby for an increasing voltage from 0V there is very little current flow and therefore, at low voltage the material is in the high resistance state (off state) and at a specific threshold voltage the current increases several fold which is the resistance state (on state) which will continue even where the voltage

decreases to below the threshold voltage, upon further decrease in the voltage the material will return to the off state [53].

These characteristics are found in organic materials referred to as “charge transfer complexes” [53] and such materials are known as organic bistable materials and exhibit aforementioned characteristics [53]. Specifically, such charge transfer complexes are molecular compounds made from two molecules of an electron donor and an electron acceptor molecule and it is the control of the ratio of these molecules that is required for the mechanism [53]. In fact, one of the promising properties of organic materials has been their electrical bistability which has been attributed to the chemical structure whereby bistability is due to the existence of two stable resistance values from a single applied voltage [53]. New data storage technology such as ferroelectric random-access memory (FeRAM) and organic polymer memory, are increasingly based on the electrically bistable materials which provide polarity upon application of an electric field [33].

2.5 Memory Device Characteristics

2.5.1 Memory cell

Semiconductor memory storage usually store the data in small memory cells comprising of capacitors and transistors, commonly made from silicon. In flash memories, each memory cell has the ability to store 1 bit of information and thus the cells have the ability of storing large amounts of information [27]. This is for the purposes of ensuring that a charged storage layer is formed. In NOR flash memories, the cells are usually connected in a parallel formation with bit lines that play an important role in ensuring that the cells

can be programmed or read individually. However, in the NAND flash memory, cells are connected in a series formation and consume little space as compared to the cells connected in parallel.

FeRAM cells consists of capacitors and transistors and access is through the use of transistors which allows sensing of the ferroelectric state of the capacitor dielectric. As a non-volatile memory, FeRAM cells have the ability of storing data without any external supply due to the use of ferroelectric materials [27].

The DRAM cell also has one capacitor and one resistor with its state being kept at the capacitor. The transistor is used for providing access to the state. When writing to the DRAM cell, the access line has to be raised for a period sufficient enough to charge the capacitor while the drain line has to be set appropriately. A DRAM cell being small allows for greater memory density and low cost manufacturing cost [29]. A drawback of the DRAM cell is that it requires refreshing on a frequent basis. The DRAM cells are usually grouped together in an array structure referred to as banks.

The development of the EPROM cell was based on a faulty integrated circuit. Each of the cells consists of a single field effect transistor, an insulating layer of oxide and a conductive layer of either silicon or aluminium. Voltage plays an essential role in controlling the state of the field effect transistor. The EPROM cell is quite sensitive to UV light which has the potential of erasing the data stored, although it does have the ability to retain data over a long time [22]. The EEPROM Cell is much smaller in size compared to the EPROM cell. The cells are usually organised in arrays comprised of floating gate transistors. The cell also has a thin gate oxide layer which is used for

enabling the chips to erase the bits, different to EPROM which requires UV light. The cells can be reverted back to erased state if electrons are injected in the floating gate drifts via the insulator [22].

2.5.2 Cycle endurance

Cycle endurance is defined as the capability of a memory device to perform continuously. The program erase cycles are mainly used during the process of quantifying the cycle endurance. It is mainly used in the flash memory device. In a flash memory device, the cycle endurance could be as low as 100 erase cycles for a flash memory. However the endurance cycle may also be as high as 1,000,000 erase cycles for a typical flash memory [54]. The cycle endurance is important in determining the ability of the memory device to wear out. Most of the flash memories in the market have a P/E cycle of 100,000. Engineers from Micronix revealed in 2012 that they will develop a NAND flash memory with the ability to endure 100 million cycles. The device will however utilise a self-healing mechanism that will require on-board heaters.

FeRAM is a fast memory and it has the ability to endure a high number of cycles and enduring up to 10^{14} cycles and hence making it faster as compared to the flash memory. The higher the endurance cycle, the more durable and faster the device is. DRAM and SRAM are also considered as a fast memory due the high endurance cycle. The endurance cycle for both SRAM and DRAM is greater than 10^{12} [54] [55]. This indicates that both the SRAM and DRAM memories are much faster compared to the flash. It is also for this reason that it used as the main memory in a personal computer device. The number of writes have a significant role in determining the memory device endurance. Other

memory devices including EEPROM, EPROM and WORM have an endurance of up to 10^4. This is an indication that they are not fast enough, and such devices can easily wear out depending on the amount of data.

2.5.3 Memory speed

The volatile memory has a higher speed as compared to non-volatile memory. The speed plays an essential role in determining its efficiency in terms of reading and writing the information. SRAM and DRAM have relatively high speed as compared to most of the other types of memory. SRAM has a memory speed of 5 ns [19]. This is considered as a very high speed when dealing with memory devices. DRAM is considered a high speed memory device as its memory speed is about 10 ns. The memory speed of non-volatile memory devices is relatively slow, except in the case of memristive switching mechanisms which have exhibit fast bipolar non-volatile switching [56]. However, a high speed memory device is linked to high power consumption. EPROM has a relatively low speed which affects the rate at which it is able to read and write the data. The speed of EPROM is up to 40 ns. This is a relatively slow speed as compared to most memory devices. However, its power consumption is quite low as compared to high speed memory devices.

FeRAM has low read and write time as compared to other memory devices such as DRAM and SRAM. The memory speed of FeRAM is about 50-60 ns which is relatively slow. It may therefore take a long period of time to carry out different activities when using the FeRAM device. The flash memory is also low, at about 20 ns [19]. This is however, higher as compared to some non-volatile memories. The memory speed of

WORM devices is however quite low at 80 ns compared to most memory devices. EEPROM is also relatively slow in terms of speed. However, technological advancement is likely to improve the speed of memory devices. This will play a significant role in making sure that the reading and writing processes are much faster and improve the effectiveness and efficiency of memory devices.

2.5.4 Retention time

Retention time is the duration that the data is able to be stored in the memory device. Non-volatile memory devices have the potential of retaining the data over a long period of time as compared to volatile memory. DRAM and SRAM have a relatively a small retention time as it is dependent on the availability of power supply. The retention time of DRAM is 16 ms which is relatively low [6]. The retention time for SRAM is similar to DRAM as it is also dependant on the availability of the power supply. It is such characteristics that make the volatile memories suitable for use in the main memory. The non-volatile memory devices such as WORM can retain data over a long period of time. Once data is stored in the device, it cannot be modified or tampered with. This means that the data can be stored for as long as the lifespan of the device. However the device does not have a long lifespan as compared to most of the non-volatile devices. This may impact negatively on its ability to retain the data over a long-time period.

EPROM has the ability of storing data over long-time periods. Most of the EPROM devices have the ability of retaining data for a period of 10 to 20 years. However, other devices have a retention time of up to 35 years. This is an indication that the device can be useful when data is required over a long period of time. EEPROM has a guaranteed

retention of period of 10 years [6]. This is the minimum period that the memory device can store data. However, depending on the manufacturer, the device may store data for more than ten years. The flash memory device is also known for long retention time. The data can be retained in the flash device for over ten years. This can be attributed to the physical characteristics as well as the quality of the flash device. Currently a lot of research on the flash memory device is on-going. This may see the device being able to store data for a much longer period of time. FeRAM has the potential of retaining data for a high period of time just like the other non-volatile memory, for a period of more than 2 years. The retention time for the memory devices is set to be increased in future due to technological advancement. However, data is a factor that may affect the selection of the device by the user.

2.6 Summary

This chapter has provided an overview of memory devices, their types, classification and characteristics towards an understanding of the memory devices tested in this research. Specifically, the types of memory device were addressed towards an understanding of the non-volatile devices, as well as classification which included resistor and capacitor type memories and device characteristics which included cycle endurance, memory speed and retention time. The following chapter presents a detailed overview of two-terminal non-volatile memory devices the specific device type considered in this study.

Chapter 3 Two terminal NVM devices and Charge Transport Mechanisms

3.1 Introduction

Two-terminal NVM memory devices are comprised of materials which include nanocomposite, semiconductors or insulators that are sandwiched between two electrodes. This structure allows them to show two different stable electrical states controllable through the application of an external electrical field. These two stable states, which are ON and OFF, exhibit resistive, capacitive or ferroelectric properties according to device structure [56], [57]. The simple structure of two-terminal NVM devices means that the scaling capability is much improved in comparison with existing floating gate MOSFET flash memory devices. The width of both the bottom and top electrodes as well as the width of the material between them determines scalability, moreover, the structure allows for ease of integration into electronic circuits. This integration is especially easy in a crossbar structure whereby the bottom electrodes are deposited onto the substrate, illustrated below in Figure 3.1.

Generally, non-volatile memory (NVM) devices come in two types according to how they are stimulated and controlled. The first type is those that are mechanically addressed, and examples include optical disks, hard disks, floppy disks and magnetic tapes. The second type, which are of concern to the present study, are those NVMs that are electrically addressed and are categorised according to structure, mechanism and electrical value for ON and OFF states.

Each area where there is a cross between the two electrodes is a storage memory cell, although it should be noted that control and external stimulus of each memory cell in this structure is not simply due to the applied stimulus causing leakage currents in neighbouring cells; this is referred to as cross talk interference. The problem may be resolved through a transistor or diode for the cells that will block or allow the current to reach the cell [58].

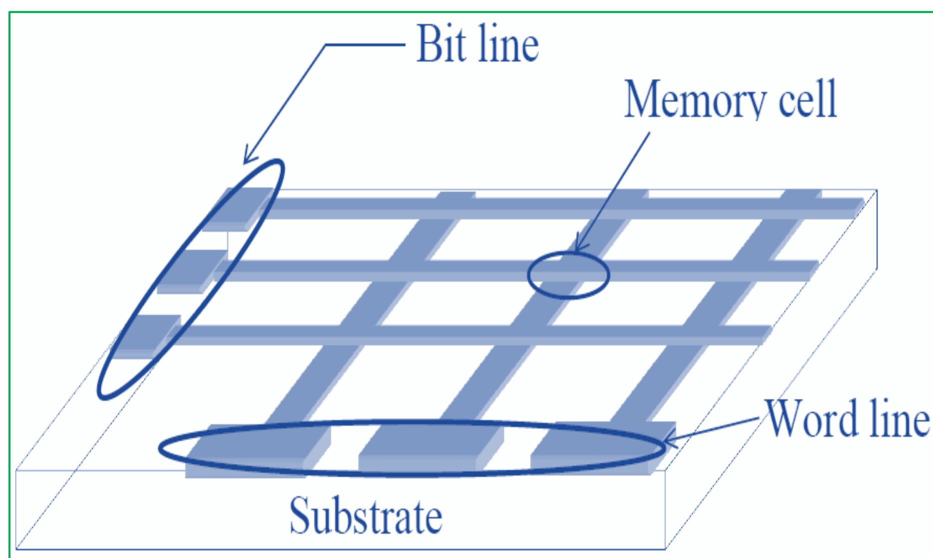


Figure 3.1 2TNVM cross bar structure.

Two-terminal NVM devices can also be integrated into architectures whereby a third dimension, specifically a stack of memory cells which is separated by an insulator, can be included in the memory stack. This vertical stack architecture allows increased memory storage, while at the same time maintaining performance. Additional layers can

be added to the top of the memory stack to allow more memory devices in the same substrate area.

The life time endurance of this type of memory device varies for different structures of two-terminal NVM devices, in fact over 10^5 cycles has been shown in devices which compares well to flash memories [59] [60]. In the following sections different types of 2TNVM devices are reviewed in addition to the MIM memory structure and different types of MIM memory.

3.2 Memristor

It was theorised in 1971 by Leon Chua that there was a fourth passive circuit element in addition to the already known resistor, inductor and capacitor, however this theory was not accepted by the community until 2008 when a device was made that behaved according to the properties of the theorised memristor, this was shortly followed by a way to build a device to create a non-volatile memory [61] [63]. This was demonstrated by Strukov et al. (2008) [64] by showing that memristance can occur naturally in nanoscale systems whereby solid state ionic and electronic will be coupled together when an external voltage is applied [64].

A memristor is a memory device that regulates the flow of current and effectively remembers the charge that has passed through [65]. In 2008 the head of the research team, Stanley Williams said that "A memristor is a two-terminal device whose resistance depends on the magnitude and polarity of the voltage applied to it and the length of time that voltage has been applied. When you turn off the voltage, the memristor remembers

its most recent resistance until the next time you turn it on, whether that happens a day later or a year later" [66]. Furthermore, the mechanism has been likened to water flowing through a pipe, where the water is the electric charge and the obstruction from the resistor is where the pipe narrows, so that the narrower the pipe, the higher the resistance, and a memristor is a pipe that will either expand or contract according to the amount and direction of the water (current) thus increasing or decreasing the resistance [66]. The specific mechanism is that the memristor remembers the diameter when charge last passed through, when the current is switched off the pipe retains it diameter [66]. Nanoscale resistive switching elements such as TiO_2 have received much attention in more recent years because they exhibit memristive behaviour which has shown great potential in non-volatile memories [67]. However, using a metal-oxide – based devices also have capacitive and inductive components showing a mix of memristive, memcapacitive and meminductive effects [68].

3.3 Oxide Based-Memory

Metal oxide semiconductors are used because metal oxides show resistance switching properties [63]. Oxides as insulators can undergo sudden switching to a conductive state, something that has been known about for decades. The first experiments that observed resistive switching in oxide materials were conducted by Hickmott in 1962 [69]. Specifically, Hickmott experimented with five oxide films which included Al_2O_3, Ta_2O_5, SiO_x, TiO_2 and ZrO_2 and found resistance in their current-voltage characteristics [70]. Interest in the resistive switching mechanism of metal oxides was revived in the 1990s, firstly, with complex metal oxides which included $SrZrO_3$ and $SrTiO_3$ and then with

binary metal oxides which included TiO_2 and NiO [71]. Furthermore, in 2004 Samsung presented a paper about the use of NiO in which they measured programming characteristics, data retention and endurance towards suggesting the use of resistive switching in memory technology [71]. There has been much interest in HfO,, AlO_x, TiO_x, NiO_x and TaO_x and they have been studied in recent years due to their properties which include being defect rich, lower reset currents, high retention times, bipolar and unipolar switching and good endurance [71].

Oxide materials that exhibited resistive switching behaviour can be categorised as binary, ternary and complex oxides and from these binary oxides have been the most investigated because they are easy to fabricate, and they give good stability [70].

In reference to these resistive switching properties of metal oxides, the structure or phase transition is attributed to different defects, specifically, linear, point or planer defects, and resistance changes occur when there is an evolution of these defect structures triggered by the application of an electrical field [70]. The switching modes of metal oxides can be unipolar or bipolar [71].

Often metal oxides are used as the active material as blend with polymers in organic memory devices and there are numerous examples which include barium titanate [72] and zinc oxide (ZnO) [73] [74][75].

3.4 Organic NVM

Organic-based electrical memory devices are electrical memory devices with active layers composed of carbon-based materials (small organic molecules and/or polymers) as opposed to inorganic materials. These organic active layers are deposited either by spin-coating, drop-casting or by dip-coating [76]. Their structure is simply a top and bottom array of electrodes structured as cross points with the organic active materials located between them. A detailed history and review of these memory devices have been presented by Prime 2010 [77]. A summarised presentation will nonetheless be given here. Depending on the type of organic active layer, three different categories of organic-based electrical memory devices can be distinguished. These categories include the resistive switch and the write once and read many times (WORM) wherein the active organic material is a resistive polymer admixture. Dependent on the type of resistive material employed in the cell formed by each cross-point of both electrodes, the device will electrically "short" resulting in a low resistance compared to the pristine state, the second type behaves as a blown fuse providing a higher resistance than the pristine state.

The second category is the molecular memory device (MMD) in which the active material is comprised of small organic molecules placed in an ordered way so that one end of the molecule is connected to the bottom electrode and the other end of the molecule is connected to the top electrode. Application of a voltage alters the molecules' conductivity, allowing data to be stored in a non-volatile way. The data is erased by applying a voltage of opposite polarity.

The third category is the polymer memory device (PMD) [78]. This is similar to MMD and WORM but different in that the organic material also has nanoparticles or some other molecules in the admixture. An applied voltage across a memory cell creates a change in the polymer admixture's conductivity, allowing a bit of data to be stored. The use of polymers is discussed in more detail below.

3.4.1 Use of Polymers in two-terminal NVM

The research here uses a polymer as the insulating material in both MIM and MIS devices. Specifically, PVAc is used and this requires a review of work in this area. In the present study different layer thicknesses are tested. Various types of polymers have been used in NVM together with active materials to achieve electrical bistable behaviour. Polymers are used as a matrix and as an active component [78]. These devices are referred to as Organic Bistable Devices (OBDs) and they are combined with nanoparticles to offer distinct memory characteristics [73]. These materials have properties which cannot be found in inorganic semiconductor devices such as mechanical flexibility and low production cost [78]. Similarly, the use of organic devices means that the materials can be tailored to suit specific purposes, allow for simple device structures, are compatible with flexible substrates and can be manufactured at low temperatures [72].

In reference to structure polymer memory devices comprises of organic material between two electrodes and the organic material is comprised of an active material mixed within a polymer matrix [79].

There are number of theories that have been proposed to explain bistability behaviour which include electronically induced charge transfer, formation of conductive filaments, a change in material properties due to the presence of nanoparticles and conformational change [80].

Prakash et al. (2006) [78] investigated the use of poly (3-hexylthiophene) with gold nanoparticles which was shown to exhibit electrical bistability. Their device exhibited a transition from a charge-injection-limited current to a trap-controlled current induced by an electric field [78]. Similarly, polyaniline was also used with gold nanoparticles which created a switching mechanism as a result of the charge transfer, induced by the electric field, from the polyaniline to the gold nanoparticles [81]. PMMA (poly methyl methacrylate) has been used as an insulating polymer layer with ZnO which also exhibited non-volatile electrical bistability [75]. Poly-vinyl-phenol (PVP) was used with C_{60} Fullerene where PVP as a polymer was an insulating material (Paul et al., 2005) [82].

3.5 Phase Change Memory

Phase change memory is a result of a change in resistance due to a switching between the amorphous and crystalline state when a current is applied. Chalcogenide resistive alloys are commonly used for phase change memory because these types of material have the ability to switch between the amorphous and crystalline phases. Specifically, when the material is in the amorphous phase there is no order in the crystalline lattice which has high resistivity, when it changes to the crystalline phase, where there is a regular crystalline structure, there is low resistivity [76] [83]. It is the difference between these

two resistive states that is exploited in phase change memory. It has been claimed that as an emerging non-volatile technology, phase change memories or PCM, are the most promising in terms of scalability and performance [84]. PCMs were first proposed in the 1960s where reversible memory switching was observed in chalcogenide materials [84].

Data retention and endurance of PCM has been measured and it has been found that data can be stored for more than 10 years [85]. It is one of the potential factors of PCM that it is suitable for fast programming and reading together with programming endurance. This has been supported because of the good signal sensing margin between the two states which allows for fast programming, endurance, low cost and scalability [83].

The process of PCM is illustrated in Figure 3.2 (b) whereby the high resistivity represented by the red line is the amorphous state of the material, and where there is an increase in the current (mA) the material transitions to the crystalline state where there is low resistivity represented by the black line. In order to achieve the switching (SET and RESET as shown in Figure 3.2 (b)) the bias is increased above the switching voltage which means that there is enough current flowing through the cell to heat up the active region which is shown in Figure 3.2 (a) [87].

It is important to note that although the resistive switching in PCM is unipolar as a result of the asymmetry of the mushroom cell, the applied polarity is also an important consideration, and that it has been shown that an incorrect polarity can lead to unreliable switching due to dissimilar material segregation effects. However, there have been some disadvantages reported to PCM, which are a disadvantage in terms of commercialisation

and include a large programming current which makes it difficult to achieve high density PCMs [76].

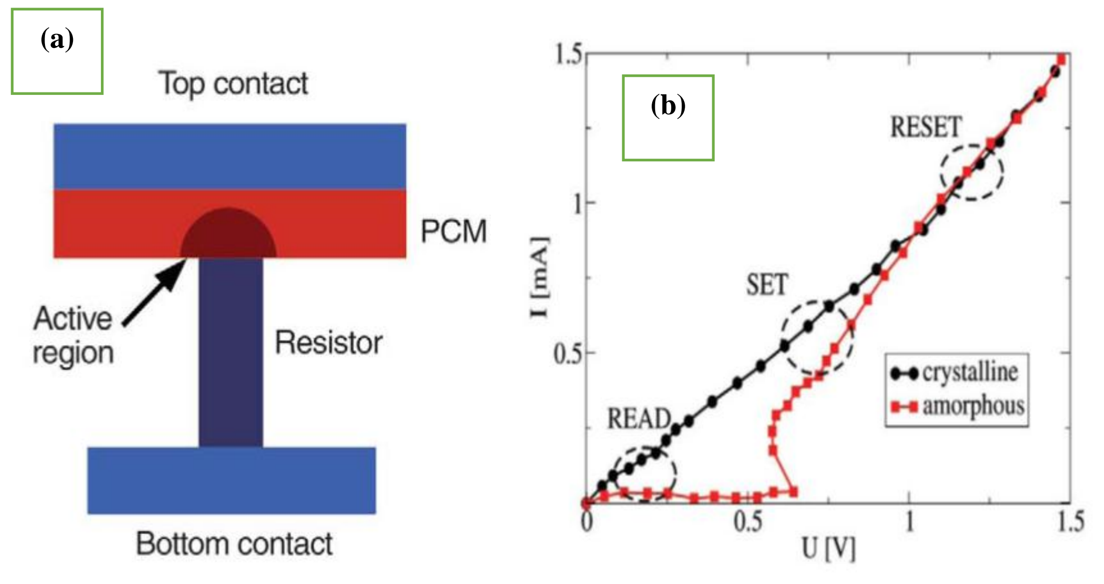


Figure 3.2 (a) Cross-section of PCM cell, (b) I-V characteristics of the set and reset states (Reprinted with permission from [86] © 2008 IEEE [87].

3.6 Magnetoresistive RAM

The development of magnetoresisitive RAM (MRAM) has included cross-tie RA and Anisotropic Magnetoresistance materials and then later the use of Giant Magnetoresistance which have higher resistance [88]. A magnetoresistive readout scheme was first proposed by Jack Raffel where he stored data in a magnetic body which resulted in a stray magnetic field [88].

Early magnetic RAM employed the natural hysteresis found in magnetic materials for the writing of memory and reading was achieved using magnetoresistance of the same place where the data is stored [88]. This type of memory is a combination of the magnetic tunnel junction and CMOS technology [76]. It has a 1T1R cell structure which is similar to phase change memory, however, the single resistor is the magnetic tunnel junction (MTJ) and the memory function is achieved through modulating the MTJ's resistance [76].

3.7 Charge transport mechanisms

For the investigation of this study an important concept that needs to be considered is the charge transport mechanisms of the different materials that are tested in this study. Although an ideal insulator will not conduct electricity, this is not often the case where a high electric field is applied where conduction will take place. Some transport mechanisms depend on the electrical property at the interface between the electrode and the active material and some depend on the properties of the active material itself such as charge trapping. The study is concerned with memory devices where the insulating material is thin which makes conduction more likely. Here the possible charge transport mechanisms are introduced.

3.7.1 Poole-Frenkel

The Poole-Frenkel effect is the way that an insulator conducts electricity. Electrons will move slowly through an insulating material because they get trapped in trap sites. When the electron has enough thermal energy, as the result of the application of an electrical field, it will be freed from the localised trapped state, or valance band and will move to

the conduction band allowing conduction to take place. The Poole-Frenkel effect describes how the electron does not require much thermal energy to enter the conduction band because part of the energy that it does require comes from the pulling effect of the electric field, therefore, not requiring a large thermal fluctuation. Thus, Poole-Frenkel emission is a bulk limited process with field-enhanced thermal excitation of trapped electrons in the insulator [89].

More specifically, in this mechanism the electric field will decrease the potential of the Coulombic barrier to prevent the electrons jumping to the conduction band and therefore, will allow the electrons to become thermally excited and leave the traps [90]. In this mechanism of the field-assisted emission the barrier decreases by an amount proportional to the square root of the applied electric field [91].

A Poole–Frenkel transport of carriers through traps leads to a current which is linear with voltage for very small voltages and exponential for high voltages [92]. The Poole-Frenkel conduction mechanism has been seen in the HRS of a number of different switching devices with materials such as ZnO [93] [94], SnO_x [95], ALO_x [96] and WO_x [97].

3.7.2 Schottky mechanisms

In the Schottky transport mechanism, where the electrons are emitted from an electrode, the electrode will become negative in relation to its surroundings which creates an electric field at its surface. The Schottky emission or thermionic emission takes place when the electrons are thermally-excited and can cross the energy barrier between the electrode and insulating material, therefore, the electrons pass into the conduction band of the insulating layer [90]. Therefore, Schottky emission is a conduction mechanism that is contact limited whereby the current is

limited by the thermionic emission over the barrier between the electrode and the insulating material [77].

It is important to note that this is a thermionic process that depends more on the thermal fluctuation of the electrons from a higher temperature than the Poole-Frenkel mechanism which depends to a lesser extent on thermal fluctuation in addition to the puling effect of the electrical filed. Schottky emission has been suggested as the conduction mechanism in a number of different switching devices by, among others, Huang *et al.* (2010) with Ti /TiO_2 /Pt [98], Mondal *et al.* (2014) with Ni/Sm_2O_3/ITO [99], and Syn *et al* with Ti/HfO_x/TiN [100].

3.7.3 Fowler-Nordheim and Direct Tunnelling

Fowler-Nordheim tunnelling is through a triangular barrier, as could be the case at higher electric fields [77]. Electron tunnelling in the Fowler-Nordheim tunnelling mechanism involves the wave-mechanical tunnelling of an electron through a rounded or exact triangular barrier. There are two states in this mechanism which are firstly, when the electron in the localised condition where no voltage is being applied and therefore, there are flat energy levels, and secondly, when the electron is not strongly localised and is a travelling wave as a result of the application of voltage causing a shift in the energy levels. In reference to the latter, the electrons are emitted from the metal electrode to the conduction band. Where a high electric field is applied the nature of the conduction band is triangular and Fowler-Nordheim tunnelling takes place. It is important to note that in this mechanism the higher the applied voltage the higher the likelihood that the tunnelling will take place and there is a reduction in the width of the energy barrier. With direct tunnelling, where tunnelling across the material also takes place, the mechanism is through a square barrier. Furthermore, direct tunnelling is more likely to be the

conduction mechanism where the material is less than 3nm [101], as opposed to Fowler-Nordheim tunnelling which would take place with a thicker material.

3.7.4 Space charge limited current (SCLC)

Within the space charge limited conduction mechanism, the current occurs through charge carriers injected from the electrode, where no compensating charge can be found in the insulator [77]. The evidence for this type of conduction mechanism is a quadratic characteristic of the current-voltage (I-V) hysteresis. Specifically, for the trapped controlled SCLC there are three portions which are the Ohmic region ($I \propto V$), Child's square law region ($I \propto V^2$) and finally, the steep increase in the high field region [89]. It is possible to identify the SCLC mechanism where Ohmic conduction is seen at a low field after which there is a power law dependence observed in a high field, and in this low-field regime the conduction mechanism is the result of free electrons that have been thermally generated [90]. When the field becomes higher than the square-law voltage the amount of electrons injected from the electrode exceeds the equilibrium concentration, and therefore, will dominate the conduction [90].

The SCLC conduction mechanism has been reported as the main mechanisms by Liu *et al.* (2008) with Au/Cr/Zr^+ implanted ZrO_2/Si [102], Wang *et al.* (2010) with Ti/Cu_xO/Pt [103] and Zeng *et al.* (2014) with Pt/ZrO_2/TiO_2/Pt [104].

3.7.5 Ionic and Ohmic Conduction

Ionic conduction involves movement of ions as a result of the applied electric field, specifically, ionic impurities move through the active material where a high electric field

is applied. Ohmic conduction is attributed to mobile electrons that are the result of thermal excitation at high temperatures. The current density expressions and electric field and temperature dependency of ionic and ohmic are shown in Table (3-1)

Table 3-1 Summary of the expressions for the potential conduction mechanisms for the dielectric film [89].

Conduction Mechanism	Current Density Expression	Voltage Dependence	Temperature Dependence
Poole-Frenkel Emission (P-F)	$J_{PF} = \frac{V}{d}\, exp\left[\frac{-q\left(\emptyset_B - \sqrt{e(V/d)/\pi\varepsilon_0}\right)}{KT}\right]$	$\ln(J) \sim \ln(V)\, \beta$	$\ln J \sim \frac{\beta}{T}$
Schottky Emission (Sh)	$J_{Sh} = A^{*}T^{2} exp\left[\frac{-q\left(\emptyset_B - \sqrt{e\,(V/d)/4\pi\varepsilon_0}\right)}{KT}\right]$	$\ln(J) \sim\ 2\beta V^{1/2}$	$\ln J \sim \ln T^{2}\, \frac{2\beta}{T}$
Fowler-Nordheim tunnelling (F-N	$J_{FN} \sim \left(\frac{V}{d}\right)^{2}\ exp\left[\frac{-4d\emptyset_B^{3/2}\,\sqrt{2qm^{*}}}{2hE\,V/d}\right]$	$\ln\left(\frac{J}{V^{2}}\right) \sim \frac{\alpha}{V}$	none
Direct Tunnelin	$J_{DT} \sim V\, exp\left[\frac{-2d\,\sqrt{2m^{*}}\emptyset_B}{h}\right]$	$J_{DT} \sim V$	none
Space charge limited conduction	$J_{SCLC} = \frac{9}{8}\, \varepsilon_i\, \mu\theta\, \frac{V^{2}}{d^{3}}$	$J_{SCLC} \sim V^{2}$	none
Ionic Conduction	$J_{ic} = \frac{V}{dT}\, exp\left[\frac{-\Delta E_{ai}}{KT}\right]$	$J_{ic} \sim V$	$\ln(JT) \sim \frac{\alpha}{T}$
Ohmic Conduction	$J_{ohc} = \frac{V}{d}\, exp\left[\frac{-\Delta E_{ae}}{KT}\right]$	$J_{ohc} \sim V$	$\ln(J) \sim \frac{\alpha}{T}$

In the above table (Table 3-1) J represents the current density, A^* represents the Richardson constant, ϕ_B the barrier height, ε_i the insulator permittivity, m^* is the effective mass, d is the insulator thickness, μ the charge carrier mobility and E_{ae} represents activation of electrons and E_{ai} the activation energy of ions. The device dependent constants are α, and β.

3.8 MIM Memory

The MIM memory structure is used in the experiments of this research to determine memory characteristics of the tested materials, specifically, the charging mechanism using I–V measurements and memory programming using WRER cycles. Here the MIM structure and functionality is reviewed.

3.8.1 Resistive switching in MIM

Resistance switching has been of interest for over 40 years and was first observed as negative resistance in I-V characteristics of metal oxides [105]. However, during that time it had received limited attention until the advent of nanoscale realisation of devices that were based on resistive switching [106].

Valence change memory (VCM) involves anion migration based on a redox process, specifically the Formation and rupture of the conductive filament is due to a redox reaction in the oxide layer upon application of a voltage [107]. With transition metal oxides (TMO) oxygen ions have increased mobility than metal ions and it is the motion

of the defects which creates a local valence change of the cations which in turns leads to resistance switching. Because of this oxide-based VCM are also known as oxide-resistive random-access memory (ox-RRAM) [106].

Because there are many different types of defects in dielectrics and that they have the ability to change the electrical properties in response to their motion, resistive switching can be observed in many oxides, these include large bandgap dielectrics such as SiO_2, many TMOs such as, WO_3, TiO_2, HfO_2, $Ta2O_5$ and ZnO_2, and perovskites such as $SrTiO_3$ and $SrZnO_3$. However, it is important to note that not all of these are suitable for memory applications, only those that exhibit good switching performance [106].

In specific reference to VCM and device functionality, a pristine device will exhibit high resistance and in order to be activated it needs to be initially electroformed, after this cycling can take place using positive and negative polarities of the electrode [106].

Memory with an electrochemical metallisation (ECM) has a solid-state electrolyte which contains mobile metal ions, where an external electric field allows these ions to make a conductive bridge between the electrodes [107]. Specifically, one of the electrodes is the source of the mobile metal ions because it is made using an electrochemically active metal, such materials include Ni, Ag and Cu. The other electrode in this type of memory is made from electrochemically inert metals including Au, Pt and W [107].

A potential mechanism for the resistance switching was found in a study of NiO where it was thought that it was due to nickel metallic filament formation and rupture in a NiO thin film between two electrodes [105]. However, in 1967 Simmons and Verderber [108]

conducted a study to see if resistive switching could be used for memory applications and found fast switching of resistance for an Al/SiO_x/Au structure was not due to filament formation and rupture, but due to an electronic effect [105]. Resistive switching emerged as a candidate for NVM because of the limitations of other types of memory [109]. Resistive-based NVM devices have two distinct states which are either resistance or conductance. In reference to resistive-based NVM devices, there are numerous types categorised according to the specific physics of the resistive switching, examples include filamentary-based, charge transfer-based, and embedded MIM structures [60] [62] [110]. In reference to materials, until now there have been numerous materials that have resistive characteristics which include NiO, TiO and ZnO [109].

3.8.2 Structure of MIM devices

The MIM, or metal-insulator-metal stack structure, is considered one of the simplest structures. The MIM structure comprises of a capacitor and insulator which is the dielectric layer (Figure 3.3 (a)). More recently, the viability of the MIM structure has been considered as a two-dimensional novel, high speed and cost efficient NVM device [62] [110] [111]. The structure is achieved by doping the insulator with charge traps resulting in resistive switching as well as the memory characteristics of MIM. Therefore, although MIM structure is similar to the capacitor, with the MIM structure charges traps are doped within the insulating material placed between the metal electrodes (see Figure 3.3 (b)).

ReRAM cells have a capacitor-like MIM structure and because of the simplicity of the structure it is possible to have a cross bar memory architecture which provide the greatest possible density together with the simplest interconnection configuration [109].

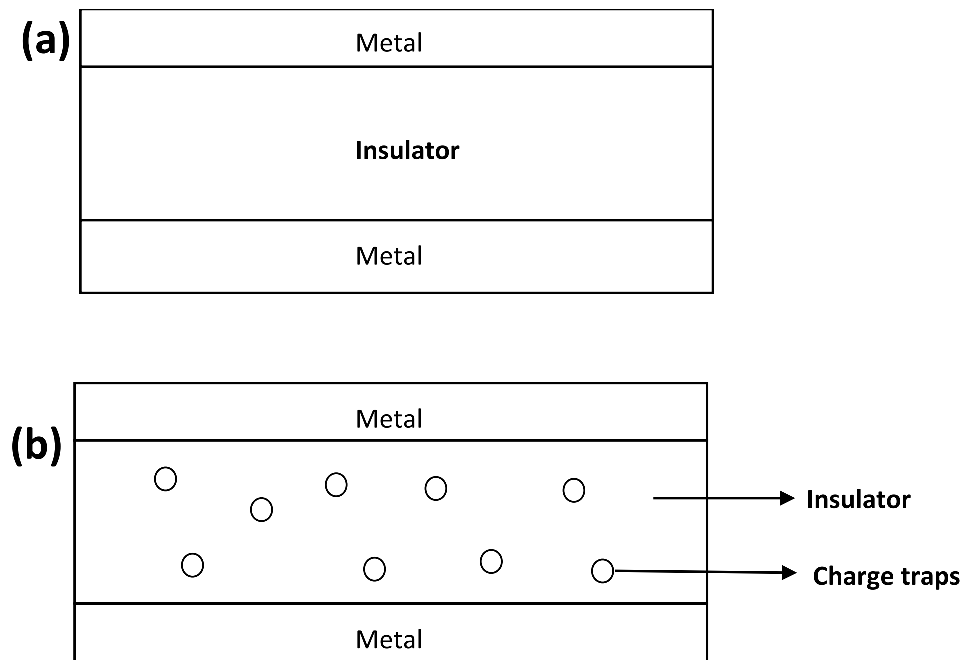


Figure 3.3 MIM device structure (a) absence of embedded charge traps, (b) with embedded charge traps.

3.8.3 MIM Current-voltage characteristic (resistive qualities)

NVMs that are electrically addressed have two distinct and stable electrical states and can carry out the WRITE, ERASE and READ processes allowing a user to WRITE the state process and then carry out the ERASE process for the other state. Additionally, the user can know the state of the device through performing the READ process [112] [58]. The present study is concerned with the embedded metal-insulator-metal (MIM).

MIM memories are resistive-type whereby the ON and OFF states are determined by two different resistance values. These two states are indicated I-V characteristics which shows the memory behaviour of MIM devices. The I-V characteristics of MIM memory devices

are illustrated in Figure 3.4. If the device is OFF (stage 1 Figure 3.4) and a sweeping bias is applied at a specific voltage (+V) (Figure 3.4 stage 1) there is a significant increase in the device current, changing it to the ON state (stage 2, Figure 3.4), therefore, the voltage is referred to as the 'writing voltage'. The device remains in the ON state, which occurs at 1.2 V, as indicated by stages 3,4,5 and 6 in Figure 3.4.

Where bias is applied in the opposite direction the current will quickly return to the original values and therefore, return to the OFF state, at this state the voltage, -0.8 V, is referred to as the erase voltage (stage 7 Figure 3.4). The MIM device can show either ON or OFF states for any voltage that is between the write and erase voltage, and therefore, any voltage that is exhibited within this range can be utilised as a read voltage of between –V and +V. (Figure 3.4).

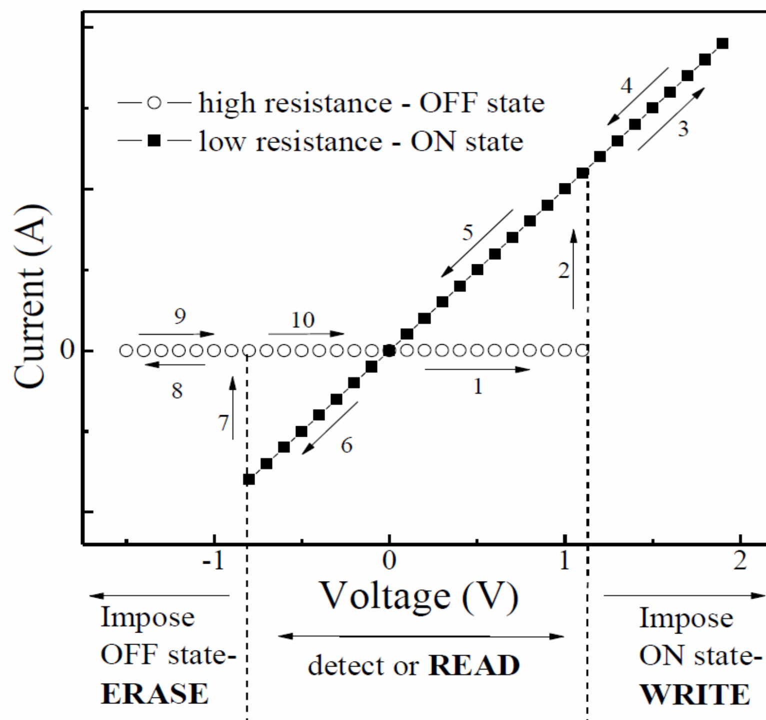


Figure 3.4 I-V characteristics of MIM memory showing RS behaviour [58].

Importantly for the present study, different organic MIM structures have shown resistive switching where different types of organic insulators have been doped with different charge traps. Such organic structures may include Au blended with PS [5] , ZnO blended with PMMA [75], and PCBM blended with PMMA [113]. In this work, we study NiO blended with PVAc, $BaTiO_3$ blended with PVAc and $CH_3NH_3PbBr_3$ blended with PVAc to investigate memory mechanism; whether it is charge trapping, filamental, dipole-based (ferroelectric) or any other mechanism.

3.8.3.1 Charge transfer based MIM memories

Memory devices that are charge transfer-based include a combination of two different materials, namely; an electron donor and an acceptor. Upon application of the bias the charge transfers from the donor to the acceptor, this results in a change in the resistivity of the acceptor. This type of MIM memory has more recently been popular with the use of organic electronics applications [114] [115]. Paul (2007) [4] demonstrates this by using C_{60} (fullerene) as an active material with 8-hydroxquinoline (8HQ) in an electronic polymer memory device, whereby upon application of a voltage, charge goes from the 8HQ as the electron donor to the C_{60} as the electron acceptor [116]. Similarly, tetracyanoethylene (TCNE) is used as the electron acceptor and 8HQ as the electron donor, also in an electronic polymer device [117] and in investigating the role played by the complex of molecules of donors and acceptors, TTF was the donor and TCNE the acceptor [2]. Another study an electric-field-induced memory using organic materials was achieved in an organic thin film which contained polystyrene as the polymer, PCBM

as the electron acceptor and TTF as the electron donor, in this case memory effect mechanism is the result of an electrically induced charge transfer [118].

3.8.3.2 Filamentary-based MIM memories

Resistive switching can be divided according to the mode of conduction in LRS which is either the filament type or the interface type [109]. Filamentary based MIM memory devices, also referred to as resistive switching RAM (ReRAM), have resistive switching that takes place between the two resistance states because the metal filament forms and then dissolves [119]. ReRAM structure in MIM devices comprises of an oxide situated between two metals and when a bias is applied a conducting filament formed and then ruptures within the oxide material. Theoretically, ReRAM (resistance switching random access memory) memory cells have the smallest area [109].

3.8.3.3 Bipolar vs unipolar resistive switching

A characteristic of ReRAM is that it has two resistance states which are high and low (HRS and LRS respectively), and by applying an electric stimulus switching can take place between these two states [109]. The first state, OFF, is high resistance with low conductance, and the ON state is low resistance and high conductance [120]. The operation which switches between the two states is known as the SET process and RESET process, the resistive state whether HRS or LRS is retained when the electric stress ceases, which is evidence of the non-volatile nature of the ReRAM device [109]. Based on this, there are two types of resistive switching, namely; bipolar and unipolar, bipolar occurs when the voltages for SET and RESET take place at opposite polarities and the unipolar

occurs with the same polarity. The SET process takes place where a positive bias being applied to the electrode. The RESET process occurs in the bipolar resistive switching mode where a negative bias is applied to the active electrode which reverses the process, results in electrochemical dissolution of the filament which returns the memory to the OFF state which is high resistance [110] [111] (figure 3.5(b)). Where the RESET process takes place for the unipolar resistive switching mode there is an occurrence of the thermochemical mechanism, whereby a fuse-antifuse process takes place when the current limit is removed resulting in a higher temperature because of high currents and rupturing of the filament [110] [111]. These processes are illustrated in Figure 3.5 (a). Unipolar resistive switching is more prevalent in devices where the filament is formed as a result of oxygen vacancies in the metal-oxides electrolytes. Bipolar resistive switching is more prevalent in ECM structures whereby the metal behaves as the active electrode.

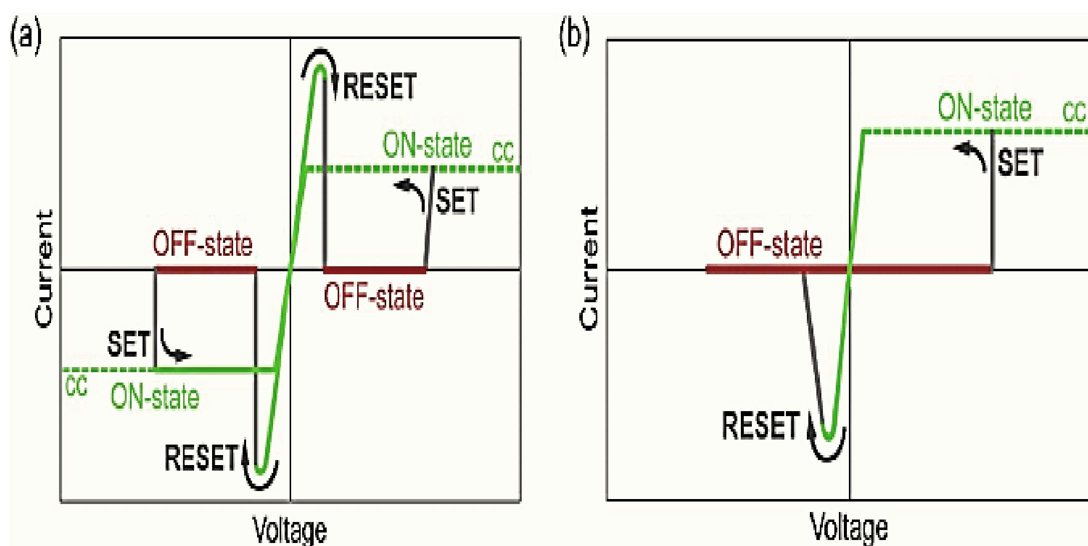


Figure 3.5 schematic of (a) Unipolar and (b) bipolar switching in resistive switching memories [86].

3.9 Principles of switching mechanisms and electrical bistability

The principles and mechanisms associated with the electric bistability have been established by Paul (2007) [4] . This study seeks to further understand and verify these principles of electrical bistability and switching mechanisms through testing new materials and material compositions. Resistive switching and electrical bistability has been observed in a wide range of nanoparticle – polymer systems and there have been a number of mechanisms proposed as explanations for the internal switching.

The internal switching mechanisms of organic memory devices has been addressed by Bozano et al. (2004) [121]. They claimed that resistive switching in organic semiconductor memory devices that contain granular metal particles demonstrated a charged storage mechanism which conformed with Simmons and Verderber [108].

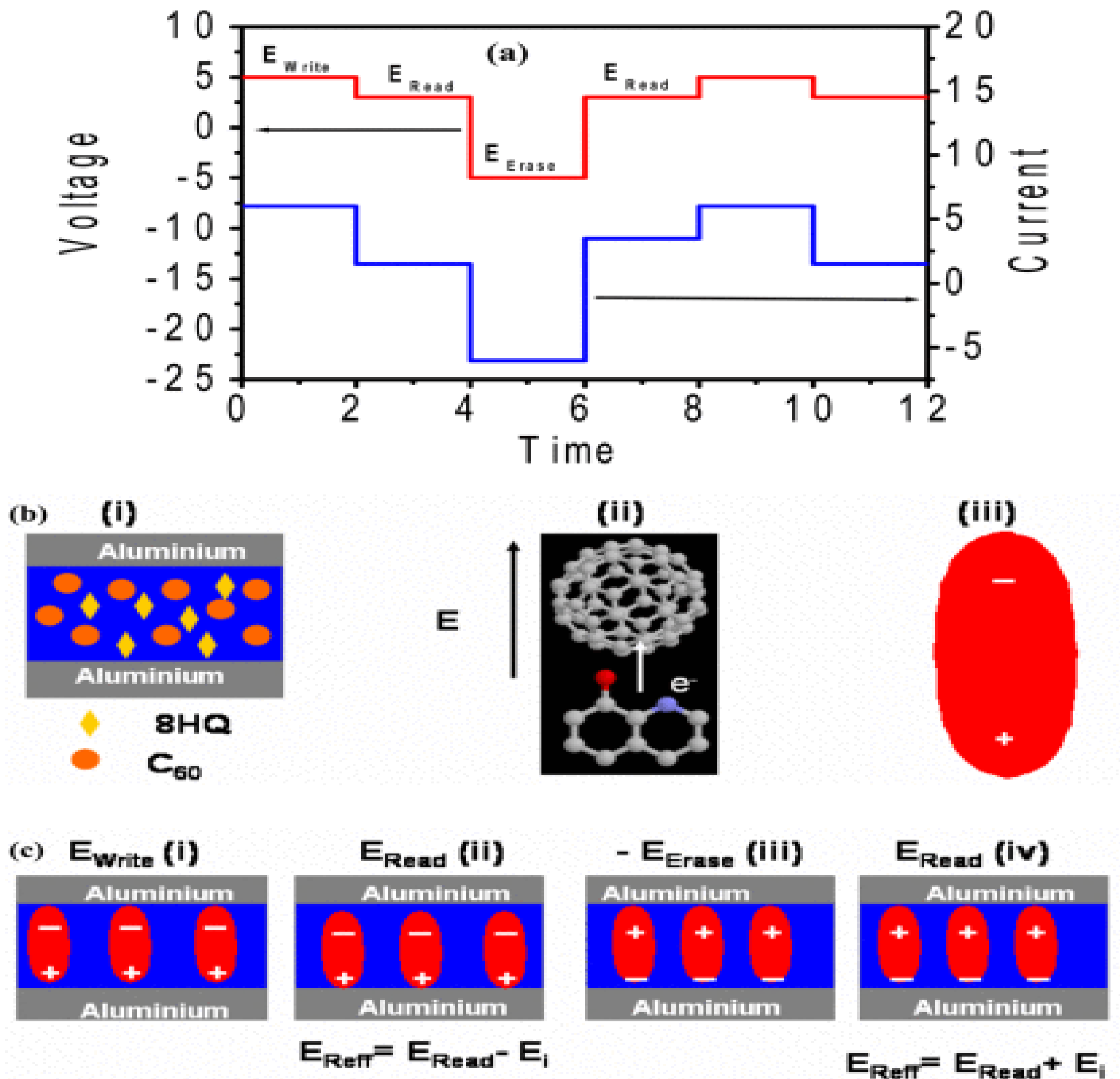


Figure 3.6 Principles of switching mechanisms in 2TNVM as proposed by Paul (2007) [4].

Towards achieving greater and more sustainable hysteresis, a reflection of capacity of a memory device, Paul (2007) presents the internal mechanism which is based on an internal electric field being created which provides bistability in the electrical conductivity. Specifically, the non-volatile memory behaviour is a result of this internal electric field upon application of an electric current across the device. Paul (2007) [4] presents this mechanism and says that the difference between the on and off states is a

result of this internal electrical field. Specifically, the C_{60} molecule accepts the electrons and the surrounding polymer acts as an insulator to retain this charge, this then leads to a charge separation (Figure 3.6 (b)) which create a surplus internal electric field. When the device is exposed to a write voltage dipole are formed in the material which creates an internal electric field and when the read voltage is applied it results in the voltage across the device being less than the external applied voltage thus reducing conductivity. Therefore, a lower current is passing through the device and the application of the *erase* current changes the orientation of the internal field leading to a higher read pulse voltage increasing conductivity (Paul, 2007) [4].

3.10 Summary

This chapter provided an overview of two-terminal non-volatile memory devices. This memory device structure, specifically the MIM structure, was used in the present research to investigate memory characteristics of the tested materials and therefore, it was necessary to present the MIM structure and its current voltage characteristics and resistive qualities as relevant to memory characteristics. Furthermore, there have been a number of different explanations proposed for the mechanisms that cause the resistive states which have been addressed in this chapter. These different mechanisms also correspond to different material properties which in turn correspond to the different materials that are tested in the present study. Particular attention is paid to organic NVM and the use of polymers.

Chapter 4 Fabrication, Characterisation and Experiment Techniques of Memory Devices

4.1 Introduction

The fabrication of the devices and their characterisation will be described in this chapter. Furthermore, the conditions of the experimental electrical measurements are given. The characterisation techniques include FTIR, UV-VIS, Ellipsometry, SEM and electrical measurements (I-V, C-V, C-t).

In this work, memory devices have either a single active layer where the material is a blend composition or multiple layers in the layered composition. These layers are inserted between a two-metal cross-point arrays of electrodes arranged in a bottom and top order [122] [123] [82] and are as shown in figure 4.1. This chapter is concerned with the deposition techniques for these layers, specifically spin coating is used to achieve the single layer that is comprised of the blend composition, and vacuum evaporation for the layered structure.

Figure 4.1 Illustration of (a) MIM devices (b) MIS structure (Metal-insulator-blend-semiconductor.

4.2 Vacuum Evaporation

Thermal evaporation is a simple Physical Vapour Deposition (PVD) technique that was used to deposit metallic thin films onto the substrate. The technique is suitable for a variety of materials which include metals and metallic oxides for electrodes and certain organic materials such as small-molecule organics [124]. The evaporator used in this research is shown in Figure 4.2. Principally, material is heated in a vacuum chamber until the point that the surface atoms have enough energy to transfer from a heated source to a substrate located a distance away to grow a film [125] [126]. Thermal evaporation is achieved by evaporation electrically of the source material under a high vacuum (with a long mean free path) using a heating element, usually tungsten wire, where the vapour is allowed to condense on the surface of the substrate. Evaporation is also carried out at low pressures about 6×10^{-6} to 10^{-8} Torr. It should be noted that a clean substrate is essential to achieve good film adhesion.

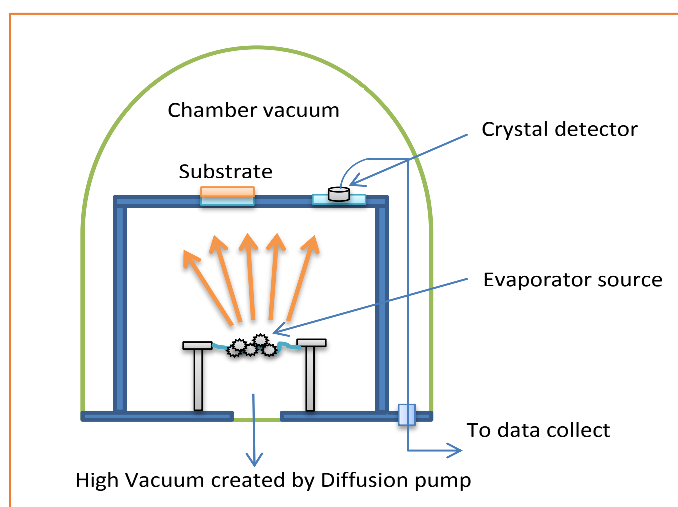


Figure 4.2 schematic diagram of vacuum evaporation.

Important factors to be observed in thermal evaporation are: pressure and temperature, source, substrate, and placement of the heater. Vacuum evaporation is not suitable for materials with very high melting points (resulting in vaporisation problems), and the possibility of cross-contamination from the heating filament or the crucible in which the source material is vaporised is the major drawback of this technique. In this work, Edwards Auto 306 thermal evaporation was used to deposit aluminium contacts.

In this research this technique was used to deposit the electrodes and the active material. Furthermore, this technique was used to deposit the active material for the layered structure. For the thickness of the bottom electrode in this research which was 100nm, and 300nm for the top electrode, an evaporation period of more than five minutes was required. This was required to ensure lower surface roughness and to ensure the quality of the interface between the active material and the electrode. Consideration of evaporation rates was important in this study, these are measured in angstroms per second [127]. The two active materials that were evaporated using this technique were NiO and $BaTiO_3$. Two thicknesses of NiO, 12nm and 44nm, and one thickness of $BaTiO_3$ were deposited using an evaporation rate of between 40 and 45 $A \cdot s^{-1}$. During this fabrication technique it was difficult to deposit the $BaTiO^3$, thus only one thickness layer was deposited. The specific deposition parameters are shown in Table 4-1.

Table 4-1 Deposition parameter of materials

Material	Density (g/cm^3)		Layer thickness (nm)	Temperature (melting point)	Evaporation rate ($A \cdot s^{-1}$)
NiO	6.67		12 nm and 44 nm	1955C°	60 – 70
$BaTiO_3$	6.08		10 nm	1625C°	40 - 60

4.3 Spin Coating

Spin coating is a simple and fast method for depositing uniform thin films from solution [128] [129]. Figure 4.3 below illustrates this procedure. This technique is used extensively for deposition of photo resists in industry, and more recently, active layers in organic light emitting diodes, the technique can also be employed to create thin films below 10 nm thickness.

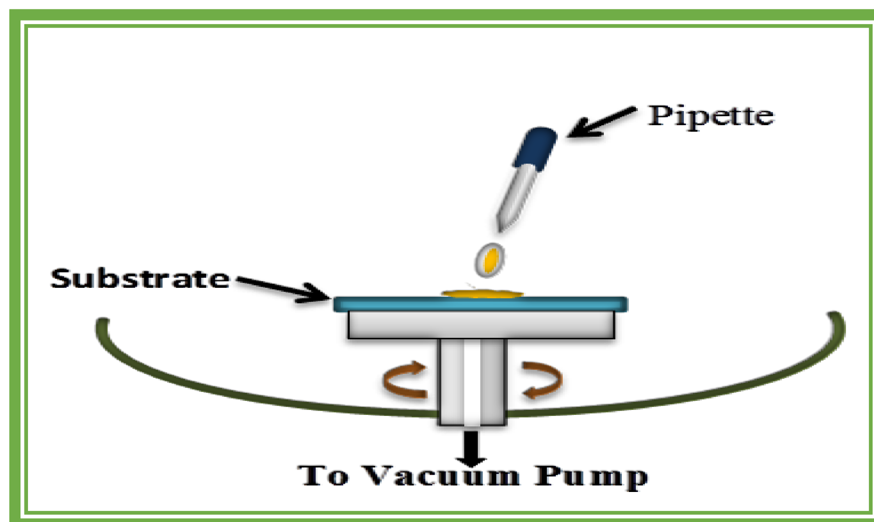


Figure 4.3 Spin coating diagram.

A few drops of the material are applied to the substrate, and then spun at high speed by centrifugal force to spread the material across the substrate. The substrate can spin at several thousand revolutions per minute. The spin speed increases to the required speed, remains at the speed for a required time and then slows to stationary, after which the substrate can be removed from the coater [130]. Often the substrate is positioned onto a rotating chuck using a vacuum pump and while the sample spins a neutral gas or air is pumped into the chamber to ensure it stays dry. Thickness and uniformity of film is mainly determined by the following factors; rotation speed, concentration of the solution used the rotation total time and the volatility of solvent used.

There are a number of variables in the spin coating process which can make it difficult, these include viscosity, evaporation rate, N_2 flow rate and spin speed, however, there is available a formula that shows the relationship between the thickness of the film (d), the angular velocity (**ω**) and the empirical constants of the material which include the solvent, the solute and the substrate, denoted as k and α [131]. This formula is as follows [131]:

$$d = k\,\omega^{\alpha} \qquad (4\text{-}1)$$

It was important in the present study, that spin coating is a suitable method for depositing thin films of organic material. It is difficult to model the spin coating process because there are numerous factors to be considered, these include the rate of evaporation, the viscosity of the solution, air flow rate and spin speed. Due to the number of variables, in order to optimise the spin process in this research a range of samples were spin coated at different speeds in order to achieve the required thickness. Specifically, speeds were

tested between 1000 and 10000 rpm and 4000 rpm was found to be optimal for material thickness, any more than 4000 rpm and the material deposition was found to be too thin.

Spin coating is a suitable method depositing organic materials. It is important to note that the viscosity of the material will affect the thickness of the layer at the same spin speed and that it is not just the viscosity of the polymer that has to be considered but also the material that is added to the polymer that can also affect viscosity [131]. Furthermore, one of the techniques whereby the material is dropped onto the spinning substrate, known as dynamic spin coating, is known for causing waste, and there is a significant amount of polymer and nanoparticle material that is lost in this process, therefore, static deposition was used in this research.

4.4 Characterisation Techniques

4.4.1 Ellipsometry

Ellipsometry as an optical technique is used to identify the thickness, surfaces and dielectric properties of thin films, and is also referred to as reflection polarimetry. As a non-contact optical method, ellipsometry is also able to determine a materials' refractive index [132]. The properties of thin films that are measured by ellipsometry include surface roughness, anisotropy, crystal nature, interfacial regions, uniformity, and composition, doping concentration, electrical conductivity, refractive index and extinction coefficient analysis (n and k respectively). Linearly polarised light is changed by compensator plate to elliptically polarised light (quarter wave). Ellipsometer is used to measures changes in optical polarisation of light when the light is reflected from a

sample and samples of almost any size and shape can be examined. If the sample has some changes in the properties, for instance the thin film thickness deposited on a substrate may not be a constant across the film, the reflection properties of the sample will also change. Therefore, using reflection properties to measure these changes will help to forecast the real changes in the thickness of the film.

Moreover, spectroscopic ellipsometry, as an optical technique, is contactless and non-destructive and due to the fact that the incident radiation can be focused, it is possible to image small sample sizes and map desired characteristics over a larger surface.

This technique is applied in numerous fields, including semiconductor physics, microelectronics and biology, and its use can range from basic research to more complex industrial applications. For thin film metrology ellipsometry is unequalled due to its sensitivity in measurement.

This technique can be used for analysing metal and dielectric films in a quick and non-destructive way [133] [134]. Furthermore, this technique is accurate because it is sensitive to surface layers and the thickness of thin layers compared to spectrophotometric methods [133]. This technique is accurate for angles of incidence between 30˚ and 70˚ for films [133].

The film thicknesses and refractive index in this work were measured by an AutoEL-III ellipsometer equipped with a 5416 A helium-neon (He-Ne, $\lambda = 632.8$ nm) laser at an incident angle of 70°. A schematic of this process is illustrated in Figure 4.4. However, it was important using this technique to use silicon as a reflective substrate.

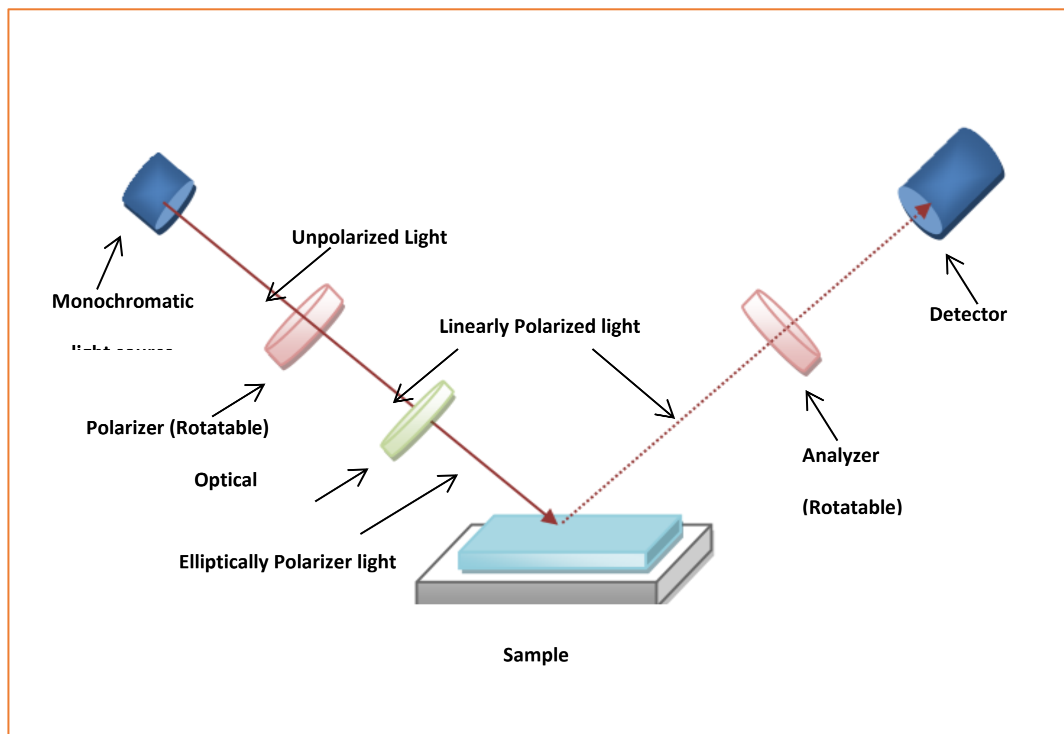


Figure 4.4 Diagram of spectroscopic ellipsometry measurement.

4.4.2 FTIR Spectroscopy

Fourier Transform Infrared (FITR) spectroscopy is a technique used to study the interaction of matter with infrared electromagnetic radiation. The infrared light absorbed by the organic compound is converted into energy of molecular vibration. The infrared absorption bands identify the various groups of the molecule function. FTIR was used here to characterise the presence of chemical groups in the tested materials.

FTIR spectroscopy is a preferred method used to gain an infrared spectrum of absorption, compared to photoconductivity, emission or Raman scattering and it is used to structurally characterise organic and inorganic molecules on surfaces of solids, liquids,

and gases [135]. In addition, it provides qualitative and quantitative information about the molecule.

Fourier transform spectrometer IR has three main parts including the source of radiation, interferometer and detector. A schematic diagram is shown in figure 4.5 below.

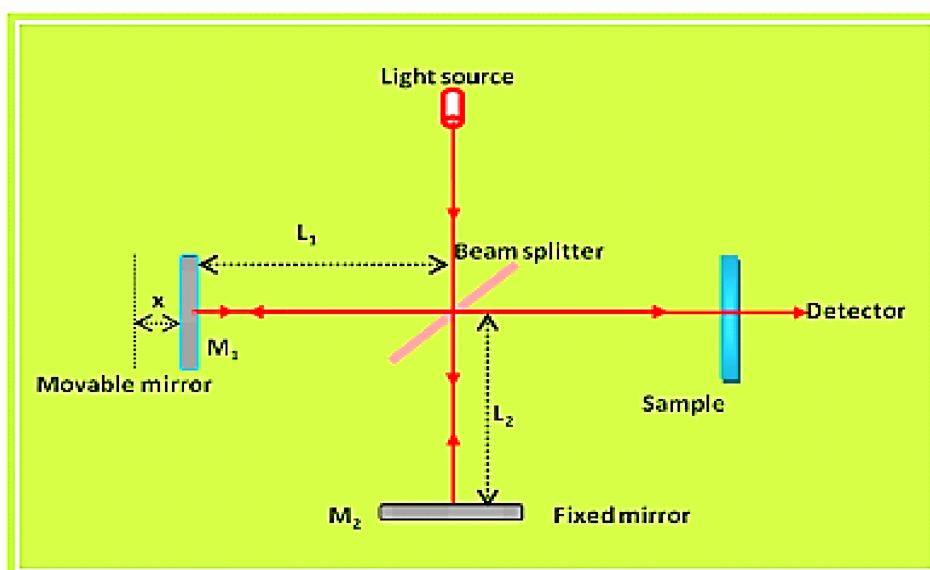


Figure 4.5 Illustration of the Michelson Interferometer, an important component of FTIR [100].

In this research FTIR spectroscopy was used to measure the integrity of the active material when blended with the polymer.

4.4.3 Ultraviolet–Visible Spectroscopy

Ultraviolet–visible spectrophotometry (UV-Vis) is reflectance or absorption spectroscopy in the ultraviolet-visible spectral region. This technique is often conducted using solutions, however, gases and solids may also be used. Although molecules to

undergo vibrational transitions when interacted with infrared light, for the shorter wavelength, whereby there is higher energy radiation in the UV (200-400 nm) and visible radiation in the (400-700 nm) range of the electromagnetic spectrum, this can cause numerous organic molecules to go through electronic transitions. Thus, when a molecule absorbs energy from UV or visible light, a single electron will jump from a lower to a higher energy molecular orbital.

It is also possible to configure the UV-Vis spectrophotometer to measure reflectance. In this way, the intensity of light (I) which is reflected from a sample is measured by the spectrophotometer, and a comparison is made to the intensity of light (I_o) that is reflected from a reference material. The ratio:

$$T = \frac{I}{I_o} \quad (4\text{-}2)$$

It is referred to as the reflectance and is normally expressed as a percentage (%R).
In this research UV-Vis is used to measure the integrity of the material after it has been mixed. Moreover, this technique was also employed to calculate the band gap of the material.

4.4.4 X-Ray Diffraction (XRD)

X-Ray diffraction (XRD) is a non-destructive analytical technique used to determine if the tested materials have a crystal structure or are amorphous [19]. In reference to the crystal structure the technique is used for the identification of phase [136] crystal

structure, crystal orientation, and structural parameters which include crystallinity, crystal defects, grain size and strain, or if the material is amorphous.

The principle working mechanism of XRD involves the constructive interference of monochromatic light. A cathode ray tube is used to create the X-rays and filtered out to produce monochromatic X-rays which are then directed at the sample material [136]. Where the X-rays strike the sample, it produces constructive interference or diffracted rays which are then detected and processed to reveal the material structure [136]. The principle is based on Bragg's law of diffraction, and when the diffracted rays meet the conditions of Bragg's law (equation 4.3) it produces a constructive interference, the law considers the wavelength of the radiation, lattice spacing and diffraction angle in the sample [136], where n is a positive integer and λ is the wavelength of the incident wave:

$$n\lambda = 2d\ sin\theta \qquad (4\text{-}3)$$

Each of the three materials was analysed when combined with the polymer in order to determine if the structure had changed from the pure form of the material. This was necessary to determine if there was a change in the structure of the material when combined with a polymer. For NiO the XRD showed that there was a cubic structure and for $BaTiO_3$ showed that cubic phase of the material changed to the tetragonal phase. For $MApbBr_3$ the XRD showed that the cubic structure mostly remained the same, apart from some lower crystallinity due to the presence of impurities.

4.4.5 Scanning electron microscope (SEM)

Scanning Electron Microscopy can be used to determine both the internal structure and surface structure. The way SEM works is to scan a beam of electrons across the surface of a material and through measuring backscattered electrons and electrons from ionisation a raster image is produced. In this technique it is possible to obtain a resolution of the wavelength of the electron, and through using the duality of particles it is possible to achieve a resolution detailed to the level of the wavelength of the electron through using wave particle duality whereby much smaller wavelengths are achieved providing improved resolution [130].

Specifically, an electron beam produces a signal at the surface of the material which can then be used to generate an image using amplification. The electron beam is then focussed using lenses, this beam is targeted at the specimen whereby electron emission takes place. This emission contains secondary electrons that have lower energy and backscattered electrons that have higher energy [137].

In this study SEM was used to gain high quality images of the film and material before and after annealing the material. The results showed an increase in particle size after annealing.

4.5 Electrical Measurements

The electrical measurements using current voltage and capacitance voltage measurements were carried out to determine the electrical behaviour of the materials used in the device's

fabrication, this included bi-stability in electrical conductivity. Electrical measurements were conducted to obtain the desired properties of the device behaviour.

For the I-V measurements in this research the HP 4140B picoammeter was used and the HP 4192A LCR bridge was used for capacitance (CV) measurements. The equipment was programmed using the Agilent VEE Pro software. Measurements were conducted inside an electromagnetic radiation shielding metal box probe station.

4.5.1 Current Voltage (I-V) Measurements

Current voltage measurements are conducted in this research in order to obtain useful parameters which includes the bistability characteristics of the tested memory devices. The Hewlett Packard HP 4140B picoammeter and DC voltage source was used to take the I-V measurements, this device is able to measure current from ± 1pA to 10mA and provide a DC voltage between ± 100V. The picoammeter was controlled using a PC. A two-probe system was used to take the measurements connected the picoammeter and the probes were positioned manually (see Figure 4.6). The readings are shown in pA and mA, but the data is saved as amperes and saved in Excel and then presented in a graph form. I–V measurements were also conducted for both the MIM and MIS structures in order to determine leakage current.

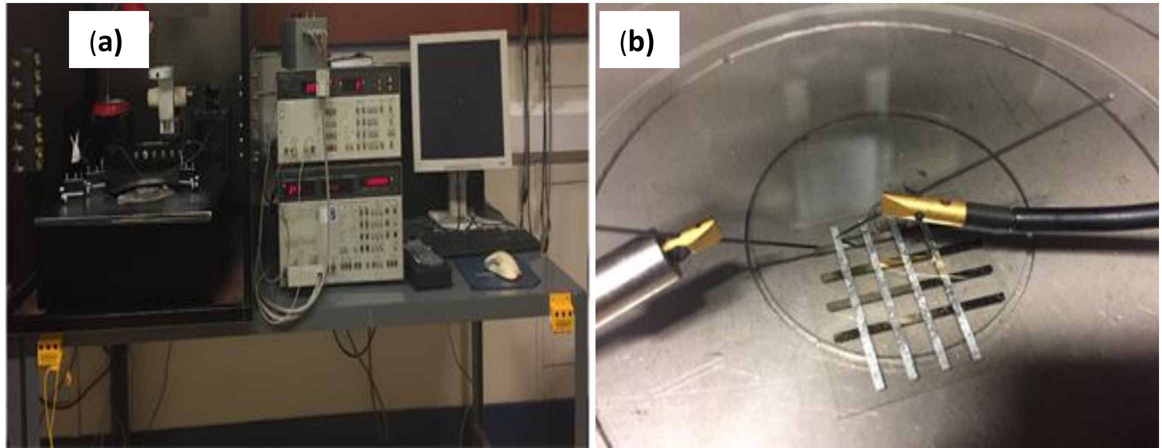


Figure 4.6 (a) Hewlett Packard HP 4140B picoammeter to test I-V (b) A two-probe system on Sample in EMTERC Lap.

4.5.2 Capacitance – voltage (C-V) measurements

In order to test capacitance which shows both memory programming and charge retention and durability the dielectric layer of the MIS structure is measured using C-V measurements. The importance of these dielectric measurements is to determine dielectric thickness, dielectric constant and flatband voltage. The following formula is used:

$$C_{acc} = \frac{e_{ox}}{t_{ox}} A \qquad (4\text{-}3)$$

Capacitance is represented by C_{acc} at the accumulation regime, the gate dielectric thickness is represented by t_{ox}, the oxide permittivity is represented by e_{ox} and A represents the gate area. Capacitance values were shown by the C-V measurements. The MIS structure was also used to measure data retention over time as a quality of memory performance. Finally, C-V measurements were also conducted for memory device programmability of $MApbBr_3$, this was achieved through WRER voltages.

4.6 Summary

In summary, this chapter has covered the fabrication techniques that were used to achieve the active material layer for the experimentation of this study, for both blend and layered material compositions. Additionally, the characterisation methods that were used to determine material integrity were also addressed. Specifically, the characteristics were used to test material properties, material integrity, consistency across films and internal and surface structure. The techniques that were used for electrical measurements were explained including current – voltage and capacitance – voltage measurements.

Chapter 5 Materials and Device Structure

5.1 Introduction

This chapter presents the tested materials that are used in the fabrication of the memory devices and their physical characterisation. Moreover, the fabrication techniques which include the use of blend and layered material compositions and the MIM and MIS device structures are also presented.

5.2 Nanoparticles

The use of nanoparticles, between 1 and 10 nm, as semiconductors has received much attention for use in non-volatile memory devices. The first to investigate the incorporation of nanoparticles in memory devices was Paul et al (2003) [138] and the first to incorporate them into a polymer was Ouyang et al. (2004) [139]. The reason that nanoparticles are particularly suitable as semiconductors lies in their structure. This has been due to low fabrication costs, but importantly their qualities which include high data storage density and low power consumption [140]. Their structure, which lies between a molecule and a bulk material, offers a greater flexibility to store information. As a semiconductor, the gap band between the valence band and conducting band is greater for the nanoparticle structure than that of the bulk material and will result in discrete energy states; which can then be exploited to store electronic charge, or in other words information.

Devices that use a polymer matrix with metal nanoparticles store data by being in either a low or high conductivity state which can be set through the application of read and erase voltages across the device [5]. The electrical properties of a non-volatile organic polymer significantly change when embedded with metallic nanoparticles, this is because of the charge that is stored within the nanoparticles [81]. The bistable effect is because of the presence of nanoparticles in the organic matrix [127]. Electrical bistability using nanoparticles within a polymer insulating material has been tested by [78] for a polymer memory device. Specifically, these researchers tested gold nanoparticles and found that the tested memory device exhibited remarkable electrical bistability. Polymer and nanoparticle composition in bistable devices come under the categorisation of Organic Bistable Devices (OBD) and offer devices that are non-volatile and have two states; ON and OFF [141].

The following table presents a number of studies that have tested nanoparticle / polymer memory devices towards revealing gaps and limitations in the research.

Table 5-1: Summary of previous studies in active nanoparticle / polymer memory.

Authors	**Nanoparticle**	**Polymer**	**Device structure**	**Tests**	**Results**	**Limitations**
Prakash et al. (2006) [78]	Gold	Poly3-hexylthiophene	Layered composition, two-terminal Different concentrations	Current-voltage (I-V) WRE Retention time	Excellent stability in both conductivity states	No layered composition tested

Tseng et al. (2005) [81]	Gold	Polyaniline nanofibers	Composite (blend), two-terminal	Current-voltage (I-V), Prolonged retention, Write, Read and Erase, electrical pulse measurements	Prolonged retention for several days, Electrical bistability achieved	Only one concentration tested No layered composition tested
Jung et al. (2006) [111]	Cuprous oxide	Polyimide	Two terminal, layered Al/PI/nanocrystalline Cu2O /PI/AlCu2O/PI/ Al	Current-voltage (I-V).	Non-volatile electrical bistability	Blend not tested
Son et al. (2009) [75]	Zinc Oxide (ZnO)	Polymethyl methacrylate (PMMA)	Blend composition nanoparticles embedded in an insulating PMMA polymer layer/ITO/PET structures	Current-voltage (I-V) Optimised nanoparticle	nonvolatile electrical bistability, flat-band voltage indicates trapping, storing, emission of charges ZnO nanoparticles	No layered composition tested
Prime et al. (2009) [5]	Gold	Poly (4-vinylphenol) (PVP)	Blend composition, two-terminal (MIS)	Capacitance voltage (C-V)	Capacitance difference due to particle charging – however, conductivity could be due to MIS structure	
Salaoru and Paul (2009) [72]	$BaTiO_3$ (Barium Titanate) (Annealed)	Polystyrene (PS) and polyvinyl acetate (PVAc)	Blend composition, MPM (MIM)	Current voltage (I- V) Capacitance voltage (C-V)	Symmetrical I – V characteristics	Different concentrations of $BaTiO_3$ not tested

Lin et al. (2011) [73]	Gold and ZnO	Poly(vinylpyrrolidone)				
Mukherjee (2009) [143]	Silver	Polymethyl methacrylate (PMMA)	Layered composition			
Yun et al. (2015) [140]	Copper zinc tin sulphide (Cu2ZnSnS4)	Polymethyl methacrylate (PMMA)	Blend composition	Current voltage (I- V) WRER	Current hysteresis behaviour	Only one concentration
Hong et al. 2013 [144]	polypyrrole (PPy) nanoparticles	Poly (vinyl alcohol) (PVA)	Blend composition Two terminal memory device One aluminium terminal One Indium tin oxide terminal	Current voltage (I- V) Three different thicknesses 20nm, 60nm, 100nm WRER	100nm no hysteresis 60nm no bistable memory behaviour 20nm bistability More than 60nm lack of charge trapping due to leakage from rough surface	
Kim et al. (2010) [145]	Silver	Polymethyl methacrylate (PMMA)	Blend composition	Current voltage (I- V) WRER	Electrical bistability exhibited	One concentration
Onlaor et al. (2014) [74]	Zinc Oxide (ZnO)	Polyvinylpyrrolidone (PVP)	Blend composition – different concentrations One Al and One In oxide terminal	Current voltage (I- V) Current retention	Switching behaviour depended on concentrations	
Mabrook, M.F et al. (2009) [146]	Au	polymethylmethacrylate (PMMA)	Layered composition	Capacitance voltage (C-V)		

5.3 Ferroelectric Properties and Perovskite Structures

Ferroelectric materials are increasingly being used in a number of different applications which include non-volatile memories with a low switching voltage [147]. A quality of ferroelectric materials that makes them suitable for memory applications is that they exhibit non-volatile properties, moreover, they can work at low voltages [148].

Pyroelectric materials that have a permanent electric dipole can have this dipole reoriented by applying an electric field, the resulting crystals are referred to as ferroelectric. Where there is a spontaneous polarisation which can be reversed by an electric field then the crystal is ferroelectric. In fact, it is the low-dimensional structure of the crystals that give ferroelectric materials these polarising properties [149]. It is this switching property whereby polarisation is reversed. Switched ferroelectric materials are used in memory devices. Importantly, the two distinct polarisation states of a ferroelectric material can be maintained where there is no electric field [148]. Specifically, ferroelectricity has been described as a mechanism whereby the direction of the electric polarisation is a result of the dynamic motion of the elements that exist between the molecules. It is important to note here that organic ferroelectric materials have weak polarisation properties which means that a lower electric field is required to reverse the polarity.

Ferroelectricity exhibits a P-V hysteresis which is the two-level logic, ON and OFF states, which forms the basis of the memory device [148]. One of the functions of memory is capacitance, which is required for retaining charge in the memory device and ferroelectric materials can be used as capacitors; as the ferroelectric materials has the capability to

retain the internal electric field in spite of the removal of external electric as in the case of non-ferroelectric capacitors [148]. Thus, such materials will lead to a non-volatile memory device. In reference to ferroelectric materials as nanoparticles, it is believed that the ferroelectricity is preserved even at several unit cells which means it is possible to scale down devices [148]. The present study investigates $BaTiO_3$ as a nanoparticle which has ferroelectric properties.

The present study is also concerned with investigating methylammonium lead bromine which is an organic - inorganic material, as opposed to barium titanate which is an inorganic ferroelectric material and has ferroelectric properties. In reference to this, ferroelectric materials that are used to fabricate non-volatile memories have included the use of organic materials Moreover, methylammonium lead bromine is lead-based and such ferroelectric materials have been popular for use in industry for many decades [149].

Some materials have ferroelectric properties due to their perovskite structure. In the present study $BaTiO_3$ and $CH_3NH_3PbBr_3$ have perovskite structures. Non-volatile memory that utilises a perovskite structure exhibits reliable memory characteristics, for example read, write and erase operations erase, data retention and durability [150].

Perovskite materials often exhibit hysteresis which in other applications is an undesirable property, however, this hysteresis is the result of a defects in the perovskite materials which can be utilised for memory applications. Specifically, resistive switching is a result of a migration of vacancy defects and conducting filaments which occur when an electric field is applied to the perovskite structure [150]. It is the internal electric field that is created by perovskite materials, that are organic, inorganic or both, that have significant

potential in the use of high performance memory devices [150], and in the present study $CH_3NH_3PbBr_3$ is a material that is an organic / inorganic hybrid and is investigated for these aforementioned memory properties.

However, perovskite materials have been known to exhibit a lack of stability in ambient conditions which prevents them from being applied to practical applications [151]. Hwang and Lee (2017) [151] passivate resistive switching memory devices that use perovskite materials through the application of metal-oxide-layers. In the present study perovskite materials are blended with a polymer to resolve the issue of instability.

5.4 Materials

There are three materials that are under investigation in combination with the polymer (PVAc) in non-volatile two-terminal memory devices (2TNVM), namely; Nickel Oxide (NiO), Barium Titanate ($BaTiO_3$) and Methylammonium lead bromine $MAPbBr_3$ ($CH_3NH_3PbBr_3$). The following sections provide an overview of these materials.

5.4.1 Polyvinyl Acetate (PVAc)

Most polymers are insulators or dielectrics due to their high current resistance. Relative to ceramics, polymers usually have much lower dielectric constants. On the other hand, their dielectric breakdown field strength can take place at high fields making them suitable for high energy density. Poly-vinyl acetate (PVAc) is an insulating polymer derived from the vinyl acetate monomer prepared from combusting of ethylene with oxygen and acetic acid using a palladium catalyst [152]. In its solid form it is a clear pellet

that is translucent and has a density of ~ 1.18g/ml [153]. It is soluble in methanol and in other alcohols and can be spin coated or drop cast. PVAc, even at high concentrations, is also water soluble which means it can be used in environmentally friendly wet coating processes [154].

PVAc is a dielectric polymer which possesses memory function (hysteresis) which leads to high local dipoles [154]. However, it is important to acknowledge that PVAc can contain ionic impurity which can affect the hysteresis [154].

The polymer chains within its structure are twisted and disordered which gives the polymer an amorphous structure which allows ions to easily diffused within its matrix [155]. PVAc has a permittivity of ~3.2 [156] and is known for being blended with varied materials such as barium titanate making it a suitable material to test for any increase in permittivity resulting from the addition of ferroelectric nanoparticles to insulating polymer layers [157] [72] as will be discussed in next chapter. In this study PVAc blended with NiO and $BaTiO_3$ and $MAPbBr_3$ nanoparticles to create electrical dipole within the polymer matrix.

5.4.2 Nickel Oxide nanoparticles (NiO)

NiO was one of the first materials to be tested in RRAM applications and that various metals, including Au, have been used as the electrodes in memories that use NiO, which often exhibits unipolar switching behaviour. Nickel oxide nanoparticles appear in black powder form and are graded as very toxic. It is versatile and is a wide band gap semiconductor. Fabrication of non-volatile memory devices using metal nanoparticles has

a number of advantages which include faster write and erase speeds, lower operating voltages and longer retention time [158]. The development of nanostructure metal oxides has received much interest due to their properties. One commonly used example is NiO which has many applications, it is used as a p-type semiconductor with a stable wide band gap ~3.5 [159].

NiO has a unipolar switching property which allows a diode to be used for read and write operations, however, it is this unipolar switching whereby the set and reset voltage polarities are the same, and consequently it is absolutely necessary to have set and reset parameters that are narrowly distributed [160]. Unfortunately, a well-known issue with NiO is poor switching uniformity which results in an unacceptable failure rate [160]. This issue has been addressed by [161] who successfully proved the use of nanostructure. The present study is concerned with resolving the same issue, however, through the use of NiO as a nanoparticle, to determine the correlation between the structure of NiO and its associated properties.

Oxide nanoparticles have unique chemical and physical properties because of their limited size and corner and edge surface sites which are of high density. Particle size influences three basic properties of a material. The first is the structural characteristics, which include the cell parameters and the lattice symmetry. Oxide materials are robust during fabrication processes and studying of high-k materials has shown it is important to control oxygen. NiO nanoparticles used in this work were obtained from Sigma-Aldrich in particle size ~<50 nm.

5.4.3 Barium Titanate ($BaTiO_3$)

Barium Titanate ($BaTiO_3$) is a ceramic oxide of barium and titanium. $BaTiO_3$ has a Perovskite structure of the form A B X_3 and A and B represent the positive ions (cations) and X is the negative ion (anion) bonded to both cations [162] [163]. The basic structure of a primitive cell is comprised of a single A cation positioned at a corner of the lattice structure and a B cation located at the centre of the lattice structure with three X anions all facing centre (see Figure 5.1).

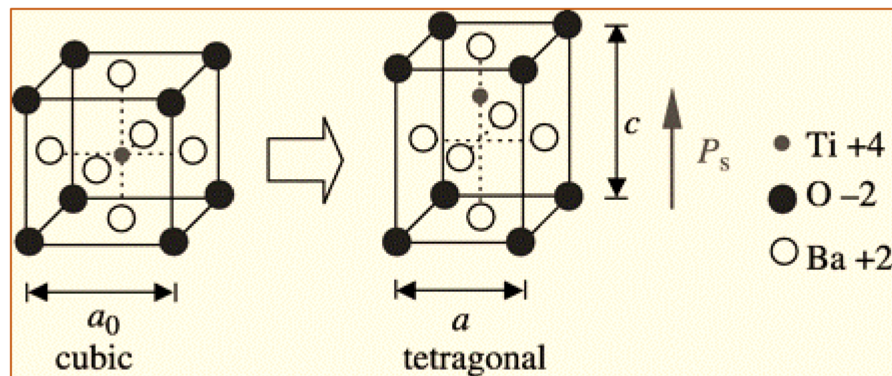


Figure 5.1: 3D Perovskite structure shown in the cubic phase and translation to tetragonal phase [164].

The remarkable switching behaviour of Barium titanate is that it has bipolar resistive switching and is non-volatile and is therefore, suitable for resistive random-access memory devices [50]. A reason that Barium titanate has been chosen for the study is because, as a ferroelectrical material, Barium titanate has electric dipoles that can be reoriented through the application of an external electric field [165]. Moreover, it has high dielectric permittivity which is important for memory [166]. However, although Barium

titanate can be deposited onto thin films using chemical deposition (CVD), it requires very high temperatures which is not suitable for many substrates [166]. Dielectrics that are polymer-based offer good processability due to their high dielectric strength which is suitable for high-energy-density capacitors, however, their storage capacity is limited [166]. Therefore, a solution has been polymer nanocomposites whereby different ferroelectric materials have been used to have an effect on the permittivity of polymers [167] [168] [169] and Barium titanate is one such material that can be used to modify the permittivity of the polymer in the memory device [131]. Barium titanate has high permittivity and as a nanoparticle can be combined with polymers that have high dielectric strength to achieve a high performing dielectric material [166]. Therefore, using a polymer nanocomposite which uses Barium titanate as a high permittivity metal oxide nanoparticle shows promise [165].

The ferroelectric property of titanates is an important attribute as ferroelectric crystals can be polarised at specific temperatures which can be reversed through the application of an external electric field [163]. In this study, Barium Titanate as a perovskite-phase oxide had a paraelectric cubic phase which would exhibit linear polarisation, however, it was required to anneal the material at 1000 °C to alter it from this phase to a tetragonal crystalline ferroelectric phase to achieve a dialelectric material with a permanent electric dipole and high permittivity (see Figure 5.1) [166] [167]. The associated permittivity effect on polymers is of interest here.

5.4.4 Methylammonium lead bromine ($CH_3NH_3PbBr_3$)

The structure of $CH_3NH_3PbBr_3$ is a framework which is comprised of corner-sharing MX6 octahedra with organic ammonium cations at the dodecahedral A sites (see Figure 5.2). The perovskite structure is apparently simple, however, by its design it is capable of complex chemical manipulations. Moreover, it is possible to tune the optoelectronic properties by heteroelemental doping or through varying halide anions, metal ions, or the organic cation.

Because ions migrate through the hybrid halide perovskite lattice structure it means that this material is suitable for electrochemical applications [170]. Specifically, the ions transport through the lattice structure of the perovskite and thus hybrid perovskites act as materials that are able to store charge [170]. An important attribute of perovskite-based electrodes is that they have high stability when there is electrochemical cycling which does not affect their crystal structure [170]. In reference to energy storage, this material has been used for anode electrodes and it is the 3D framework of the MX_6 octahedrons that have organic methylammonium cations between them that allows this [170].

As an organic / inorganic perovskite material, $CH_3NH_3PbBr_3$ contains defects which migrate when an external electrical field is applied, this provides I–V hysteresis [171].

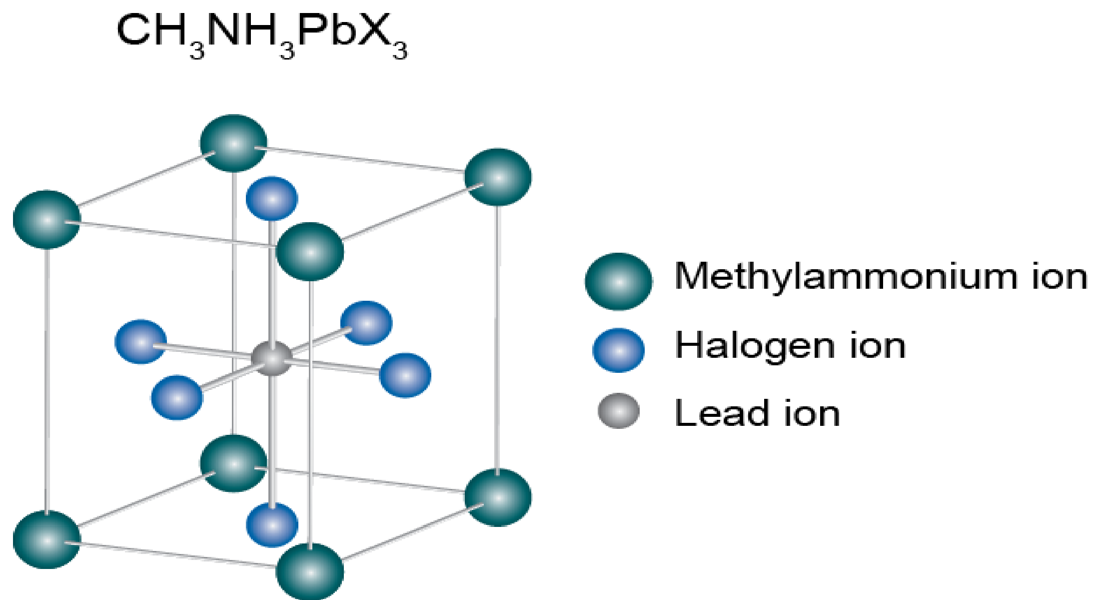


Figure 5.2 Crystal structure of $CH_3NH_3PbX_3$ perovskites (X=I, Br and/or Cl). The methylammonium cation (CH_3NH_3+) is surrounded by PbX_6 octahedra [172].

To summarise, each of the three materials have been presented and an explanation for testing these materials has been provided against the aim to test their suitability in memory devices and to verify the internal switching mechanism. Specifically, this has included an explanation of their role in the internal switching mechanism as a memory function. Different materials with different properties are tested in order to see if there are differences in the internal switching mechanisms. The materials and the associated properties are shown in Table 5-2.

Table 5-2: Material Properties.

	Nanoparticle	Ferroelectric	Perovskite structure	Organic	inorganic
NiO	Yes	No	No	No	Yes
$BaTiO_3$	Yes	Yes	Yes	No	Yes
$CH_3NH_3PbBr_3$	No	Yes	Yes	Yes	Yes

5.5 PVAc Conduction Mechanisms and Polymer Layer Optimisation

This section presents the technique and results for determining the quality and thickness of the polymer layer from spin coating and the potential conduction mechanisms of this active material. Spin coating as the technique for applying the PVAc can affect the thickness and quality of the layer which can also have an effect on the conduction mechanism.

5.5.1 Spin coating collaboration in PVAc

There were nine specific thicknesses of the PVAc that were tested. These different thicknesses were achieved through spin coating at various speeds, whereby the faster the spin speed, the thinner the layer, this is illustrated in Figure 5.3 (a) where spin speeds between 2000 rpm and 10000 rpm were used to achieve the nine various thicknesses. The thicknesses for each sample were measured using the Rudolf Research Auto Ellipsometer, the measurement was taken as an average from different measurements. At the same time

the refractive index provided the quality of the polymer layer which was 1.4, the same as the theoretical refractive index for PVAc (see Figure 5.3 (b)).

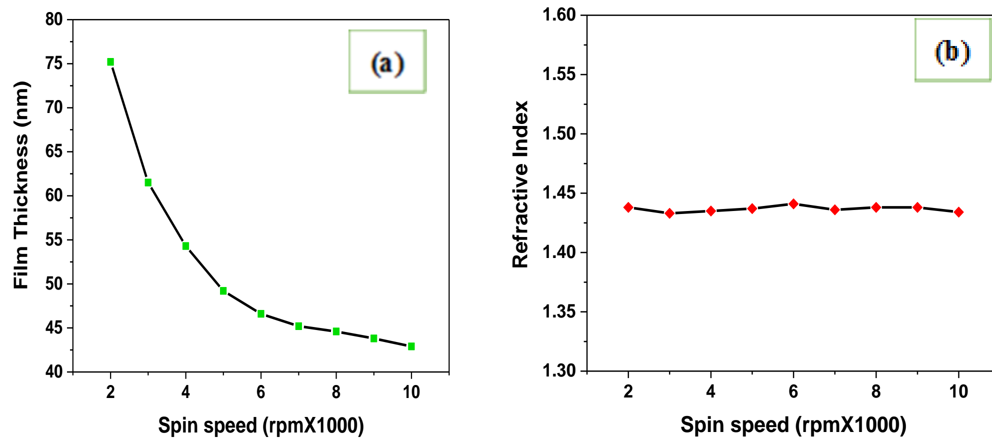


Figure 5.3 (a) Polymer film thickness and (b) Refractive index.

5.5.2 Conduction Mechanism

Towards understanding the conduction mechanisms of the active material with the polymer in the polymer memory device, it is necessary to establish and understand the conduction mechanisms in the polymer itself. There are a number of different potential conduction mechanisms in insulating materials, and it may be the case that more than one conduction mechanism is responsible at the same time (PRIME). Specifically, nine different thicknesses of the PVAc are tested in this study and it is likely that either Schottky emission or Poole-Frenkel emission is the conduction mechanism. It is important to note that these two mechanisms have similar temperature and voltage dependencies which would make it difficult to distinguish between them [77]. For this research the assumed I-V curves for both Poole Frenkel and Schottky emissions are

illustrated in Figures 5.4 (a) and 5.4 (b) together with the I-V curves for the PVAc layer. However, from this it is not possible to determine the exact mechanism as both I-V curves are similar.

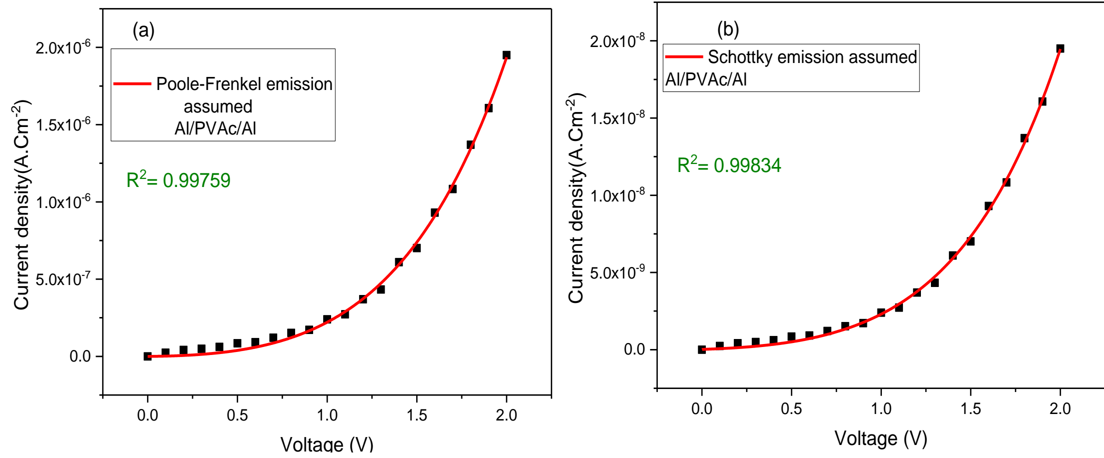


Figure 5.4 (a) Poole-Frenkel emission assumed and (b) Schottky emission assumed. R^2 represent the goodness of fit, If R^2 approaching 1, it means that the fit is good.

Therefore, it was required to determine the exact conduction mechanism through applying the Poole-Frenkel and Schottky emission equations to the I-V data. These mechanisms are expressed in a simple form, as shown in the following:

Poole-Frenkel has the following equation:

$$J_{PF} = C_o V exp(\beta V^{1/2}) \quad (5\text{-}1)$$

The Schottky emission takes the equation:

$$J_{SE} = C_o exp(\beta V^{1/2}) \quad (5\text{-}2)$$

From equation (5-1) and (5-2):

$$\beta_{PF} = \beta_{SE} = \frac{1}{KT}\left(\frac{e^3}{\pi n^2 \varepsilon_o d}\right)^{1/2} \quad (5\text{-}3)$$

From the equation it is noticeable that for the Poole-Frenkel emission the β coefficient is twice as large in comparison to the Schottky emission, which means that it is possible to distinguish between these mechanisms through looking at the I-V data.

The I-V characteristics of the polymer are calculated in the abovementioned equations and plotted as $J\ vs.V$ in order to calculate the experimental β value which can then be checked against theoretical values. These experimental plots are shown in Figure 5.5 (a) (1) and (b) (1) for Poole Frenkel emission and Schottky emission respectively, against the theoretical emissions (Figures 5.5 (a) (2) and (b) (2)). The Poole Frenkel emission for different thicknesses of PVAc corresponded with the theoretical Poole Frenkel emissions for the same thicknesses and therefore, it likely that Poole Frenkel is the conduction mechanisms.

Further verification that Poole-Frenkel emission was the conduction mechanism can be seen where the experimental and theoretical β values are plotted against each other (see Figure 5.6)

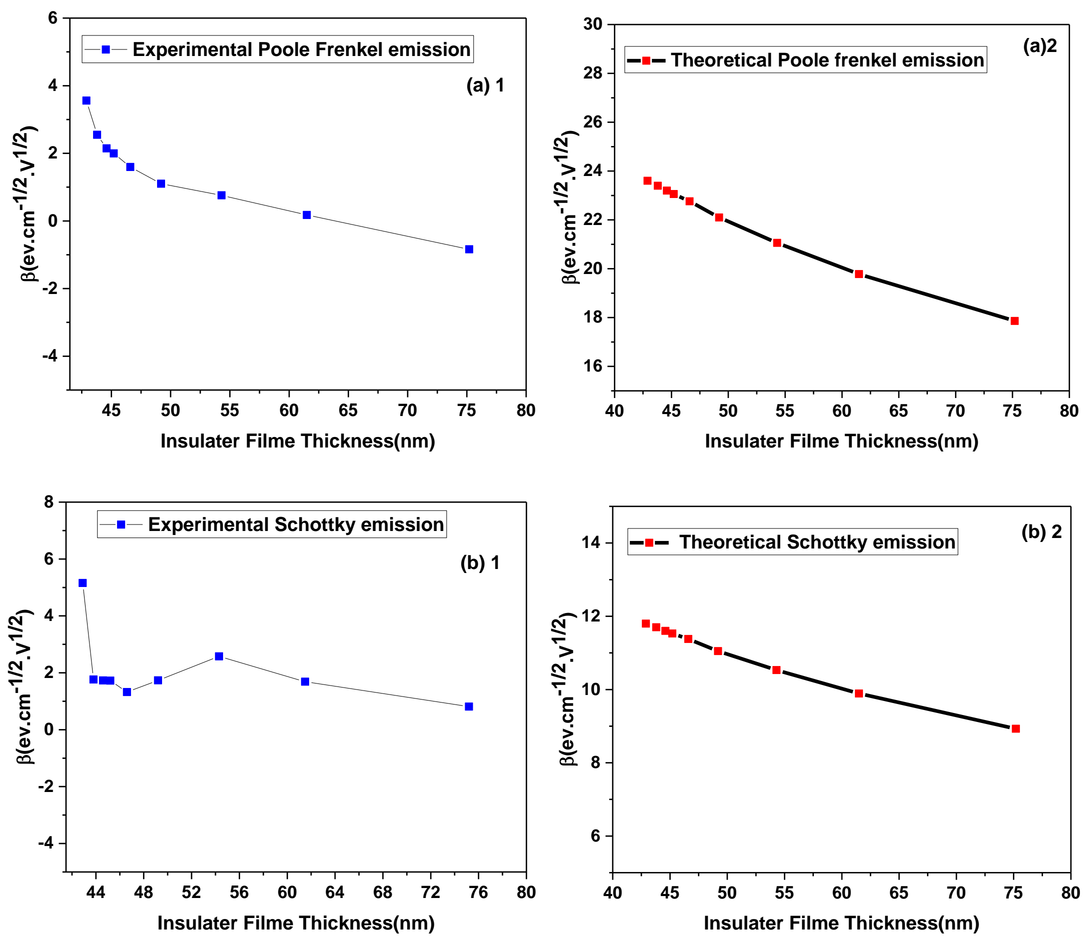


Figure 5.5 Experimental (a) 1 and theoretical (a) 2 β values for Poole-Frenkel emission. Experimental (b) 1 and theoretical (b) 2 β values for Schottky emission.

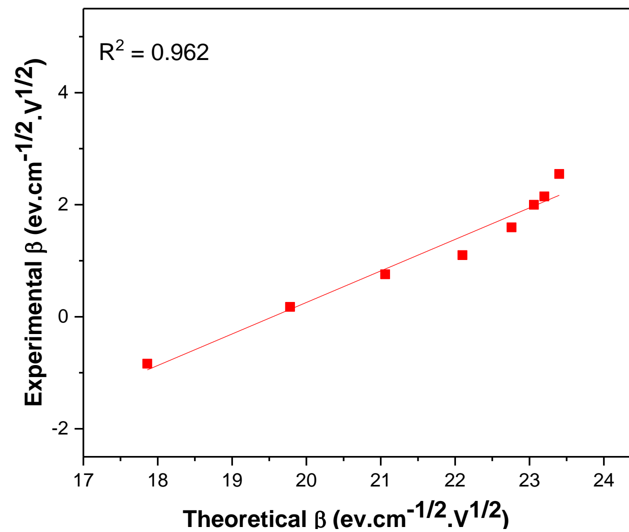


Figure 5.6 Experimental β values vs. Theoretical β values for Poole-Frenkel emission. On the basis of R^2 = 0.962, we can assume that there is a linear relationship between theoretical and experimental value of β. This will result in $\beta_{theoretical} = m\,\beta_{experimental}$. Here, m is positive number. The m can be used as an "adjusting constant" for the β values, obtained by fitting, from the experimental data.

5.6 Physical characterisation

The purpose of testing the physical characterisation of the material is to test the integrity of the material when in a composition with the polymer. This is achieved through SEM (Scanning Electron Microscopy), XRD (X-ray Diffraction), FTIR (Fourier-transform infrared spectroscopy) and UV – visible spectroscopy, which will confirm any morphology in the tested material.

5.6.1 Nickel Oxide (NiO)

Towards determining material properties, chemical composition, quality, and structure of the NiO nanoparticle and NiO blend with PVAc, XRD and FTIR analysis were performed

respectively, moreover, FTIR was used to analyse the PVAc alone and PVAc blend with NiO. The FTIR spectrometer was taken in the range of 4000 - 400 cm^{-1} at room temperature. Samples were prepared by dropping the NiO blend with PVAc and PVAc alone onto KBr substrate and the results are shown in Figure 5.7(a). The results for the PVAc and NiO blend show a strong band at 412.24 cm^{-1} that corresponds to the vibration of the Ni–O bond [173] [174] when compared to the polymer alone. Absorbance bands for PVAc tested alone were as follows: 1441 cm^{-1}, 1371 cm^{-1}, 1228 cm^{-1} and 1026cm^{-1} and 943 cm^{-1}. To quantify the presence of PVAc the 1228 cm^{-1} and 1026 cm^{-1} were used [175] [176] [177].

The standard stable phase of NiO is the cubic structure as confirmed by XRD (figure 5.6(b). The XRD for NiO nanoparticle (< 50nm) is illustrated in Figure 5.7 (b). The sample gave five peaks at 37.1, 43.2, 62.8, 75.4, and 79.3 degrees and these correspond to the 111, 200, 202, 311 and 222 planes of diffraction peaks for crystal planes of the cubic NiO [178] [179] [180].

The UV–visible absorption spectrum of NiO nanoparticles blended with PVAc shows an intense peak at 320 nm in comparison with PVAc only [178] [179]. It can be seen that the absorption edge corresponding to NiO appeared at 320 nm (Figure 5.8(a)). The optical direct band gap values of the NiO samples as shown in Figure 5.8(b) were determined by Tauc's relation [180] [181]:

$$\alpha\, hv = \alpha_o\, (hv - E_g)^{n} \qquad (5\text{-}1)$$

In this equation hv, α_o and E_g denote photon energy which is a constant and optical band gap of the nanoparticles 'n' is index related to the density of states for the energy band. It is assumed, n = ½ for direct allowed and n = 2 indirect allowed transitions. The absorption spectra are used to calculate the absorption coefficient (α) of the powders at different wavelengths. The values of E_g were calculated by extrapolating the linear regions of the plot $(\alpha h\upsilon)^2$, against photon energy. EDX analysis of the NiO in Figure 5.9(b) shows the high purity of the sample.

The morphology of the PVAc and NiO nanoparticles blend sample, spin coated at room temperature, is illustrated in Figure 5.9 (a). The properties show promise in respect to device application. The formation of the metal nanoparticle at room temperature is integrated with the semiconductor and polymer dielectric which makes a non-volatile memory which is polymer-base.

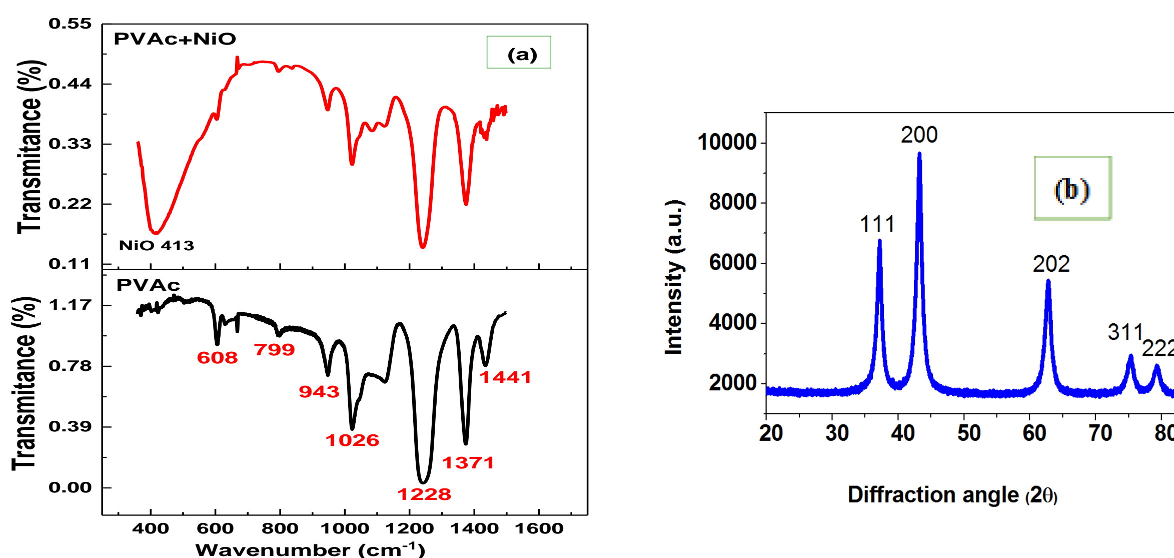


Figure 5.7 Present (a) FTIR Spectra of PVAc and PVAc blend with NiO, and (b)XRD pattern for NiO powder (Particle size <50nm).

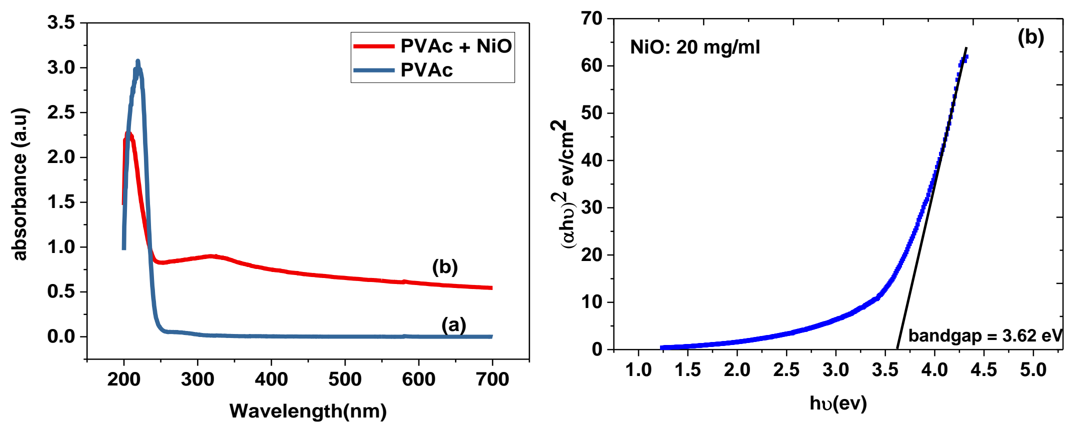


Figure 5.8 (a) UV–Visible absorption spectrum of PVAc and PVAc blend with NiO, and (b) Optical band gap of the NiO.

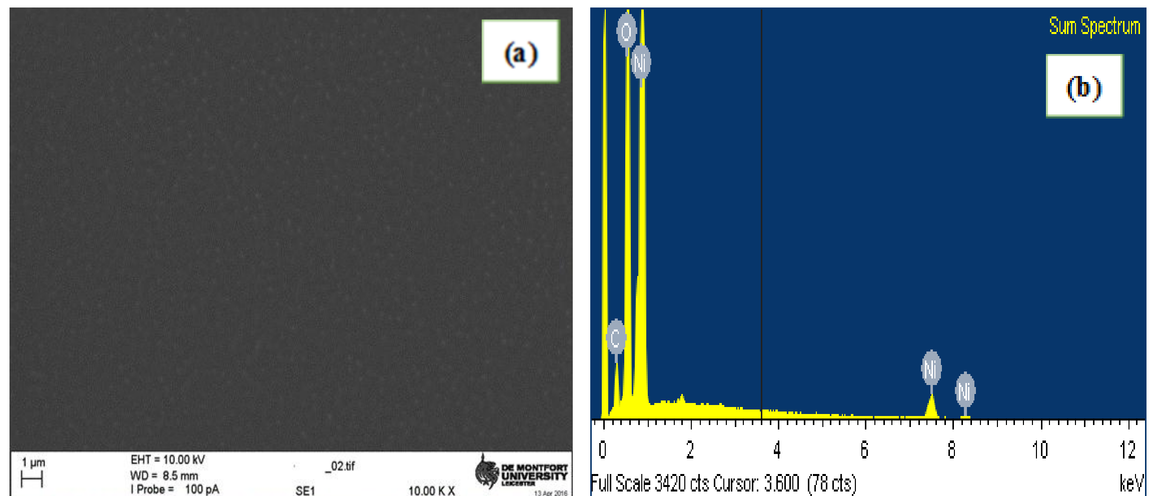


Figure 5.9 (a) SEM images of PVAc +NiO blend showing the smooth surface (b) EDX of NiO.

5.6.2 Barium Titanate

Barium titanate nanoparticles tested in this study were obtained from Sigma Aldrich in the condition of a cubic phase ~100nm in size. Annealing was conducted to change the structure of the $BaTiO_3$ nanoparticles from a cubic phase to a tetragonal phase. Peak

splitting of around 2θ = 45 occurred after annealing and obtained (200) and (002) peaks. The change in the phase of the $BaTiO_3$ nanoparticles and the annealed sample was shown by XRD (Figure 5.10). However, annealing also causes the particle size to increase (~200nm) which could affect the uniformity of the thin films and device functionality. In reference to the specific process, a quantity of Barium titanate is put into a ceramic boat and heated to a temperature of 1000˚C for one hour in the air as the process requires oxygen [182] [183].

Transition from the para electric cubic to ferroelectric tetragonal (a, b = 3.98 Å ; c = 4.03 Å) phases in the structure occurs when the temperature goes below Tc of the material. In the case of $BaTiO_3$, this transition occurs at Tc ~ 120°C [183]. The tetragonal perovskite phase is responsible for polarisation and thus, the ferroelectric behaviour of the material (Figure 5.10). Above the Curie temperature (T_c), the structure is a face centred cubic (F_{CC}) structure (lattice constant = 4.01 Å) whereby the Barium and Oxygen atoms occupy all of the corners and faces respectively. The Titanium atom occupies the body-centre on the octahedral site formed by the Oxygen octahedron.

SEM (Scanning Electron Microscopy) examination shows that there is a clear difference in the size of the crystal structure between the cubic and tetragonal phase (see Figure 5.11) and verified using X-Ray diffraction (XRD). The XRD results (Figure 5.10) illustrate a difference between the cubic phase and the tetragonal phase at the 2θ = 45 position, this is clearly seen in the shape of the peak which features a distinct shoulder which cannot been seen in the cubic phase, therefore, this is an indication that phase change has taken place.

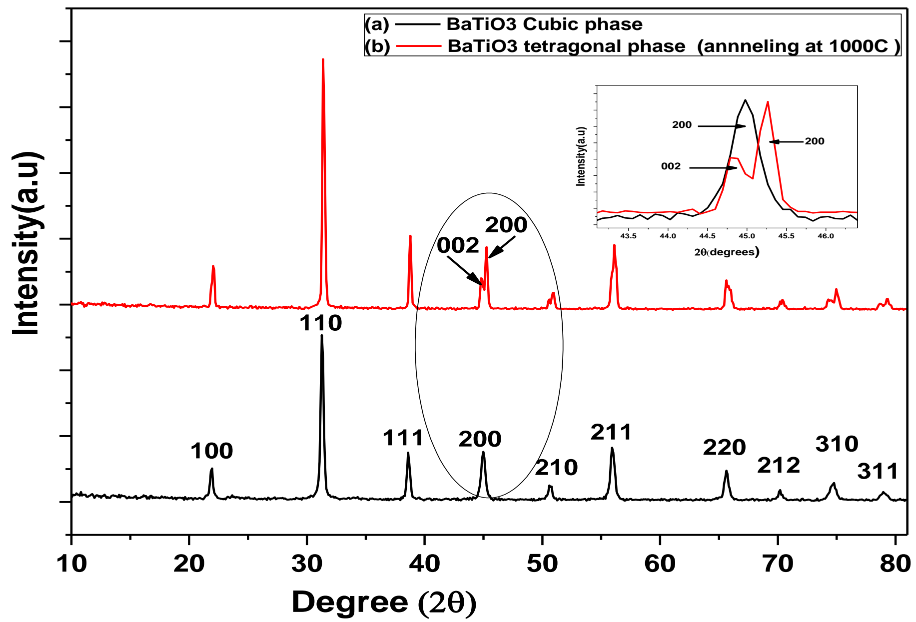


Figure 5.10 XRD patterns of (a) $BaTiO_3$ nanoparticles as-purchased and (b) $BaTiO_3$ nanoparticles annealed at 1000℃ in air. It can be observed that the phase of nanoparticles has changed from cubic to tetragonal phase. The inset illustrates an asymmetric

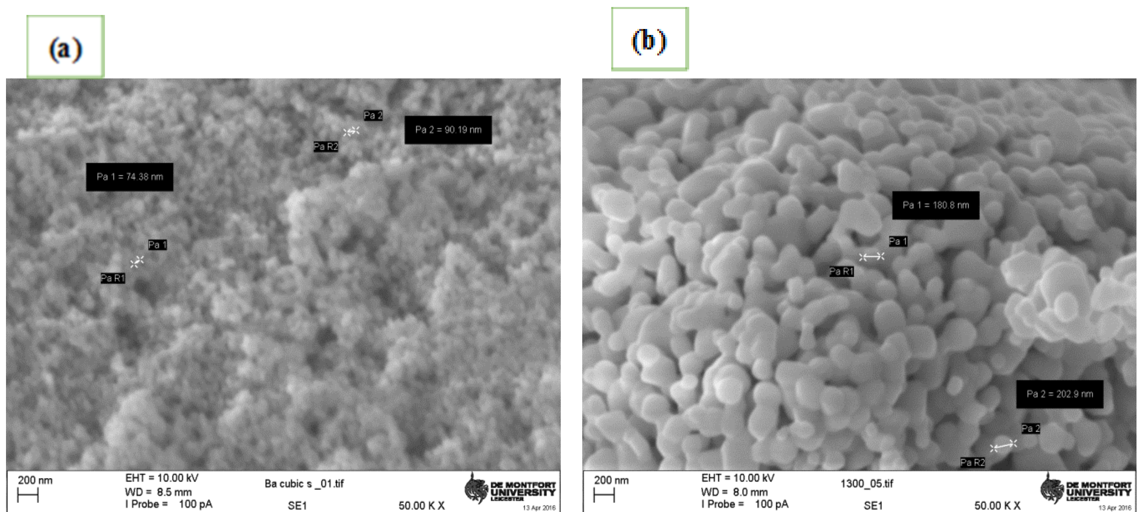


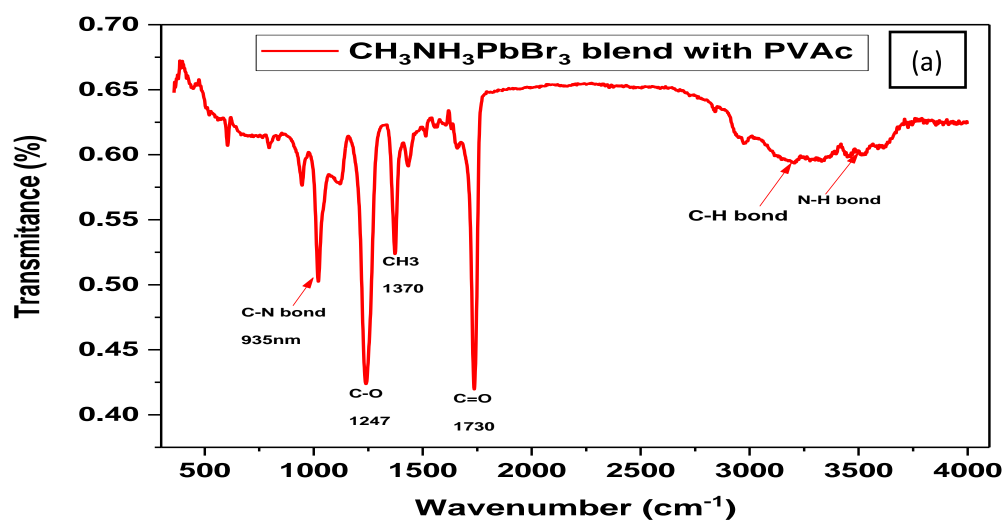
Figure 5.11 SEM images of barium titanate (a) cubic phase and (b) tetragonal Phase.

5.6.3 Methylammonium lead bromine ($MAPbBr_3$)

Methylammonium lead bromine (MAPbX3), as an organic-inorganic lead halide perovskite material, was fabricated using inverse temperature crystallization [184]. For the first step one molar solutions of PbX2 and MAX ($X = Br^-$) and were prepared in dimethylformamide (DMF) solvent. These solutions were mixed into a growth solution which was heated to 60˚C while constantly stirring for 15 minutes. The mixture was then filtered using a polytetrafluoroethylene (PTFE) filter with a pore size of 0.2 µm and 2 ml of the filtrate was placed in a vial and then placed in an oil bath at 80˚C. At humidity of between 55 – 57 % crystals formed within the growth solution. Throughout these procedures ambient conditions were maintained. Under these conditions the reaction yield for $MAPbBr_3$ under these conditions was recorded at 35 wt. This process was prepared and approved using FTIR and XRD by Hessa Alsulaimi (department colleague)

The chemical composition, material integrity and structure of $MAPbBr_3$ in the polymer were investigated by FTIR and XRD technique (Figure 5.12). The FTIR spectrometer was taken in the range of 4000–400 cm-1 at room temperature. Samples were prepared as explained in section 5.3.1. FTIR spectrum of the polymer blend showed vibration peak at around 1736 cm-1 (C=O stretching), 1370 cm^{-1} (CH_3 bending) and 1264 cm^{-1} (C-O stretching) corresponding to the vibration of the PVAc [164]. An additional peak was observed around 3198 cm^{-1} and 3464 cm^{-1} identical to C-H and N-H stretching. The presence of Pb-Br and H-Br in the FTIR are below the finger point region of FTIR which may be in the range of 300-500 cm^{-1} (figure 5.12(a)). Figure 5.12(b) prove the material colour.

XRD measurements were used to verify the crystallisation of the perovskite film, as shown in Figure 5.11(c). Diffraction peaks were present in XRD pattern at 14.83°, 21.31°, 32.23°, 36.5, 42.8° 43.2°, 45.12°, 47.5°, 52.1° and 55.1° which corresponded to the crystal facets of (100), (110), (200), (210), (211), (220) (300), and (310) which indicate the typical Cubic $CH_3NH_3PbBr_3$ phase with high crystallinity in the film [185] [186] [187] [188]. However, some peaks were in the XRD pattern which may be associated with trace amounts of impurities of $PbBr_2$ (as present by (*)), and CH_3NH_3Br [189], which have been commonly found in perovskite films and impurities of PVAc blend.



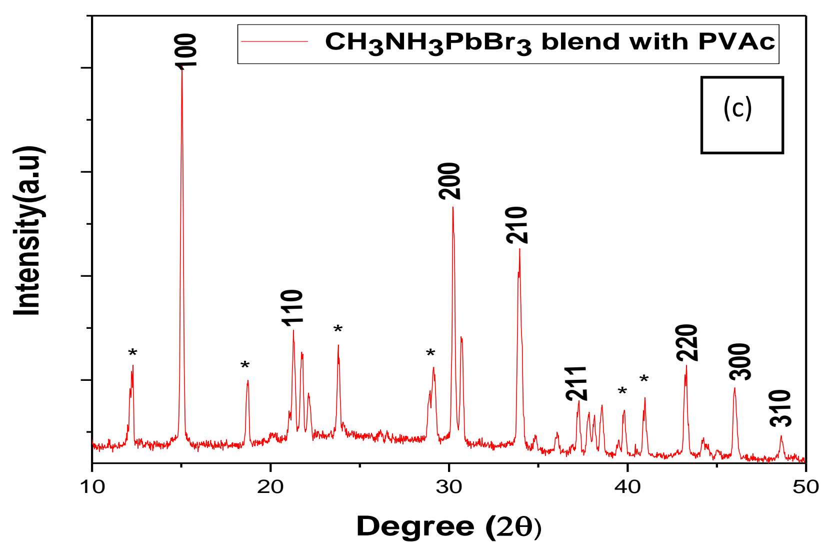


Figure 5.12 (a) FTIR spectra, (b) Photo image of the $MAPbBr_3$ thin film on glass substrate, and (c) XRD pattern of $MAPbBr_3$ blend with PVAc, peak with (*) related to $PbBr_2$.

5.7 Devices Fabrication

In this section, there is a description the fabrication for both types of devices, MIM and MIS, and both blend and layered material compositions. These two types of two-terminal devices were fabricated with two different methods to create the internal electric field; the MIM structure was used to test the charging mechanism and memory device programming and the MIS structure was used to measure capacitance and charge retention and durability. These tests were conducted for the three tested materials as a blend or layers with the polymer PVAc. In this section the methods for the blend composition and layered deposition, as well as the MIM and MIS structures is described.

5.7.1 MIM and MIS structures

In order to test the materials for memory device programming and charge retention two different device structures were required. The MIM structure was used to investigate charging mechanisms for memory and memory device programming and the MIS structure was used to investigate capacitance and charge retention and durability. The memory device MIM structure with the tested material blended with the polymer was fabricated by initial thermal evaporation with base pressure 1×10^{-6} Pa vacuum, of the Aluminium bottom contact electrode tracks: 100 nm thick, 1 mm wide and 22 mm long were placed onto the glass substrate, then a 10nm insulating layer of the PVAc (10mg/ml) film as blocking layer. Where the layered structure is tested, after the blocking layer a layer of the material is deposited followed by a layer of PVAc, thereafter, the electrode tracks are deposited on the top. For the blend structure, the blend layer is spin coated onto the electrodes with the additional electrode placed on top (Figure 5.13 a1).

In order to perform the C-V measurements to determine how much charge can be retained, and the charge retention and durability test to determine how long the charge can be retained for, both as measurements of memory ability, a capacitor structure is used, specifically the MIS (Metal-Insulator-Semi-conductor) structure. The tested material blended or layered are formed onto a p-type silicon substrate with an ohmic back contact. The PVAc / active material blend was spin-coated onto the substrate using a methanol solvent at 4000 rpm. Al was thermally evaporated for the upper electrode. Figure 5.13(b) below is a schematic representation of the devices. I-V and C-V measurements took place respectively on using HP4140B Picoammeter, and on an HP 4192A Impedance Analyser performed at 1 MHz frequency, presented in the following chapter.

For the memory device, there needs to be consideration of the fabrication methods in terms of the material itself, whether it is a blend, or it is a layered structure and whether the device is MIM or MIS. For both MIM and MIS device structures, regardless of material deposition, the evaporation technique is used for the deposition of the terminals as electrodes. Specifically, the devices were fabricated onto a clean glass and p-type silicon substrates. Aluminium tracks were then thermally evaporated onto the glass substrate using a vacuum pressure of approximately 6 x 10^{-6} Pa to form Al bottom contact in an Edwards Auto 306 evaporation chamber. Finally, the thermal evaporation of top the Al contact electrodes was deposited in a perpendicular direction to the bottom contacts, resulting in a cross-level architecture (Figure 5.13).

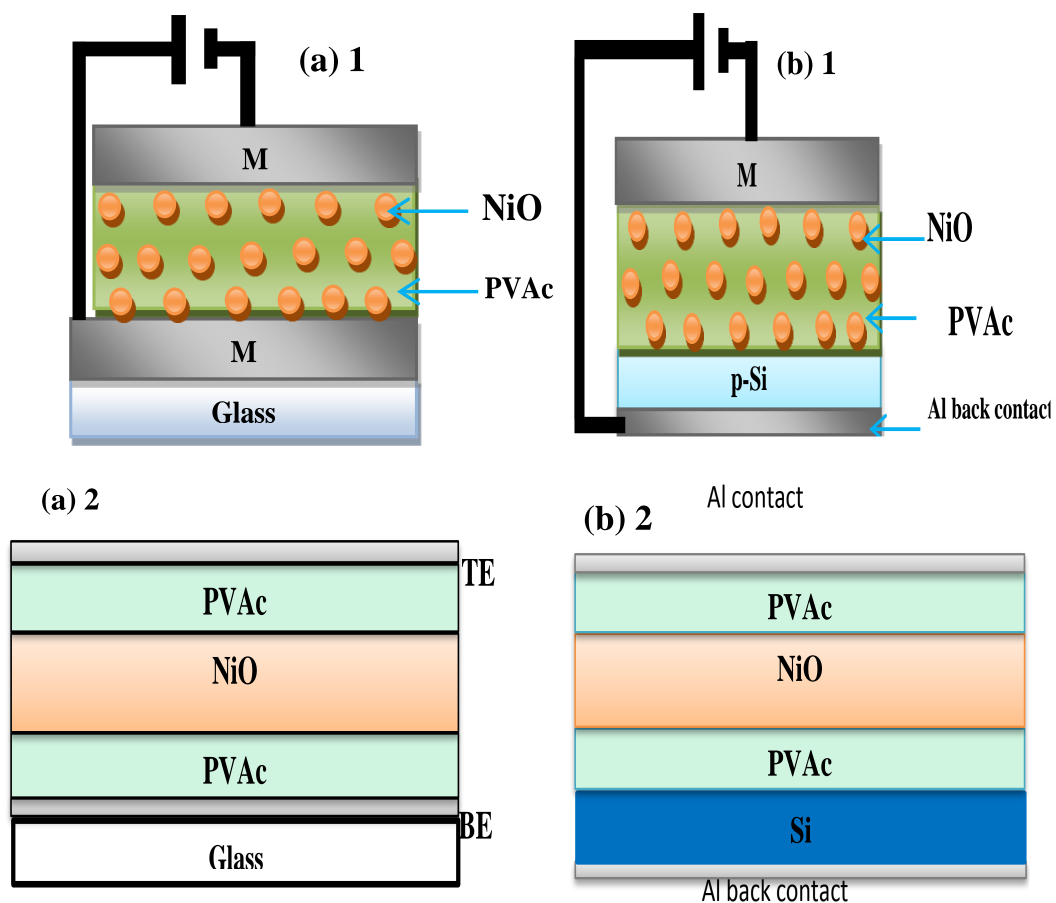


Figure 5.13 Figure 5.12 (a) 1 MIM (blend) and (a) 2 MIM (layered). (b) 1 MIS (blend) and (b) 2 MIS (layered).

It is important to note that all the devices were constructed on glass substrate (2.25 cm^2) and p-type silicon <100> wafers (boron-doped silicon) with aluminium ohmic back contact.

5.7.2 Blend deposition

Both MIM and MIS structured are tested with a blend of the three tested materials (NiO, $BaTiO_3$ and $CH_3NH_3PbBr_3$) and PVAc using a solution method achieved through spin

coating. Spin coating (as presented in section 4.3) was used for depositing the different blends of varying material concentrations onto cleaned substrates, which comprise of the deposited Al electrodes, at 4000 revolutions per minute (rpm). An Al electrode was deposited on the top as the final step in the fabrication procedures of these devices. It should be noted that before every fabrication, the substrates are well cleaned with acetone, IPA and rinsed with DI water (18MΩ).

5.7.3 Layered deposition

The MIM and MIS structures are tested as layered structure and is comprised of the tested material between polyvinyl acetate layers. This structure is achieved through the evaporation method and through spin coating. Specifically, the spin coating method is used for the polymer layer and then the evaporation method is used for the layer of the tested material.

The PVAc (polymer) layer was deposited by spin coating at room temperature, followed by evaporation of tested material NiO and $BaTiO_3$ and using a vacuum evaporator, the spin-coating of PVAc (30 mg/ml) dielectric film on top of the tested material.

5.8 Summary

In summary, this chapter has presented the materials that are to be tested, their composition, physical characterisation and how they are prepared for experimentation in this study. The devices structures and how they were fabricated, as well as the reasons for using both MIM and MIS structures was also presented. Moreover, there was a

presentation of the blend and layered structures of the tested materials and how this was achieved through spin coating and evaporation techniques.

Chapter 6 Memory Characterisation – MIM structure

6.1 Introduction

As part of investigating the role that the tested materials as a blend and as a layer with the polymer in various concentrations plays in terms of performance of memory behaviour and device switching mechanisms, electrical measurements were performed on MIM structures. Specifically, current-voltage measured through I-V hysteresis was used to measure the charging mechanism and for memory device programming write, read, erase, read (WRER) cycles were conducted on the MIM structure. Experimentation for testing the charging mechanism was conducted for each of the three tested materials. Specifically, each material was tested as a blend with the polymer (PVAc) and then as a layered structure of the tested material and the polymer. The following sections present the experiments and the findings presented for memory characterisation as IV hysteresis measurements and associated charging mechanism. Furthermore, the MIM structure has been investigated, for blend and layered compositions, to understand the bistability phenomenon towards approving the switching polarisation mechanism proposed by Paul [4].

6.2 Memory Characterisation of Nickel Oxide

In consideration of the possible reasons for the hysteresis observed here it is important to take account of the fact that as the active material, NiO, is a metal oxide which have demonstrated filamentary conduction in previous work. Through the application of an

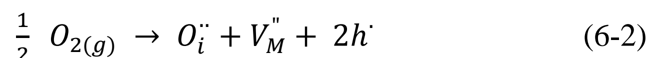
electric field the formation of a conducting filament (CF) would be initiated [189]. As the field is removed, the CFs are destroyed. It is believed that the making and breaking of these CFs takes place over a nanometre-scale region within a short time period in nanoseconds [3] [141] [189]. The formation of CF is a consequence of the electric stress which results in a decrease in resistance of the cell.

CF formation involves the transfer of charge (electrons) via ions (redox reaction). A significant decrease in cell resistance can increase power dissipation and as a consequence the cell can be damaged (dielectric breakdown).

It must be remembered that NiO is a hyper-stoichiometric transition metal oxide ($MO_{x+\delta}$, $\delta > 0$) [189] [190]. This hyper-stoichiometry is a result of cation vacancies or oxygen interstitials, this is denoted in the Kröger–Vink notation [191] as follows:

$$\frac{1}{2}\ O_{2(g)} \rightarrow O_i^{\cdot\cdot} + 2h^{\cdot} \qquad (6\text{-}1)$$

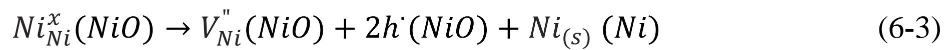
And respectively



$$\frac{1}{2}\ O_{2(g)} \rightarrow O_i^{\cdot\cdot} + V_M^{''} + 2h^{\cdot} \qquad (6\text{-}2)$$

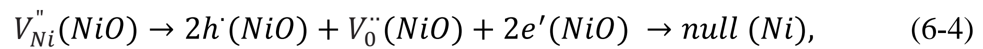
Defects in the material are the result of electrochemical or thermodynamic oxidation which acts as acceptors so $MO_{x+\delta}$ becomes a p-type semiconductor. In electroforming, an electrolysis reaction occurs at the location of the anode, resulting in a reduction of the transition metal oxide. Therefore, the anode acts as a defect source. There is a switching cell which undergoes electroforming and has a defect source which is the anode, the sink and a spacer, these are resistive for the ion / defect migration, which creates a separation

between the sink and the source [192] [193] [194]. Rodriguez et al. and other researchers suggest that oxygen vacancies and not Ni interstitials are created when there is reduction [195] [196]. Moreover, NiO is considered to possess an inherent defect nickel vacancy instead of oxygen interstitial [189] [197] (Figure 6.1 (a)), which means the defects, which are oxygen and nickel vacancies, exist together in the electroforming voltage. Oxygen and nickel vacancies migrate towards the cathode and the anode, respectively, under an electroforming voltage (Figure 6.1 (c)). With an absence of a nickel vacancy source, there is a decrease in the concentration of nickel vacancies at the location of the cathode, this is because they migrate to the anode (Figure 6.1 (d)). At the same time, there is a pile up of oxygen vacancies from the anode at the location of the cathode (Figure 6.1 (d)). Where there are increased concentrations of oxygen vacancies at the location of the cathode, it results in more single-phase instability of the NiO at the cathode. Because the principles of thermodynamics will not permit oxygen-deficient NiO, the NiO that is close to the cathode could go through phase separation. The Kröger–Vink notation [189] [191] for this is shown as follows:



$$Ni_{Ni}^{x}(NiO) \rightarrow V_{Ni}^{''}(NiO) + 2h^{\cdot}(NiO) + Ni_{(s)}\ (Ni) \qquad (6\text{-}3)$$

And



$$V_{Ni}^{''}(NiO) \rightarrow 2h^{\cdot}(NiO) + V_{0}^{\cdot\cdot}(NiO) + 2e'(NiO) \ \rightarrow null\ (Ni), \qquad (6\text{-}4)$$

NiO and Ni shown in parentheses show the location of the defects (Figure 6.1 (a)). As a result of this, the metallic Ni phase will grow from the cathode to the anode (Figure 6.1 (b)), resulting in an electroformed state (Figure 6.1 (c)). It is not possible for the Ni phase

to grow from the anode due to a decrease in the number of Ni ions. Furthermore, equation shows the phase boundary located between the Ni and the NiO acts as a nickel vacancy source, which were not present before the phase separation took place. The procedure of conducting Ni filament growth whilst electroforming is taking place is shown in Figure 6.1 below.

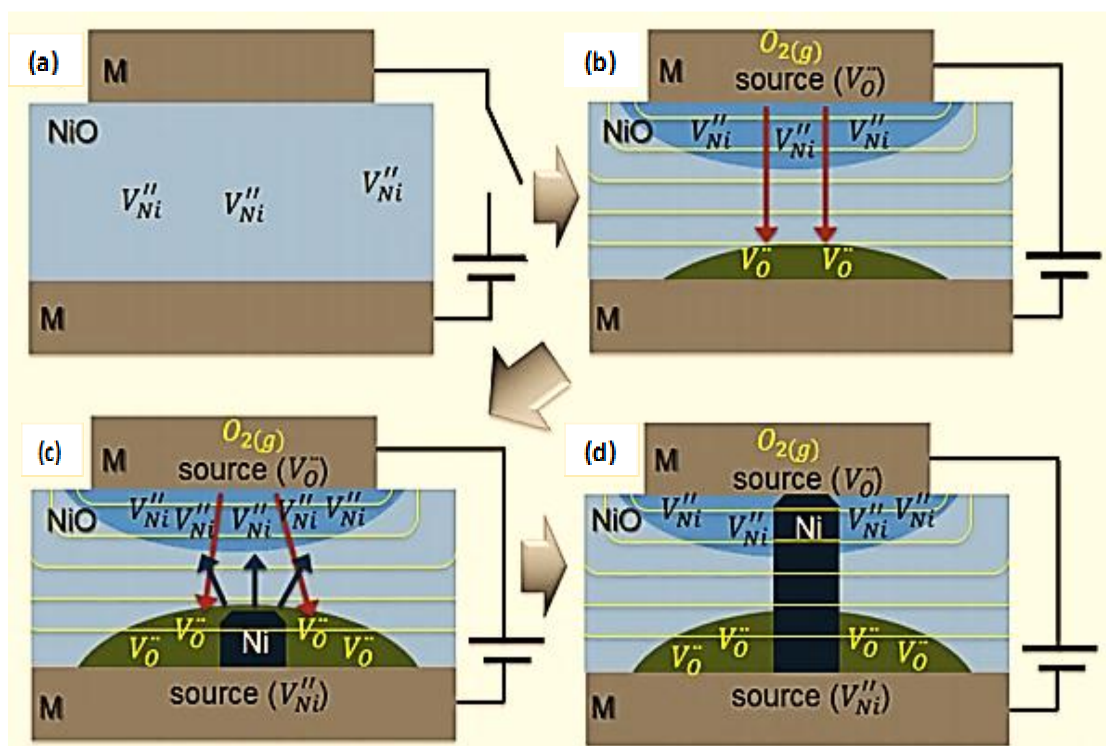


Figure 6.1 Diagram of CF growth in hyper-stoichiometric NiO[166].

This may be due to the stronger internal electrical field consequence of a larger number of charges in the dipole system.

In the present study, because NiO was tested, it would be expected that the linearity curves would indicate ohmic conduction behaviour which are the result of the formation of conductive filaments in NiO, therefore, filamentary conduction would have taken place [198]. However, this was not observed in the present study, as the results in the following section will show.

6.3 Results for Memory Characterisation of Nickel Oxide (NiO) (Blend).

Current – Voltage measurements are conducted in order to determine the memory characteristics of the various concentrations of NiO, specifically, blended concentrations of 5, 10, 20, 25, 30 and 35mg / ml of NiO. This is achieved by measuring the current through negative and positive voltage sweeps to verify if there is hysteresis in the I–V behaviour. The voltage sweep is between -1Vand +1V. It is expected that there will be different electrical behaviour observed for the different NiO concentrations.

The I-V plots can be found in Figure 6.2 below. From the curves, it was observed all devices (containing different concentrations; 5, 10, 20, 25, 30 and 35mg/ml of NiO (Table 6-1) exhibit hysteresis of varied widths.

From these I-V characteristics (Figure 6.2) it is evident that NiO in various concentrations has an important role in the electrical behaviour of these devices. Firstly, there is a very significant increase in current of order of 2 in devices containing NiO compared to devices containing just PVAc as a control sample. Furthermore, it was observed that the

samples with higher concentrations of NiO exhibited higher magnitudes of current. This has implications for the various NiO concentrations in terms of current hysteresis.

Table 6-1 : Concentration of NiO in PVAc.

Sample No.	PVAc (mg/ml)	NiO (mg/ml)
0	10 (control sample)	0
1	10	5
2	10	10
3	10	20
4	10	25
6	10	30
7	10	35

The increase in hysteresis occurs as a result of the charge being trapped, this amount of trapped charge is something that is indicated by the area found within the loop. Therefore, is was necessary to carry out a comparison of this area for the various NiO concentrations. These I-V characteristics are typical of resistive switching devices [199]. At this point it is important to reiterate that the expected filamentary conduction was not observed in the results of this research. In light of the results that were observed it is therefore appropriate here to consider possible explanations.

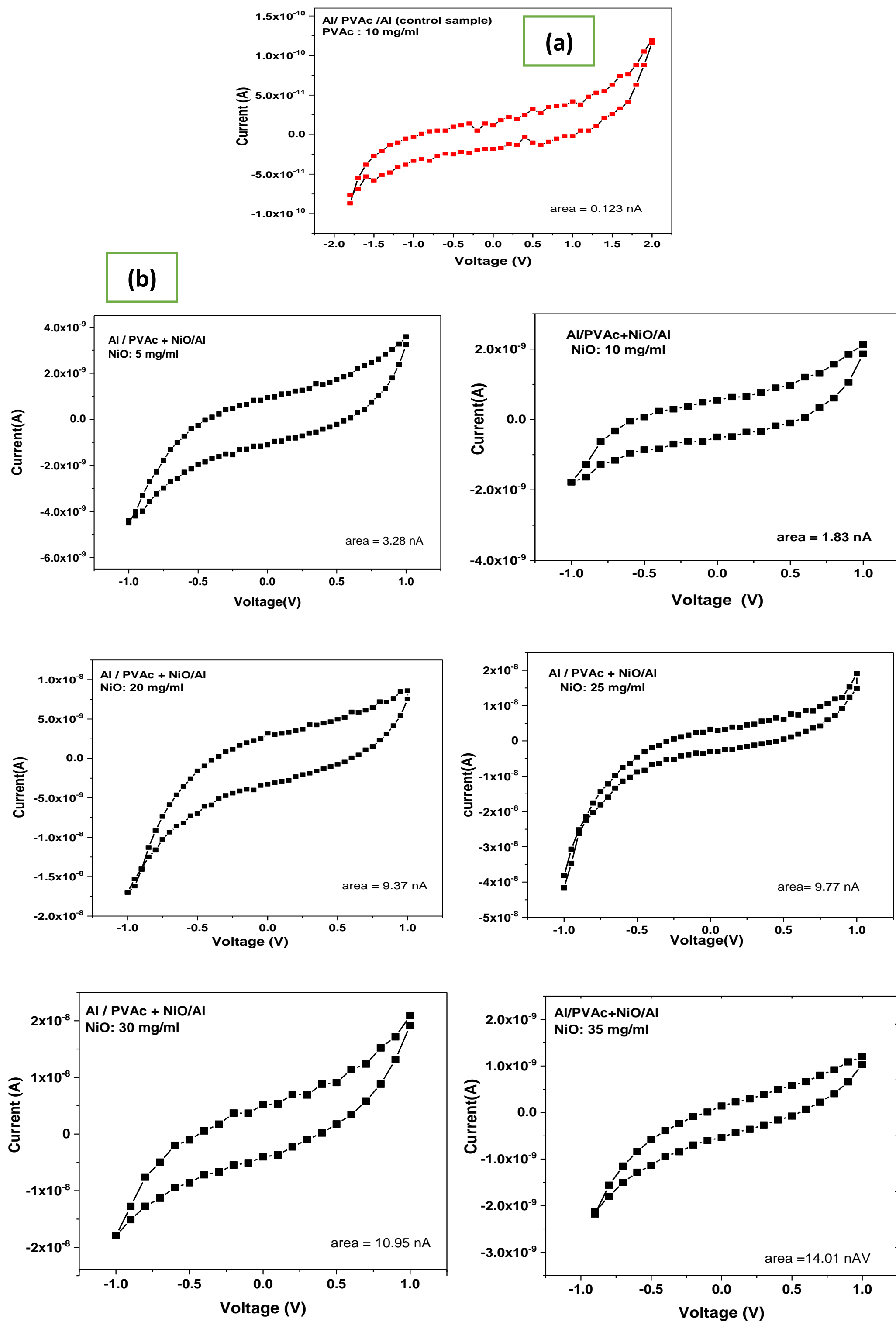


Figure 6.2 I-V characteristics of pristine (a)Al/PVAc/Al device (control sample) and (b) Al/PVAc+NiO/Al device at different concentration of NiO with PVAc.

The possibilities for the observed hysteresis in this study include charge trapping which could take place at the surface between the NiO / polymer and the top electrode or inside the material where the defect state causes charge trapping.

Because filamentary conduction was not observed, and hysteresis was observed, it was necessary to verify if this hysteresis was due to charge trapping. One indication of charging trapping in a NiO resistor memory is that the bond between the nickel and the oxygen is not broken if the bond is broken it is an indication of filamentary conduction. This was achieved through FTIR analysis. For this procedure the aluminium electrodes are placed onto the substrate followed by the NiO/ polymer blend which was drop cast onto the substrate. The two electrodes were connected to a picometer and measurements were taken. It is important to note that this is a horizontal structure, in contrast to the actual device structure which is vertical, therefore, for verification purposes, it was also necessary to conduct the same FTIR analysis for the device structure. Initially, the material was measured without any voltage being applied, then different voltages were applied and measured, readings were also taken between each voltage. The FTIR analysis was conducted using two different substrates which were KBr and SiO_2 (see figure 6.3(a)). When the voltage is applied KBr may affect conductivity which could affect the result, therefore, SiO_2 was used as a control.

The results showed that the bond for NiO remained intact, at 412 cm^{-1} for all voltages which indicates charge trapping and not filamentary conduction. This was found for both substrates KBr and SiO_2 (see figure 6.3(b)). Other wavenumber peaks (Figure 6.3 (b) 1) were observed which were an indication that the polymer bonding also remained intact.

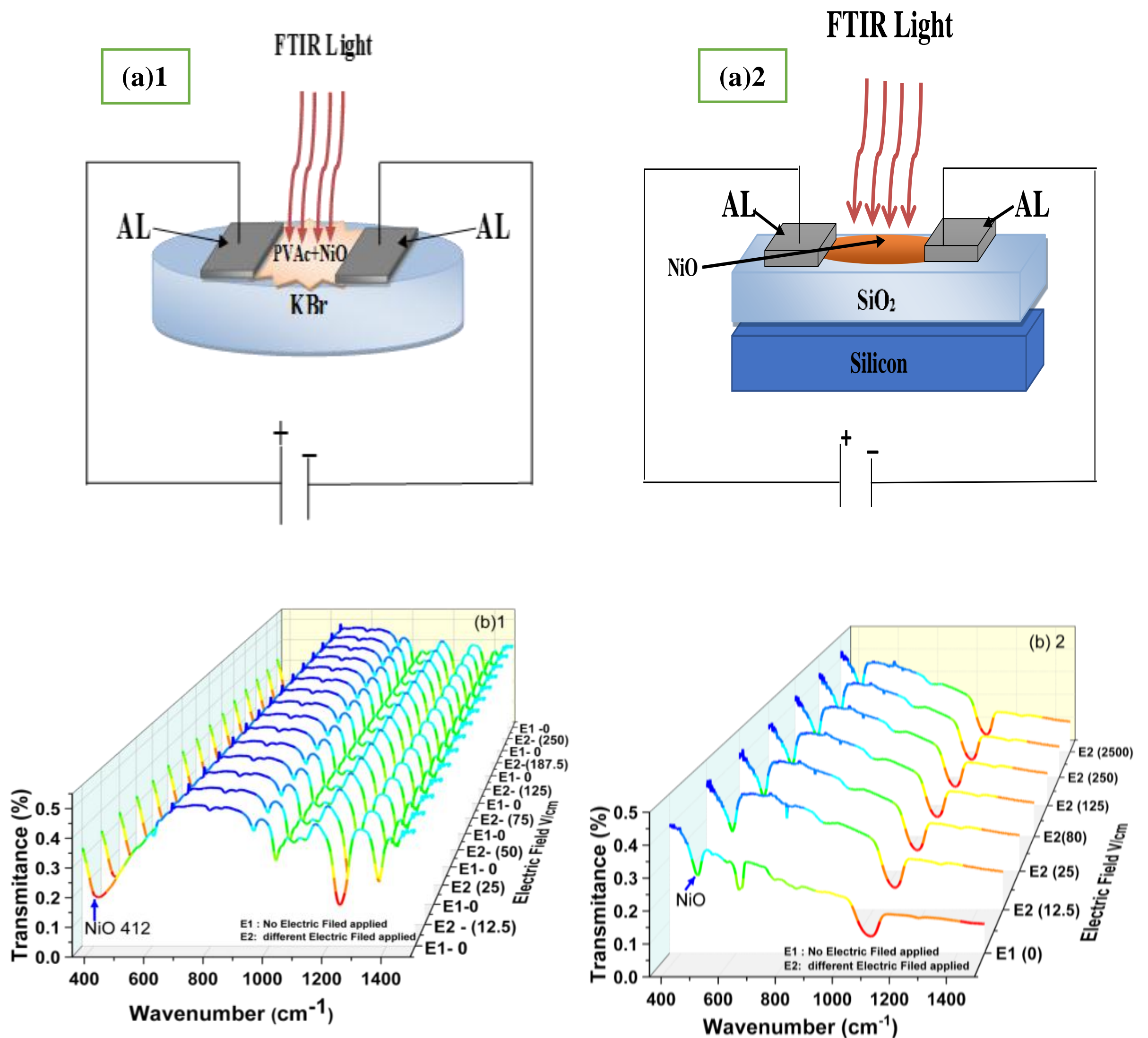


Figure 6.3 (a) FTIR Experiment diagram on (1) KBr substrate and (2) SiO2 substrate. (b) FTIR result of (1) PVAc +NiO on KBr substrate and (2) NiO on SiO2 at different Electric field V/cm.

In specific reference to the charge trapping within the material and in consideration of the fact that an insulating polymer is used in this material, there are three types of charge trapping that take place within the material, namely fixed insulator charge, the insulator

trapped charge and the mobile ionic trapped charge. The non-ideality of these charges provides the fixed insulator states and memory application in the MIM structure

The fixed insulator charge can be found at the interface between the NiO and the PVAc in the blend and it is the fixed traps in this insulating layer that causes the I-V hysteresis that has been observed here, providing the memory effect.

Another possibility for the observed hysteresis is insulator trapped charge which is found in the PVAc and can result from the manufacturing process or normal operation resulting from injection of electrons or holes from the substrate [78]. A further consideration is mobile ionic trapped charge which is a result of contaminants in the polymer, which could include sodium as it is used in the manufacturing process and not completely removed [77].

It is also necessary to consider the idea of charge at the surface between the top electrode and the active material, known as interface trapped charge. This could be due to structural defects in the top electrode. A mechanism has been proposed by Simmons and Verderber (1967) [108]. Upon bias being applied to the electrode, atoms move from the electrode to the insulating layer whereby an impurity band of charge transport levels is formed, in addition to deeper charge trapping levels [121]. When a low voltage is applied the charge is injected from the electrode and goes through the transport states when the voltages reach the negative differential resistance (NDR) region then there is a build-up of charge tunnels and a space charge field [121]. These build-ups then oppose the field at the injecting electrode resulting in a reduction in current, and when the current is removed

the charge remains in the traps, this results in the bistability that is evident in the results here.

In Figure 6.2 the I-V characteristics have shown bistability, however, to prove the long-term performance of the tested memory device it is necessary to conduct experiments for Write, Read, Erase and Read cycles are tested. The WRER cycles were conducted to investigate memory properties using write and erase voltages of ±1 V and a read voltage of 0.6 V in 25, 30 and 35 mg/ml of NiO nanoparticle in PVAc admixture. The WRER characteristics are shown in Figure 6.4.

It was observed that the devices switched between two resistive states as the write-read-erase-read voltage pulses were applied. When a write pulse of 1 V was applied and read at 0.6V, a high resistive state (HRS) (low current ≈ 2 nA for the 25 mg/ml NiO device for example) was recorded and when erased at -1V and again read at 0.6V, the device switched to a lower resistive state (LRS) (higher current ≈ 5 nA for the 25 mg/ml NiO device). This was observed for all tested devices and these two states stayed constant for more than a thousand Write-Read-Erase-Read cycles. Generally, the read current after the write pulse was lower than the read current after the erase pulse. The switching from HRS to LRS can be compared to the digital “0” to “1” states in a non-volatile memory device. The HRS and the LRS can also be termed the “OFF” and “ON” states respectively of the device. For non-volatility, it is desirable that the on/off ratio should remain constant. This was the case seen with all the devices.

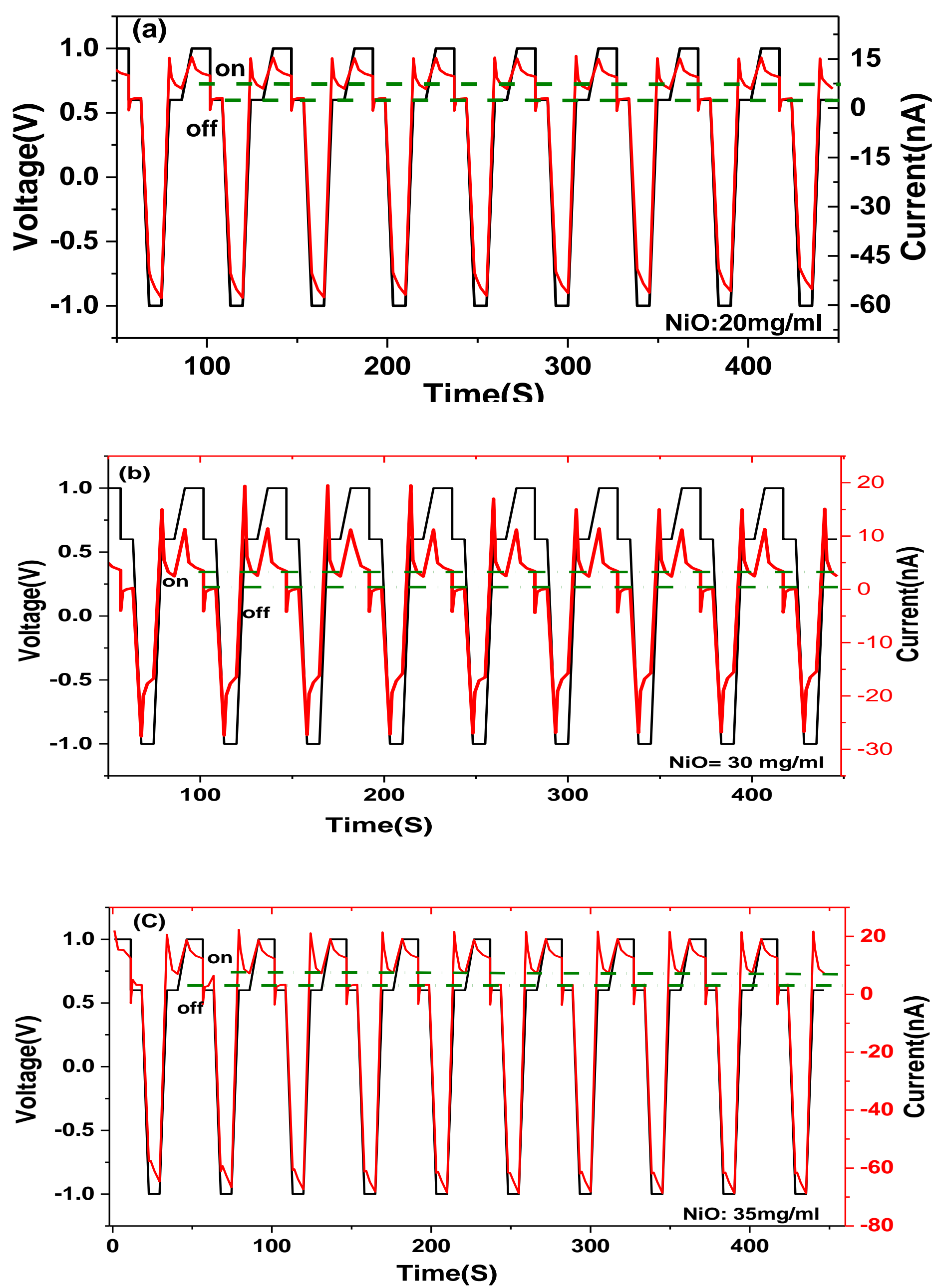


Figure 6.4 WRER pules of Al/PVAc+NiO /Al device, showing applied voltage and the current response (a) 20 mg/ml, (b) 30 mg/ml, (c) 35 mg/ml of NiO.

6.4 Memory Characteristics Nickel Oxide (NiO) (Layered)

I-V measurements were carried out to determine the memory characteristics of layered NiO with the polymer at two different thicknesses of the NiO component layer. Current is measured using negative and positive voltage sweeps, between -4 and +4 V, to reveal if there is hysteresis in the I–V behaviour, as shown in figure 6.5.

Initial I-V measurements were carried out through applying current for negative and positive sweeps. Again, as with the blend composition the results revealed hysteresis (see Figure 6.4). To determine the memory behaviour of the device a maximum voltage is set required for the WRER actions. Figure 6-5 shows the hysteresis that occurred in the MIM structure Al/PVAc/NiO/PVAc/Al.

It is expected that different electrical behaviour will be observed for the different thickness of the NiO layers. The results showed that the thicker layer of the NiO nanoparticles corresponds with a relative increase in the hysteresis (12nm at 0.193nA and 44nm at 0.612nA). This could be explained by the increase in the NiO in that where the oxide (NiO) has a substantial number of traps, or oxygen vacancies, and it is these traps that assist tunnelling which leads to additional conduction [160].

Towards proving longer term performance, the RWER voltage pulse cycles were conducted to verify the memory properties of the two different layered structures, with write and erase voltages of ±3 V and a read voltage of 1V for the two NiO nanoparticle thicknesses in the layered structure. The WRER results are shown in Figure 6.5.

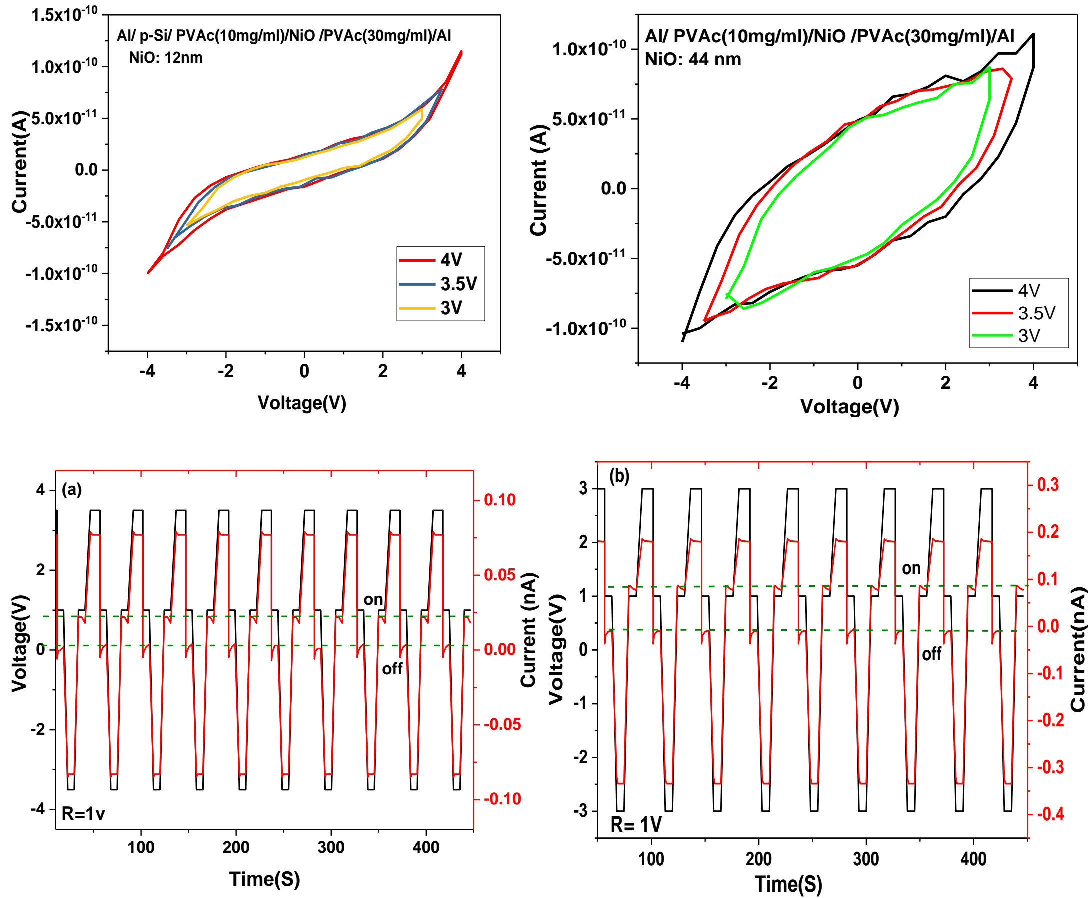


Figure 6.5 I-V Hysteresis for NiO film at 12nm and 44nm. And WRER results for NiO film at (a) 12nm and (b) 44nm.

6.5 Memory Characteristics Barium Titanate ($BaTiO_3$) (Blend)

Typical I–V behaviour of Al–PVAc+ $BaTiO_3$–Al structures are illustrated in figure 6.6 (b). The I-V scan exhibited large hysteresis for negative and positive voltages in comparison to polyvinyl acetate alone. This may be because of the stronger internal electrical field consequence of a larger number of charges in the dipole system. I-V measurements were conducted for the MIM structure in various concentrations of $BaTiO_3$ as seen in (Table 6-2) for the positive and negative voltage sweeps.

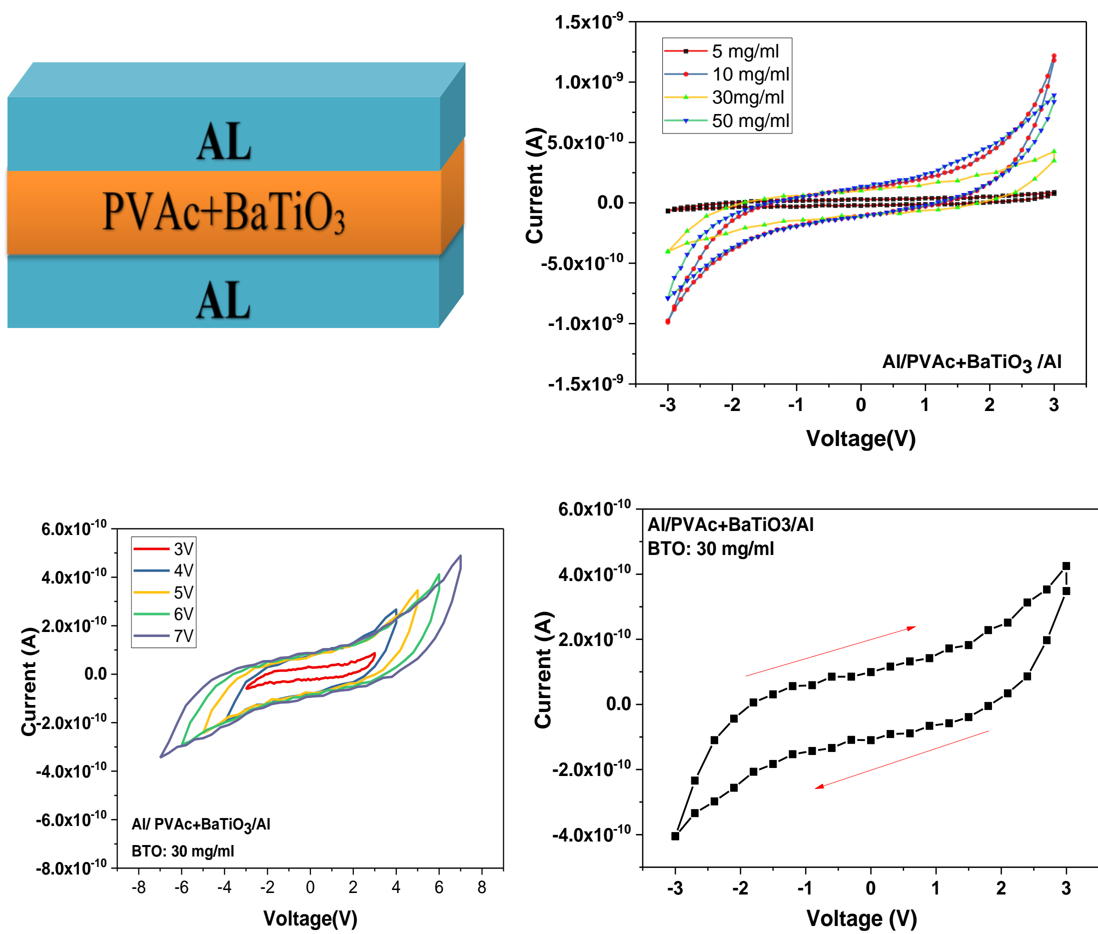


Figure 6.6 (a) MIM structure. (b) current–voltage behaviour: of a sample Al/PVAc +BTO/Al.

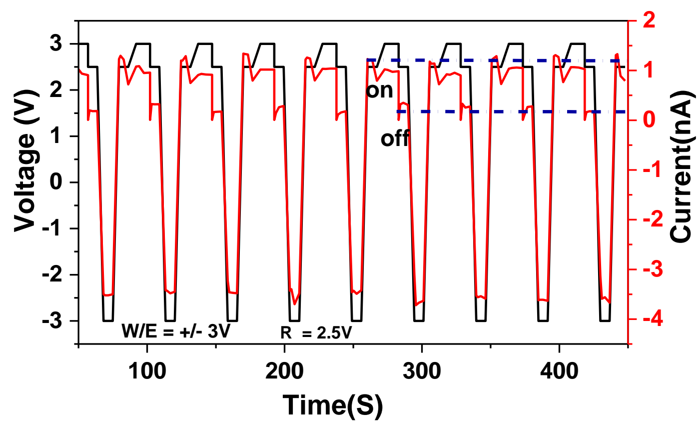


Figure 6.7 RWE characteristics of Al/PVAc+BTO/Al device.

Table 6-2 : Different concentration of $BaTiO_3$ in PVAc.

Sample No.	PVAc (mg/ml)	$BaTiO_3$(mg/ml)
0	10 (control sample)	0
1	10	5
2	10	10
3	10	30
4	10	50

The read-write-erase voltages (RWE) cycles were conducted to reveal properties of these memory structures, using write and erase voltages of ±3 V, and a read voltage 2.5V. The resulting behaviour is shown in Figure 6.7.

It was shown that the ferrorelectrical properties of $BaTiO_3$ was the cause of the hysteresis in the I-V behaviour in the blend composition of $BaTiO_3$ with PVAc. Upon application of the external electrical field there is alignment of the electrical domains that are in the $BaTiO_3$, this alignment is along the electrical field resulting in an internal electrical field in the material. Therefore, the evident switching mechanism is determined by the electrical field.

Therefore, there is a significant possibility that the $BaTiO_3$ nanoparticles are the reason for the observed increase in the I–V hysteresis between the pristine samples that only contained the polymer and the sample with $BaTiO_3$ as a blend.

It was required to determine that the tested materials play an important part in the switching mechanism in the MIM device with a $BaTiO_3$-polymer blend. In order to achieve this endurance studies were conducted, this was achieved through applying Write Read and Erase voltages to the device. When these tests were conducted the voltage was sufficient to create an internal electric field, but not too high as it may cause physical damage to the device.

In reference to the WRER cycles, for the Write voltage where the electrical field is applied the $BaTiO_3$ becomes polarised which in turn leads to an intrinsic electrical field in the material and the formation of dipoles in $BaTiO_3$; we can replace $BaTiO_3$ with electric dipoles. The internal electric field was found to be opposite to the external electric field. Where the Read pulse was applied (2.5 V) the voltage across the device is less than the applied external voltage which reduces conductivity in the device which means that a lower current will pass through the material. For the Erase pulse (-3 V) the orientation of the internal electrical direction changes so that it becomes the same as the external electric field, therefore, there will be an increased Read current. Overall, therefore, the results here have demonstrated the internal working mechanisms that are an explanation of the memory behaviour in terms of I -V of the $BaTiO_3$ / polymer blend, and the results have also proven the difference in polarity between ON and OFF states.

The observed switching behaviour in the present study is observed in materials that have ferroelectric properties, whereby the information storage mechanism is due to the polarisation of these ferroelectric materials. The results of this study have shown the polarising effects on $BaTiO_3$ as a ferroelectric material and how the application of an

external electric field on the memory device can switch this polarisation. The electric field that is a result of the polarising charge is consistent with the $BaTiO_3$ which exhibits I-V hysteresis and resistive switching [137].

Random access memories that use ferroelectric materials also exhibit this behaviour where there is ferroelectric polarisation, and as mentioned in the above where an electric field is applied to ferroelectric materials they show spontaneous polarisation. Therefore, hysteresis can be seen from the I–V characteristics, as well as resistive switching behaviour.

6.6 Memory Characterisation of Barium Titanate ($BaTiO_3$) (Layered)

I-V measurements were conducted to investigate the memory characteristics of $BaTiO_3$ layered with the polymer. In order to reveal hysteresis for the charging mechanism in the I-V curve both negative and positive voltage sweeps, between -1V and +1 V, were applied to the device. As with the other materials that are investigated in this study there is the expectation that electrical behaviour will be observed for the thickness of $BaTiO_3$, however, it is important to note that only one thickness of Barium Titanate was investigated in this work because it was difficult to modify with the evaporation technique used. The resulting hysteresis is shown in Figure 6.8.

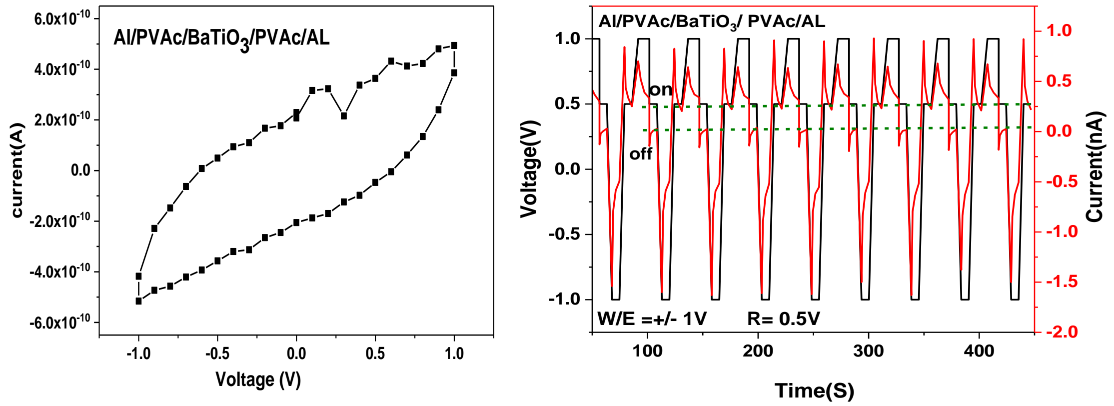


Figure 6.8 current–voltage behaviour: of a sample Al/PVAc/BaTiO3/PVAc/Al and RWE characteristics of a device.

In figure 6.8 the I-V characterisation illustrated that it is possible to achieve bistability with a layered $BaTiO_3$-polymer composition, however, in order to determine the longer-term performance of this type of memory device Read, Write and Erase cycles needed to be conducted. Therefore, to test the memory device programming for the layered composition of $BaTiO_3$ voltage for the required WRER functions was applied to the MIM device. Figure (6.8) illustrates the resulting hysteresis.

For the Write voltage the results of this study suggest that the electrons have tunnelled through the polymer layer and then get trapped in the $BaTio_3$. Upon application of the Read pulse there is a decrease in conductivity across the device, this was also found in the blend composition, and is due to the fact that the current going through the device is less than the external voltage. During the Erase pulse the direction of the internal field changed.

In comparison to the results for the blend compositions, the layered $BaTiO_3$ showed a much lower I–V hysteresis, with the exception of the 5mg/ml, this is because the polarisation already present in the $BaTiO_3$ can affect the working mechanism or performance of the device. In a layered composition internal electric charge trapping which creates hysteresis is greater at the $BaTiO_3$ / polymer interfaces, however, with a blend composition the interfaces between the $BaTiO_3$ and the polymer occur throughout the material, therefore, the insulating effect of the polymer is much more effective leading to increased charge trapping and therefore, greater hysteresis.

6.7 Characterisation of Methylammonium lead bromine (Blend)

I-V measurements were conducted to test the memory characteristics of $MAPbBr_3$ blended with the polymer. Hysteresis was revealed by the application of negative and positive voltage sweeps (-6V and +6V) to the device. The I-V behaviour of the Al–PVAc+$CH_3NH_3PbBr_3$–Al structure is illustrated in Figure 6.9. The results show that a $MAPbBr_3$ blend exhibits a large hysteresis upon application of voltage.

The I-V characteristics have shown the level of bistability as a memory characteristic, another memory characteristic which shows the long-term performance of the memory device the Write, Read, Erase and Read (WRER) cycles. Specifically, WRER cycles were used to investigate the memory properties of the $MAPbBr_3$ – PVAc blend using write and erase voltages of ±6 V and a read voltage of 1V for 5 mg/ml and 3V for 50 mg/ml of $MAPbBr_3$ in PVAc admixture. The WRER characteristics are illustrated in Figure 6.9.

When the external electrical field is applied an alignment of the electrical domains in the MAPbBr3 along the electrical field which creates an internal electrical field which determines the switching mechanism. The tests were conducted with enough voltage to create an internal electric field evidenced by the hysteresis.

These results are consistent with the fact that $MAPbBr_3$ is an organic / inorganic perovskite material which contains defects which migrate when an external electrical field is applied, resulting in I–V hysteresis [151]. Specifically, the hysteresis occurs as a result of the formation of charge trapping which change the resistance from high to low. Where the resistance is high (high resistance state) it results in the OFF state because the charge cannot flow through the material, where the resistance is low (low resistance state) it results in the ON state because it is possible for the charge to flow through the material. Upon application of a negative charge the current decreases and resistance changes from a low to high resistance state. This process is possible because the migration of the ions is dependent on the applied electrical field and the defects in the material. There are a number of different defects in perovskite materials which include interstitials, vacancies, interstitials, cation substitutions and antisite substitutions which all influence switching behaviour [151]. The vacancies that can be found in $CH_3NH_3PbBr_3$ include CH_3NH_3 vacancies, lead vacancies and bromide vacancies and they have a relatively low formation energy [151].

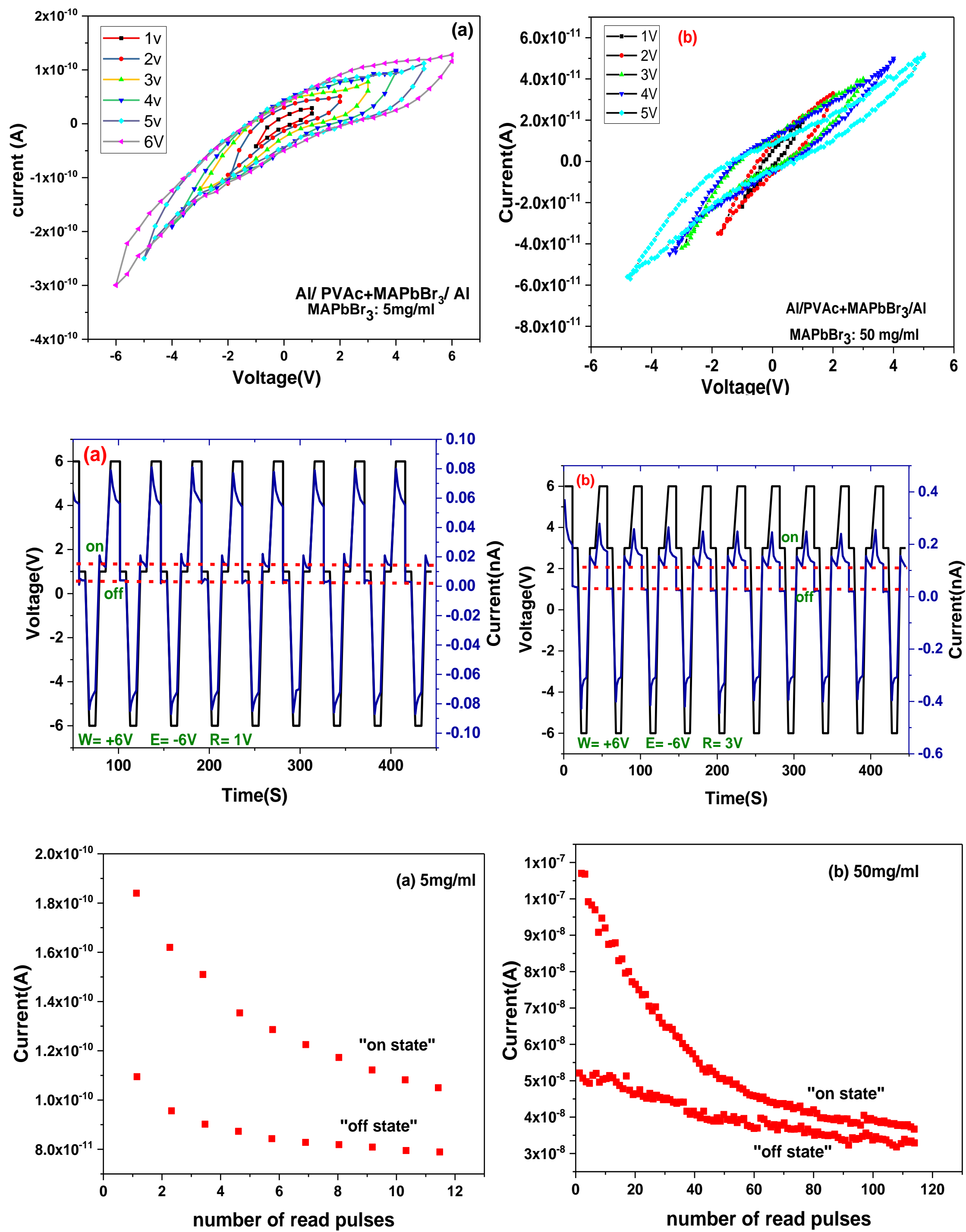


Figure 6.9 Current–Voltage behaviour: of a sample Al/PVAc+MAPbBr/Al, RWE and retention time characteristics of a device contain (a) 5mg/ml and (b)50 mg/ml respectively.

The charging mechanism of the perovskite material takes place during HRS, whereas the charge trapping takes place during LRS. Therefore, it is the atomic defects in the perovskite material which are the trap sites. When a positive voltage is applied the I–V curves at the HRS state have two linear regions which are ohmic conduction at a low voltage and a quadratic region at a high voltage [151].

Overall therefore, hysteresis in $MAPbBr_3$ as a perovskite material is because of ion migration or because of charge trapping, and the switching mechanism explained by charge trapping and defect migrations where an electrical field is applied [151]. Figures 6-9 (WRER) show that the switching process from cycle to cycle is reproducible.

6.8 MAPbBr - single crystal structure

In the previous experiments $MPbBr_3$ was blended with a polymer and part of the process was to crush the $MAPbBr_3$ when it was in a crystallised bulk form to reduce it to a powder which removed its crystalline properties, and as the results have suggested the resulting blend showed charge trapping in the device. Furthermore, it has been speculated that the charge trapping could be attributed to ferroelectric properties which creates electric dipoles or attributed defects in the materials which creates vacancies.

Organic-inorganic lead halide perovskites have been used in other applications including optoelectronics [200] not only for use in thin films, but also as a single crystal preparation which improves performance in terms of efficiency and also allows better understanding of the material's intrinsic properties [200]. The reason this is possible is because the single

crystal structure does not have any grain boundary, unlike solution-processed films which often have many grain boundaries and defects [200].

Towards further understanding this material in terms of its memory properties it is tested as a bulk material in its single crystal form. The reason that it was tested in the crystal form is because the crystals are facing in one direction in a uniform way which means that the applied charge will pass through the material easily. This is as opposed to the powdered form when mixed with a polymer whereby the charge has to jump because the crystal facets are facing different directions and the aforementioned grain boundaries and defects.

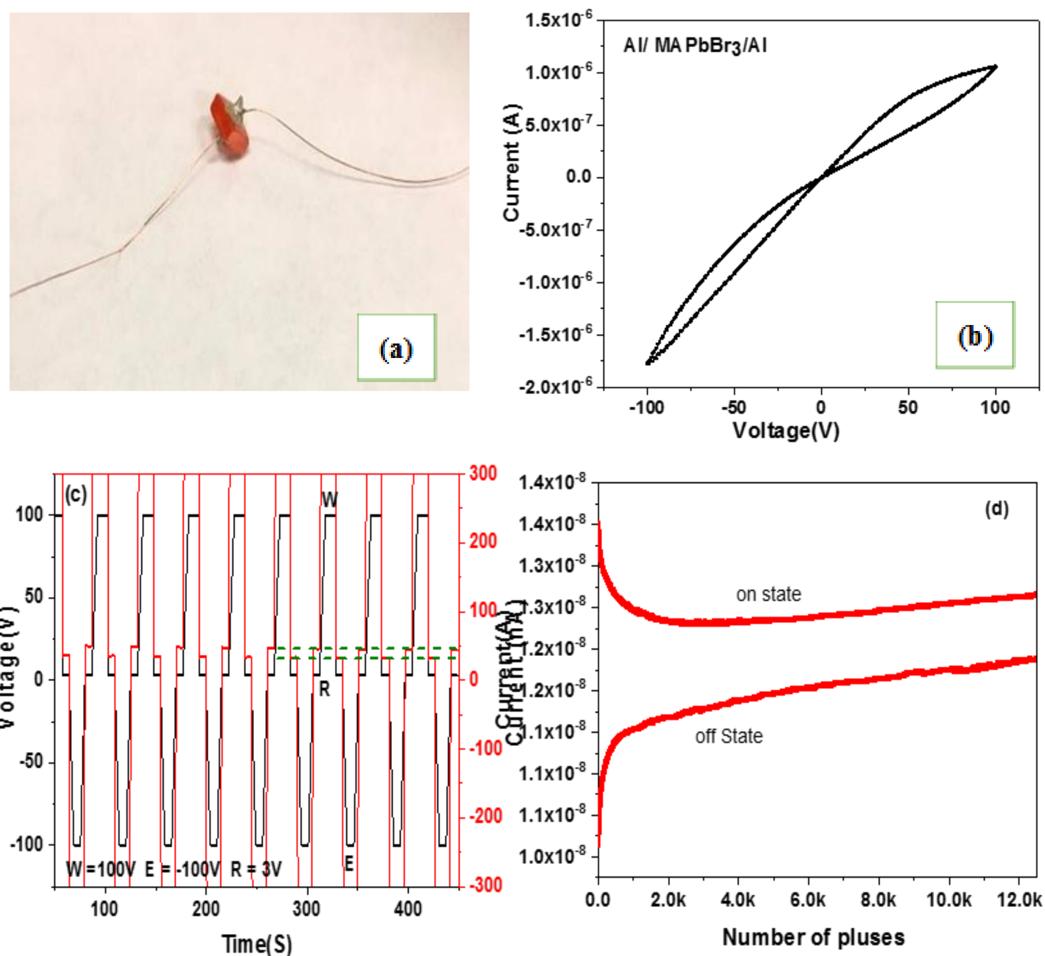


Figure 6.10 Present of (a) Picture of Al/MAPbBr$_3$/Al device structure as single crystal and (b) current–voltage behaviour of Al/MAPbBr$_3$/Al, (c) RWE characteristics and (d) retention time the same devices.

Importantly, the results of the blend composition have showed hysteresis, however, this may not be due to the active material, it may be due to grain boundaries, dangling bonds, surface states and defects which become sites for charge trapping. Therefore, in order to test the material to see if it is not these factors that are causing retention, the material needs to be tested in a way where these factors are not present. This was achieved through

testing $MAPbBr_3$ in a single crystal form whereby any charge trapping would not be due to defects and because there are no grain boundaries.

Current – voltage (IV) measurements were conducted to show memory function to test the memory characteristics of $MAPbBr_3$ as a single crystal structure. Hysteresis was shown through the application of negative and positive voltage sweeps (-100V and +100V). The I-V behaviour of the Al– $MAPbBr_3$ –Al structure is illustrated in Figure 6.10 (b). The results indicate that $MAPbBr_3$ single crystal structure exhibited a large hysteresis when negative and positive voltages are applied, specifically, 172.2 nA.

Because the results of the testing showed hysteresis which indicated that there was retention, and because this was not due to the aforementioned factors, there has to be another reason for the observed results. One possible explanation for the charge retention is the ferroelectric properties of the $MAPbBr_3$ single crystal.

Other possible explanations for the observed charge retention include Schottky junction and trapping at the location near the contacts. In order to verify these two possibilities CV measurements were conducted on the single crystal $MAPbBr_3$ the result of the CV measurement showed a straight line (see Figure 6.11) which is an indication that there was no interface trapped charges and no Schottky junction, which is a further indication that it is the ferroelectric properties that caused the hysteresis, however, this would require further research to establish the exact reason.

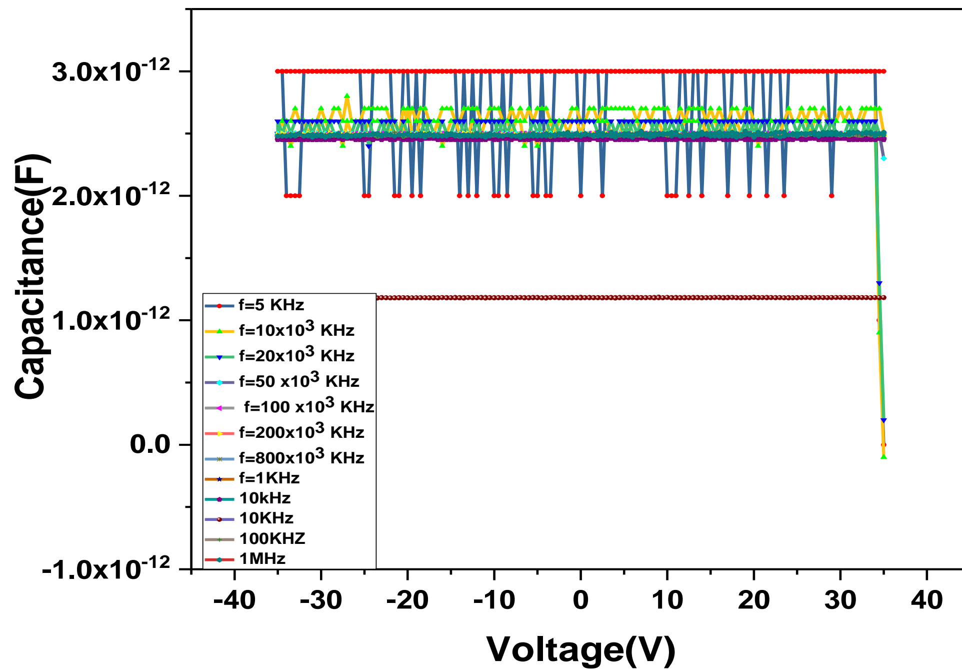


Figure 6.11 C-V measurement at different Frequency.

Towards further possible explanation it is necessary to note that the hysteresis curve was a distinctive shape where the current passes through the origin (see Figure 6.10) where the voltage is 0. Therefore, it is a possibility that this distinctive hysteresis shape is a result of the crystal being in the ferroelectric state when the voltage is applied, this is evident in the I-V curve where it corresponds with the applied sweeping voltage (see Figure 6.10 (b).

The I-V characteristics have revealed bistability in the device, however, long-term memory performance also needed to be tested through conducting Write, Read, Erase and Read cycles. The WRER cycles were carried out with write and erase voltages of ±100 V respectively and a read voltage of 3 V. The WRER characteristics are shown in Figure

6.10 (c). The device switched between two resistive states, when a write pulse of 100 V was applied and read pulse of at 3 V was applied, a high resistive state (HRS) was recorded and when the erase voltage was applied at -100 V and again read at 3V, the device switched to a lower resistive state (LRS).

Another attribute of memory function is for how long the device can retain the information which was determined using data retention time measurements where two states are monitored over time. A read voltage of + 1 V was used after the application of write and erase voltages of ± 100 V. Once writing the memory device had been performed, the ON state was observed and after the erase process, the OFF was observed with a different current value. The current value difference 0.83 nA.

For all of the memory functions that have been tested and presented in this section, the results have been consistent for all of the five tested devices (Al- $MAPbBr_3$-Al) with the single crystal $MAPbBr_3$ structure (see Appendix 3).

6.9 Verification of Mechanism Principles

Paul (2007) introduces a model that shows how the behaviour of the 2TNV is a result of the internal electrical field that is created when voltage is applied to the memory device. The working principle of the proposed 2TNV memory device using a NiO – Polymer blend is based on Paul's (2007) model. Specifically, the results of the experiments here show that there is a verification of the principle determined by Paul (2007) which represents what happens within the memory device in terms of electrical field and the resulting polarisation.

An attribute of the memory effect is the charging ability of the NiO nanoparticles. The model below illustrates how the internal electric field is created and how it is exploited to achieve bistability for electrical conductivity. Both the electrical bistability and the reliability of the memory device using NiO – Polymer blend have been tested in this section. Towards verifying the approach by Paul (2007) the specificities of what takes place within the tested memory device in relation to interplay between the external electrical field for the W R E R processes and the associated internal electrical field, is relevant here.

Because of the formation of a negative internal electrical field during the read process, the voltage across the memory device is less than the voltage that was applied. The negative current shows that it is both higher and in an opposite direction. Low conductivity could represent the state ‘0’ of a memory bit. During the erase process where the same voltage is applied, however, in the opposite direction, the electrons will leave the NiO nanoparticles. Where the read process is conducted again following the erase process, the direction changes where a high current state is observed, illustrated in Figure 6.12.

Therefore, the results show that an electrical field is formed when the NiO nanoparticles are charged, and it is the direction of the internal field that can oppose or augment the external electric field, as indicated by the electrical bistability and the I- V hysteresis. This principle was also found to be true for the other two materials as illustrated in Figure 6.12.

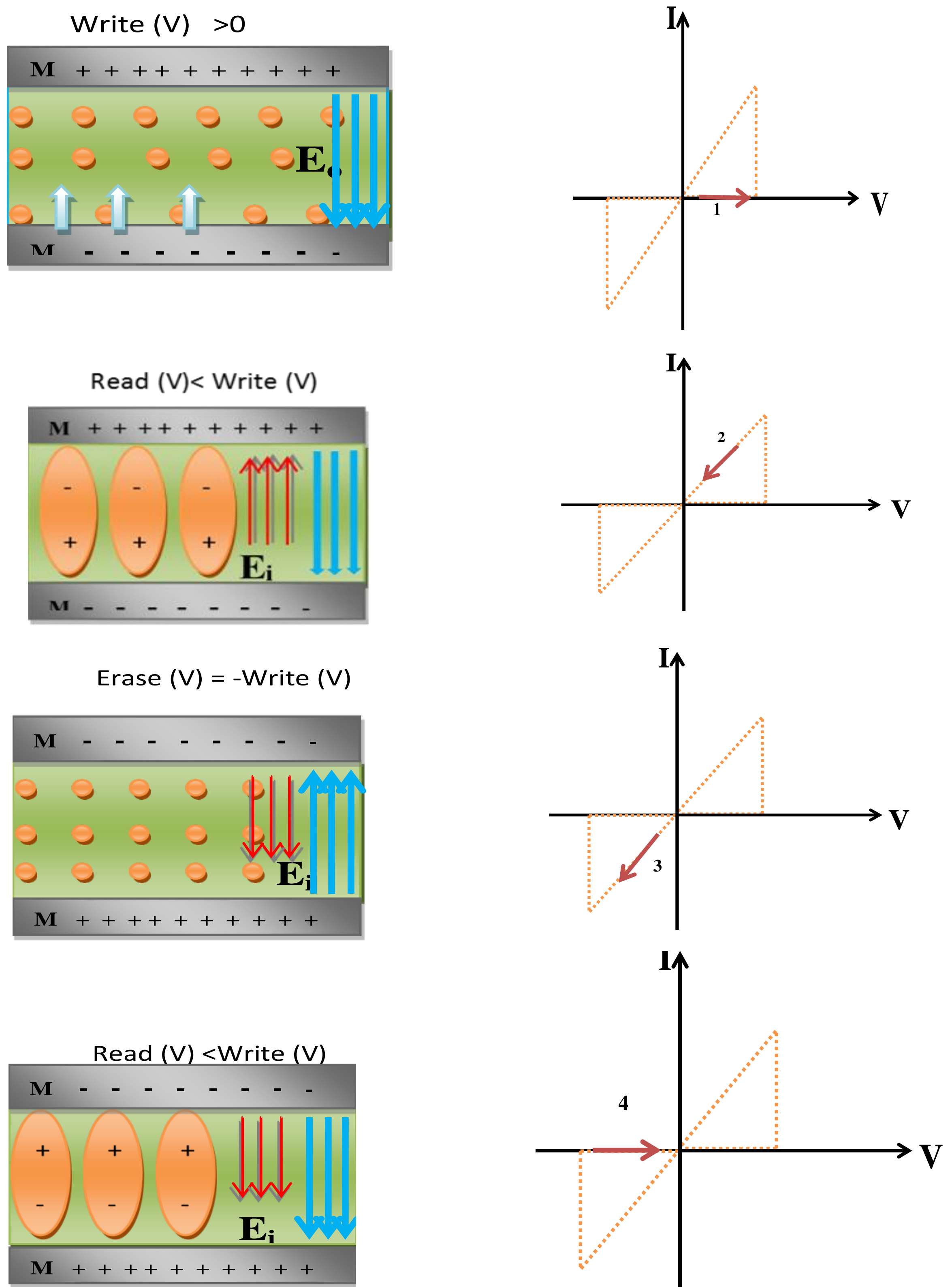


Figure 6.12 Schematic demonstration of working internal mechanism of 2TNV memory device for WRER processes based on blend of NiO with PVAc.

Further support for the internal mechanism that has been proposed by Paul (2007) is that the results from barium titanate WRER pulses show the same internal switching behaviour as NiO. When the write voltage is applied this created a dipole in the polymer matrix, this will create an internal electrical field. The read pulse which is less than the write voltage will affect the voltage across the device which will in turn decrease the conductivity and thus, the current in the device becomes lower. The polarity of the active material is in the opposite direction to the external polarity. The flow of current is in the expected direction from the external negative to positive polarity and the internal resistance is in the opposite direction. Upon application of the erase pulse switching takes place whereby the external polarity, the polarity of the active material, the direction of current flow and the direction of resistance all switch to the opposite direction (see Figure 6.13). When the read pulse is applied it is a high voltage and the direction of the current changes to the same direction of the resistance (see Figure 6.13), which creates the difference between the on and off states. This same switching phenomenon was observed by Paul (2007).

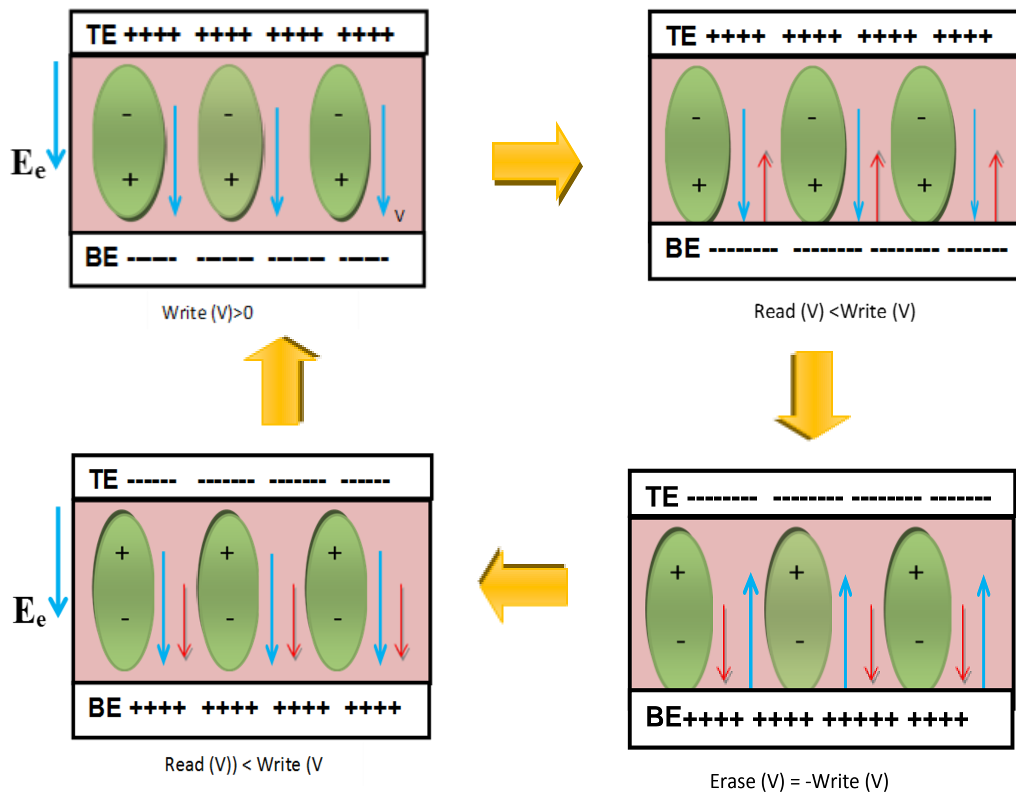


Figure 6.13 Schematic demonstration of working internal mechanism of 2TNV memory device for WRER processes based on blend of perovskite material with PVAc.

6.10 Summary.

Table 6-3 : Summary of result

Device / material composition	Area enclosed in I-V hysteresis (nAV)	Difference between on /off state
PVAc (control sample)	**0.123**	
NiO Blend (Al/PVAc+NiO/Al)		
5 mg/ml	**3.28**	**1.32 nA**
10 mg/ml	**1.83**	**1.95 nA**
20 mg/ml	**9.37**	**2.43nA**
25 mg/ml	**9.77**	**3.23nA**
30 mg/ml	**10.95**	**4.174nA**
35 mg/ml	**14.01**	**5.399nA**
NiO Layered Al/PVAc/NiO/PVAc/Al		
12nm	**0.193**	**0.016 nA**
44nm	**0.612**	**0.052 nA**
$BaTiO_3$ Blend Al/PVAc+$BaTiO_3$/Al		
5 mg/ml	**0.251**	**0.0166 nA**
10 mg/ml	**1.275**	**0.073 nA**
30mg/ml	**1.1755**	**0.6818 nA**
50 mg/ml	**1.491**	**0.2069 nA**
$BaTiO_3$ Layered: Al/PVAc/$BaTiO_3$/PVAc /Al		
10nm	**0.743**	**0.255 nA**
MAPbBr Blend Al/PVAc+MAPbBr/Al		
5 mg/ml	**0.9044**	**0.109nA**
50mg/ml	**1.3402**	**0.097nA**

As part of the electrical characterisation of the MIM structure experiments were conducted to determine the charging mechanism and memory device programming. The results of the experiment are presented in table 6-3.

The charging mechanism of NiO in various concentrations blended with PVAc was tested using I-V hysteresis. The results revealed that generally as the NiO concentrations increased it resulted in a higher hysteresis. However, it is important to note that there were exceptions. The lowest concentration of NiO at 5mg/ml resulted in a much higher hysteresis (3.28nA) than 10mg/ml of NiO at only 1.83nA. Between 20 and 25mg/ml of NiO the increase in the area of hysteresis was marginal, from 9.37nA to 9.77nA, but where there was a significant increase in hysteresis was between 30 and 35mg/ml where the hysteresis increased from 10.95nA to 14.01nA (see table 6-3). Therefore, the results reveal that an increased concentration of NiO is better for the charging mechanism as a function of memory, however, only for concentrations of NiO of 20mg/ml and above.

The layered composition of NiO and PVA was also tested for charging mechanism using I-V hysteresis, two different thicknesses of the NiO layer were tested: 12nm and 44nm. There was a significant increase in the area of the hysteresis where it was 0.193nA and 0.612nA for 12nm and 44nm of NiO respectively. Therefore, an increase in the amount of NiO also has a positive effect on the charging mechanism, however, in comparison to the blend the charging mechanism was much less evidence by a much lower hysteresis. The possible reasons for this may include that it is much more difficult for the voltage to pass from one layer to another as the electron would have to tunnel its way through these

layers, this is a factor of performance, however, deterioration in the material could have been another contributing factor.

The memory device programming for NiO was tested using WRER voltage sweeps. For the blend composition concentrations of 25, 30 and 35 mg/ml of NiO were tested. The results showed that an increase in the concentration of NiO led to an increase in the efficiency of memory device (see Table 6-3). Where the material was tested as a layered composition there was much less efficiency in terms of memory device programming, moreover, an increase in the thickness of the layer did result in a marginal increase in memory device programming efficiency.

Barium titanate ($BaTiO_3$) was also tested for charging mechanism using I-V hysteresis measurements. Although different concentrations of $BaTiO_3$ were used compared to NiO, there was still a corresponding increase between an increase in concentration and an increase in I-V hysteresis, however, in comparison to NiO the hysteresis was much less. Even where there was a much larger concentration of $BaTiO_3$ (50mg/ml) it only resulted in a hysteresis of 1.491nA (see Table 6-3). $BaTiO_3$ as a layered composition was only measured for one thickness (10nm), however, the resulting hysteresis was greater than the 12nm and 44nm thicknesses for NiO.

Therefore, the results discussed until now show that NiO as a blend is more effective for the charging mechanism than $BaTiO_3$ as a blend, but $BaTiO_3$ as a layered composition is much more effective. This pattern was also found to be the case for the memory device programming whereby $BaTiO_3$ was less effective than NiO for the blend compositions,

but more effective in a layered composition. This finding was expected because charging mechanism and memory device programming.

Methylammonium lead bromide was tested only as a blend composition, specifically, 5mg/ml and 50 mg/ml compositions. The findings also revealed that an increase in the concentration of $MAPbBr_3$ lead to an increase in the efficiency of the charging mechanism, however, much like $BaTiO_3$ the effect of increasing concentrations was very low in comparison to NiO which had a much greater effect.

The efficiency of memory device programming for $MAPbBr_3$ was found to be much less effective than both NiO and $BaTiO_3$ and it is important to note that the latter two materials were tested as nanoparticles. Therefore, the results of this study show that nanoparticles are much more effective for memory.

The RWER cycles over a 10-cycle period showed an off/on current of ~10. The results of the experimentation showed that this was typical for all the materials as a blend with on and off states.

Chapter 7 MIS Structure for Capacitance Measurement

7.1 Introduction

Capacitance-voltage measurements are conducted an MIS structure as a capacitor. In order to measure capacitance which is an indication of how much charge can retained by the devices. Moreover, capacitance-voltage measurements are conducted on the MIS structure in order to determine charge retention and durability. In this chapter, these capacitance capabilities are tested for each of the three materials as a blend and layered structures with PVAc. The results from these two experiments for capacitance and charge retention using C–V measurements will serve to further verify the electrical bistability that was established using I–V measurements in the previous chapter.

7.2 Nickel Oxide (NiO) (Blend)

CV measurements for capacitance were conducted to determine the ability of the tested material in terms of the amount of charge it can accept. This was conducted using the MIS device structure described in the above in section 5.4.1 in chapter 5. Specifically, this structure is comprised of a Metal Insulator Semi-conductor whereby the material that is being tested, whether as a blend or layered, is placed onto a p-type silicon substrate with an ohmic back contact.

The C-V curves of MIS capacitors elucidate the memory programming behaviour from the charge that is stored in the memory device. This memory programming behaviour is

also estimated by the C-V hysteresis area. The width of the hysteresis changes when there is an increase in concentration of the NiO nanoparticle, which is an indication of the amount of charge that is stored (see Figure 7.1). Because NiO is a binary transition metal oxides material there is the presence of oxide charge which can negatively affect the performance of the memory device in terms of C-V capacitance. Because the oxide charge is independent of the gate bias, it is possible to study the effect of oxide charge by conducting C-V analysis of MIS capacitors. Positive and negative oxide charges have an effect on the C-V curve, the shift in the curve is defined as V_{FB} and the relationship between this shift and the density of the oxide charge is defined in the following equation:

$$V_{FB} = - \frac{Q}{c_0 x} \qquad (7\text{-}1)$$

For the MIS structure, a NiO / polymer blend where either a positive or negative charge (indicated as Q) is within the oxide a shift in the C-V curve along the voltage axis is obtainable.

Capacitance measurements were conducted considered as a function of voltage or frequency. To make sure the capacitance measurement was precise an MIS device structure that did not contain NiO was compared to the MIS device with the polymer-NiO blend.

In order to determine the defect states of the capacitors as an MIS structure, Capacitance-Voltage (C-V) sweeps were performed at room temperature. The response time of the trap states are determined by the frequency of the AC signal that is used in the C-V measurement. The area enclosed by the hysteresis is observed to increase with a

corresponding increase in NiO concentration in PVAc as show in Figure 7.1(c). This further clarifies the role of NiO in the behaviour of the device.

Charge retention and durability are used to confirm the reliability of a memory device in terms of how long the material can retain charge as an attribute of memory function. Capacitors were used with admixtures comprising of PVAc 10 mg/ml with various concentrations of NiO nanoparticles, shown in Figure7.2 (5, 10, 20, 25, 30, 35 mg/ml). Stability and charge retention tests were performed on MIS capacitors as devices that have comparable designs to 2TNV memory devices including charge injection and trapping. In this device, the stability test for ten thousand (10,000) cycles at two conductivity states were performed to assess the long-term retention capability of the memory devices consisting NiO nanoparticle at the aforementioned concentrations.

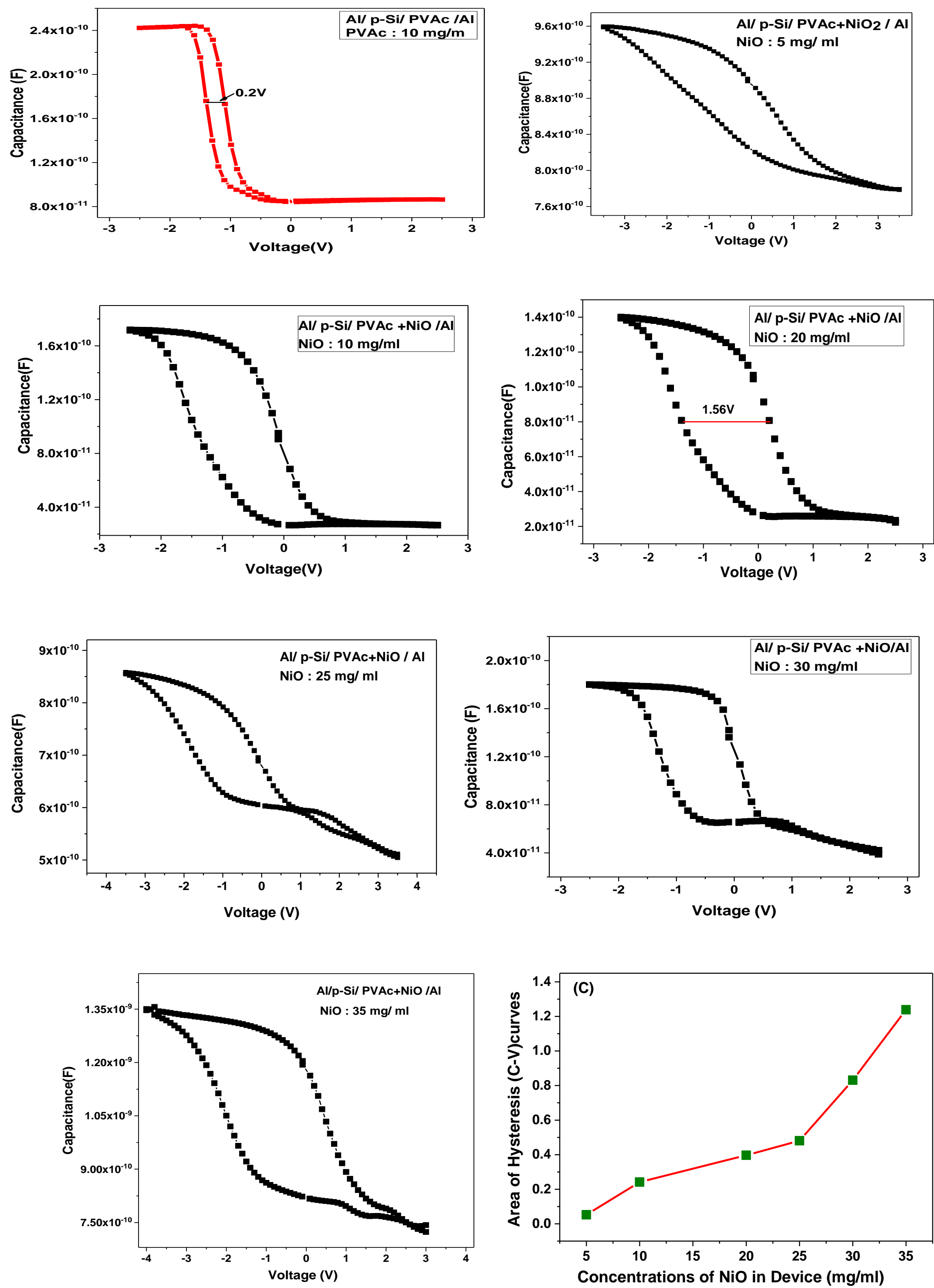


Figure 7.1 Capacitance-Voltage curves for (a) Control sample-PVAc only, (b) Devices with different concentrations of NiO in PVAc (c) Area enclose of C-V curve at different concentrations of NiO in blend.

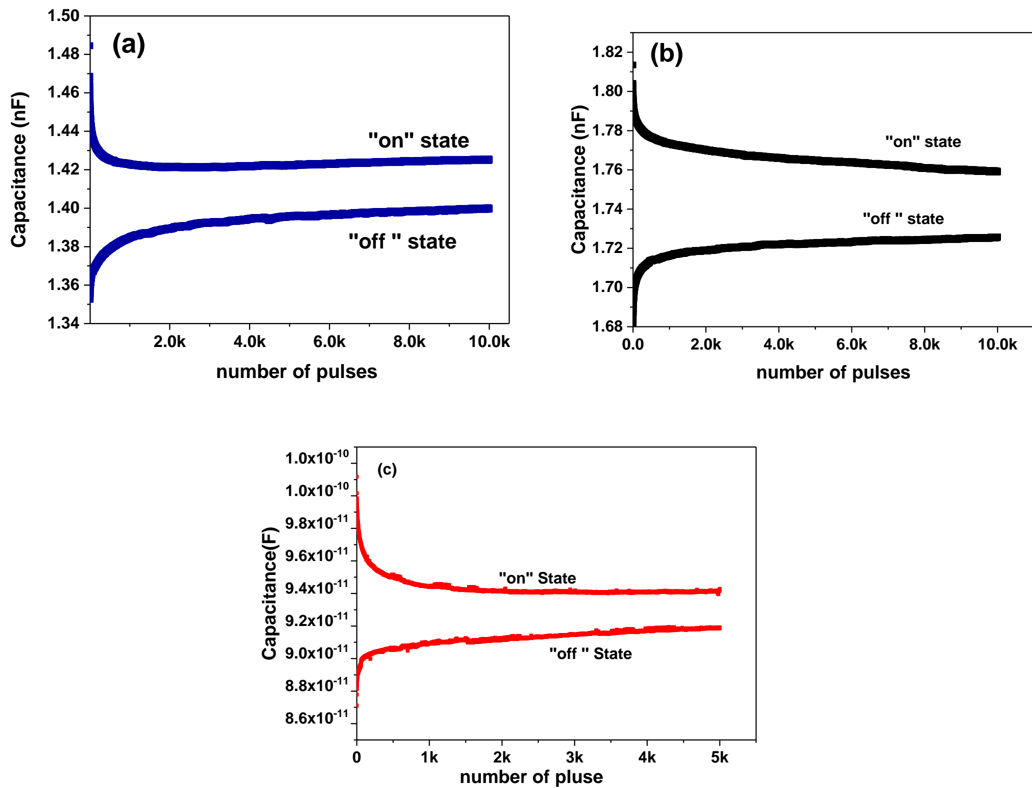


Figure 7.2 Retention time of P-Si/ PVAc+NiO/AL; NiO: (a) 5 mgml^{-1}, (b) 20 mgml^{-1} and (c) 30 mgml^{-1}; PVAc: 10mgml^{-1}

7.3 Nickel Oxide (NiO) (Layered)

C-V curves of MIS capacitors was used to determine the charging behaviour. The charge stored in the device is estimated by the C-V hysteresis area and the difference in the hysteresis width according to the two different thicknesses of NiO nanoparticle layers, is an indication that the amount of charge stored, as shown in Figure 7.3.

As a function of voltage or frequency, capacitance measurements were conducted, and to ensure the capacitance measurement was precise a MIS device that did not contain NiO was compared to the MIS device with the NiO – PVAc layers.

The defect state of the MIS devices as capacitors was measured by conducting Capacitance-Voltage (C-V) sweeps at room temperature. The frequency of the AC signal determined the response time of the trap states.

The area enclosed by the hysteresis is observed to increase with increase in the thickness of the NiO layer (Figure 7.3). This is a clear indication of the role of NiO in the behaviour of the 2TNV memory device.

The amount of time that information can be retained is an important factor of memory. In light of this, this study conducts data retention time measurements, which involved the monitoring of two states over a period of time. Charge retention and durability are measurements of reliability. As with C-V capacitance measurement, capacitors were also used with two samples of NiO – PVAc layers at two different thicknesses of NiO, namely 12nm and 44nm. Stability and charge retention tests were conducted on MIS capacitors because they have a design that is comparable to that of 2TNV memory devices,

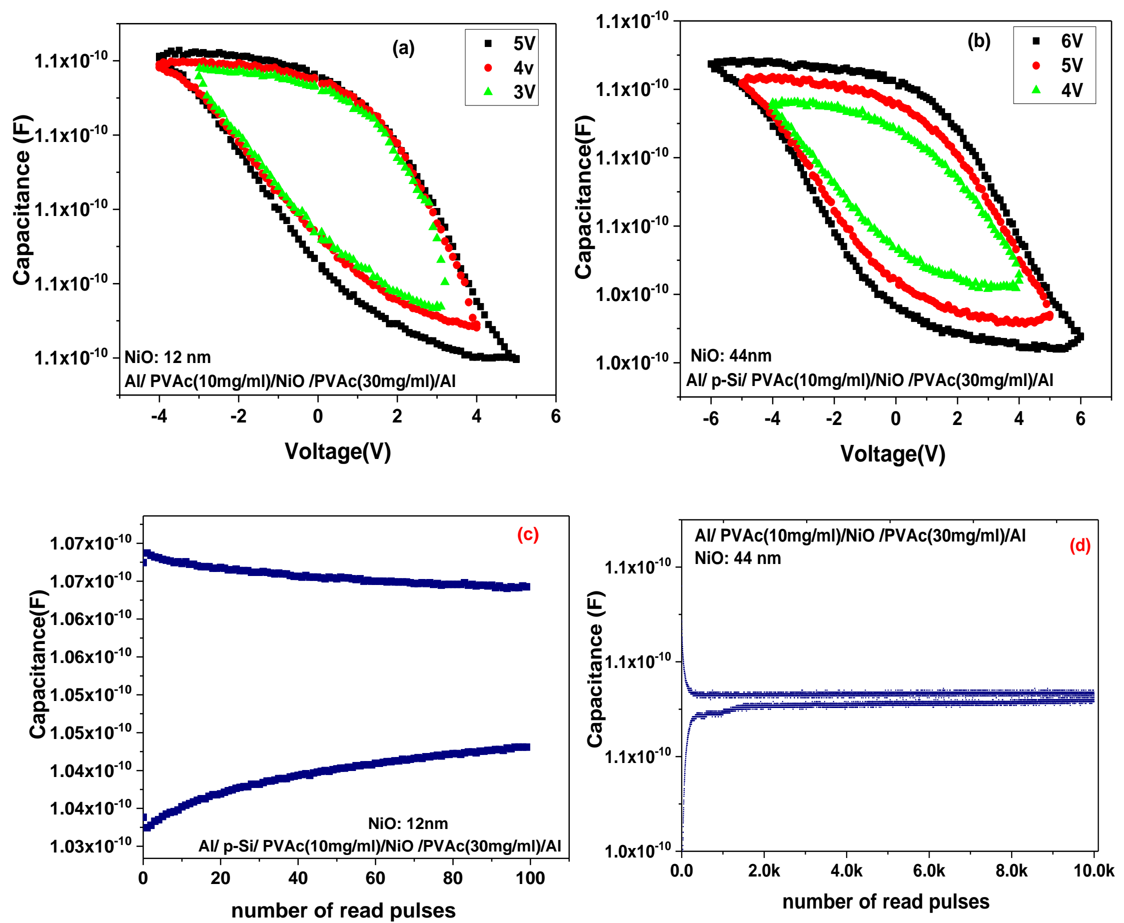


Figure 7.3 C–V Characterisation for NiO at (a) 12nm and (b) 44nm. And Charge endurance time for NiO at (c) 12nm and (d) 44nm.

especially charge injection and trapping function. A stability test for ten thousand (10,000) cycles at two conductivity states were conducted in order to determine the long-term retention capability of the memory devices comprising the layered structure of two different thicknesses of NiO (see Figure 7.3).

Figure 7.3 (b) shows the retention time, represented as capacitance over a period of time, for the NiO – polymer layered structures at two different thicknesses. A read voltage of-0.5V was used based on a write and erase voltage of ±6V of 12nm of NiO and ±5 V44

nm of NiO The ON state was observed then after erase the OFF state was observed for the different value between the two (see Figure 7.3).

The results showed that with the 12nm layer of NiO there is a higher level of capacitance, however, the retention was only for 10000 pulses after which there was a rapid deterioration in capacitance. Additional testing revealed that this was this is a result of damage resulting from prolonged application of the electric field. In contrast, the results from the 44nm layer of NiO showed a much lower capacitance, however, for a much longer retention time (see Figure 7.3).

7.4 Barium Titanate (BaTiO3) (Blend)

Barium Titanate as a blend with the polymer was investigated for capacitance using capacitance voltage and charge retention and durability, using the MIS structure. C-V scans were conducted through applying a sweeping voltage between -6V to +6V in order to determine the area enclosed within the C-V hysteresis. For the C-V capacitance measurements the MIS device with a BTO – PVAc blend resulting in a threshold voltage of 3.5V which is an indication of the switching behaviour using these devices

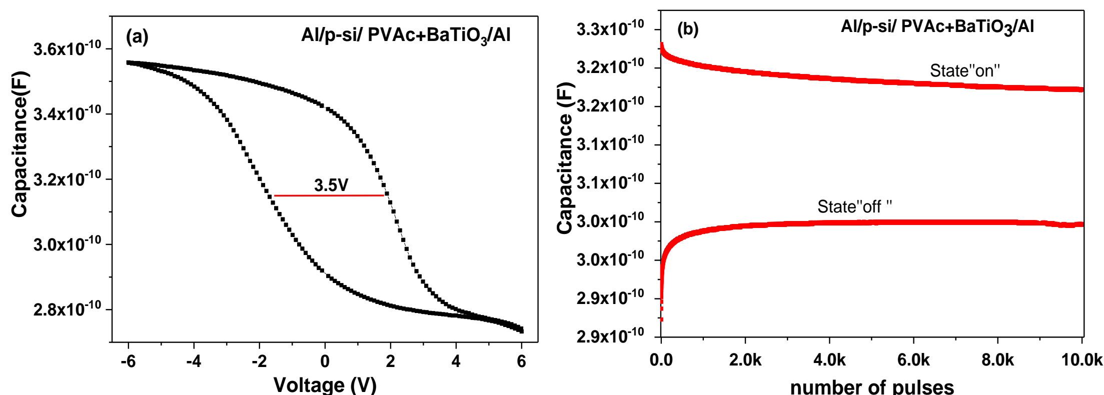


Figure 7.4 (a) C-V curves of MIS Structure (Al/p-Si/ PVAc+BaTiO3 /Al). (b) Retention time variation at ("off") and erased ("on'') state of devices

In order to find out the charge retention time, the electrical switching behaviour over a period of time using high (0) and (1) conductivity was carried out. The results show that for the device P-Si/PVAc+$BaTiO_3$/AL the difference between the high and low states was approximately 0.62 n F (see Figure 7.4(b)).

Furthermore, stability tests were conducted on the MIS device containing the admixture of PVAc with 30mg/ml of $BaTiO_3$. These tests were conducted at two conductivity states for 10000 reading pulses, the results show that the electronic memory device showed consistent performance.

7.5 Barium Titanate (BaTiO3) (Layered)

C-V curves were used to determine the memory programming behaviour of Barium Titanate layered with the PVAc. Again, the area within the C- V hysteresis curve was an indication of the charge stored in the memory device. Capacitance-voltage (C-V) sweeps were carried out at room temperature. The results showed that an area within the

hysteresis curve was observed, this was an indication of the role of $BaTiO_3$ in the memory device (see Figure 7.5 (a))

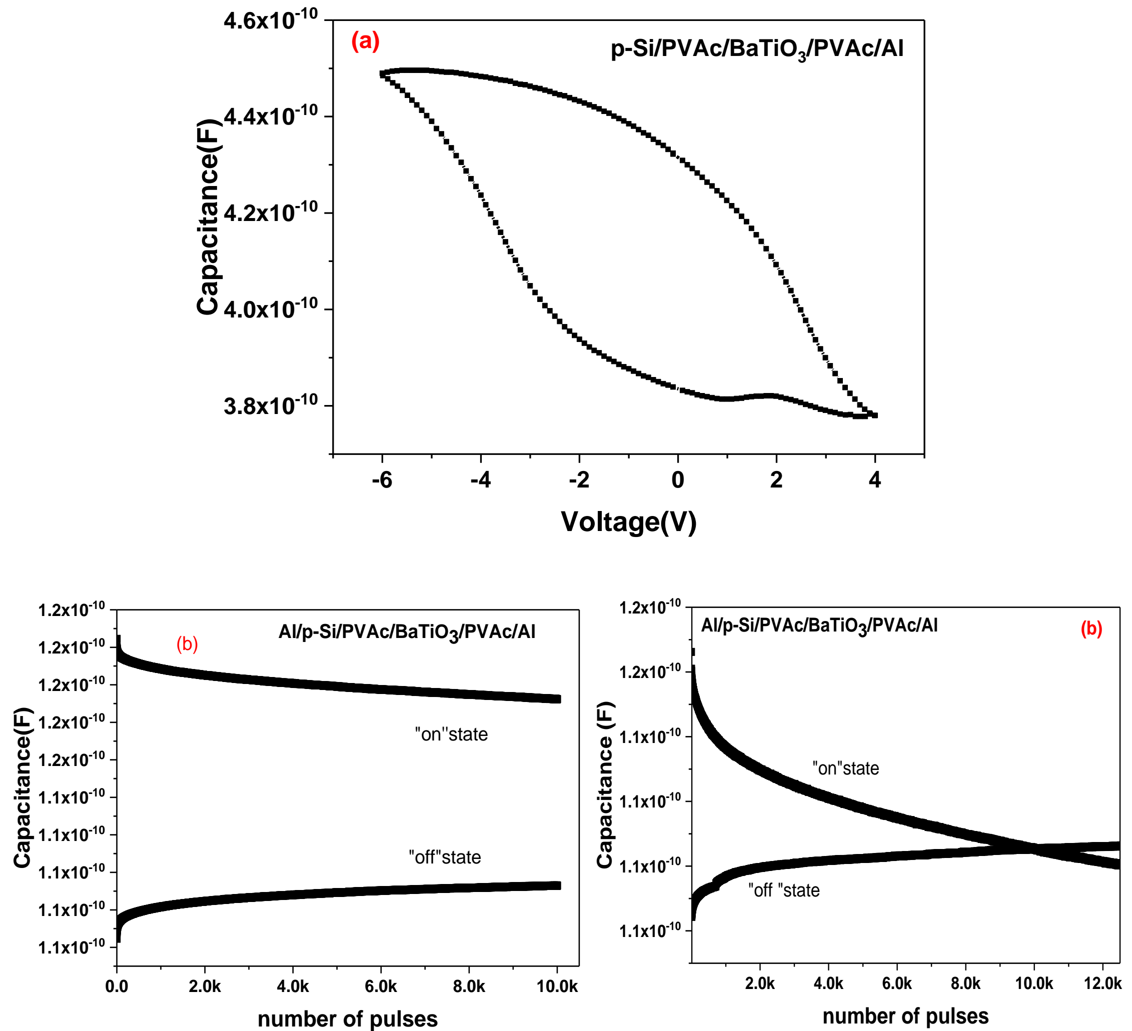


Figure 7.5 Electrical characteristics of devices Al-PSi/PVAc/BaTiO3 /PAVc/Al, (a) C-V hysteresis (b) retention time and stability over multiple cycles of the MIS capacitor.

As a factor of memory, the amount of time that charge can be retained was tested using retention time measurements, again through monitoring the high (0) and low (1) states for a certain period of time for a number of pulses. For the Barium Titanate layered with

PVAc only one thickness of Barium Titanate was used due to practical difficulties in achieving another thickness.

A stability test using 10,000 pulses at the two conductivity states was conducted in order to determine the long-term retention capability. Figure 7.5(b) shows the retention time, represented as capacitance over a period of time, for the $BaTiO_3$ – polymer layered structure.

Where nanoparticles are used in MIS capacitors the results have showed there is hysteresis exhibited in the capacitance-voltage characteristics, this is in contrast to devices where nanoparticles are not used [177]. An explanation for this hysteresis is that electrons from the electrode are injected into the nanoparticles which causes them to become charged which allows data to be stored.

The hysteresis that was exhibited in the results here in the C–V behaviour is an indication of the dipole rotation in the ferroelectric material, specifically, the crystalline domains upon application of an opposite polarity [75]. A contributing factor to the capacitance of the nanoparticles materials is that the polymer does not play a role in the electronic transition because it is an inert matrix the $BaTiO_3$ and NiO nanoparticles [120].

7.6 Methylammonium lead bromine (Blend).

CV measurements for capacitance were conducted to determine the ability of $MAPbBr_3$ to accept charge. In chapter six it was revealed that charge retention could possibly be due to the ferroelectric properties of $MAPbBr_3$. Again, the MIS structure as a capacitor

was used. The C-V curves of MIS capacitors reveals the memory programming behaviour where the charge stored in the MIS device which contains the $MAPbBr_3$ as a blend.

The differences in the widths of the C-V hysteresis was tested for two different concentrations of $MAPbBr_3$: 5mg/ml and 50mg/ml. This was achieved through the application of sweeping charge between +1V to -3V. The results showed that there were differences in the area with the hysteresis C-V curve for the different concentrations of $MAPbBr_3$. For the 5mg/ml concentration the enclosed area between +1V to -3V was 0.0641659 nF and for 50mg/ml the width was 0.15259715 nF. Therefore, an increase in the concentration of $MAPbBr_3$ leads to an increase in capacitance.

Write Read Erase Read (WRER) cycles were conducted for the MIS structure containing the $MAPbBr_3$ – Polymer blend to further determine capacitance (see Figure 7.6 (b)).

The charge retention over time as a factor of MIS was tested using high (0) and low (1) states for a certain period of time for 10,000 pulses. This was conducted for both 5mg/ml and 50mg/ml concentration of $MAPbBr_3$ Figure7.6(c) shows the retention time, shown as capacitance over a period of time for a number of pulses.

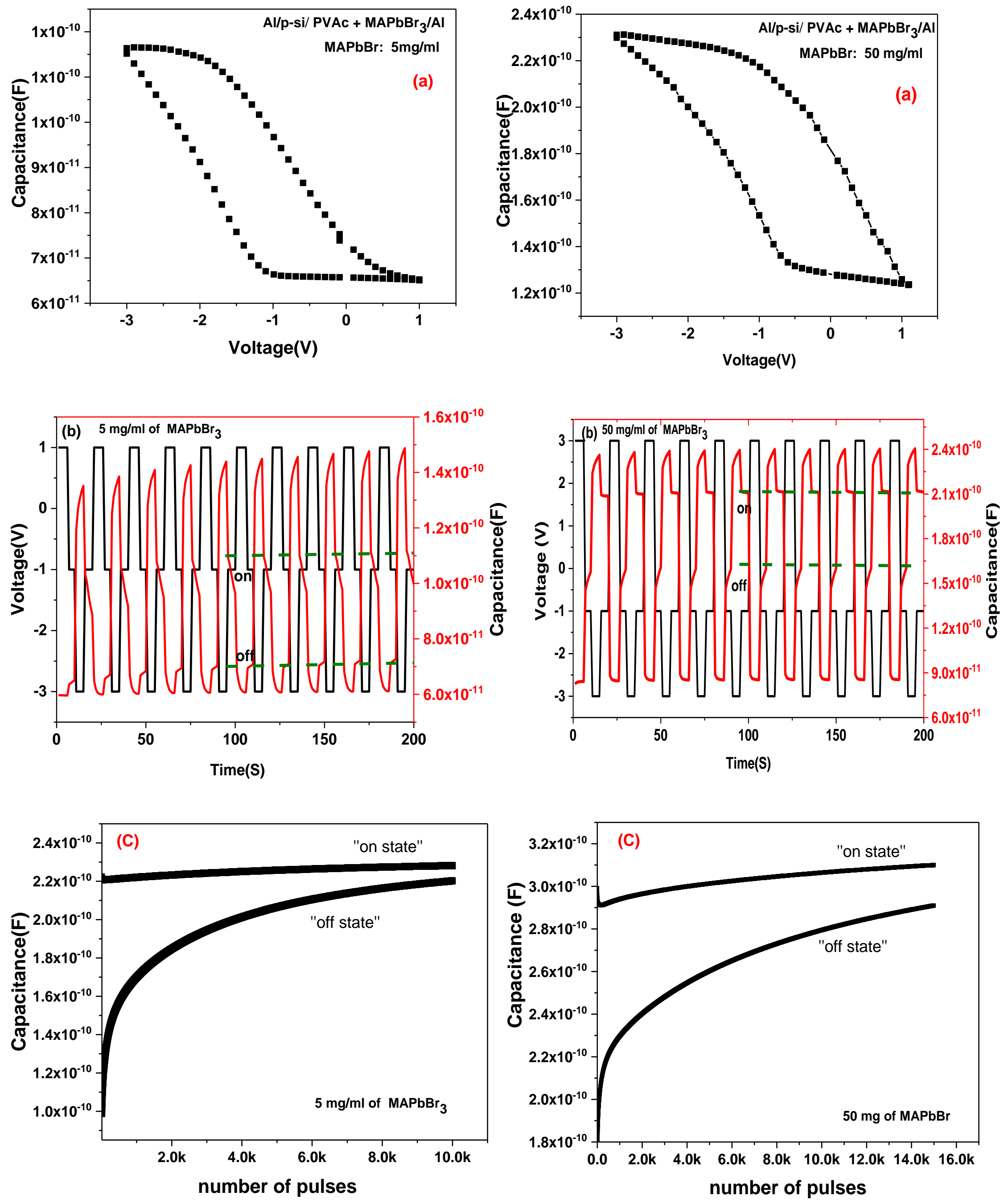


Figure 7.6 Electrical characteristics devices contain 5mg/ml and 50 mg/ml respectively, (a) C-V (b) W-R-E-R pulses, (c) retention time and stability over multiple cycles of the MIS capacitor.

7.7 Summary.

Table 7-1 : Summary of results.

Device / material composition	Area in C-V hysteresis (Coulomb)	Charge retention
PVAc (control sample)	0.04416	
NiO Blend (Al-P-Si/PVAc+NiO/Al)		
5 mg/ml 10 mg/ml 20 mg/ml 25 mg/ml 30 mg/ml 35 mg/ml	0.05238 0.24155 0.39686 0.48086 0.83113 1.23858	0.0259 nF 0.0346 nF 0.0182 nF 0.0431nF 0.0462nF 0.0513nF
NiO Layered Al-P-Si /PVAc/NiO/PVAc/Al		
12nm 44nm	0.0139 0.0225	0.019 nF 0.325 nF
$BaTiO_3$ Blend Al-P-Si /PVAc+$BaTiO_3$/Al		
5 mg/ml 10 mg/ml 30mg/ml 50 mg/ml	0.171 0.197 0.235 0.364	0.00152nF 0.00835nF 0.0172 nF 0.0253nF
$BaTiO_3$ Layered Al-P-Si /PVAc/$BaTiO_3$/PVAc/Al		
10nm	0.3054	0.0099 nF
MAPbBr Blend Al-P-Si /PVAc+$MAPbBr_3$/Al		
5 mg/ml 50mg/ml	0.0641659 0.15259715	0.00873nF, RWE: 0.0387nF 0.0194nF, RWE: 0.0489nF

CV measurement for capacitance and charge retention and durability using the MIS structure was conducted for the tested materials, in blend and layered compositions.

NiO was tested for capacitance using C-V hysteresis in a blend composition. The results revealed that an increase in the concentration of NiO corresponded to an increase in the charge storage of the capacitance (see Table 7-1). However, NiO was much less effective in terms of capacitance when in a layered composition, although it should be noted that an increase in the thickness of the layer did correspondent to an increase in charge storage of capacitance.

The effect that NiO of the ability of the blended composition to retain charge showed mixed results. Although between the 5 and 10mg/ml concentration there was an increase in charge storage, between 10 and 20mg/ml there was a significant decrease in charge retention storage. These results therefore suggest that an increase in concentration of NiO does not necessarily improve memory ability.

The various concentrations of $BaTiO_3$ in a blended composition were also found to have an increasingly positive effect on capacitance charge storage as the concentrations increase (see Table 7-1). However, where $BaTiO_3$ is in a layered composition it has a much greater positive impact on capacitance charge storage, even though the layered composition for $BaTiO_3$ is only 10nm, it has a much greater positive impact than NiO at 44nm with 0.3054nF and 0.0225nF respectively.

Methylammonium lead bromide was tested for capacitance with two blend compositions; 5mg/ml and 50mg/ml, between which there was a corresponding increase in capacitance. The test for charge retention revealed that there was a corresponding increase between an increase in blend concentration and charge retention.

Overall, all three of the tested materials were found to have a positive effect on capacitance charge storage with increasing concentrations. However, the effectiveness was varied with NiO being far more charge storage than the other two materials. In reference to charge retention, NiO in increasing concentration as a blend composition had little effect, however, in a layered composition at 44nm it had a positive impact, however, $BaTiO_3$ at only 10nm had the largest impact on capacitance charge storage.

Chapter 8 Conclusion and future work

The research of this thesis involved the testing of three materials in 2TNVM devices to determine memory function. Specifically, the research aimed to compare between three different materials through investigating the optimal combination of material constitution, including different blend and layered constitutions together with different fabrication techniques. This was achieved through the use of a MIM structure to test charging mechanism and memory device programming, and a MIS structure to test for capacitance and charge retention.

In reference to the tested materials the findings of the experiments showed that the blended compositions of the tested material and the polymer were generally more effective than the layered compositions for all of the four tested functions of memory performance. However, it should be noted that these findings for the blend composition could possibly be the result of alternative factors which include grain boundaries, surface states and defects which can result in charge trapping, dangling bonds, Schottky junction or trapping at contacts. This study has sought to verify this with $MAPbBr_3$ as a single crystal which showed hysteresis, thus eliminating these alternative factors as possibilities. Therefore, for $MAPbBr_3$ in this study has shown that it is very likely that it is the intrinsic properties that contribute to memory function.

Moreover, an increase in the amount of NiO and $BaTiO_3$ correlated with an improvement in performance for charging mechanism, memory device programming and capacitance, however, for NiO as a blend no corresponding increase was found for charge retention.

$MAPbBr_3$ proved to be the least performing material for memory device programming, capacitance and charge retention, although it performed similarly to $BaTiO_3$ for charging mechanism.

A contribution of this study was the experimentation of three materials with PVAc for 2TNVM devices that have not been previously tested. Another contribution of the study was a verification of the principles established by Paul (2007) of the internal switching of 2TNVM devices. The research investigated the internal working mechanisms for the different materials and fabrication methods to approve the principles presented by Paul (2007) referring to the behaviour of the 2TNVM device, specifically, in relation to the internal and external electrical fields. These principles were verified as part of understanding how the internal electrical field is created for the different materials and the resulting polarisation which provides bistability. The experiments in this study verified the principles of Paul (2007) which show what happens in terms of internal electrical field and polarisation when an external electrical field is applied. The internal electrical field is exploited to provide bistability for all three of the tested materials. Specifically, it was shown for NiO that its charging ability was due to its nanostructures, and through the principles established by Paul (2007) how the internal electric field was formed and its exploitation for bistability and conductivity was addressed.

The study has strengthened the model that is based on formation of the electrical dipole in polymer-based electrical devices, this has been approved using the different material compositions with a polymer. Therefore, electric dipole formation and the switching associated with a change in the external electric field has been demonstrated in this study.

8.1 Future Work

One of the findings of the study was for NiO it was found that less of this material was better for memory device programming, however, more of this material was better for charge retention. This has implications for future study in two main ways. Firstly, because less or more of this material has a differing effect, there is a need to determine the optimal amount for the optimal performance of the memory device. Secondly, the differing effect is experienced by two of the different functions of overall memory performance, i.e. memory programming and charge retention, therefore, any future consideration of optimisation in terms of amount of material would have to consider the effect on performance that each function has, in other words in consideration of the amount of material which function is more important for optimal memory.

A future study may find that all the functions are equally important and material optimisation would have to be a balance between these functions. Another finding that requires further investigation is that layered compositions were much less effective for memory function and a future study could determine the reasons why. However, although layered compositions were not as effective, where $BaTiO_3$ was tested in a layered composition it was found to be more effective, therefore, a future study could further understand the internal mechanisms in terms of electrical switching and physical composition of this material that contribute to this phenomenon.

Future work should include optimising and improving the application of the tested materials towards achieving a low cost 2TNVM device. This could include testing

memory function over a longer period of time to approve the use of the tested materials commercially.

The experiments in the study have shown that it is the internal electrical mechanisms that allow the memory abilities of the memory device. A future study could, for each of the three tested materials, investigate further how these internal electrical mechanisms can be controlled in order to increase memory capability.

Nanoparticles have been shown to be effective in memory devices when blended with a polymer. This effectiveness has been attributed to the fact nanoparticles have a high surface to volume ratio which means that more of its material interacts at the polymer interface. The present study investigated different thicknesses of a NiO nanoparticle active layer and found that an increase in thickness lead to an increase in hysteresis. However, only two thicknesses were tested, and further testing could reveal whether additional increases in layer thickness of the active material would continue to result in increased hysteresis or if there would be a decrease due to the thickness of the material. This idea is based on the principle of the increased surface area to volume ratio resulting in a more effective material in terms of hysteresis, and that an increase thickness in the layer whereby the surface area to volume ratio is decreased may result in less of the NiO nanoparticle interfacing with the polymer layer which could reduce hysteresis.

Because the results for the $MAPbBr_3$ single crystal structure eliminated the alternative possibilities for hysteresis (grain boundaries, surface states, defects, charge trapping, dangling bonds, Schottky junction, trapping at contacts) in blend compositions that are

related to the active material, there is a need to do the same single crystal tests for NiO and $BaTiO_3$.

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Appendices

9.1. Appendix A – List of Polymer and chemical Acronyms

PVAc…………………………………………………………………. poly-vinyl acetate

NiO………………………………………………………..… Nickel oxide nanoparticles

$BaTiO_3$…………………………..barium titanate

$MAPbBr_3$ ……………………………………………...… Methylammonium lead bromine

9.2. Appendix B – List of Acronyms

2TNVM ……………………………………...…. Two-terminal non-volatile memory

IT ……………………………………………………………. Information technology

CMOS…………………………….........complementary metal-oxide-semiconductor

RAM……………………………………………..………Random Access Memory

WORM……………….…………………………………… write-once read-many times

EPROM………………………………………………. Electrically Programmable ROM

EEPROM)…………………………………... Electrically Erasable Programmable ROM

ROM…………………………………………………………... Read Only Memory

MOM...Metal-Organic-Metal

MIM……………………………….……….……….…………...Metal-insulator-metal

MIS……………………………………………..…...metal-insulator-semiconductor

MOS……………………………...………..….…. Metal-oxide-Semiconductor

NVM……………………………………………………………… Non-volatile memory

ONVM…….……………………...…………….…….. Organic-Non-volatile memory

FTIR………………………….....................Fourier-transform infrared spectroscopy

UV-VIS…………………………………….…….……. Ultraviolet–visible spectroscopy

SEM……………………………………..………..… Scanning electron microscope

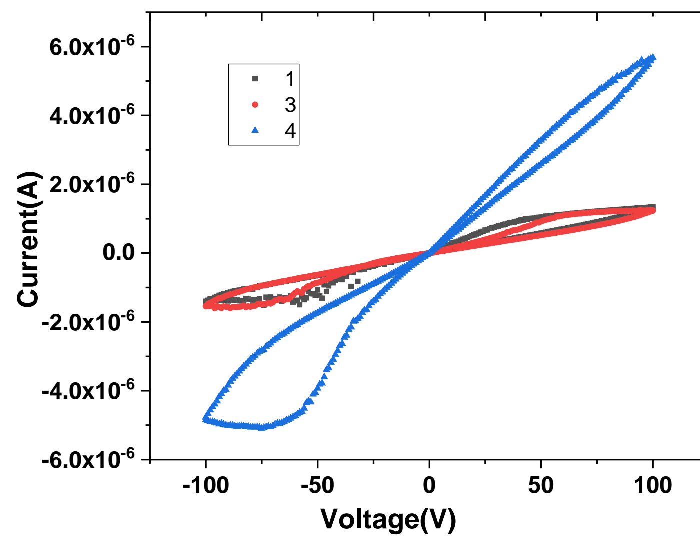
XRD…………………………………..………………………X-Ray Diffraction

I-V………………………………………………………………………. Current-Voltage

C-V ……………………………………………………............. Capacitance-Voltage

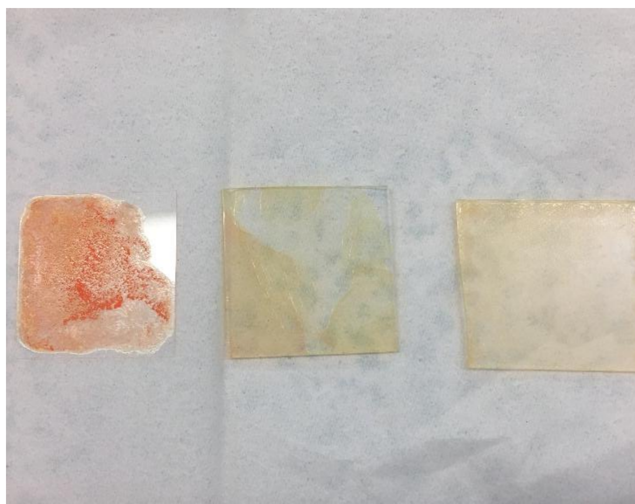
9.3. Appendix C – Supplement Data of $MAPbBr_3$ Single crystal.

Crystal Structure and IV test and



9.4. Appendix d – Supplement sample of $MAPbBr_3$ blend with PAVc as thin film.

Sample used to test XRD (drop cast and spin coating)



Sample used to test FTIR (drop cast)