Investigation of the Effects of GaAs Substrate Orientations on the Electrical Properties of Sulfonated Polyaniline Based Heterostructures

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Abstract

In this work we present a detailed study of the influence of the GaAs substrate orientation on the electrical properties of heterojunctions based on GaAs and sulfonated polyaniline (SPAN) using Current-Voltage (I-V), Capacitance-Voltage (C-V), Deep-Level Transient Spectroscopy (DLTS) and Laplace DLTS techniques. Three different GaAs substrate orientations have been investigated, namely (100), (311)A and (311)B. The I-V results revealed that the turn-on voltage (V_{on}) of SPAN/(311)B GaAs heterojunction is higher than that for SPAN/(100) GaAs and SPAN/(311)A GaAs heterojunctions. The DLTS results showed that the number of electrically active defects present in devices based on the lower index (100) plane of GaAs substrate is higher than those of higher index (311)A and (311)B GaAs substrates, corroborating with I-V results. In order to investigate the role of interface states, capacitance-frequency measurements were performed in forward bias on all three devices.

Keywords: (100) GaAs, (311)A GaAs, (311)B GaAs, hybrid device, I-V, C-V and DLTS

1. Introduction

SPAN is a p-type organic semiconductor with a direct band gap energy of 2.786 eV [1]. Due to the nature of its bandgap, it has many applications in electronic, optoelectronic and photovoltaic devices [2,3]. Furthermore, this polymer is considered as a conjugated polymer for applications in the field of rechargeable batteries, cell scaffolds and junction devices. SPAN, self-doped water soluble conducting polyaniline derivative, has attracted significant attention over the past few years due to its unique physical properties in a wide range of solutions, improved processability and potential industrial applications [4–6]. It also can be readily grown as thin film over large areas [7]. SPAN has been grown successfully on SiC [8] and Silicon [9] substrates depending on the applications. However, there are very limited studies of SPAN grown on GaAs substrates. However, SPAN/GaAs heterostructures are considered as promising candidates for solar cells application. Most of the research concentrated on the devices based on the conventional (100) GaAs substrates [10]. Recently, high index planes such as (311)B [10,11] and (311)A [11] have received more attention since structures grown on these surfaces have exclusive properties allowing improved devices performance [10,11], which significantly depends on substrates characteristics and the quality of the films as is well known. The substrates play a very important role on the incorporation of defects and impurities, and thus on the electronic properties of devices [12]. As reported by L. Yan and W. You [13] the surface orientation of semiconductors substrates influences energy levels, the density of surface states, and other important properties of the devices. They showed that the better performance of polymer/inorganic hybrid solar cells is associated to the lower density of surface states.

In this paper the electrical properties of SPAN grown on (100), (311)A and (311)B GaAs substrates are investigated for the first time by utilizing conventional DLTS, Laplace

DLTS, I-V and C-V techniques. Our results show that the (311)B based devices exhibit better performance when compared with (100) and (311)A devices.

2. Sample Details

The thin film polymers were grown using the same route as reported in reference [14]. In summary, (100), (311)A and (311)B n-type (silicon-doped: 2×10^{18} cm^{-3}) GaAs substrates were used for the self-assembly growth of SPAN thin films. After cleaning of substrates, Ohmic contacts to the wafer backside consisting of nickel (Ni) and gold (Au) deposited by thermal evaporation at a base pressure around 10^{-6} Torr utilising a BOC Edwards 306 system. For more details see process explained elsewhere [15]. This was followed by a deposition of a SPAN film of 200 nm layer onto (100), (311)A and (311)B GaAs substrates at a rate of 1.8 nm/h by adopting a technique developed by Yang et al. [16] and explained in Ref. [15], except that the growth temperature (10 °C), the aniline amount (455 μl) and the metanilic acid amount (1.715 g) were different. Finally, a circular electrical contact consisting of 99.99% Au with an area of 0.0020 cm^2 was obtained by thermal evaporation on top of the SPAN films by shadow mask evaporation to form Ohmic contacts. Finally, forming heterostructures p-n junction diode (p-SPAN/n-GaAs). The Raman system used was a LabRAM Horiba spectrometer with a 405 nm laser line as excitation and a 50 objective

3. Results and Discussions

3.1 Raman Measurements

Raman spectra of SPAN thin films on GaAs substrates were obtained and are shown in Fig. 1. The intense peaks located at ~295 cm^{-1} and ~270 cm^{-1} are the unscreened longitudinal optical and transverse optical phonon modes of GaAs, respectively [17]. The spectrum exhibits several characteristic bands of the polyaniline (see inset in figure 1). The

peaks located at ~1646, ~1590, and ~1507 cm^{-1} correspond to a C–C stretching vibration, C=C stretching vibration benzene rings, and C=N stretching vibration, respectively [18,19]. The bands at 1165 and 1320 cm^{-1} refer, respectively, to the stretching of the C–H and C–N bonds present in the quinoid segment [18,19].

3.2 Current-Voltage (I-V) Measurements

Fig.1 shows room temperature I-V curves of SPAN samples grown on (100), (311)A and (311)B GaAs substrates. It can be observed from Fig. 2(a) that the leakage current of SPAN/(311)B GaAs at reveres bias of -2V is approximately three and two orders of magnitude less than those of (100) and (311)A GaAs samples, respectively. Likewise, the linear I-V plots at 300 K for (100), (311)A and (311)B samples (see Fig. 2(b)) show that the turn-on voltage (V_{on}) values are different.

It can be observed from Fig. 2(b) that V_{on} of (311)B is higher than the other two samples. Y. Li and M. Niewczasa [20] reported that grown GaP films on (311)A GaAs produced flat surfaces, while GaP/(311)B GaAs films have rough surface morphology. Additionally, Hsu et al. [21] showed that GaAs/AlAs superlattices grown on (311)A GaAs substrates by molecular beam epitaxy (MBE) improve the flatness of hetero-interfaces and they related this to the stable surface reconstruction of (311)A. It is worth pointing out that optical properties of inorganic heterostructures grown on high index (311)A and (311)B GaAs substrates are considerably better than the similar samples grown on the conventional (100) GaAs substrates, suggesting that the starting high index (311)A and (311)B GaAs substrates are more stable and smoother [20,22,23]. According to Meng [24] hole-injection occurs at low voltages for the diodes with low hole-injection barrier and therefore the turn-on voltage is low. It is important to mention that the value of V_{on} can only be taken into account as qualitative because there are many parasitic currents paths that shunt the hetero-barrier and

leading to more complicated I-V characteristics. However, the major influence to the current is through the interface states between SPAN and GaAs substrates. Thus, the general trend is that the low index (100) samples exhibit a higher leakage current and a lower turn-on voltage which are in agreement with the fact (also as demonstrated throughout this study) that the (100) introduces more interface traps than the (311) high index samples. Yan and You [13] reported that a decrease of the density of surface states at the polymer/GaAs interface leads to a reduction of the surface recombination at the polymer/GaAs interface. Consequently, the tunnelling current can be decreased considerably by decreasing these interface states. This will result in an increase in the efficiency of solar cells. F. Yakuphanoglu et al. [25] argued that in addition to the interface states, the barrier inhomogeneity effect could influence the current through the devices as illustrated by the I-V characteristics measured at different temperatures and discussed in our earlier paper (Ref. [14]). Halliday et al. [26] claimed that the interface characteristics of the polymer semiconductor junction are controlled by surface states of the semiconductor layer. Therefore, one can conclude that the higher interface state is the major contribution to the higher leakage current in the (100) samples, as will be discussed later.

3.3 Capacitance-Voltage (C-V) Measurements

The C-V results at room temperature have been used to obtain the density of interfacial states (D_{it}). As expected, the D_{it} from SPAN/(100) GaAs devices is higher than in SPAN/(311)A and (311)B GaAs ones (the results will be presented in the next section). The capacitance of an ideal heterostructure is represented by [27]:

$$C = \beta(V_R + V_{on})^{-1/2} \qquad (1)$$

where "V_R" is the applied reverse bias, "V_{on}" is the diffusion or turn-on voltage and β is a constant containing the electron charge, the dielectric constants of the semiconductors, and the doping concentration on both SPAN and GaAs as given by:

$$\beta = \left[\frac{q\varepsilon_0\varepsilon_1\varepsilon_2 N_a N_d}{2(\varepsilon_1 N_a + \varepsilon_2 N_d)}\right]^{1/2} \quad (2)$$

where N_a and N_d are doping densities in *p* and *n* region of the diodes, and ε_1 and ε_2 are dielectric constants of SPAN and GaAs, respectively.

Plotting $1/C^2$ versus (V_R + V_{on}) in any type of ideal heterojunction or homojunction system is clearly linear. However, the nonlinearity of $1/C^2$ versus (V_R + V_{on}) of heterojunctions, particularly near (V_R + V_{on}) = 0, is a behaviour well known in the literature [28]. They are mainly produced by the interface states present on each side of the heterojunction, making the equivalent circuit significantly complicated than a simple series circuit, which consist of two equivalent devices (a conductance in parallel with a capacitance).

In this study it is revealed that the connection of two capacitances in a simple parallel model as described by Vasudev et al. [29], one symbolising the interface contribution and the other suggesting the total capacitance of the heterostructures,.

In the subsequent investigation we will introduce the interesting case where the plot of $1/C^2$ versus (V_R + V_{on}) at 300 K is non-linear for both SPAN/(100) GaAs and SPAN/(311)A GaAs devices whereas this plot is linear for SPAN/(311)B GaAs, as shown in Fig. 3. V_{on} values are obtained from the I-V measurements at 300 K.

It can be shown from Fig. 3 that $1/C^2$ versus (V_R + V_{on}) is not linear for SPAN/(100) GaAs and SPAN/(311)A GaAs heterojunctions. This behavior confirms that the junction doping profile is not abrupt. However, it is linear for SPAN/(311)B heterojunction. These

results imply that the orientation of GaAs could affect the doping profile characteristics and has a strong effect on the electrical properties of the samples

From the *C-V* results, it can be deduced that the nonlinearity of the plot $1/C^2$ as a function of $(V_R + V_{on})$ of SPAN/(100) and (311)A GaAs devices confirms that the doping in the region of 0 V to -1.5 V bias range is neither uniform nor linearly graded [30]. These results could refer to non-uniformity in the carrier distribution both at the interface and away from the interface. However, the linearity of $1/C^2$ versus $(V_R + V_{on})$ characteristics of the SPAN/(311)B GaAs devices (Fig. 3) indicates that the doping is uniform in the same bias range (depletion width). Therefore, the barrier height could be homogeneous for (311)B GaAs samples due to the uniformity of the carrier distribution at the interface and away from the interface [14]. The analysis of the C-V data showed that a lower value of V_{on} in the SPAN/(100) GaAs devices is not essentially a confirmation of lower interfacial states.

3.4 Capacitance-Frequency (C-F) Measurements

Complementary study of capacitance (C) as a function of frequency (F) was undertaken from 1 kHz to 2MHz to obtain the interface states in the three samples. Fig. 4 exhibits C-F characteristics for a DC-bias of 0 V at room temperature for the three samples. It is well-known that the behaviour of the higher values of capacitance (C) at low frequencies (F) are attributed to the additional capacitance produced from the interface states as explained elsewhere [31,32]. However, the charges at the interface are able to follow under AC voltage at low frequencies and as a result they contribute to the measured capacitance. Whereas at higher frequencies, the charges cannot follow under AC voltage (capture-emission rates are much slower) and, consequently, only the junction capacitance persists. It can obviously be seen from Fig. 4 that the value of capacitance is considerably higher at low frequencies (~1kHz) and reduces significantly as the frequency increases. This can be interpreted as a confirmation of the existence of interface states in the three samples. It can also be observed

from Fig. 4, that the capacitance of SPAN/(100) GaAs devices is much higher than those of SPAN samples grown on (311)A and (311)B GaAs substrates , which further supports our C-V analysis discussed in the previous section.

In order to determine the density of interface states (D_{it}), capacitance (C) measurements as a function of frequency (F) were performed at 300K in the forward DC-bias range 0.0-0.30 V with steps of 0.02 V. The density of the interface states was calculated by using Equation (3), as follows.

$$D_{it} = \frac{1}{qS}\left[\left(\frac{C_{LF}.C_{ox}}{C_{ox}-C_{LF}}\right) - \left(\frac{C_{HF}.C_{ox}}{C_{ox}-C_{HF}}\right)\right] \qquad (3)$$

where *S* is the area of rectifier contact (0.002 cm^2 for all three samples) and *q* is the electronic charge; C_{LF} is the value of capacitance at lowest frequency (10 kHz), C_{HF} is the capacitance at high frequency (2 MHz) and C_{ox} (oxide capacitance) is the capacitance measured in strong accumulation (i.e. in SPAN/n-GaAs heterostructures system). The C_{ox} value is obtained from the peak capacitance of the forward C-V characteristics at high frequency of 2 MHz as shown in Fig. 5 for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs samples. By using Equation (3), D_{it} values were determined and the plot of D_{it} as a function of V is illustrated in Fig. 6.

The value of D_{it} for SPAN/(311)B GaAs devices is lower than those for SPAN/(100) and (311)A GaAs devices, as shown in Fig. 6. D_{it} values obtained for SPAN devices grown on (100), (311)A and (311)B GaAs substrates are within the range of previously reported value (~10^{12} eV^{-1} cm^{-2}) found for similar devices [8]. Interface traps play a significant role in barrier inhomogeneity and in the electrical properties of heterostructures[33,34]. Consequently, the high interface trap density determined in SPAN/(100) and (311)A GaAs devices is most probable the cause of their large leakage currents, the high excess capacitance, and lower value of turn-on voltage. This confirms that the electrical performance

of SPAN/(311)B GaAs devices is better than that of SPAN/(100) and (311)A GaAs samples. As can be seen from Fig. 6, D_{it} for the three samples increases at low forward bias and then decreases from 0.15V and 0.25V for SPAN/(100) GaAs, and both SPAN/(311)A and (311)B devices, respectively.

3.5 DLTS Measurements

In order to determine the effects of GaAs crystallographic orientation on the electrical properties of SPAN/GaAs based devices, it is important to investigate the presence of electrically active defect levels. DLTS [35] and Laplace DLTS [36] are the most powerful non-destructive methods to detect traps lying within the band gap of electronic devices. DLTS experiments were carried out at different reverse bias conditions to investigate the electrically active defects both close to interface and far away from the interface for three devices studied here.

3.5.1 DLTS Measurements on SPAN/(100) GaAs Heterojunction

The depletion region where trapping and de-trapping of charge carriers processes occur can be controlled by applying different reverse biases. In order to investigate the electrically active traps at the interface and near to the interface in SPAN/(100) GaAs sample, DLTS and LDLTS measurements were carried out at small forward and reverse biases. For this, the DLTS signals from the SPAN/(100) GaAs devices were recorded at reverse bias V_R= (0 and -0.25V), filling pulse height V_P = (0.25 and 0V), pulse width t_P = 1msec and rate window = 200 s^{-1}, as illustrated in Fig. 7(a) and 6(b). On the other hand, in order to probe the defects away from the interface a large bias voltage is applied. For this, the following DLTS experimental parameters were utilized: reverse bias V_R = -1.5V, filling pulse height V_P = 0V,

pulse width t_P = 1msec and rate window = 200 s^{-1}, as shown in Fig. 7(c). The samples were scanned by DLTS from 10K to 450K.

It can be observed that for reverse bias condition V_R = 0V and V_P = 0.25V (the region considered is towards the interface) only positive peaks (due to electrons which are majority carriers) are detected (see Fig. 7(a)). Likewise, the DLTS signal for bias V_R = -0.25V and V_P = 0V (the region considered is very close to the interface) displays only positive peaks as illustrated in Fig. 7(b). While, by applying a large reverse bias of V_R = -1.5V and V_P = 0V negative (due to holes which are minority carriers) and positive peaks are observed, as shown in Fig. 7(c). The full width at half maximum (FWHM) of the peaks found by conventional DLTS at biases (V_R = 0V, V_P = 0.25V), (V_R = -0.25V, V_P = 0V) and (V_R = -1.5V, V_P = 0V) (see Fig. 7) is higher than 0.1Tm (Tm is the maximum peak intensity). The reason for this behaviour is that the defects are in multiple states [37].

All the detected peaks are broad, and in order to resolve them the isothermal Laplace DLTS technique (LDLTS) is used. By plotting the temperature as a function of emission rate one can determine the energy of the trap from the slope. First of all, the LDLTS measurements for the forward bias condition (V_R = 0V, V_P = 0.25V, t_p = 1msec) are performed on SPAN/(100) GaAs samples to probe the electrically active traps at the interface. The LDLTS at a wide temperature range (~175–390 K) revealed the presence of three electron traps (see Fig. 7(a)), the first two traps are shallow electron traps $E_{11(100)}$ and $E_{12(100)}$ with activation energies of (0.027 ± 0.002 eV) and (0.103 ± 0.007 eV), respectively, and the third one is deep electron trap $E_{13(100)}$ with activation energy of (0.167 ± 0.005 eV). The activation energies of these traps are calculated by using Arrhenius plots as illustrated in Fig. 8(a). All these defects are expected to originate from (100) n-GaAs substrate. The electron defect level ($E_{12(100)}$) detected in SPAN/(100) GaAs samples could be related to level M0 (0.10 eV) in MBE grown n-GaAs studied by D. V. Lang et al. [38]. Trap ($E_{13(100)}$) could

be associated with level M1 (0.17 eV) in n-GaAs analysed by W. C. Dautremont-Smith et al. [39]. Whilst, by applying a small reverse bias of V_R = -0.25V and V_P = 0V two electron traps are detected, namely $E_{21(100)}$ and $E_{22(100)}$ at the temperature range (~225–395 K) as shown in Fig. 7(b)). The activation energy of shallow defect $E_{21(100)}$ (0.053 ± 0.003 eV) is comparable to the activation energy reported by R. H. Mari et al. [40] in n-type GaAs grown by MBE on (100) and (211)B GaAs planes. This energy is significantly smaller than previously reported in n-type GaAs grown by MBE for the same temperature range [41]. However, deep trap level $E_{22(100)}$ (0.207 ± 0.007 eV) has almost a similar energy as M1 (0.21 ± 0.01 eV) that was reported already in GaAs by D. V. Lang et al. [38]. It was proposed that M1 could be associated with a chemical impurity or a complex formed between impurities and intrinsic defects. Arrhenius plots for the detected electron traps at reveres bias V_R = -0.25V and V_P = 0V is presented in Fig. 8(b). The electron peaks observed in this sample could be the reason of inhomogeneities at the interfaces due to growth process of SPAN on (100) GaAs. Furthermore, electron defect states produced very close to the interfaces have a strong influence on the values of leakage currents obtained in this sample.

Additionally, in order to study the electrically active defects away from the interface of SPAN/(100) GaAs heterojunctions, the LDLTS technique is carried out for a reverse bias V_R = -1.5V and V_P = 0V. Increasing the reverse bias from V_R = -0.25V to V_R = -1.5V leads to the appearance of two new hole traps. The LDLTS demonstrates the presence of four traps for the SPAN/(100) GaAs heterojunction at V_R = -1.5V as shown in Fig. 7(c): (1) a shallow and deep hole trap $H_{1(100)}$ and $H_{2(100)}$ with energies (0.045 ± 0.003 eV) and (0.26 ± 0.003 eV) over a broad temperature range (~15–290 K), respectively, and (2) two deep electron traps $E_{31(100)}$ (0.302 ± 0.007 eV) and $E_{32(100)}$ (0.46 ± 0.03 eV) at temperature range (~300–395 K). The activation energies of these traps are obtained from the slope of the Arrhenius plots as illustrated in Fig. 9. The shallow trap $H_{1(100)}$ is observed for the first time in SPAN. *Shallow*

traps in polymers are due to the distribution of energetic states (tail states) around the lowest unoccupied molecular orbital LUMO and the highest occupied molecular orbital HOMO levels within the energy gap. Nevertheless, the energetic levels of the *deep traps in* polymers materials are energetically situated far from the LUMO and the HOMO levels [42]. The values of the thermal activation energy of deep hole trap $H_{2(100)}$ in this heterojunction has the same energy as $H2_{4H}$ and $H1_{6H}$ in SPAN/4H-SiC and SPAN/6H-SiC heterostructures determined by DLTS techniques [8]. Additionally, this energy is almost similar to that of the polaron band from sulfonated polyaniline as reported by Sutar et al. [43]. They have used Atomic Force Microscopy to measure the polaron bands with energy around 0.25 eV between the LUMO and HOMO levels. [43]. Therefore, the origin of the trap level $H_{2(100)}$ could probably be related to the polaron band. The activation energy of $E_{31(100)}$ is similar to that of level EL7 reported in MBE grown GaAs, but its origin is unclear [44]. Whereas, trap level $E_{32(100)}$ is assigned to the well-known M4 electron trap (0.45 – 0.51 eV) [38,39]. Regarding the origin of M4 defect, there are two controversial suggestions reported in the literature: (i) a complex involving a native defect and a chemical impurity [38], and (ii) carbon or oxygen impurities [39]. The activation energies, and defect concentrations for this sample are summarised in Table 1 for reverse bias V_R= (0, -0.25 and -1.5 V) and filling pulse height V_P = (0.25 and 0V).

In summary, only electron defects (from GaAs substrate) are detected at and close to the interface region between SPAN and GaAs. However, two hole defects are present in the region away from the SPAN/(100) GaAs interface. These traps are expected to originate from polymer SPAN. Furthermore, it can be revealed that more traps are detected in SPAN/(100) GaAs samples away from the interface region.

3.5.2 DLTS Measurements on SPAN/(311)A GaAs Heterojunction

The DLTS spectra obtained from SPAN/(311)A GaAs samples are illustrated in Fig. 10. Three peaks are obtained by Laplace DLTS for V_R = 0V and V_P = 0.25V (region probed is closer to the interface). These defects ($E_{11(311)A}$, $E_{12(311)A}$, and $E_{13(311)A}$), whose properties are calculated from Arrhenius plots as displayed in Fig. 11, are majority electron traps from n-GaAs substrate. It is important to note that although defect $E_{11(311)A}$ has the same energy and origin as defect $E_{13(100)}$ (0.167 eV) that was discussed already in previous section, the trap concentration of $E_{11(311)A}$ (4.05×10^{14} cm^{-3}) is approximately one order of magnitude less than that of trap $E_{13(100)}$ (5.24×10^{15} cm^{-3}). Furthermore, the energy level of trap $E_{12(311)A}$ (0.216 ± 0.018 eV) is almost similar to that of $E_{22(100)}$ detected at reverse bias of -0.25V in SPAN/(100) GaAs devices but its concentration is lower. $E_{12(311)A}$ has the same energy and origin as M1 [32]. Moreover, the LDLTS results indicate that $E_{13(311)A}$ for V_R = 0V in SPAN/(311)A GaAs and $E_{31(100)}$ for V_R = -1.5V in SPAN/(100) GaAs have almost the same thermal activation energy, whereas the trap concentration of $E_{13(311)A}$ (7.32×10^{14} cm^{-3}) is around one order of magnitude lower than that of $E_{31(100)}$ (1.26×10^{15} cm^{-3}). The decreasing of trap concentration could be related to the n-GaAs substrate orientation and/or its surface interaction with SPAN. Therefore, the low trap concentration could probably explain the smaller reverse leakage current observed in SPAN/(311)A GaAs as compared to (100) devices (see section 3.1).

The most significant characteristic in Fig. 10(a) is the shape of the peaks in SPAN/(311)A GaAs samples (temperature range 250K-430K) as compared to those observed in the SPAN/(100) GaAs devices. Nonetheless, while the peak extends on both sides in the SPAN/(100) GaAs samples, when the reverse bias is increased to -0.25 and -1.5V in the SPAN grown on (311)A GaAs substrate the peaks compress mostly on the left hand side whilst an increasing contribution from hole capture-emission appears on the left hand side as

a negative peak. As a result, some peaks start annihilating for a reverse bias V_R = (-0.25, and -1.5V) by changing the orientation of GaAs substrate from (100) to (311)A. Nevertheless, as shown in Fig. 10(b) new peaks appear, which were absent in the SPAN/(100) GaAs samples. These new peaks start appearing for a reverse bias $V_R \geq$ -0.25V.

It can also be seen from Fig. 10 that at a reverse bias of V_R = -0.25V and -1.5V, electron and hole peaks are clearly visible in the temperature range 250 - 440K. However, this hole peak was not found close to the interface region in SPAN/(100) GaAs devices when a small reverse bias of V_R = -0.25V was applied.

It can be noted from the Arrhenius plots for the reverse bias V_R = -0.25V (see Fig. 12) that only two traps, one hole and one electron trap, can be detected. The hole peak $H_{21(311)A}$ with energy of (0.23 ± 0.01 eV) in the SPAN/(311)A GaAs samples has not been reported previously and is observed here for the first time. This defect is predicted to originate from polymer (SPAN) between HOMO and LUMO levels because this polymer is a p-type semiconductor. However, the activation energy of electron trap $E_{21(311)A}$ (0.51eV) is similar to that of the well-known M4 trap (0.51eV) as explained in the previous section [38,39].

The Arrhenius plots for the reverse bias V_R = -1.5V (region probed is away from the interface) are illustrated in Fig. 13. It can be observed that in SPAN/(311)A GaAs only two peaks, hole $H_{31(311)A}$ and electron $E_{31(311)A}$ traps are observed. In contrast, at the same reverse bias in SPAN/(100) GaAs samples four traps (two hole and two electron traps) were found as discussed in the previous section. In other words, both hole ($H_{31(100)}$) and electron ($E_{31(100)}$) traps at high reverse bias (-1.5V) are annihilated by changing the substrate orientation of GaAs from (100) to (311)A. Due to this decreasing number of traps, the electrical characteristics of (311)A structures are improved, and consequently the substrate surface has a strong influence on the electrical properties of the devices. This is an evidence that $H_{31(100)}$ and $E_{31(100)}$ contribute significantly to the reverse leakage current obtained in the (100)

samples. The activation energy of hole defect ($H_{31(311)A}$ = 0.26 ± 0.02 eV) is the same as that of trap $H_{2(100)}$, and has the same origin ($H2_{4H}$ and $H1_{6H}$) as it was already discussed in the case of the SPAN/(100) GaAs devices. However, the electron trap $E_{31(311)A}$ with an activation energy (calculated from Arrhenius plot shown in Fig. 13) of (0.54 ± 0.01eV) is assigned to the well-known EL3 trap in GaAs which originates from a complex of Arsenic-interstitial (As_i) and Arsenic-vacancy (V_{As}) [45]. The activation energies and defect concentrations are summarised in Table 1 for a reverse bias (V_R = 0V and V_P = 0.25V), (V_R = -0.25V and V_P = 0V) and (V_R = -1.5V and V_P = 0V).

3.5.3 DLTS Measurements on SPAN/(311)B GaAs Heterojunction

Fig. 14 illustrates the DLTS spectra obtained for the regions at/close to the interface and away from the interface of the p-n devices by using a low and high reverse biases. The conditions of the DLTS experiments are V_R = (0, -0.25 and -1.5V), V_P = (0.25 and 0V), t_P = 1msec, and rate window = 200 s^{-1}. It is worth noting from Fig. 14(a) that for the (311)B samples at V_R = 0 and V_P = 0.25V (probing the interface region) only two peaks, namely $E_{11(311)B}$ and $E_{12(311)B}$, are obtained in the temperature range (~270 – 395 K). These traps are related to electron emitting defect levels determined from Arrhenius plots as displayed in Fig. 15. Level $E_{11(311)B}$ (0.38 ± 0.01eV) in this substrate orientation has a similar activation energy as EL16 (0.38 eV) reported in Vapour Phase epitaxy (VPE) grown GaAs layers [41,44]. The origin of EL16 is still unknown. However, the activation energy of $E_{12(311)B}$ (0.495 ± 0.018eV) is comparable to that of the defect M4 detected in the (100) and (311)A samples. On the other hand, it is important to mention that at the same reverse bias for the other substrates orientations, three electron traps were observed as illustrated in Fig. 7(a) and Fig. 10(a). The defect levels $E_{13(100)}$ in SPAN/(100) GaAs and $E_{13(311)A}$ in SPAN/(311)A GaAs samples, which are identified as M1 and EL7, respectively, are absent in SPAN/(311)B GaAs

samples. This investigation confirms that these traps are contributing to the higher reverse leakage current of the (100) and (311)A samples. The I-V characteristics displayed in Fig. 2 show that the SPAN sample grown on (311)B substrate has the smallest reverse current than all the other samples. This obviously confirms that the decrease of the reverse current in (311)B samples is due to the annihilation of M1 and EL7.

It can also be seen from the right side of Fig. 14(a) that the electron peaks observed at V_R = (-0.25 and -1.5V), V_P = 0V, and t_P = 1msec in the temperature range (~350 – 425 K) are very symmetric with FWHM < 0.1Tm which is the finger print of a single level [37]. However, the hole peaks obtained in the temperature range (~210 – 348 K) and shown in Fig. 14(b) are asymmetric. By increasing the reverse bias from V_R = 0 to -0.25 and decreasing the forward filling pulse from V_P = 0.25 to 0V (region probed is close to the interface), the hole peak ($H_{21(311)B}$ displayed in Fig. 14(a)) with an activation energy (calculated from Arrhenius plot presented in Fig. 16) of (0.43 ± 0.04 eV) is found in (311)B samples. This defect, which is predicted in SPAN films, is observed here for the first time and therefore can be considered as a new trap. Additionally, this is a good contribution for understanding the electrical properties for futures devices using SPAN as active layer. Also, one deep electron defect labelled as $E_{21(311)B}$ with an energy of ~ 0.89eV is observed in the same depletion region of SPAN/(311)B GaAs samples. This trap is identified as EL2 trap which is well-known in GaAs. The location of EL2 trap in the energy gap as obtained by DLTS measurements is ~ 0.80eV below the conduction band edge [46]. Bardeleben et al. [47] suggested EL2 has a complex nature involving an Arsenic antisite (As_{Ga}) and an intrinsic interstitial (As_i) rather than just an isolated As_{Ga} defect.

In order to probe the electrically active defects in regions away from the interface and the effect of substrate orientation, further DLTS experiments with larger reverse biases are performed. By applying reverse bias of V_R = -1.5V and V_P = 0V negative (deep hole trap) and

positive (deep electron trap) peaks are detected, as shown in Fig. 14. The activation energy of these hole and electron traps (calculated from Arrhenius plot shown in Fig. 17) are $H_{31(311)B}$ = 0.37 ± 0.03 eV and $E_{31(311)B}$ = 1.08 ± 0.04 eV, respectively. This hole trap is almost the same as that reported by Sutar et al. [43] which has already been discussed for the case of SPAN/(100) GaAs. However, the origin of the electron defect ($E_{31(311)B}$), which is from GaAs, is not known yet. The activation energies and trap concentrations for these samples at all biases (V_R = 0V, V_P = 0.25V), (V_R = -0.25V, V_P = 0V) and (V_R = -1.5V, V_P = 0V) are shown in Table 1.

It can be noted from Table 1 that the numbers of defects in all three samples at reverse bias of V_R = -0.25V (region close to the interface) are equal, but with different activation energies. On the other hand, by increasing the reverse bias (V_R) from 0 to -1.5V and decreasing the forward filling pulse (V_P) from 0.25 to 0V, the number of the traps increases from three to four traps in SPAN/(100) GaAs samples. However, the number of defects in SPAN/(311)A GaAs samples decreases from three to two defects, while, in the SPAN/(311)B GaAs structures the number of traps remains two. Consequently, the number of traps in SPAN/(100) GaAs samples is higher than that of (311)A and (311)B substrates. This confirms that the orientation of n-GaAs substrate has a significant influence on incorporation of impurities and defects, and subsequently on the electronic properties of SPAN/n-GaAs devices. It can also be observed from this Table that the defects $E_{13(100)}$, $E_{22(100)}$, $E_{11(311)A}$ and $E_{12(311)A}$ have same origin as M1 but with different trap concentrations as it was already discussed in previous section. Additionally, the trap concentration of $E_{31(100)}$ (in the region away from the interface of SPAN/(100) GaAs) is one order of magnitude higher than that of $E_{13(311)A}$ (at the interface region of SPAN/(311)A GaAs devices) although the energy and origin of both traps are the same as EL7. The defects M1 and EL7 are absent in SPAN/(311)B. Moreover, the defect $H_{2(100)}$ has the same energy and origin as defect $H_{31(311)A}$,

however, the trap concentration of $H_{2(100)}$ (1.40×10^{16} cm^{-3}) is approximately one order of magnitude greater than that of trap $H_{3(311)A}$ (1.43×10^{15} cm^{-3}). This difference could be due to the change of substrate orientation from (311)A to (311)B. Furthermore, one can also conclude from Table 1 that the three defects $E_{32(100)}$, $E_{21(311)A}$ and $E_{12(311)B}$ have the same origin as M4 but having different concentrations in different depletion regions.

Our results lead us to conclude that the electrical properties of the devices are related to the interface characteristics between the polymer and the GaAs substrate. Indeed, density of surface states was shown to be dominant over the electrical properties of the devices. We know that the (311)A substrate surface contains twofold coordinated (100)-like As atoms and threefold coordinated (111)A-like Ga atoms, while the (311)B substrate surface contains twofold coordinated (100)-like Ga atoms and threefold coordinated (111)B-like As atoms. Thus, the substantial difference on the electrical properties of the devices is related to the termination of the surface atoms of the substrates.

The (311)A substrate has a Ga-based native oxide on its surface, that is an amphoteric oxide, which in the acid solution will act as a base, i.e., will capture the protons from the polyaniline solution. It is important to note here that the SPAN films were grown using an aqueous acid solution, i.e., the surface of the substrates was in contact with the solution during the growth of the polymer film. On the other hand, the (311)B substrate has an As-based native oxide on the substrate surface, which is a mildly acidic oxide, which is a substance that commonly dissociates in water. This could be a reasonable reason to explain the fact that lower density of interface states observed in the devices based on (311)B substrate. In the case for devices grown on (100) orientation, the high Dit and defects are due to two effects; crystallographic orientation and the interaction of the substrate with the polymer during growth process in acid aqueous solution.

4. Conclusion

In summary, the effects of substrate orientations of n-type GaAs, namely (100), (311)A and (311)B, on the electrical properties of p-n SPAN/GaAs samples are studied. The reverse bias current-voltage measurements of all three samples revealed that the leakage current is lower in SPAN/(311)B GaAs samples than in both SPAN/(100) GaAs and SPAN/(311)A GaAs samples. Additionally, the higher V_{on} in SPAN/(311)B GaAs samples was tentatively attributed with the lower number of defects than in SPAN/(100) and (311)A GaAs structures. The elaborated C-V analysis and C-f measurements also confirmed that the change of substrate orientation from (100) and (311)A to (311)B results in a decrease of the density of interface states (D_{it}). This is also supported by the larger number of defects obtained by DLTS in the (100) and (311)A samples at/very close to the interface region between SPAN and GaAs. Amongst these traps, M1 ($E_{13(100)}$, $E_{22(100)}$, $E_{11(311)A}$ and $E_{12(311)A}$) is the main midgap trap revealed in both SPAN/(100) GaAs and SPAN/(311)A GaAs samples. However, this defect is entirely annihilated in SPAN/(311)B GaAs samples. M1 trap plays a role at and near the interface between polymer (SPAN) and GaAs. These results confirmed that the M1 defect contributes to the higher reverse leakage current of (100) and (311)A devices. Nonetheless, it is obvious from this work that the electrical properties of the samples grown on the (311)B GaAs are better than those grown on (100) and (311)A GaAs in terms of the number of electrically active traps.

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Figures and Captions

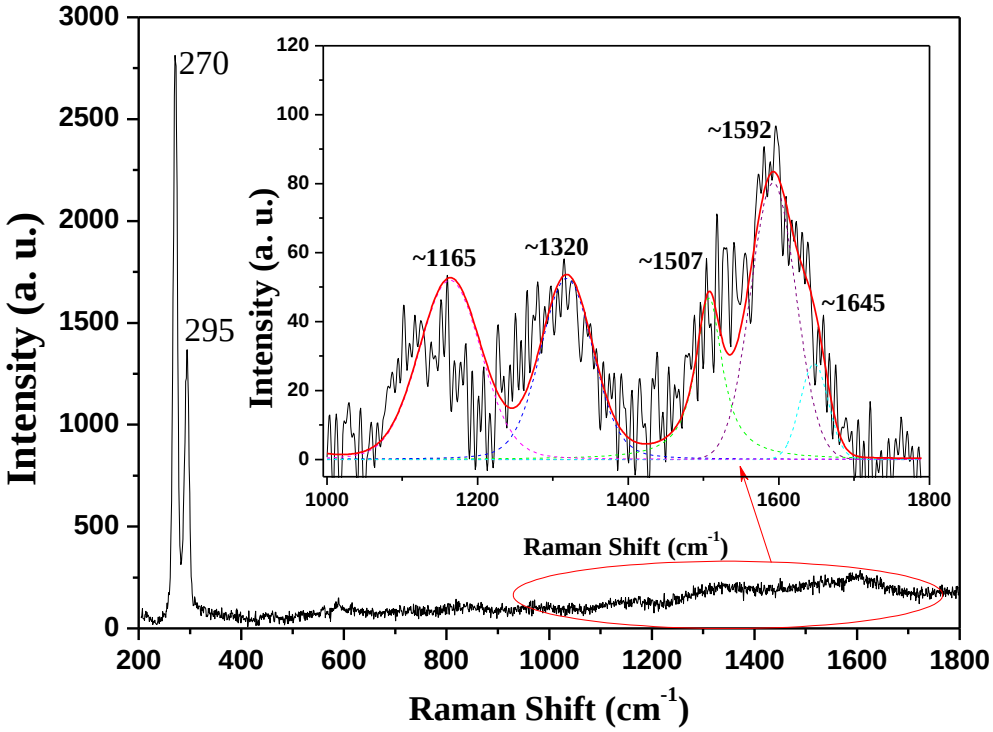

Fig. 1. Raman spectrum for SPAN film on the GaAs (311)B substrates. The inset shows the enlarged view where the most of Raman peaks of SPAN are located. Dashed trace and read color under curve are Lorentzian fittings of characteristics Raman peaks of SPAN.

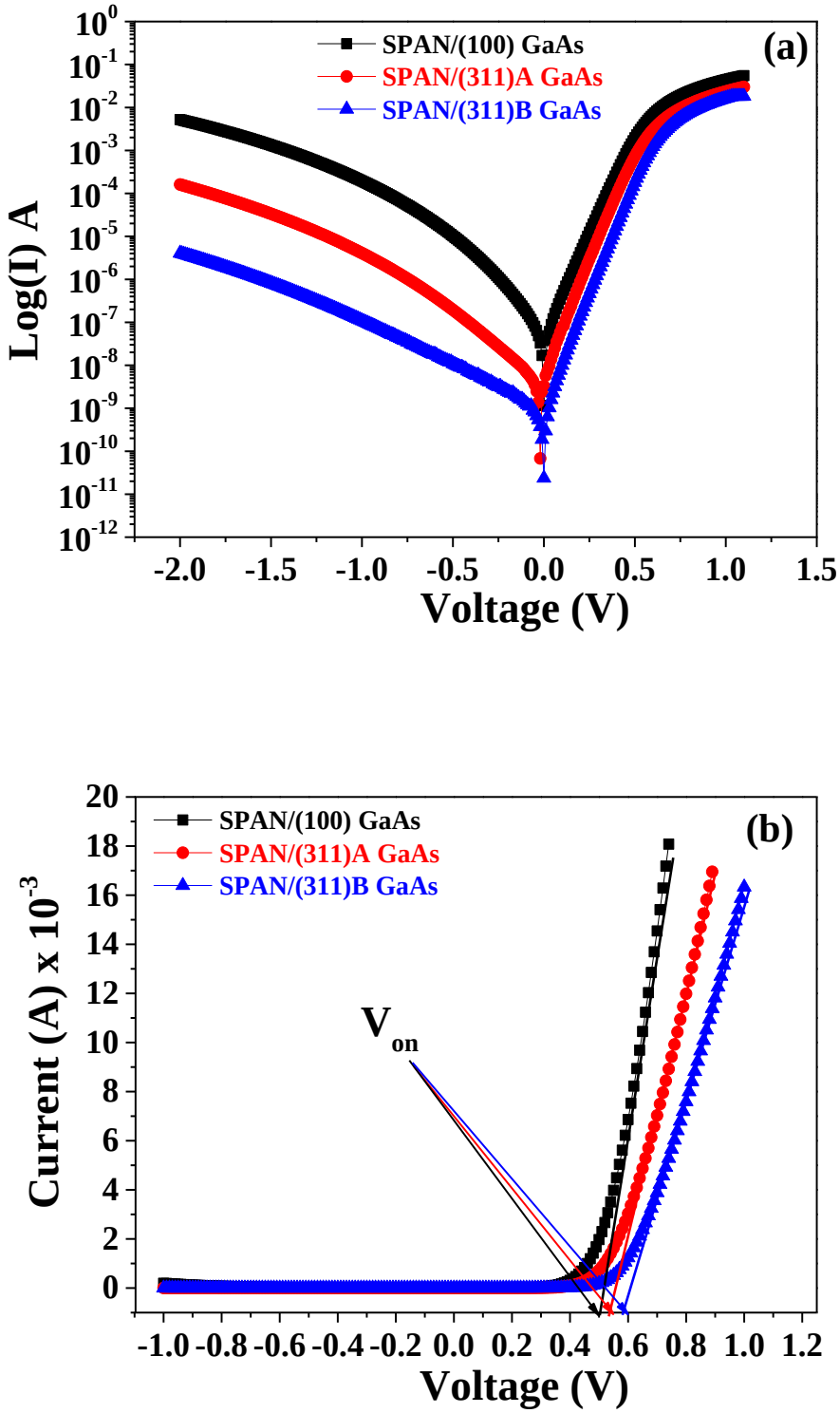

Fig. 2: (a) Current voltage (I-V) characteristics of SPAN grown on (100), (311)A and (311)B GaAs, and (b) The turn on (V_{on}) values of SPAN grown on (100), (311)A and (311)B GaAs.

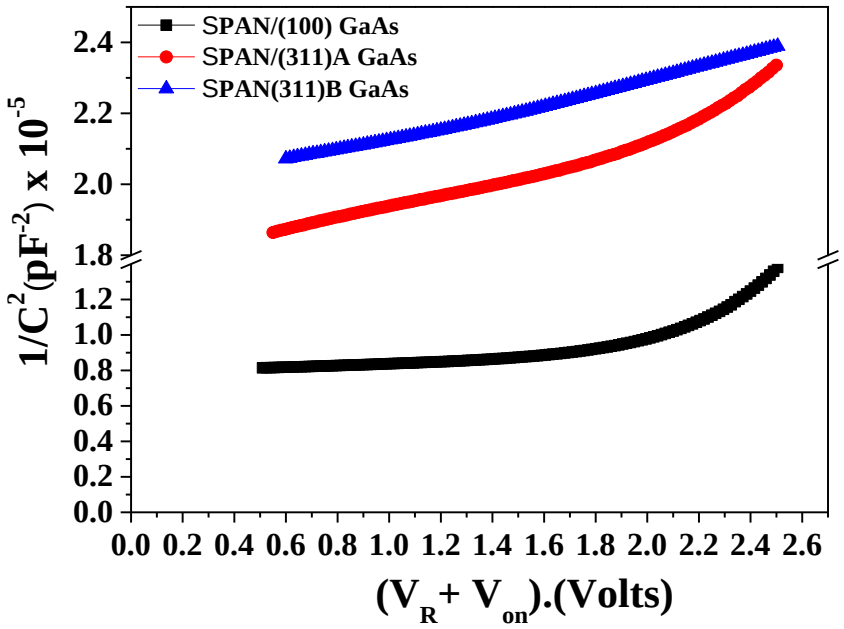

Fig. 3: Plot of $1/C^2$ versus (V_R + V_{on}). The capacitance was measured at a frequency of 1MHz.

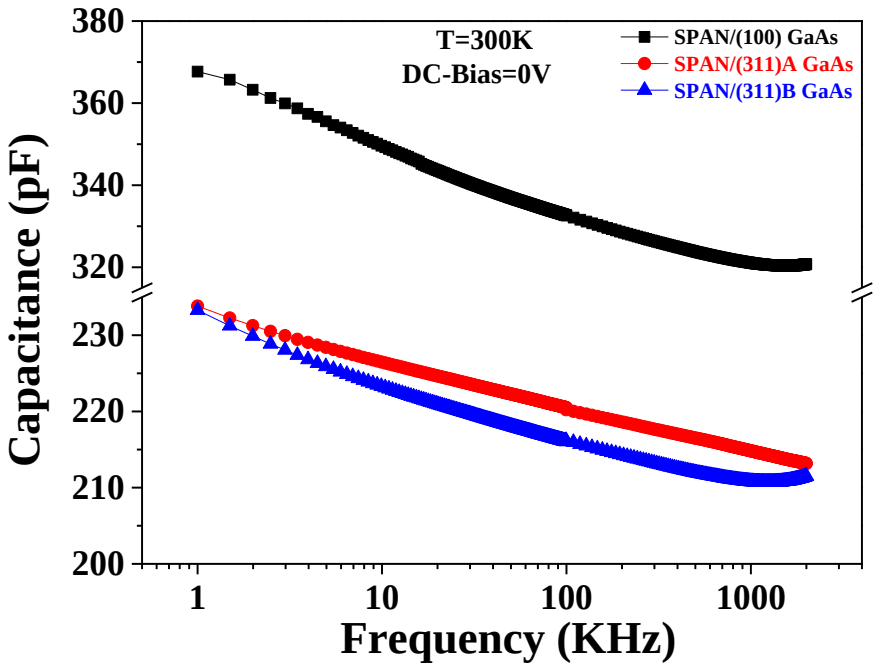

Fig. 4: Capacitance (C) as a function of frequency (F) characteristics at room temperature of SPAN/(100), (311)A and (311)B GaAs heterojunctions.

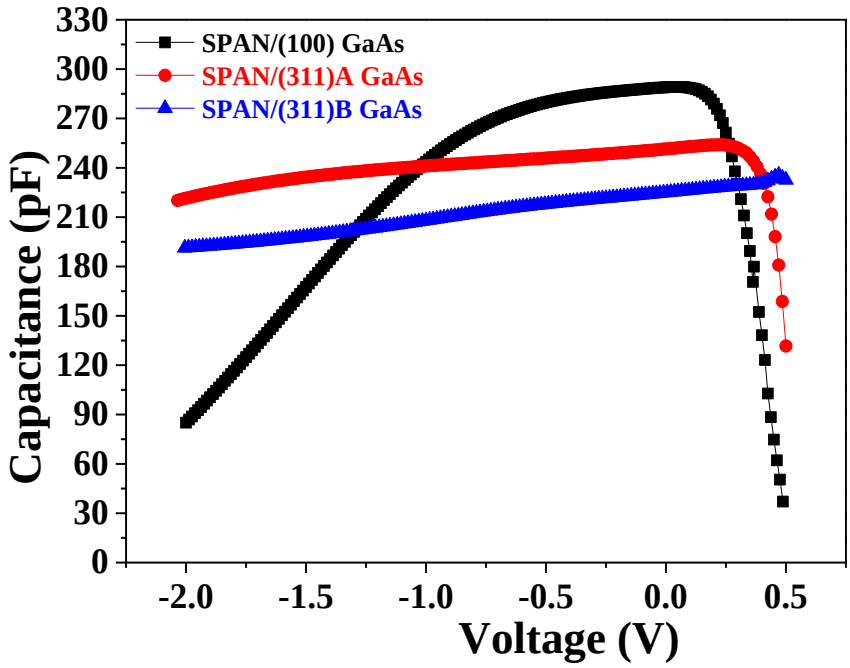

Fig. 5: The experimental C–V plots of the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs samples at T = 300 K and frequency of 2 MHz.

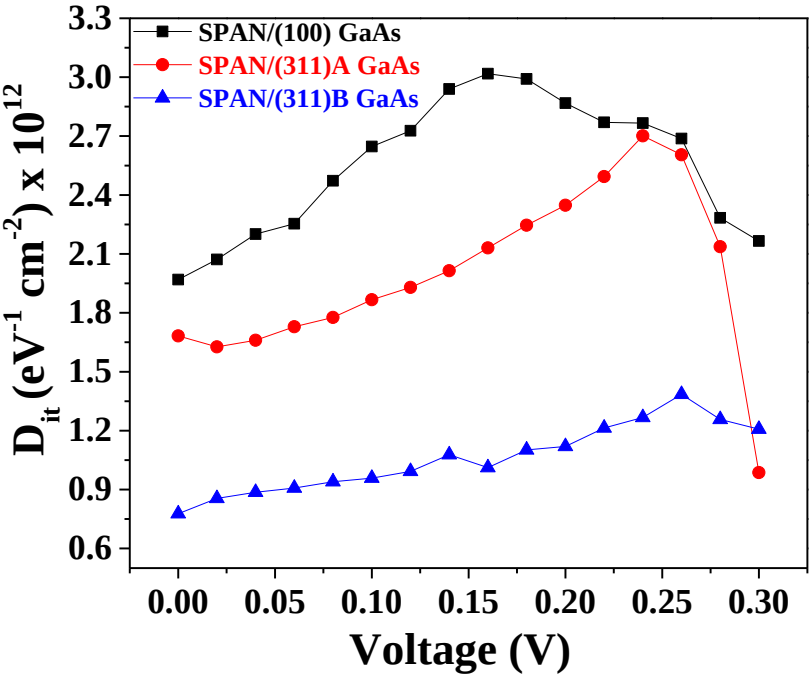

Fig. 6: Plot of D_{it} versus V obtained from high-low frequency capacitance technique for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs devices at room temperature.

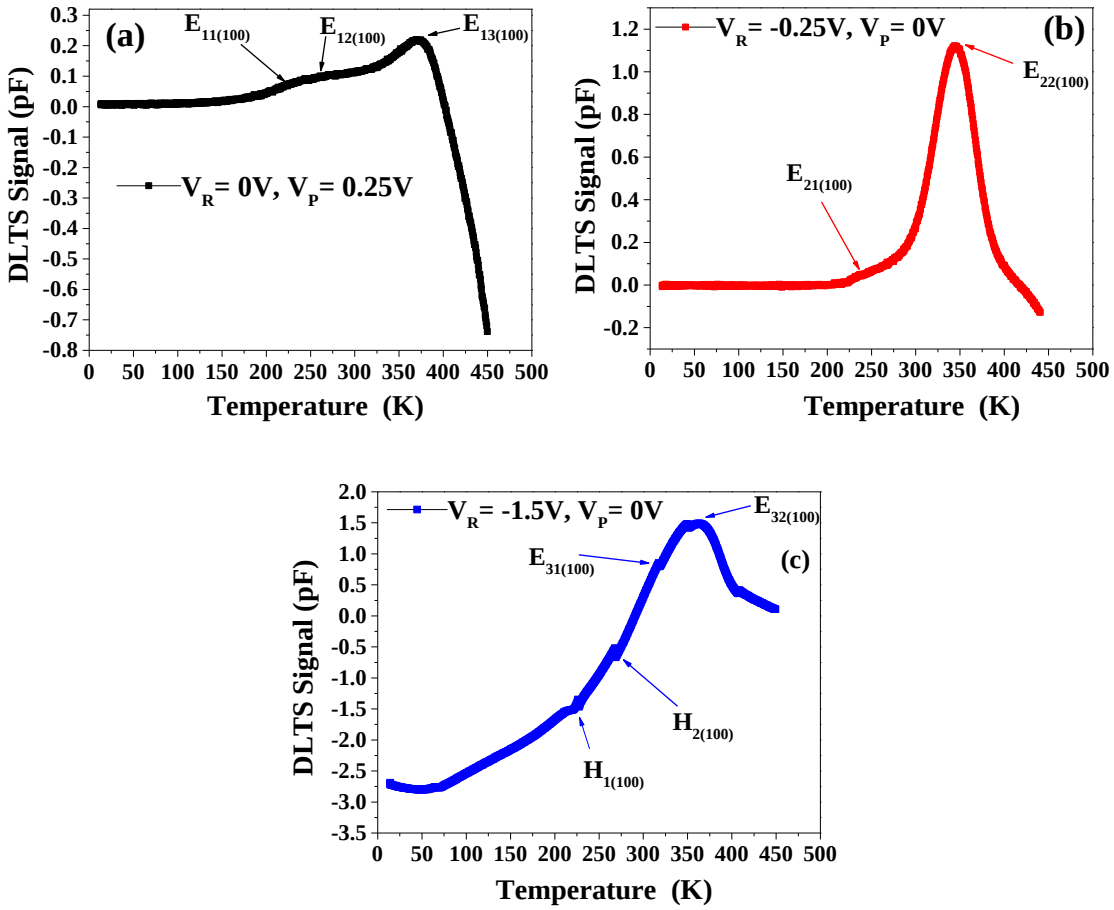

Fig. 7: DLTS measurements SPAN/(100) GaAs heterojunctions at different reverse biases, (a) V_R = 0V and V_P = 0.25V in order to inspect the interface between SPAN and (100) GaAs substrate, (b) V_R = -0.25V and V_P = 0V in order to probe the region near to interface, and (c) V_R = -1.5V and V_P = 0V which allows probing region away from the interface of this sample. A rate window of 200 s^{-1} and t_P = 1msec were used.

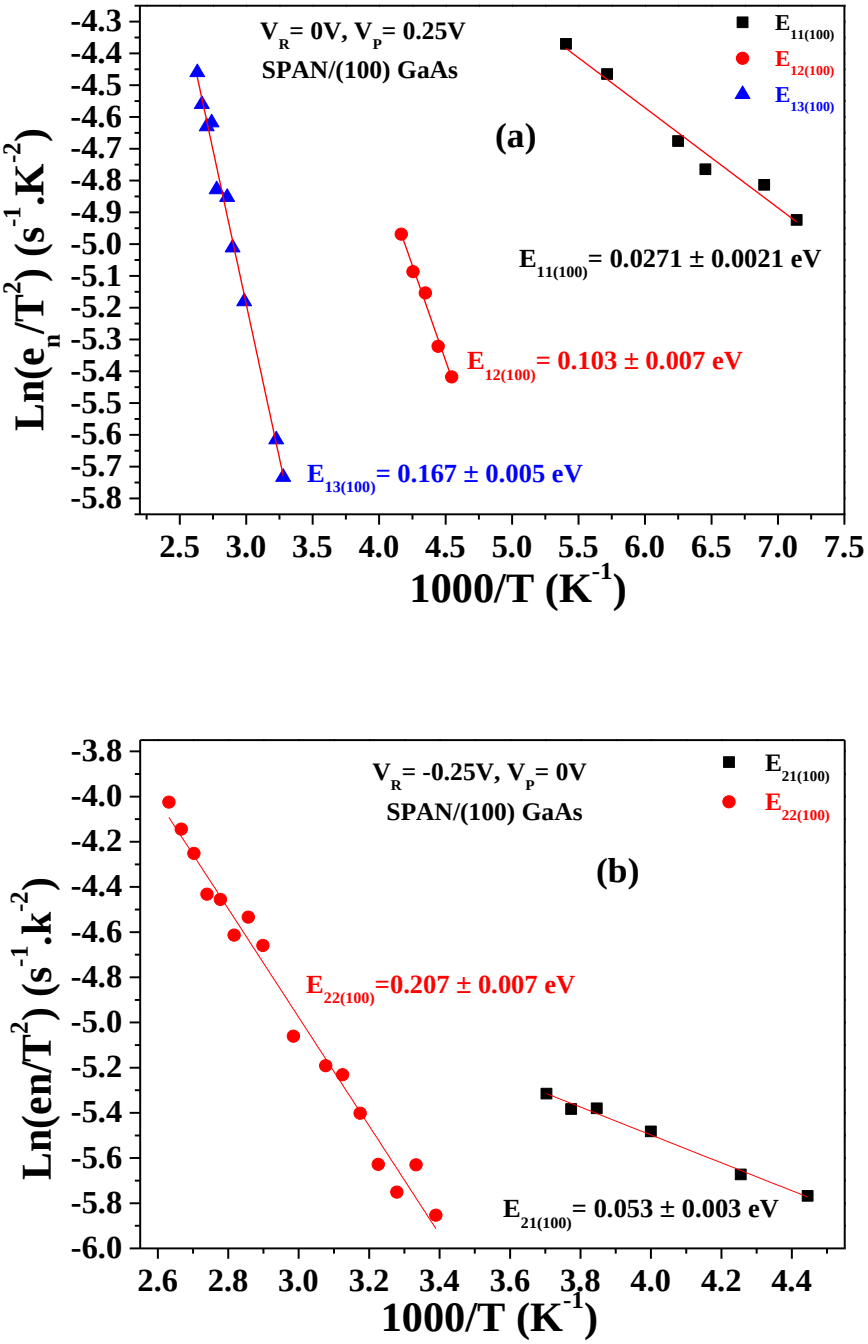

Fig. 8: Arrhenius plots obtained from Laplace DLTS at different biases, (a) V_R = 0V and V_P = 0.25V which allows probing the interface region of SPAN/(100) GaAs heterojunction devices, there are only three traps at this bias, and (b) V_R = -0.25 V and V_P = 0V bias condition used to probe the region close to the interface of this sample (it can be seen that there are only two traps in this region). The rate window is 200^{-1} and t_P = 1msec.

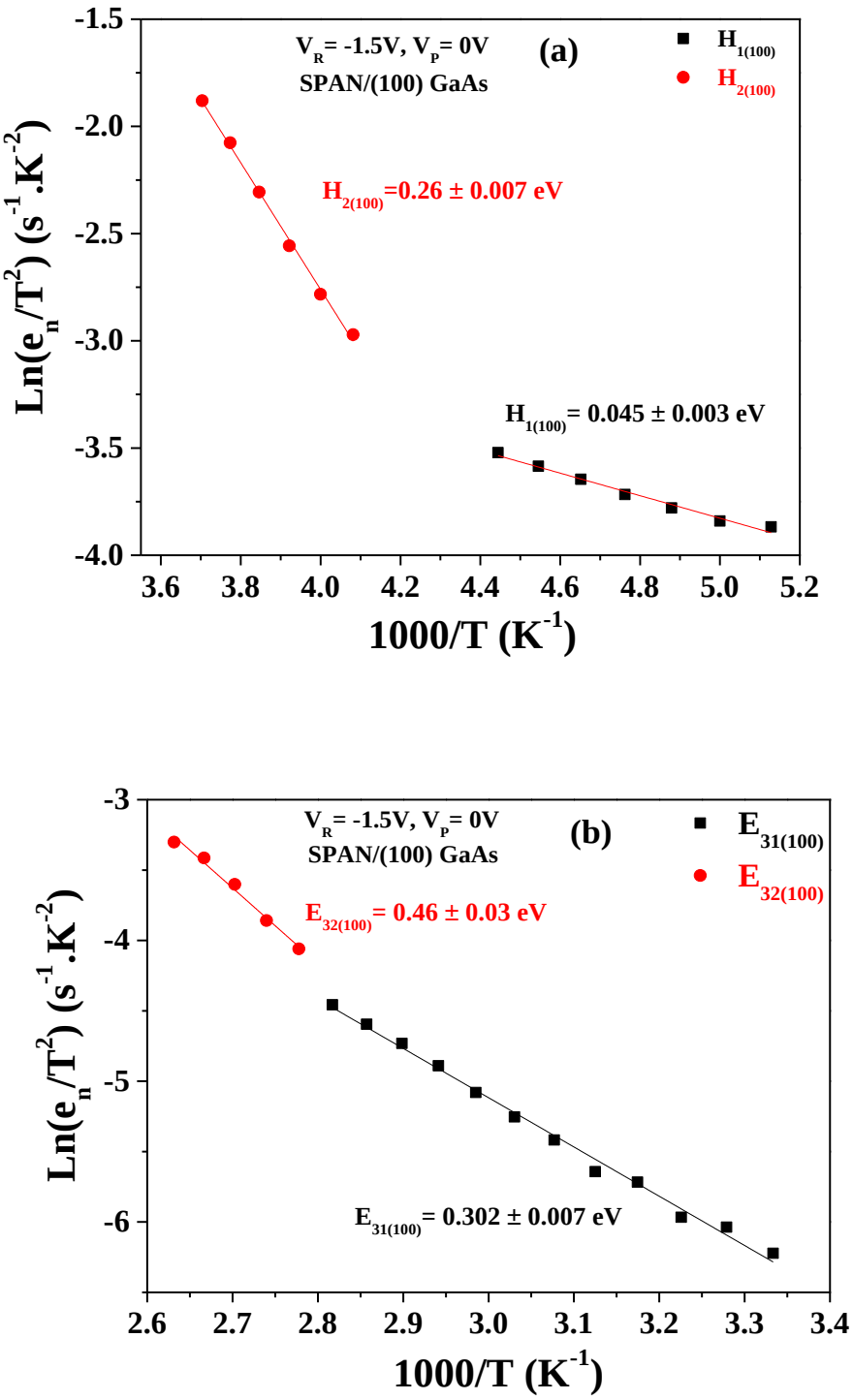

Fig. 9: Arrhenius plots determined from LDLTS data of SPAN grown on (100) GaAs hybrid devices using a revers bias of V_R = -1.5V, V_P = 0V and t_P = 1msec, in order to probe the electrically active traps away from interface (a) hole traps which originate from polymer and (b) electron traps which are present in the (100) GaAs substrate.

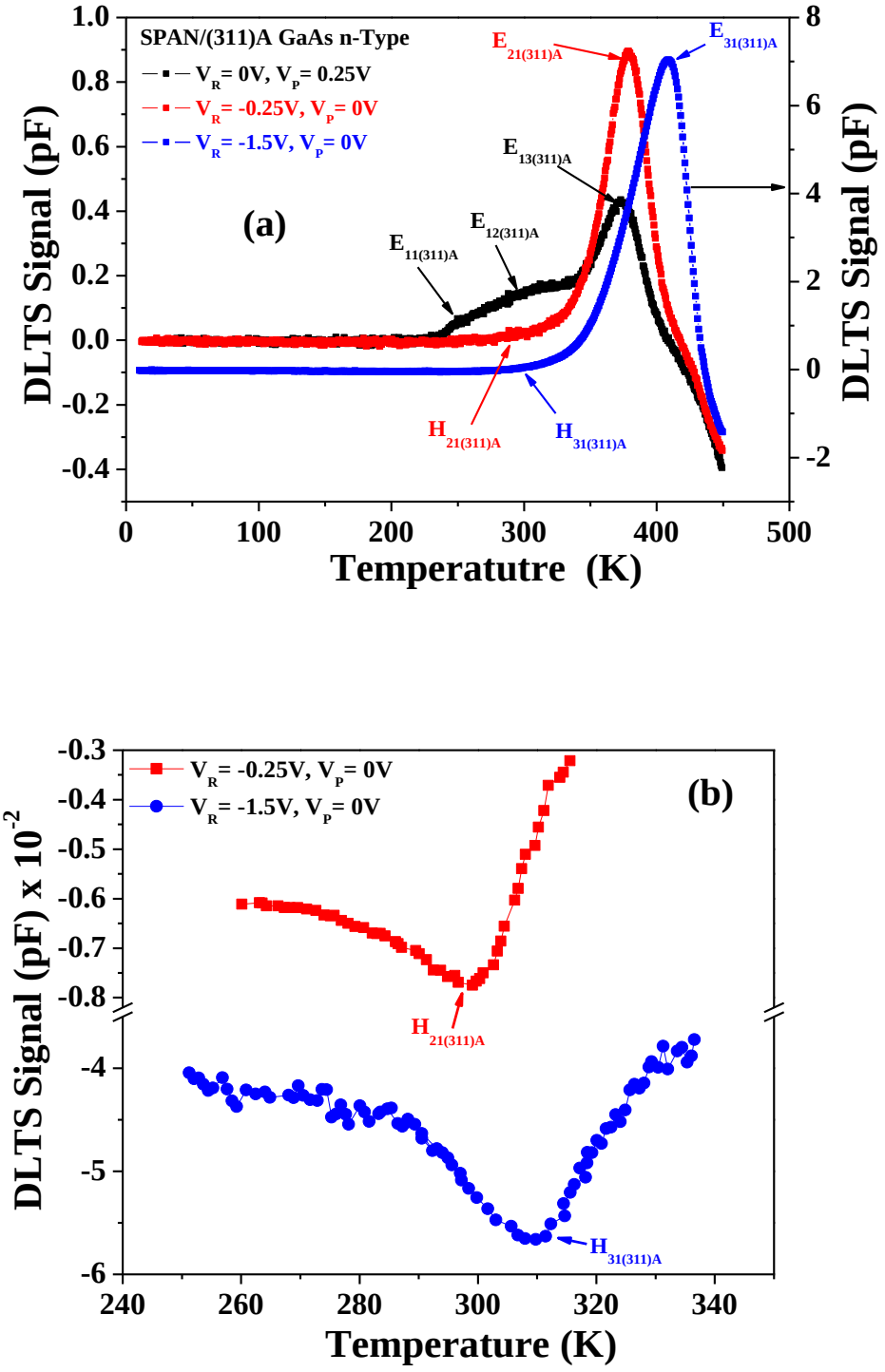

Fig. 10: (a) DLTS measurements of SPAN/(311)A samples at different reverse biases from V_R = (0, -0.25V) and V_P = (V_R + 0.25V) to V_R = -1.5V and V_P = 0V. The filling pulse characteristics were: t_p = 1msec, and rate window = 200s^{-1} and (b) For clarity the low temperature peaks are shown for reverse bias V_R = -0.25V and -1.5V.

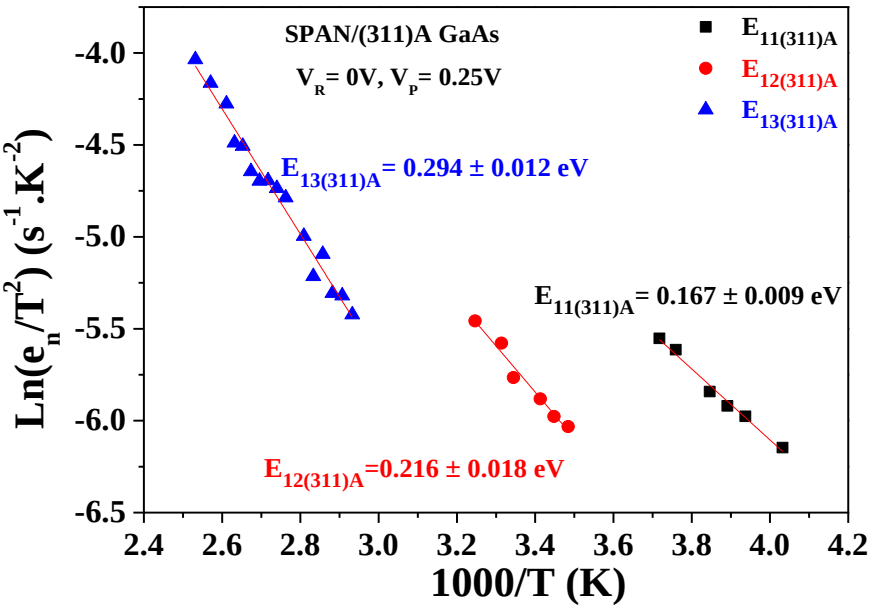

Fig. 11: Arrhenius plots derived from Laplace DLTS spectra of SPAN/(311)A GaAs samples at reverse bias V_R = 0V and V_P = 0.25V.

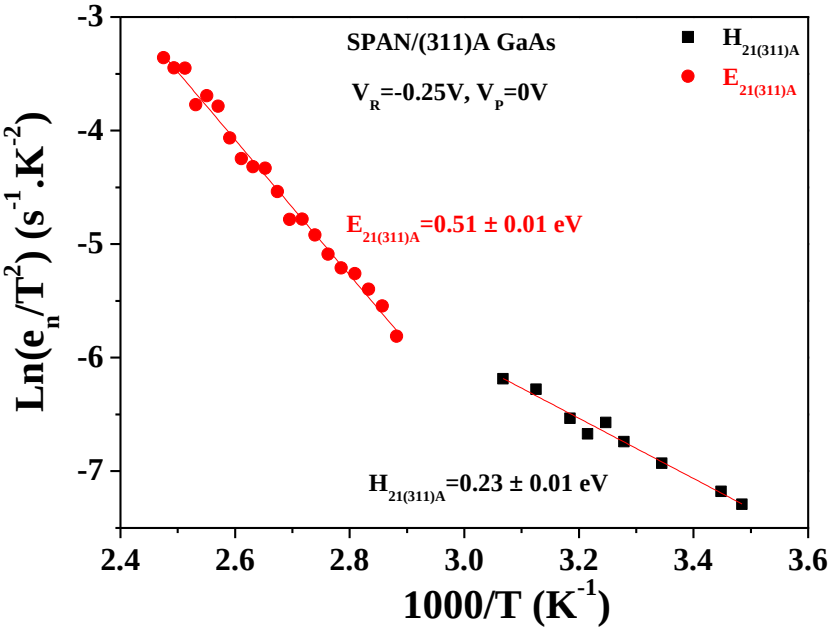

Fig. 12: Arrhenius plots obtained from Laplace DLTS for hole and electron traps detected in SPAN/(311)A GaAs samples at a reverse bias V_R = -0.25V and V_P = 0V.

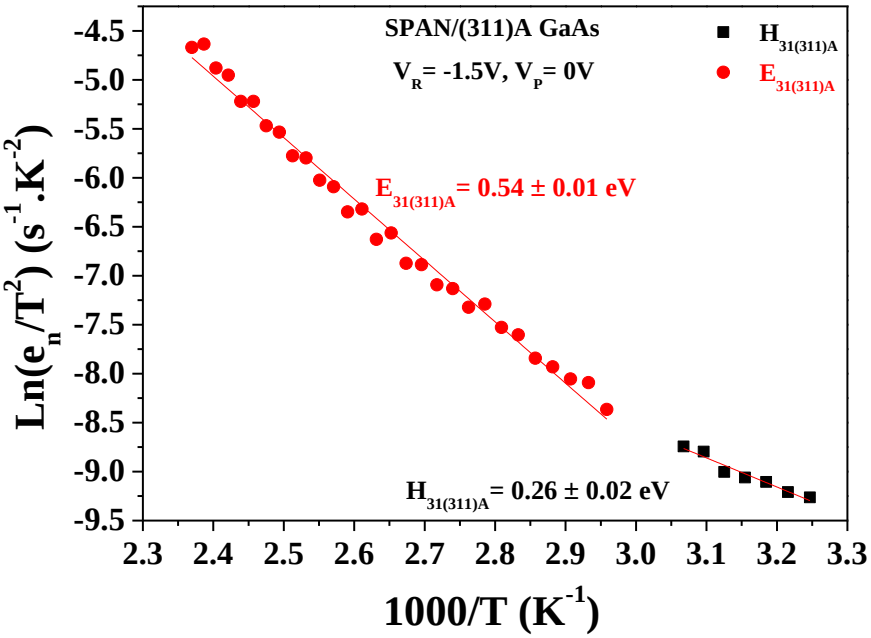

Fig. 13: Arrhenius plots derived from Laplace DLTS for hole and electron traps obtained in SPAN/(311)A GaAs samples at a reverse bias V_R = -1.5V and V_P = 0V.

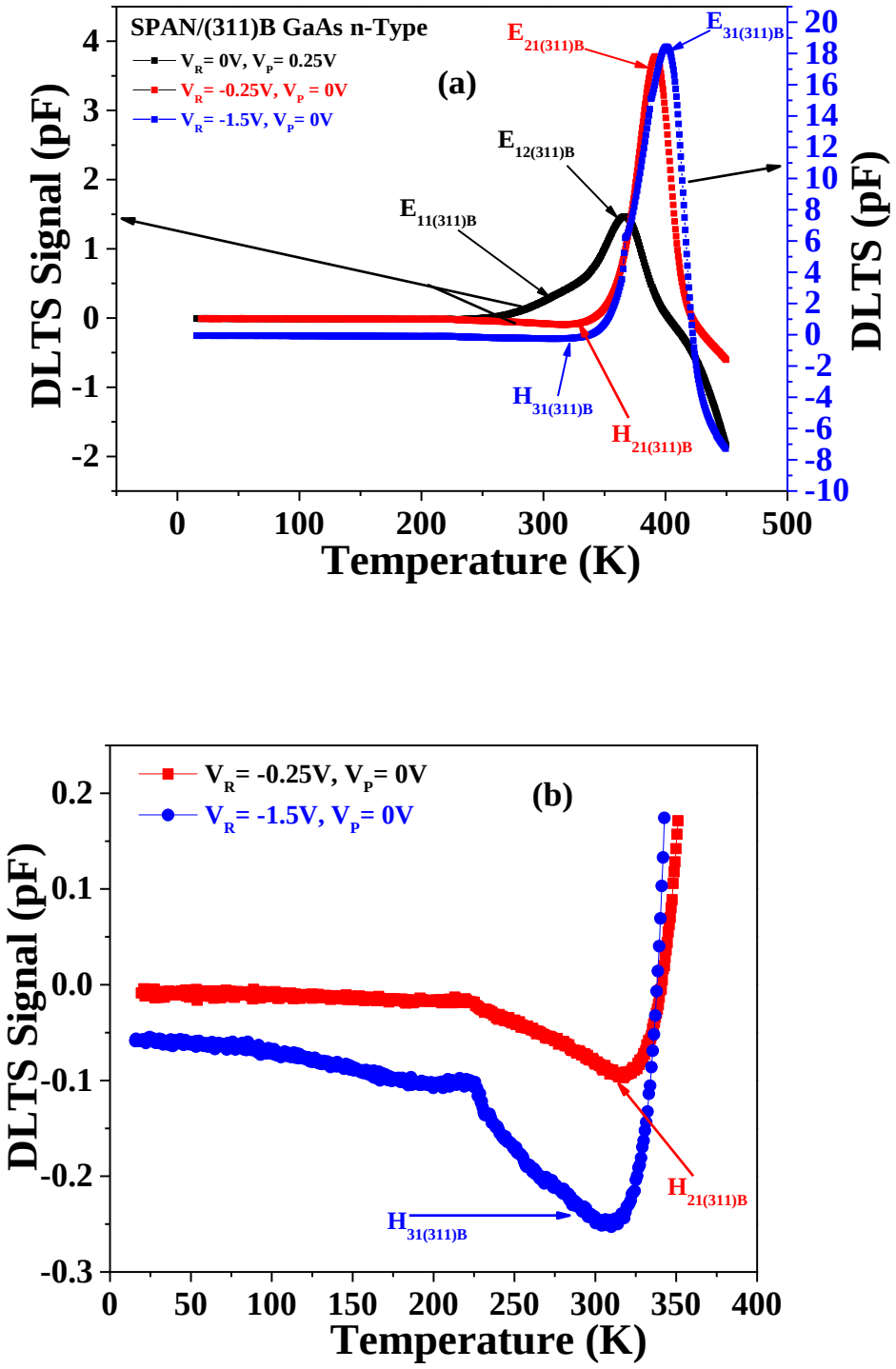

Fig. 14: (a) DLTS spectra of SPAN/(311)B samples at different reverse biases V_R = (0, -0.25, -1.5V) and V_P = (0.25, 0V). The filling pulse characteristics are t_p = 1msec, and rate window = 200s^{-1}; and (b) For clarity the low temperature peaks are shown for reverse bias V_R = -0.25V and -1.5V.

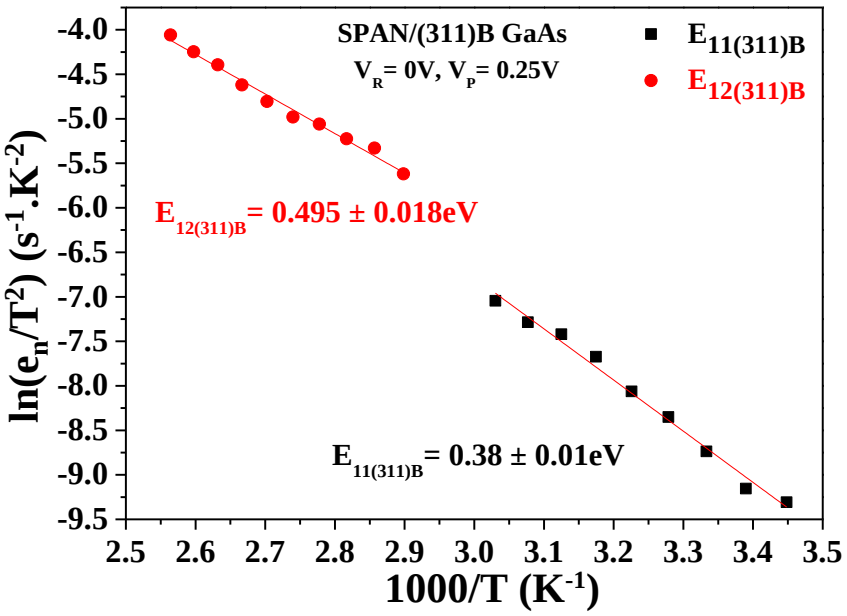

Fig. 15: Arrhenius plots obtained from Laplace DLTS data for SPAN/(311)B GaAs samples at reverse bias of V_R = 0V and V_P = 0.25V which allows probing the region at the interface of SPAN/(311)B GaAs heterojunction devices.

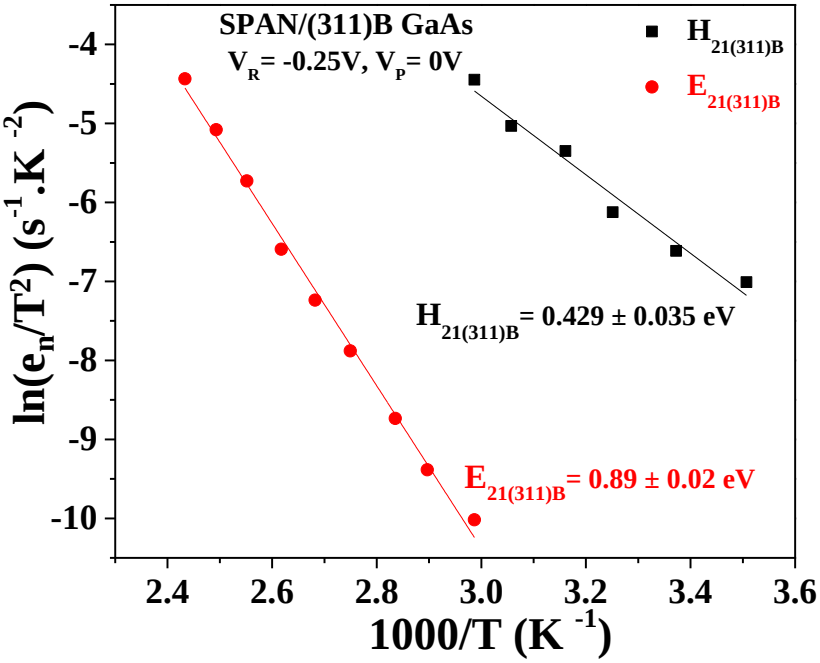

Fig. 16: Arrhenius plots derived from DLTS and Laplace DLTS data for SPAN/(311)B GaAs samples at reverse bias of V_R = 0V and V_P = 0.25V which allows probing the region close to the interface between SPAN and (311)B GaAs.

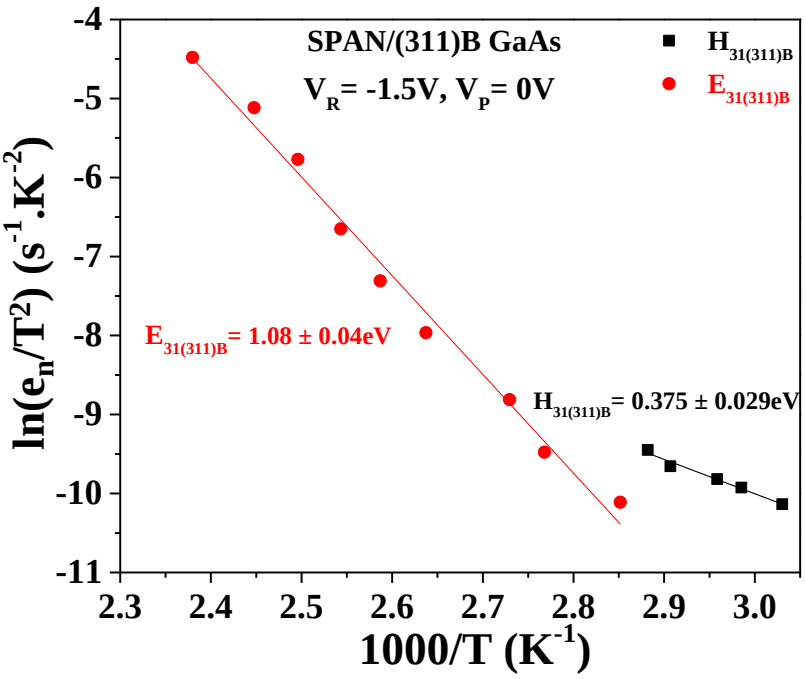

Fig. 17: Arrhenius plots obtained from DLTS and Laplace DLTS data for SPAN/(311)B GaAs samples at reverse bias of V_R = -1.5V and V_P = 0V which allows probing the region away from the interface of SPAN/(311)B GaAs heterojunction devices.

Table

Table 1: Summary of trap parameters for the three SPAN samples grown on n-type (100), (311)A and (311)B GaAs substrates for the following experimental conditions: (V_R = 0V, V_P = 0.25V), (V_R = -0.25V, V_P = 0V), and (V_R = -1.5V, V_P = 0V) and t_p=1msec.

Sample name with experimental conditions	Trap name	ET (eV)	Trap concentration (cm^{-3})
V_R=0V, V_P=0.25V SPAN/(100) GaAs	$E_{11(100)}$	0.027 ± 0.002	$5.23x10^{14}$
	$E_{12(100)}$	0.103 ± 0.007	$9.04x10^{14}$
	$E_{13(100)}$	0.167 ± 0.005	$5.24x10^{15}$
V_R=-0.25V, V_P=0V SPAN/(100) GaAs	$E_{21(100)}$	0.053±0.003	$4.521x10^{14}$
	$E_{22(100)}$	0.207 ± 0.007	$7.82x10^{15}$
V_R=-1.5V, V_P=0V SPAN/(100) GaAs	$H_{1(100)}$	0.045 ± 0.003	$6.88x10^{15}$
	$H_{2(100)}$	0.26 ± 0.007	$1.40x10^{16}$
	$E_{31(100)}$	0.302 ± 0.007	$1.26x10^{15}$
	$E_{32(100)}$	0.46 ± 0.03	$1.30x10^{15}$
V_R=0V, V_P=0.25V SPAN/(311)A GaAs	$E_{11(311)A}$	0.167 ± 0.009	$4.04x10^{14}$
	$E_{12(311)A}$	0.216 ± 0.018	$1.87x10^{15}$
	$E_{13(311)A}$	0.29 ± 0.001	$7.32x10^{14}$
V_R=-0.25V,V_P=0V SPAN/(311)A GaAs	$H_{21(311)A}$	0.23 ± 0.01	$1.41x10^{15}$
	$E_{21(311)A}$	0.51 ± 0.01	$1.92x10^{16}$
V_R=-1.5V, V_P=0V SPAN/(311)A GaAs	$H_{31(311)A}$	0.26 ± 0.02	$1.34x10^{15}$
	$E_{31(311)A}$	0.54 ± 0.01	$1.77x10^{17}$
V_R=0V, V_P=0.25V SPAN/(311)B GaAs	$E_{11(311)B}$	0.38 ± 0.01	$4.97x10^{15}$
	$E_{12(311)B}$	0.495 ± 0.018	$2.68x10^{16}$
V_R=-0.25V,V_P=0V SPAN/(311)B GaAs	$H_{21(311)B}$	0.43 ± 0.04	$1.3x10^{15}$
	$E_{21(311)B}$	0.89 ± 0.02	$4.31x10^{16}$
V_R=-1.5V, V_P=0V SPAN/(311)B GaAs	$H_{31(311)B}$	0.37 ± 0.03	$6.94x10^{14}$
	$E_{31(311)B}$	1.08 ± 0.04	$2.15x10^{17}$