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Harmonics and unbalanced load compensation by a modular multilevel cascaded converter active power conditioner

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Abstract: This paper presents a novel control scheme for a modular multilevel cascaded converter (MMCC) functioning as an active power conditioner (APC) to control the reactive power, eliminate the current harmonics, and compensate unbalanced load current simultaneously. This combines a modified predictive current controller with the inter-cluster and intra-cluster voltage balance control for MMCC sub-module capacitors. Simulation studies of this MMCC-APC for a power network containing both an unbalanced thyristor controlled rectifier and a reactive load are performed and results verifying its performance under varying degrees of load current distortion measured by THD levels are presented.

1 Introduction

Recent years have seen a proliferation of power electronics device applications, resulting in an increasing number of non-linear loads connected to power systems and consequently high levels of current harmonics (i.e. 5th, 7th, and 11th) in distribution networks. These currents lead to an increase in winding copper losses, reducing conductor current transmission capability, and life time [1]. Another issue in the distribution network is the supplying of unbalanced load current. This is often due to large single-phase loads such as traction drives, arc furnaces, and switch-mode power supplies [2]. Moreover, renewable energy-sourced generators which connecting on different phase lines may frequently inject unequal phase power hence causing unbalanced current. Harmonic extraction techniques have been proposed and are reviewed in [3, 4]. Generally, either tuned passive filters or power electronic-based active filters can deal with the problem. Disadvantages of the former include aging of components, limited compensating capabilities, resonance effects, and inflexibility regarding the orders of harmonics needing to be compensated [5]. Power electronic-based active filters (APF) have been proposed to address these issues [6]. These are mainly based on using voltage source converters (VSC) to inject an anti-phase but equal magnitude current to the point of common coupling (PCC) and hence achieve cancellation. Methods of dealing with load current imbalance have also been actively researched [7], and the general approach also involves using the VSC-based Static Compensator (STATCOM) with a control method that identifies and actively eliminates the negative sequence component in the line current, hence re-balancing the three-phase current at the PCC.

Most STATCOMs are based on the conventional two-level (2L) VSCs, which require high switching frequencies and higher voltage stress in medium-voltage power system applications. Recent development has seen a new family of topologies known as the modular multilevel cascaded converter (MMCC) being proposed to cope with these issues [8]. The MMCCs have the advantages of modularity, flexibility, and reliability. Most importantly, they can generate a good quality output waveform with low switching frequency.

However, a well-known challenge in the MMCC-based applications is the DC capacitor voltage unbalancing, which falls into two categories: one is the intra-cluster DC capacitor unbalance, due to the converter producing current harmonics which cause the sub-module isolated DC capacitors to charge and discharge unequally. The other unbalance occurs when dealing with the unbalanced load current compensation between the three MMCC phase legs, called inter-cluster unbalance [9]. For the former, the author proposed a carrier-swap technology to achieve DC capacitor voltages balanced at the nominal value [10]. However, for the latter, the DC capacitor voltage imbalance occurs both between clusters and every individual DC capacitor. This is owing to the average active power flowing through the MMCC three-phase limbs not being balanced, resulting in an unavoidable circulating current flowing within the converter and leading to voltage imbalance of the DC capacitors. For a star connected MMCC and with line current of low harmonic corruptions, the problem can be effectively alleviated by injecting a common zero sequence sinusoidal voltage V_0 into the converter phase limbs to cancel out the unbalanced power components [11, 12]. However, when load current contaminated with low-order harmonics, this scheme may become less effective. Assessment and further improvement are, therefore, required.

This paper presents a novel application for the MMCC as an active power conditioner (APC) [9] achieving the following functions simultaneously: eliminating the current harmonics, rebalancing the unbalanced load current, and compensating reactive power to the grid. The objective is to maintain a balanced and sinusoidal three-phase current at the PCC. A modified predictive current controller is applied for accurate reference current tracking. Simulation studies are presented for the control strategy applied to an MMCC-APC consisting of two full-bridge three-level flying capacitor converters per phase. The results are compared with the cases when harmonic levels measured by THD are different.

2 System configuration

The structure of the power system with MMCC-based APC is shown in Fig. 1. V_{S_ABC} at Bus 1 represents the grid three-phase voltage source; Bus 2 is the system PCC connected with the MMCC and a load bus. The load consists of a three-phase thyristor-controlled rectifier and an R–L load. The former draws different levels of current with harmonic components from the grid according to the phase angle values. To create unbalanced load current, an extra resistance R is inserted at the phase A input terminal of this load.

The MMCC-based APC in Fig. 1, uses a three-level (3L) flying capacitor converter (FCC) as the basic sub-module (SM). Each of its three phases has two SMs connected in series, and three phases are connected together to form a single-star configuration. An SM consists of eight transistors, three capacitors, one is SM DC

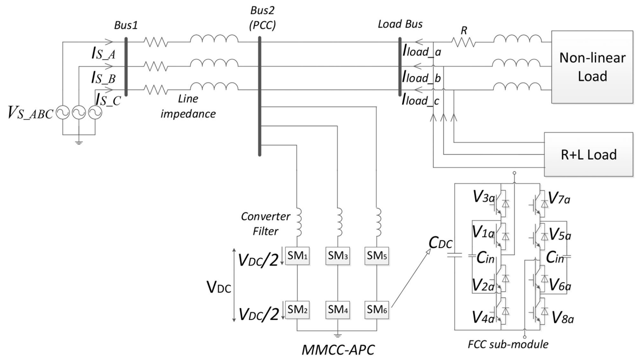

Fig. 1 *MMCC APC circuit and power system diagram*

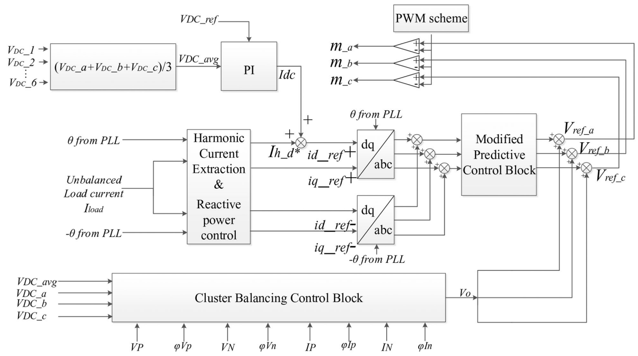

Fig. 2 *Overall control block diagram*

capacitor $C_{\rm DC}$ and two flying capacitors $C_{\rm in}$. The FCC will synthesise five voltage levels, i.e. $\pm V_{\rm DC}$, $\pm(1/2)V_{\rm DC}$ and 0 V. With two such SMs per phase, there are nine voltage levels including zero voltage. The number of sub-modules may vary according to the PCC voltage and SM voltage ratings. Having multiple SMs per phase, higher AC voltage magnitudes and lower switching frequencies hence also lower switching losses can be achieved simultaneously.

3 Control strategies

The overall control scheme is shown diagrammatically in Fig. 2, which is divided into three main parts:

- The negative sequence and harmonic currents extraction for reference current generation;
- The modified current predictive control which enables accurate and fast tracking of reference current;
- The intra-cluster and inter-cluster voltage balancing controls due to harmonics and unbalanced load current compensation.

3.1 Negative sequence and harmonic current extraction

Cancellation of the load current harmonics and re-balancing the unbalanced load current require extraction of negative sequence and harmonic current components from the unbalanced load current. These are taken as the reference components to be eliminated by the MMCC current controller, so that only fundamental positive sequence current is supplied at the PCC as shown in Fig. 3.

The procedure first applies Fortescue's theorem to decomposing the measured three-phase unbalanced load currents into balanced positive and negative sequence elements. The results are then transformed into equivalent synchronous rotating reference frame (SRRF) representations via the Park transformation namely, $I_d^{\pm}$ and $I_q^{\pm}$ Note in this application, the three-phase voltage at the PCC is assumed balanced hence it is taken as the reference vector and its phase angle θ is estimated by a phase-locking loop (PLL). A set of $(h-1)$ order harmonics remains in the $I_d^{\pm}$ and $I_d^{\pm}$ where h denotes the three-phase AC current harmonics order; subsequently, the

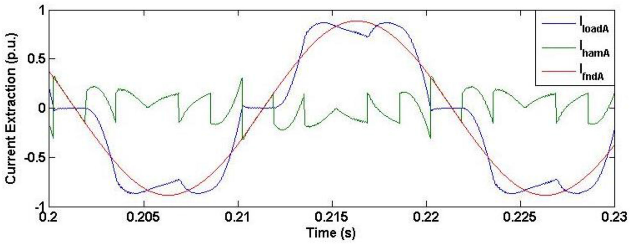

Fig. 3 *Current harmonics extraction from phase-A load current*

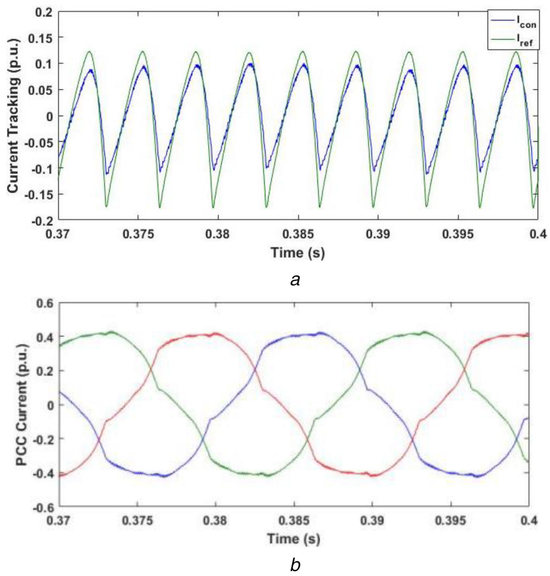

Fig. 4 *Reference tracking*

(a) Converter current reference tracking and ***(b)*** Three phase PCC current without modification

harmonic current in the positive d complex component is extracted as $I^{+}_{d\_\rm ref}$ via a first-order low-pass filter (LPF) with cut-off frequency f_0 chosen around 100 Hz, thus the harmonics of the third order and above can be filtered completely. Finally, the positive q element and negative d-q components, which include both fundamental and harmonics, taken as $I^{+}_{d\_\rm ref}$ and $I^{-}_{dq\_\rm ref}$ are combined with the harmonic components $I^{+}_{d\_\rm ref}$ to form the reference current supplying to MMCC current controller as shown in Fig. 2.

3.2 Modified current predictive control

The reference currents are time varying periodical quantities at steady-state and the rates-of-changes can be high due to the harmonic components. High performance current control at both steady and transient states requires the MMCC current controller having fast reference tracking capability. With the conventional one-step ahead predictive controller, it has an inherent one sample delay feature which prevents fast and accurate current tracking particularly when reference current changes. An example is as shown in Fig. 4, the conventional predictive controller could not give accurate peak reference current tracking and the resultant currents on PCC are distorted.

In order to compensate the above-stated deficiency, a modification is made to the conventional predictive controller. This is done by changing the reference current applied to the controller; instead of using the reference current obtained at the kth sample instant only, the derivative of reference current is evaluated using reference currents of the current of both last samples and the current sample times. Thus, the new reference current for the compensator is as shown below.

$$\vec{i}^{*\prime}(k) = \vec{i}^{*}(k) + \tau\frac{\vec{i}^{*}(k) - \vec{i}^{*}(k-1)}{T_s} \tag{1}$$

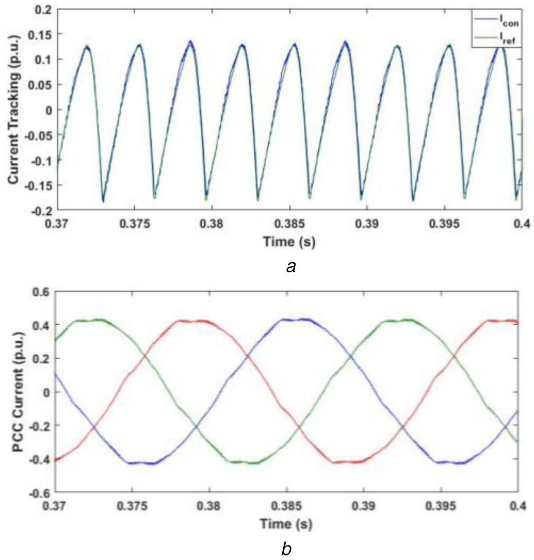

Fig. 5 *Reference tracking (τ = 0.12)*
(a) Converter current reference tracking and ***(b)*** Three phase PCC current with modification ($\tau = 0.12$)

A coefficient τ is applied to weight the derivative term, normally $0 < \tau < 0.5$ was found to be sufficient in all cases. Thus, according to conventional predictive controller formula and replacing reference current at kth sample by (1), the equations for positive and negative sequence voltages calculated at the kth sample can be derived as

$$\overrightarrow{V_{\mathrm{sh}}^{*}}^{\pm}(k) = \overrightarrow{V_{\mathrm{pcc}}^{*}}^{\pm}(k) - \left[\frac{L_{\mathrm{sh}}}{T_s} + \tau\frac{L_{\mathrm{sh}}}{T_s^2}\right]\overrightarrow{i^{*}}^{\pm}(k) + \tau\frac{L_{\mathrm{sh}}}{T_s^2} \times \overrightarrow{i^{*}}^{\pm}(k-1) + \left[\frac{L_{\mathrm{sh}}}{T_s} - \tau R_{\mathrm{sh}}\right]\overrightarrow{i}^{\pm}(k) \tag{2}$$

Fig. 5*a* shows the reference current tracking using the modified predictive current control scheme and (b) shows the three-phase PCC current obtained using this controller. The performance of the resultant current waveform is clearly better than the one shown in Fig. 4*b*.

3.3 Capacitor balancing control

3.3.1 Intra-cluster capacitor: The MMCC individual SM capacitor voltages may drift away from their nominal value even under balanced load conditions**,** due to load and switching pattern changes and converter switch losses. A controller is, therefore, used to maintain the DC voltage across each sub-module to its required value. This calculates the average value of the measured three-phase limb capacitor voltages as

$$V_{\mathrm{DC\_avg}} = \frac{V_{\mathrm{DC}\_a} + V_{\mathrm{DC}\_b} + V_{\mathrm{DC}\_c}}{3} \tag{3}$$

This value is compared with the required nominal $V_{\mathrm{DC\_ref}}$ and the error is applied to a $P + I$ controller to generate a reference current signal $I_{\mathrm{dc\_ref}}$. This is superimposed onto the d-component of the load reference harmonics current $I_{h\_d}^{*}$ so that to form the converter positive sequence reference current $I_{d\_\mathrm{ref}}{}^{+}$. It is worth noting that when SMs are FCCs, the voltage balancing of the SM inner floating capacitors can be achieved by using phase-shift PWM (PS-PWM) scheme [13], which enables natural balancing of inner floating capacitors.

3.3.2 Inter-cluster capacitor: When the load is unbalanced, the average active power flowing through MMCC three-phase limbs are not balanced as analysed below:

The converter phase voltage and current can be written as

$$V_{\mathrm{Sm}} = V_P\sin\left(\omega t + \phi_{Vp} - k \times \frac{2}{3}\pi\right) + V_N\sin\left(-\omega t + \phi_{Vn} - k \times \frac{2}{3}\pi\right) \tag{4}$$

(see (5))

where k is 0, 1, and 2 while m represents phases A, B, and C, respectively.

The product of (4) and (5) gives the powers per phase as (see (6))

In (6), $V_P I_P$ and $V_N I_N$ represented as P_{Sm}^{++} and P_{Sm}^{--}, are, respectively, means the balanced positive sequence and negative sequence voltage current products, which denote converter losses and filter components losses. $V_P I_N$ and $V_N I_P$ denoting as P_{Sm}^{+-} and P_{Sm}^{-+} are the unbalanced powers. They lead to the active power in the converter three phases' unequal, hence causing phase limb DC voltages drifting away from their nominal values. Consequently, the APC cannot function accurately to compensate reactive power or cancel current harmonics under imbalance condition.

To overcome the above-stated issue, an inter-cluster balancing control method [14] is applied. Its block diagram is as shown in Fig. 2 overall control block diagram. A common zero sequence voltage V_{o} is injected into the converter each phase to cancel the above cross coupling terms, hence the new phase voltage is shown as

$$V_{\mathrm{Cm}} = V_{\mathrm{Sm}} + V_o\sin(\omega t + \phi_o) \tag{7}$$

and the power equation is

$$P_{\mathrm{Cm}} = \frac{1}{2}\left[P_{\mathrm{Sm}}^{+-} + P_{\mathrm{Sm}}^{-+} + V_{\mathrm{o}} I_P\cos\left(\phi_{\mathrm{o}} - \phi_{\mathrm{Ip}} + k \times \frac{2}{3}\pi\right) - V_{\mathrm{o}} I_N\cos\left(\phi_{\mathrm{o}} + \phi_{\mathrm{In}} - k \times \frac{2}{3}\pi\right)\right] \tag{8}$$

Note V_{Cm} and P_{Cm} are the converter phase voltage and phase active power including zero sequence voltage component, while $V_{\mathrm{o}} I_N$ part represents P_{Cm}^{o+} and $V_{\mathrm{o}} I_N$ part represents P_{Cm}^{o-}. This control scheme detail is revealed in the block diagram in Fig. 6.

Consequently, a summation of $(P_{\mathrm{Sm}}^{+-} + P_{\mathrm{Sm}}^{-+} P_{\mathrm{Cm}}^{o+} P_{\mathrm{Cm}}^{o-})$ equals to zero can ensure that P_{Cm} to be equal and achieve cluster phase balanced. The corresponding zero sequence voltage magnitude V_{o} and its phase shift angle ϕ_{o} are calculated in (9) and (10).

$$V_{\mathrm{o}} = \frac{2P_{\mathrm{CA}} - X_{a3}}{\cos\phi_{\mathrm{o}} \times X_{a1} + \sin\phi_{\mathrm{o}} \times X_{a2}} \tag{9}$$

$$\phi_{\mathrm{o}} = \tan^{-1}\left(\frac{X_{a1}(2P_{\mathrm{CB}} - X_{b3}) - X_{b1}(2P_{\mathrm{CA}} - X_{a3})}{X_{b2}(2P_{\mathrm{CA}} - X_{a3}) - X_{a2}(2P_{\mathrm{CB}} - X_{b3})}\right) \tag{10}$$

$$I_{\mathrm{Sm}} = I_P\sin\left(\omega t + \phi_{Ip} - k \times \frac{2}{3}\pi\right) + I_N\sin\left(-\omega t + \phi_{In} - k \times \frac{2}{3}\pi\right) \tag{5}$$

$$P_{\mathrm{Sm}} = \frac{1}{2}\left[V_P I_P\cos(\phi_{Vp} - \phi_{Ip}) + V_N I_N\cos(\phi_{Vn} - \phi_{In}) - V_P I_N\cos\left(\phi_{Vp} + \phi_{In} + k \times \frac{2}{3}\pi\right) - V_N I_P\cos\left(\phi_{Vn} + \phi_{Ip} + k \times \frac{2}{3}\pi\right)\right] \tag{6}$$

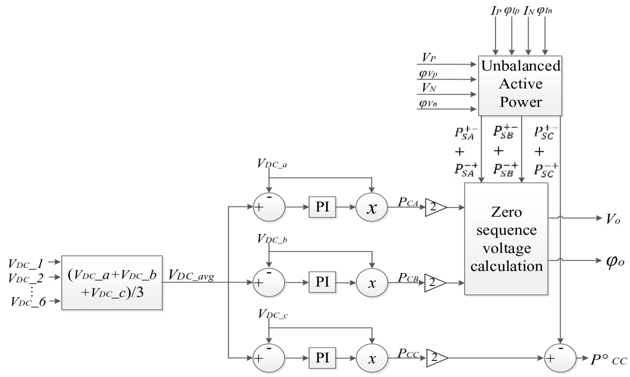

Fig. 6 *Cluster Balancing control block diagram*

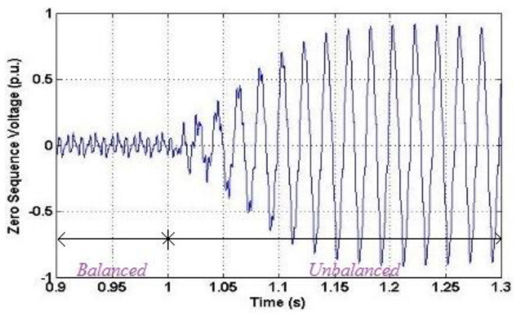

Fig. 7 *Zero sequence voltage waveform*

Table 1 MMCC-APC system rating

Components	Rating
3-Phase source voltage V_{pcc}	110 V
fundamental frequency f_0	50 Hz
switching frequency f_C	1 kHz
RL filter	1.0 Ω, 1.0 mH
SM numbers per phase	2
SM DC capacitor C_{dc}	1120 µF
SM flying capacitor C_{fc}	560 µF
nominal SM DC voltage V_{dc}	100 V
delay coefficient τ	5×10^{-5}
rated power S	3.3 kVA
non-linear Load	3-phase thyristor rectifier
firing angle α	0°; 30°; 60°
$R + L$ load	10.0 Ω, 48.0 mH
extra resistor R on phase A	5.0 Ω

Thus, the instantaneous zero sequence voltage expression is: $v_o = V_o \sin(\omega t + \phi_o)$ Fig. 7 shows the zero sequence voltage waveform in which amplitude becomes significant when the unbalanced load current is presented starting from 1.0 s. Since the APC generates anti-phase load current harmonics, the V_o will distort to some extent, but the injected V_o in each phase will be cancelled in the converter line-line voltage, hence will not affect the grid voltage.

4 Simulation results

The proposed system given in Fig. 1 and the corresponding control scheme are verified through SIMULINK/MATLAB. The system parameters are shown in Table 1: Three-phase voltage rating at PCC is 110 V, 50 Hz; the MMCC DC voltage rating is 200 V containing two SMs in each phase, while the main DC capacitor per SM is 200 V and the floating DC capacitors are rated at 100 V. The levels of harmonics in the load current can be varied by changing the firing angle α of the three-phase thyristor rectifier. The $R + L$ load is chosen to have a power factor of 0.8.

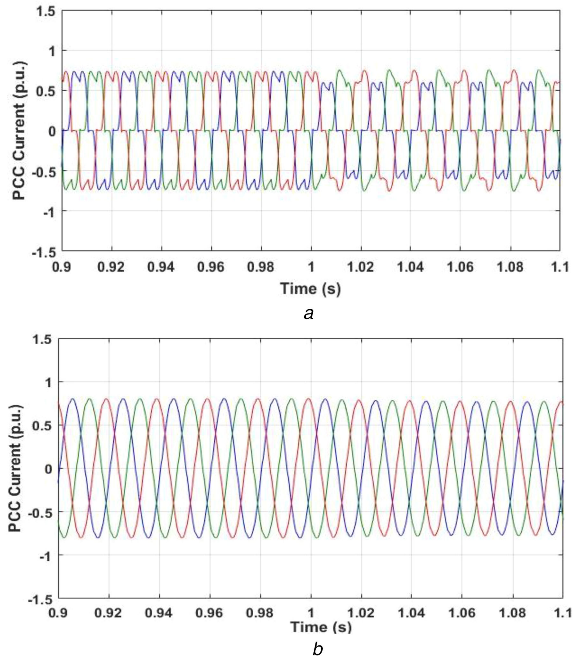

Fig. 8 *3-phase PCC current waveform*
(a) 3-phase PCC current without MMCC-APC compensation and ***(b)*** with MMCC-APC compensation

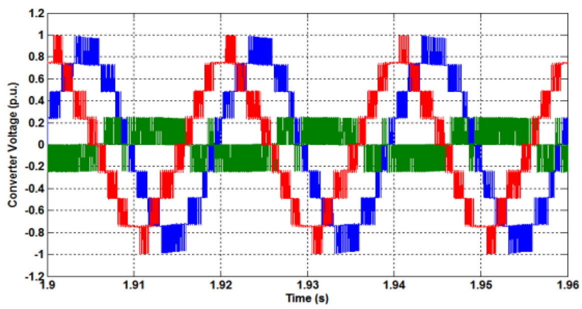

Fig. 9 *3-phase converter terminal voltage*

The fixed value resistor added on phase A line creates the load imbalance, and the degree of imbalance measured by the ratio of negative sequence current magnitude I_n to positive sequence current I_p is noted as $K_{ir} = I_n/I_p$ [11]. It is set around 45% in this work. The degree of K_{ir} that the MMCC can work with and achieve balanced operation depends on the converter voltage rating. Excessive level of load imbalance would lead to the MMCC working in over-modulation mode and hence malfunction.

Fig. 8 shows the three-phase currents at PCC with and without the MMCC-APC control when the load imbalance is imposed at 1.0 s. The distorted and unbalanced PCC current without the compensation is as shown in (a) and the waveforms in (b) show the PCC current with the MMCC-APC compensation, which is balanced and sinusoidal. Fig. 9 displays the PWM modulated MMCC three-phase voltage with the zero sequence voltage added. Clearly, they are unbalanced and with different harmonic spectra. Fig. 10 shows the six SMs DC voltage waveforms without the zero sequence voltage injection (Fig. 10*a*) and with the zero sequence voltage injection (Fig. 10*b*). The former cannot hold their voltages stable at the nominal level after 1.0 s when unbalanced load is connected.

In Fig. 11, the waveforms for the thyristor-controlled load firing angle changing from 0° to 30° at 1.2 s and to 60° at 1.3 s are presented: (a) shows the three-phase PCC voltage; (b) the compensated PCC current, which is clearly balanced, desirable and in phase with the voltage in (a); the corresponding unbalanced and distorted load current is shown in (c), while the level of distortion is increased with the firing angle increase; (d) and (e) represent the converter reference voltage and zero sequence voltage,

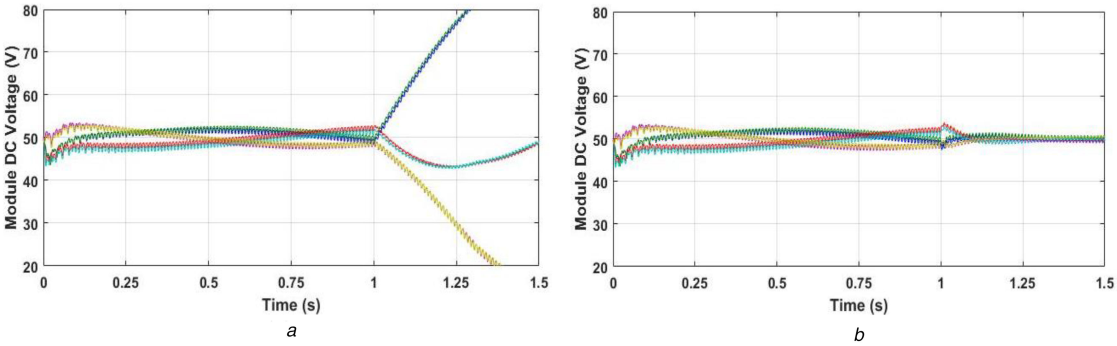

Fig. 10 *SM DC voltage*
(a) without zero sequence voltage injection and ***(b)*** with zero sequence voltage injection

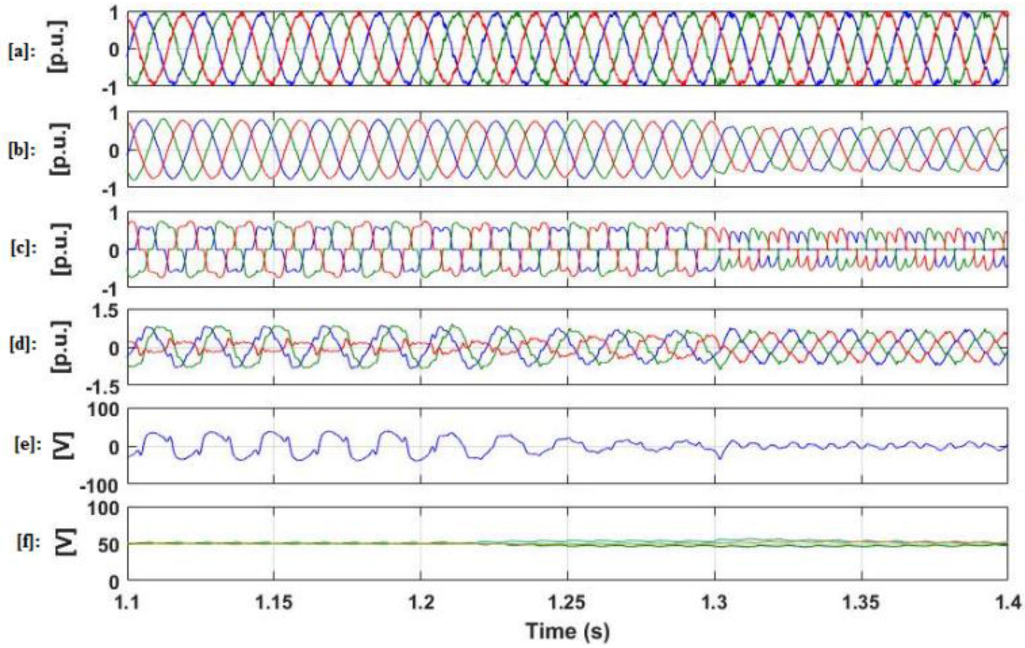

Fig. 11 *Operating results of the MMCC-APC compensation*

Table 2 Load current analysis

	I_n, p.u.	I_p, p.u.	K_{ir}	THD_A, %	THD_B, %	THD_C, %
0°	0.075	0.19	0.39	23	16	18
30°	0.042	0.25	0.17	27	25	26
60°	0.021	0.24	0.088	41	37	41

respectively; finally, Fig. 11*f* shows the six SMs DC voltages, which are maintained to their nominal levels as expected. The total harmonic distortions (THD) and K_{ir} of the load current at different firing angles shown in Fig. 11 are presented in Table 2.

There are two points worth noting: on the one hand, the PCC current can be controlled by the MMCC-APC rapidly and smoothly under the unbalanced condition plus various harmonic distortion levels due to the firing angle changing from 0° to 60°. On the other hand, with the load unbalance caused by load-side phase impedance discrepancies, where the load is a significant harmonic generating source, Table 2 illustrates that increasing the harmonic distortion level may actually reduce the level of load fundamental current unbalance. The negative sequence current changes from 0.075 to 0.021 p.u. while positive sequence current increases from 0.19 to 0.24 p.u., hence K_{ir} decreases from 0.39 to 0.088, current becomes more balanced. Consequently, the zero sequence voltage required in Fig. 11 reduces since the MMCC module voltages can be balanced.

5 Conclusion

This paper has shown that the proposed MMCC-APC can compensate simultaneously unbalanced and harmonic corrupted load current as well as reactive power. The proposed novel control scheme achieves high performance reference current tracking using a modified predictive current controller. Combined with an inter-cluster and intra-cluster voltage balancing schemes it prevents the converter sub-module capacitor voltage from drifting away. The results also show that under unbalanced load conditions, the harmonic components in the load current may alleviate the degree of load unbalance, hence extending the MMCC-APC operating range and performance.

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