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Polydimethylsiloxane as Polymeric Protective Coating for Fabrication of Ultra-Thin Chips

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Abstract

The bendable silicon-based ultra-thin chips (UTCs), with thickness below 50 µm are needed to provide high-performance flexible electronics for several emerging applications ranging from flexible displays to robotic e-skin. The UTCs from standard silicon wafer are obtained by etching the bulk material from the backside of the wafer using a wet chemical etchant. During the etching process, it is imperative to protect the front processed side from the etchant as in most cases, the etchant is incompatible with the metals and other materials used in the fabrication of devices. This paper reports a new method using polydimethylsiloxane (PDMS) as the protective coating during wet etching of silicon. The silicon sample is thinned to sub-25 µm thickness using Tetramethylammonium hydroxide (TMAH), while PDMS acting as a protective coating, which is removed after thinning by using a chemical composition involving a nucleophilic attack on siloxane bond. As a bulk material with low-temperature processing requirements, PDMS offers an interesting alternative to other commercially available materials. The presented approach offers a range of advantages compared to other polymeric materials that are being used for the above-mentioned purpose.

Keywords: Ultra-Thin Chips; Wet Etching; PDMS; Polymeric Protection.

1. Introduction

The immense growth in microelectronics have revolutionised the modern era and with the fast pace of advancement, it is expected to open new application areas. For example, over the past few years, we have seen the transformation of Moore's Law towards more Moore and More than Moore [1]. With fast approaching physical limits of transistor scaling, there is a need to look for non-traditional methods such as 3-dimensional (3D) integration or vertical devices etc. to improve the device performance [2, 3]. According to the International Technology Roadmap for Semiconductors (ITRS) report, conventional transistor density scaling is likely to end by 2021 and will be replaced by 3D stacking and vertical interconnection scheme such as through-silicon vias [4]. To this end, the wafer thinning is being explored to obtain UTC with a thickness less than 50 µm to accommodate more functional chip in limited vertical space [5, 6]. Moreover, with reduced flexural rigidity the UTCs can bend and conform to the curvy substrates. Thus, they can meet the high-performance flexible electronics requirements of several emerging applications such as internet of things, flexible displays, robotics, and smart cities, etc.[7-9]. Due to reduced substrate parasitic capacitance, the UTCs could also exhibit superior performance than their bulk counterparts[10]. Furthermore, the possibility to tune the response of devices on UTCs with controlled bending offers a new path for addressing challenging issues such as drift compensation and mobility variation in conventional devices [11-13].

In a standard industrial process flow, the UTCs are obtained by back-grinding of semiconductor wafers after front end manufacturing and before the integration of silicon chips into packages [2, 3, 14]. Due to issues such as wafer warping, fragility, and inducement of deep sub-surface damages, which could reduce the chip strength, the back-grinding is used to thin the wafers down to about 100µm. Thus, a range of other methods have been explored for further thinning of the wafers, as discussed in recent review articles [2, 15, 16]. These involve a combination of mechanical grinding, dry and wet

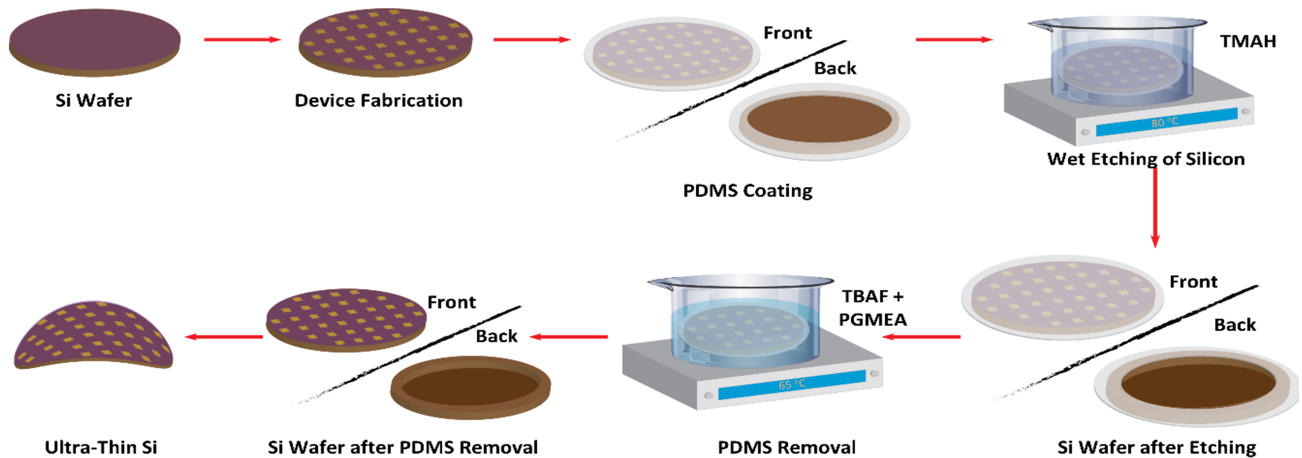


Figure 1.: Illustration of the process followed to realise ultra-thin silicon using a PDMS as protective layer.

chemical etching etc. The wet chemical etching, which is an important pillar for the development of microelectromechanical systems (MEMS) devices, offers an attractive, tuneable, and batch level processing capability for realising UTC [3].

The thinning methods require the front side of the wafer to be well protected during the removal of semiconductor material from the backside. For example, during wet etching, the leakage of the etchant on the frontside could damage the devices. To address these issues, one of the basic arrangements that is currently used during chemical etching is to place the wafer in Teflon based holders with rubber O-ring. In this arrangement, the latter acts as a sealant and prevents the etchant from reaching the front side. Further, the holder is used in combination with a hard mask for the backside to prevent the sipping of the etchant due to undercutting [17]. Silicon dioxide (SiO_2) and Silicon Nitride (SiN) are widely used for this purpose as they provide good selectivity to the etchant. However, due to the likelihood of the presence of pinholes in SiO_2/SiN hardmask, protection is not guaranteed. Any pinhole formation during thinning can provide the path for etchant to leak on the front side and hamper the functionality of the devices. A few works using metals such as gold, chromium, and titanium, deposited by e-beam evaporation or sputtering have been reported to address this issue [18]. However, the poor adhesion of metal with the substrate, in many such cases, allows the etchant to creep underneath the edges, causing the mask to peel or bubble off. Further, the small contaminants on the wafer surface could lead to the formation of large blisters [19]. The SiN and metal layers also exhibit high young's modulus values and so produces high stress on the underlying thin silicon as the thinning progress. The malfunction of O-ring could also lead to the etchant seeping onto the front side. To address the above-mentioned issue, often the front side is coated with commercially available polymers (e.g. ProTEK® B3). Such polymeric compositions are expensive, require curing temperature up to 210ºC, and their removal after the backside etching is cumbersome [20, 21]. For this reason, other polymers such as poly(methyl methacrylate) (PMMA) have also been used and have been shown to be resistant towards potassium hydroxide (KOH) [22, 23]. But the protection capability of PMMA decreases with the etchant temperature and can only last for 32 minutes when the temperature goes above 80ºC [22]. Similarly, other materials such as a photo-sensitive spin-on polymer divinylsiloxane benzocyclobutene (BCB), which have been explored for backside protection, tend to peel off under long KOH etches due to local stress generated during the curing process [18, 24]. Nonetheless, the polymer as a protection layer during bulk micromachining is still an attractive technique, as it does not introduce any (or minimal) mechanical stress. Considering the shortcomings associated with above mentioned techniques, an ideal protective coating should have low value of young's modulus, low temperature processing requirements, cost-effective, can tolerate temperature upto 100ºC and be resistive towards etchant for a long duration, and can easily be applied and removed without any residues. We have found that the commonly used PDMS could address these shortcomings and provide an easy and cost-effective polymeric protection during wet etching of silicon.

This work presents the investigations related to the compatibility of PDMS as the protective frontside coating during Si wafer etching using TMAH. The readily available PDMS, is cheaper than other alternatives and requires lower processing temperature (~80ºC), and introduces minimal stress during the thinning process because of its low Young's Modulus [30]. Extending its usability, we are using PDMS for protecting the frontside of the wafer from alkaline etchant during prolong etching.

This paper is organised in six sections. Section II presents the fabrication of test devices (e.g. capacitors) and the post-

Table 1. Comparison between different materials used as etch mask or front side protection.					
	ProTEK B3	**LPCVD Nitride**	**Metal (Ti)**	**PMMA in $CHCl_3$**	**PDMS**
Price per 2" wafer (in USD)	3.96	25	16	0.55	0.465
Processing Temperature	205	400	RT	90	80
Primer Requirement	Yes	No	No	No	No
Primer price/ litre (in USD)	300	NA	NA	NA	NA
Remover	ProTEK remover	o-phosphoric acid	$NH_3 + H_2O_2$ + DI	Acetone	TBAF+ PGMEA
Shelf life	1 year	NA	NA	1 year	2 year
Young' Modulus	3.1 ± 0.47 GPa [25]	222 ± 3 GPa [26]	90 GPa [27]	3.5 GPa [28]	2.61 ± 0.021 MPa [29]

processing steps followed to realise the thin silicon-based devices. The PDMS removal technique and the etch chemistry are discussed in detail in Section III. The electrical characteristics of the devices before and after thinning are presented briefly in Section IV. This is followed by Section V where the test experiment performed over PDMS to check the effect of etchant is described. Finally, the key outcomes of the paper are summarized in Section VI.

2. Device Fabrication and Post-Processing

The capacitive test structures, using silicon dioxide as dielectric, were fabricated on a 2-inch silicon wafer of thickness ~300 µm. The wafer was cleaned by standard cleaning process using acetone, isopropyl alcohol (IPA) and deionised (DI) water. The 500 nm thick dielectric was deposited using plasma-enhanced chemical vapor deposition (PECVD) and the electrodes were realised by evaporating 20nm/100 nm stack of nichrome and gold, followed by lithography and patterning. For the frontside protection layer, PDMS was mixed with curing agent in 10:1 ratio and degassed in a vacuum desiccator for 30 minutes to remove any air bubbles created during mixing. It was then spin- coated over the front-side of the wafer (i.e. on top of capacitive test structures) with speed of 1500 rpm for 1 minute and the sample was cured at 80ºC for 1 hour. The thickness of the PDMS was measured to be ~50 µm, using surface profilometer. Following this, the backside etch window was defined by applying PDMS at the rim of wafer and cured. An image of the sample's backside after curing is shown in Fig. 2(a). Often high-quality masking layer using SiN or SiO_2 or stack of them is used to define the etch window.

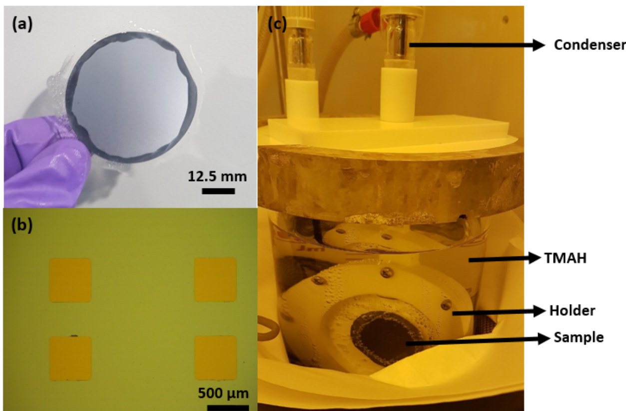


Figure 2: Image of (a) wafer backside showing the etching window defined using PDMS; (b) optical image of capacitive device on frontside; and, (c) the etching setup.

However, the high temperature needed by the deposition tools such as low-pressure chemical vapour deposition (LPCVD), to obtain such a high-quality masking layer, can induce unwanted thermal stress. Moreover, LPCVD deposition on both sides of the wafer makes the process planning difficult in a multi- stage fabrication run. For these reasons, PDMS was used here to define the etching window. Moreover, during the curing stage, PDMS was not chemically bonded to the silicon and thus was free to flow over it owing to its high thermal expansion coefficient ($\alpha_{PDMS} = 310 * 10^{-6}\, K^{-1}$) [31]. As a result, silicon did not experience any major thermal stress, despite having ~100 times lower thermal expansion coefficient ($2.6 * 10^{-6}\, K^{-1}$) than PDMS [32].

Before etching, the sample was treated with 10% hydrofluoric acid (HF) solution to remove any native oxide on the backside. The etching was performed in 25% TMAH doped with IPA (10 vol %) solution at 85ºC for 6 hours in a condenser cladded quartz flask, which is shown in Fig.2(c). The heating was controlled via an external controller and the sample was clamped in a custom-made Teflon holder to keep it in a vertical position.

During the etching process, the sample was immersed in 85ºC solution with cured PDMS bonded to silicon. Due to bonded PDMS, the silicon may have experienced thermal stress. This stress can be calculated by using:

$$\sigma = E_{si} * \Delta\alpha * \Delta T \qquad (1)$$

Where, E_{si} is young's modulus of silicon (130 GPa), $\Delta\alpha$ is difference between the thermal expansion coefficient of silicon and PDMS, and ΔT is the difference in temperature. Substituting the values given above in (1), we get about 3 times lesser stress value ($\sigma = 2.39\, GPa$) then the ultimate tensile strength of silicon (7 GPa) [33]. This means the silicon may not have warped or did not break during processing.

After the etching, the decontamination of the sample was done by immersing them into the solution of water, hydrogen

peroxide, and hydrogen chloride, mixed in the ratio of 5:1:1, for 2 minutes and then rinsing in distilled water. To remove the PDMS after etching, 1wt% solution of Tetrabutylammonium Fluoride (TBAF) in Propylene Glycol Methyl Ether Acetate (PGMEA) was used [34]. The sample was placed in a beaker containing the PDMS etching solution at 50ºC for 5 hours, until no traces or blobs of PDMS remained in the solution. The detailed chemistry of PDMS etching is discussed in the next section.

After the PDMS removal, the sample which now supported on a ring of bulk silicon, similar to TAIKO® processed wafer, was dried in ambient condition. The small part of the wafer consisting of the devices was separated using laser dicing and then integrated over a flexible polyimide foil using a low-stress adhesive. The sample was able to conform over a 3D printed jig with a bending radius of 10mm, as shown in Fig.7(a). A 3D scan carried out from the rim to the etched surface (Fig.3(a)), shows the anisotropic step profile with PDMS providing protection at the rim. The thickness of the sample after etching was measured using scanning electron microscopy (Fig.3(b)), and a 23 µm thick silicon was obtained after 6 hours, giving the etch rate ~46 µm/hour at 85ºC. The backside of the etched surface was observed to be populated with etch pits (Fig.4(a)) and low density of hillocks (Fig.4(b)).

Surface populated with pyramidal hillocks and etch pits produced by anisotropic etchant is a common irritant in the case of thin chips. The rougher surface leads to stress localisation which eventually compromises the bending limit. Moreover, excessive presence of hillocks does not allow the formation of reliable vias and conductive filling for interconnects. As result it is important to reduce the roughness arising due to hillocks and etch pits. The pyramidal hillocks are formed due to micro masking by hydrogen, which is formed as a by-product of the reaction between silicon and alkaline etchant. There are also pieces of evidence of hillocks formation due to preferential etching of different planes associated with silicon crystallographic structure. The etch pits formation mechanism is more complex and inherent to etching process. They can appear in various shapes and sizes and are mostly shallow and round due to anisotropic etching process between pit nucleation and step propagation [35]. In order to achieve a smoother surface, we used a mixture of TMAH and IPA, along with mechanical stirring using magnetic stirrer (200 rpm). While the addition of IPA is known to provide a smoother surface and reduce the undercutting, mechanical stirring prohibits the hydrogen bubble from sticking to the surface.

3. PDMS Removal

The methods known for removing cured PDMS from the silicon surface are: (i) scrapping; (ii) dry etching using fluorine-based reactive ion etching [36]; (iii) swelling of PDMS using appropriate organic solvent [30]; (iv) chemical-mechanical removal [37]. Depending on the application, one or a combination of these methods is employed to remove PDMS. In the present case, where PDMS is over thin silicon, mechanical scrapping using tweezers and further cleaning using pressurised spray is not possible as these steps are likely to break the chip. Similarly, swelling the PDMS with a nonpolar organic solvent such as hexane, toluene, chloroform, and peeling it off can introduce mechanical stresses on thin silicon [38] and lead to breakage. Furthermore, these processes do not guarantee PDMS residues free surface. Likewise, dry etching of PDMS produces substantial surface roughness and can also damage Si surface as the recipe used for dry etching of PDMS is similar to that for silicon (Si) and silicon dioxide (SiO_2) [39, 40]. Another method is the chemical-mechanical removal which uses a strongly alkaline solution such as sodium hydroxide (NaOH) in lower boiling point alcohols such as methanol, isopropanol, causing a base induced chemical degradation of —Si—O—Si— chain resulting in removal/dissolution of silicone residue from surfaces. However, using a low boiling solvent with strong alkali has safety and flammability issues along with environmental concerns.

Considering the above issues, the wet chemical etching is explored here to remove PDMS after thinning. The organic reactive reagents-based chemistry such as quaternary ammonium fluoride (QAF) (e.g. TBAF) in low solubility solvents such as di-substituted amides (e.g. N-methylpyrrolidinone (NMP), dimethylformamide (DMF)),

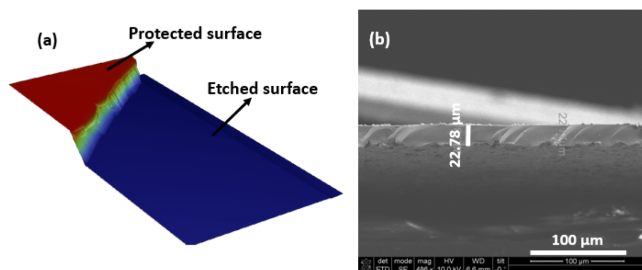


Figure 3: 3D scan of etched step showing the masking property of PDMS. The red area was masked with PDMS and the blue area shows the silicon region.

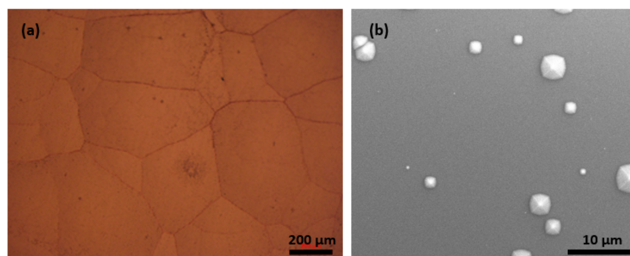


Figure 4: (a) Optical image of the etched backside showing the etch pits created during etching due to preferential etching of different crystallographic planes. (b) SEM image of hillocks formed on the silicon surface due to micro masking effect.

tetrahydrofuran (THF) or PGMEA) have been shown to yield good results for removal of PDMS [34]. These solutions cause fluoride-ion-assisted rapid disruption/disintegration of the PDMS polymer matrix to monomers/ oligomers, followed by

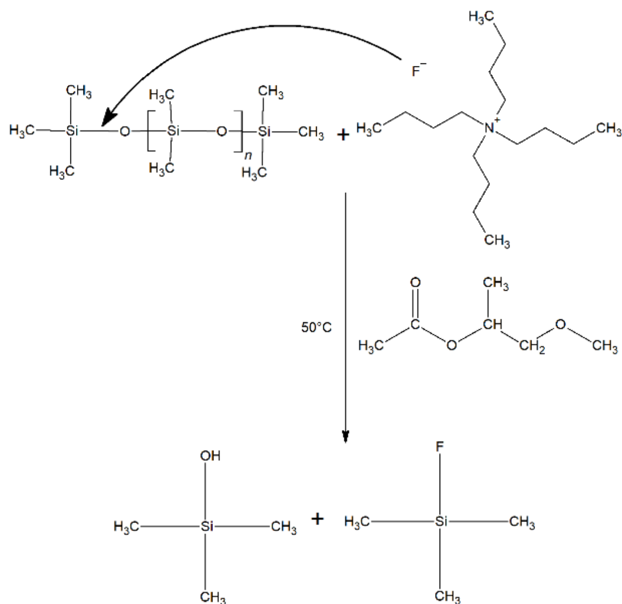


Figure 5: Reaction mechanism between TBAF and PDMS based on nucleophilic attack of fluoride ion on siloxane bond leading to dissolution of PDMS chain in the solvent.

its dissolution in the solvent. This mostly removes the residues by dislodging PDMS from the surface and, to a large extent, by dissolving PDMS residues by breaking Si–O bonds and forming Si–F bonds, which is similar to the etching of glass in hydrogen fluoride. Similar chemistry, with a dilute solution of TBAF (1% weight concentration) in hydrophobic non-hydroxylic aprotic PGMEA, has been used in this paper. This solution is compatible with the silicon and used metals, as evident from the unaltered surface and device characteristics of the capacitor after PDMS removal, as can been seen from Fig. 7(b).

The reaction mechanism between PDMS and TBAF is thought to be assisted by nucleophilic substitution at Si-O-Si bond by naked fluoride generated from TBAF followed by siloxane bond cleavage [41, 42]. Nucleophilic substitution is an important class of reactions in which an electron-rich nucleophile selectively bonds with or attacks the positive or the partially positive charge of an atom or a group of atoms to replace a leaving group [43]. Nucleophilic substitution requires the attacking species to be a strong base, which at first seems to be impossible with naked fluoride since it is a weak base due to lower electronegativity. However, nucleophilicity is not a property inherent to a given species; it can be affected by the medium it is dissociating in. For example, in a polar-protic solvent, where the nucleophile can participate in

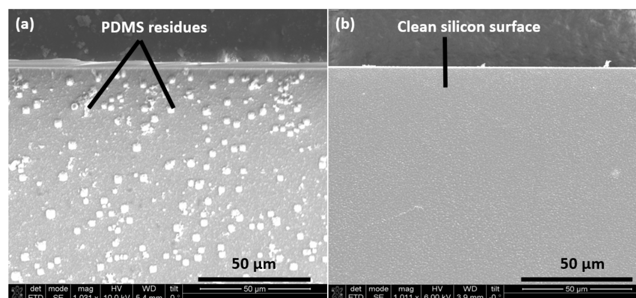


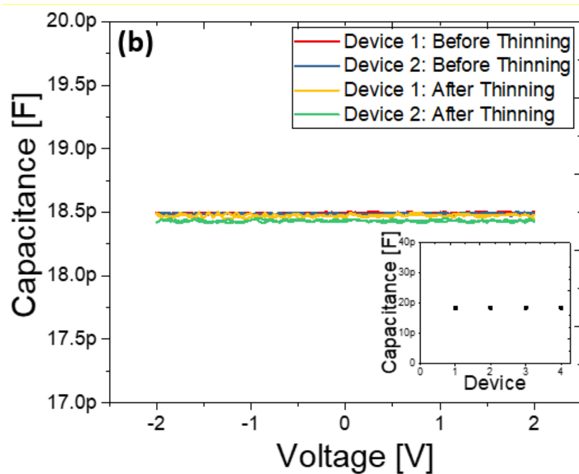
Figure 6.: SEM image of silicon sample during (a) midway of PDMS etching (b) at the completion of PDMS etching.

hydrogen bonding. In doing so, the nucleophile is considerably less reactive since its lone pairs of electrons are interacting with the electron-poor hydrogen atoms of the solvent. This is the reason why polar aprotic solvent is used in this work for utilising the reactivity of unstable fluoride. In polar aprotic solvent, nucleophiles do not have hydrogen bonds, allowing the nucleophiles to have greater freedom in solution. Under these conditions, nucleophilicity connects well with basicity and fluoride ion, being the most unstable of the halide ions and so best nucleophile [44], reacts fastest with electrophiles, which in this work is siloxane bond.

The mechanism of fluoride-induced siloxane bond cleavage is represented in Fig. 5. The fluoride ion attacks the silicon atom of Si-O-Si bond, which breaks towards the oxygen due to higher electronegativity, thus breaking the polymer chain in oligomers. PDMS removal rates depend on two factors: (1) the reactivity of TBAF with Si – O bonds in the solvent, which in turn depends on the polarity of the solvent, and (2) the degree of dissolution offered by solvent to the oligomers of PDMS. At this point, solvent plays an important role in the dissolution of oligomers. The PGMEA was considered a more suitable solvent for TBAF than THF, due to a higher boiling point (145ºC) compared to that of THF (66ºC) [41]. The sample was immersed in the solution of TBAF in PGMEA for 5 hours, and then in pure PMA solution for 1 hour to make sure that there is no residue left on the front surface. This can be observed more clearly from Fig.6(a) which shows the SEM image of sample in mid-way during PDMS removal step, and small spherical residues of PDMS can be seen, whereas Fig.6(b) shows the image at the final stage of PDMS removal and a clean surface of the silicon substrate can be observed. This experiment furthers strength our previous work of PDMS removal reported in [34].

4. Electrical Characterisation

The fabricated devices on the front side of the sample were characterised before and after the thinning process. A summit 12k autoprober with control measure units were used to run capacitance-voltage (C-V) measurements, and plotted in Fig. 7(b). As can be seen from the plot, the capacitance values remain almost unchanged (~18.5 pF) in the scan range of -2V



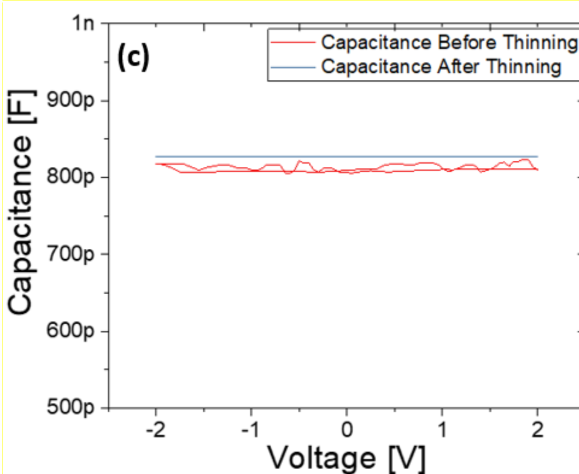
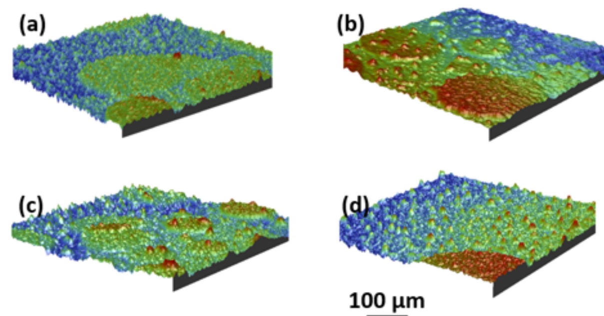


Figure 7: (a) Image of thinned sample integrated with polyimide foil and placed over a 3D printed jig with bending radius of 10 mm. (b) C-V plot of capacitive structures before and after thinning obtained using PDMS as protection coating. (c) C-V plot of a sample capacitive device before and after thinning using ProTEK as protection coating.

to 2V before and after thinning. Moreover, the device to device variation measured for 4 devices also shows minimal deviation (inset of Fig. 7(b)).

To further validate the efficacy of the approach presented in this, we repeated a similar silicon etching process with a commercially available ProTEK protection layer. The sample



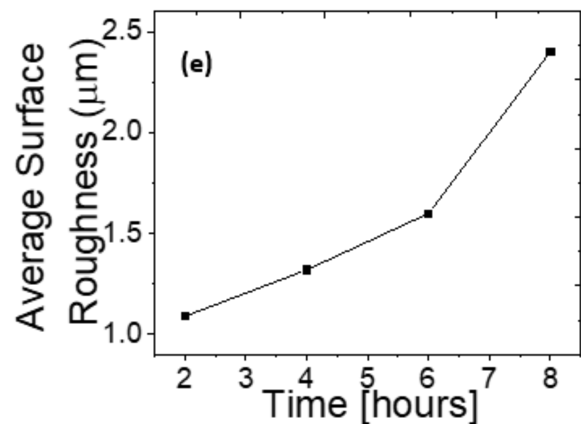


Figure 8: The 3D profile scan of PDMS surface at the end of: (a) 2 hrs; (b) 4 hrs; (c) 6 hrs; and (d) 8 hrs; (e) Plot of surface of PDMS vs etching time showing almost linear increase in the roughness with time.

was composed of capacitive structures with aluminium nitride as dielectric. The protective coating was removed after etching using the chemical composition supplied by the supplier. The electrical characterisation of the device carried out before and after etching shows negligible change, as can be seen from Fig.7(c).

5. Effect of TMAH exposure on PDMS

The chemistry discussed in Section 3 can also be used to understand why TMAH in water does not affect the PDMS. Due to the polar protic nature of water, the nucleophilicity of OH^- ion decreases significantly because of partial hydrogen bonding between water molecules and hydroxide ion [45]. The OH^- ion with reduced nucleophilicity cannot break the siloxane bond. Furthermore, water cannot dissolve any monomer/oligomer of PDMS and which has led to its usage as sealing rings [46]. Therefore, a thin film of PDMS is resistant to TMAH and so can be used as a protective layer. In order to confirm this observation, we carried out tests to analyse the effect of prolonged exposure of PDMS to TMAH. A strip of PDMS, with thickness 1900 µm, was immersed in 25 wt% TMAH at 85°C and the initial and final thickness was measured using the Logitech Contact Measurement Gauge tool, and no decrease in thickness was observed. Moreover,

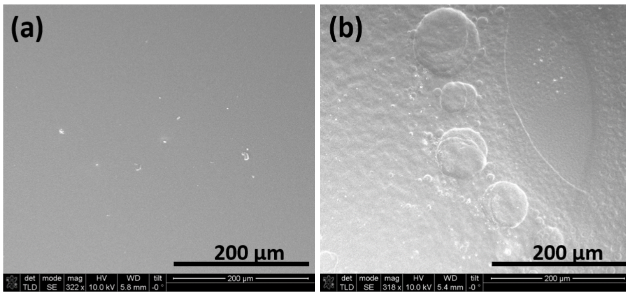


Figure 9: SEM image of PDMS surface (a) before the etching process (b) at the end of etching process.

the surface roughness was measured during the etching at the interval of 2 hours (Fig.8(a-d)), and it is observed to increase with time but remained much less when compared to the thickness of the film, as can be seen from Fig.8(e). However, during the etching, circular depressions on PDMS surface were observed. These could be the major factor behind the surface roughness, as can be observed from the surface scan and scanning electron microscopy (SEM) images shown in Fig. 9(b).

6. Conclusion

The ultra-thin chips realised from the wet etching technique require the front processed side to be protected from the etchant. This paper presents the new method with PDMS, a silicone elastomer, as a protective layer for the frontside of processed wafer. The PDMS was also used to define the etching window on the backside of the wafer. The cured polymer showed good chemical resistance during anisotropic etching in alkaline solutions heated at 80–90ºC for whole duration and its mechanical and thermal properties prevent the undesirable effects due to stress generated during thinning process by keeping the thermal stress well below the ultimate tensile strength of silicon, and resulted in silicon with thickness in the range of sub-25 µm. The protective layer was effectively removed using the solution of TBAF in PGMEA, a composition of nucleophilic agents in polar-aprotic solvent. The effect of etching time and etchant on PDMS morphology has also been studied to see if there is any microscopic level change in PDMS surface after exposure to etchant, and it was observed that prolonged exposure to the etchant increases the surface roughness, but does not lead to a decrease in the thickness or pinhole formation. Post removal, the device characteristics (capacitance-voltage) of fabricated capacitors were similar to the one measured before initiating the thinning process. In summary, this study shows the promising case of using an economical method of protecting top-side of the UTCs during thinning by using the readily available elastomer. The use of PDMS also aligns with other works related to printed electronics where PDMS has been used as a carrier substrate to transfer ultra-thin chip and microstructures on to flexible substrate [3, 14, 34, 47].

Acknowledgements

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