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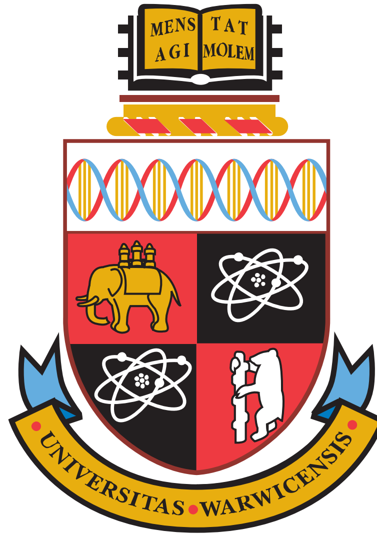
Dielectrics for Narrow Bandgap III-V Devices



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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has been composed by myself and has not been submitted in any previous application for any degree. The work presented (including data generated and data analysis) was carried out by the author except in the cases outlined below:

- Epitaxially-grown material in chapters 5 and 8 was prepared by Principal Research Fellow Dr. Mark Ashwin to the author's specification
- Some electrical measurements presented in chapters 6 and 7 were performed by an undergraduate summer student, Miss Naomi Meakin, under direct supervision from the author, using equipment, software and procedures prepared by the author
- Some devices in chapters 6 and 7 were fabricated by Fabrication Process Technician Ms. Corinne Maltby under supervision from the author, using fabrication procedures developed by the author and included in appendix A
- Training and support for X-ray photoelectron spectroscopy (XPS) in chapter 6, including review of spectrum fitting, were provided by XPS Facilities Manager Dr. Marc Walker
- Transmission electron microscopy (TEM) sample preparation and imaging in chapter 7 were performed by Reader Dr. Richard Beanland, following the author's brief
- Diode devices in chapter 8 were fabricated by Ms. Corinne Maltby using a fabrication procedure that is standard to the research facility and outlined in chapter 8. These devices were characterised by the author.
- Atomic force microscopy measurements in chapter 8 were taken under the author's direction by PhD student Mr. Alan Brunier and post-processed by Mr. Brunier.

- Potential studies into the effect of dielectric passivation on etched diode structures, included in chapter 10, were discussed and jointly developed by the author and Principal Research Fellow Dr. Richard Jefferies.

Abstract

Indium antimonide is a narrow bandgap semiconductor material with properties that make it ideal for mid-infrared optoelectronics, ultra-high speed electronics and emerging spin-based quantum technologies. A significant limitation to its practical application is the lack of a dielectric technology for surface passivation and gate control.

Modelling and analysis techniques for MOS capacitors have been tailored to InSb and verified, including nonparabolic band structure models and oxide capacitance extraction methods. High-field effects, such as Zener tunnelling and impact ionisation, have been modelled to identify limitations on material doping ($<10^{16}$ cm^{-3}) and quantisation effects have been similarly modelled to verify their impact on characterisation and analysis.

InSb/Al_2O_3 MOS capacitor test structures have been fabricated to investigate a series of dielectric deposition processes. Wet chemical treatments using HCl were found to produce an $InCl_3$ surface layer, but only if diluted in and rinsed with isopropanol. This layer was associated with a flatband voltage shift of +0.79 V. HCl treatment was found to reduce hysteresis voltage but not significantly affect other figures of merit. In-situ plasma pretreatments were found to cause deterioration in MOSCAP structures, in particular increased DC leakage current. Post-metallisation annealing was investigated and optimum treatments determined to be around 300°C, 1 hr. At 400°C or greater, MOSCAP behaviour broke down, showing increased frequency dispersion and potential shift to p-type behaviour. Some AlInSb layers were grown but provided limited information on the effect of Al composition, with layers significantly affected by growth methods and material strain.

Alternative dielectrics were also examined. AlN offered slightly improved hysteresis but slightly increased interface trap density, whereas HfO_2 produced deterioration in all figures of merit, particularly hysteresis voltage. These results provide a foundation for further process development and integration into improved FET/diode device structures.

Nomenclature

Abbreviations

AC Alternating current

AFM Atomic force microscopy/microscope

ALD Atomic layer deposition

BOE Buffered oxide etch

C-V Capacitance-voltage

CB Conduction band

CMOS Complementary metal-oxide-semiconductor

CVD Chemical vapour deposition

DC Direct current

DLTS Deep-level transient spectroscopy

DOS Density of states

eV Electron volt

FET Field effect transistor

FG Forming gas (5% H_2, 95% N_2)

G-V Conductance-voltage

HF High frequency

I-V Current-voltage

ICP Inductive coupled plasma

LED Light-emitting diode

LF Low frequency

MBE Molecular beam epitaxy

MESFET Metal-semiconductor field effect transistor

MISCAP Metal-insulator-semiconductor capacitor

MOSCAP Metal-oxide-semiconductor capacitor

MOSFET Metal-oxide-semiconductor field effect transistor

PDA Post-deposition anneal/annealing

PEALD Plasma-enhanced atomic layer deposition

PECVD Plasma-enhanced chemical vapour deposition

PIPS Precision ion polishing system

PMA Post-metallisation anneal/annealing

PVD Physical vapour deposition

QW-MOSFET Quantum well metal-oxide-semiconductor field effect transistor

QWFET Quantum well field effect transistor

RIE Reactive ion etching

SRH Shockley-Read-Hall

TEM Transmission electron microscopy/microscope

TEMAH Tetrakis(ethylmethylamino)hafnium

TMA Trimethylaluminium

TMAH Tetramethylammonium hydroxide

VB Valence band

XPS X-ray photoelectron spectroscopy

Chemical Formulae and Symbols

Al Aluminium

Al_2O_3 Aluminium oxide

AlGaAs Aluminium gallium arsenide

AlInSb Aluminium indium antimonide

AlN Aluminium nitride

AlSb Aluminium antimonide

Ar Argon

As Arsenic

Be Beryllium

C Carbon

Ga Gallium

Ga_2O_3 Gallium oxide

GaAs Gallium arsenide

GaN Gallium nitride

GaP Gallium phosphide

GaSb Gallium antimomide

Gd_2O_3 Gadolinium oxide

Ge Germanium

H_2 Hydrogen (gas)

HCl Hydrogen chloride/hydrochloric acid

He Helium

HfO_2 Hafnium oxide

In Indium

InAs Indium arsenide

InGaAs Indium gallium arsenide, usually $In_{0.53}Ga_{0.47}As$

InP Indium phosphide

InSb Indium antimonide

La_2O_3 Lanthanum oxide

N_2 Nitrogen (gas)

O_2 Oxygen (gas)

P Phosphorus

Sb Antimony

Si Silicon

SiO_2 Silicon oxide

Te Tellurium

Symbols

α Nonparabolicity parameter

α_V First Varshni parameter

β_V Second Varshni parameter

ΔE Trap energy level displaced from the majority band edge

ϵ_0 Permittivity of free space

ϵ_{semi} Absolute permittivity of the semiconductor

η Electron/hole kinetic energy in reduced units ($\frac{E-E_C}{k_B T}$ for electrons, $\frac{E_V-E}{k_B T}$ for holes)

$\frac{d\psi_s}{dV_G}$ Stretch-out of C-V response

κ Relative permittivity. Also known as dielectric constant

ω Angular frequency

ψ Surface potential

σ Trap capture cross-section

τ_{it} Time constant of interface-trapped charge

φ Electrical potential

φ_b Bulk electrical potential

C Bowing parameter

C_m Measured capacitance

C_s Semiconductor capacitance

C_{FB} Flatband capacitance

C_{hf} Capacitance at high frequency

C_{lf} Capacitance at low frequency

C_{ox} Oxide capacitance

D_{it} Interface-trapped charge density

E_C Energy level at conduction band edge

E_F Fermi level

E_g Energy gap (of individual band minimum or globally for semiconductor)

E_I Intrinsic Fermi level

E_P Momentum matrix element

E_V Energy level at valence band edge

E_{off} Split-off valence band offset energy

F Kane parameter

G_m Measured conductance

G_P Conductance of sample using the parallel model

h Planck's constant

J_L Leakage current per unit area

k_B Boltzmann's constant

m^* Relative effective mass (of electrons/holes)

m_e^* Absolute effective mass of electrons

m_h^* Absolute effective mass of holes

m_0 Electron rest mass

$n[\varphi(x)]$ Concentration of electrons in the conduction band

N_A Concentration of acceptor dopants

N_c Density of states in the conduction band

N_D Concentration of donor dopants

n_i Intrinsic carrier concentration

N_v Density of states in the valence band

N_{ot} Quantity of oxide-trapped charge

$p[\varphi(x)]$ Concentration of holes in the valence band

q Electron charge

Q_s Sheet charge

T Temperature (in units of kelvin)

U Electron/hole energy in reduced units ($U = \frac{\varphi q}{k_B T}$)

U_b Bulk potential in reduced units

U_s Surface potential in reduced units

V_G Gate voltage

V_H Hysteresis voltage

V_T Threshold votage

V_{FB} Flatband voltage

V_{ox} Voltage across oxide only

v_{th} Thermal velocity of electrons/holes

Vocabulary

Γ valley Conduction band minimum at the Γ wavevector

Accumulation A condition where majority carriers in a MOSCAP are attracted and accumulate at the surface

Accumulation layer A thin surface region where majority carriers have accumulated due to applied potential

Annealing A fabrication technique where samples are exposed to high temperature (and, potentially, reactive gases)

Annealing Thermal and/or chemical treatments performed at elevated temperature

Binary semiconductor A semiconductor formed from a compound of two elements

Castagné-Vapaille See 'high-low'

Cryostat A test/measurement instrument capable of cooling samples and holding them at low temperature

Depletion A condition where majority carriers in a MOSCAP are repelled and depletion region is formed

Depletion layer See 'depletion region'

Depletion region A region of semiconductor where applied bias and ionised dopants repel charge carriers

E-beam Electron beam (evaporation)

Epitaxial Material grown as an extension of the existing crystal structure

Flatband The condition in a MOS structure where the bands in the semiconductor are not bent

Flatband voltage The voltage applied to a MOS structure at which the bands in the semiconductor are not bent (zero for an ideal MOSCAP)

Frequency dispersion Frequency-dependant C-V response (usually of accumulation capacitance)

Group III An element from group 13 of the periodic table

Group IV An element from group 14 of the periodic table or a semiconductor formed from a single such element only

Group V An element from group 15 of the periodic table

Heavy hole band Valence band maximum with high effective mass

High-low A technique for quantifying interface-trapped charge density based on high frequency and low frequency response (discussed in section 4.3.1)

Hysteresis Dependancy of flatband voltage on direction of voltage sweep

III-V A semiconductor formed from a 1:1 compound of elements from group 13 and elements from group 15 of the periodic table

Impact ionisation A semiconductor phenomenon whereby additional electrons/holes are generated due to a high electric field

Inversion A condition where minority carriers in a MOSCAP are attracted and accumulate at the surface

Inversion layer A thin surface region where minority carriers have accumulated due to applied potential

IV-IV A semiconductor formed from a compound of elements from group 14 of the periodic table

L valley Conduction band minimum at the L wavevector

Light hole band Valence band maximum with low effective mass

Mobility A property of solids: the distance an electron/hole will travel per unit voltage and unit time

Monolayer A layer consisting of a single atomic layer (or single crystalline unit cell for crystalline/compound materials)

n-type A semiconductor material/region doped with a donor impurity, adding excess electrons (negative charge)

p-type A semiconductor material/region doped with an acceptor impurity, adding excess holes (positive charge)

Photolithography A fabrication technique whereby areas of the sample are selectively masked

Precursor A reactive gas used as an elemental source in deposition

Split-off band Valence band maximum at lower energy level

Terman A technique for quantifying interface-trapped charge density based on high frequency response and modelled response (discussed in section 4.3.2)

Ternary semiconductor A semiconductor formed from a compound of three elements

X valley Conduction band minimum at the X wavevector

Zener tunnelling A quantum tunnelling phenomenon whereby electrons move between the sharply bent conduction and valence bands

Chapter 1

Introduction

This thesis is focused on the surface of the narrow bandgap semiconductor material indium antimonide (InSb) and interfaces between InSb and dielectric (insulating) materials. The aim of this thesis is to develop fabrication techniques to deposit dielectrics with a low density of defect states in the dielectric and at the interface.

Within the field of InSb dielectric interfaces, this thesis focuses on building a strong foundation to drive further development of the interface system, although some improvements have been demonstrated. Methodologies and models have been tailored to the InSb material system and a range of treatments from the scientific literature have been applied to InSb to identify the most promising routes to good dielectric interfaces.

1.1 Semiconductor Technology Applications

Electronics technology has become ubiquitous in the past century. Applications are extremely varied and include computing, telecommunications, electrical power management, light-emitting diodes (LEDs), photodetectors and sensors. To meet these requirements, the field of electronic devices has developed, covering the design of device structures, fabrication techniques and semiconductor materials. Semiconductor materials and their properties, such as bandgap energy and character, carrier mobility, carrier saturation velocity and critical electric field - are fundamental to effective devices but the dominant semiconductor material remains silicon. Silicon occupies the largest share of the semiconductor materials market, with only niche roles filled by other materials, such as germanium and gallium arsenide (GaAs).

1.1.1 Niches for Alternative Materials

The most important material parameter for semiconductor materials is the bandgap energy. This parameter influences or correlates with many others, such as mobility and critical electric field, and dictates the type of applications the material is best suited for. Wide bandgap materials, such as silicon carbide or gallium nitride, are best suited to high power devices (such as power converters for domestic or industrial use) and light-emitting diodes (LEDs)/photodetectors in the blue (including white) and ultraviolet wavelength regions. Conversely, narrow bandgap materials, such as germanium, indium arsenide (InAs), gallium antimonide (GaSb) and indium antimonide (InSb), are best suited to low-power applications (such as low-noise amplifiers, communications and possibly digital logic) and LEDs/photodetectors in the infrared spectrum. Narrow bandgap materials, particularly InSb and materials based on it, are the focus of this thesis.

1.1.2 Use of Narrow Bandgap Materials

When narrow bandgap materials are fabricated into diodes and transistors, they require less power to turn on and drive, allowing computing systems to run at higher speeds without overheating and mobile communications modules to operate at a higher frequency without rapidly draining battery energy. When fabricated into optoelectronic devices (LEDs and photodetectors) they will emit/absorb in the infrared band, allowing sensing and imaging at very long wavelengths. When fabricated into photovoltaic devices, they will absorb at long wavelengths, allowing high efficiency when coupled with wide bandgap materials and capture of energy from 'waste heat' infrared radiation. Narrow bandgap materials are also well-suited to sensor applications, such as Hall effect magnetic sensors which rely on the high charge mobility in these materials, and for emerging quantum computing applications, due to strong coupling between electric field and quantum states.

1.2 III-V Semiconductor Materials

1.2.1 Elemental and Compound Semiconductors

Semiconductor materials can be a pure single element or a chemical compound. Silicon and germanium are pure elemental semiconductors from group 14 of the periodic table and are frequently referred to, using an old convention, as group IV semiconductors. The two can be alloyed, along with the other group IV materials carbon and tin, to form IV-IV alloys. Conversely, compound semiconductors usually

use elements from different groups of the periodic table. The most common family of compound semiconductors is formed from 1:1 mixtures of elements from group 13 and group 15, also known under an old convention as group III and group V, giving them the name III-V semiconductors. The most common example is gallium arsenide (GaAs), formed from a 50:50 mixture of gallium (Ga) and arsenic (As) but other elements can be combined to form III-V semiconductors. The most common group III materials are aluminium, gallium and indium and the most common group V materials are phosphorus, arsenic and antimony, giving compounds such as gallium phosphide (GaP), aluminium antimonide (AlSb) and indium arsenide (InAs). Each compound has unique properties but, as a general trend, utilising elements from further down the periodic table results in a narrower bandgap and using elements from further up the periodic table results in a wider bandgap. When considering narrow-bandgap applications, indium antimonide (InSb) is the III-V compound with the narrowest bandgap: 0.17 eV at room temperature, lower than any other simple semiconductor. With this low bandgap, and the other material parameters which come with it such as high charge mobility, InSb has the potential to offer significant improvements to devices in low power applications.

1.2.2 Semiconductor Alloys

A unique feature of compound semiconductors when compared to elemental semiconductors is the greater freedom when preparing alloy material. In a III-V semiconductor, the group III and group V elements can be alloyed independently, within the limits of material solubility, and the wide range of possible alloys allows the desired properties to be more easily obtained. As an example, a quantum well is formed when a thin layer (approximately 10 nm) of a narrow bandgap material is sandwiched between material of a wider bandgap. This can be achieved for a GaAs-based system by growing a layer of aluminium gallium arsenide (AlGaAs), with a wider bandgap due to its aluminium content, followed by a thin layer of indium gallium arsenide (InGaAs), with a narrower bandgap due to its indium content, followed by another layer of AlGaAs. These materials also have a very good match of lattice constant (atomic spacing in the crystal structure), allowing these materials to be grown together without introducing defects from material strain. Quantum wells generate interesting physical phenomena and are frequently used in devices. In the case of InSb, it is often alloyed with aluminium, forming aluminium indium antimonide (AlInSb), to control the bandgap energy.

A simple III-V semiconductor with no alloying is referred to as a binary compound or binary semiconductor. An alloy utilising one additional element (i.e. three

elements in total) is referred to as a ternary alloy or ternary semiconductor, an alloy utilising two additional elements is referred to as quarternary and so on.

1.3 Review of Narrow Bandgap Material Applications

A wide range of III-V materials have been considered for improved performance in low-power applications. The most widespread use of narrow bandgap III-V semiconductors is in infrared LEDs and photodetectors, where they have been widely adopted and commercialised[1][2]. Within this application, InSb-based $Al_xIn_{1-x}Sb$ alloys are of particular interest, as they can produce optoelectronic devices which operate in the commercially-important 3 µm-6 µm wavelength range (0.21 eV to 0.41 eV), where absorption lines exist for CO_2 and CH_4. Within this application, device structures are etched vertically, forming exposed surfaces with defects states. These states cause surface leakage and impact on device performance but they can be passivated by depositing a dielectric. Surface passivation processes are critical for plasmonic micro-antenna and nano-antenna technologies, where light focusing using surface structures[3] is combined with fine etching of features to significantly improve signal-to-noise ratio[4]. Etching of fine features exposes a significant surface area and increases surface-to-volume ratio, necessitating effective passivation of exposed surfaces in order to benefit from the plasmonic structures.

Another potential application for narrow bandgap III-V semiconductors, which has received significant investigation, is high speed devices. Whilst commonly-used radio frequency (RF) and microwave electronics usually use metal-semiconductor gate structures, the application of digital logic demands low power consumption and metal-oxide-semiconductor (MOS) gate structures are preferred. Narrow bandgap semiconductors have been extensively studied for digital logic applications[5], with InSb offering not only the highest electron mobility and saturation velocity of any conventional semiconductor but one of the highest hole mobilities of any III-V semiconductor, rivalled by GaSb and exceeded only by germanium and diamond[6][7]. For digital applications, low power consumption is critical and MOS gates with a low density of interface and oxide trap states are required.

An additional emerging application for narrow bandgap III-V materials is in quantum devices, particularly quantum computing and the quantum bits (qubits) which form the 'building blocks' of quantum computing systems. Semiconductor qubits have been demonstrated using silicon-based[8] and GaAs-based systems[9], utilising electron spin as the foundation of the qubit system. Within this system,

InSb offers an exceptionally high Landé g-factor - a measure of the interaction between the electron spin and orbital angular momentum - which in turn gives rise to a very large Rashbah interaction[10][11]. This indicates not only that spin manipulation may be stronger in InSb than in other semiconductors but that spin manipulation may be possible without external magnetic fields[11]. In such structures, gate stacks with low leakage and low density of trap states would be essential, as qubits would be operating as single-electron devices, and high-quality MOS gates are an essential requirement to realising InSb-based quantum technologies.

The results reported in this thesis aimed to develop a dielectric deposition process on InSb-based materials suitable for surface passivation and MOS (metal-oxide-semiconductor) gate stack applications.

1.4 Thesis Outline

In chapter 2, a review of III-V dielectric processes is presented. Focusing on InSb but also InAs, GaSb, InGaAs and other III-V materials, dielectric materials are assessed as potential routes to high-quality interfaces in section 2.2. In section 2.3, trap states and their effect on MOS capacitor test structures are characterised, including a review of trap models. Pre-deposition and post-deposition techniques are reviewed in sections 2.4 and 2.5, followed by a review of characterisation techniques in section 2.6 and a short review of the limited work on dielectrics on AlInSb - an important alloy and encapsulating material - in section 2.7.

Chapter 3 presents an inventory of fabrication and analysis processes and details of processes used in the project's practical work. The chapter covers semiconductor crystal growth, chemical and physical deposition techniques, photolithography, etching and annealing fabrication techniques, as well as characterisation techniques for electrical, cryogenic, x-ray photoelectron spectroscopy (XPS), electron microscopy and atomic force microscopy methods.

Chapter 4 presents an overview of key theory for MOS capacitors, their impedance-voltage response and details on parameterisation of models. Section 4.2 covers ideal, trap-free response, which is then developed in section 4.3 to cover the effect of trap states and how these effects can be used to characterise and quantify them. Peculiarities in the band structure and their effect on ideal response modelling is discussed in section 4.4. An additional trap characterisation method, using conductance-voltage-frequency data, is discussed in section 4.5 and the modelling and parameterisation of the semiconductor materials is discussed in section 4.6.

In chapter 5, the theory from chapter 4 is applied and extended. Section 5.2

details the implementation of the modelling and analysis methods, section 5.3 details data extraction required for modelling devices and section 5.4 details verification of the model and its parameterisation. A sample of measured and extracted data is discussed in detail in section 5.5, highlighting common and/or unusual features. Finally, as the narrow bandgap of InSb can cause high electric field effects to occur at unusually low fields, these phenomena are modelled for InSb and their effects on the material quantified.

The experimental work begins in chapter 6, focusing on Al_2O_3 as the dielectric. Sections 6.2 and 6.3 investigate the effect of wet cleaning with HCl, focusing particularly on surface and interface layers, their formation and their impact on MOS devices. Section 6.4 investigates in-situ pre-treatments using plasma and attempts to replicate improvements demonstrated in the literature.

Chapter 7 is a study on post-deposition annealing. It reveals regimes and behaviour of material breakdown at high temperatures in section 7.3 and regimes for improving device performance in sections 7.4, 7.5 and 7.6.

Chapter 8 presents a brief snapshot study into AlInSb materials. Two regimes are studied: InSb and $Al_{0.001}In_{0.999}Sb$ on InSb, nominally free of strain relaxation, and InSb and $Al_{0.1}In_{0.9}Sb$ on GaAs, with a large mismatch of lattice constant but with a greater degree of freedom for material composition and characterisation. Surface morphology of the materials on InSb is studied by atomic force microscopy in section 8.2.2 and electrical characterisation of MOSCAPs from the materials is covered in section 8.4.

The final experimental study in chapter 9 compares Al_2O_3 to AlN and HfO_2. AlN is discussed in section 9.3.1 and HfO_2 in section 9.3.2. The project's findings are summarised in chapter 10, including recommendations for follow-up work in section 10.3. Appendicies cover the standard experimental procedure in appendix A, a summary of results from the literature review in appendix B and a partially-completed device study in appendix C.

Chapter 2

Literature Review

2.1 Introduction

As electronic device technology continues to evolve, the focus of the electronics industry is beginning to shift away from silicon and towards a wider range of materials. These materials, with different properties such as wider and narrower direct and indirect bandgaps, are gaining prevalence within a variety of niche markets. This project is concerned with devices fabricated using narrow bandgap compound semiconductors from the III-V family, specifically indium antimonide (InSb) and related compounds. These materials have displayed great promise for infrared emitters and detectors, as well as high-speed transistors and emerging applications such as spintronics and quantum computing.

A significant problem facing new electronic materials is the integration of dielectric (insulating) layers. The interfaces between semiconductor and dielectric materials are prone to high defect density, greatly limiting the practical applications of devices such as MOSFETs (metal-oxide-semiconductor field effect transistors). Dielectrics are essential in modern transistors, such as MOSFETs, as they reduce gate leakage current to a negligibly small amount and offer greater control of threshold voltage V_T. Dielectrics are also used in very small devices with a high surface-to-volume ratio, such as LEDs and photodiodes, to reduce surface leakage current by passivating the surface and the charged states associated with it. An extensive résumé of semiconductor device principles can be found in textbooks such as Sze[12] and Pierret[13].

This review focuses on dielectric interface studies on indium antimonide (InSb) and aluminium indium antimonide compounds (AlInSb and AlSb) but work has also been included on gallium arsenide (GaAs), indium arsenide (InAs), indium gallium arsenide ($In_{0.53}Ga_{0.47}As$, a ternary alloy with a lattice constant matching

InP, hereafter referred to simply as 'InGaAs'), indium phosphide (InP), gallium antimonide (GaSb) and gallium nitride (GaN), which have also been a part of post-Si research. Certain methodologies and characterisation techniques, demonstrated on group IV materials germanium (Ge) and silicon (Si) relevant to III-V materials, have also been included.

2.1.1 Deposition Techniques

Fundamentally, there are 4 basic techniques used to form oxide layers. Two techniques rely on the oxidation of the substrate (bulk oxidation processes): thermal oxidation and anodic oxidation. The other two techniques form deposited layers (deposition processes): physical vapour deposition and chemical vapour deposition. Bulk oxidation processes have historically been used to form high-quality oxide layers, most notably thermal oxidation of silicon substrates. Bulk oxidation processes are rarely used for III-V substrates, as the oxides of gallium, indium, arsenic and antimony have poor stability and/or electrical properties[14][15]. Anodisation tends to be used over thermal oxidation, as III-V compounds can become unstable at high temperatures (for example, the melting point of InSb is only 527°C). Physical vapour deposition (PVD) involves the source material being dispersed by physical phenomena and depositing on the substrate. PVD techniques include thermal and electron beam evaporation, sputtering and molecular beam deposition. Evaporation and sputtering techniques, while offering good layer conformity, tend not to produce dielectric interfaces or films of a high quality. Molecular beam deposition (MBD, also known as molecular beam epitaxy when applied to semiconductor growth) can produce moderately high-quality layers but must be done in extremely high vacuum, resulting in a slow process which uses expensive equipment and has limited industrial potential. Chemical vapour deposition (CVD) involves the chemical reaction of source gases to form the deposited layer and includes both conventional CVD, such as low pressure CVD and plasma enhanced CVD, and atomic layer deposition. As with PVD, conventional CVD can give a high deposition rate and good conformity but despite CVD giving reduced film stress compared to PVD, the film porosity and defect density are still high, giving low-quality dielectrics and interfaces overall, particularly when compared to established thermal oxidation processes on silicon. Additionally, as the growth rate of conventional CVD is so high, it can be difficult to control the thickness of very thin films. Atomic layer deposition (ALD) involves two precursor gases, alternately pumped into the reactor chamber between inert gas purges. The precursor of the first half-cycle adsorbs onto the substrate's surface, then the precursor of the second half-cycle reacts with the adsorbed precursor to

produce a deposited layer of, at most, a single atomic layer in thickness. This process is then repeated until the desired thickness is achieved. ALD is considered desirable for dielectric formation, as the pulsed deposition of precursors allows superior control of the surface when compared to PVD and conventional CVD, allowing film and interface quality between bulk oxidation of silicon and conventional deposition processes. The energy for these chemical processes can be supplied thermally, by heating the substrate, by a plasma, giving higher growth rates and/or reduced deposition temperature, or by UV-initiation. UV-initiated chemical deposition processes have been applied to InSb before, with encouraging results[16], and UV-initiated ALD technology is becoming more widespread[17] but no deposition instruments equipped with UV sources are available for this project.

The quality of the interface between a semiconductor and dielectric can be quantified using several figures of merit. Most critical and widely-reported is interface-trapped charge density (D_{it}). This is the density of defect states present at the interface and is a critical figure of merit for processes and structures. These states decrease device performance by several mechanisms: charge cannot easily accumulate and deplete as the voltage applied to gate structures is varied, the trapped charge increases resistance of surface channels by scattering electrons and the states offer undesirable paths for charge carriers, causing large leakage currents. These states exist at finite energy levels within the band structure of the semiconductor and the energy profile of the trap states can be extracted, as detailed in chapter 4[18]. Within published literature, figures for D_{it} are frequently quoted, with their energy levels being described as 'near valence band edge', 'midgap' (i.e. close to the centre of the semiconductor bandgap), 'near conduction band edge' and 'inside conduction band'. The energy context of the trap states is important for example, midgap states hinder the formation of an inversion layer but states in the conduction band hinder current flow and increase series resistance. D_{it} tends to be in the order of 10^{12} cm^{-2} eV^{-1} for III-V dielectric interfaces, with changes of an order of magnitude denoting a significant change in performance. Another key figure of merit is leakage current density (J_L). Leakage current is affected by the oxide's bulk quality as well as the interface. The applied electric field or voltage can be different for each study and must be included in the summary of results. A typical value for J_L is 10^{-8} Acm^{-2} at 1 MVcm^{-1}[19]. Other figures of merit - flatband voltage, hysteresis and frequency dispersion - are discussed in section 2.3.

2.1.2 Origin of Interface Trap States

Interface-trapped charge is generally considered to have three sources: group III dangling bonds, group V dangling bonds and group V dimers (two atoms of e.g. arsenic bonded at the surface). Robertson *et al.*[20] discuss trap origins in GaAs, modelling these three defects relative to the semiconductor bandgap. They also discuss the effect of surface reconstruction (i.e. the layout of atoms at the material surface) - while the consideration of surface reconstruction is beyond the scope of this thesis, Robertson *et al.* note the need to break complex multi-atom surface reconstructions into simpler ones. The role of plasma and gas treatments in breaking surface bonds/dimers is discussed below, and Robertson *et al.* note that the small size of the aluminium precursor (trimethyl aluminium, TMA) allows it to more efficiently access and break group V dimer bonds. Robertson *et al.* also note the need for effective diffusion barriers to limit the oxidation of the substrate beneath the dielectric - diffusion resistance is considered further throughout section 2.2. Finally, Robertson *et al.* note the potential benefit of nitridation and the integration of aluminium nitride (AlN), which is discussed further in section 2.2.6.

2.2 Dielectric Materials

Due to extensive research in CMOS technology, a wide range of dielectrics has been studied in an attempt to improve device performance. The dielectrics highlighted in reviews by Robertson and Falabretti[21], Shamiryan *et al.*[22] and Engel-Herbert *et al.*[23] illustrate the range of materials under investigation, with Shamiryan *et al.* describing the desirability of various material properties. Most prominently, the dielectric constant (κ) of a dielectric defines the capacitance per unit volume. For MOSFETs, a higher gate capacitance gives a higher on-state current for a given gate voltage, making a high κ value desirable. In addition to κ, however, Shamiryan *et al.* highlight the importance of stability and maturity of the dielectric, as well as compatibility between the dielectric and the substrate. The dielectrics discussed within this review are silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), gadolinium oxide (Gd_2O_3), gallium oxide (Ga_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3) and aluminium nitride (AlN). Although other dielectrics can be used, here we focus on the most thoroughly studied ones, as they provide the best prospects for a practical engineering outcome within the timescale of this project. This section is a qualitative summary of results, with a summary of important dielectrics shown in table 2.1 and a quantitative summary table included in table B.1 in appendix B.

2.2.1 Silicon Dioxide

Silicon dioxide is the most widely used dielectric, as it is native to silicon, the most widely used substrate material. SiO_2 has been used extensively with III-V materials due to its maturity and, while the interface is rarely studied by itself, the symptoms of a poor interface, such as large leakage currents and poor capacitance-voltage (C-V) response, have been observed[14][24]. SiO_2 has a dielectric constant of 3.9,[22] which is considered the baseline for work on gate dielectrics.

2.2.2 Gadolinium/Gallium Oxide

Gadolinium has been used in conjunction with gallium oxide to form dielectric layers on GaAs and these layers have been widely studied[25][26][27][28]. Gallium oxide is native to GaAs and can offer good substrate-dielectric compatibility, but the band offset (i.e. the barrier to electrons entering the dielectric from the substrate) is very low and can be increased by using an alloy of gallium oxide and gadolinium oxide[27]. Ren *et al.*[26] discuss the anodisation process for GaAs - the presence of other forms of gallium oxide such as GaO and GaO_2 preclude the use of an anodisation process without additional processing (annealing) to stabilise the oxide. Additional processing steps place a larger strain on the thermal budget for fabrication - i.e. they add to the cumulative degradation the wafer experiences from high-temperature exposure - and deposited Ga_2O_3/Gd_2O_3 is preferred[26][27][28]. The dielectric constants for Ga_2O_3 and Gd_2O_3 are both approximately 10,[22][29] offering a modest improvement on SiO_2.

Although these results are interesting and raise the prospect of similar alloy systems for other substrate materials, there is no literature regarding an analogous system for InSb. It is unclear whether an In_2O_3-based system would include similar band offset issues and whether addition of an additional element (analogous to Gd) would be required to produce a suitable dielectric. The prospect of an analogous In_2O_3-based system may be worth further investigation but, given the lack of existing literature when compared to other better-established, ALD-based dielectric systems discussed below, is not investigated in this thesis.

2.2.3 Aluminium Oxide

Aluminium oxide is more mature than most dielectrics discussed here and is already used extensively in devices[22]. It has also been applied to III-V materials, such as GaAs,[30][31] InGaAs,[32][33] and InSb[34][35]. Al_2O_3 has demonstrated excellent interface quality when compared to other deposited dielectrics, such as

HfO_2 and La_2O_3[31][33]. It has been observed that the ALD deposition process results in a thinning of the native oxide layer[31][32] and the accepted mechanism for this thinning is the reaction between the aluminium precursor of the ALD process, trimethylaluminium (TMA), and the native oxide[36]. Effectively, the ALD process for Al_2O_3 acts as self-cleaning, a process discussed in section 2.4.2. Al_2O_3 has a dielectric constant of approximately 9, which is significantly higher than SiO_2 but lower than all other dielectrics discussed within this review[22]. Al_2O_3 forms the foundation of the project, establishing low interface-trapped charge before shifting attention to dielectrics with a higher κ and other desirable properties.

2.2.4 Hafnium Oxide

Hafnium oxide has received significant attention, as it has displayed good compatibility with Si[22]. Hafnium oxide has a high dielectric constant of approximately 25, offering a significant improvement when compared to both SiO_2 and the previously discussed dielectrics Al_2O_3, Ga_2O_3 and Gd_2O_3. As a trade-off, experiments with GaAs and InGaAs have shown a poorer interface quality for HfO_2 than for other dielectrics[31],[33]. HfO_2 has also been known to crystallise at the relatively low temperature of 600°C, giving rise to increased leakage current due to the defects at the grain boundaries[37] - this is not an issue for InSb, as InSb itself has a melting point of 527°C, limiting the thermal budget. HfO_2 performs better than Al_2O_3 as a diffusion barrier, preventing group III and group V atoms diffusing into the oxide[38][39], although Hf can diffuse from the oxide into the semiconductor[39].

Due to its high dielectric constant, relative maturity and effectiveness as a diffusion barrier, HfO_2 has been used as a middle/top layer in complex dielectric stacks. Suzuki *et al.*[40] demonstrate a HfO_2/Al_2O_3 dielectric stack on InGaAs and Trinh *et al.*[38] show a similar stack on InSb. Both processes show a combination of the low D_{it} of Al_2O_3 and the low leakage current & atomic interdiffusion of HfO_2. Suzuki *et al.* show TEM images from HfO_2 and HfO_2/Al_2O_3 interfaces, reproduced in figure 2.1, which contrast the organised and abrupt Al_2O_3 interface with the visibly less organised HfO_2 interface. This may be due to the self-cleaning effect of TMA, discussed in section 2.4.2, and Trinh *et al.* show a similar interface for HfO_2/Al_2O_3/InSb. If the results from Trinh *et al.* can be replicated, a combination HfO_2/Al_2O_3 dielectric may offer the most promising route to device improvement.

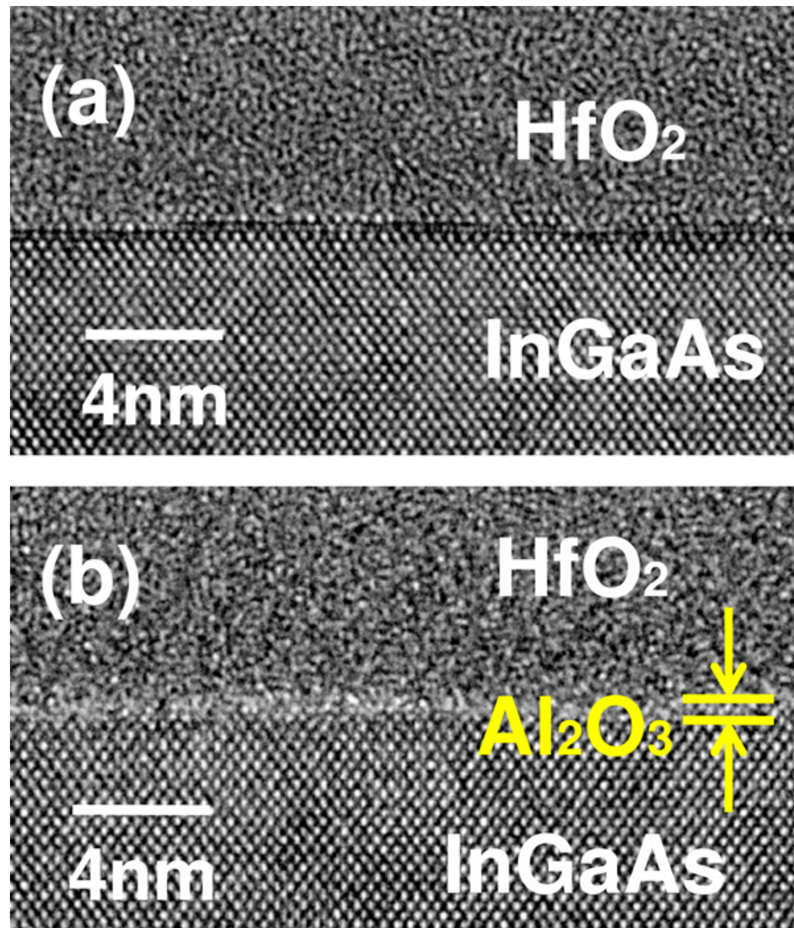

Figure 2.1: TEM images of (a) the HfO_2/InGaAs interface and (b) the HfO_2/Al_2O_3/InGaAs interface. Reproduced from Suzuki *et al.*[40], with the permission of AIP Publishing

2.2.5 Lanthanum Oxide

Lanthanum oxide and other rare earth metal oxides have been the subject of study due to their high dielectric constants. La_2O_3 has a dielectric constant of approximately 30,[22] although it is not chemically stable under normal atmospheric conditions, readily reacting with water and organic molecules to form carbonates and $La(OH)_3$[41]. Several techniques have been attempted to reap the benefits of La_2O_3 while counteracting the downsides. For one, historical work (2006-2009) has focused on alloying La_2O_3 with other dielectrics, most prominently Al_2O_3[33][41]. $LaAlO_3$ has been found to offer a compromise between the high interface quality of Al_2O_3 and the higher dielectric constant of La_2O_3 and HfO_2, with a dielectric constant of approximately 12 in an experiment where the dielectric constants of Al_2O_3 and HfO_2 were measured to be 8 and 17 respectively.[33] The alloys are generally produced by alternating layers of La_2O_3 and Al_2O_3 in the ALD process and, if TMA is used as the first precursor, it may be possible to use a complex layer structure to obtain both the high interface quality of Al_2O_3 and the high dielectric constant of La_2O_3. In contrast with other dielectrics, $LaAlO_3$ presents increased potential for defects within the material, such as antisite defects, and may require more stringently controlled processing[42].

Later work indicated that lanthanum may be capable of passivating surface and interface defects, offering comparable or superior performance to Al_2O_3-based interfaces[43][44]. La_2O_3 films deposited on InGaAs by evaporation and inspected using x-ray photoelectron spectroscopy (XPS) showed significant reduction in Ga_2O_3 and As_2O_x and a moderate reduction in In_2O_3 compared to using HfO_2[43] and Zadeh *et al.* assert that this is due to La passsivating the native oxide, forming III-O-La bond systems. This system has been investigated by a more systematic study, using ALD La_2O_3 on InGaAs, by Chang *et al.*[45]. Chang *et al.* compared La_2O_3 with Al_2O_3 and a series of Al_2O_3/La_2O_3 dielectric stacks with different La_2O_3 thicknesses. La_2O_3 gave the lowest D_{it} - 3×10^{11} $cm^{-2}eV^{-1}$ - but gave high frequency dispersion and was a poor diffusion barrier. The high frequency dispersion was attributed to atomic interdiffusion, although the moisture-induced breakdown of La_2O_3 into $La(OH)_3$ may also be contributing to this effect. When compared to La_2O_3, the Al_2O_3/La_2O_3 stacks showed less $La(OH)_3$ in XPS, less atomic interdiffusion in TEM/EDX and less frequency dispersion. In electrical characterisation, a positive correlation is observed between La_2O_3 thickness in the structure and frequency dispersion and a negative correlation is observed between La_2O_3 thickness and D_{it}. A trade-off is present between frequency dispersion and D_{it}. The thickness of the Al_2O_3 capping layer also affects D_{it}: higher Al_2O_3 thickness results in higher

D_{it}. Chang *et al.* present this result as evidence of interaction and interdiffusion between the Al_2O_3 and La_2O_3 layers. The minimum D_{it} - 1.8×10^{11} $cm^{-2}eV^{-1}$ - is obtained for a thick La_2O_3 layer (2.9 nm) and a thin Al_2O_3 layer (3 ALD cycles, thickness not measured). This device still displayed high frequency dispersion, consistent with other thick La_2O_3 layers.

The La_2O_3-based dielectric system shows promise for interfaces with low D_{it} but also a significant potential issue with raising frequency dispersion. If the results of Chang *et al.* can be replicated for InSb, it may be possible to reduce D_{it} using lanthanum and protect other figures of merit (chiefly frequency dispersion) by capping with other dielectrics, such as Al_2O_3 or HfO_2.

2.2.6 Aluminium Nitride

Aluminium nitride has also been investigated for use as dielectrics and interfacial layers in III-V systems. Krylov *et al.*[46] performed an extensive systematic study comparing Al_2O_3 and AlN as dielectrics on InGaAs and found that AlN can outperform Al_2O_3 under certain conditions. Al_2O_3 was deposited using a thermal ALD process and AlN was deposited using thermal and plasma-enhanced processes, post-metallisation anneal processes were performed at 300°C and 400°C and the resultant MOSCAPs were analysed for D_{it}, frequency dispersion and leakage current. The thermal AlN process was also used to compare Al-first and N-first ALD processes. It was found that AlN had higher frequency dispersion, which showed a higher sensitivity to annealing conditions, but that the best AlN process - plasma-enhanced with a PMA at 400°C - gave a lower minimum D_{it} than the Al_2O_3 process: 1.5×10^{12} $cm^{-2}eV^{-1}$ and 2.5×10^{12} $cm^{-2}eV^{-1}$ respectively. Al_2O_3, however, showed superior I-V performance, with a critical electric field of 7.5 $MVcm^{-1}$ compared to 5.0 $MVcm^{-1}$ for AlN. The Al-first processes outperformed the N-first processes, shown by a smaller 'hump' feature typically associated with interface traps. Krylov *et al.* note that AlN is prone to surface oxidation in the top $\sim$5 nm of the layer, which may account for the reduced performance compared to Al_2O_3.

In addition to continuous AlN layers, AlN has also been investigated as an interfacial layer for Al_2O_3[47] and HfO_2[48] dielectrics. Both processes perform similarly to other dielectric systems, with a minimum Terman D_{it} of 7.5×10^{12} $cm^{-2}eV^{-1}$ and 5.2×10^{12} $cm^{-2}eV^{-1}$ for Al_2O_3 and HfO_2, respectively, on n-type InGaAs. Variants of this system, using p-type substrates and different D_{it} extraction techniques, showed slightly lower D_{it} but no lower than 4×10^{11} $cm^{-2}eV^{-1}$. Luc *et al.*[48] also reported elemental interdiffusion, measured by TEM-EDX: AlN acts as a good diffusion barrier but not significantly better than HfO_2.

Table 2.1: Summary of relative properties of dielectric materials

Dielectric	D_{it}	Dielectric constant	Diffusion resistance	Ease of deposition	Chemical stability
Al_2O_3	Low	9	Low	Easy	Good
HfO_2	High	25	High	Moderate	Good
La_2O_3	Low	30	Very low	Difficult	Poor
AlN	Low	9	High	Difficult	Poor

AlN shows some promise as an interfacial layer and further investigation may offer low D_{it} and a good diffusion barrier. However, reliable deposition of AlN is difficult, as oxygen easily displaces nitrogen during deposition, forming aluminium oxynitride. As mentioned above, the study by Krylov *et al.* implicates oxidation as the cause of higher frequency dispersion, compared to Al_2O_3. Some investigation into AlN is included in this thesis, but lack of suitable deposition equipment limited this to a brief comparison against the core work on Al_2O_3.

2.3 Trap Characteristics

In addition to interface-trapped charge - sometimes described as 'fast' traps due to their short time constants - other trapped charges can interfere with device performance. Schroder[18] describes four types of charge which interfere with MOS systems (as a quantity of charge, Q, a number of states, N, or a density of states, D):

1. Interface-trapped charge (Q_{it}, N_{it}, D_{it})
2. Fixed oxide charge (Q_f, N_f)
3. Oxide-trapped charge (Q_{ot}, N_{ot}, D_{ot})
4. Mobile oxide charge (Q_m, N_m, D_m)

Interface-trapped charge has already been discussed. Fixed oxide charge causes the C-V response to shift in the x (voltage) axis, usually described by the voltage at which the flatband condition occurs (discussed in section 4.2, ideally zero volts) - this is known as flatband voltage (V_{FB}). Mobile oxide charge consists of ionic impurities (typically alkali metals such as Na, K, Li, but potentially also H or heavy metals) which are capable of diffusing through the oxide (with low mobility at room temperature and higher mobility at elevated temperature). Since alkali

metals have been removed from fabrication facilities, mobile charge has been all but eliminated from MOS structures. The remaining oxide-trapped charge consists of neutral or charged defects or impurities in the oxide which, while not fixed, change their occupancy with a much longer time constant than interface-trapped charge. These charges, sometimes also referred to as near-interface charge/traps, slow charge/traps or 'border' traps, play a prominent role in III-V MOS interfaces, giving rise to frequency dependency (frequency dispersion) and hysteresis.

Colleoni, Pourtois and Pasquarello[49] investigated the source of oxide-trapped charge in InGaAs/Al_2O_3 MOSCAPs using modelling techniques. They used density-functional molecular dynamics to model impurities in the oxide - In and Ga displacing Al in the oxide - to rationalise the bimodal distribution of oxide-trapped charge observed in other papers, such as Franco *et al.*[50] and Vais *et al.*[51]. The model provided a good fit to measured data, implicating atomic interdiffusion as a source of oxide-trapped charge.

Lin *et al.*[52] investigate hysteresis in InGaAs/HfO_2 MOSCAPs, particularly focusing on the effects of oxide thickness and bias voltage. Critically, they report a roughly constant density of hysteresis-inducing trapped charge per unit area for oxide thicknesses between 10 nm and 30 nm. They conclude that the hysteresis-inducing charge is present in a plane at or close to the interface, rather than distributed uniformly through the oxide. Lin *et al.* also demonstrate that increased bias stress time and voltage can increase measured hysteresis and that, for long bias stress time, the hysteresis increase plateaus. They conclude that the dependency on bias stress time is due to a 'wide range of [trap] capture cross sections' and that the dependence on bias stress voltage is due to the activation of traps at different energy levels. Lin *et al.* also note that the density of hysteresis-inducing states is comparable to or greater than the density of interface-trapped charge (D_{it}) and highlight the importance of 'slow' states alongside D_{it}.

Yuan *et al.* investigated frequency dispersion using similar model-based methodologies[53][54]. Yuan *et al.* modelled the oxide traps using a 'distributed bulk-oxide trap model', where the total oxide capacitance is broken down into a series of capacitances and a series of admittances, 'ΔY_{bt}' is added, connecting points within the oxide to the substrate. ΔY_{bt} is then defined using time constant models for trapping/detrapping via tunnelling. They confirm that the frequency-dependant effects are consistent with oxide-trapped ('border') charge but they also employ their model to quantify the quantity of oxide-trapped charge, N_{ot}. Similar methodologies have been used by Gu *et al.*[55] and Taoka *et al.*[56], using model-fitting techniques to quantify N_{ot}. Vais *et al.*[51] also use a model-fitting method but their

work highlights a few additional features. They demonstrate the relationship between oxide-trapped charge and hysteresis effects, quoting an equation for quantity of oxide-trapped charge as a function of hysteresis voltage:

$$\Delta N_{eff} = \frac{\Delta V_{FB} C_{ox}}{q} \tag{2.1}$$

Where ΔN_{eff} is the effective trapped charge in cm^{-2}, ΔV_{FB} is the hysteresis in V, C_{ox} is the oxide capacitance in Fcm^{-2} and q is the electron charge. After determining the quantity of charge, a binomial Gaussian energy distribution is then fitted to measured data, similar to previous examples. A similar technique was used by Taoka *et al.*[56] for the measured conductance-voltage response, fitting both D_{it} and N_{ot} to the measured data.

Despite the widespread use of model fitting techniques, they are not ideal for data extraction, as they rely on the implementation and fitting of an additional oxide-trapped charge model. The hysteresis-based data extraction demonstrated by Vais *et al.* may present opportunities to extract N_{ot} data without an oxide-trapped charge model, streamlining data extraction and allowing N_{ot} data to be extracted routinely.

Further papers have provided details and more complete pictures of trap characteristics. Tao *et al.*[57] studied frequency dispersion for high-κ dielectrics on silicon. In addition to behaviour already described in this section - a 'lossy interfacial layer' - they also discussed how frequency dispersion can be induced by parasitic impedance - common for Si bulk material and ohmic contact cases but less common in narrow bandgap III-V systems - and by intrinsic properties of the dielectric layer. In the case of the complex ternary dielectrics studied in the paper - $La_xZr_{1-x}O_3$ and $Ce_xHf_{1-x}O_3$ - frequency dispersion was observed in the dielectric constant of the dielectric itself, although this should not be the case for the simple binary, stoichiometric Al_2O_3 and HfO_2 which this project is based on ($LaAlO_3$ may display intrinsic frequency-dependent behaviour). It should be noted that Tao *et al.* observed that binary ZrO_2 did not display a frequency-dependent dielectric constant at the frequencies of a C-V measurement. Tao *et al.* also investigated surface roughness as a potential cause of frequency dispersion but concluded that roughness was not responsible for the frequency dispersion.

Vais *et al.*[58] observed temperature dependency in frequency dispersion for III-V MOSCAPs. They showed lower frequency dispersion at lower temperature for a range of dielectrics, including Al_2O_3 and HfO_2 on InGaAs and InP and investigated potential mechanisms for these observations by modelling the trapping of

charge. They used a simplified model for trap capture cross-section and time constant based on a more sophisticated non-radiative multi phonon model and thus described a combination of tunnelling and thermally-activated trapping phenomena as the source of frequency dispersion. These findings suggest that the cryogenic C-V measurements required for InSb characterisation will underestimate frequency dispersion, compared to room temperature operation. Kadoda *et al.* [59] fabricated Al_2O_3/InSb MOSCAPs - some grown on Si but some grown on InSb, all characterised at cryogenic temperature - with hysteresis response displayed. The Al_2O_3/InSb system displayed a large hysteresis voltage for the DC sweep range: approximately 1.85 V of hysteresis for a DC sweep from -8 V to +5 V, or 0.14 V/V. As a final point to note, Taoka *et al.*[60] discussed the role of traps with energy levels above the conduction band edge and noted that traps above the conduction band edge can affect C-V response and must also be considered for an optimal MOS system.

2.4 Pre-deposition Processing

A significant improvement to the interface properties of InSb may be achieved through the use of pre-deposition cleaning treatments. Wet ex-situ treatments are the most obvious route to clean surfaces but, in particular because of InSb's rapid surface oxidation, in-situ treatments based on reactive precursor gas and in-chamber plasma may offer superior interfaces compared to wet treatments alone.

2.4.1 Wet Treatments

A range of wet treatments have been attempted to improve III-V dielectric interfaces. Hou *et al.*[36] demonstrate the use of CP4A etchant solution (acetic, nitric, hydrofluoric, water in a ratio of 1:2:1:10) as a cleaning agent on InSb. They demonstrate a superior native oxide removal process compared to a TMA clean alone, with x-ray photoelectron spectrometry (XPS) measurements showing no detectable amount of native oxide remaining. Hou *et al.* also show C-V characteristics of the fabricated structures, with the CP4A-cleaned sample showing a rise in capacitance at highly negative gate voltages when compared to the other samples, which could be interpreted as the onset of inversion. Hou *et al.* explain this by trap states arising from loss of stoichiometry, citing Barber and Heasell[61]. The presence of additional trap states would conflict with the positive results of the XPS measurements and D_{it} calculation, casting the hypothesis into doubt.

Table 2.2: Summary of process differences between Trinh and Brammertz

Parameter	Substrate	Deposition conditions	Post-deposition processing	D_{it} extraction technique
Trinh *et al.*[62]	InAs	200°C	N_2, 400°C, 30 s	Hill's method
Brammertz *et al.*[68]	GaAs	300°C	FG, 380°C, 30 s and FG, 400°C, 30 min	Conductance method

In addition to the CP4A solution, Trinh *et al.*[62] and Wu *et al.*[63] have demonstrated the use of hydrochloric acid (HCl) for native oxide removal. Trinh *et al.* quantitatively compared HCl to sulphide treatment and no ex-situ cleaning, where all 3 samples received TMA cleaning in-situ. The HCl treatment offered the lowest D_{it}, leakage current and frequency dispersion of the 3 treatments, suggesting it can be used effectively to improve interface performance. Wu *et al.* do not include comparable figures, instead citing contact resistance figures and MOSFET device parameters. Surface science studies - XPS, Auger electron spectroscopy (AES), low-energy electron diffraction (LEED), electron energy loss spectroscopy (EELS) etc. - have been performed by Tereschenko *et al.* on GaAs[64] and InSb[65]. Both studies showed that, when HCl cleaning and sample transfer were performed in a dry nitrogen atmosphere, HCl cleaning reduced native oxide below the detection limit of XPS but induced a thin group III chloride surface layer ($GaCl_3$/$InCl_3$). They also showed that surface V:III ratio could be manipulated by UHV annealing, bringing surface stoichiometry closer to 1:1 and simultaneously eliminating the group III chloride. An alternative acid process was presented by Kent *et al.*[66], using the fluorine-based buffered oxide etch (BOE). BOE did give lower D_{it} than no process but the difference was small - no greater than other wet treatments - and BOE failed to significantly reduce oxide-trapped charge.

Sulphidation treatments have been used on III-V substrates to aid surface passivation. The sulphidation process acts as cleaning and pre-treatment, removing the deleterious native oxide by displacing oxygen from the surface and reducing the density of trap states when the dielectric is deposited. Bessolov and Lebedev offer an overview of the benefits of sulphidation and selenidation treatments,[67] with the improvement of metal-insulator-semiconductor and p-n systems being of particular interest for this project. The rest of this review focuses on the more widely studied sulphidation treatment rather than selenidation treatment.

Pre-treatment processes were studied and published by Trinh *et al.*[62] on InAs and Brammertz *et al.*[68] on GaAs, with the results summarised in table B.1 in ap-

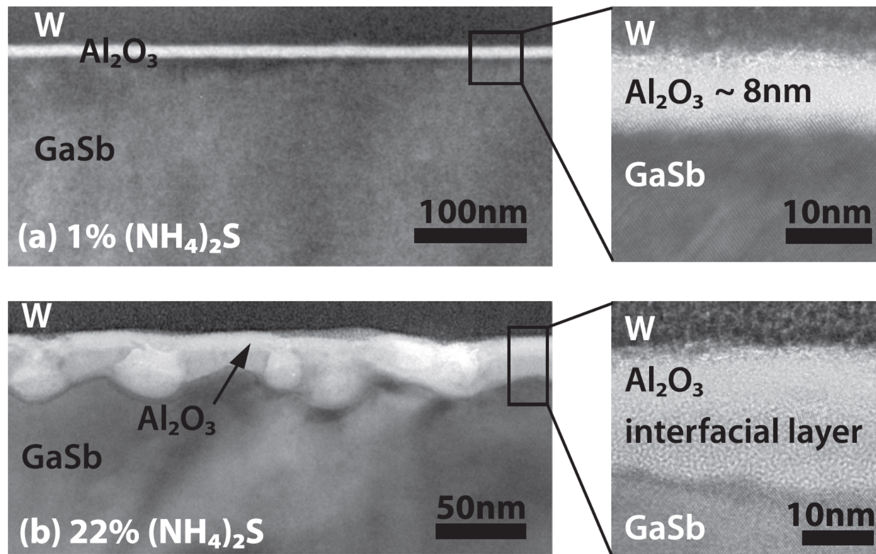

Figure 2.2: Cross-sectional TEM micrographs of (a) 1% and (b) 22% $(NH_4)_2S$ treated W/Al_2O_3/p-GaSb samples. Reproduced from Peralagu *et al.*[70], with the permission of AIP Publishing

pendix B. Trinh *et al.* observed that HCl etch pre-treatment gave MOSCAP devices with superior leakage performance and marginally superior D_{it} when compared to a comparable sulphidation process. In contrast, Brammertz *et al.* reported a sulphidation process superior to HCl cleaning, with a noticeably higher D_{it} observed in the HCl sample throughout the bandgap: $\sim 1.5\times$ higher in n-type material near the conduction band edge and approximately an order of magnitude in p-type material near the valence band edge. Several factors could explain this discrepancy, as summarised in table 2.2. The factor of greatest significance is the post-deposition processing: Brammertz *et al.* performed a short annealing process on the HCl-cleaned sample and a long annealing process on the sulphide-treated sample. As explained in section 2.5 below, annealing in forming gas is conventionally used to reduce D_{it} and could explain the discrepancy between these results. A study of sulphidation process parameters was done by Brennan *et al.*[69] - temperatures from room temperature to 60°C, times of 10 and 20 mins and solution concentrations of 5 to 22% on InGaAs - and they found treatment in 10% ammonium sulphide solution at room temperature for 10 minutes offered the best results of the processes studied. Brennan *et al.* also include an inventory of literature on sulphidation treatments covering a wider range of parameter space.

The sulphidation process has known shortfalls, particularly the stability of the passivating layer. When exposed to high-intensity light, a reaction occurs at the treated surface and the performance benefit associated with the sulphidation treat-

ment diminishes permanently[67][71]. Bessolov *et al.*[67] cite some structures and systems - e.g. InP passivated surfaces and GaAsSb photodiodes - more resistant to radiation damage but these systems still show light sensitivity and a performance lifetime of less than 1 year. This degradation mechanism is particularly critical for this project, as the passivation process would be included in infrared emitters and detectors. Even if the infrared radiation associated with device operation does not affect the sulphur passivation, the device may need additional encapsulation to be sheltered from the ambient light of the environment. It has also been observed that the sulphur layer at the surface undergoes chemical changes when exposed to high temperatures[72], which raises concerns for the treatment's compatibility with annealing processes. Peralagu *et al.*[70] studied a range of sulphidation treatments on GaSb and, while most treatments offered superior performance to the untreated control sample, the lowest concentration of ammonium sulphide (1%) offered the best treatment and higher concentrations (10% and 22%) gave lower capacitance swing and higher flatband voltage. TEM figures from Peralagu *et al.* are shown in figure 2.2: the higher sulphide concentrations introduced a thick interfacial layer, in comparison with the abrupt interface of the 1% treatment. This thick interfacial layer appears to be deleterious to device performance and recalls the other shortcomings of sulphidation treatments. Finally, although sulphur is expected to act as an n-type dopant in III-V materials, this effect and its potential consequences have not been discussed in publication.

Additional processes based on alkaline chemistry have been emerging over the past few years. Sakong *et al.*[73] used tetramethylammonium hydroxide (TMAH) as a wet passivation treatment on gallium nitride (GaN), resulting in D_{it} dropping from 2.8×10^{12} cm^{-2}eV^{-1} to 1.1×10^{11} cm^{-2}eV^{-1} and N_{ot} dropping from 5.4×10^{19} cm^{-3}eV^{-1} to 2.5×10^{19} cm^{-3}eV^{-1}. While this improvement is substantial, the context must be accounted for, as these measurements were performed on recessed-gate MOSFET structures, not planar MOSCAPS. The TMAH was specifically selected to compensate the damage induced by the dry etch process used to form the recessed surface, acting as a slow anisotropic etch. A more standard interface study was conducted by Lechaux *et al.*[74], exploring the effect of both ammonium hydroxide and oxygen plasma on InGaAs MOSCAPs using electrical measurements and XPS. For the electrical characterisation, the ammonium hydroxide process was not compared to a control but performed well, giving a D_{it} of 6×10^{11} cm^{-2}eV^{-1} without the oxygen plasma process. In XPS, the ammonium hydroxide was shown to effectively reduce native oxide components, eliminating the As_2O_5 component completely. Xu, Wang and Ye[75] present another device structure fabricated using an alkali process: HCl

followed by ammonium hydroxide on a GaSb surface. They assert that, while the HCl removed the native oxide from the sample, the ammonium hydroxide removed elemental Sb - this would eliminate group V dimer bonds and may move the stoichiometry towards equilibrium. Further work on alkali processes, particularly in combination with acid processes, may offer an effective route to good ex-situ surface preparation.

2.4.2 Gas Treatments

This review has already mentioned the use of in-situ TMA cleaning: cycling the aluminium precursor of the ALD reaction over the substrate surface has been shown to remove surface contamination and improve device performance[36][62][76]. The mechanism by which the TMA cleans the surface is unclear Hou *et al.*[36] assert that a ligand substitution reaction occurs, with the group III and group V atoms from the native oxide undergoing substitution with the aluminium from the TMA, forming a stable and reliable Al_2O_3 layer and removing the group III and V atoms in volatile complexes. However, Klejna and Elliot propose a wider range of reaction pathways and suggest that multiple mechanisms may be responsible for the cleaning effect[76].

The benefits of TMA cleaning are demonstrated by Suzuki *et al.*[40] and Trinh *et al.*[38] for HfO_2/Al_2O_3 dielectric systems on InGaAs and InSb, respectively. Both papers include high resolution TEM images which show the Al_2O_3 interfacial layer (the image from Suzuki *et al.* is reproduced in figure 2.1 and similar to the image in Trinh *et al.*), electrical measurements and D_{it} responses, which demonstrate the performance of these systems (and, for Suzuki *et al.*, their benefits over a HfO_2-only system). Trinh *et al.* also show XPS measurements, which demonstrate the reduction in native oxide components associated with native oxides, reproduced in figure 2.3. Note that, although the O 1s feature obscures the native Sb_2O_x feature at the strong Sb $3d_{5/2}$ emission energy (shown on the right), native Sb_2O_x can still be observed and analysed using the weaker Sb $3d_{3/2}$ feature, visible on the left.

A more in-depth study was performed by Hwang, Engel-Herbert and Stemmer[77], investigating nucleation of HfO_2 on untreated and TMA-treated surfaces and the electrical response of the resulting MOSCAPs. SEM images showed that TMA pre-treatments aid nucleation on a group-V-rich (2×4) surface (acting as a surfactant) but that this effect is not observed for the group-III-rich (4×2) surface. Electrical characterisation highlighted several features, most prominently that TMA doses with a higher pressure, time and temperature resulted in poorer interfaces than low temperature, low pressure doses. The optimal process gave qualitatively better

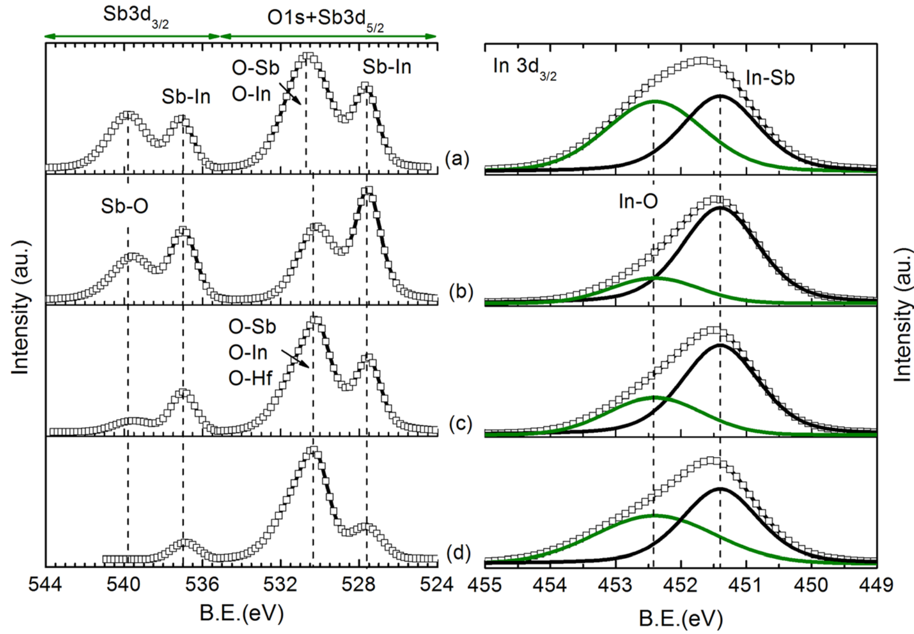

Figure 2.3: In $3d_{5/2}$ and Sb 3d plus O 1s XPS spectra of (a) native InSb surface, (b) as HCl treated InSb surface, (c) as deposited HfO_2/InSb interface, and (d) HfO_2/InSb interface after annealing at 250°C, in N_2, for 30 s. Reproduced from Trinh *et al.*[38] , with the permission of AIP Publishing. Fitted components shown in the right-hand pane for In-Sb (black) and In-O (green).

C-V responses and a minimum D_{it} of $6{\times}10^{12}$ cm^{-2}eV^{-1}.

When considering alternative gas treatments, La may offer similar benefits to Al, as discussed in section 2.2.5. Little else has been reported for ALD processes, particularly as the chemistry involved in ALD is sensitive and easy to disrupt during the deposition process, although Liu *et al.* report a deposition process aided by forming gas[78]. Their letter, however, lacks detail in fabrication and analysis procedures, particularly their deposition process which is described only as 'molecular-atomic deposition', an expression which has not been used or reported elsewhere. They display superior electrical and D_{it} performance for their forming gas-enhanced processes compared to their control, suggesting the inclusion of hydrogen may aid passivation.

2.4.3 Plasma Treatments

In addition to ex-situ wet treatments and in-situ gas treatments, in-situ plasma pre-treatments have also been investigated. Koh *et al.*[79] show a typical plasma pre-treatment: an InGaAs substrate was given a wet HCl treatment and loaded into the ALD system, where it was exposed to an Ar plasma induced with the low power of 20 W. After this process, a dielectric and gate stack were deposited, patterned etc. When compared to a sample prepared without the Ar plasma treatment, the

plasma treatment showed lower D_{it} (9×10^{11} cm^{-2}eV^{-1} to 6×10^{11} cm^{-2}eV^{-1}), V_{FB}, hysteresis (approx. 0.075 V/V to 0.05 V/V) and drift in threshold voltage under voltage stress conditions. Koh *et al.* investigated their samples using XPS and revealed a potential source/mechanism for this improvement: the XPS component for As_2O_3 was reduced by the plasma treatment to less than half its untreated magnitude, and the Ga_2O_3 component was reduced slightly as well. Koh *et al.* assert that the Ar plasma treatment reduces residual native oxide, resulting in a superior interface compared with HCl treatment alone.

There is limited information in the literature regarding alternative plasma gases. Chobpattana *et al.*[80] compare N_2 and H_2 plasma pre-treatments on InGaAs and found a clear difference: nitrogen plasma resulted in a consistently lower D_{it} for both continuous HfO_2 and HfO_2/Al_2O_3 layered dielectrics, reduced from a minimum of 1×10^{13} cm^{-2}eV^{-1} to one of 2×10^{12} cm^{-2}eV^{-1}. By contrast, Luc *et al.*[48] show no significant difference between a N_2/H_2 post-deposition plasma process and a NH_3 one on InGaAs. The ionised species are likely to be similar between the two processes - it may be that the mere presence of ionised or radical nitrogen and/or hydrogen is the critical factor of the treatment, rather than specific plasma species. The findings of Luc *et al.* may also have been influenced by the plasma process being performed after dielectric deposition, as opposed to Chobpattana *et al.*, who performed it before. The gas/plasma atoms are likely to interact with the interface through the ∼4 nm dielectric but the interface may be sheltered from low energy plasma species.

Plasma treatments show great promise for combined use with reactive gas treatments. Carter *et al.*[81] investigated the effects of TMA gas treatment (5 cycles), H_2 plasma treatment and a combination treatment utilising both H_2 and TMA, all on InGaAs substrates after a HCl dip. The TMA treatment alone gave a D_{it} of 4.6×10^{12} cm^{-2}eV^{-1} at 0.2 eV below the conduction band edge, practically identical to the control sample without gas/plasma treatment. The H_2 plasma improved the D_{it} to 2.5×10^{12} cm^{-2}eV^{-1} and the combination H_2/TMA treatment improved it further, to 1.7×10^{12} cm^{-2}eV^{-1}. A similar result was reported by Kent *et al.*[66], showing combination TMA and H_2 plasma treatments on InGaAs outperforming H_2-only treatments at deposition temperatures of both 120°C and 300°C. Kent *et al.* also showed that a larger number of treatment cycles (10) produced a lower D_{it}, although N_{ot} was minimised for a 5-cycle treatment.

When applied to other substrates, plasma treatments have demonstrated dramatic improvements, far greater than the improvements seen on InGaAs substrates. Ruppalt *et al.*[82] applied a 1:7 H_2/Ar plasma treatment to p-type GaSb grown in-

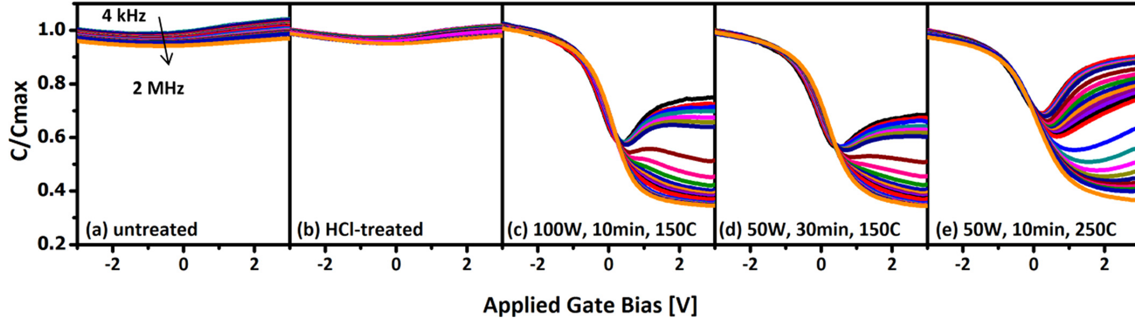

Figure 2.4: Variable frequency C-V sweeps for GaSb/Al_2O_3 MOSCAPs with the following treatments prior to dielectric ALD: (a) no treatment; (b) HCl wet etch; (c) 100 W, 10 min, and 150 °C H_2/Ar-plasma exposure; (d) 50 W, 30 min, 150 °C H_2/Ar-plasma exposure; and (e) 50 W, 10 min, and 150 °C H_2/Ar-plasma exposure. Reproduced from Ruppalt *et al.*[82], with the permission of the American Vacuum Society

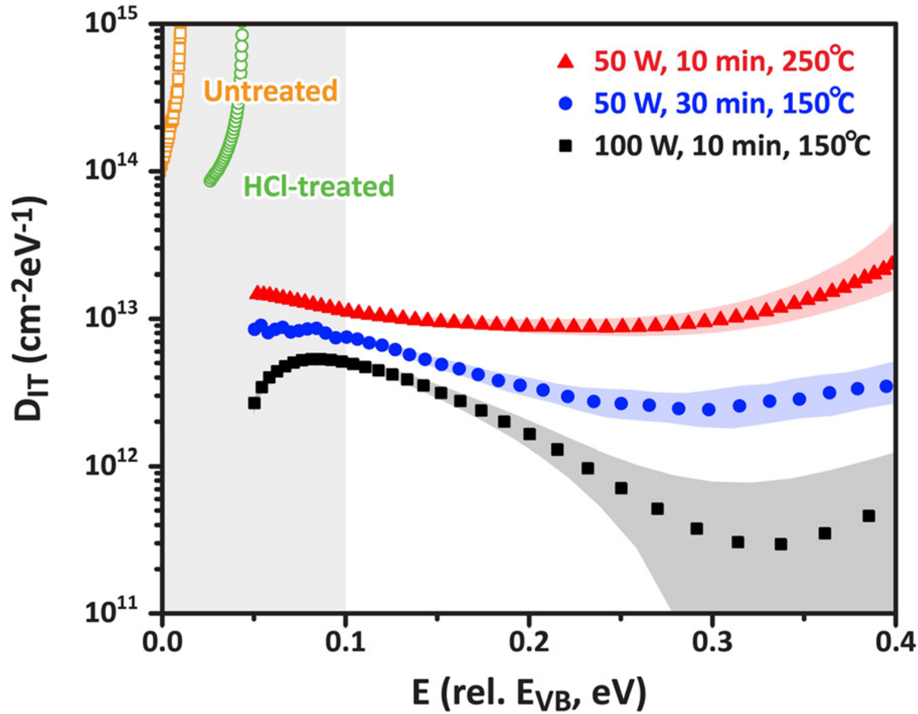

Figure 2.5: Density of interface trap states, D_{it}, estimated using Terman's method for GaSb/Al_2O_3 MOSCAPs undergoing various treatments prior to ALD. Dark shaded regions along plasma-treated sample plots indicate variation in estimated D_{it} assuming 10% deviation from calibrated N_A. For energies, E<0.1 eV, valence band states may contribute to measured capacitance and calculated D_{it} within that region are interpreted as approximate minimum levels. Reproduced from Ruppalt *et al.*[82], with the permission of the American Vacuum Society

house and not given any wet treatment. The plasma-treated samples were compared to an untreated control and to a sample treated with HCl only. The C-V responses are shown in figure 2.4 and the D_{it} profiles in figure 2.5. Without the plasma treatment, the MOSCAP devices show almost no charge modulation, whereas the samples with plasma treatment show much greater charge modulation and D_{it} reduced by, in the most extreme cases, two orders of magnitude. The treatment conditions were highly variable, with plasma power, exposure time and temperature varying across the three treatments in an unsystematic way and it is, therefore, difficult to determine where the most promising region in parameter space is for this process. Finally, Ruppalt *et al.* show a reduction in Sb_2O_x using XPS which is consistent with the reduction in As_2O_3 shown by Koh *et al.* which, again, is implicated in the improved electrical performance.

Thayne *et al.*[83] applied a series of plasma and gas treatments to $Ga_{0.7}In_{0.3}Sb$, using H_2 plasma rather than Ar and using higher plasma power (150 W and 250 W). They observe deterioration in capacitance modulation and frequency dispersion (without reporting D_{it}) for all processes except the 250 W plasma, followed by a TMA treatment. Their results imply that plasma power of 150 W or greater can result in deterioration, although this may not be a valid conclusion. Their study likely used the cluster tool sited in Glasgow, with their plasma process being performed in an ICP chamber rather than an ALD chamber. ALD plasma processes usually filter energetic charged ions using an electrically earthed grating between the plasma and sample and, as such, performing the treatment in an ICP chamber may have resulted in additional damage to the sample. Thayne *et al.* also report that performance improved significantly following an anneal process, suggesting that the sample may have been damaged and the damage subsequently relieved by the anneal.

Cho *et al.*[84] applied a treatment similar to Rupplat *et al.* to GaN, with similarly dramatic results. Ar plasma treatments were applied to solvent-cleaned GaN grown on Si by MOCVD and analysed by C-V and conductance techniques. The optimal Ar plasma treatment - 50 W exposure for 5 min - gave a D_{it} two orders of magnitude lower than the untreated control sample, frequency dispersion one order of magnitude lower and hysteresis reduced from 0.25 V to 0.07 V. It should be noted that the D_{it} was extracted using the conductance method and the conductance peak used to characterise D_{it} changed voltage position as well as magnitude after the Ar plasma pretreatment. This implies that the treatment reduced D_{it} within a specific energy region in the bandgap - presumably a region characteristic of a specific bond/trap state - resulting in the conductance method being dominated by trap

states in a different region of the bandgap (further from the conduction band edge).

Despite the dramatic results achieved using plasma treatments, no investigations have been reported on the mechanism for improved performance. The treatments may be affecting the substrate by chemical action (e.g. etching, passivation), physical action (e.g. sputtering) or by UV action. To understand how these processes contribute to surface interaction, the configuration of plasma induction kits for ALD must be discussed. Profijit *et al.*[85] present a review of plasma ALD configurations and note that the majority of modern plasma ALD instruments, including the popular Oxford Instruments OpAL and FlexAL and Cambridge Nanotech/Ultratech Fiji systems, use a remote inductive-coupled plasma (ICP) configuration. In this configuration, the surface is exposed to ions and radicals from the plasma, normally without filtering, but there is a degree of isolation, allowing plasma and substrate conditions to be varied independently. This configuration does not normally allow direct manipulation of bias/potential difference between the plasma and the substrate, although the plasma potential can be affected by plasma pressure and power. The contrast between this configuration and that of ICP plasma systems should be noted: in ICP plasma systems, the ions are accelerated towards the sample surface to aid material removal.

When considering physical action, Koh *et al.*[79] assert that charged Ar ions break III-oxygen and V-oxygen bonds at the surface but, beyond presenting a figure, this assertion is not elaborated and the role of other actions (principally UV action) are not considered. If the treatment is, indeed, dominated by physical plasma action, it would follow that damage from such an indiscriminate process could offset the benefits of breaking down surface oxides, dimers etc. This is reflected in Cho *et al.*[84], where the optimal treatment was performed at the lowest power - a potential contradiction appears in Ruppalt *et al.*[82] where the optimal treatment had a higher power but it also had a shorter duration/lower temperature than other processes.

Chemical action may be significant: Chobpattana *et al.*[80] showed that H_2 plasma and N_2 plasma had different effects on the samples. If the treatment were dominated by chemical action, this would also explain the observations of Luc *et al.*[48]: both N_2/H_2 and NH_3 plasmas could be reliant on the chemistry of nitrogen and hydrogen. However, this fails to account for the observations of Ruppalt *et al.* and Cho *et al.*: both demonstrated two orders of magnitude improvement in D_{it} using argon plasma, which has no chemical interactions with the substrate at the temperatures and pressures of ALD. Furthermore, when Barth *et al.*[86] applied a H_2 plasma treatment to GaSb, the result was poorer than the chemically-inactive Ar plasma process shown by Ruppalt *et al.*.

Plasmas emit photons at UV wavelengths and UV photons possess energy of the same order of magnitude to most chemical bonds, allowing UV sources to break bonds in processes such as UV-initiated CVD and ALD. This raises the possibility that UV light emitted from the induced plasma may be breaking bonds (e.g. oxides and dimers) at the substrate surface. If the treatment were dominated by UV action, this would explain the effectiveness of Ar processes on GaSb and GaN while also explaining the differences and similarities between treatments using different plasma compositions. It might also explain the differences between substrates, as even a small change in bond enthalpy could result in UV photons gaining or losing the ability to break the bonds.

Plasma treatments present significant opportunities to improve interfaces, as they have demonstrated dramatic improvements in III-V dielectric systems. The mechanism for these processes are still unclear, however, and a wide range of experiments could clarify the role that different parameters and potential interaction mechanisms play in surface preparation.

2.5 Post-deposition Processing

After dielectric deposition, additional processes can be performed to improve performance, most prominently annealing (i.e. thermal or chemical treatments at elevated temperature). Elevated temperature allows diffusion of atoms and molecules, allowing solid materials to re-organise, gas species to diffuse towards active sites and some endothermic chemistry, which would not be possible at room temperature, to activate. For MOS devices, the most common process is annealing in hydrogen or forming gas (5% H_2 and 95% N_2) as a chemically reducing atmosphere, used in the Si-SiO_2 system for decades to reduce D_{it} and V_{FB} by passivating dangling bonds and oxide trap states[18]. Inert gases, such as nitrogen and argon, can be used when only thermal effects are desired and oxidising atmosphere (e.g. O_2 gas) can also be used. Annealing can be done as a long-duration process - in a tube furnace, typically lasting minutes, hours or days - or as a short-duration process using a rapid thermal annealing (RTA) instrument, typically lasting seconds or a few minutes.

The chemistry of annealing and post-deposition processes must be considered carefully: it must not be assumed that the optimal passivation methods for silicon and III-V materials are identical. Trinh *et al.*[87] compared nitrogen and hydrogen post-deposition annealing (PDA) processes on InGaAs: although quantitative D_{it} values are only provided for nitrogen processes, the hydrogen process qualitatively performs much better, showing greater capacitance modulation at low and high fre-

quencies and no prominent 'hump' features, which implies a low D_{it}. Trinh *et al.* also show XPS data, which shows that H_2 annealing reduces native oxide components, most notably in the Ga and As spectra. Hong *et al.*[19] report a range of annealing processes, principally for Ga_2O_3/Gd_2O_3, with some results reported for ALD Al_2O_3 annealed in O_2. For Ga_2O_3/Gd_2O_3, the forming gas process resulted in higher D_{it} than nitrogen, helium and oxygen processes but the comparison was not like-for-like. The forming gas process being performed at 450°C, compared to 600°C for the He and O_2 processes and 750°C for N_2 (the best process reported) - it may not be correct to conclude that forming gas is an inferior process and Hong *et al.* state that forming gas performed better at a temperature of 375°. Hong *et al.* report that, for a He ambient, higher temperatures up to 600°C produce lower D_{it} but a low-temperature anneal in He at 450°C increases D_{it} compared to no annealing treatment. Finally, Hong *et al.* show that an O_2 anneal process performed on ALD Al_2O_3 had minimal effect on leakage current density, without reporting D_{it}. A similarly inconclusive result was reported by Lechaux *et al.*[74] for an O_2 plasma post-deposition process on InGaAs: although leakage current and qualitative indicators show noticeable improvement, frequency dispersion and conductance D_{it} became poorer after the process (8×10^{11}, compared to 6×10^{11} before). It is concluded that there is insufficient evidence on oxygen post-deposition treatments and they should be investigated in parallel with inert and reducing processes.

A different kind of study was conducted by Burek *et al.*[88], investigating the influence of post-metallisation annealing for different metallisation processes. Thermal evaporation and electron beam (e-beam) evaporation were used to deposit gate metal and forming gas was used to anneal the samples after deposition. Burek *et al.* found that e-beam evaporation without annealing caused damage to the samples (presumably caused by x-ray radiation from the energetic e-beam interactions), increasing D_{it} to 1.1×10^{13} compared to 5.7×10^{12} by thermal evaporation. After annealing in forming gas at 400°C for 50 mins, the thermal evaporation samples had slightly reduced D_{it} (3.4×10^{12}) and the e-beam samples had significantly reduced D_{it} ($<5.2\times10^{12}$), approximately in line with the thermal process. From these observations, Burek *et al.* surmise that the improvements from the annealing process are predominantly due to annealing out damage from the gate metal deposition, rather than chemical passivation by hydrogen, as in a Si-SiO_2 system, and this would mean that the thermal component of the process dominates the chemical component.

Annealing treatments have a large parameter space - temperature, time, gas composition, flow rate, in-situ/ex-situ etc. - and processes can be difficult to optimise, with temperature playing a critical role. Trinh *et al.*[89] investigated a series

of post-deposition anneal treatments for InAs/InGaAs with a HfO_2 dielectric, from 400°C to 550°C in forming gas for 5 mins. They found that the optimal temperature was 500°C but that performance degraded at 550°C - XPS suggests this may be due to increased As-As dimer defects or In_2O_3 but atomic interdiffusion, discussed in sections 2.2 and 2.3 may also be contributing. This is reinforced by comparing a number of papers investigating GaSb and InSb. Wang *et al.*[37] observe a tradeoff between D_{it} and N_{ot}: their anneal process at 600°C in N_2 for 30 s lowers N_{ot} but raises D_{it}. This is corroborated by Xu, Wang and Ye[75], who observe that, for a p-MOSFET process, the lowest thermal dose (600°C 30 s implant activation, 200°C deposition) outperformed the higher thermal doses (600°C 30 s, 300°C maximum), reducing conductance D_{it} from 2.9×10^{13} cm^{-2}eV^{-1} to 1.5×10^{13} cm^{-2}eV^{-1} and increasing channel mobility. Despite increases in D_{it}, annealing has proven effective at reducing fixed charge and oxide-trapped charge, particularly in GaSb. In addition to Wang *et al.*, Nainani *et al.*[90] show a process of forming gas at 350°C for 30 mins to reduce V_{FB} and hysteresis to almost zero, reportedly by passivating oxygen dangling bonds without encouraging 'intermixing at the semiconductor/dielectric interface and desorption of hydrogen at higher temperatures'.

The effect of diffusion is exaggerated in III-Sb materials: antimony bonds to group III and group V elements more weakly than arsenic does, resulting in lower melting points[6] and a tendency for Sb to diffuse out of the lattice. This effect is further exaggerated for InSb, as the In-Sb bond is weakest and results in the lowest melting point of any binary III-V semiconductor. Trinh *et al.*[91] performed electrical characterisation on InSb after annealing processes at 300°C, 350°C and 400°C in N_2 for 30 s but, unfortunately, analysis was only performed at room temperature, limiting its effectiveness (see section 3.10 for further details). The only figure of merit likely to be reliable at such high temperature is low-frequency capacitance modulation and this deteriorates after all 3 annealing processes. Frequency dispersion and hysteresis are also reported - although these figures of merit are highly unreliable at room temperature, it is interesting to note that they show little-to-no deterioration after the 300°C process, although higher temperatures cause both parameters to deteriorate. It is highly likely that InSb will suffer severely from atomic interdiffusion at temperatures above 300°C - Eftekhari[92] discusses the mechanism within anodic oxides as an explanation for improvement and deterioration in I-V response after several annealing processes.

The clearest conclusion to be drawn on annealing processes is best demonstrated by Luc *et al.*[93]. Luc *et al.* performed a systematic study of anneal processes on InGaAs, covering a temperature range of 300°C to 400°C, using N_2 and FG

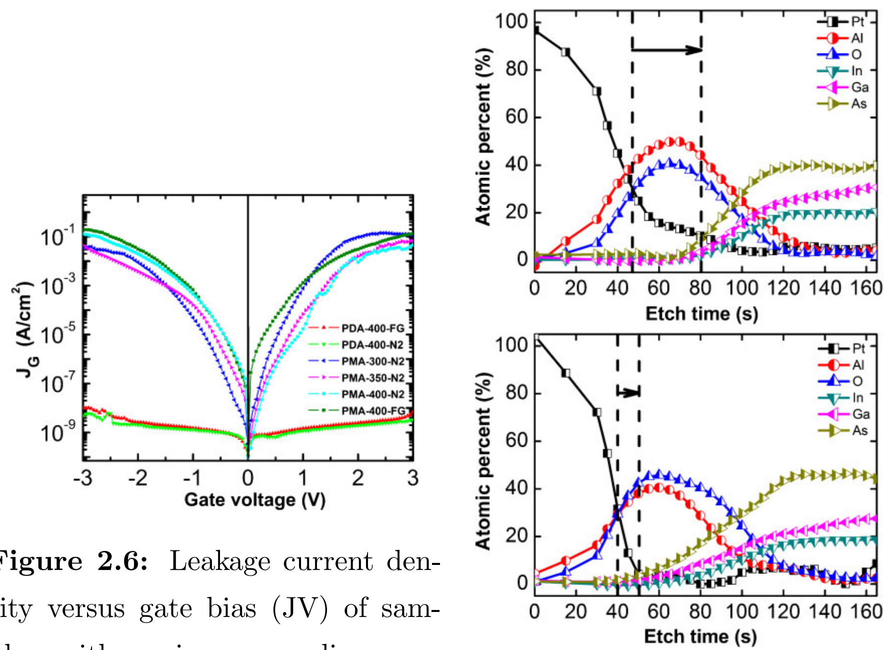

Figure 2.6: Leakage current density versus gate bias (JV) of samples with various annealing processes. Reproduced from Luc *et al.*[93], with the permission of the Japanese Society of Applied Physics

Figure 2.7: The Auger depth profiling analyses of (above) sample annealed after gate formation and (below) sample annealed before gate formation. Reproduced from Luc *et al.*[93], with the permission of the Japanese Society of Applied Physics

atmospheres and performed as both post-deposition (PDA) and post-metallisation (PMA) processes. Little quantitative data is reported: the PDA-400°C processes in N_2 and FG gave conductance D_{it} values of 1.5×10^{12} cm^{-2}eV^{-1} and 1.375×10^{12} cm^{-2}eV^{-1} respectively. Hysteresis is reduced by: increasing temperature, changing from N_2 to FG and changing from PMA to PDA - from a maximum ΔV of 117 mV, for the PMA-300°C-N_2 process, to a minimum of 40 mV for the PDA-400°C-FG process. A greater volume of qualitative data is reported: leakage current density and Auger depth profiles are reproduced in figures 2.6 and 2.7 - PDA noticeably outperforms PMA in leakage current, with little difference between temperature/gas variations, and depth profiling shows reduced gate metal diffusion for the PDA process. All the data, including data from other papers, highlights that annealing is sensitive to changes in all dimensions of the parameter space, sometimes resulting in only small changes, as multiple mechanisms (chemistry, diffusion, stress relief etc.) trade off against each other. The methodology for studying annealing and post-deposition processing is critical and it is essential to study processes systematically if valuable data is to be gathered, particularly for InSb, which lacks annealing results in current literature and is likely to be highly sensitive to thermal budget.

2.6 Characterisation

The outcomes of an experiment depend on the experimental conditions but they also depend on measurement and data processing techniques. The process of extracting a D_{it} value is quite involved, with several available techniques potentially offering different results. The basics of D_{it} extraction are covered by Schroder[18], elaborated in chapter 4 of this thesis and outlined in brief below:

2.6.1 Methods

C-V measurements determine D_{it} by a comparison between a trap-free response and a response which includes traps, with two methods being widely used. The high-low method (also known as the Castagné-Vapaille method) compares a high-frequency C-V response, which is assumed to include no AC trap response, and a low-frequency response, which is assumed to include full AC trap response. The Terman method compares a high-frequency C-V response, with no AC trap response but with DC trap response, and a theoretically calculated C-V response, naturally free of traps. The energy level of the traps can be determined from the gate bias, although the relationship between gate bias and surface potential can be difficult to extract. The traditional method of extracting the surface potential (and therefore, the energy

level of the traps) is an integral equation proposed by Berglund[94], although other methods, such as calculations from carrier concentration models, can also be used to determine trap energy levels.

Conductance methods rely on the time constant of the trap states. When conductance is normalised with respect to frequency ($\frac{G_P}{\omega}$) and plotted as a function of frequency, a maximum can be observed when the applied frequency is equal to the characteristic response time/frequency of the active traps at a given gate bias. When this condition is met, D_{it} can be calculated for one energy level and the process can be extended to different energy levels by changing the gate bias.

Charge pumping methods use a MOSFET structure rather than a MOSCAP structure. The source and drain of the MOSFET are connected together with a small bias voltage applied and the current flow between source/drain and the remote bulk contact is measured. The gate voltage is then varied, causing the interface states to charge and discharge, and the magnitude of displaced charge can be measured by the current flow, allowing trap density to be determined. The applied gate voltage is usually a square or tri-level waveform and the amplitude and frequency can be used to determine the energy level of the traps being probed.

2.6.2 Comparison

Engel-Herbert *et al.*[23] discuss some pitfalls in applying conventional characterisation techniques to III-V materials (specifically InGaAs). The study focuses predominantly on C-V techniques and the effect of the unusual conduction band structure in III-V materials. III-Vs have a lower density of states (DOS) in the conduction band and this allows the Fermi level to enter the conduction band - when it does, established approximations, such as the Boltzmann distribution for electrons and the Berglund integral for surface potential, begin to break down and a more detailed model must be used. Engel Herbert *et al.* outline a suite of density-of-state calculations to correct for the unconventional conduction band structure of III-Vs, including higher conduction band valleys and nonparabolicity. These corrections can be used to derive a more representative theoretical C-V response for use in the Terman method.

Engel-Herbert *et al.* also note that the low DOS in the conduction band also makes it difficult to reliably apply the Berglund integral, shown in equation 2.2:

$$\psi_s(V_G) = \int_{V_{G1}}^{V_{G2}} (1 - \frac{C_{lf}(V_G)}{C_{ox}}) dV_G + \Delta \tag{2.2}$$

Equation 2.2 is discussed in detail and derived in 4.3.1. V_G is the gate bias (i.e. the total voltage/potential applied to the MOSCAP), ψ_s is the surface potential (i.e. the potential difference in the semiconductor only), C_{ox} is the capacitance of the oxide (a fixed value, which is considered in series with the variable capacitance in the semiconductor) and C_{lf} is the measured capacitance at low frequency. Δ is the constant of integration and is equal to the surface potential at V_{G1}.

For the classical Berglund integral to be used, a stable reference point is required where surface potential does not vary strongly with gate bias (for Si, this is the band edge in strong inversion). Veksler *et al.*[95] present an alternative implementation of the Berglund integral for III-V materials, shown in equation 2.3:

$$\psi_s(V_G) = \int_{V_{FB}}^{V_G} (1 - \frac{C_{lf}(V_G)}{C_{ox}}) dV_G \tag{2.3}$$

Where V_{FB} is the flatband voltage. Although this method circumvents the need for a stable reference point, which is unavailable for III-V materials, it requires the independent extraction of V_{FB}. This can be achieved using a capacitance model, as would be used for the Terman method, but an alternative method is presented by Winter *et al.*[96]. The Winter method takes the point of inflection of the C-V curve as the flatband point, assigning the flatband voltage accordingly, using the second derivative to identify the point. This method is easily applicable but the second derivative introduces noise and exaggerates small deviations in C-V response, e.g. 'hump' features at the onset of inversion. Such exaggerated features can readily introduce additional points of inflection, making the Winter method difficult to implement in automated/batch data analysis.

When a comparison was done by Engel-Herbert *et al.* between the high-low method and the Terman method, a discrepancy in the calculated D_{it} was observed[23]. The suspected explanation for this was that the high- and low- frequency C-V responses were not of sufficiently high and low frequencies to exclude and include all trap response, respectively. Engel-Herbert *et al.* also comment on the unreliability of conductance techniques for measuring large values of D_{it} (specifically, cases where $C_{ox}<qD_{it}$) and for low-temperature measurements (as electrons become unable to escape the traps due to low energy). The conductance method can also only provide data close to the majority carrier band edge, limiting characterisation of mid-bandgap D_{it}. The advantages and disadvantages of the three methods are summarised in table 2.3. Ideally, all three methods would be used in parallel and discrepancies between the three outputs could be used to characterise traps in more detail.

Table 2.3: Advantages and disadvantages of different D_{it} extraction techniques

Method	Advantages	Disadvantages
High-low	• Easy to implement	• Liable to underestimate if probe frequencies not sufficiently low/high • Energy mapping using Berglund integral requires special methods for III-Vs
Terman	• Integrated energy mapping and modelling • Errors equally likely to under- and over-estimate	• Requires an accurate C-V model • Sensitive to C_{ox} and N_{dop} input parameters • Requires high frequency measurement free from minority carrier response and AC trap effects
Conductance	• Easy to extract D_{it} • Accurate for low D_{it} • Widely-used and widely-documented	• Liable to underestimate high D_{it} values • Probe range limited to near band edge • Unusual data (trap capture cross-section) required for accurate energy mapping

Martens *et al.*[97] also discuss the pitfalls of conventional characterisation techniques, predominantly in the context of germanium but with a secondary focus on GaAs and III-Vs. In addition to the challenges of extracting the energy-voltage relationship and the sensitivity of the conduction method to high D_{it} values, Martens *et al.* also discuss the issues with interpreting data from weak and strong inversion responses and with longer trap time constants interfering with measurements near the band edges. The paper proposes a 'full conductance' method to eliminate variability associated with inversion.

2.7 Aluminium Indium Antimonide

This review has focused generally on techniques used for III-V semiconductor MOS interfaces, rather than for InSb specifically, largely due to the dearth of published research on InSb. This is exaggerated for AlInSb - despite being used for tuning LED emission wavelength and encapsulating quantum well structures, which would necessitate oxide deposition/passivation to an AlInSb surface rather than an InSb one, research has rarely progressed to such practical structures and dielectric studies are almost non-existent. The most relevant source available is Datta *et al.*[98], where C-V responses from Al/Al_2O_3/AlInSb/InSb structures (Al composition not given but likely to be between 5% and 20% Al) were shown as part of a wider study into InSb-based quantum well FETs (QWFETs). The best C-V response is reproduced in figure 2.8 and a number of striking features are visible. The most noticeable is frequency-dependent response in inversion, suggesting that minority carrier generation-recombination - by thermal and/or trap-assisted mechanisms - has been reduced, possibly as a consequence of the increased bandgap of AlInSb, inhibiting thermal processes. The other most striking feature is the hysteresis response visible in the inset: a maximum hysteresis voltage of 86 mV for a voltage sweep from -1 V to +1 V or 43 mV/V, much lower than the value of 0.14 V/V displayed in InSb by Kadoda *et al.*[59]. This may be due to decreased atomic interdiffusion, as AlSb has a higher melting point and the increased bond energy from a high Al composition may inhibit diffusion of substrate elements into the oxide. It may also be influenced by the lower range of the voltage sweep: the -1 V to +1 V range may not fill/empty the same slow states as Kadoda *et al.*'s -8 V to +5 V sweep.

Uddin *et al.*[99] compared an Al_2O_3/InSb interface with an Al_2O_3/$Al_{0.1}In_{0.9}Sb$ one for gated quantum well Hall bar structures - although the gated Hall characterisation techniques are not comparable to or as reliable as C-V characterisation,

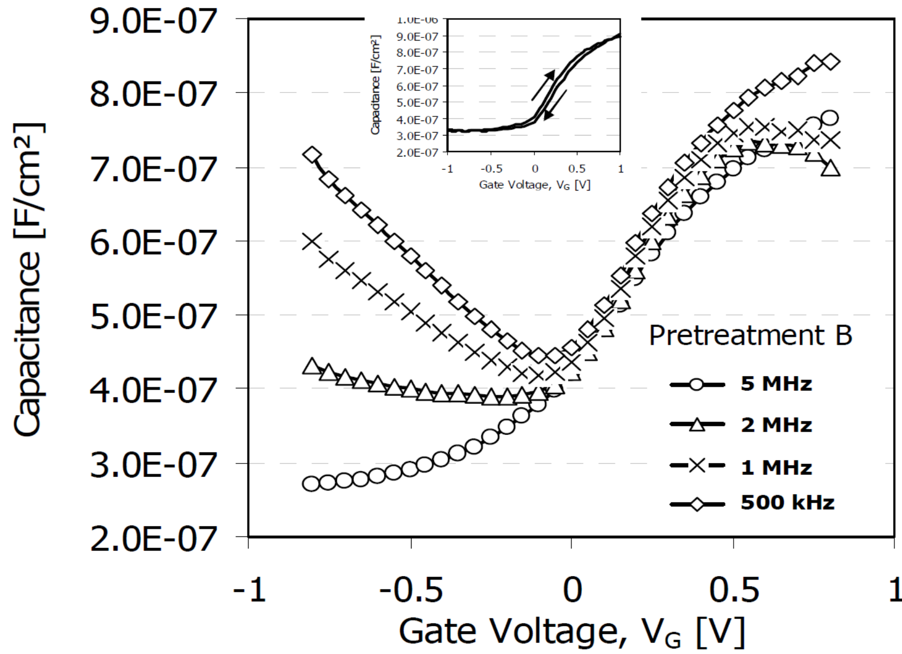

Figure 2.8: Room temperature C-V characteristics of Al/Al_2O_3/AlInSb/InSb MOSCAP. Reproduced from Datta *et al.*[98]

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they still provide information on the material interface. Uddin *et al.* found the Al_2O_3/$Al_{0.1}In_{0.9}Sb$ interface to be superior to the Al_2O_3/InSb one, showing greater charge modulation for a lower potential, lower D_{it} extracted from capacitance modelling and lower hysteresis. In this respect, Uddin *et al.* corroborates the good hysteresis results from Datta *et al.*, and it must be noted that Uddin *et al.* performed the ALD process at the low substrate temperature of 130°C (to allow a lift-off process), which would have inhibited atomic interdiffusion. The D_{it} extraction from Uddin *et al.* must be reviewed carefully: only one D_{it} data point could be extracted from the Al_2O_3/InSb sample (due to parallel conduction around the quantum well invalidating the model) and the weak modulation places this data point much closer to the valence band edge than the data from the Al_2O_3/$Al_{0.1}In_{0.9}Sb$ sample. The D_{it} data shows an order of magnitude difference between the two samples, with the Al_2O_3/$Al_{0.1}In_{0.9}Sb$ sample reporting a minimum D_{it} of 1×10^{12} cm^{-2}eV^{-1} around both midgap and the conduction band edge, compared to 1.6×10^{13} cm^{-2}eV^{-1} near the valence band edge in the Al_2O_3/InSb sample.

The only other source on AlInSb found in this review was a similar quantum well Hall bar study by Yi *et al.*[100]. They fabricated gated Hall bar structures, this time using HfO_2 as a gate dielectric, using a PEALD process at 175°C. Similarly to Uddin *et al.*, little interface characterisation was performed, with only a D_{it} of 8.4×10^{11} cm^{-2}eV^{-1} quoted - a figure extracted from the slope of carrier concentra-

tion with respect to gate voltage. These results on AlInSb are promising but there remains a substantial knowledge gap in AlInSb dielectric interfaces and more work must be done.

2.8 Conclusion

Limited work has been reported on InSb and InSb-based materials but a greater body of work on other III-V materials - $In_{0.53}Ga_{0.47}As$, GaSb, GaN etc. - can guide process development for InSb. The preferred deposition technique is atomic layer deposition, due to its fine control, conformal coverage and low process temperature, although photo-initiated chemical deposition processes may provide significant opportunities. The well-researched materials of SiO_2 and Ga_2O_3/Gd_2O_3 - favoured for Si and GaAs substrates - have been eschewed for In and Sb-containing III-V materials in favour of high-κ dielectrics and integrating in-situ processes based on other elements. Al_2O_3, La_2O_3 and AlN offer high-quality interfaces, at the expense of poorer bulk oxide properties, whereas HfO_2 presents promising bulk oxide properties but poorer interfaces, and it may be possible to combine materials. Impurities and defects in the oxide act as 'slow traps', introducing hysteresis and frequency dispersion, and must be minimised alongside interface traps.

Additional treatments before and/or after oxide deposition can improve dielectrics and interfaces. Wet chemical pretreatments must be supplemented with in-situ pretreatments, based on reactive gases or plasmas, for high-quality interfaces and the role of UV radiation may be important. Post-deposition processes must be designed, optimised and studied carefully, as there are many parameters to adjust and many competing mechanisms, such as chemical reactions, relaxation and solid-state diffusion. Multiple electrical characterisation techniques are available and they must be modified for III-V materials if they are to be reliable. Aluminium indium antimonide, despite being an essential material in practical InSb-based devices, remains practically unstudied in interface literature but may offer benefits over InSb interfaces.

Chapter 3

Experimental Techniques

3.1 Introduction

The fabrication and characterisation of metal-oxide-semiconductor capacitor (MOSCAP) test structures requires a series of stages. An extensive résumé of techniques is given in this chapter, each with a degree of detail commensurate with its use in this thesis.

The majority of material used in this thesis is bulk indium antimonide (InSb) from Czochralski-grown wafers, although epitaxial layers grown by molecular beam epitaxy (MBE) are used in chapter 8. Dielectric deposition was performed using atomic layer deposition (ALD) and metal deposition using electron-beam evaporation. The preferred wet chemical cleaning recipe used hydrochloric acid (HCl), annealing was performed using a tube furnace and photolithography was used throughout.

Electrical characterisation was performed using capacitance-voltage (C-V) and occasionally current-voltage (I-V) methods. The material properties of InSb required the characterisation to be performed at a temperature of 80 K, so a cryostat was used. Additional characterisation was performed using X-ray photoelectron spectrometry (XPS) to study surface chemistry, transmission electron microscopy (TEM) to study thin interfacial layers and atomic force microscopy (AFM) to study surface defects.

3.2 Process Technology Outline

A range of techniques are required to effectively fabricate MOSCAP structures and, once fabricated, a range of characterisation and techniques are also required. Initially, the substrate material must be formed by a bulk growth technique and the growth of epitaxial layers - layers grown as an extension of the monocrystalline

substrate - may also be required. For epitaxial growth, interfacial layers may be required to improve material quality and the setup of the growth tool is essential but material growth is not the focus of this thesis and growth techniques are discussed for background information only. Once the substrate is prepared, it must be cleaned before deposition. This typically requires wet chemicals - such as hydrochloric acid, ammonium hydroxide and hydrofluoric acid - but may also require additional treatment. Cleaning and pre-deposition treatment are essential for effective dielectric processes and are investigated in depth in chapter 6.

The clean surface is then ready for the deposition of the dielectric, which typically requires a chemical deposition process such as atomic layer deposition (ALD). The details of the deposition process are essential and ALD is investigated in detail in chapters 6 and 9 of this thesis. The subsequent gate and contact metal requires a different process: a physical deposition process such as evaporation or sputtering. To form the required regions, photolithography is required to selectively mask the sample surface, allowing chemical etching or a lift-off process. Metal deposition and photolithography are discussed here for background information, with fabrication process details included in appendix A. Annealing processes may also be used to improve dielectric quality and/or reduce interface trap states and an investigation into these processes is detailed in chapter 7.

Once the fabrication is complete, characterisation is required. Electrical measurements on narrow bandgap semiconductors require low sample temperatures, which can only be accomplished using cryogens and specialised equipment. The physical and electrical setup of the probe equipment is also critical, as samples can be easily damaged by probe needles and bonding. An alternative characterisation technique is X-ray photoelectron spectroscopy (XPS), where samples are transferred to a vacuum chamber and probed by an x-ray beam to analyse composition and chemical bonding states, and XPS is used in chapter 6. Finally, electron microscopy can be used to investigate micro- and nano-scale features, down to individual atoms, and is used in chapter 7 to image interfacial layers.

It must be noted that the use of InSb imposes strict restrictions on the thermal budget of fabrication (the material's cumulative tolerance to high-temperature processing). The melting point of InSb is very low compared to other semiconductors, 527°C, but InSb also undergoes an non-congruent transition between 300°C and 400°C. The antimony in the lattice begins to desorb from the surface/interface, impacting on the bulk semiconductor, bulk oxide and interface between the two. This degradation process can be prevented by limiting the process temperatures (generally to 300°C or less) and the time at these elevated temperatures.

3.3 Material Growth

Bulk material is usually prepared by the Czochralski method. Epitaxial material is usually prepared by molecular beam epitaxy.

3.3.1 Czochralski Growth

The Czochralski method is used to prepare macroscopic single crystals. The material is first extracted as elemental chunks (or rods, shot, powder etc.) of high purity and melted together to form polycrystalline feedstock. This polycrystalline ingot is commonly refined to even higher purity using the zone refining technique: a region at one end of the sample is heated above its melting point and heating/cooling gradients across the ingot's length slowly move the melted region through the ingot to the other end. Impurities preferentially dissolve in the melted region and, as it is moved through the ingot, the impurities are 'collected', leaving behind ultra-high purity feedstock.

The polycrystalline feedstock is transferred to a crucible and melted under inert atmosphere. A small monocrystalline seed crystal is inserted into the melt and is slowly rotated and withdrawn, as illustrated in figure 3.1. The melted feedstock solidifies on the surface of the seed crystal in an ordered manner, extending the monocrstalline structure. The process continues until a large monocrystalline ingot is formed. The ingot is then sawn into a large number of semiconductor wafers, which are polished to produce a clean and smooth surface. Wafers from each end ('seed' end and 'tail' end) are characterised to provide data on the ingot and the wafers are ready to use.

The InSb wafers used for this project were purchased from Wafer Technology Ltd. and grown using the liquid encapsulated Czochralski method and GaAs wafers were purchased from AXT Inc. and grown using the vertical gradient freeze method.

3.3.2 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is used to grow additional material as an extension to an existing crystal structure. The process is typically used to produce layer structures in semiconductors, as composition and dopants can be controlled.

Elemental feedstock is used, similarly to the Czochralski method, but the elemental material is loaded into effusion cells. The cells are attached to a vacuum chamber and raised to high temperature. The vacuum in maintained at extremely low pressure ($\sim 10^{-12}$mbar) to prevent impurities from incorporating into the grown material. When a cell is opened to the vacuum chamber, its contents will effuse into

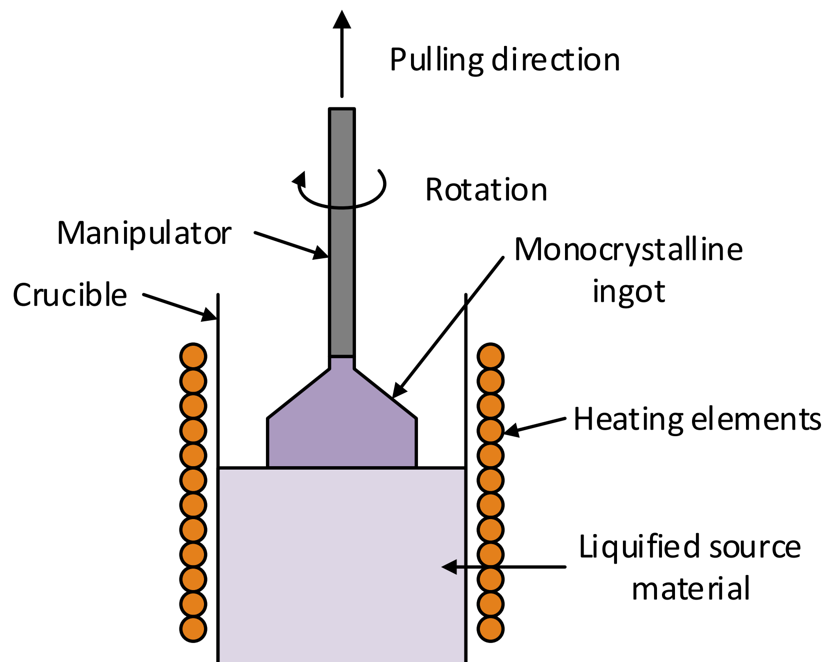


Figure 3.1: Diagram of Czochralski growth system

the chamber and form a flux. The flux will deposit around the chamber, onto the walls and any samples in the chamber, forming epitaxial material. This process is illustrated in figure 3.2.

MBE offers very fine control of layer structures. The low growth rate, typically $1\,\mu m\ hr^{-1}$, allows control down to a few atomic layers and shutters can be used to open and close effusion cells. The technique is also very sensitive, with sample temperature, cell temperature and the ratio of group V material to group III material (V:III ratio) affecting the quality of the material grown. Given the non-congruent effects in InSb discussed above, InSb and AlInSb are usually grown with a high V:III ratio, with the excess antimony preventing desorption from the surface.

The MBE system used for this project was a Veeco GEN II equipped with indium, gallium, aluminium and bismuth effusion cells, antimony and arsenic cracker cells and beryllium and gallium tellurium (tellurium) dopant cells.

3.3.3 Alternative Techniques

The Bridgman-Stockbarger technique is also used for the growth of bulk monocrystalline material. Whereas the Czochralski technique pulls a monocrystalline ingot from the melt solution, the Bridgman-Stockbarger technique forms the crystal by solidifying it inside the crucible. The crucible is prepared with a liquid solution of the desired material held above its melting point by a heating system. The heating

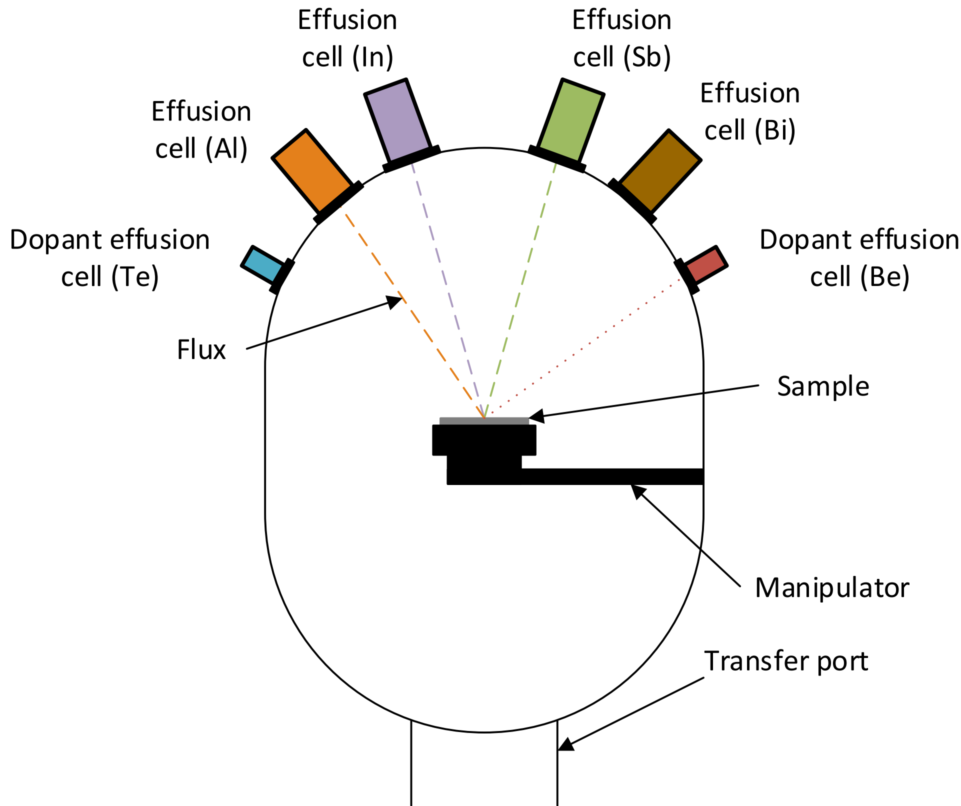


Figure 3.2: Diagram of MBE system

system has a gradient, with the highest temperature in the centre and the lowest at the ends of the crucible, allowing a seed crystal to be placed at one end. The crucible is slowly withdrawn from the heat, allowing the ingot to form at the solid-liquid interface slowly as a single crystal. For some materials, the Bridgman-Stockbarger technique offers lower defect densities but the Czochralski process offers a higher growth rate and is preferred for InSb.

Chemical vapour deposition (CVD) of dielectrics is discussed in detail in section 3.4, but it can also be used for epitaxial growth. In such context, it is frequently referred to as metalorganic chemical vapour deposition (MOCVD) or metalorganic vapour phase epitaxy (MOVPE). Compared to MBE, MOCVD offers much faster growth but the requirement for reactive precursor gases limits the technique's flexibility and incurs extra running costs for more stringent safety systems.

Liquid phase epitaxy (LPE) has historically been employed for cost-effective layers with low defect density. The sample, as a solid, is immersed in a solution containing a solvent and the desired epitaxy materials. The solute precipitates and deposits on the sample surface to form the desired layer. This technique has fallen out of favour due to its lack of scalability, control and flexibility in layer compositions when compared to MBE and MOCVD.

3.3.4 Doping

Unlike group IV semiconductors, where doping can easily be accomplished by substituting the group IV atoms with boron, phosphorus, arsenic etc., III-V semiconductors must be doped with care. A dopant may displace a group III or group V element depending on growth conditions and dopants must be chosen carefully to give repeatable doping without straining the system. The most commonly used n-type dopant in indium antimonide (InSb) is tellurium (Te) but there are several elements frequently used for p-type doping. Bulk material growth typically uses germanium (Ge) as a p-type dopant, with the germanium displacing antimony to give an acceptor site. In MBE growth, beryllium (Be) is more frequently used (displacing indium/aluminium).

When growing material, there will be a level of background doping introduced by any contamination in the system. For InSb, background doping typically makes the material n-type: undoped bulk wafers are usually specified with a background doping between 1×10^{13} cm^{-3} and 1×10^{15} cm^{-3} and undoped MBE-grown material usually has higher doping, in the range of 1×10^{16} cm^{-3}.

As an additional note, deviations from the ideal zincblende crystal structure can also cause doping effects. As an example, if a group V site is vacant or occupied by an atom of lower valence (e.g. a group III atom), the site becomes electron deficient and can act as an acceptor

3.4 Chemical Vapour Deposition (Dielectrics)

A variety of techniques are used to deposit thin film materials but they can be broadly split into chemical and physical deposition techniques. Chemical deposition techniques are capable of depositing metals but are more frequently used for dielectrics and are used throughout this thesis for such a purpose. Metals are not usually deposited by chemical deposition techniques because metal films from CVD have poor reliability and reproducibility. Chemical vapour deposition (CVD) techniques rely on the chemical reaction of gaseous, highly reactive precursor sources to form the desired layer.

3.4.1 Conventional Chemical Vapour Deposition

In a conventional CVD process, the sample is placed in a sealed chamber, typically in low vacuum at relatively high pressure (>1 mbar), with an inert carrier gas flow (typically argon). The deposition process is initiated by introducing two precursor

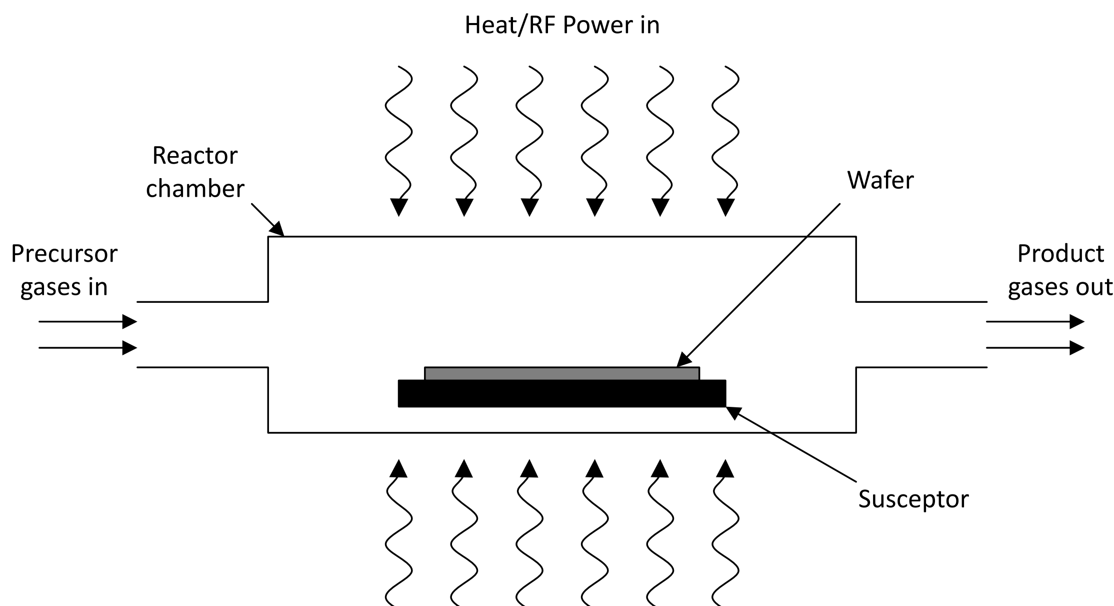


Figure 3.3: A generic CVD system. The sample rests on a holder/susceptor and carrier/precursor gases flown across it. Energy from heating the substrate or RF plasma power drives the chemical reaction

gases, which react to form a layer of the desired material on the sample. The process is illustrated in figure 3.3. The process is sometimes performed at low pressure (LPCVD) (<0.1 mbar) to reduce contamination in the deposited layer.

Despite the volatility and reactivity of the precursor gases, CVD requires additional energy to initiate the desired reaction. In thermal CVD, this energy is supplied by raising the chamber to high temperature (>300°C) - this is a standard, well-established technique but the low incongruent temperature of InSb prohibits the use of most thermal CVD reactions using conventional precursors. An alternative technique, plasma-enhanced CVD (PECVD), uses an electrical induction system to supply one or more precursors in the plasma phase, with the plasma induction power providing the energy required for the CVD reaction. PECVD enables deposition at lower temperatures but also gives higher growth rates than thermal CVD. Finally, photo-induced CVD (PICVD) uses UV light to stimulate the reaction but is not as widely used as thermal CVD or PECVD.

Conventional CVD was not used for this project and is discussed for background understanding only.

3.4.2 Atomic Layer Deposition

Conventional CVD provides high-quality films with good conformal coverage and high growth rate. However, it is difficult to form very thin layers with conventional

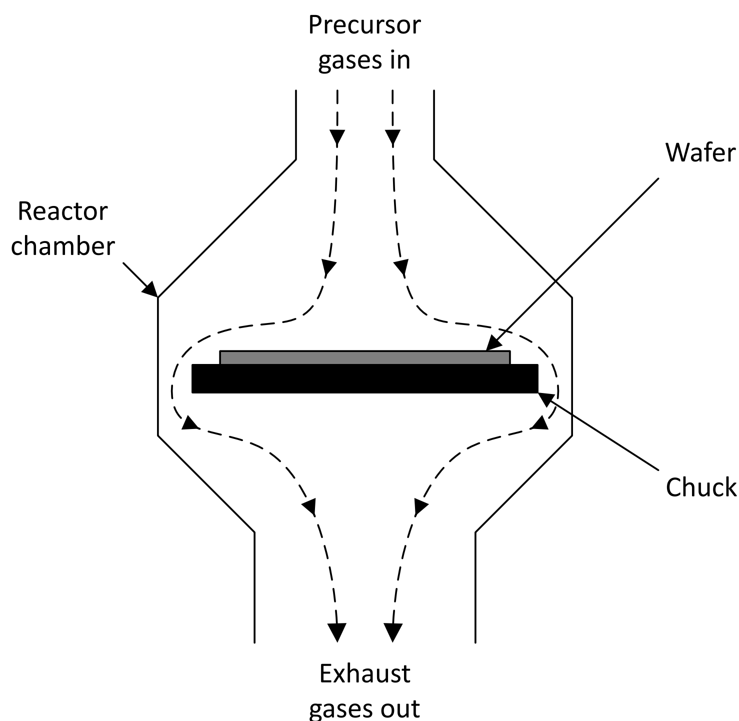


Figure 3.4: A generic ALD system. The sample rests on a holder/chuck and carrier/precursor gas flows across the sample surface

CVD, which has prompted the development of a new technique. Atomic layer deposition (ALD) utilises the same fundamental reactions and processes of conventional CVD but provides a much greater level of control over deposition rate and surface chemistry.

The sample is placed in a sealed medium-pressure ($\sim 10^{-3}$ mbar) vacuum chamber with inert gas flow, similar to conventional CVD. The reactor topology is similar but ALD typically uses a showerhead-like inlet and vertical flow of precursors, as illustrated in figure 3.4. Unlike conventional CVD, one precursor is then delivered into the chamber in a short pulse. The precursor adsorbs onto the sample surface and molecules of the precursor remain on the surface after the pulse is complete. The second precursor is then pulsed into the chamber, reacting with the adsorbed layer and, ideally, forming a single atomic layer (monolayer) of the desired material. The process is then repeated until the desired thickness is achieved and is illustrated in figure 3.5.

The ALD process is influenced greatly by the adsorption and reaction of precursors. The substrate temperature greatly influences these processes in turn, as illustrated in figure 3.6a, where an optimal 'window' of temperature exists. At low temperatures, the ALD process breaks down due to either insufficient energy to drive the ALD reaction or due to one or more precursors condensing on the surfaces in

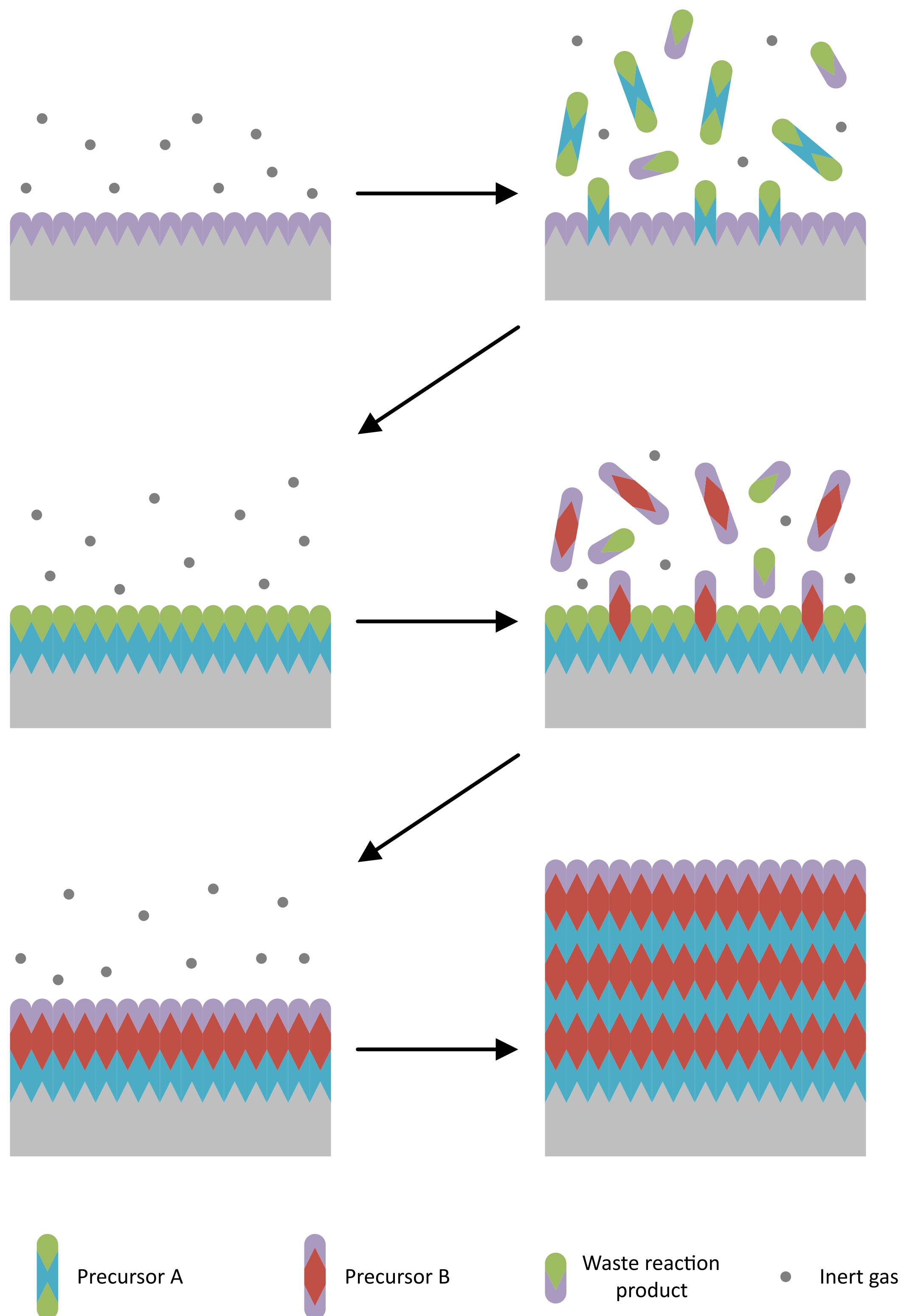
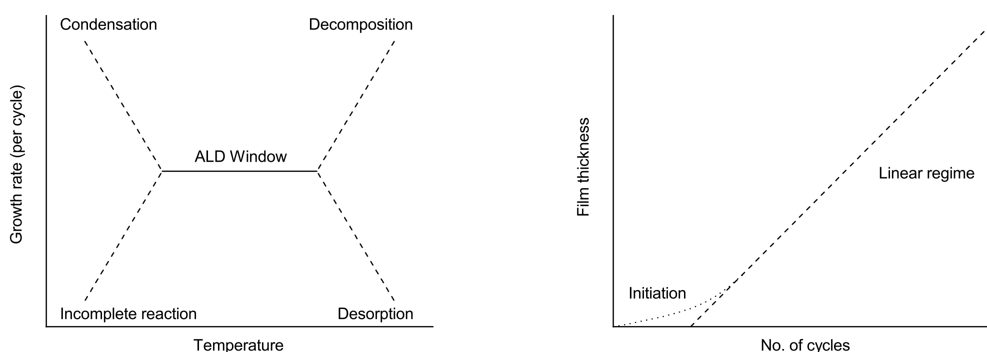


Figure 3.5: The ALD process shown diagrammatically. Precursors adsorb and react in a layer-by-layer manner to build up films in steps of individual atomic layers



(a) Deposition rate vs. temperature

(b) Thickness vs. number of cycles

Figure 3.6: Graphs illustrating mechanisms within ALD. (a) Temperature dependency of deposition rate, showing process breakdown at extreme temperatures and a stable 'ALD window' at intermediate temperature (b) ALD film thickness dependency on number of cycles, showing initiation and linear growth regimes

layers thicker than the desired monolayer. At high temperatures, the process breaks down either due to precursors decomposing on the surface in layers thicker than a monolayer or due to them desorbing from the surface before reacting. Between these conditions, deposition proceeds in a stable and controllable manner, typically in the temperature range of 200-400°C.

Additionally, the initiation of ALD growth can result in deviations from ideal layer-by-layer behaviour. Figure 3.6b illustrates how material deposition progresses as process cycles are performed and highlights the presence of an initiation period. The first few cycles typically result in a much lower deposition rate, due to, for example, reactions between precursor gases and surface contamination, or incomplete nucleation onto a surface that has not been ideally functionalised (i.e. where not all surface bonding states are ideal for precursors to adsorb to). Following the initiation period, ALD proceeds with a linear deposition rate.

For this project, ALD was performed using an Oxford Instruments OpAL at the University of Liverpool and an Ultratech Fiji at the University of Warwick.

3.4.3 Choice of Precursors

The choice of precursors can affect CVD processes, particularly ALD, significantly. Precursors must be volatile and reactive but not damaging to the substrate. Safety is also a concern, as many precursors are highly flammable and/or pyrophoric and some are highly toxic. Gas and plasma sources can be used, with plasma sources

offering a higher growth rate (in conventional CVD and potentially in ALD), lower deposition temperature and a deposited layer with lower porosity (higher density) at the expense of potential damage to the substrate by energetic ion species.

The aluminium precursor considered in this thesis is trimethylaluminium (TMA). TMA is extremely flammable, even when compared to other precursors, but is gaseous at room temperature and its high reactivity provides opportunities for surface cleaning. The hafnium precursor considered in this thesis is tetrakis(dimethylamino)hafnium (TDMAH). TDMAH is less volatile than TMA and requires heating to its container and the gas pipes to deliver it in gaseous form to the chamber. TDMAH is also less reactive than TMA, so requires higher deposition energy (i.e. higher temperature/use of plasma) and gives lower growth rates.

The most frequently used oxygen precursor is water. Water has a low boiling point and moderate reactivity and is favoured for being gentle when compared to oxygen plasma and ozone. Both oxygen plasma and ozone offer higher growth rates but their higher reactivity can potentially damage the substrate. Similarly, nitride materials can be deposited using either ammonia (NH_3) as an analogue to water or nitrogen plasma as an analogue to oxygen plasma. The deposition of nitrides is difficult, as trace amounts of oxygen can easily displace nitrogen and form oxynitride materials instead of nitrides.

3.5 Physical Vapour Deposition (Metals)

Physical vapour deposition techniques are the complement to chemical vapour deposition techniques. Physical deposition techniques are capable of depositing dielectrics but are more frequently used for metals and are used throughout this thesis for such a purpose. Dielectrics are not usually deposited by physical deposition techniques because the stress and stoichiometry of the deposited layers are generally poor. Physical vapour deposition (PVD) techniques rely on an energetic physical process displacing material from a crucible or target to the sample surface under vacuum to form the desired layer.

3.5.1 Evaporation

In evaporation, the source material is evaporated from a crucible and deposits on the sample. There are multiple techniques for evaporating the source material, most prominently thermal evaporation and electron beam (e-beam) evaporation.

In thermal evaporation, the source material is evaporated from the crucible by simply heating it to sufficient temperature, noting that it will evaporate more easily

in the low pressure vacuum environment. Conversely, e-beam evaporation utilises an electron beam to locally heat a small area of source material to evaporation temperature, while the surrounding material remains cooler. Since only a small volume of the source material is melted in e-beam evaporation, contaminants are less likely to be incorporated into the vapour (and deposited film) but the more energetic e-beam process emits high energy radiation, which may damage the substrate.

The evaporation system used for this project was a Scientific Vacuum Services (SVS) e-beam evaporator.

3.5.2 Sputtering

In sputtering, a target of the source material is bombarded by plasma ions (usually argon). The bombardment sputters off the surface of the target, which diffuses through the chamber and deposits on the sample. When compared to evaporation, sputtering has a lower deposition rate, potentially causes damage from high energy plasma ions and can incorporate impurities more easily but it offers less directional deposition and greater control. Advanced sputtering recipes can use different plasma species (such as nitrogen or oxygen) to form compounds, e.g. compounding a titanium target with nitrogen to form titanium nitride (TiN) and depositing the TiN on the sample.

This project requires only simple metal structures and, as such, e-beam evaporation is used throughout.

3.5.3 Choice of Metal

A wide range of metals are used in semiconductor fabrication for a wide range of roles. The choice of metal is based on a wide range of criteria, most prominently: availability, melting/boiling point, chemical and physical stability, electrical conductivity and work function. As an obvious set of criteria, the metal must be available, it must not have too high a cost relative to its role in the project and it must be suitable for deposition in the tools available. Metals with a high melting point, such as tungsten and molybdenum, are ill-suited to evaporation but their high melting point may be desired for certain applications. Sufficient chemical stability is essential, as the metal will be in contact with both the substrate and oxygen in the atmosphere and some metals, such as titanium, will readily oxidise during and after deposition if the conditions allow. Physical stability can be considered an extension, as some metals (most prominently gold) diffuse easily and may have undesired effects on the sample. Electrical conductivity may be essential, for example, in interconnects or

contact pads. Finally, the work function of a metal can play a significant role, either as the gate contact on a MOS structure to manipulate the surface potential or as a metal-semiconductor contact (high work functions tend to form Schottky contacts, whereas low work functions tend to form ohmic contacts).

In this thesis, aluminium is used as a gate metal due to its ease of evaporation and gold is used for ohmic contacts due to its high conductivity and chemical stability, with a thin layer of titanium to aid adhesion. Alternative gate metals include titanium (readily available in most systems) and platinum (for its chemical stability and high work function).

3.6 Photolithography and Patterning

Photolithography is a universal technique for defining patterns in semiconductor fabrication. Photosensitive polymer (photoresit or simply 'resist') is deposited and is exposed and developed similarly to photography film, forming a pattern in the polymer. This pattern is used to define features, utilising the photoresist's different properties to the feature material. Photolithography is performed under controlled lighting, in a 'yellow room'. It should be noted that, when discussing process recipes, photolithography stages are usually omitted but are assumed by implication when patterned features are discussed.

3.6.1 Spin Deposition

In semiconductor processing, polymers (such as photoresist) are deposited in the liquid phase and cured. Once the sample has been cleaned (typically using solvents: acetone and isopropanol), it is placed in a spinner and secured on the chuck using vacuum pressure on the back side. The polymer is deposited either by pipette or by pouring, the spinner is closed and the sample and chuck are physically spun to spread the polymer and to control thickness. Once the spinner programme is complete, the sample is placed on a hotplate to cure the polymer, often with a baking tray to limit the temperature ramp rate. This process can be used for polymer dielectrics, such as polyimide, in addition to photoresists.

The spinner used for this project was a Spin 150 manual system.

3.6.2 Photolithography Process

Once the photoresist layer is deposited, it must be exposed and developed. Several exposure tools and techniques exist, such as contact masks, steppers and scanning

beams, but contact mask alignment is used in this thesis. The sample is set on a chuck, with a photomask secured above it, and raised nearly into contact with the mask, with only a few µm separation. The photomask contains an image of the desired pattern, usually in chromium on a quartz plate, and casts a shadow over the substrate. The mask aligner features microscopes and fine alignment tools so the user can align the mask with existing patterns on the sample.

Once the alignment is complete, the microscope is removed, the sample is brought into contact with the mask and a ultraviolet (UV) light source is used to expose the sample surface to a dose of UV light through the mask. The exposed regions of photoresist undergo a change: positive photoresists become soluble in developer solution, whereas negative photoresists become insoluble. The sample is removed and placed in developer solution, which selectively removes the photoresist to form the desired patterns. Developer solutions are typically dilute alkaline solutions, such as tetramethylammonium hydroxide. Alkali metals (Li, Na, K) are avoided, as they cause major impairments in devices and dielectrics.

The mask aligner used for this project was a Suss Microtech MA/BA8 system. Photomasks were fabricated by Compugraphics.

3.6.3 Lift-off Patterning

Once a photoresist pattern has been deposited and developed, the pattern is usually transferred to another material by etching or lift-off. In a lift-off process, the photoresist is deposited, developed and another material is deposited on top. The second material deposits partially on the photoresist and partially on the substrate. The photoresist is then dissolved (usually in acetone or a more aggressive solvent) and the material on top of it floats off in the solvent, leaving only the material originally in contact with the substrate.

In large-scale production, lift-off is avoided, as it is less reliable and repeatable than well-established and characterised etch processes. In a research setting, however, unusual deposition materials, which do not have pre-established etch processes, are frequently used, and lift-off offers a universal patterning technique that is less reliant on chemistry.

Lift-off processes require thick photoresist layers to ensure that the material deposited on it floats off when the photoresist is dissolved rather than contacting the substrate. If the material contacts the substrate and is allowed to dry then Van der Waals forces will form a strong bond between them and the material cannot be removed - thick photoresist helps to prevent this scenario. Frequently, a bi-layer photoresist process is used: the top layer forms an overhang relative to the bottom

layer at the boundary of the photoresist. This structure shadows a small region from the deposition, preventing sidewings. A sidewing is formed when material deposits on the side of the photoresist - these sidewings usually remain in place when the photoresist is dissolved and can impact on device operation.

3.7 Wet Chemical Etching and Cleaning

Once a pattern has been developed in photoresist, it can be transferred to another material using lift-off or etching. Etch processes use chemical or physical action to selectively remove regions of the substrate that are not masked by photoresist. Etch processes can be wet etches, using aqueous solution, or dry etches, using plasma. Wet etch processes use chemical action exclusively, acting on the surface and preventing damage to the underlying substrate. Dry etching is not used in this project.

3.7.1 Acid Processes

Most acid processes are based on hydrochloric acid, nitric acid or sulphuric acid, diluted in a solvent (usually deionised water). The acid undergoes a reaction with the substrate surface, resulting in products which are soluble in the solvent. The products desorb, exposing the surface for further reaction and progressing the etch.

Semiconductor processing often uses hydrofluoric acid, enabling etching of otherwise chemically stable materials with its aggressive chemistry. Oxide compounds are rarely etchable in conventional etchants but fluorine can displace oxygen, forming soluble fluoride compounds.

Conventional acid processes are not used for etching in this project but dilute hydrofluoric acid is used to etch aluminium oxide.

3.7.2 Alkali Processes

Alkali processes are not often used in semiconductor fabrication, as alkali metal ions have significant deleterious effects in semiconductor devices. Ammonium hydroxide is a notable exception, forming the basis of some cleaning and etching processes, most notably the well-known ‘RCA SC-1’ process.

Within this project, an alkaline tetramethylammonium hydroxide process is used to etch aluminium without damaging the underlying InSb. The photoresist developer solution ‘MF-319’ is a 1% solution of tetramethylammonium hydroxide in water and this solution is used straight from the bottle as an etchant. The process details are given in appendix A.

3.7.3 Wet Chemical Cleaning

Wet chemistry is frequently used to clean surfaces in preparation for further processing. The same fundamental chemistry as the etch processes is used: cleaning processes are either a short etch or a self-limiting wet chemical treatment. As an example, a HCl-based cleaning solution may form a passivating chloride layer which protects the surface from oxidation.

Wet chemical cleaning processes are a critical component of this project, and are discussed in more depth in chapter 6.

3.7.4 Isotropy

It should be noted that not all etch processes act in all directions equally. An etch is described as isotropic if it etches in all directions equally and anisotropic if it does not. Wet etches are mostly isotropic, but, as an example, potassium hydroxide-based etches will etch different crystallographic planes of silicon at different rates.

3.8 Annealing

In addition to etch and deposition techniques, annealing is used as a transformative technique. Raising the temperature of the sample allows atoms to move and re-organise, which can be beneficial or deleterious depending on the composition of the sample, temperature, ambient and duration. Annealing is most commonly used after ion implantation to activate dopants, after oxide deposition to re-organise the interface and after ohmic contact deposition to form interfacial layers to lower contact resistance. Ion implantation is not used in this project and ohmic contact resistance is sufficiently low without annealing - the only requirement for annealing in the project is as post-deposition annealing.

It is essential to remember that the properties of InSb prohibit high temperature annealing. Antimony begins desorbing from the sample at approximately 300°C, tightly restricting the thermal budget, and InSb melts at 527°C, restricting the maximum anneal temperature.

3.8.1 Annealing Modes

A range of furnace designs and anneal procedures are available. The semiconductor cleanroom facility at the University of Warwick is equipped with tube furnaces and rapid thermal anneal (RTA) furnaces.

Tube furnaces provide a closed environment for anneal processes. A quartz or alumina tube is connected to a gas supply at one end, with flow gauges to indicate gas flow rate, and vented to the cleanroom environment or an exhaust system at the other. The tube is heated by a resistive heating furnace equipped with temperature monitoring and a temperature controller. Tube furnaces are capable of only slow temperature changes, between 5 and 8 °C/min, and are suited for long anneal processes (>5 mins) only. The tube furnace used for the project was a Carbolite ????.

RTA furnaces are capable of much higher ramp rates than tube furnaces, typically still in closed atmosphere. The tight thermal budget for InSb, however, limits the maximum process temperature to a range where RTA processes offer little benefit over long tube furnace-based processes and development of RTA processes was deemed unnecessary for this project.

3.8.2 Annealing Chemistry

Annealing can be performed in inert, oxidising or reducing ambient. Inert ambient, such as N_2 or Ar, is normally used for implant activation annealing, where physical re-ordering is the desired goal. Oxidising ambient, such as O_2 or N_2O, is conventionally thought of as an ambient for thermal oxidation but can also be used for transformative processes, such as forming interfacial oxide layers. Reducing ambient, such as H_2 or forming gas (5% H_2, 95% N_2) is usually used for passivation, with hydrogen atoms breaking and occupying deleterious bonds and states.

3.9 Electrical Characterisation

Fabricated structures must be characterised and characterisation based on electrical measurements can be versatile and intensive. The foundation of electrical measurement is analysing how current or capacitance varies with different voltage biases - for this project, capacitance-based characterisation is preferred. Analysis techniques are discussed elsewhere in this thesis but this section discusses practical considerations: how the measurement apparatus is set up to minimise noise and error

Electrical characterisation was performed locally at the University of Warwick and using facilities at the University of Glasgow. Both characterisation setups were variable-temperature systems - the theory of cryogenic equipment is discussed in section 3.10.

3.9.1 Setup at University of Warwick

The electrical characterisation setup at the University of Warwick was used to take current-voltage (I-V) and capacitance-voltage (C-V) measurements. The I-V measurements were taken using a HP (subsequently rebranded Agilent and Keysight) 4145B parameter analyser and an Agilent 4155C parameter analyser and the C-V measurements were taken using an Agilent E4980A LCR meter. Both instruments were controlled by PC using National Instruments LabVIEW (laboratory virtual instrument electronic workbench). The C-V measurements were all performed with an AC voltage of 20 mV and in C_p-C_p mode. The test instruments were connected to a Leybold RDK 10-320 cryostat - a closed-cycle system cooled with compressed helium (see section 3.10).

The sample was mounted to a printed circuit board (PCB) using GE varnish. Aluminium wire bonds were used to connect the sample to 10 contact pads on the PCB. These pads were connected to a Harwin Datamate connector, chosen for its high reliability and tolerance of cryogenic conditions. The entire PCB assembly was free of tin to ensure stability below tin's phase transition temperature. The Harwin connector was crimped to 10 coaxial cables with a characteristic impedance of 50 Ω and capacitance of 102 pF/m to match the Keysight cable specification. These cables were connected to a hermetically sealed connector, purchased from Fischer Connectors, with 11 pins - the 11th pin was used to connect the shields of the internal and external coaxial cables through a common connection. The cable terminates at a 10-plug metal breakout box, with a total of 1 m of cable between the plugs of the breakout box and the Harwin connector. The connection configuration for the I-V measurements was a non-Kelvin connection using coaxial cables with coaxial-triaxial converters interfacing the coaxial cables with the triaxial plugs on the parameter analyser. The connection configuration for the C-V measurements was an extended 2-terminal configuration: 1 m of shielded 4-terminal cabling to the breakout box, Y-piece connectors to join the Hcur to Hpot and Lcur to Lpot, followed by 1 m of shielded 2-terminal cabling to the device under test (DUT).

3.9.2 Setup at University of Glasgow

The measurements taken at the University of Glasgow were C-V measurements only, taken using an Agilent (now Keysight) B1500 parameter analyser equipped with a capacitance measurement unit (CMU). The B1500 was connected to a LakeShore variable temperature probe station, cooled by a closed-cycle helium system. Due to vibration from the helium cooling, measurements were performed with the compres-

sor turned off, reducing the temperature control on measurements.

The connection configuration was similar to the cryostat: two T-piece connectors joined the 4 terminals as they were connected to the probe station. The sample was electrically isolated from the chuck using a piece of quartz and the probe needles were beryllium copper alloy.

3.9.3 Measurement Correction

Impedance measurements are sensitive to calibration errors and corrections should be made before every measurement. Open circuit and short circuit corrections were used only, as no load standard was available. Open circuit corrections were performed on the probe station by moving the probe needles a short distance from the sample and from each other. On the cryostat they were performed by leaving two bond pads unconnected. Short circuit corrections were performed on the probe station by touching the probe needles away from the sample. On the cryostat they were performed by bonding one pad directly to another (adjacent).

As measurement correction connections occupied lines on the cryostat that would otherwise be used for devices, a trial was performed to investigate whether performing the corrections, changing the sample and running with no further corrections would influence the measurement. This did not affect the capacitance data significantly but did influence a conductance artefact, believed to represent a leakage or miscalibration. As such, measurement corrections were performed after periods of equipment downtime and not for every sample run.

3.10 Cryogenic and Vacuum Techniques

The electrical measurement analysis techniques used for dielectric interfaces are based on the silicon-silicon dioxide system. These techniques, discussed in chapter 4, are broadly applicable to other materials but a critical difference of the InSb-dielectric system is the high generation-recombination (G-R) rate in the semiconductor. For InSb-based test structures to be compatible with the analysis techniques, the measurements must either be performed at very high frequency (>1 GHz) or at very low temperature (80 K) to manage the effect of G-R. Low temperature systems are used for this project and are discussed below, along with the vacuum systems required to minimise convection losses.

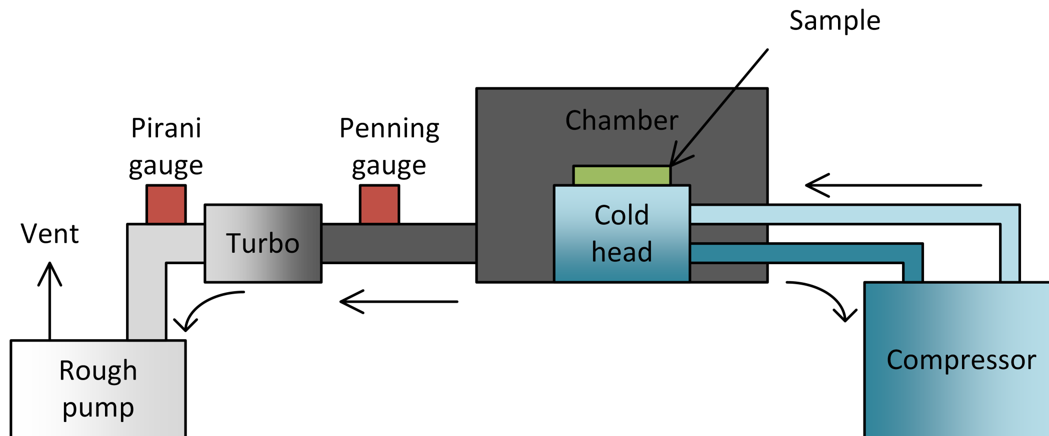


Figure 3.7: Components and setup of a typical cryogenic system

3.10.1 Cryogenic System Architecture

Figure 3.7 shows a typical cryogenic system diagrammatically. The sample is held in a vacuum chamber and cooled using a cold head assembly. The vacuum system is shown on the left and the cooling system on the right.

3.10.2 Heat Transfer

There are three heat transfer mechanisms relevant to cryogenic systems: conduction, convection and radiation.

Conduction is the mechanism central to cooling, i.e. the mechanism which connects the sample to the cryogen. In well-managed cryogenic systems heating through conduction can be neglected but if cold and ambient-temperature parts touch in a poorly-managed system, excessive heat leakage can occur.

Convection is a critical loss mechanism and must be minimised during operation. This can be easily accomplished by encasing the sample and evacuating the chamber. Once a fine vacuum has been established, convection losses will be minimised. Vacuum techniques are discussed in section 3.10.4.

Radiation has less of a heating effect than conduction and convection but it is still essential that it must be minimised in cryogenic systems. Even when cold and ambient bodies are separated by empty vacuum, infrared radiation can raise the cold body's temperature. Moreover, radiation can stimulate the sample (e.g. exciting electrons in InSb diodes) and so must be controlled and minimised. This is accomplished by a secondary enclosure in the vacuum chamber which is cooled independently of the sample. This radiation shield absorbs radiation from the outer walls but remains at a low enough temperature that the sample held within stays cool and unstimulated.

3.10.3 Cryogenic Cooling

Cooling requires a refrigerant and cryogenic cooling requires a cryogen. The cryogens in common use are liquid nitrogen and liquid helium and they can be delivered from a dewar (storage vessel) or compressor. Liquid nitrogen is cheap and almost disposable it can be vented from a dewar freely and large quantities are available for minimal cost. Liquid helium is expensive and must be recaptured but it has a much lower boiling point - the boiling point of nitrogen is 77.4 K and the boiling point of helium is 4.2 K. Moreover, if helium is separated by atomic mass and He^3 is isolated, advanced cryogenic systems such a dilution refrigerators can be used to achieve temperatures below 1 K.

The cheapest method to deliver cryogens is a sealed dewar. The cryogen is decanted into the dewar and stored in a sealed vessel under the pressure of the evaporating cryogen. This pressure, often combined with a vacuum pump on the exhaust, is used to deliver the cryogen to the cold head. Liquid helium has a low viscosity and is easily transferred, while liquid nitrogen requires wider transfer tubes and, occasionally, additional pressure to the dewar. When liquid helium is delivered this way, it is recaptured from the exhaust.

By contrast, closed-cycle systems are more expensive up-front and consume more power but they do so by recycling the cryogen. A compressor cools the cryogen by first compressing it (raising its temperature), then transferring the heat from the compression away to cooling water and allowing the cryogen to expand inside the cold head, lowering its temperature down to as low as the boiling point of the cryogen. This process can operate continuously with negligible leakage, although the expansion at the cold head occurs in a pulsed manner, causing vibration and potentially issues with sample damage and contact. The Leybold RDK 10-320 cryostat used for this project is a closed-cycle helium-cooled system with a base temperature of $\sim$20 K.

3.10.4 Vacuum Techniques for Cryogenic Systems

As mentioned previously, cryogenic systems require vacuum conditions. These are achieved through a combination of pumps and monitored with a combination of sensors.

Before discussing pumps and sensors, it is essential to discuss units. The SI unit of pressure is the Pascal (1 Pa = 1 Nm) but vacuum systems often use millibar (1000 mbar = 100 kPa $\approx$ 1 atmosphere) and, occasionally, Torr or mTorr (1 Torr = 1.33 mbar). The psi unit is rarely used to measure vacuum pressure but may be

used elsewhere in the system. The preferred unit in this thesis is mbar.

A rotary vane pump is usually used as a 'rough pump'. This handles the first stage of pumping, from atmospheric pressure (1 bar) to 10^{-3} mbar, but is not suitable for any finer vacuum. Notably, the rotary vane pump contains sealing and lubricating oil, which may flow from the pump into the vacuum system (a process known as 'backstreaming').

The rough pump is usually accompanied by a Pirani gauge. This type of gauge can be used to measure pressure at rough vacuum and is based on heat transfer and thermal conductivity. A heated filament is held in the vacuum, connected in a Wheatstone bridge and current passed through it to maintain a constant resistance. In a coarse, high pressure vacuum, the filament will lose heat rapidly and will require a large current (and associated heating effect) to maintain a constant resistance (noting that resistance increases with temperature). By contrast, in a finer, low pressure vacuum, the filament will lose heat slowly and will require only a small current to maintain a constant resistance. This allows the pressure to be measured and monitored.

To achieve a finer vacuum, a turbomolecular pump is required. More commonly referred to as a turbo pump (or turbopump or simply 'turbo'), the turbomolecular pump contains two arrays of vanes, one of which rotates at extremely high speeds. Any gas molecules which the vanes strike will be accelerated to the exhaust, allowing the vacuum to be refined. Once operating at full capacity, the vacuum can be refined to 10^{-6} mbar or finer.

Turbomolecular pumps are usually accompanied by a low pressure gauge. This is usually an ionisation gauge, which ionises a sample of the remaining gas with an electron plasma and measures the electrical current from the ionisation. The ionisation gauge used for this project is the Penning gauge a cold cathode gauge which uses strong electric and magnetic fields to trap electrons. This electron plasma then ionises the gas. An alternative technology is a hot cathode gauge, where the electron plasma is generated from thermionic emission.

The final pumping effect which must be discussed is cryopumping. When a cryogenically cooled object is in a chamber with any gas, the gas may condense onto the object. If the object is cooled with liquid nitrogen then water, oxygen, carbon dioxide and argon will condense on it and a liquid helium cooled object will also collect nitrogen and hydrogen. This trapping effect will reduce the pressure in the chamber, allowing the vacuum to be refined even further from the level achieved using the turbopump.

Vacuum technologies for ultra-high vacuum, such as ion pumping and titanium

sublimation pumping, are not used in this project.

3.11 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a measurement and characterisation technique which is used to study the chemical bonding state of atoms on or close to the surface of the sample. XPS is used in this project to investigate the semiconductor surface and semiconductor-dielectric interface, aiming to correlate electrical performance with chemical bonding features to provide a more complete, holistic understanding of fabrication processes.

3.11.1 XPS Fundamentals

The sample is stimulated with an X-ray source to excite electrons from the sample. The energy of the X-rays is higher than the binding energy of electrons in the sample and they are ejected from the sample as a result. The electrons are collected in a detector, producing a spectrum of detected intensity vs. kinetic energy of the electrons. The binding energy of the states the electrons were ejected from can be deduced using equation 3.1.

$$Binding\ energy = X-ray\ energy - (kinetic\ energy + work\ function) \tag{3.1}$$

The binding energy of electrons is characteristic of the element and orbital the electron was ejected from (e.g. the indium 3d orbital, the strongest photoemission from indium, has a binding energy of 444 eV) but an additional shift is applied based on the chemical bonding state of the electron. As a rule of thumb, electronegative elements induce chemical shift to higher binding energy and electropositive elements induce shift to lower binding energy.

A survey scan with a large energy range and low energy resolution can identify the elements in the sample volume. Subsequent 'core level' scans focus on specific photoemission features (e.g. aluminium 2p) with high energy resolution, allowing a series of components with different chemical shifts to be resolved (e.g. one Al 2p component of aluminium bonded to antimony, one component bonded to oxygen and another bonded to sulphur). Based on the elements observed in the survey spectra and existing information in the scientific literature detailing component shapes and energy levels, the chemical bonding states in the sample can be identified. These components can be analysed quantitatively once fitted.

The area surveyed by XPS is dependent on the spot size of the X-ray source but is approximately 1 mm in diameter. The probing depth is dependent on the stimulating X-ray energy and the density of the top layers of the sample, as emitted electrons must be able to escape the sample. An aluminium Kα source gives a probing depth of approximately 10 nm, with weaker photoelectron emission from deeper parts of the sample. Alternative sources, such as silver and copper sources, give higher X-ray energy (and associated probing depth) but lower intensity (necessitating longer acquisition time for spectra).

3.11.2 XPS Apparatus

The XPS instrument used for this project was a Kratos Axis Ultra DLD. It was equipped with a monochromated aluminium Kα X-ray source, a magnetic immersion lens, a delay line detector and both a spherical mirror analyser and a concentric hemispherical analyser. The system also includes a sputter gun for depth profiling and charge neutraliser for insulating samples, neither of which were used for this project. Acquired spectra were fitted and analysed using the CasaXPS software package

3.12 Transmission Electron Microscopy

Conventional optical microscopy magnifies transmitted/reflected light through/from a sample, allowing fine features to be imaged, but it is limited by the wavelength of visible light. This limit can be surpassed by substituting photons for electrons, as the de Broglie wavelength of an electron is less than 1 nm, even for acceleration voltages as low as 10 V. In a transmission electron microscope (TEM), an electron beam source can be combined with electrostatic lenses and an image detector (or fluorescent screen) to emulate an optical microscope and produce a high-resolution image, providing contrast based on the absorption/transmission of electrons. Transmission electron microscopy (TEM) is used in this thesis to investigate cross-sections of fabricated devices, allowing imaging at sub-nanometre resolution and identification of interfacial layers.

Sample preparation for TEM is critical, as electron transmission and subsequent imaging are only possible for extremely thin samples ($<1\,\mu$m). To prepare TEM specimens, the samples are first cleaved into small pieces ($\sim$1 mm thick) and mounted into a sample holder ring using wax. After further mounting the sample holder onto a resin block, the samples are then ground using silicon carbide paper. The remaining thickness after each grinding step is measured using an optical

microscope, based on the difference in focus between the top and bottom of the sample. Grinding is used to thin the sample to ∼10 µm, at which point further thinning is achieved using Ar ion milling. A precision ion polishing system (PIPS) rotates the sample continuously while Ar ion beams are focused on the front and rear sides of the sample, allowing it to be uniformly thinned to zero thickness. Once the PIPS process has formed visible holes in the sample, it is removed - the regions surrounding the holes are suitable for TEM.

The TEM used in this thesis was a Japanese Electron Optics Limited (JEOL) 2100+. The PIPS system was a Gatan unit. TEM sample preparation and imaging were performed by Dr. Richard Beanland.

3.13 Atomic Force Microscopy

Atomic force microscopy (AFM) is a technique for studying surface morphology. It is capable of lateral resolution of ∼1 µm and vertical resolution <1 nm, and is used in this project to study features from material growth and to search for surface features ('decorations') resulting from crystal defects and their propagation through the material as it grows.

AFM achieves fine actuation control using piezoelectric actuators. When voltage is applied to piezoelectric materials, they deform proportionally to the applied electric field and can be engineered to enable fine actuation down to displacements around 1 nm resolution. To achieve fine measurements of vertical height, a probe tip on a cantilever arm is used. The tip is micro-machined down to a tip radius of <1 µm and a laser aimed at the end of the cantilever, above the tip, and the reflected light collected using a 4-quadrant photodiode detector. As the cantilever deforms, due to the morphology of the surface, the laser is deflected and the relative signal detected in the four quadrants of the photodiode detector can be used to identify the direction and magnitude of the deflection. When combined with the lateral control for scanning and the vertical control for feedback control/measurement of vertical height, 2-dimensional images of surface morphology can be acquired down to atomic step resolution.

The AFM used in this project was a Park XE-100 AFM. The tips were Pt coated NSC-14 tips from MikroMasch and measurements were made in contact mode. AFM imaging and operation, including post-processing of images, was performed by Mr. Alan Brunier.

3.14 Conclusion

A range of techniques for material preparation, fabrication and characterisation have been discussed. The standard MOSCAP (metal-oxide-semiconductor capacitor) fabrication and characterisation procedure is included in appendix A and relies on wet cleaning, metal evaporation, tube furnace annealing, photolithography and, most critically, ALD. Electrical measurements are then performed in stages: I-V measurements for device screening and C-V measurements for data extraction. Variants on these standard processes are discussed in chapters 6, 7 and 8.

Chapter 4

Theory of III-V MOS Capacitors

4.1 Introduction

In order to characterise the behaviour of fabricated metal-oxide-semiconductor capacitor (MOSCAP) test structures, the physical phenomena and theory in these structures must be considered. The principle of a MOSCAP test structure is to investigate the dielectric-semiconductor interface by depositing a metal cap layer and measure the impedance of the structure at variable DC gate voltage. In doing so, deviations from 'ideal' response will be observed due to defect/trap states in the system and these deviations can be used to characterise the trap quantities and characteristics. As an example, when an impedance-voltage measurement is performed on a semiconductor-dielectric interface with a high interface-trapped charge density, it will show a higher AC conductance due to charging and discharging of the interface states, and when a dielectric layer with a high fixed charge density is analysed it will show a DC voltage shift proportional to the fixed charge. A capacitor formed from a metal-dielectric-semiconductor layer structure is referred to as a MISCAP (metal-insulator-semiconductor capacitor) or, more frequently, MOSCAP and MOSCAPs are widely used to characterise semiconductor-dielectric interfaces by way of electrical measurement.

4.2 Ideal MOSCAP C-V Response

MOSCAPs are typically analysed using impedance measurement - most commonly the capacitance-voltage (C-V) response but also the conductance-voltage (G-V) and conductance-voltage-frequency (G-V-f) response, discussed in section 4.5. The C-V response is the dependant response of capacitance (measured by applying a small AC voltage) for variable DC voltage. It must be acknowledged that, despite the

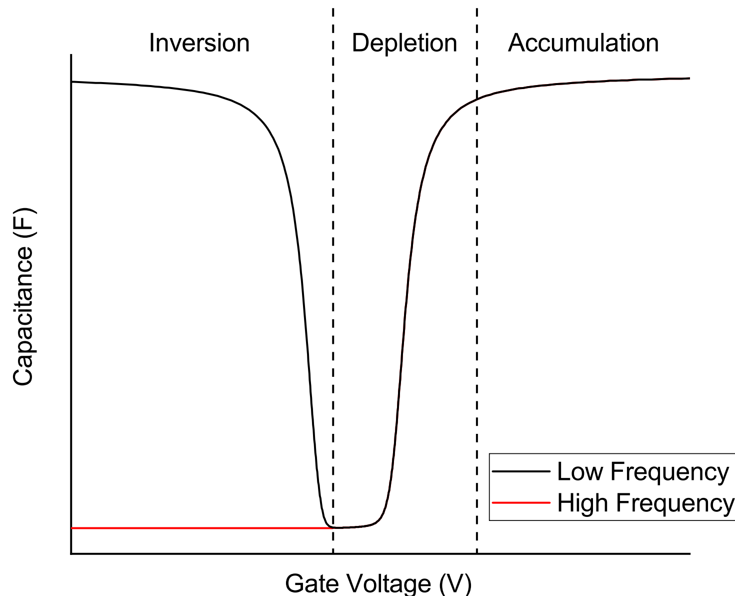


Figure 4.1: An ideal MOSCAP C-V response, with accumulation, depletion and inversion regions labelled for low frequency (black) and high frequency (red) cases

MOS structure forming a simple parallel-plate capacitor, the semiconductor displays voltage-dependant capacitance response as charge carriers are redistributed. This response is discussed qualitatively here and quantitatively in section 4.4.2.

4.2.1 Accumulation

When an n-type MOSCAP has a large positive DC bias applied, the electrons in the semiconductor accumulate at the surface. The semiconductor bands bend down (states closer to the interface become more energetically favourable for electrons) and electrons accumulate in the most favourable states closest to the interface (figure 5.14). A p-type MOSCAP displays the same response for a large negative DC bias, with the bands bending upwards and holes, rather than electrons, are accumulated. In the accumulation regime, the AC voltage causes the charge to change in the accumulation layer and the capacitance is dominated by the dielectric - in an ideal (silicon) MOSCAP, the capacitance associated with the semiconductor, C_s, is very large and can be neglected from the equivalent circuit (figure 4.2). As such, the measured capacitance is high and equivalent to a parallel-plate capacitor formed solely of the dielectric, as if the semiconductor were a metal. This high capacitance associated with the dielectric represents the maximum capacitance and is referred to as the oxide capacitance, C_{ox}.

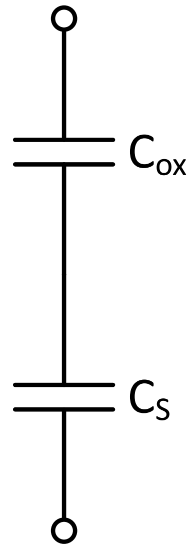


Figure 4.2: Equivalent circuit of ideal MOS capacitor

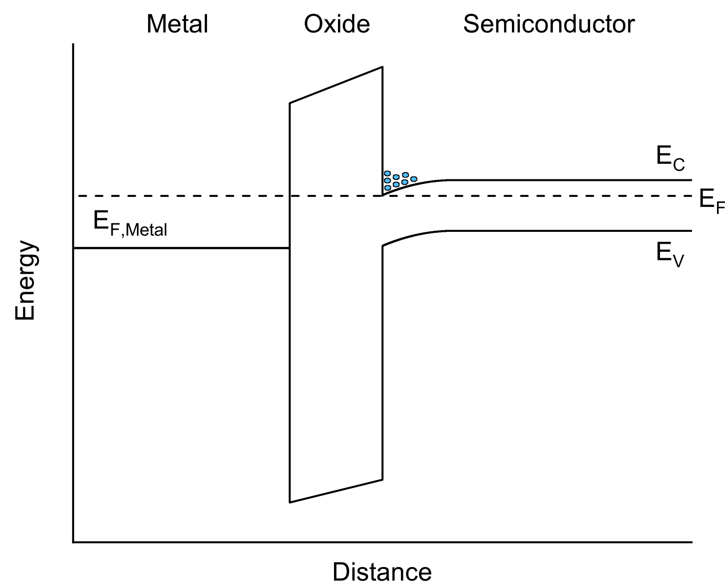


Figure 4.3: Band diagram for a MOS capacitor in accumulation. Excess electrons in the accumulation layer shown diagrammatically in blue

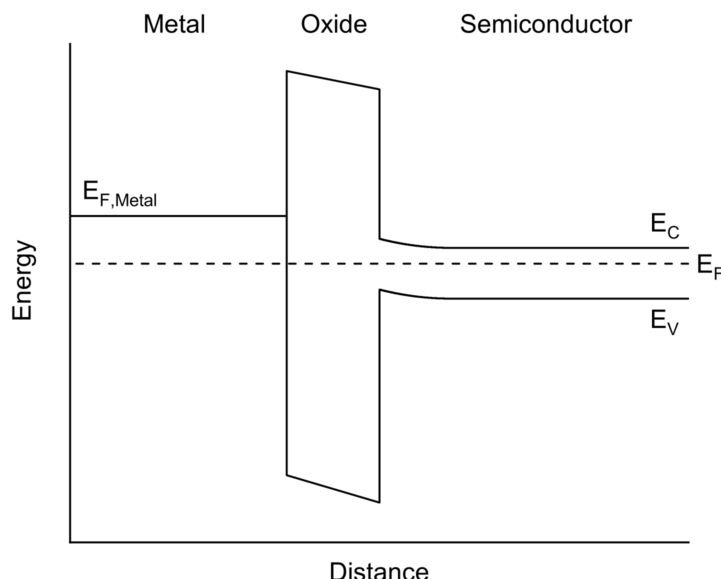


Figure 4.4: Band diagram for a MOS capacitor in depletion

4.2.2 Depletion

As the DC bias is decreased (increased for p-type) the accumulation regime breaks down, the band bending reduces and, ultimately, the bands begin to bend in the opposite direction (figure 4.4). For small negative DC bias (positive for p-type), the band bending causes charge at the interface to deplete and a depletion layer to form. In the depletion regime, the AC voltage causes charge modulation deeper in the semiconductor, beyond the depletion layer and the overall measured capacitance becomes dependant on both the dielectric and the depletion layer. One can consider the semiconductor capacitance C_s to have decreased to the point where it cannot be neglected, or one can consider the effective plate separation of the overall capacitor to have increased, but ultimately, the measured capacitance decreases in depletion.

4.2.3 Inversion

When a large negative DC bias is applied to an n-type MOSCAP, the bands bend up by such a large amount that the surface begins to resemble p-type material. The holes in the valence band accumulate in the states at the surface (high-energy states, unfavourable for electrons but favourable for holes) and form an inversion layer (figure 4.5). The same effect occurs for p-type material at high positive voltages, forming an electron inversion layer.

In contrast to the accumulation and depletion regimes, the inversion regime

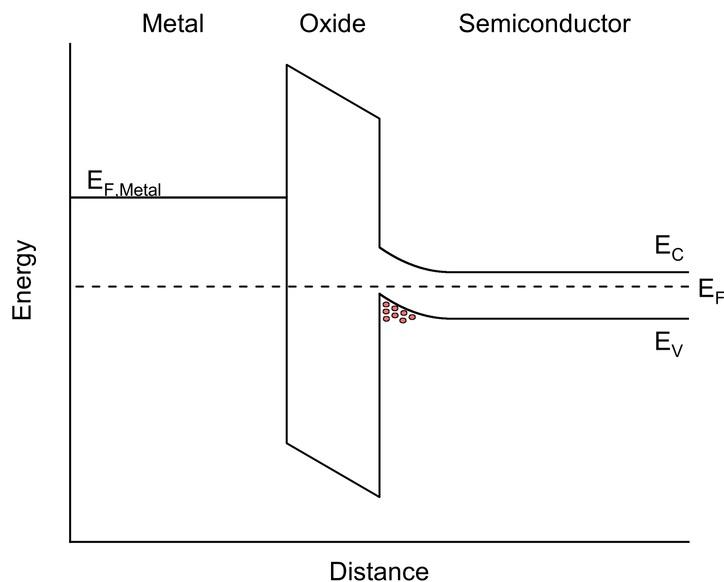


Figure 4.5: Band diagram for a MOS capacitor in inversion. Excess holes in the inversion layer shown diagrammatically in red

shows a frequency-dependant response. At low frequency, typically <1 kHz for silicon at room temperature, the generation, recombination and re-organisation of charge carriers is significantly faster than the AC oscillation used to measure capacitance. For low frequencies, where the minority carrier response time is shorter than half the period of the AC voltage, the charge in the inversion layer can follow the AC voltage, accumulating and depleting as the voltage is changing, similarly to the accumulation regime. As such, the measured capacitance for the inversion regime at low frequency is, as in the accumulation case, dominated by C_{ox} and the low frequency C-V response rises from the capacitance minimum in depletion back to C_{ox} in inversion.

At high frequencies, ∼1 MHz for silicon at room temperature, the minority carrier response time is longer than half the AC frequency. In this regime, an inversion layer exists but the generation and recombination of carriers is now sufficiently slow relative the the AC probe frequency that the charge in the inversion layer cannot follow the AC voltage and the density of charge carriers in the inversion layer remains constant over the period of the AC voltage. As such, the charge modulation induced by the AC voltage occurs at the edge of the depletion layer, similarly to the depletion regime, and the measured capacitance remains at the minimum observed in the depletion regime. Some re-organisation of charge in the inversion layer can occur, and quantitative modelling of this phenomenon is detailed in section 4.4.2.

4.3 Effect of Trapped Charge on C-V Response and Data Extraction

As previously outlined in section 2.3, Schroder[18] describes four types of charge which interfere with MOS systems (as a quantity of charge, Q, a number of states, N, or a density of states, D):

1. Interface-trapped charge (Q_{it}, N_{it}, D_{it})
2. Fixed oxide charge (Q_f, N_f)
3. Oxide-trapped charge (Q_{ot}, N_{ot}, D_{ot})
4. Mobile oxide charge (Q_m, N_m, D_m)

Mobile oxide charge consists of ionic impurities (typically alkali metals such as Na, K, Li, but potentially also H or heavy metals) which are capable of diffusing through the oxide. This process is most notable at elevated temperature, particularly high temperature bias-stress conditions, and gives rise to changes in device performance which cannot be reversed without similar bias-stress conditions on the structure. This behaviour is usually minimised for ambient temperature conditions. Mobile oxide charge is neglected for this thesis, as the removal of alkali metals and heavy metals has all but eliminated mobile oxide charge from modern devices.

Fixed oxide charge incorporates all charged oxide impurities and defects that do not change their charge over device operation. The effect of fixed charge is to shift the measured C-V response in the voltage (x) axis and this can be quantified by taking the flatband voltage. The flatband condition occurs when the semiconductor bands undergo no bending; in an ideal structure, free of trapped charge and with zero difference between the metal and semiconductor work functions (which can induce additional band bending), this occurs at 0 V but the addition of trapped charge will shift the voltage where this condition occurs. Methods to measure the flatband voltage (V_{FB}) are discussed in section 2.6 - the flatband point can be identified by the point of inflection when transitioning between accumulation and depletion but multiple differentials can exaggerate other trap-related features in the C-V response, reducing the reliability of the technique. As an alternative method, extracting the capacitance at the flatband condition (C_{FB}) from the modelled response and identifying the voltage where C_{FB} occurs in the measured response, requires a reliable MOSCAP model but is the preferred method in this thesis. Differences in work function between the semiconductor and the metal gate can also contribute to flatband voltage, however, these are difficult to calculate, as different deposition techniques

can affect the work function of metal thin films. As Al gate metal on InSb substrates is used almost exclusively in this thesis, work function differences are neglected.

Oxide-trapped charge is not as well-characterised for III-V MOSCAP systems as for Si-SiO_2 systems. Additional effects have been observed in III-V MOSCAPs which suggest trapping with a time constant longer than the better-characterised interface-trapped charge, contributing to hysteresis and to frequency dispersion in accumulation. These traps - their effect, models and analysis methods - are reviewed in section 2.3. For the purposes of this thesis, they are quantified using hysteresis voltage at C_{FB} (V_H) and occasionally using frequency dispersion in accumulation, expressed as percentage shift in accumulation capacitance per decade increase in frequency.

Interface-trapped charge (D_{it}), comprised of charge states at the interface which interact with the semiconductor with a short time constant, is the most widely-studied and well-modelled type of trap state in the MOS system. It has effects on a MOSCAP C-V associated with both AC and DC voltages independently. The AC effect of D_{it} can be observed in low-frequency C-V measurements: the minimum capacitance for low-frequency (LF) measurements is higher than for high-frequency (HF) measurements (figure 4.6). This is due to the trap states responding to the AC voltage, changing their occupancy as the conduction/valence band states would in accumulation and inversion and effectively forming a capacitor in parallel with C_s (figure 4.7), causing the measured capacitance to rise. This effect is observed in the low frequency response only, as the trap states cannot change their occupancy over the timescale of half a high frequency period.

These effects can be used to quantify the density of interface-trapped charge (D_{it}), with extraction techniques also enabling D_{it} to be mapped to energy levels in and close to the semiconductor bandgap. All equations in this section are taken from Schroder[18]

4.3.1 The High-Low Method

The AC effect of interface traps can be used to measure the magnitude of D_{it}. Scroder[18] outlines a series of equations for measured capacitance: based on the equivalent circuits shown in figures 4.2 and 4.7, the measured capacitance for high frequency (free of AC trap effects) and low frequency (including trap effects) are given by equations 4.1 and 4.2.

$$C_{hf} = \frac{C_{ox} C_S}{C_{ox} + C_S} \tag{4.1}$$

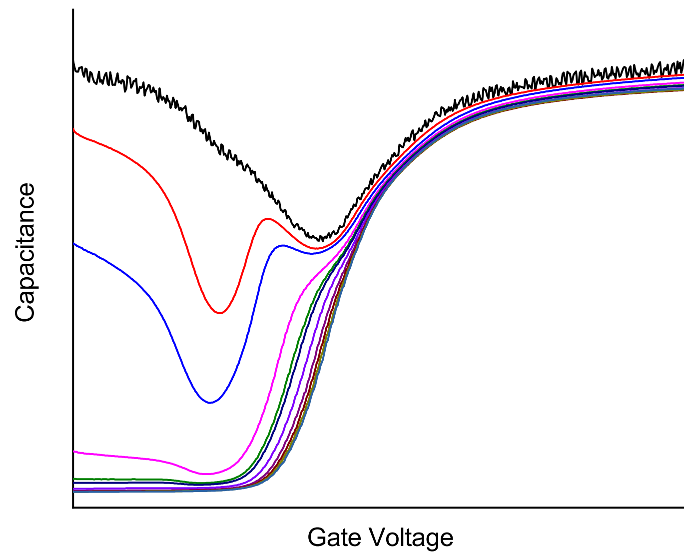


Figure 4.6: Example measured MOSCAP C-V response for InSb MOSCAP at 80 K

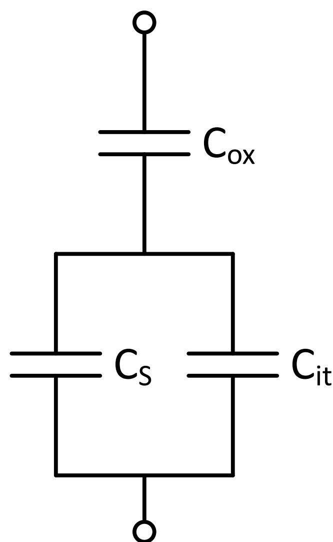


Figure 4.7: Equivalent circuit of real MOS capacitor, including interface-trapped charge

$$C_{lf} = \left(\frac{1}{C_{ox}} + \frac{1}{C_S + C_{it}}\right)^{-1} \tag{4.2}$$

In equations 4.1 and 4.2, C_{hf} and C_{lf} are the measured capacitance per unit area in the high-frequency and low-frequency regimes, C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance (i.e. the capacitance associated with the depletion region) and C_{it} is the capacitance associated with the interface-trapped charge. Equation 4.2 can be rewritten to give D_{it}, giving equation 4.3. Note that the factor of $\frac{1}{q}$ applies for D_{it} in energy units of electron volts, and is substituted for $\frac{1}{q^2}$ for energy units of joules.

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_S\right) \tag{4.3}$$

In equation 4.3, q is the electron charge. By rearranging equation 4.1 to give C_S and substituting the resultant equation into equation 4.3, D_{it} can be expressed using only measured values, as shown in equation 4.4.

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{4.4}$$

Equation 4.4 expresses D_{it} as a function of gate voltage, V_G. In order to convert gate voltage to a surface potential (energy level), an integral expression - presented by Schroder but first developed by Berglund[94] - is used.

For a MOSCAP in accumulation, C_{lf} can be expressed as a function of total capacitor charge (Q) and total applied voltage (gate voltage, V_G), as in equation 4.5:

$$C_{lf}(V_G) = \frac{dQ}{dV_G} \tag{4.5}$$

However, dQ can also be expressed using the C_{ox} and the potential difference across the oxide alone (V_{ox}), as in equation 4.6:

$$C_{ox}(V_G) = \frac{dQ}{dV_{ox}} \tag{4.6}$$

Substituting dQ in equation 4.5 results in equation 4.7:

$$C_{lf}(V_G) = C_{ox}\frac{dV_{ox}}{dV_G} \tag{4.7}$$

As gate voltage is the sum of surface potential (ψ_s, the energy difference between the semiconductor bulk and the surface/interface) and V_{ox} (equation 4.8), equation 4.7 can be rewritten as 4.9:

$$V_G = V_{ox} + \psi_s(V_G) \tag{4.8}$$

$$C_{lf}(V_G) = C_{ox}\left(1 - \frac{d\psi_s(V_G)}{dV_G}\right) \tag{4.9}$$

Equation 4.9 can be rearranged to give equation 4.10:

$$\frac{d\psi_s(V_G)}{dV_G} = 1 - \frac{C_{lf}(V_G)}{C_{ox}} \tag{4.10}$$

When integrated with respect to dV_G, the result is the widely-used Berglund integral equation, shown in equation 4.11

$$\psi_s(V_G) = \int_{V_{G1}}^{V_{G2}}\left(1 - \frac{C_{lf}(V_G)}{C_{ox}}\right)dV_G + \Delta \tag{4.11}$$

In equation 4.11, Δ is the surface potential at V_{G1}. For conventional silicon MOSCAPS, the high density of states in the conduction and valence bands prevents the Fermi level from shifting into the bands and, even in strong accumulation, the surface potential cannot rise above/below the conduction/valence band edge, respectively (N.B. in silicon nanodevices, such as nanowires and finFETs, reduction in DOS can allow E_F to drift 20 meV into the conduction band). As a consequence, when strong accumulation is taken as one of the integral limits (V_{G1} or V_{G2}), it can be assumed that the surface potential for this limit is at the conduction/valence band edge (for n-type/p-type). As discussed below in section 4.4, the density of states in the conduction band of III-V materials cannot be assumed to be sufficiently high for this approximation to hold and the surface potential can increase past the band edge. In this case, the flatband point is taken as the integral limit, setting Δ to zero and producing equation 4.12.

$$\psi_s(V_G) = \int_{V_{FB}}^{V_G}\left(1 - \frac{C_{lf}(V_G)}{C_{ox}}\right)dV_G \tag{4.12}$$

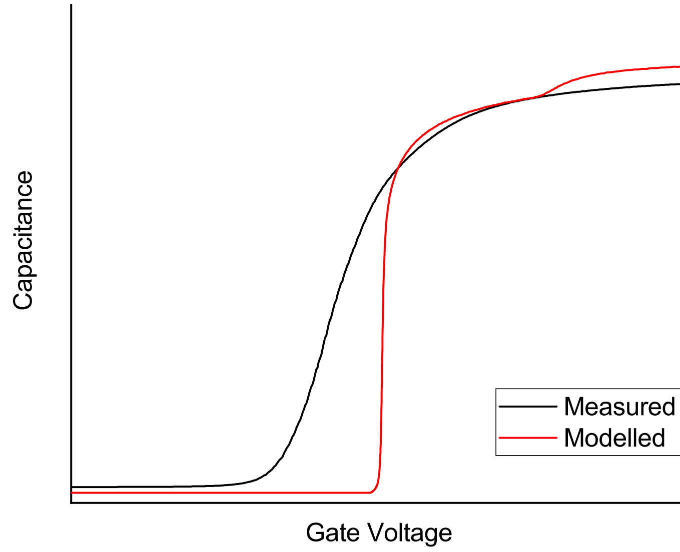


Figure 4.8: Example MOSCAP C-V response for InSb MOSCAP at 80 K. Black: measured response, red: modelled response following section 4.4 and section 5.2.

Equations 4.4 and 4.12 can be used in conjunction to map D_{it} within a finite region of the bandgap. This technique is referred to as the high-low method.

4.3.2 The Terman Method

The DC effect of D_{it} is observed as a 'stretching-out' of the real C-V response compared to the ideal response. This 'stretching' effect is simply due to trap states filling/emptying as V_G is varied, reducing the band bending of the semiconductor. An example is shown in figure 4.8, with the features of the modelled response detailed in section 4.4.

To derive an equation to extract D_{it} quantitatively, equation 4.13 for gate voltage, taken from Schroder[18] must first be considered.

$$V_G = V_{FB} + \psi_s - \frac{Q_S + Q_{it}}{C_{ox}} \tag{4.13}$$

In equation 4.13, V_{FB} is the flatband voltage, ψ_s is the surface potential, Q_S is the total charge per unit area in the semiconductor, Q_{it} is the charge per unit are in trap states and C_{ox} is the oxide capacitance. By differentiating equation 4.13 with respect to ψ_s and rearranging, equation 4.14 is produced, expressing D_{it} in terms of

V_G, ψ_s, C_S and C_{ox}.

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\left[\frac{dV_G}{d\psi_s} - 1\right] - \frac{C_s(\psi_s)}{q} \tag{4.14}$$

Equation 4.14 can be further modified to give equation 4.15, expressing D_{it} in terms of voltage shift ('stretch-out'), measurable from comparison between modelled and measured C-V.

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\frac{d\Delta V_G}{d\psi_s} \tag{4.15}$$

In equation 4.15, $\Delta V_G = V_{G,Meas} - V_{G,Sim}$ is the voltage shift between the measured and modelled C-V responses. This technique also enables D_{it} extraction and mapping to surface potential (energy level) and is referred to as the Terman method, after its pioneer.[101]

4.4 Ideal Response of III-V MOSCAPs

The equations for MOSCAP analysis and response found in textbooks such as Sze[12] and Pierret[13], particularly those involved in modelling the ideal response for the Terman method, typically assume a silicon substrate and SiO_2 dielectric. By contrast, narrow bandgap III-V materials such as InSb and InGaAs have different band structures, with features that affect C-V response.

4.4.1 Band Structure of III-V Materials

In III-V materials, there are several parts of the valence and conduction bands which contribute to the overall charge carrier concentration. The valence band is practically identical to group IV materials, with a heavy hole band dominating, a light hole band occurring at the same energy with a lower density of states (DOS) and a split-off band occurring at much lower energy, so low that it will be completely filled for the purposes of this thesis. The conduction band contains three relevant minima, occurring at three different wavevectors which are assigned the labels Γ, L and X. The Γ valley offers a direct transition to the valence band maximum, whereas the L and X valleys occur at different wavevectors. In aluminium and phosphorus-containing binary III-Vs, the Γ valley often occurs at a higher energy than the L and X valleys, giving an indirect bandgap, but the InSb and AlInSb modelled in

this thesis, as well as the InGaAs modelled for background and comparison, have a direct bandgap and are dominated by the Γ valley.

The effect of the higher valleys can be seen in the modelled response in figure 4.8, where a 'hump' feature is visible in strong accumulation. This hump feature is absent from measured data - this may be due to the L valley occurring at a higher energy than predicted, as the offset between the Γ valley and higher valleys in InSb is not well-known. The comparison to measured charge data in figure 5.6 supports this explanation, with the highest data point showing the greatest deviation from the modelled response. The absence of the feature may also be due to the effect of interface traps, such as the 'stretch out' effect discussed in section 4.3.2 or the AC effect discussed in section 4.3.1.

Narrow bandgap III-Vs have a low density of states (DOS) in the Γ valley of the conduction band, described by a low electron effective mass m^* (see table 4.3). The low DOS results in a lower electron concentration for a given bias potential and a lower capacitance for a given gate voltage than a classical Si approximation. As a specific example, even at very high bias which strains the breakdown limit of the dielectric, the maximum capacitance will be lower than C_{ox}.[23]

The Γ valley of narrow bandgap III-Vs also exhibits another unique property in that it does not follow the parabolic DOS approximation. The standard approximation for DOS in the conduction band of a material is a parabolic function of energy, but in narrow bandgap III-Vs the DOS increases more sharply with energy. The nonparabolicity results in higher electron concentrations at high bias potential than in a classical parabolic model and, as a result of low DOS and nonparabolicity, the capacitance of a narrow bandgap III-V C-V response will continue to rise for high gate voltages.

The final feature of III-V materials which affects C-V response is the presence of the valleys at the L and X wavevectors. While these valleys are not easily filled due to their high energy and indirect transition from the valence band, the high bias potential from the extreme end of a C-V sweep can cause the higher valleys to fill. This gives rise to a 'shoulder' feature in the C-V response, as the additional charge in the higher valleys causes the capacitance to rise higher than if the Γ valley alone is considered.

4.4.2 Modelling of III-V C-V Response

The complex band structure of narrow bandgap III-V materials necessitates a more comprehensive model than those featured in textbooks. Engel-Herbert et al[23] present a model for a complex III-V band structure:

The electron concentration associated with an individual conduction band minimum is given by equation 4.16 and the hole concentration associated with an individual valence band maximum is given by equation 4.17.

$$n_i[\varphi(x)] = \frac{4}{\sqrt{\pi}} \left(\frac{2\pi k_B T m_0 m^*}{h^2}\right)^{3/2} \int_0^\infty \frac{\sqrt{\eta}\sqrt{(1+\alpha\eta)}(1+2\alpha\eta)}{exp[\eta - \frac{q\varphi(x)}{k_B T} + \frac{E_g - E_I}{k_B T}] + 1} d\eta \tag{4.16}$$

$$p_i[\varphi(x)] = \frac{4}{\sqrt{\pi}} \left(\frac{2\pi k_B T m_0 m^*}{h^2}\right)^{3/2} \int_0^\infty \frac{\sqrt{\eta}}{exp[\eta + \frac{q\varphi(x)}{k_B T} + \frac{E_I + E_{off}}{k_B T}] + 1} d\eta \tag{4.17}$$

In equations 4.16 and 4.17, the independent variables are temperature T, electrostatic potential φ, given by $\varphi = \frac{E_F - E_I}{q}$ (E_F and E_I are the Fermi level and intrinsic Fermi level, respectively, with E_F determined numerically and $E_I = \frac{E_g}{2} + 0.75 k_B T log(\frac{m^*_{hh}}{m^*_e})$), and normalised electron kinetic energy η, given by $\eta = \frac{E - E_C}{k_B T}$. The constants from the equation are given in table 4.7 and the material parameters for individual conduction band minima and valence band maxima are given in tables 4.1 and 4.2 for InSb. Energy levels are referenced to the top of the valence band.

The most notable non-standard features of equations 4.16 and 4.17 are the non-parabolicity terms in equation 4.16 - the terms of $\sqrt{(1+\alpha\eta)}$ and $(1+2\alpha\eta)$ - and the valence band offset term, E_{off}, in equation 4.17. E_{off} accounts for the offset between the heavy hole/light hole valence bands and the split-off valence band: the term is zero for the heavy hole and light hole bands and non-zero for the split-off band. Apart from these additional features, equations 4.16 and 4.17 are identical to standard carrier concentration equations, such as those presented in Sze[12] and Pierret[13].

The nonparabolicity model is developed from **k**.**p** modelling of III-V semiconductors:[102][103][104]. A nonparabolicity factor α governs a polynomial (quadratic) expression of energy, resulting in higher-order dependencies between energy and DOS ($E^{\frac{3}{2}}$). Notably, when α is set to zero, the model reduces to the classical parabolic approximation.

By solving the Poisson equation and applying Gauss's law, as presented in Engel-Herbert *et al.*, it is possible to express the semiconductor's total charge per unit area, Q_s, as a function of surface potential (the electrostatic potential of the surface, ψ_s). Equation 4.18 shows this relationship.

Table 4.1: InSb material parameters for conduction band minima

Parameter	Symbol	Units	Γ valley	L valley	X valley
Energy level of minima	E_g	eV	See section 4.6.1	0.68	1.0
Electron effective mass	m^*	m_0	See section 4.6.1	0.25	0.61
Nonparabolicity parameter	α	eV^{-1}	4.1	0	0

Table 4.2: InSb material parameters for valence band maxima

Parameter	Symbol	Units	Heavy hole	Light hole	Split-off
Energy level of maxima	E_{off}	eV	0	0	0.8
Hole effective mass	m^*	m_0	0.43	0.015	0.19

$$Q_s(\psi_s) = -\mathrm{Sign}(\psi_s)\sqrt{2\int_{\varphi_b}^{\varphi_b+\psi_s} -q\epsilon_{semi}\{N_D - N_A + p[\varphi(x)] - n[\varphi(x)]\}d\varphi(x)} \tag{4.18}$$

In equation 4.18, ϵ_{semi} is the permittivity of the semiconductor (ϵ_0 multiplied by the relative permittivity κ), N_D and N_A are the electron donor and acceptor concentrations, respectively, and $p[\varphi(x)]$ and $n[\varphi(x)]$ are the total hole and electron concentrations, respectively. φ_b is the electrostatic potential in the bulk substrate, unperturbed by the applied gate voltage, $\varphi_b = \frac{E_{F,bulk}-E_I}{q}$, and is calculated numerically by applying the charge neutrality condition to equations 4.16 and 4.17 (i.e. for the correct E_F value and $\varphi = 0$, $N_D - N_A + p[\varphi(x)] - n[\varphi(x)] = 0$). Once Q_s is known, the semiconductor capacitance C_{dos} and gate voltage V_g can be calculated using equations 4.19 and 4.20 (where $\Delta\phi_{ms}$ is the difference between the metal and semiconductor work functions).

$$C_{dos}(\psi_s) = -\frac{dQ_s(\psi_s)}{d\psi_s} \tag{4.19}$$

$$V_g = \psi_s + \Delta\phi_{ms} - \frac{Q_s(\psi_s)}{C_{ox}} \tag{4.20}$$

Alternative equations are required for the high frequency case. In the low frequency case, it is assumed the change in AC stimulus voltage is slower than the minority carrier response time and that equilibrium conditions can be assumed for

carrier concentration. In the high frequency case, however, the change in AC stimulus voltage is assumed to outpace than the minority carrier response time and, consequently, quasi-Fermi levels must be used to describe majority and minority carrier concentrations. Moreover, although the minority carrier population does not change, the minority carriers in the inversion layer will polarise in response to the AC stimulus: for a hole inversion layer, rising potential will cause holes to shift away from the surface and falling potential will cause holes to shift towards the surface (vice versa for electrons) without the total population changing.

In order to model these conditions, the following equations are used, taken from Brews[105] and Nicollian and Brews[106].

$$F(U) = \sqrt{2}\sqrt{e^{-U} + U - 1 + e^{2U_b}(e^U - 1)} \tag{4.21}$$

$$\Delta = \frac{F(U_s)}{e^{U_s} - 1} \int_0^{U_s} \frac{e^U - e^{-U} - 2U + (\frac{n_i}{N})^2 (e^U(U-2) + U + 2)}{F(U)^3} dU - (1 + \frac{n_i}{N}) \tag{4.22}$$

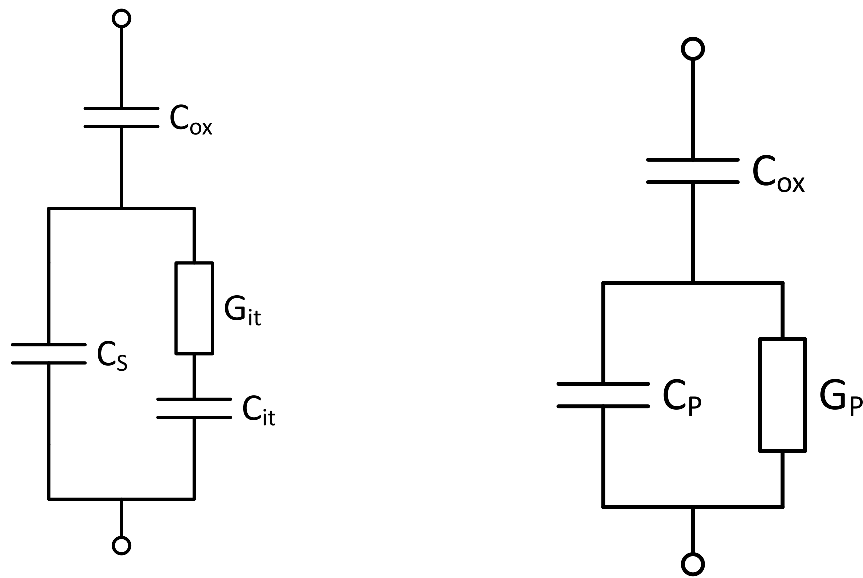
$$C_{dos}(U_s) = C_{FB}(1 - e^{-U_s} + \frac{n_i)}{N}^2 ((e^{U_s} - 1)\Delta + 1))F(U_s)^{-1} \tag{4.23}$$

In equations 4.21-4.23, potential is expressed in reduced units $U = \frac{\varphi q}{k_B T}$, with U_s and U_b corresponding to ψ_s and φ_b in equation 4.18. n_i is the intrinsic carrier concentration, N is the majority dopant concentration and C_{FB} is the flatband capacitance, here calculated from equations 4.16-4.19 at $\psi_s = 0$.

4.5 Conductance Response and Analysis

The conductance method is predicated on the principle of electron/hole capture/emission by trap states being a lossy process (this model is discussed in finer detail in Nicollian and Brews[106]). An equivalent circuit is shown in figure 4.9a, where G_{it} (reciprocal of resistance R_{it}) represents losses from the capture/emission of carriers to/from the interface traps, represented by C_{it}. When considering measurement and device characterisation, it is convenient to redraw figure 4.9a as figure 4.9b, representing all capacitance and resistance/conductance elements as lumped elements C_P and G_P.

At very low frequencies, the emission/capture from/to interface traps can be considered instantaneous relative to the AC probe frequency and the energy loss is



(a) Equivalent circuit showing interface trapped charge (C_{it}) and the associated loss element (G_{it})

(b) Equivalent circuit showing C_P and G_P lumped elements

Figure 4.9: Equivalent circuits for real MOSCAPs, including conductance response elements

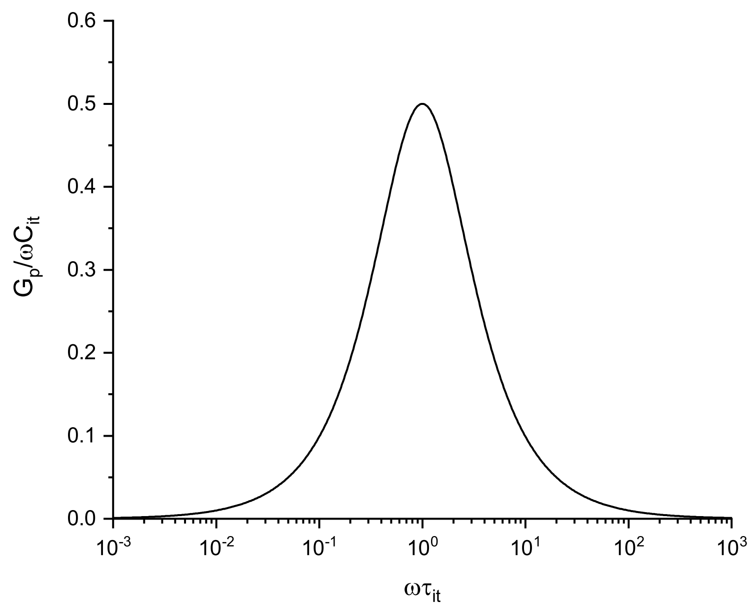


Figure 4.10: Trap-induced energy loss ($\frac{G_P}{\omega C_{it}}$) as a function of angular frequency (ω) normalised by interface trap time constant τ_{it}

low. This is shown on the left side of figure 4.10, with $\frac{G_P}{\omega C_{it}}$ representing the energy loss (with the frequency represented as angular frequency, ω) and the AC frequency normalised by multiplying it with the time constant of the interface traps which are filling/emptying with the AC oscillation ($\tau = \frac{C_{it}}{G_{it}}$). As the AC frequency increases, the energy loss increases to a maximum, when $\omega = \tau$. Above this, traps become unable to respond to the AC oscillation and the energy loss drops and ultimately becomes negligible at very high frequencies. Figure 4.10 illustrates these phenomena.

4.5.1 Conductance Modelling of Interface-trapped Charge Density

Following this principle, Schroder[18] presents equation 4.24 for a simplified single-level trap model. Equation 4.24 expresses normalised parallel conductance ($\frac{G_P}{\omega}$) as a function of angular frequency (ω), trap time constant (τ_{it}), electron charge (q) and interface-trapped charge density (D_{it}).

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}^2 D_{it}}{1 + (\omega\tau_{it})^2} \tag{4.24}$$

When modelling interface-trapped charge as a continuum of states, a more generalised form is used, detailed in Schroder. This equation, however, reduces to an approximate expression, given in equation 4.25 for interface-trapped charge density as a function of maximum $\frac{G_P}{\omega}$.

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_P}{\omega}\right)_{max} \tag{4.25}$$

As equation 4.25 uses equivalent parallel conductance (G_P), with the contribution of oxide capacitance (C_{ox}) removed, the measured conductance and capacitance, G_m and C_m, must be used to extract $\frac{G_P}{\omega}$ following equation 4.26.

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{4.26}$$

Using these equations, D_{it} can be quantified using capacitance and conductance data. This is known as the conductance method.

4.5.2 Interface-trapped Charge Energy Level in Conductance Response Models

The method and equations discussed in section 4.5.1 allow D_{it} to be quantified for a finite energy range close to the Fermi level. Any traps which change their occupancy over the period of the AC oscillation contribute to the measured conductance and can be quantified. As the DC voltage is varied and the Fermi level shifts, the sampled trap energy level changes but, as the traps capture/emit carriers predominantly to the majority carrier band edge, the time constant, τ_{it}, for the capture/emission process changes too. Equation 4.27, adapted from Engel-Herbert *et al.*[23], gives τ_{it} as a function of ΔE, the difference in energy level between the active traps and the majority carrier band edge.

$$\tau_{it} = \frac{exp[\frac{\Delta E}{k_B T}]}{\sigma v_{th} N_{maj}} \tag{4.27}$$

In equation 4.27, v_{th} is the thermal velocity of majority carriers, σ is the trap capture cross-section, q is the electron charge, k_B is Boltzmann's constant, T is the temperature in kelvin and N_{maj} is the effective density of states for the majority carrier band. As the conductance maximum, characterised in equation 4.25, occurs when $\omega\tau_{it} = 1$, equation 4.27 can be rewritten to give equation 4.28 for trap energy level (relative to the majority carrier band edge).

$$\Delta E = k_B T \log \frac{v_{th} \sigma N_{maj}}{\omega} \tag{4.28}$$

The calculation of N_{maj} is discussed below in section 4.6.1, as these parameters can vary with temperature. v_{th} can also be calculated, using equation 4.29.

$$v_{th} = \sqrt{\frac{3k_B T}{m^* m_0}} \tag{4.29}$$

In equation 4.29, k_B is Boltzmann's constant, T is the temperature in kelvin, m^* is the effective mass of carriers (effective mass of electrons for v_{th} of electrons, similar for holes) and m_0 is the electron rest mass. The only other outstanding material parameter from equation 4.28 is the trap capture cross-section (σ). Trap capture cross-section can be extracted using deep-level transient spectroscopy (DLTS) but it is uncommon for published work to study and/or report this data and, as scarcity of material data is exaggerated for lesser-studied materials such as InSb, no literature

values have been found for the parameter. Engel-Herbert *et al.*[23] note the role the parameter plays in energy mapping of D_{it} data, but they also note that it is relatively insensitive to inaccuracy, noting ~60 meV per decade error in σ at room temperature and reduced error at low temperature. As a consequence, the value of σ they report for InGaAs (1×10^{-14} cm^2) is taken as an approximation for InSb. Taking this value may result in inaccurate energy mapping of D_{it}, although analysis and discussion in subsequent chapters focus on minimum D_{it}, further reducing the influence of σ.

Based on the principles discussed here, D_{it} can be quantified and mapped to energy levels based on conductance data, as well as capacitance data.

4.6 Material Modelling

Material data for III-Sb compound semiconductors is scarce and most data used in this thesis is taken from Vurgaftman *et al.*[107], Levinstein *et al.*[6] and Landolt-Börnstein (group III volume 17 subvolume a) [108]. Material data used for modelling is summarised in table 4.3.

Data for $In_{0.53}Ga_{0.47}As$ is taken from Engel-Herbert et al [23]. For InSb, the energy gap of the L valley, E_L, was taken from Asauskas et al.[109], as this figure was calculated for a low temperature experiment similar to the characterisation used in this thesis. The effective mass of electrons in the X valley, m_X^*, for InSb was calculated in house by Dr. Neophytos Neophytou, employing the sp3s*d5 tight-binding model[110]. The tight-binding parameters used for InSb were taken from Jancu *et al.*[111]

For InSb, the best-known material parameter from table 4.3 is the bandgap: $E_\Gamma = 0.17\ eV$ at room temperature. The effective mass of the Γ valley is also well-known, as is the effective mass of heavy holes, relative permittivity and intrinsic carrier concentration. The properties of the L and X valleys are less well-known, with the energy gap of the valleys showing ~0.6 eV variability within the reviewed literature and models. The nonparabolicity factor is also only reported in Levinstein *et al.*, and so its effect on carrier concentration is verified in section 5.4.2. Other lesser-known parameters - the effective mass of the L and X valleys and the properties of the split-off band - are not expected to impact on data extraction.

Table 4.3: Material parameters of III-V semiconductors

Parameter	Units	Symbol	$In_{0.53}Ga_{0.47}As$	InSb	AlSb	GaSb	Si
Energy gap of Γ valley	eV	E_Γ	0.81	$0.17^\dagger$	$2.300^\dagger$	$0.727^\dagger$	N/A
Energy gap of L valley	eV	E_L	1.29	0.68	$2.210^\dagger$	$0.753^\dagger$	2.0
Energy gap of X valley	eV	E_X	1.27	1.00	$1.616^\dagger$	$1.03^\dagger$	1.12
Split-off energy	eV	E_{so}	0.25	0.81	0.676	0.76	0.044
Effective mass in Γ valley	m_0	m^*_Γ	0.043	$0.014^\dagger$	$0.14^\dagger$	$0.031^\dagger$	N/A
Effective mass in L valley	m_0	m^*_L	0.42	0.25	1.12	0.59	0.36
Effective mass in X valley	m_0	m^*_X	0.74	0.61	0.57	0.87	1.09
Effective mass of heavy holes	m_0	m^*_{hh}	0.46	0.43	0.94	0.71	0.81
Effective mass of light holes	m_0	m^*_{lh}	0.052	0.015	0.11	0.044	0.16
Effective mass in split-off band	m_0	m^*_{so}	0.16	0.19	0.22	0.12	0.24
Nonparabolicity factor	eV^{-1}	α	1.24	4.1	0.31	1.46	N/A
Relative permittivity	ϵ_0	κ_{semi}	13.9	16.0	11.2	16.0	11.68
Intrinsic carrier concentration	cm^{-3}	n_i	4.3×10^{-9}	$2\times10^{16\dagger}$	$4.12\times10^{5\dagger}$	$1.02\times10^{13\dagger}$	1.0×10^{10}

Table 4.4: Varshni parameters for III-Sb semiconductors

Material	Valley	$E_g(0)$ (eV)	α_V (meV K^{-1})	β_V (K)
InSb	Γ	0.235	0.32	170
AlSb	Γ	2.386	0.42	140
AlSb	L	2.329	0.58	140
AlSb	X	1.696	0.39	140
GaSb	Γ	0.812	0.417	140
GaSb	L	0.875	0.597	140
GaSb	X	1.141	0.475	94

4.6.1 Temperature Dependence of Material Parameters

Material parameters such as band energies and effective masses are dependent on temperature. In order to accurately model test structures at the cryogenic temperatures required for characterisation, some parameters are modelled as temperature dependent. All temperature-dependent models were verified against data at 300 K (taken from e.g. Levinstein *et al.*[6]) and, where available, data from previous models. Equation 4.30 below is the empirical Varshni expression, taken from Vurgaftman [107].

$$E_g(T) = E_g(0) - \frac{\alpha_V T^2}{T + \beta_V} \tag{4.30}$$

In equation 4.30, $E_g(0)$ is the energy gap at zero kelvin, T is temperature in units of kelvin and α_V and β_V are the Varshni parameters. The Varshni parameters for of InSb, AlSb and GaSb, where available, are given in table 4.4. Where Varshni paramaters are unavailable, constant, temperature-independent values are used (see table 4.1).

The effective mass also displays temperature dependency. Equation 4.31, taken from Vurgaftman, allows effective mass to be calculated from the temperature-dependent energy gap value and is a reliable temperature-dependent model for the Γ valley, reproducing values reported at specific temperatures.

$$m^* = (1 + 2F) + \frac{E_P(E_g + 2E_{so}/3)}{E_g(E_g + E_{so})} \tag{4.31}$$

†typical room temperature value, see section 4.6.1 for details of temperature sensitive calculation

Table 4.5: Parameters for temperature-dependent effective mass calculation

Material	E_{so} (eV)	F	E_P (eV)
InSb	0.81	-0.23	23.3
AlSb	0.676	-0.56	18.7
GaSb	0.76	-1.63	27.0

Equation 4.31 is based on the multiband $\mathbf{k} \cdot \mathbf{P}$ method for band structures. The matrix elements of the momentum operator between the conduction and valence bands can be condensed into a single material parameter, E_P, and the contribution to the conduction band from higher bands can be expressed using the Kane parameter, F. E_{so} is the split-off energy of the valence band. F and E_P are given by Vurgaftman for different materials, where their derivation is also discussed in more detail. These parameters are outlined for InSb, AlSb and GaSb in table 4.5.

The final parameter calculated with temperature dependence is intrinsic carrier concentration. This is calculated from the other temperature-dependent parameters using equations 4.32 - 4.34, taken from Sze [12] and Pierret [13].

$$N_c = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{3/2} \tag{4.32}$$

$$N_v = 2\left(\frac{2\pi m_h^* k_B T}{h^2}\right)^{3/2} \tag{4.33}$$

$$n_i = \sqrt{N_c N_v} e^{-E_g/2k_B T} \tag{4.34}$$

In equations 4.32 - 4.34, m_e^* and m_h^* are the density of states electron and hole effective masses, respectively, N_c and N_v are the effective densities of states in the conduction and valence bands, respectively, E_g is the energy gap of the dominant conduction band valley and n_i is the intrinsic carrier concentration. The dominant valley in InSb is the Γ valley and the dominant valley in AlSb is the X valley but, in GaSb, the conduction band valleys lie close together. In GaSb, the dominant energy gap is that of the Γ valley, which lies lowest, but the higher effective mass of the L valley, which lies only 26 meV higher at room temperature, causes it to dominate the effective density of states calculation. This distinction is also important for ternary materials as the bandgap changes from direct to indirect.

Table 4.6: Bowing parameters for III-Sb ternary alloys

Material	Parameter	C
AlInSb	E_Γ	0.43
AlInSb	E_{so}	0.25
AlInSb	m^*_Γ	0.038
GaInSb	E_Γ	0.415
GaInSb	E_L	0.4
GaInSb	E_X	0.33
GaInSb	E_{so}	0.1
GaInSb	m^*_Γ	0.0092
GaInSb	m^*_{lh}	0.011

4.6.2 Ternary Alloys

Material models for ternary III-V alloys are usually based on an interpolation between the more well-known binary materials. The simplest model is a linear interpolation but a more sophisticated quadratic approximation is sometimes available for more well-known parameters and material systems. This approximation is referred to as a bowing equation, with a typical bowing equation for energy gap shown in equation 4.35

$$E_g(x) = (1-x)E_g(0) + xE_g(1) - x(1-x)C \tag{4.35}$$

In equation 4.35, x is the decimal composition of one constituent, $E_g(0)$ is the energy gap of the binary where $x = 0$, $E_g(1)$ is the energy gap of the binary where $x = 1$ and C is the bowing parameter. As an example, consider $Al_{0.2}In_{0.8}Sb$. In this case, $x = 0.2$, $E_g(0)$ is the energy gap of InSb and $E_g(1)$ is the energy gap of AlSb. Note that the bowing equation is reversible, i.e. calculating the same parameter for $Al_{0.15}In_{0.85}Sb$ and $In_{0.85}Al_{0.15}Sb$ will produce the same result. Table 4.6 summarises known bowing parameters, taken from Vurgaftman [107]. The bowing parameter for effective mass of AlInSb is taken from a previous model.

4.7 Conclusion

The ideas and equations above are essential to characterising dielectric interfaces. By understanding the features of a MOS capacitor C-V and G-V measurement, interface-trapped charge and fixed charge can be characterised. Furthermore, using the quantitative model, unique features of different materials can be investigated,

Table 4.7: Physical constants for equations in chapter 4

Parameter	Symbol	Value	Units
Electron charge	q	1.602×10^{-19}	C
Boltzmann's constant	k_B	1.38×10^{-23}	J K^{-1}
Electron mass	m_0	9.109×10^{-31}	kg
Planck's constant	h	6.626×10^{-34}	J s
Permittivity of free space	ϵ_0	8.854×10^{-14}	F m^{-1}

highlighting their advantages and disadvantages in a range of test and practical applications.

Chapter 5

Modelling and Analysis of InSb MOS Capacitors

5.1 Introduction

The foundational theoretical work on modelling and data extraction for MOS capacitors must be applied and expanded for InSb. The content of this chapter extends on the standard models and methods in chapter 4 to effectively characterise InSb MOS capacitors specifically, and to guide experimental work. A modelling and analysis code suite has been developed for InSb and verified against literature data. This code suite has been supplemented by revised and extended methods of data extraction and modelling performed on phenomena unique to InSb which influence C-V measurements. In this chapter, details are provided on the implementation and verification of standard modelling and analysis techniques for InSb, how data extraction and analysis were performed (including development of a revised technique) and how modelling techniques were used to investigate narrow bandgap phenomena that influence InSb MOSCAPs.

5.2 Architecture of Modelling and Analysis Code

A code suite was built in MATLAB to analyse data from MOS capacitors. The suite included import, conditioning (e.g. removal of data points measured as short/open circuit), modelling/generation of C-V curves and extraction of data such as interface-trapped charge (D_{it}), flatband voltage shift (V_{FB}) and hysteresis voltage (V_H). The block diagram for the suite is shown in figure 5.1, which also shows what types of data are passed between functions and a hierarchical breakdown of components.

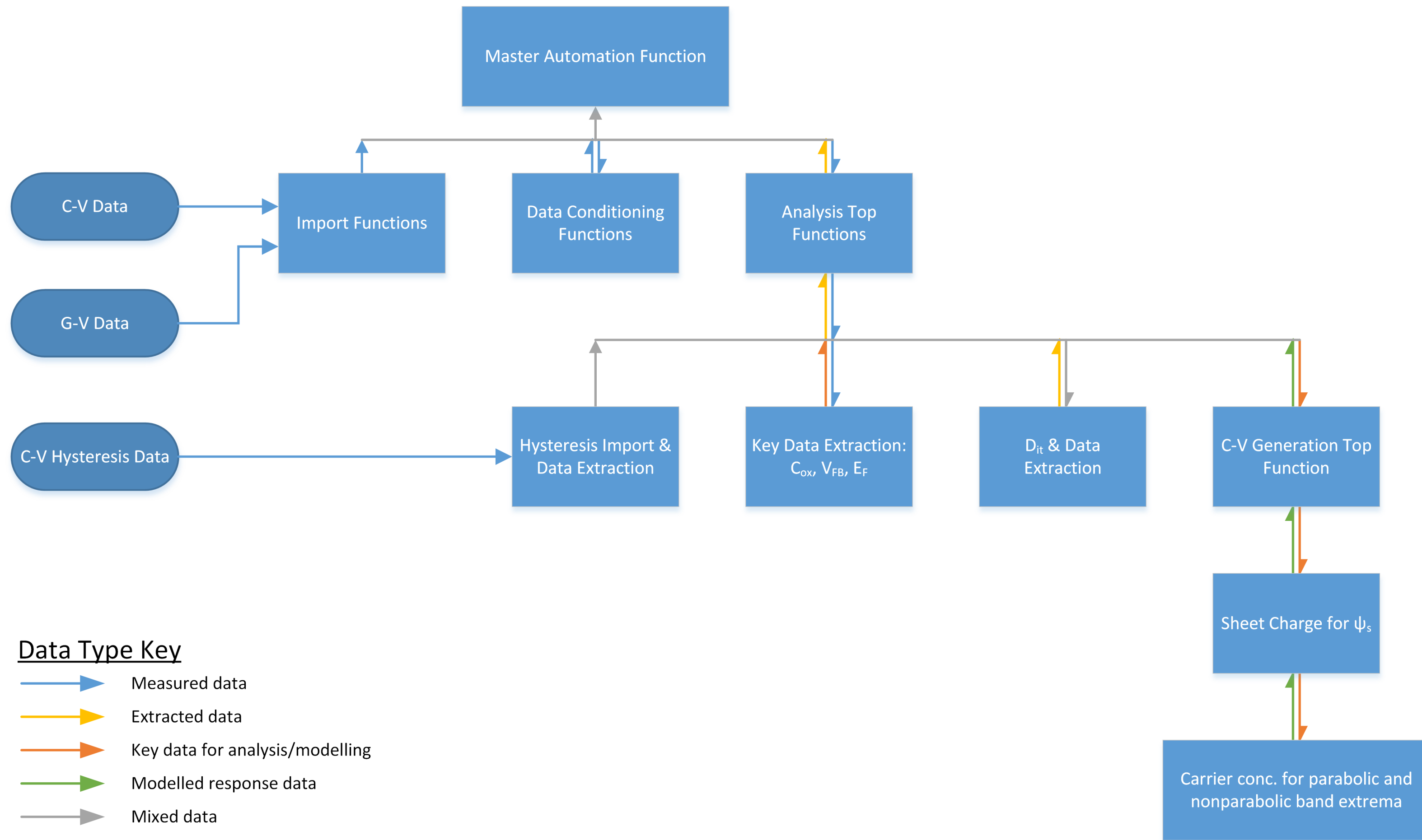


Figure 5.1: Block diagram of modelling and analysis code

The master automation function collates and saves data for each device, generates data plots at each stage of the analysis process and automatically cycles through devices in a batch, allowing many devices to be analysed efficiently. Data is first imported, then conditioned, using the following steps:

- Normalise per unit area
- Discard data at a given frequency if it fails one of the following criteria:
  - The maximum capacitance exceeds 100 µF (characteristic of dielectric breakdown)
  - The minimum capacitance is negative (characteristic of dielectric breakdown and excessive leakage)
  - The peak-to-peak noise in accumulation is greater than 10% of the accumulation capacitance (small capacitors measured at low frequency can display excessive noise)
  - A capacitance maximum occurs which is greater than 150% of the accumulation capacitance (characteristic of dielectric breakdown)
  - The accumulation capacitance for the highest frequency exceeds the accumulation capacitance for the lowest frequency, with a 5% margin (characteristic of a calibration error)
- Identify whether the highest frequency displays only low-frequency inversion response by comparing the accumulation and inversion capacitance to the depletion capacitance (at the centre of the array of values). If both the accumulation and inversion capacitance are higher than the depletion capacitance, truncate the inversion data (thereby enabling an approximate data extraction for poor samples using the same procedure as good samples)

The data is plotted immediately after import and again after conditioning. One plot displays C-V and G-V curves at each measurement frequency and another displays normalised parallel conductance ($\frac{G_P}{\omega}$, discussed in section 4.5) as a surface plot, with voltage and frequency as x and y parameters and $\frac{G_P}{\omega}$ as the z parameter. Analysis and data extraction are performed as described in section 5.2.2, first on the forward voltage sweep, then an attempt is made to import data from the bidirectional measurement and analyse it using the same procedure.

Within this analysis procedure, a C-V response is generated for Terman D_{it} analysis. The model used to generate the C-V response is a 1-dimensional electrostatic model: the equations used are detailed in section 4.4.2 and their implementation is

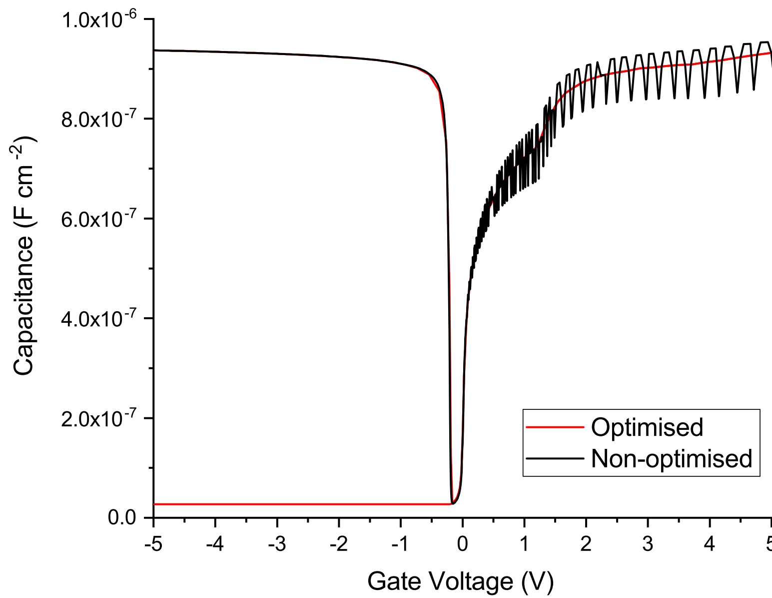


Figure 5.2: MOSCAP C-V response generated using the one-dimensional electrostatic model. Response with optimised integration resolution shown in red, low integration resolution shown in black

detailed in section 5.2.1. This model can also be employed out of context to investigate C-V response and the 'band bending' relationship between bias voltage and surface potential for different oxide capacitance, doping and temperature conditions, as well as different materials and band structures.

Once analysis is complete, plots are generated for D_{it} and band bending and, finally, the key figures of merit are collated into a data array, ready for transfer to the master repository for further analysis.

5.2.1 Modelling Parameters and Optimisation

C-V responses are modelled for devices using the equations from section 4.4.2. In order to generate a full C-V response, the a range of surface potential (ψ_s) values are set for the model. For each ψ_s value, an integral is performed from bulk potential (φ_b) to ψ_s, as described in equation 4.18, using the trapezium rule. The range of ψ_s can be chosen arbitrarily (accommodating different bias conditions and materials), as can the step size of ψ_s and the number of integration steps for the integral from equation 4.18. If the number of integration steps is too low, the modelled C-V response is affected, with a potential-dependant oscillation appearing in the C-V response, as shown in figure 5.2. The source of the oscillation is unclear but, as

Table 5.1: Optimised parameters for 1-dimensional electrostatic model

Parameter	Value
Maximum/minimum ψ_s (eV)	+1.0, -1.0
Number of ψ_s values	100
Number of integration steps (Q_s integral)	2000
Integration step size ($n(\varphi)/p(\varphi)$) (reduced energy units)	1
Integration termination threshold ($n(\varphi)/p(\varphi)$) (cm^{-3})	10^{-3}

increasing the number of integration steps eliminated the oscillation and the model otherwise matched the implementation by Engel-Herbert *et al.* (see section 5.4), the number of integration steps was increased to eliminate the oscillation and no further modifications were performed. After tuning, the optimal number of ψ_s values was 100 and the optimal number of integration steps was 2000.

Within the integral, the total carrier concentration is calculated for each band extremum. This is also calculated using an integral, following equations 4.16 and 4.17 and using the trapezium rule with a tunable step size. Unlike the integration for equation 4.18, however, the integrations for equations 4.16 and 4.17 do not terminate after a predetermined number of steps. Because the incremental carrier concentration decays in magnitude as the potential moves far away from the band edge, the integration is programmed to terminate when the incremental carrier concentration drops below a threshold of 10^{-3} cm^{-3}. This allows the calculation to approximate the infinite limit of the equation without excessive computation time.

The model parameters and optimised values are listed in table 5.1.

5.2.2 Analysis and Key Figures of Merit

Data is extracted from C-V and conductance data. Once the data has been imported and conditioned, key data required for further analysis is extracted: oxide capacitance (C_{ox}), flatband voltage (V_{FB}) and bulk Fermi level. As the dielectric thickness and relative permittivity (dielectric constant) cannot be determined with sufficient accuracy to calculate C_{ox}, it is extracted using the method detailed in section 5.3.2. V_{FB} is then extracted by determining C_{FB} via C-V modelling (as described in sections 4.4.2 and 5.2) and searching the measured response (at high frequency) for a match to this capacitance value (with linear interpolation used to extract a more accurate value). This model also generates a value for bulk Fermi level. The critical figure of merit is interface-trapped charge density (D_{it}) and it is extracted using the Terman, high-low and conductance methods, described in sections 4.3.1 and 4.3.2.

For the Terman method, a modelled C-V response is generated, as described in sections 4.4.2 and 5.2, using the extracted C_{ox} value, as well as the set temperature and the dopant concentration (taken from the wafer conformance certificate or from Hall measurement for epitaxial material, described in section 5.3.1). This modelled response (at high frequency) is then compared to the measured response point-by-point as described in section 4.3.2, with linear interpolation used to ensure a more accurate stretch-out value. The extracted D_{it} values are mapped to energy levels, using the ψ_s values associated with each modelled capacitance point, to give a full D_{it} profile.

The high-low method also required C_{ox} to be known but it additionally requires V_{FB} to enable the integral from equation 4.12 to be used. By applying equations 4.4 and 4.12 to each measured data point, a D_{it} profile is extracted. The high-low method frequently underestimates D_{it} when compared to other methods and is more prone to large disruptions, and so data from the high-low method is not included in the studies presented in this thesis.

For the conductance method, the density of states in the valence and conduction bands are first calculated from materials data and temperature, as well as the thermal velocity of electrons and holes. Trap capture cross-section data is unavailable for InSb - Engel-Herbert *et al.*[23] note that the sensitivity of energy mapping to this parameter is low, ~60 meV per decade at room temperature and lower at cryogenic temperature, and the value they report for InGaAs is taken as an approximation. The magnitude of extracted D_{it} is unaffected. Following calculation of material data, the conductance data is normalised, as subsequent calculations use $\frac{G_P}{\omega}$ rather than G. A 3D plot of $\frac{G}{\omega}$ against voltage and frequency is shown in figure 5.3 for a typical device measured with high resolution in voltage and frequency at 80 K. The characteristic D_{it} 'ridge' feature can be seen in light blue but an additional hillock feature, visible in green/yellow/red, normally appears at extreme negative gate voltage, attributed to slow states and/or leakage. For the purposes of D_{it} extraction, the hillock feature is omitted and the 'ridge' feature isolated by using a 3-dimensional reference feature, generated using exponential functions. MATLAB's 'goodness of fit' function is then used to scan for the region in the $\frac{G}{\omega}$ data that best matches this reference signal and this region is taken for subsequent analysis. Twin iteration loops then scan each frequency for the maximum $\frac{G_P}{\omega}$ value. This peak value is converted to a D_{it} value using equation 4.25 and the energy level associated with it determined using equation 4.28 and the frequency it occurs at. This process is then repeated for all frequencies, generating a D_{it} profile.

In addition to D_{it}, other figures of merit are extracted from measured data. V_{FB}

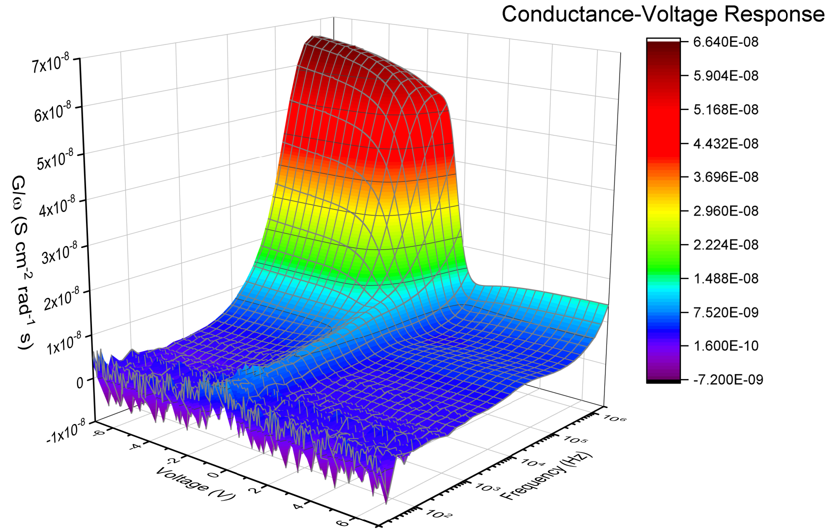


Figure 5.3: 3D surface plot of normalised conductance-voltage-frequency data

is extracted for a forwards-direction sweep of DC voltage (normally from inversion to accumulation, eliminating 'deep depletion' features from residual minority carriers) but an additional reverse-direction sweep is often taken. The flatband voltage extracted from the reverse sweep is often different to the forward sweep, i.e. the response displays hysteresis. Hysteresis voltage (V_H) is extracted at C_{FB} and all the D_{it} and V_{FB} extraction techniques performed on the forward sweep are also attempted on the reverse sweep data. This potentially gives 6 D_{it} profiles, although the standard measurement procedure does not collect enough conductance data when performing the reverse sweep to perform a meaningful conductance D_{it} extraction (as the measurement would become excessively long). Hysteresis effects are assumed to be due to trap states with a long time constant, longer than 1 s, which do not relax to equilibrium until the DC voltage sweep (in one direction) has completed.

Three other 'alternative' figures of merit are included in data extraction and occasionally studied for analysis: capacitance modulation at low frequency, capacitance modulation at high frequency and frequency dispersion in accumulation. These figures of merit are less reliable and/or less well-characterised than D_{it}, V_{FB} and V_H but occasionally offer alternative perspectives or show trends to support other figures of merit. Capacitance modulation at low frequency - i.e. the ratio between maximum and minimum capacitance in the low frequency regime - can be taken as a simplified approximate indicator of D_{it}, following the same principles as the high-low method, described in section 4.3.1. Capacitance modulation at low frequency is occasionally quoted as a figure of merit as a simplified alternative to the

high-low method, and its extraction allows comparison with such data, but for this thesis it is superseded by the D_{it} extracted by the Terman and conductance methods. Capacitance modulation at high frequency can be used as a check for unwanted generation-recombination in the inversion regime, as this would raise the minimum capacitance. Finally, slow 'near interface' trap states are known to cause frequency dispersion in accumulation[54] and this dispersion can be quantified as an average percent per decade as a method of quantifying the influence of slow traps. While these figures of merit are included in data extraction they present several issues: they are normally superseded by other methods or not relevant; they show high sensitivity to noise and extraction uncertainty and low sensitivity to treatments and processes; and, as such, they show correlations with process treatments weakly and/or infrequently. They are mentioned here for completeness but only frequency dispersion is mentioned in this thesis, in chapter 9.

5.3 Extraction of Key Data

In addition to the measured C-V and conductance response, additional data on the samples is required to perform data extraction, analysis and characterisation. Most notably, accurate dopant concentration and oxide capacitance (C_{ox}) values are essential to data extraction. These can be easily extracted from silicon MOSCAP C-V responses but the additional trap states in III-V materials necessitate different methods for extracting these key values[23].

5.3.1 Dopant Concentration

Dopant concentration can, classically, be extracted from C-V responses. The swept DC bias induces a depletion region, which changes thickness (and, consequently, capacitance) at a rate which depends on the dopant concentration: high doping and high ionised charge in the depletion region causes the capacitance to change slowly as a function of voltage and vice versa. Dopant concentration can then be quantified from the derivative of $\frac{1}{C^2}$ with respect to voltage.

However, the classical C-V dopant extraction cannot be used for III-V MOSCAPs. The introduction of a significant amount of trap charge (predominantly D_{it}) affects the slope in depletion and interferes with doping extraction[23]. In order to determine dopant concentration for bulk material, an average value is taken from the wafers' certificates of conformance, which provides doping measurements at seed and tail end. For epitaxially grown material on semi-insulating GaAs substrates, Hall effect measurements were performed.

The Hall measurements were performed on an Ecopia HMS-3000 system using the Van der Pauw method on 1 cm square samples. Ohmic contacts were made using InSn solder and measurements were performed at 77 K by immersion of the samples in liquid nitrogen. As the intrinsic carrier concentration and electron mobility of InSb are both very high (2×10^{16} cm^{-3} and $\sim7\times10^{4}$ cm^{2}V^{-1}s^{-1} respectively, at room temperature), room temperature measurements are unsuitable for dopant characterisation: intrinsic electrons in p-type material dominate the extrinsic holes, preventing the acceptor concentration from being measured. All dopant concentration values listed in this thesis were extracted at 77 K, ensuring that only extrinsic carriers are measured.

5.3.2 Oxide Capacitance

In section 4.4.1, it is observed that, for III-V semiconductors, the low density of states in the Γ valley of the conduction band affects the extraction of oxide capacitance (C_{ox}). In group IV semiconductors and other indirect bandgap semiconductors, the lowest conduction band minimum occurs at a different wavevector to direct bandgap materials and the density of states in these minima is higher[6]. As a consequence, when these materials are driven into strong accumulation in n-type material, the electron concentration is high enough that the structure can be approximated to a parallel plate capacitor (i.e. a metal-insulator-metal structure) and the accumulation capacitance can be used as an accurate approximation of C_{ox}. In III-V materials with a direct bandgap and dominated by the low density of states in the Γ valley - including InSb, $Al_{0.25}In_{0.75}Sb$, InAs and GaAs - other techniques must be used to determine C_{ox}.

A technique for determining C_{ox} independently from C-V measurements is to measure thickness and calculate capacitance from dielectric permittivity values from reference sources. The most accurate and most resource-intensive thickness measurement is high resolution transmission electron microscopy (TEM), which requires specialist training to operate and lengthy sample preparation. A less accurate and more easily-performed technique is ellipsometry, where elliptically polarised light is beamed onto the sample and the change in polarisation measured at the detector. A model can then be constructed, accounting for the dielectric and reflective properties of the underlying substrate and additional layers, and fitted to produce a value for layer thickness. Some ellipsometers are capable of only a single wavelength measurements, whereas spectroscopic ellipsometers are capable of multiple-wavelength measurements. A similar technique is interferometry, also based on fitting of optical data but instead fitting to an optical or UV interferogram.

The ALD suite at the University of Liverpool, used for many samples in this project, is equipped with a spectroscopic ellipsometer. A standard thickness measurement procedure is used for all deposition runs: a silicon 'witness' piece was measured before deposition, given the same deposition process as the InSb samples and was measured again after deposition, using the first measurement as a reference substrate. The silicon-Al_2O_3 system is well-characterised and easy to model accurately, allowing an accurate measurement of film thickness for the 'witness' sample, whereas non-silicon substrates are difficult to model accurately and thickness values cannot be quoted with good accuracy. The facility at the University of Warwick is equipped with a Filmetrics interferometer and a similar procedure was used, with similar limitations.

When ellipsometry thickness measurements and a dielectric constant of 9.1 for alumina were used to calculate the C_{ox}, the resulting values were significantly higher than the accumulation capacitance (C_{acc}) measured in accumulation. As an example, a 20 nm thick layer of Al_2O_3 - measured by ellipsometry and with an added porosity of 5% - was calculated to give a C_{ox} of 1.95×10^{-9} F for a device with a measured C_{acc} of 1.40×10^{-9} F. The one-dimensional electrostatic model indicates that, for an InSb MOSCAP in strong accumulation, the accumulation capacitance should be ~98.8% of C_{ox}, suggesting that C_{ox} cannot be reliably calculated. This may be due to inaccuracies in the ellipsometry measurement or fitting, the dielectric constant of the Al_2O_3 being low (potentially due to doping/impurities) and/or a higher degree of porosity in the film (potentially due to poor nucleation of ALD deposition).

An alternative technique has, therefore, been developed, based on the one-dimensional electrostatic model. The measured C_{acc} is taken as a first approximation of C_{ox}. Using this approximation, the model is used to generate a modelled response and, from this, a predicted discrepancy between C_{acc} and C_{ox} is determined (~98.8%, as mentioned above). This predicted discrepancy is then taken as a correction factor to calculate a revised estimate of C_{ox}. This method has not been demonstrated previously and is used throughout this thesis for data extraction and calculation.

5.4 Verification Against Literature Data

To provide confidence in the one-dimensional electrostatic model, its implementation and its parametrisation, its performance was verified against literature data. To verify the implementation of the model, charge and capacitance plots from Engel-Herbert *et al.*[23] were traced, replicated in the model and the model data compared

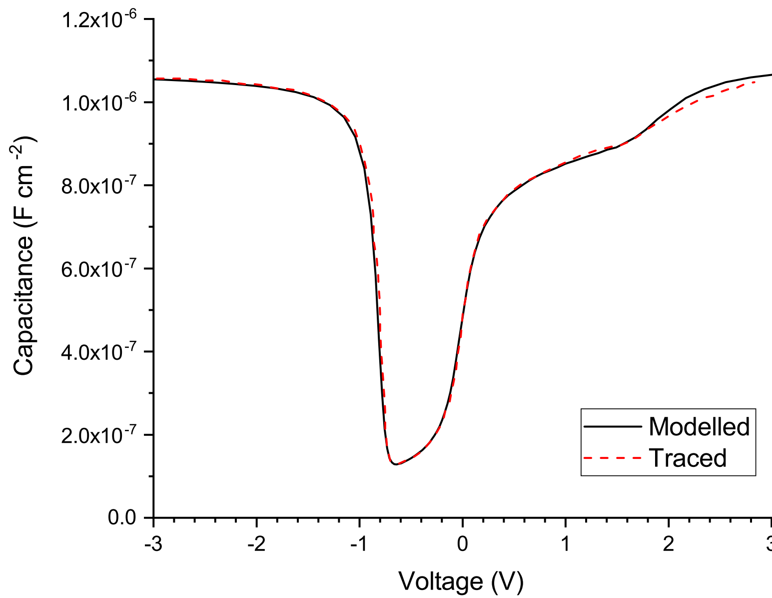


Figure 5.4: Modelled C-V response for $In_{0.53}Ga_{0.47}As$ MOSCAP. Solid: modelled using the one-dimensional electrostatic model, dashed: traced from Engel-Herbert *et al.*

to the traced data. To verify the parametrisation, Moss-Burstein shift data was extracted from Zawadzki[104] and compared to charge-potential data from the model.

5.4.1 C-V Curve for InGaAs

The capacitance and charge plots from Engel-Herbert *et al.* were traced from the paper using an open-source MATLAB script, producing a numerical data array. The one-dimensional electrostatic model was then parametrised for $In_{0.53}Ga_{0.47}As$, capacitance and charge data was generated using the model and overlaid against the traced data - the results are shown in figures 5.4 and 5.5.

5.4.2 Carrier Concentration for InSb

The band structure of a semiconductor can be inferred from the shift in apparent bandgap as the dopant concentration is changed: high donor concentrations will fill the bottom of the conduction band (acceptors will empty the top of the valence band), resulting in a higher optical transition energy as electrons can only fill higher-energy states. This phenomenon - Moss-Burstein shift - is used here to infer the band structure (specifically, density of states as a function of energy) as verification for the one-dimensional electrostatic model and the parameters from chapter 4.

The Moss-Burstein shift data was extracted from Zawadski[104]: carrier con-

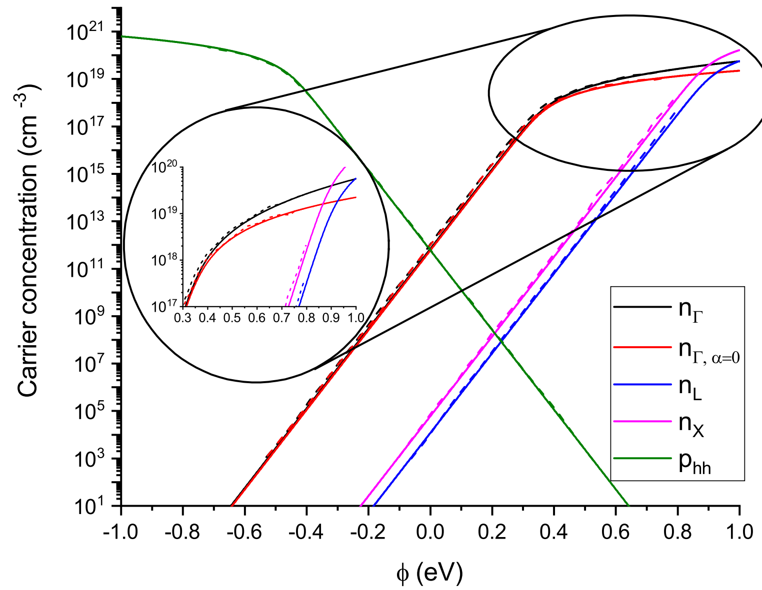


Figure 5.5: Carrier concentration in each band minimum/maximum of $In_{0.53}Ga_{0.47}As$ as a function of electrostatic potential. Solid: modelled using the one-dimensional electrostatic model, dashed: traced from Engel-Herbert *et al.*

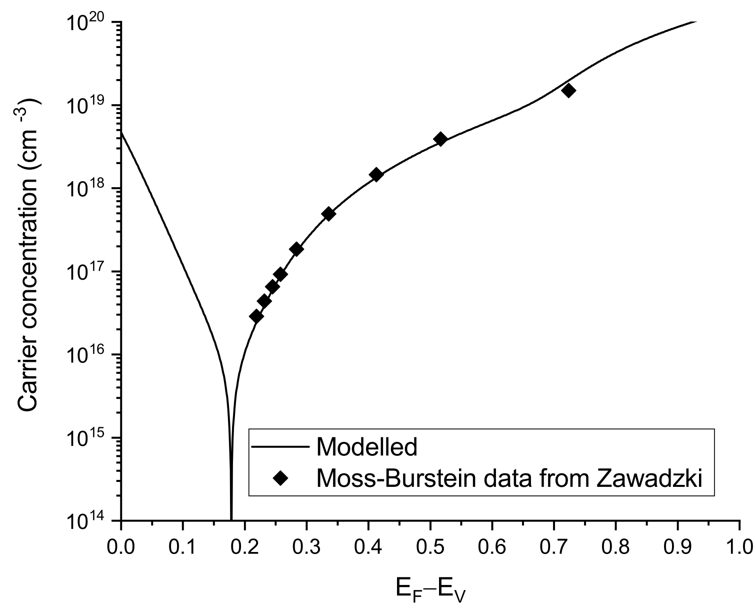


Figure 5.6: Moss-Burstein shift (symbols) and modelled (line) data for carrier concentration vs. Fermi level

centration as a function of Fermi level extracted from the x-axis scales in Zawadzki figure 2. The same data was generated from the one-dimensional electrostatic model and the two datasets are shown in figure 5.6. The fit is excellent at low Fermi level positions and still very good at higher energy, although data for very high Fermi level positions is not available. The data confirms that the model has been parametrised correctly (in particular, the nonparabolicity factor, α=4.1, which is not widely reported or verified in the literature) and that the model tracks practical data accurately.

An alternative method for modelling nonparabolicity is to generate a more extensive band structure model using e.g. multiband $\mathbf{k} \cdot \mathbf{P}$ models and empirical tight-binding models. When correctly parameterised, these models can give more reliable band structure and charge modelling but are more difficult to implement and can be challenging to parameterise for lesser-studied materials such as InSb. The nonparabolicity factor model is derived from multiband $\mathbf{k} \cdot \mathbf{P}$ modelling[112] and has been applied extensively to calculation of charge carrier concentration in III-V materials[113][102][23]. Given its widespread use and successful verification against literature data, the nonparabolicity model with α=4.1 is used throughout this thesis.

5.5 Typical Features of Electrical Characterisation

Detailed data and plots from a typical MOSCAP are shown below. The MOSCAP was fabricated using $\sim 1\times 10^{14}$ cm^{-3} n-type bulk InSb, a wet chemical clean using dilute hydrochloric acid, atomic layer deposition Al_2O_3 and aluminium metal, as detailed in section 6.3. The characterisation was performed at 80 K using a Leybold RDK 10-320 cryostat and an Agilent E4980A LCR meter.

The measured capacitance-voltage response is shown in figure 5.7. The accumulation response is consistent with other III-V MOSCAPS, such as those shown by Veksler *et al.*[95], Engel-Herbert *et al.*[23], Suzuki *et al.*[40], Trinh *et al.*[38] and Koh *et al.*[79] - the capacitance increases as the voltage increases, without plateauing, but frequency dispersion is observed. In inversion, significant deviation is observed from both classical Si response and typical III-V response:

- In strong inversion, capacitance rises to $\sim C_{ox}$ at low frequency and decreases to a uniform minimum at high frequency. For some devices, 'low frequency' high capacitance response is not observed.

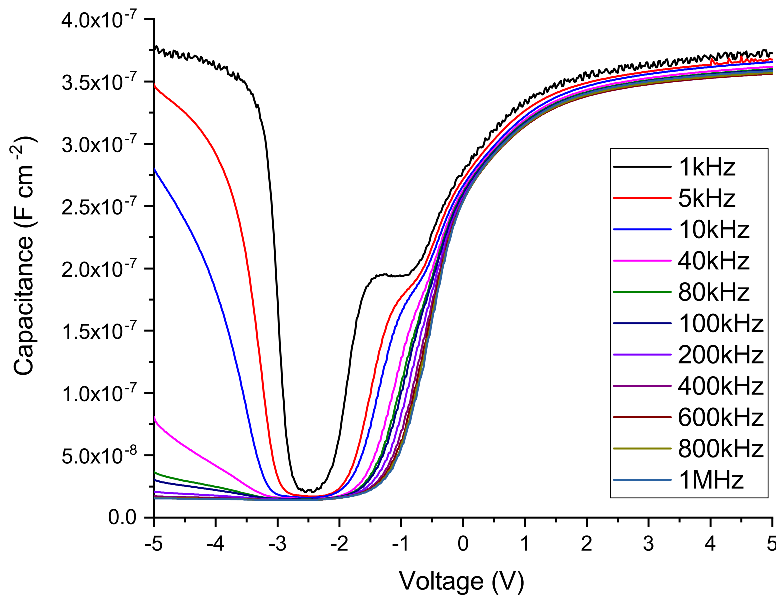


Figure 5.7: Typical capacitance-voltage response of Al_2O_3-InSb MOSCAP

- In weak inversion, capacitance continuously decreases for high frequency but increases at low frequency, suggesting either the onset of inversion or an interface trap 'hump' feature
- In moderate inversion, capacitance drops to the minimum level for all frequencies

This behaviour is attributed to a combination of a typical III-V 'hump' feature (e.g. Engel-Herbert *et al.*[23], Suzuki *et al.*[40]) and high-field effects discussed below in section 5.6. Specifically, impact ionisation is predicted to occur to a limited degree even for low doping, such as used for the device in figure 5.7, suggesting that the high capacitance low frequency behaviour shown in figure 5.7 may be stimulated by impact ionisation. As such, the uniform drop to minimum capacitance in moderate inversion can be classified as typical 'high frequency' response, exaggerated by cooling to 80 K.

The 'hump' feature is commonly seen in III-V MOSCAP response. An example is shown in figure 5.8 for a HfO_2-$In_{0.53}Ga_{0.47}As$ MOSCAP[23]. Although this feature is occasionally attributed to minority carrier ('true' or 'weak' inversion) response, it is more likely due to interface-trapped charge (potentially high midgap D_{it}), due to its dependence on gate voltage and treatment, and due to the magnitude of the effect. The feature is discussed in further detail by Engel-Herbert *et al.*[23] in section III.

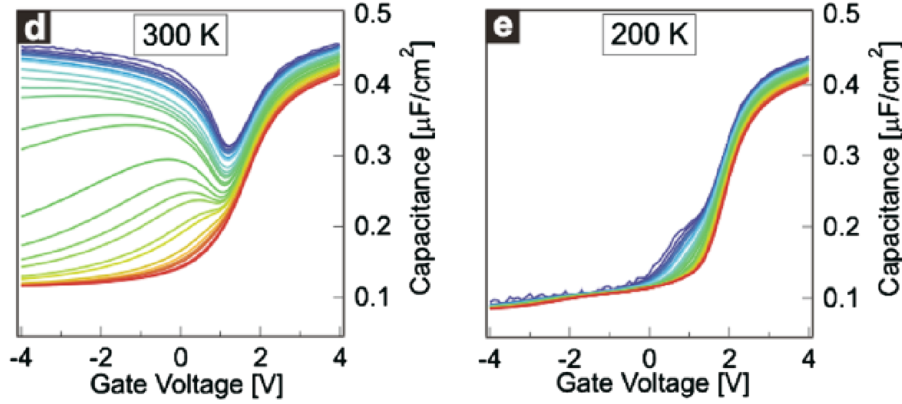


Figure 5.8: Frequency-dependent CV characteristics measured at 300 K and 200 K for MOSCAPs with HfO_2 on n-type $In_{0.53}Ga_{0.47}As$. The HfO_2 lm was about 30 nm thick and was annealed in nitrogen after deposition.. Reproduced from Engel-Herbert *et al.*[23], with the permission of AIP Publishing

The measured conductance-voltage response of the same MOSCAP is shown in figure 5.9. As figure 5.9 is dominated by high-frequency response, the $\frac{G_P}{\omega}$-voltage response is shown in figure 5.10 and a 3-dimensional surface plot of $\frac{G_P}{\omega}$-voltage-frequency response is shown in figure 5.11. The D_{it}-induced 'peak' features are prominently visible, and its response to both frequency and voltage is highlighted in figure 5.10. An additional feature is visible at large negative voltage, particularly in figure 5.10, and is attributed to high-field effects (impact ionisation and possibly Zener tunnelling), as discussed above for C-V response and in section 5.6 in additional detail.

The extracted D_{it} for the same device is shown in figure 5.12. The high-low method gives an approximately flat C_{it} profile with energy and, although not shown here, frequently reports minimum D_{it} more than an order of magnitude below the other methods. In addition to the limitation, discussed in sections 2.6 and 4.3.1, that the minimum and maximum frequencies must include AC response from all an none of the interface traps, respectively, the high-low method is influenced by frequency dispersion in accumulation. An additional capacitance offset will be captured by equation 4.4 as D_{it}, resulting in further deviation from the 'true' D_{it} profile. Due to all these effects, the high-low method is deemed unreliable for D_{it} extraction and results from the method are not discussed further in this thesis.

The conductance method covers only a small region close to the majority carrier band edge. It shows decreasing D_{it} closer to the band edge, consistent with the conductance-voltage-frequency response shown in figure 5.11, which shows peak $\frac{G}{\omega}$ decreasing as frequency increases and the response approaches the band edge. The

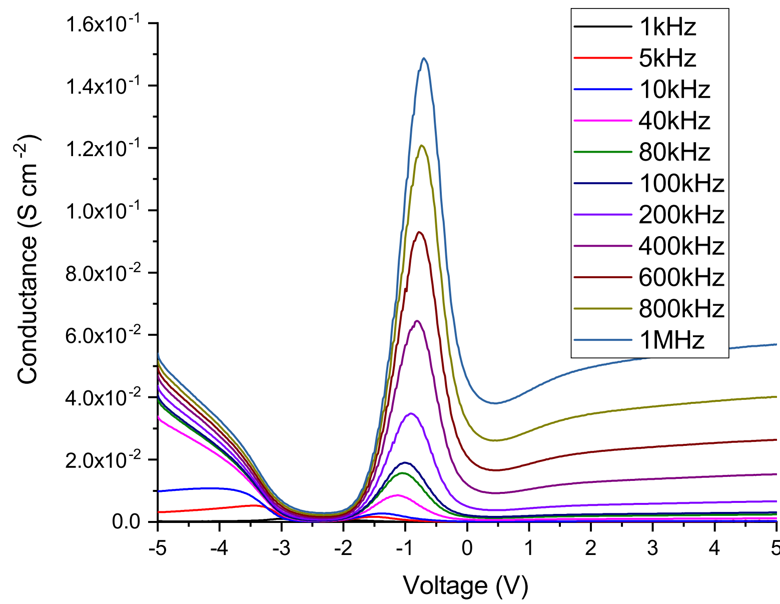


Figure 5.9: Typical conductance-voltage response of Al_2O_3-InSb MOSCAP

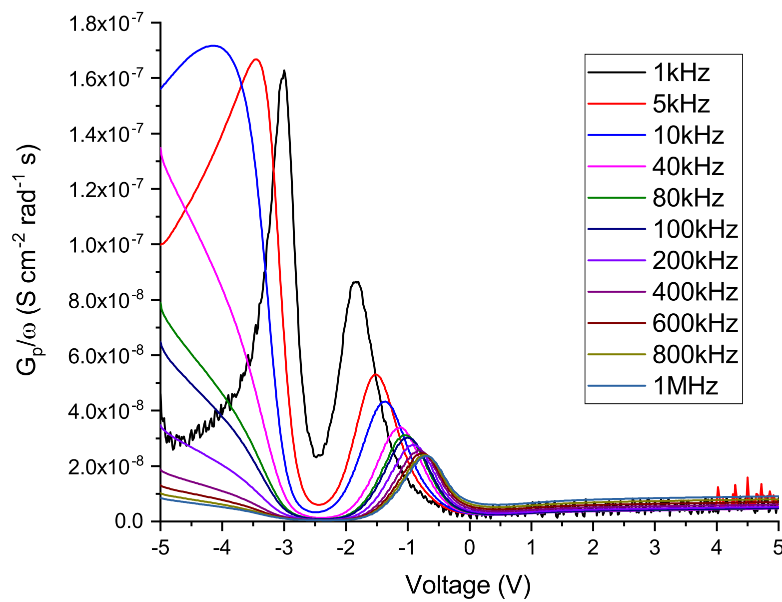


Figure 5.10: Typical $\frac{G_P}{\omega}$-voltage response of Al_2O_3-InSb MOSCAP

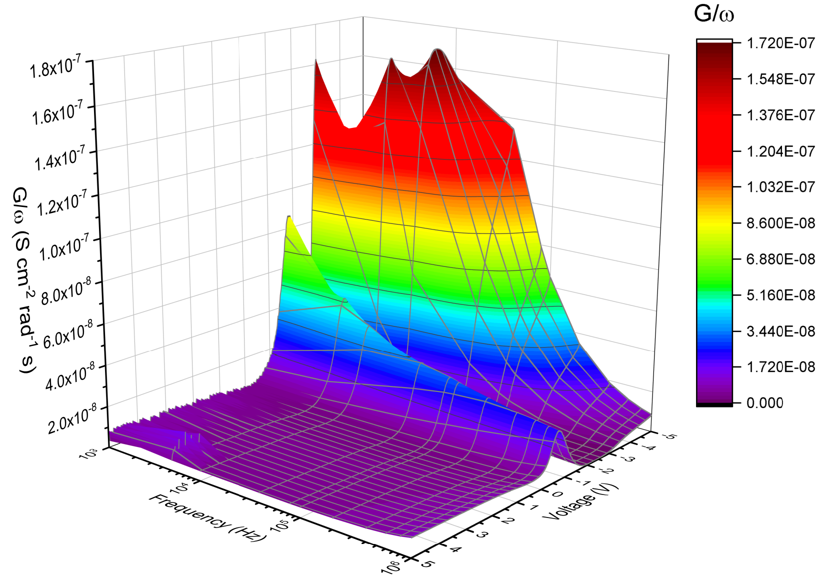


Figure 5.11: Typical $\frac{G}{\omega}$-voltage-frequency response of Al_2O_3-InSb MOSCAP as a 3D surface plot. Note the change in X and Y axes compared to figure 5.3

D_{it} profile shows a small upturn for the last point, not present in the $\frac{G}{\omega}$ response - this is due to the extraction process for equivalent parallel conductance, shown in equation 4.26, exaggerating leakage features at low frequency, defeating the method of isolating the 'ridge' feature described in section 5.2.2. This artefact impacts minimally on the extracted minimum D_{it} and the conductance method can otherwise be considered reliable over the energy range it covers.

The Terman method gives approximately the same minimum D_{it} as the conductance method but with a small energy displacement of ~100 meV. This may be due to model inaccuracy, AC effects from interface traps due to the measurements frequency not being sufficiently high, underestimation of C_{ox} or effects from 'slow' traps (e.g. additional stretch-out). As the Fermi level approaches the valence band, the apparent Terman D_{it} increases by two orders of magnitude but this effect may not be a genuine effect of D_{it}. As discussed in section 5.2.2, additional generation-recombination can raise the minimum capacitance in high frequency inversion above the theoretical minimum (see figure 4.8). As the Terman method is predicated on the lateral stretch-out, the shallow gradient of the measured high-frequency inversion response is interpreted as a steep increase in interpreted D_{it}. The D_{it} near the conduction band edge can be more effectively characterised using p-type material.

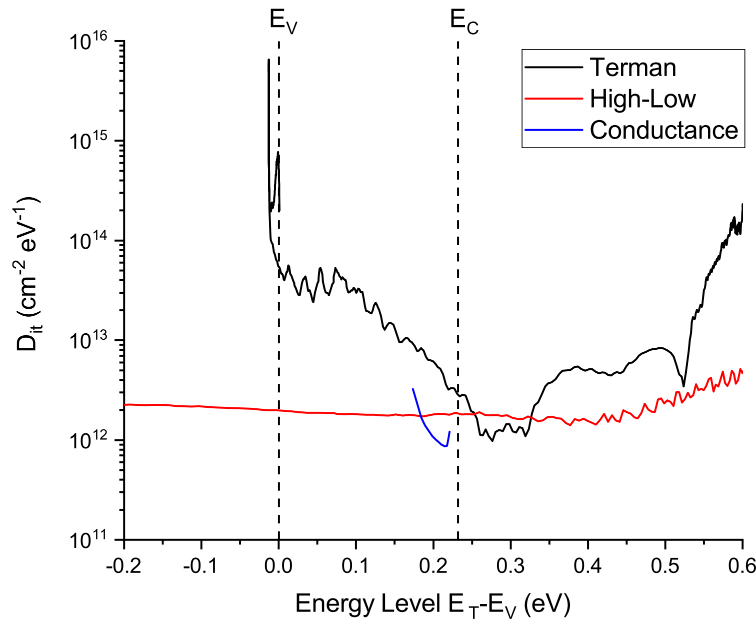


Figure 5.12: Typical D_{it} profile of Al_2O_3-InSb MOSCAP

5.6 High-Field Narrow Bandgap Effects

Due to the exceptionally narrow bandgap of InSb, phenomena typically associated with high voltages and electric fields can occur under relatively normal conditions, rendering devices unusable. Two such phenomena - band-to-band Zener tunnelling and impact ionisation - have been investigated with modelling techniques and are discussed below. In addition, very strong band bending, particularly given the low density of states in III-V materials, has been reported in the literature to cause quantisation and changes in device/structure response[110][114] and, as such, additional modelling has been undertaken to investigate its influence in InSb MOSCAPs in the accumulation regime, where the C_{ox} extraction technique of section 5.3.2 is performed.

It is important to note, within this section, the comparison between low-doped epi and bulk material (undoped n-type, n<10^{15} cm^{-3}) and medium-high-doped epi material (Te-doped, n≈10^{17} cm^{-3}). Figure 5.13 shows C-V responses from 3 samples with different material preparation - both epi materials were grown on InSb substrates to eliminate lattice mismatch and minimise material defects. Both low-doped materials perform similarly, regardless of preparation technique, but the higher-doped epi material shows high capacitance in inversion at all frequencies. This indicates that a larger quantity of charge is being modulated by the AC probe signal and implies that the G-R rate has been increased.

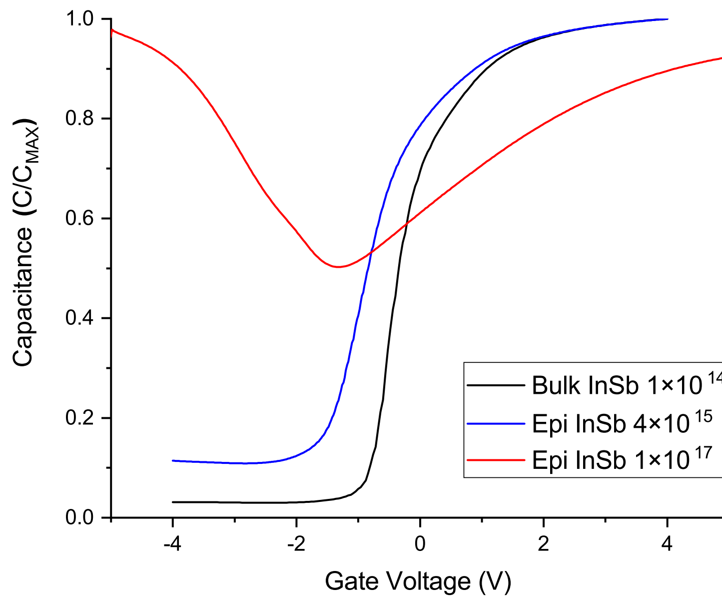


Figure 5.13: C-V responses from epi and bulk material with different dopant concentrations

5.6.1 Zener Tunnelling

The states that electrons occupy are wavefunctions, with a probability of an electron occupying the state at a given spatial position. This probability function extends beyond the classical position of the state/band but decays rapidly - under normal conditions, the classical position is a good approximation. Under high bias conditions, however, the conduction and valence bands bend sharply enough that the spatial separation between equipotential points in the conduction and valence bands becomes very small, as shown in figure 5.14. This separation is small enough that a wavefunction in the conduction band extends into the valence band with a sufficiently high probability that electrons become able to tunnel from the conduction band to the valence band. The reverse is true for wavefunctions in the valence bands and this process is known as band-to-band tunnelling or Zener tunnelling. A consequence of this process is an apparent rise in generation-recombination (G-R) rate, as the tunnel current through the depletion region will allow the carrier concentration at the surface to change more rapidly than through bulk G-R alone.

The band profile in figure 5.14 is generated using equations 5.1 and 5.2, following Pierret[13] and Sze[12] for a MOSCAP in strong inversion. In equations 5.1 and 5.2, W is the depletion layer width, κ_{semi} is the relative permittivity (dielectric constant) of the semiconductor, ϵ_0 is the permittivity of free space, E_F is the Fermi level, q is

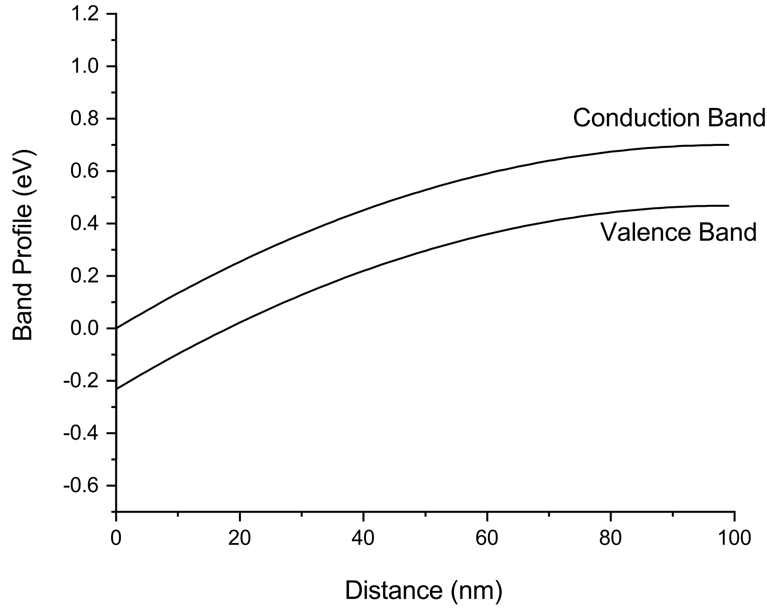


Figure 5.14: Band profile of p-MOSCAP in strong inversion

the electron charge, N is the majority carrier dopant concentration, φ is the electrical potential (i.e. the instantaneous band bending) and x is the distance from the interface (the independent variable). The surface potential for strong inversion, ψ_s, and the Fermi level, E_F, are determined using the 1-dimensional electrostatic model, with C_{ox} and dopant concentration input parameters matching fabricated devices and the surface potential taken at the highest V_G the MOSCAP could sustain.

$$W = \sqrt{\frac{4\kappa_{semi}\epsilon_0 E_F}{qN}} \tag{5.1}$$

$$\varphi = \psi_s \left(1 - \frac{x}{W}\right)^2 \tag{5.2}$$

In order to investigate the Zener tunnelling phenomenon, the minimum distance between the conduction and valence bands at the same potential (i.e. the distance between the lowest point of the conduction band and the edge of the valence band at the same potential) is extracted. The total depletion width is dependant on dopant concentration and, as the bands bend as an exponential function between surface and bulk, the minimum distance between bands is also dependant on dopant concentration. This relationship is shown in figure 5.15.

In order to make a quantitative judgement on the critical dopant concentration

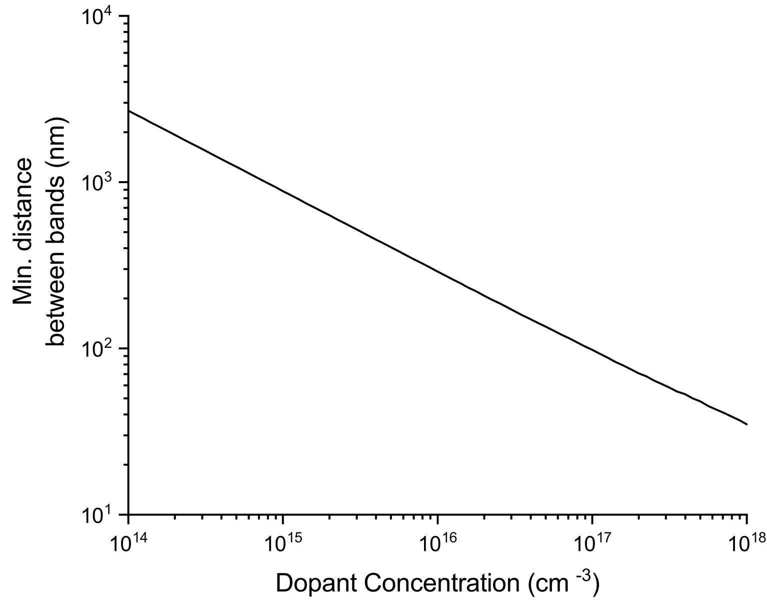


Figure 5.15: Dependency between dopant concentration and minimum distance between bands

for Zener tunnelling, the de Broglie wavelength was taken as an approximation for the minimum distance before significant tunnelling occurs. The de Broglie wavelength is given by equation 5.3.

$$\lambda = \frac{h}{m^* v_{th}} \tag{5.3}$$

In equation 5.3, h is Planck's constant, m^* is the absolute effective mass and v_{th} is the thermal velocity, taken from Levinshtein *et al.*[6]. The de Broglie wavelength of carriers is influenced by their effective mass and thermal velocity and, as such, electrons and holes have different de Broglie wavelengths: 104 nm for electrons at the conduction band edge and 19 nm for holes at the valence band edge. The worst-case scenario is assumed, where tunnelling is limited solely by the properties of electrons at the edge of the conduction band. In such a scenario, the carrier concentration at which tunnelling becomes significant is approximately 10^{17} cm^{-3}.

This simple model supports the observations of figure 5.13: below a dopant concentration of 10^{16} cm^{-3}, tunnel current (and implied G-R rate) should be lower than bulk G-R processes, whereas at 10^{17} cm^{-3} the tunnel current is higher and will contribute to the perceived G-R, raising the measured capacitance.

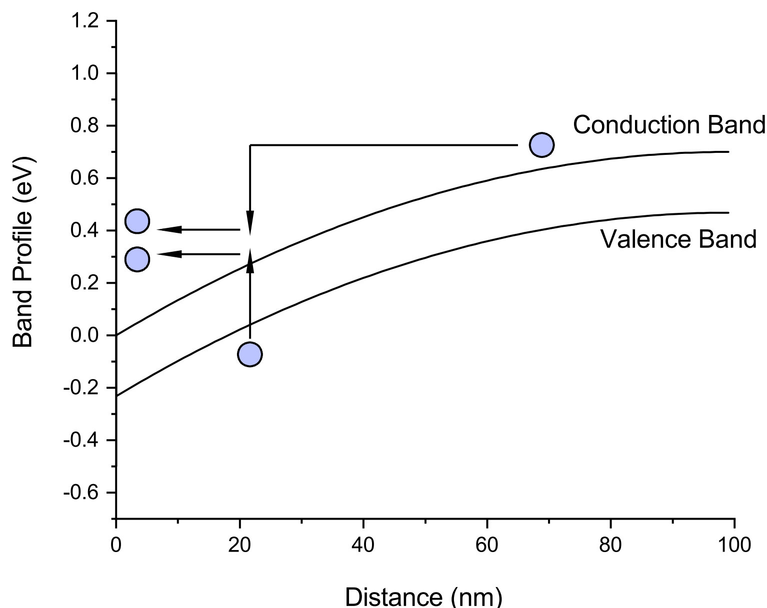


Figure 5.16: Band profile of p-MOSCAP in strong inversion with illustration of impact ionisation process

5.6.2 Impact Ionisation

Another phenomenon which occurs in all semiconductors at high electric fields but which is exaggerated for narrow bandgap materials is impact ionisation. Impact ionisation can is an electric field-stimulated generation process and is responsible for avalanche breakdown: when an incident carrier (an electron or hole) has sufficient energy, it is capable of dropping to a lower state and transferring its excess energy to an additional electron, promoting it to the conduction band and leaving an additional hole in the valence band. This is shown diagrammatically in figure 5.16.

Impact ionisation has the same practical effect as Zener tunnelling: increasing the population of electrons/holes in the inversion layer - in this case more directly through increased generation of carriers - and subsequent measured capacitance. The rate of generation through impact ionisation is dependant on the electric field in the semiconductor, which is in turn dependant on the thickness of the depletion region, as all the potential difference in the semiconductor is assumed to be dropped in the depletion region.

The potential difference in the semiconductor is calculated using the one-dimensional electrostatic model. Input parameters C_{ox} and dopant concentration were matched to fabricated devices, as in section 5.6.1 and the surface potential extracted for the

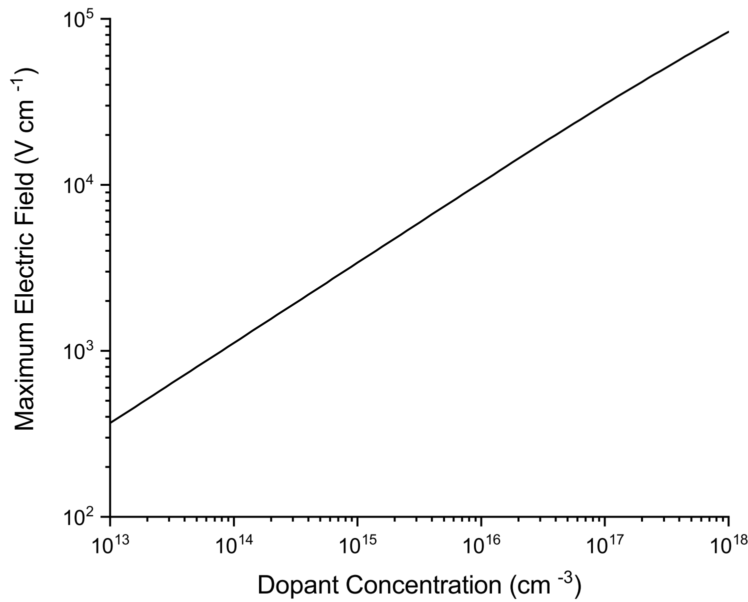


Figure 5.17: Dependency between dopant concentration and electric field in the depletion region

maximum applied voltage (5 V). The potential dropped in the semiconductor was determined to be 0.3 V. The depletion region thickness was then calculated using equation 5.1 and the electric field in the semiconductor quantified. This process was then repeated for different dopant concentrations, as the depletion region thickness is dependant on the dopant concentration. The resultant profile of maximum electric field as a function of dopant concentration is shown in figure 5.17.

To contextualise the data in figure 5.17, the critical electric field of InSb is approximately 10^3 Vcm^{-1}[6]. The electric field in the MOSCAP is only below this potential for very low dopant concentrations - below 10^{14} cm^{-3} - but the small thickness of the depletion width, where the potential is dropped, prevents generated carriers from multiplying to avalanche conditions. This extends the non-breakdown regime beyond the very low dopant concentrations and is consistent with the observations in figure 5.13, where typical behaviour is observed up to a dopant concentration of 10^{16} cm^{-3}.

5.6.3 Quantum Capacitance

For extreme band bending scenarios, the classical model for the conduction and valence bands - a continuum of states - no longer holds. Near the oxide-semiconductor interface, where the bands bend most steeply, a triangular potential well is formed

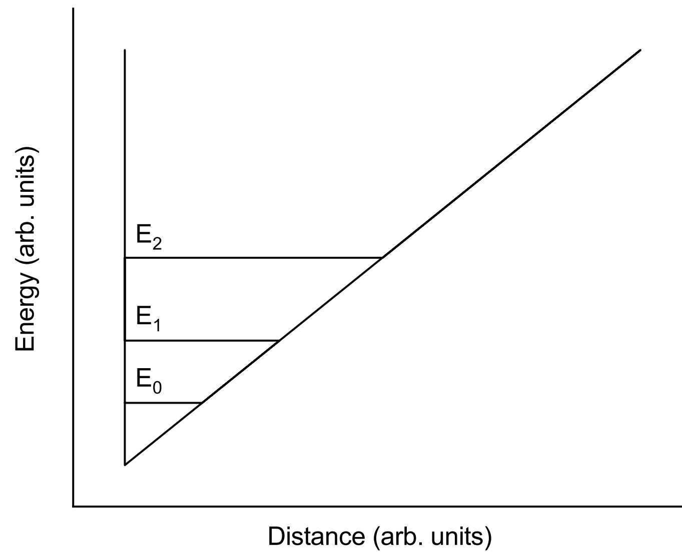


Figure 5.18: Diagram of generic triangular potential well, including three quantised states

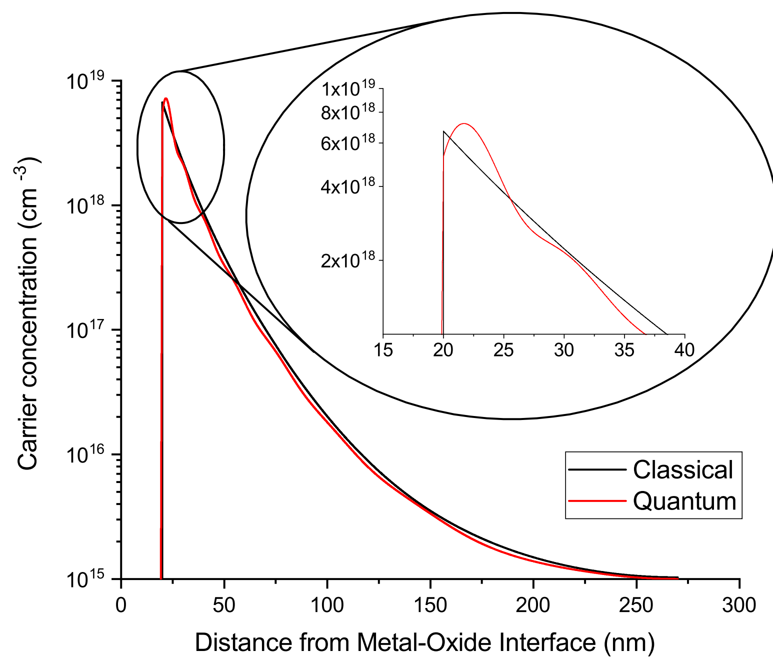


Figure 5.19: Typical profile of carrier concentration vs. depth for InSb MOSCAP in strong accumulation. Inset: enlarged view of region with greatest discrepancy

that contains quantised states rather than a continuum, illustrated in figure 5.18. The effect of this phenomenon is to artificially lower the charge modulation compared to the classical model: the states nearest the interface, which couple strongly with the potential changes in the metal and can be most easily modulated, have a lower population than expected and charge modulation is instead dominated by states deeper in the semiconductor which do not couple as strongly and overall charge modulation is lower as a result. This can also be conceptualised as shown in figure 5.19: in the classical model, the maximum carrier concentration occurs at the interface but, in the quantum model, the maximum carrier concentration occurs a short distance away from the interface, due to the limited states available for the carriers to occupy. This influence on capacitance is known as quantum capacitance.

This phenomenon is important to characterise because the oxide capacitance extraction technique described in section 5.3.2 relies on strong band bending in accumulation and if the classical model is no longer applicable then C_{ox} will be underestimated and data extraction will be influenced. In order to characterise quantisation behaviour in InSb MOSCAPs, a freeware Schrödinger-Poisson solver, developed by Prof. Gregory Snider[115], was used. The model was parameterised for InSb as far as possible, using bandgap and effective mass parameters as outlined in chapter 4, but the model was only capable of modelling a single conduction band minimum using a parabolic band model - this was judged to be sufficient for the assessment of the potential impact of quantum capacitance, as it will provide an overestimate when compared to the non-parabolic band model. A first approximation for surface potential in the accumulation case was determined using the one-dimensional electrostatic model but, as this first approximation resulted in high carrier concentrations in the oxide, this was refined empirically until carrier concentration in the oxide dropped to negligible levels. The dopant ionisation module included in the package was overridden and the structure was assumed to be fully ionised.

Figure 5.20 shows the quantised states in an n-type InSb MOSCAP in accumulation and figure 5.19 shows the electron concentration as a function of distance from the metal-oxide interface. The introduction of quantised states to the model causes the peak carrier concentration to shift approximately 2 nm from the oxide-semiconductor interface. Modelling this as an entirely depleted region (an ideal capacitor, as a worst-case estimate) in series with the oxide capacitance produces a deviation of 14% for a C_{ox} of $1\,\mu\mathrm{F\,cm^{-2}}$ (i.e. a total capacitance of 8.76×10^{-7} F cm^{-2}). This is, according to Engel-Herbert *et al.*[23], is may be significant and further refinement of the C_{ox} extraction method may be necessary.

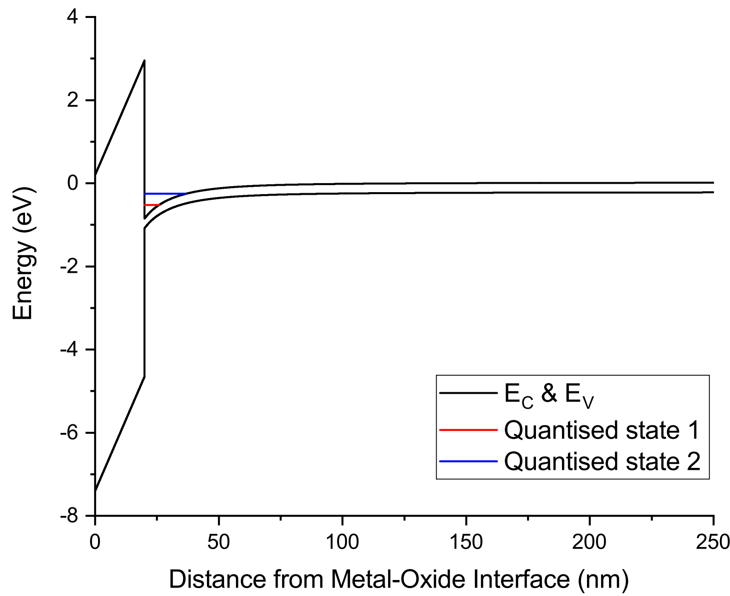


Figure 5.20: Band structure of typical InSb MOSCAP in strong accumulation, with the energy levels of the two lowest quantised states shown in red and blue

5.7 Conclusion

Standard modelling and analysis techniques have been extended and supplemented for InSb. A detailed electrostatic model has been built, parametrised and verified for InSb which, combined with analysis code, is capable of extracting key figures of merit from MOS capacitors. Electrical measurements have been supplemented by Hall effect measurements and a revised oxide capacitance extraction technique to ensure reliable data has been developed for analysis.

Modelling has also been used to investigate the occurrence of high electric field phenomena in InSb at moderate electric fields, due to its narrow bandgap. Zener tunnelling and impact ionisation cause standard response features to break down at moderate dopant concentrations, between 10^{16} and 10^{17} cm^{-3}, limiting the range of dopant concentration which can be tolerated for MOSCAP characterisation. Quantisation of conduction band states is also expected to occur at high electric fields and additional work on data extraction techniques may be necessary to accommodate this effect.

Chapter 6

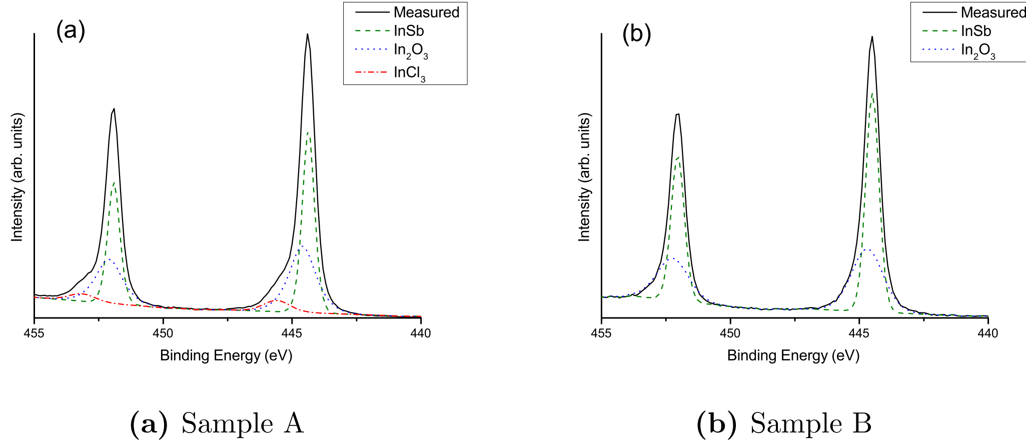
Pre-Deposition Treatments

6.1 Introduction

As discussed in chapter 2, pre-deposition treatment is critical to the preparation of high-quality dielectric-III-V interfaces. Wet treatments, gas treatments and plasma treatments have been used to clean III-V surfaces prior to dielectric deposition, but the applicability of these processes on InSb is under-reported. This chapter explores promising wet chemical and plasma treatments to ascertain their benefit to dielectric-InSb interfaces and their nuances.

6.2 XPS of HCl-Cleaned Surfaces

Literature on surface cleaning of InSb is sparse, though some notable results have been presented on vacuum cleaning processes in the context of surface science research and on fabricated metal-oxide-semiconductor capacitor (MOSCAP) structures. Tereschenko *et al.*[65] cleaned InSb surfaces in an inert dry nitrogen atmosphere using a solution of HCl diluted in isopropanol (IPA). When these samples were studied using X-ray photoelectron spectroscopy (XPS), a surface layer of indium chloride ($InCl_3$) was observed. This presents the possibility of using HCl wet cleaning and chlorine-based interfacial layers for surface passivation but does not account for oxidation and possible displacement of chlorine in oxygen-containing solutions and atmospheres. Furthermore, when annealed at 230°C, the layer was observed to have desorbed from the surface, presenting further questions about the stability of chloride interfacial layers under dielectric deposition conditions. Trinh *et al.*[34] fabricated metal-oxide-semiconductor capacitors (MOSCAPs) using InSb substrates, HCl cleaning, atomic layer deposition (ALD) of aluminium oxide (Al_2O_3) and Ni/Au metal and performed capacitance-voltage (C-V) measurements for char-



(a) Sample A **(b)** Sample B

Figure 6.1: XPS data for the In 3d region of (a) sample A and (b) sample B. The measured data is shown in black, the fitted components for In-Sb, In-O and In-Cl are shown in green, blue and red, respectively

Table 6.1: Breakdown of the atomic percentages in each observed bonding environment from the as-loaded surfaces of Samples A and B. Values accurate to ±2%.

Sample	Sample A	Sample A	Sample B	Sample B
Component	In $3d_{5/2}$ binding energy (eV)	% of In $3d_{5/2}$ region	In $3d_{5/2}$ binding energy (eV)	% of In $3d_{5/2}$ region
InSb	444.37	51.2	444.49	59.3
In_2O_3	444.60	42.1	444.67	40.7
$InCl_3$	445.60	6.7	N/A	<1

acterisation. Critically, when the ALD process temperature changed from 200°C to 250°C, a small change in flatband voltage was observed which, when accounting for the observations by Tereschenko *et al.*, suggests that residual interfacial chlorine may be influencing the electrical characteristics of devices. This behaviour is of particular interest due to the uptake of HCl wet treatments in place of sulphidation treatments,[62][80][48][79] necessitating a more complete understanding of how HCl wet treatments influence surfaces and dielectric interfaces. As such, a study has been performed to investigate the role of $InCl_3$ on InSb MOSCAPs, to ascertain whether an $InCl_3$ layer forms under normal processing conditions; how quickly it desorbs as the temperature rises through the ALD process temperature window (150°C to 300°C) and how the MOSCAP electrical behaviour changes as the $InCl_3$ layer is introduced and desorbed.

An XPS study was first performed to investigate the formation and change of

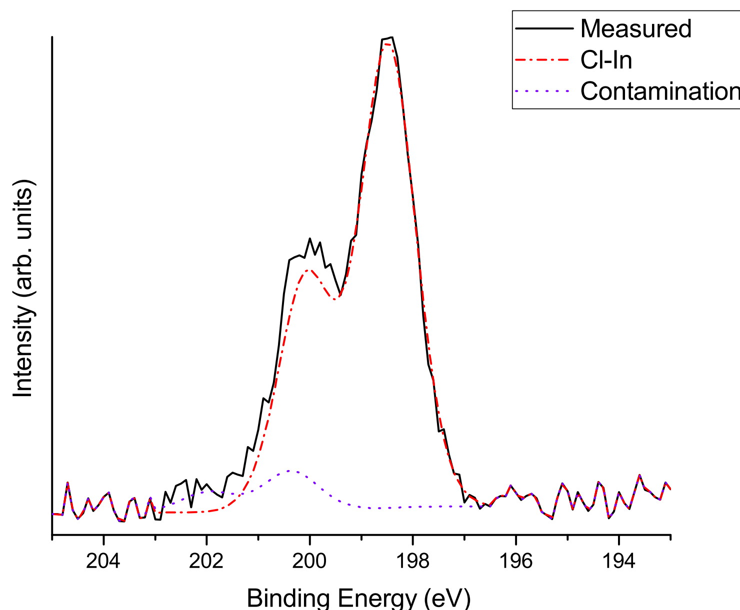


Figure 6.2: XPS data for the Cl 2p region of sample A. The measured data is shown in black, the fitted components for Cl-In is shown in red and an additional contamination component shown in purple

$InCl_3$ layers after HCl cleaning. Two samples - 1 cm squares of undoped bulk InSb - were prepared and immersed in cleaning solution for 30 s. Sample A was cleaned in a 1:5 solution of 37% HCl and IPA and rinsed in IPA and sample B was cleaned in a 1:5 solution of 37% HCl and deionised (DI) water and rinsed in DI water. After cleaning and rinsing, both samples were blow-dried using dry nitrogen and loaded into a vacuum desiccator for transfer to a Kratos Axis Ultra DLD spectrometer for XPS measurements. During this process, the samples were exposed to air for approximately 1 minute during loading into the desiccator and 20 seconds during transfer from the desiccator to the vacuum system. XPS data was acquired at a take-off angle of 90° with respect to the surface plane at a resolution of approximately 0.4 eV. The samples were illuminated with Al Kα X-rays and the spectrometer work function was calibrated using polycrystalline Ag foil prior to the experiments. XPS data was acquired from the as-loaded surface and following annealing for 30 minutes at 150°C, 200°C, 250°C and 300°C. The data were analysed using the CasaXPS software package, employing linear backgrounds and Voigt (Gaussian-Lorentzian) lineshapes.

The In 3d spectra acquired from the as-loaded surfaces are shown in figure 6.1. Both spectra exhibit components at 444.4 eV, assigned to InSb[116][117] and at 444.6 eV, assigned to In_2O_3[118][119][120]. Figure 6.1a shows the spectrum acquired

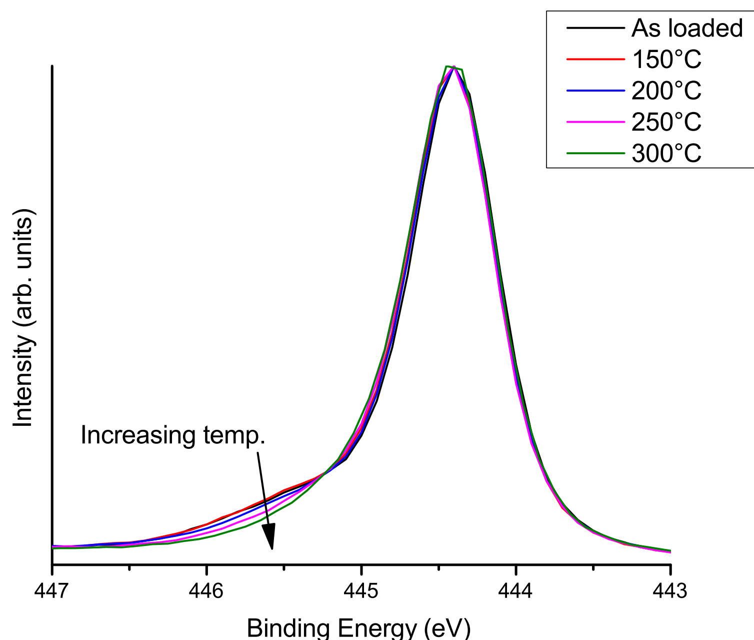


Figure 6.3: XPS data for the In $3d_{5/2}$ region of sample A. The as-received spectrum is shown in black (top), with spectra after a series of annealing steps shown in colour (below)

from sample A and exhibits an additional component at 445.6 eV when compared to sample B in figure 6.1b, a component attributed to the existence of $InCl_3$ on the surface[121]. Although this component occurs at a relatively low binding energy for In in its +3 oxidation state, as in $InCl_3$, quantitative comparison between In-Cl components from the In 3d and Cl 2p spectra, discussed below and included in table 6.3, indicate an In:Cl ratio of approximately 1:3, confirming the attribution of $InCl_3$. Table 6.1 shows a breakdown of the different bonding environments found in the In $3d_{5/2}$ region and reveals that 6.66% of the detected intensity from sample A was due to $InCl_3$. The InSb surface oxidises rapidly and the relative absence of oxygen in the HCl-IPA solution and IPA rinse is shown in figure 6.1a to hinder the formation of In_2O_3 and preserve the $InCl_3$ surface layer.

To further corroborate the existence of the $InCl_3$ layer, the Cl 2p spectrum from sample A is shown in figure 6.2 (no Cl 2p photoemission is observed from sample B). The spectrum shows two pairs of components, with the Cl $2p_{3/2}$ peak of the main pair found to be at 198.48 eV, corresponding well with the expected energy for $InCl_3$[121]. An additional, smaller, pair of components occurs with the Cl $2p_{3/2}$ peak at 200.37 eV, attributed to organochloride contamination, as intentionally-prepared organochloride compounds display photoemission at a similar binding energy[122][123].

The variation of the relative intensity of the $InCl_3$ component in the In $3d_{5/2}$

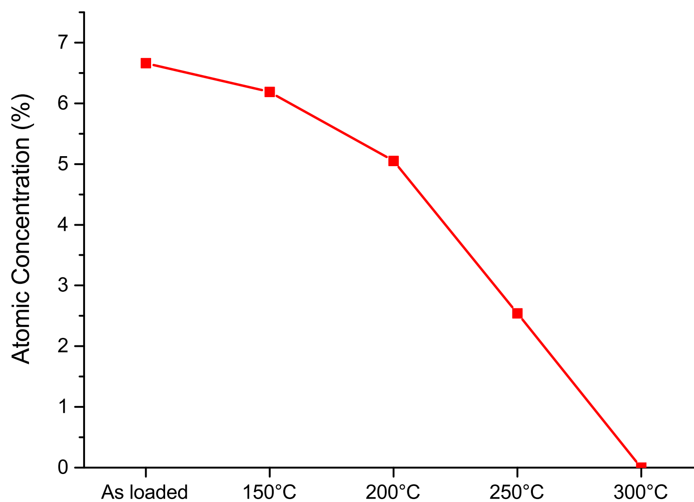


Figure 6.4: Atomic concentration of $InCl_3$ component relative to total In 3d region as-deposited and after each annealing stage

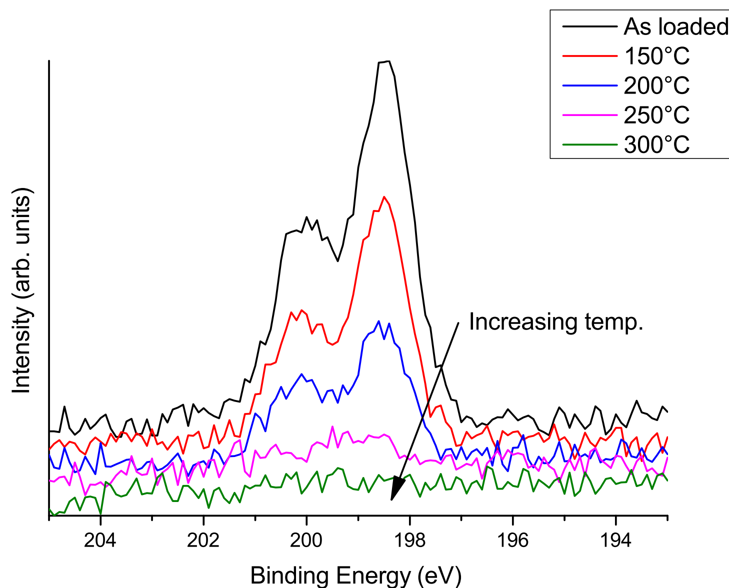


Figure 6.5: XPS data for the Cl 2p region of sample A. The as-received spectrum is shown in black (top), with spectra after a series of annealing steps shown in colour (below)

Table 6.2: Breakdown of the atomic percentages in each observed bonding environment from sample A as a function of annealing temperature. Values accurate to ±2%.

Component	As-loaded	150°C	200°C	250°C	300°C
InSb	51.2	51.4	52.1	53.5	54.8
In_2O_3	42.1	42.4	42.9	44.0	45.2
$InCl_3$	6.7	6.2	5.0	2.5	<1

Table 6.3: Variation in the In 3d & Cl 2p component atomic concentrations in the near-surface region of sample A as a function of annealing temperature. Values accurate to ±2%.

Component	As-loaded	150°C	200°C	250°C	300°C
In-Sb	40.7	44.4	47.3	51.9	54.8
In-O	33.6	36.6	39.0	42.8	45.2
In-Cl	5.3	5.3	4.6	2.5	<0.1
Cl-In	18.8	13.3	7.9	2.9	<0.1
Cl-Contam.	1.6	0.4	1.1	<0.1	<0.1

region is shown in figure 6.3, figure 6.4 and table 6.2. After annealing at 150°C only a small reduction in the relative $InCl_3$ contribution is observed, accelerating as the annealing temperature is increased until 300°C where the $InCl_3$ contribution is completely lost. The In_2O_3 component is unchanged, retaining the same ratio with the InSb component after all annealing processes.

Further evidence for the evolution of the surface of sample A as a function of annealing temperature was gathered from the Cl 2p region, as shown in figure 6.5. Here we see the total chlorine reducing with annealing temperature, with the chlorine loss accelerating rapidly above 150°C until it is completely removed at 300°C. Table 6.3 summarises the changes in the total atomic percentages of each component present on the surface during the annealing process, further proving the removal of the $InCl_3$ layer with increasing annealing temperature.

To verify the time-dependency of the desorption of $InCl_3$, an additional InSb sample was prepared with the same HCl-IPA treatment as sample A and transferred to an Omicron Multiprobe instrument equipped with a Sphera hemispherical analyser in a similar manner to samples A and B. XPS spectra were taken as-received and the temperature of the sample was then raised to 250°C, over 30 minutes with a ramp rate of approximately 7.7 °C per minute. Once the sample had reached 250°C, snapshot XPS spectra were taken to quantify the remaining Cl 2p emission and the In-Cl component in the In 3d spectrum. Within 5 minutes, the Cl 2p emission had

dropped below the detection limit of the instrument.

These results clearly indicate that a surface layer of $InCl_3$ forms for HCl-IPA treatments but not for HCl-water treatments, and that exposure to higher temperatures accelerates the desorption of $InCl_3$. As such, further study into MOSCAP structures was performed to investigate the effects of forming this $InCl_3$ layer.

6.3 HCl-Cleaned MOS Capacitors

Three 2" (∼50 mm) wafers of InSb without intentional doping but with a carrier concentration of approximately 1×10^{14} cm^{-3} n-type were cleaved in half, producing six samples of which five were used. Two samples received the same HCl-IPA treatment as sample A, two received the same HCl-water treatment as sample B and a control sample received no treatment. The samples were loaded into an Oxford Instruments OpAL ALD reactor promptly, with approximately 2 minutes exposure time in ambient air after removal from the rinse solution and before the ALD reactor was sealed and evacuated. Two samples, one for each wet treatment, and the control underwent deposition of 10 nm of Al_2O_3 at 200°C as an Al-first process. The other two samples underwent the same process at the higher temperature of 250°C. Following oxide deposition, the samples were degreased using acetone and isopropanol and 1 µm of Al metal was deposited in an SVS electron beam evaporator to serve as a gate contact. The gate metal was pattered using AZ 9260 photoresist as a mask and Microposit MF-319 photoresist developer (dilute tetramethyammonium hydroxide) as an etchant. The samples were diced for characterisation and characterised at a temperature of 80 K using a Leybold RDK 10-320 cryostat with a HP 4145 parameter analyser for I-V measurements and an Agilent E4980A LCR meter for C-V measurements, at frequencies between 1 kHz and 2 MHz. A typical C-V response is shown in figure 6.6.

During fabrication, it was observed that the surface wetting properties differed between the two wet treatments. The HCl-IPA solution and IPA rinse produced a surface with high wettability, consistent with a hydrophilic behaviour, whereas the HCl-water-treated surface displayed low wettability and was hydrophobic. For the HCl-water process, the sample surface repelled the etch and rinse solutions, accelerating their removal and potentially depositing particulates on the surface. For the HCl-IPA process, the sample surface retained the etch and rinse solutions until blown dry, thereby allowing particulates to be blown to the sample edge. For each process, four dies were prepared and 9 devices characterised per die, giving between 32 and 36 valid devices per process after wire bond failures were excluded.

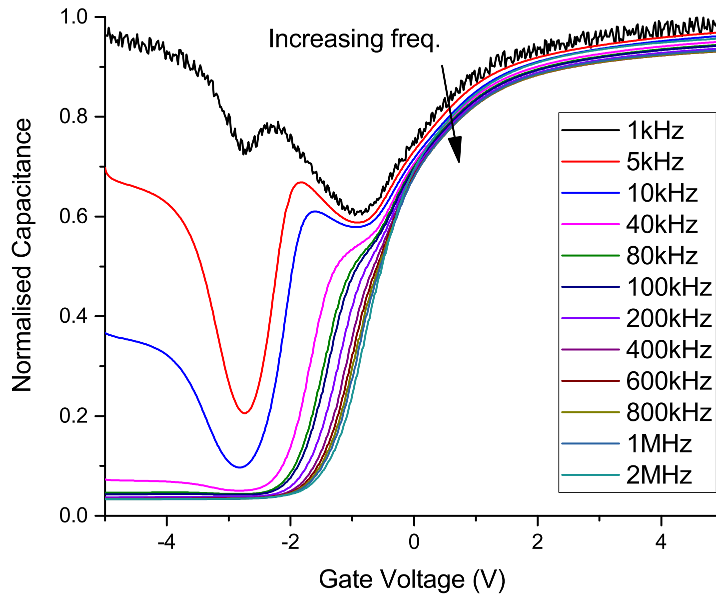


Figure 6.6: Typical multifrequency C-V response, taken for the HCl-water process and a deposition temperature of 200°C. Strong inversion response is discussed in section 5.6, weak inversion 'hump' feature is discussed in section 5.5 and accumulation freuency dispersion is discussed in section 2.3.

The HCl-water process displayed an overall yield poorer than the HCl-IPA process and also showed greater variability between repeating 10.9×9.2 mm device fields, with some fields matching the overall yield of the HCl-IPA process.

The flatband voltage (V_{FB}) was extracted and interface-trapped charge density (D_{it}) was extracted using the Terman and conductance methods, as detailed in sections 4.3, 4.5 and 5.2.2. In the C-V measurement, the DC voltage was swept from -5 V to +5 V, with reverse sweeps performed at low and high frequency (5 kHz and 2 MHz), enabling D_{it} and V_{FB} to be extracted for both sweep directions on many samples, as well as hysteresis voltage at C_{FB} (V_H). A typical C-V hysteresis response is shown in figure 6.7, with the initial zero-bias measurement and C-V sweep from this point to +5 V also shown. As the starting point lies on the forward sweep (-5 V to +5 V), V_{FB} has been extracted for the forward sweep direction.

After removing outliers, the distributions overlapped significantly and statistical hypothesis testing was necessary to extract significant trends. Distribution data for D_{it}, V_{FB} and V_H for all fabrication processes are shown in figures 6.8, 6.10 and 6.11 respectively, with box plots showing the median, interquartile range and range. These plots illustrate that the data do not conform to the normal (Gaussian) distribution and, as such, a nonparametric test was chosen. While the Wilcoxon test

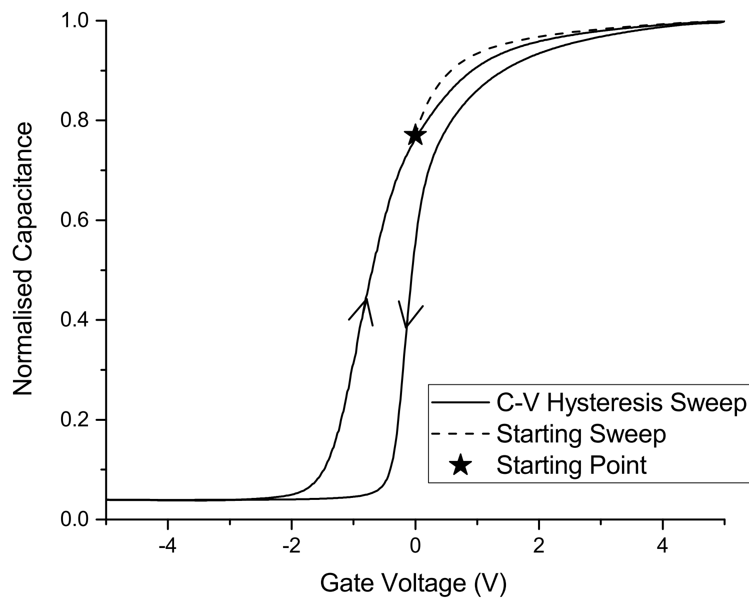


Figure 6.7: Typical bidirectional C-V response, taken at 2 MHz for the HCl-water process and a deposition temperature of 200°C. The initial zero-bias measurement, before electrical stimulation, is shown by the star symbol and the initial sweep from the zero-bias point to +5 V is shown by the dashed line. The hysteresis has been attributed to 'slow traps' in the oxide near the interface[52][51], discussed further in section 2.3.

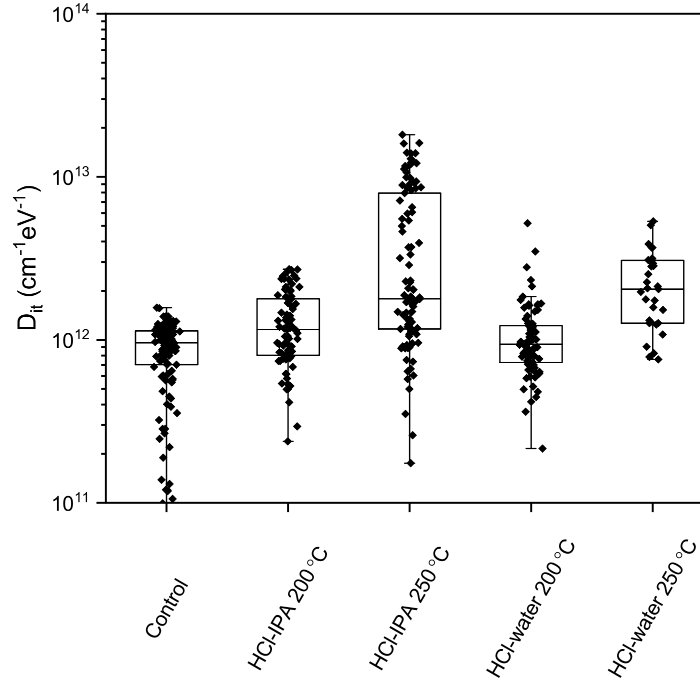


Figure 6.8: Distributions and variability of minimum D_{it} for the different fabrication processes. Box plots are shown for illustrative purposes only and statistical hypothesis testing was applied independently.

is a well-known nonparametric test, it does not control for multiple testing, rendering it unsuitable for this application, as treatments must be compared to each other as well as the control. The Steel-Dwass test is both nonparametric and controls for multiple testing, enabling pairwise comparison of all data sets. A confidence interval of 95%, $\alpha = 0.05$ was used for all samples and mean values are provided in table 6.4.

When comparing samples, only the HCl-IPA process with a deposition temperature of 200°C includes a substantial $InCl_3$ interfacial layer, as XPS shows that it is either not formed (as in the HCl-water process) or is significantly desorbed (as

Table 6.4: Mean average values of D_{it}, V_{FB} and V_H for the different fabrication processes

Process	D_{it} ($cm^{-2}eV^{-1}$)	V_{FB} (V)	V_H (V)
Control	8.7×10^{11}	-1.0	1.4
HCl-IPA 200°C	1.3×10^{12}	-0.2	1.1
HCl-IPA 250°C	4.3×10^{12}	-1.6	1.3
HCl-water 200°C	1.0×10^{12}	-1.0	1.2
HCl-water 250°C	2.3×10^{12}	-1.4	1.3

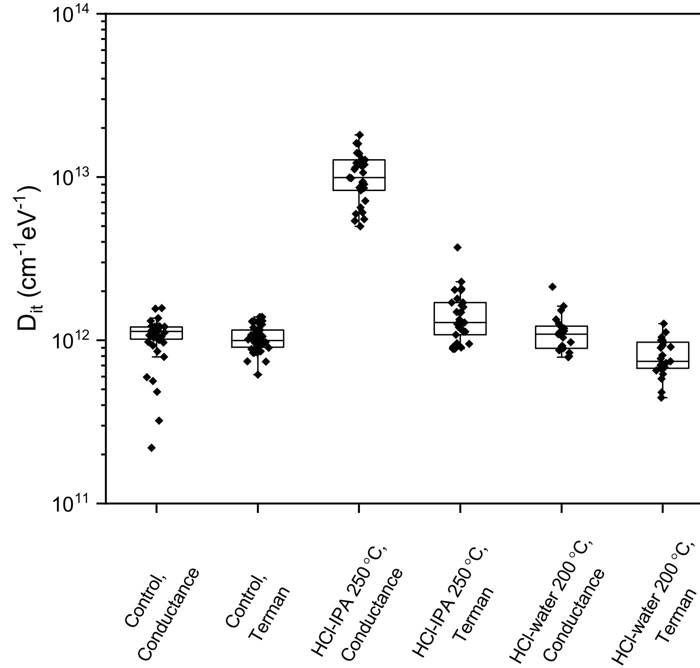


Figure 6.9: Distributions and variability of minimum D_{it} for the different fabrication processes and D_{it} extraction techniques. Box plots are shown for illustrative purposes only and statistical hypothesis testing was applied independently.

with 250°C deposition temperature) for other samples. The HCl-IPA process at 200°C shows a large positive shift in V_{FB} relative to the control (+0.79 V), whereas the HCl-water process at 200°C showed no significant shift and the 250°C processes showed negative shifts (-0.38 V and -0.61 V) with no statistically significant difference between the HCl-IPA and HCl-water cleaning processes. Figure 6.10 shows the V_{FB} distributions for the different fabrication processes.

InSb MOSCAP devices have shown high hysteresis in previous publication[59] and similar results have been reproduced here, with >0.1 V of hysteresis per volt of the C-V sweep. However, all cleaning processes resulted in a decrease in hysteresis compared to the control sample, with the best results obtained with a lower deposition temperature of 200°C and with no statistically significant difference between the cleaning processes. Figure 6.11 shows the distributions of absolute V_H for the different fabrication processes.

The D_{it} showed no statistically significant improvement on the control sample, with an average minimum D_{it} of 8.71×10^{11} $cm^{-2}eV^{-1}$ (see figure 6.8). Although both 200°C processes resulted in a small D_{it} increase relative to the control, the data variability is great enough that this result was found not to be statistically significant when tested. The 250°C process, however, resulted in a significant in-

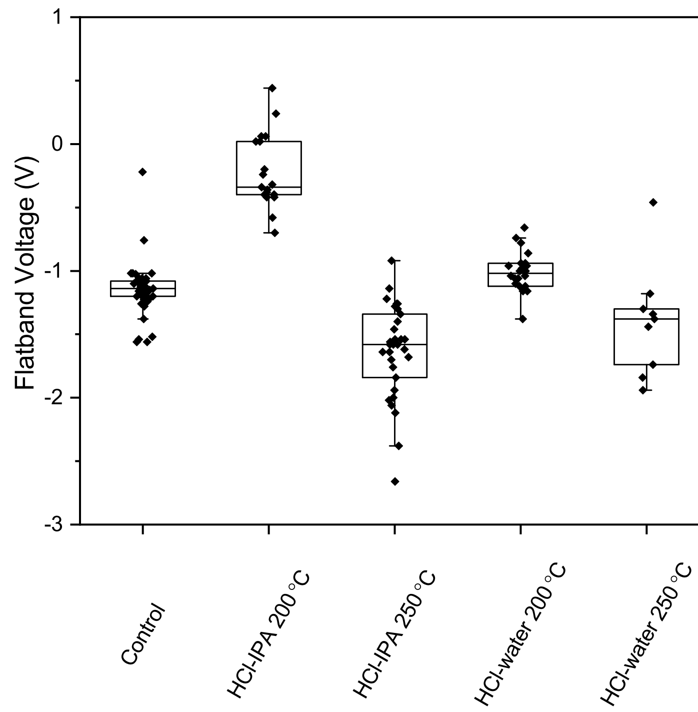


Figure 6.10: Distributions and variability of V_{FB} for the different fabrication processes. Box plots are shown for illustrative purposes only and statistical hypothesis testing was applied independently

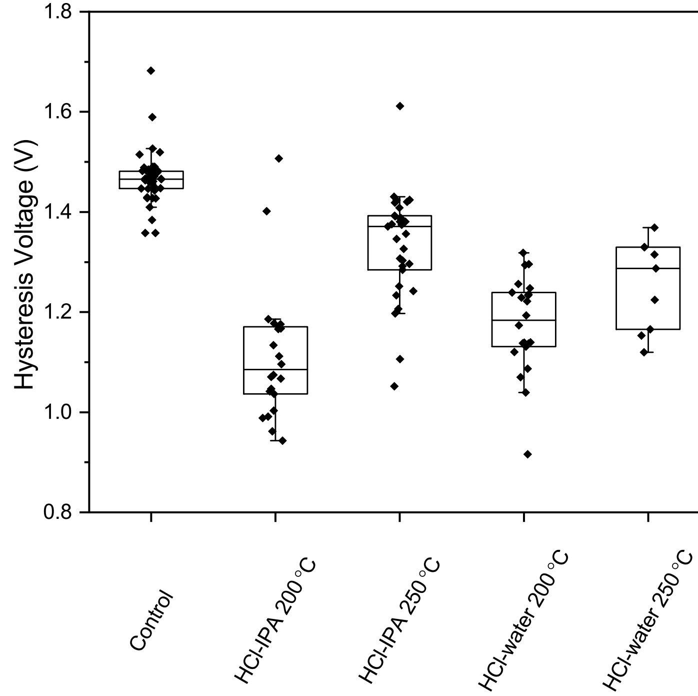


Figure 6.11: Distributions and variability of absolute V_H for the different fabrication processes. Box plots are shown for illustrative purposes only and statistical hypothesis testing was applied independently

crease in D_{it} for both cleaning processes, with a larger increase for the HCl-IPA process (to a D_{it} of 4.34×10^{12} cm^{-2}eV^{-1}) than for the HCl-water process (to a D_{it} of 2.25×10^{12} cm^{-2}eV^{-1}). This indicates that, although the $InCl_3$ interfacial layer can shift V_{FB} without affecting D_{it}, desorbing the $InCl_3$ layer will reverse the V_{FB} shift and increase D_{it}. Although the different D_{it} extraction processes showed the same trends, not all methods are equally sensitive to changes in fabrication process. The conductance method, in particular, showed a larger D_{it} increase for the HCl-IPA 250°C process than the Terman and high-low methods, as shown in figure 6.9.

The critical difference between the HCl-IPA and HCl-water processes for a deposition temperature of 200°C is the change in V_{FB}. This suggests that only fixed charge is introduced, without affecting D_{it} or 'slow' hysteresis charge and presents the opportunity to manipulate V_{FB} of MOSCAPs and, by extension, the threshold voltage of MOS transistor structures without impacting other figures of merit. The shift is substantial enough to move a MOS transistor threshold voltage from a depletion-mode device to an enhancement-mode device and may offer a promising route to fabricate both types of devices using similar fabrication processes.

Table 6.5: Plasma process parameters for plasma pre-treatment trials

Sample set	Plasma process	Ar flow (sccm)	H_2 flow (sccm)	Pre-plasma stabilise (s)	Power (W)	Time (mins)	Post-plasma purge (s)
A	Ar	60	0	10	50	5	10
A	Ar/H_2	40	20	10	50	5	10
B	Ar	80	0	20	50	5	20
B	Ar/H_2	50	30	20	50	5	20

6.4 Plasma-Cleaned MOS Capacitors

Plasma pre-treatments have been discussed previously in section 2.4.3. To investigate their applicability to InSb, two experiment runs were performed: at the University of Liverpool, thermal ALD at 200°C was combined with Ar and Ar/H_2 plasma pre-treatments and, at the University of Warwick, thermal ALD at 200°C and plasma ALD at 100°C were combined with Ar and Ar/H_2 plasma pre-treatments.

6.4.1 Experimental Methodology

Samples were prepared using bulk InSb: sample set A used undoped 2" InSb wafers with a carrier concentration of approximately $1{\times}10^{14}$ cm^{-3} n-type cleaved into 3 half-wafers and sample set B used Te-doped 2" InSb wafers with a carrier concentration of approximately $8{\times}10^{14}$ cm^{-3} n-type cleaved into 5 quarter-wafers. The wafers were all purchased from Wafer Technology Ltd. After the samples were cleaved, they all received an oxide strip in HCl (1:5 37% HCl and deionised (DI) water) and nitrogen blow-dry before being promptly loaded into their respective ALD instruments.

Sample set A underwent deposition using an Oxford Intruments OpAL at the University of Liverpool and sample set B underwent deposition using an Ultratech Fiji at the University of Warwick. Before oxide deposition, the samples were exposed to Ar and Ar/H_2 plasma, using the process recipes shown in table 6.5. Following plasma treatment, 10 nm of Al_2O_3 were deposited using TMA and water at 200°C as a thermal ALD process at both facilities and an additional two samples were prepared at Warwick, one with an Ar plasma treatment and one with no treatment, using plasma ALD at 100°C. ALD recipes are shown in table 6.6.

Table 6.6: ALD process parameters for plasma pre-treatment trials

Sample set	Process	TMA Dose (s)	TMA Purge (s)	Co-reagent Dose (s)	Co-reagent Purge (s)	Plasma Power (W)
A	Thermal, 200°C	0.03	3	0.02	3	N/A
B	Thermal, 200°C	0.06	8	0.06	8	N/A
B	Plasma, 100°C	0.06	4	6	4	300

After ALD, the samples were unloaded and transferred to an SVS electron-bean evaporator and received 1 µm of Al as a gate contact. Sample set B was transferred promptly but sample set A were transported between fabrication facilities and degreased using acetone and isopropanol before loading. Following metal deposition, the samples were cleaved, mounted to carrier PCBs using GE varnish and wire bonded, then loaded into a Leybold RDK 10-320 cryostat for characterisation at 80 K. Current-voltage (I-V) measurements were performed using a HP 4145 parameter analyser, an Agilent 4155C parameter analyser and a Keithley Sourcemeter and capacitance-voltage (C-V) measurements were performed using an Agilent E4980A LCR meter, at frequencies between 1 kHz and 2 MHz.

6.4.2 Results and Discussion

The results from electrical analysis are shown below. The yield for the Ar and Ar/H_2 processes in sample set B was 0% - to examine the cause of this issue, DC leakage and breakdown data is shown in figures 6.12, 6.13 and 6.14. Figure 6.12 shows the leakage current density (J_L) at -5 V (the maximum applied voltage) for 'good' devices, which did not undergo dielectric breakdown. Figure 6.13 shows sub-breakdown leakage current density for 'bad' devices which underwent dielectric breakdown at less than -5 V and figure 6.14 shows the breakdown voltage - the lowest voltage where I_{leak}>0.09 A, noting that the compliance limit was set to 0.1 A. Note, also, that some devices underwent 'soft' breakdown, with leakage current rising continuously towards the compliance limit, and, in such case, the definition of 'breakdown voltage' is largely arbitrary.

Figure 6.12 shows that, relative to the untreated control from sample set A, introducing either plasma treatment within the same ALD system increased DC

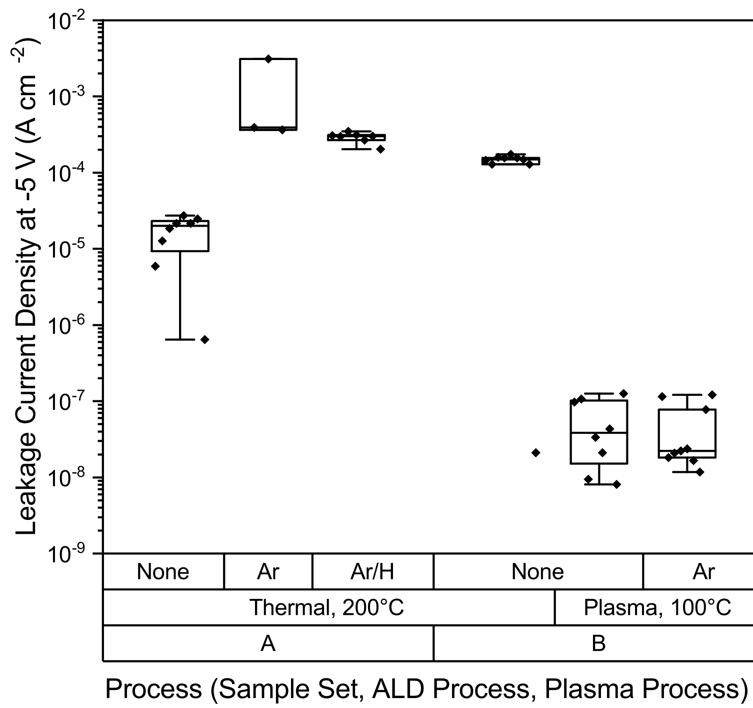


Figure 6.12: Distributions and variability of DC leakage current density at -5 V for good devices from different plasma processes.

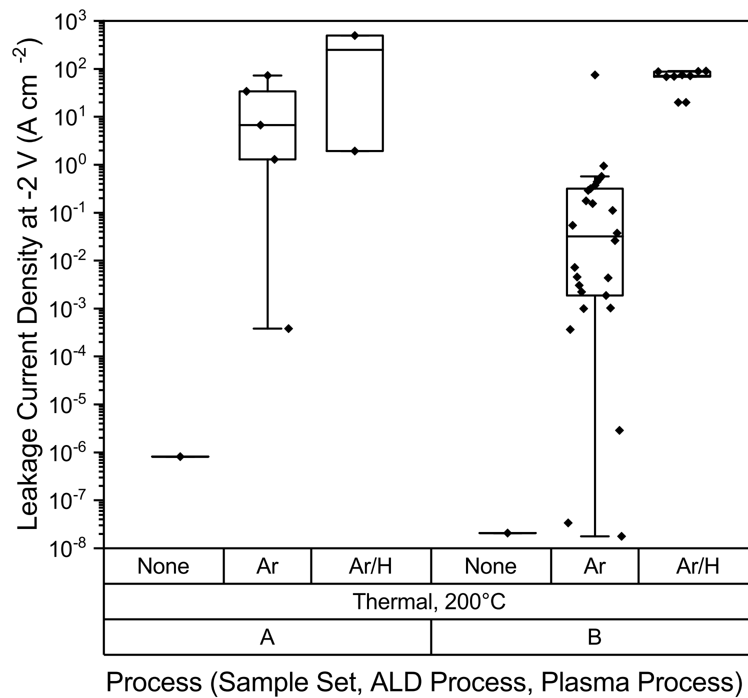


Figure 6.13: Distributions and variability of DC leakage current density at -2 V for bad devices from different plasma processes

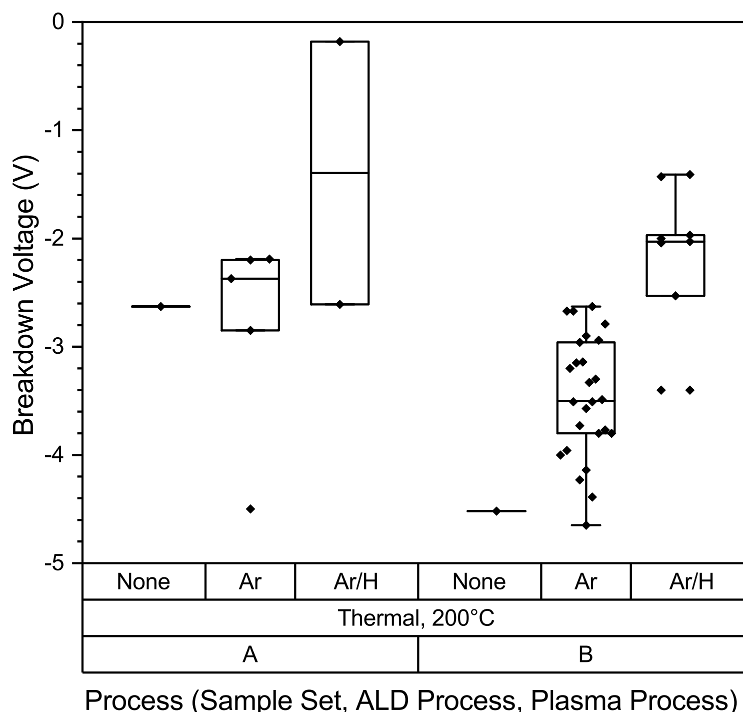


Figure 6.14: Distributions and variability of DC breakdown voltage (lowest voltage where I_{leak}>0.09 A) for bad devices from different plasma processes

leakage by approximately an order of magnitude but the same effect is also observed for the untreated control from sample set B. The increased leakage in sample set B may be a result of the ALD process not being optimised, as the recipe used for the study and detailed in table 6.6 was provided with the ALD system and has not been modified. The increase in DC leakage following the introduction of the plasma processes was unexpected - DC leakage has not been discussed in the literature and it is unclear if the increased leakage is peculiar to InSb or if it is potentially a more widespread issue. The mechanism for such an increase is unclear, particularly as the plasma power is low and there is no applied DC bias to the system, suggesting that the degree of surface bombardment would be low. Despite this, surface roughening may play a role in increased leakage, particularly if selective removal or reaction of In/Sb at the surface is affecting the nucleation of dielectric deposition. Further investigation using XPS may offer a route to characterising these changes, although sample thinning in XPS using Ar sputtering may affect the results, so samples must be prepared with thin oxide by ALD to allow characterisation of the interface without sputter thinning.

Figure 6.12 also shows significantly reduced DC leakage when plasma-enhanced deposition is used for the Al_2O_3 deposition. Although not highlighted in figure

6.12, both plasma deposition samples are at or below the minimum distinguishable current for the system (the 'noise floor'). As the measured oxide capacitance is also greater for these samples, the plasma-enhanced deposition can be concluded to offer a higher dielectric density, as expected for plasma-enhanced ALD. The plasma-enhanced deposition also shows no discernible increase in leakage following plasma pre-treatment, although the difference may simply be below the detection limit of the characterisation system. It is difficult to speculate over the mechanism preventing change due to plasma pre-treatment, as both the ALD co-reagent and deposition temperature were changed simultaneously - to validate this effect, additional samples should be studied so that all combinations of temperature, co-reagent and plasma treatment have been explored.

Consistent with the leakage results in 'good' devices, figure 6.13 shows high sub-breakdown leakage for plasma-treated devices. However, it also shows that the addition of H_2 to the plasma causes further increased DC leakage compared to Ar alone in both sample sets. This suggests that the mechanism of increased leakage may include chemical interactions between the plasma and substrate but further study is required to characterise the degradation mechanism. A similar effect is observed in the breakdown voltage shown in figure 6.14: Ar/H plasma causes more rapid onset of breakdown than Ar alone in sample set B.

The distributions for interface-trapped charge (D_{it}), flatband voltage (V_{FB}) and hysteresis voltage (V_H) in 'good' devices are shown in figures 6.15, 6.16 and 6.17. In contrast to section 6.3, many samples contained too few devices to reliably apply statistical hypothesis testing methods, and so estimations of significance are made based on the interquartile range and overall range, and the intersection thereof between samples.

For D_{it} in figure 6.15, sample set A shows higher variability than sample set B - this may be due to differing cleanliness between the two fabrication facilities. The interquartile ranges for all 3 samples in set A overlap over a wide range and so observed differences in minimum D_{it} cannot be considered significant. By contrast, the interquartile ranges for the samples in set B do not intersect (or do so over a small range only) and so differences can be considered significant. The data from the Terman and conductance method is generally consistent for the samples in this study, increasing confidence in the acquired data.

When comparing the untreated control samples for thermal ALD at 200°C and plasma-enhanced ALD at 100°C for sample set B, a small but significant decrease in D_{it} is observed, from 1.0×10^{12} cm^{-2}eV^{-1} to 8.0×10^{11} cm^{-2}eV^{-1}. As noted above, the simultaneous change of both deposition temperature and ALD co-reagent pre-

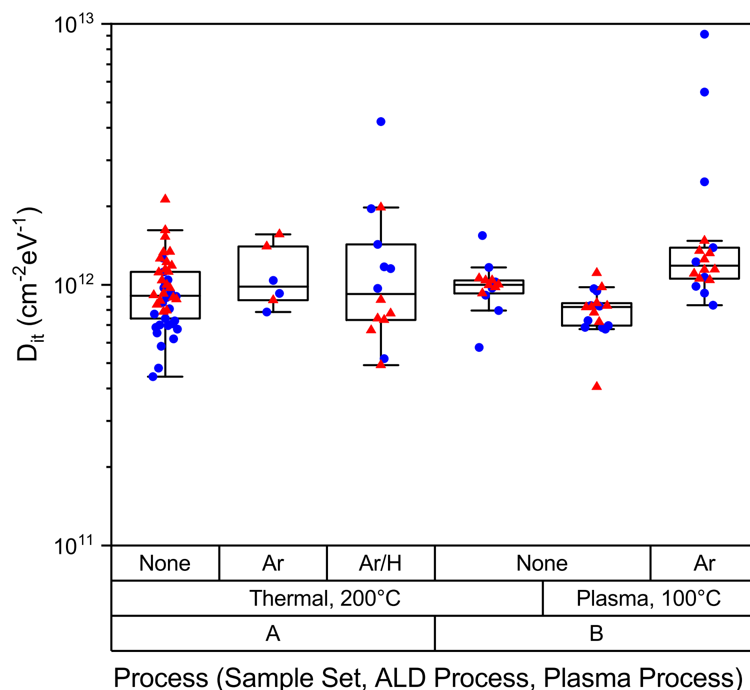


Figure 6.15: Distributions and variability of minimum interface-trapped charge for different plasma processes. Blue circles: D_{it} extracted by the Terman method, red triangles: D_{it} extracted by the conductance method

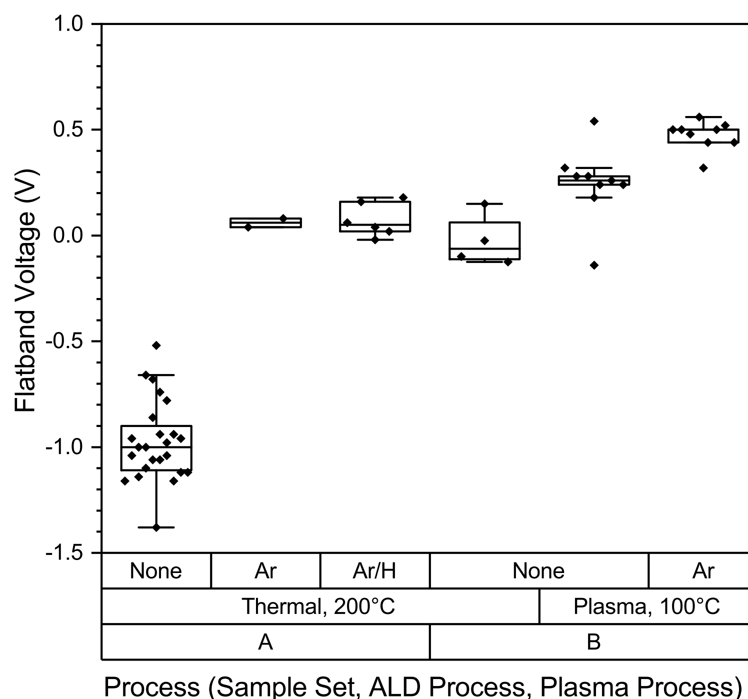


Figure 6.16: Distributions and variability of flatband voltage for different plasma processes

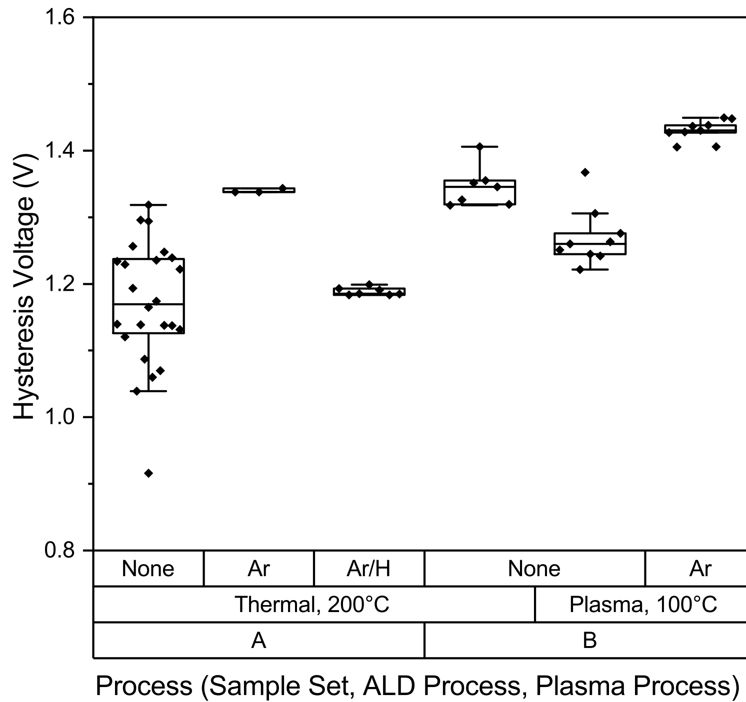


Figure 6.17: Distributions and variability of hysteresis voltage for different plasma processes

vents reliable assessment of this change: additional samples for thermal ALD at 100°C and plasma-enhanced ALD at 200°C should expose the relative contribution for both changes. A further significant change is, however, observed for the introduction of the Ar plasma pre-treatment. D_{it} increases from 8.0×10^{11} $cm^{-2}eV^{-1}$ to 1.9×10^{12} $cm^{-2}eV^{-1}$, indicating that the Ar plasma treatment performed in this study is detrimental to D_{it}, rather than beneficial. Further investigation into the plasma and ALD process parameters and optimisation may elucidate whether this detrimental effect is specific to this process or general to the InSb-Al_2O_3 material system.

Significant changes are observed for flatband voltage in figure 6.16, the largest of which is a shift of 1.04 V between the untreated control and the Ar plasma treatment in sample set A. The source of this shift in unclear, particularly as the flatband voltage behaviour of sample set B is very different to sample set A. The control sample from sample set B is approximately in line with the other samples from set B but they are also closely aligned with the plasma-treated samples from set A, with the control sample from set A displaced approximately 1 V from the global median. When this large displacement is considered together with the smaller shift between samples from set B with and without Ar plasma treatment (0.23 V),

it may be that the control sample from set A is incorporating contamination that is eliminated by the plasma treatment in sample set A and that is not present is sample set B.

An additional change is observed between the thermal ALD process at 200°C and the plasma ALD process at 100°C for sample set B - from -0.03 V to 0.24 V. As discussed previously, the simultaneous change of deposition temperature and ALD co-reactant limits scope for discussion but it is possible that the O_2 plasma is affecting V_{FB} similarly to the Ar plasma pretreatment, and that the reduced deposition temperature is inducing additional trap states and trapped charge in the oxide.

For V_H, the introduction of the Ar plasma pre-treatment is associated with a significant increase in hysteresis: from 1.17 V to 1.34 V for thermal ALD at 200°C in sample set A and from 1.27 V to 1.43 V for plasma ALD at 100°C. Suspected deterioration mechanisms are discussed above: surface roughening, selective removal of In/Sb and their effect on ALD initiation are potential causes for increased hysteresis. For hysteresis, however, this change is reversed for the Ar/H_2 process in sample set A (V_H decreases to 1.19 V) and further investigation is required into the relative contributors to different figures of merit.

Two additional changes in V_H are observed. The first is the increase in V_H for sample set B, compared to sample set A, for the thermal ALD at 200°C control samples (1.17 V to 1.35 V). This change is similar to the change observed in DC leakage current and may similarly be a result of the process not being fully optimised. The second additional change was a decrease in V_H for the plasma ALD process at 100°C and this is, again, similar to trends observed in DC leakage current. This may be related to the increased density of the oxide.

6.5 Conclusion and Further Work

Wet chemical pre-treatments using HCl and plasma pre-treatments using Ar and Ar/H_2 plasma have been studied. X-ray photoelectron spectroscopy (XPS) study into HCl treatments showed that an $InCl_3$ surface layer, previously observed in the literature for treatments in inert atmosphere, only forms in ambient atmosphere when the HCl is diluted in isopropanol and rinsed in isopropanol. This layer significantly desorbs when the substrate temperature is raised from 200°C to 250°C. In electrical measurements, the $InCl_3$ layer was associated with a large shift in flat-band voltage (V_{FB}) relative to the control without HCl treatment (+0.79 V). When the ALD deposition temperature was increased from 200°C to 250°C to investigate

the effects of desorbing $InCl_3$, the V_{FB} change was reversed but all figures of merit deteriorated. HCl treatments were found not to improve interface-trapped charge density (D_{it}) relative to the untreated control but hysteresis voltage (V_H) was improved from 1.4 V to a minimum of 1.1 V, with increased deposition temperature causing both figures of merit to deteriorate.

If $InCl_3$ were to be taken further as a route to manipulate flatband voltage, its stability and reproducibility would require further study. In addition to slow/partial desorption at 200°C, the layer may not be stable with further thermal processing and additional study would establish its stability. The chemical states and physical interfacial layers in MOSCAPs could also be further investigated using XPS, to ascertain bonding configurations after deposition, and using high-resolution cross-sectional transmission electron microscopy (TEM) to image the dielectric-semiconductor interface, potentially also using energy-dispersive X-ray spectroscopy (EDX) and/or electron energy loss spectroscopy (EELS) to study composition. Furthermore, alternative wet treatments, such as ammonium hydroxide, hydrofluoric acid and tetramethylammonium hydroxide may offer superior MOSCAP response to HCl alone, or as additional steps in a multiple-step wet cleaning process (e.g. the RCA clean). Further XPS studies may offer particular insight, showing removal of contaminants and resulting reaction products of specific wet treatments. It may also be appropriate to perform the treatments under inert atmosphere in a glove box and transfer to the XPS instrument under inert atmosphere to prevent the products/contaminants under investigation from oxidising.

Plasma pre-treatments were found to consistently cause deterioration in InSb-Al_2O_3 MOS capacitors. DC leakage current increased for both Ar and Ar/H_2 plasma pre-treatments, preventing many devices from being characterised by C-V methods. Some increases in D_{it} were observed following plasma pre-treatments, whereas, for V_H, Ar plasma treatment gave increased V_H but an Ar/H_2 treatment gave a V_H consistent with the untreated control sample. Plasma pre-treatment caused V_{FB} to increase in all cases but a larger change was observed for devices which underwent ALD at the University of Liverpool than at the University of Warwick - this change may be related to contamination or processes requiring further optimisation. Further process trials may establish whether the detrimental effects are specific to the process parameters or general to plasma treatments on InSb and XPS may reveal physical/chemical mechanisms associated with degradation.

Further changes were observed between the control samples deposited using the different facilities and between a thermal ALD process at 200°C and a plasma-enhanced ALD process (using O_2 plasma as an oxygen precursor) at 100°C. Sam-

ples prepared at the University of Warwick had higher DC leakage current, V_{FB} closer to 0 V and increased hysteresis - this may be related to process optimisation. The plasma-enhanced process produced significantly lower DC leakage current and higher oxide capacitance, consistent with a higher oxide density, slightly reduced D_{it}, slightly increased V_{FB} and slightly decreased V_H. Further study is required to isolate the effects of changing deposition temperature and ALD co-reagent.

Chapter 7

Post-deposition Annealing

7.1 Introduction

Post-deposition annealing is a standard, widely-employed technique in the field of Si-SiO_2 interfaces but is less frequently explored in III-V materials. In addition to the potential benefit available through post-deposition annealing, the low melting point of InSb presents constraints and challenges (the material may partially or completely break down below its melting point).

As such, a systematic study into the annealing on InSb metal-oxide-semiconductor capacitor (MOSCAP) structures was performed and is presented here. The study uses a relatively small volume of samples to begin to chart the 'parameter space' - the multidimensional space of temperature, time, gas, flow rate etc. - for InSb annealing, identifying regions where the material breaks down and regions where device performance can be improved. A wide range of parameter space is covered in moderate detail to identify regions which merit more detailed investigation and optimisation. The anneal processes presented here are post-metallisation anneal processes: by depositing and patterning the gate metal before dicing, annealing and characterising, fabrication overheads could be reduced and a larger number of samples studied.

7.2 Experimental Methodology

Three 2" (∼50 mm) Te-doped n-type wafers of InSb with a carrier concentration of approximately 8×10^{14} cm^{-3} n-type were loaded into an Oxford Instruments OpAL ALD reactor, without pre-treatment, where they received 10 nm of Al_2O_3 at 200°C as an Al-first process. Following oxide deposition, the samples were degreased using acetone and isopropanol and 1 µm of Al metal was deposited in an SVS electron

beam evaporator to serve as a gate contact. The gate metal was pattered using AZ 9260 photoresist as a mask and Microposit MF-319 photoresist developer (dilute tetramethyammonium hydroxide) as an etchant.

The wafers were then diced into 1 cm square samples and treated with a range of annealing processes. A Carbolite tube furnace was used with three anneal gases, each maintained at a flow rate of 100 sccm: N_2, O_2 and forming gas ('FG', a mixture of 5% H_2 and 95% N_2 by volume). The furnace was pre-heated to each process temperature, the samples each loaded into an alumina crucible and inserted directly into the furnace. When the samples were unloaded, the crucible was withdrawn and deposited into a larger alumina crucible to cool in air at room temperature - the temperature ramp rate up and down was not directly controlled and the samples were exposed to air while still close to process temperature. Samples were annealed for a range of times between 5 mins and 10 hrs, at a range of temperatures between 200°C and 500°C. One sample from each wafer was retained as a control sample, receiving no anneal treatment.

After annealing, each samples was mounted to a sample carrier printed circuit board (PCB) using GE varnish and wire bonded to the PCB using Al bond wires. These sample PCBs were then mounted to a Cu carrier block using GE varnish and loaded into a Leybold RDK 10-320 cryostat for characterisation at 80 K. Current-voltage (I-V) measurements were performed using a HP 4145 parameter analyser, an Agilent 4155C parameter analyser and a Keithley Sourcemeter and capacitance-voltage (C-V) measurements were performed using an Agilent E4980A LCR meter, at frequencies between 1 kHz and 2 MHz. Data analysis was used to extract interface-trapped charge (D_{it}) by the Terman and conductance methods, flatband voltage (V_{FB}) and hysteresis voltage (V_H), as well as frequency dispersion in accumulation, as described in sections 4.3, 4.5 and 5.2.2. This data is presented in sections 7.4, 7.5 and 7.6 as box plot distributions. For most samples, between five and nine devices were measured - as this sample size is too small to reliably apply statistical hypothesis testing methods, estimations of significance are made based on the interquartile range and the intersection thereof between samples.

A typical C-V from a control sample is shown in figure 7.1. The D_{it} for the control sample was 1.2×10^{12} cm^{-2}eV^{-1}, the average V_{FB} was -1.05 V, the average V_H was 1.38 V and the average frequency dispersion was 1.4 %dec^{-1}.

Specific results of interest at high anneal dose, including cross-sectional transmission electron microscopy images, are discussed in section 7.3. General results, including identification of optimal anneal regimes, are discussed in sections 7.4, 7.5 and 7.6.

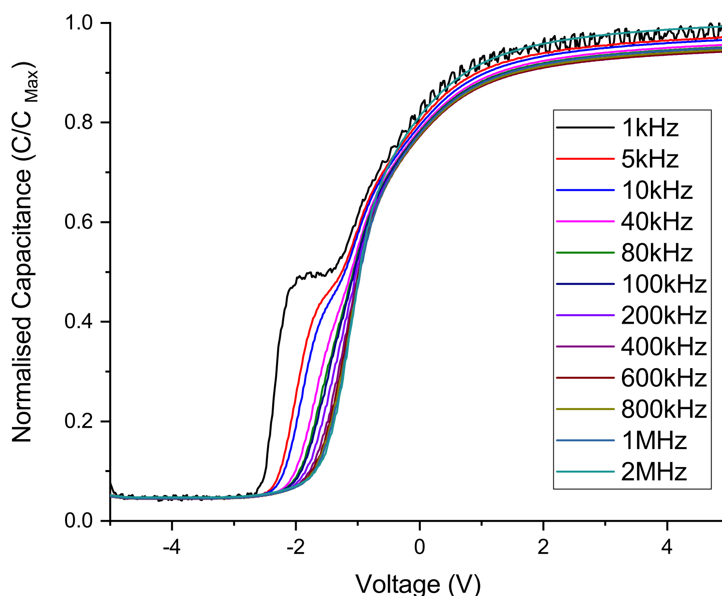
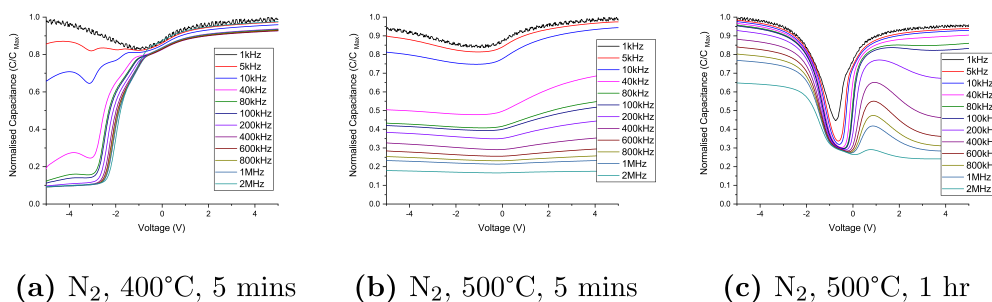


Figure 7.1: Typical multifrequency capacitance-voltage response from MOSCAP devices without annealing

7.3 Material Breakdown at High Temperature

Typical C-V responses from high annealing dose samples are shown in figure 7.2.

Qualitatively, figure 7.2a, obtained from an anneal in N_2 at 400°C for 5 minutes, shows increased stretch-out and a more prominent 'hump' feature at high frequencies, implying increased D_{it}. The sample is discussed quantitatively in more detail below, in sections 7.4, 7.5 and 7.6, but with an average D_{it} of 3.6×10^{12} cm^{-2}eV^{-1}, an average V_{FB} of -1.75 V, an average V_H of 0.98 V and an average frequency dispersion of 1.7 %dec^{-1}, the hysteresis voltage is the only improvement on the control,



(a) N_2, 400°C, 5 mins **(b)** N_2, 500°C, 5 mins **(c)** N_2, 500°C, 1 hr

Figure 7.2: Typical multifrequency capacitance-voltage response from MOSCAP devices with a high annealing dose. (a) N_2, 400°C, 5 mins (b) N_2, 500°C, 5 mins (c) N_2, 500°C, 1 hr

with D_{it}, V_{FB} and frequency dispersion all deteriorating

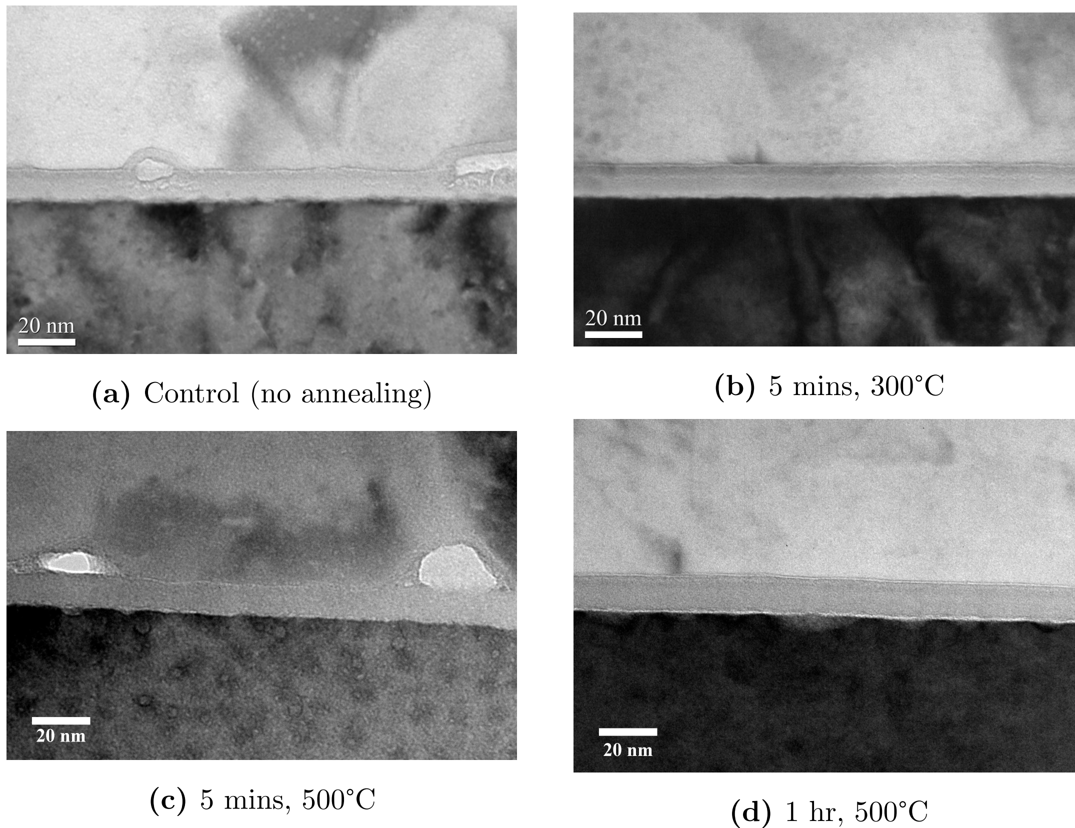
Increasing the annealing dose results in a dramatic change, attributed to the accelerated onset of material breakdown. Figure 7.2b shows C-V response after annealing in N_2 at 500°C for 5 minutes but a similar result is obtained after annealing in N_2 at 400°C for 1 hr. Qualitatively, the classical C-V features are breaking down, with frequency dispersion-like behaviour dominating over classical accumulation-depletion-inversion behaviour. As such, quantitative analysis cannot be performed reliably, with the exception of frequency dispersion in accumulation, which has increased to 38 $\%dec^{-1}$.

Further increasing the annealing dose to 500°C for 1 hr or 400°C for 10 hrs results in another dramatic change, shown in figure 7.2c. While the capacitance measured at positive bias continues to display highly frequency-dependent behaviour, the capacitance measured at negative bias becomes significantly more stable. Furthermore, the gradient and profile of the C-V in depletion has come to resemble a p-type device. This is consistent with the theory of Sb desorption above the non-congruent temperature of InSb: deficiency of the group V element will result in deficiency of electrons, acceptor-like behaviour of vacancy sites and p-type behaviour of the material.

To investigate the interface and possibility of diffusion, samples were prepared for cross-sectional transmission electron microscopy (TEM) characterisation. The samples taken were a control sample (which had received no annealing), a sample annealed below the threshold of breakdown (for 5 mins at 300°C in N_2), a sample annealed slightly above the threshold (for 5 mins at 500°C in N_2) and a sample annealed significantly above the threshold (for 1 hr at 500° in N_2).

The TEM specimens were prepared using conventional methods: a small piece, ~1 mm thick, was cleaved from each sample, mounted in a sample holder ring, ground down to a thickness of <10 µm, then ion milled using a Gatan precision ion polishing system (PIPS) until holes formed. The material surrounding the hole is sufficiently thin to allow electron transmission and imaging. The specimens were imaged up to a magnification of 100000× using a JEOL 2100+ TEM and high-magnification images are shown in figure 7.3, showing the Al metal (upper), substrate (lower) and Al_2O_3 dielectric (centre).

The key feature from these images is a thin interfacial layer, ~0.8 nm thick, visible as a high-brightness feature between the substrate and oxide in figures 7.3c and 7.3d but not figures 7.3a and 7.3b. Although delamination can be observed between the Al metal and the Al_2O_3 dielectric in figures 7.3a and 7.3c, the interfacial layer can be distinguished from delamination due to its uniformity, extending over



(a) Control (no annealing)

(b) 5 mins, 300°C

(c) 5 mins, 500°C

(d) 1 hr, 500°C

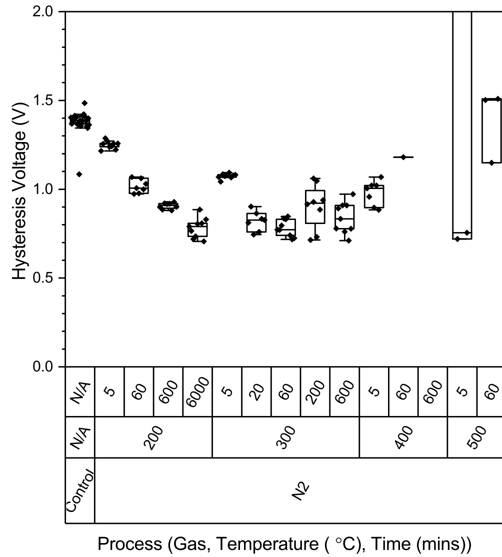
Figure 7.3: Cross-sectional TEM images of annealed samples

the entire image, in contrast to the delamination features, which are typically only 20 nm in length.

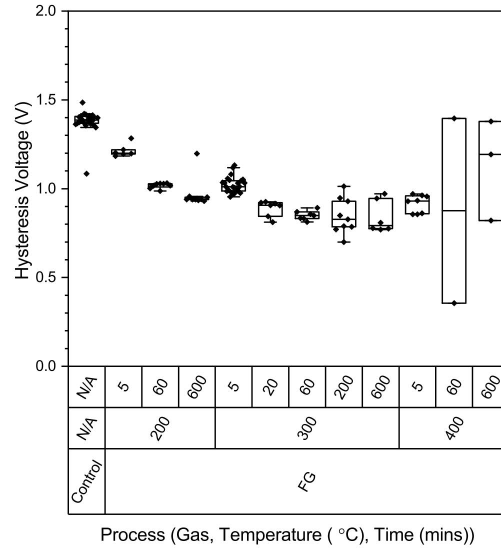
While these images identify a feature correlating with breakdown, the JEOL 2100+ does not have sufficient resolution to image the interfacial layer in more detail, or to analyse it using energy-dispersive X-ray spectroscopy (EDX), nor is it equipped with an electron energy loss spectroscopy (EELS) analysis unit. Both EDX and EELS would allow compositional analysis and, if combined with scanning TEM (STEM), would allow composition mapping. These techniques would allow composition of the interfacial layer to be determined and the diffusion of elements across the interface to analysed. Further work should attempt these techniques using a suitable instrument, such as the JEOL ARM200F sited at the University of Warwick.

7.4 Hysteresis Response to Annealing

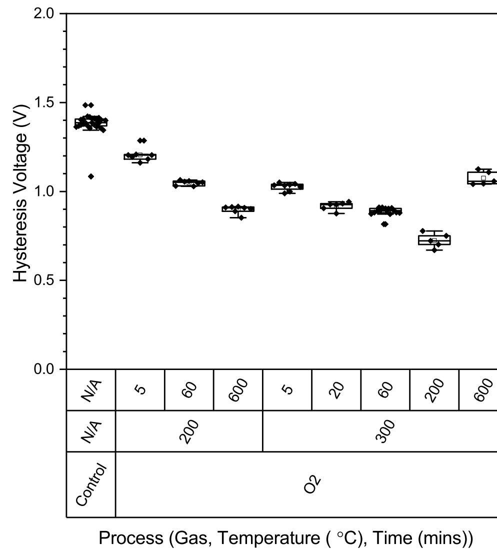
The distributions of hysteresis voltage for the N_2 gas processes are shown in figure 7.4a. All anneal processes below the breakdown threshold of the material offer a reduction in V_H, with a minimum occurring at approximately 1 hr for an annealing



(a) N_2 anneal processes



(b) Forming gas anneal processes



(c) O_2 anneal processes

Figure 7.4: Distributions and variability of hysteresis voltage for control and different anneal gas processes. X-axes: top: anneal time (mins), middle: anneal temperature (°C), bottom: anneal gas

temperature of 300°C and a similar result obtained for a 100 hr anneal at 200°C. From the control sample to these minima, V_H decreases from 1.38 V to 0.79 V for the 300°C minimum and 0.78 V for the 200°C minimum. While the 100 hr 200°C process offers the best results for V_H, deterioration is observed in other figures of merit, discussed below in sections 7.5 and 7.6, as well as increased variability. The 1 hr 300°C process produces comparable V_H results, without impacting on other figures of merit

At 300°C, V_H appears to increase for anneal times longer than 1 hr, increasing to 0.90 V for a 200 min anneal and 0.84 V for a 10 hr anneal. This increase (∼0.08 V) is approximately the same magnitude as the interquartile range for the 'optimal' 1 hr process. This change is relatively small but a similar change of a larger magnitude is also observed for the 5 min 400°C process (the only >300°C process that does not cause gross breakdown), which, when taken together with the 300°C results, suggests that the total thermal dose may be causing the material to deteriorate below the breakdown threshold. The samples in this regime also show increased variability, particularly when compared to the control samples.

The distributions of hysteresis voltage for the forming gas and O_2 processes are shown in figures 7.4b and 7.4c, respectively. Similar trends to the N_2 processes are observed: decreasing V_H with anneal time at 200°C, a minimum at approximately 1 hr at 300°C and deterioration when annealed at 400°C. The lowest V_H minima are 0.84 V and 0.72 V for forming gas and O_2, respectively - the forming gas does not demonstrate any improvement over the N_2 processes and, while O_2 shows a small improvement, its magnitude is approximately the same as the interquartile range of the optimal N_2 process and the improvement may not be significant.

The forming gas and O_2 processes show different trends for 300°C anneals above 1 hr when compared to the N_2 processes. Whilst both forming gas and O_2 show increased variability above 1 hr, similarly to the N_2 processes, they do not immediately show an increase in V_H. For the forming gas processes, V_H plateaus at 1 hr, with no significant improvement or deterioration for the 200 min and 10 hr doses. For the O_2 processes, the V_H minimum occurs after annealing for 200 mins and deteriorates after a 10 hr anneal.

The optima for the 3 gas processes occur at approximately the same temperature and time, implying that the benefits of the anneal process are from the thermal dose rather than the chemistry of the gases. This may be due to the gate metal presenting a sufficient barrier to gas molecules, preventing them from interacting with the interface, but it may also be due to insufficient process temperature. When the process temperatures used here are compared to processes in the literature (see sec-

tion 2.5), these temperatures are significantly lower than other processes performed on III-V materials, which are usually performed at 400°C or higher. As such, the processes performed here at 300°C may not have sufficient energy to activate chemical processes in forming gas or O_2. Additional investigations into anneal processes before metallisation and into high-temperature, short-duration processes by rapid thermal annealing may provide further insight.

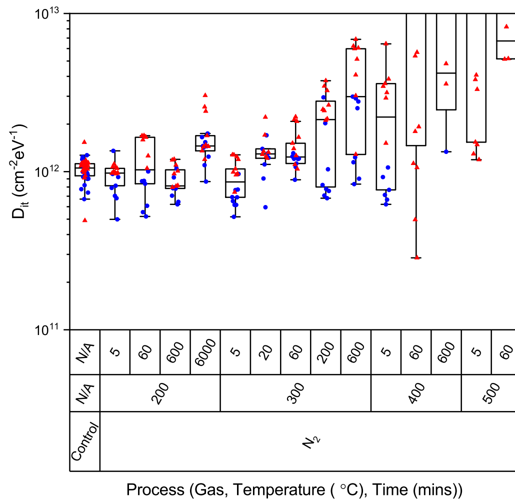
As the 300°C, 20 mins to 10 hr regime studied here displays high variability, particularly for N_2 processes, the optimal conditions and 'true' minimum cannot be clearly identified and are 'obscured' by variability and imprecision, e.g. sample ramp rate upon loading. A general statement can be made that the optimal anneal time is around 1 hr to 10 hr at 300°C, with some evidence of sample deterioration at longer doses, particularly in N_2, but a more tightly-controlled study, potentially with larger sample volumes and additional repeat measurements, would be required for a more accurate estimate of the optimal post-metallisation anneal process.

7.5 Interface-Trapped Charge Response to Annealing

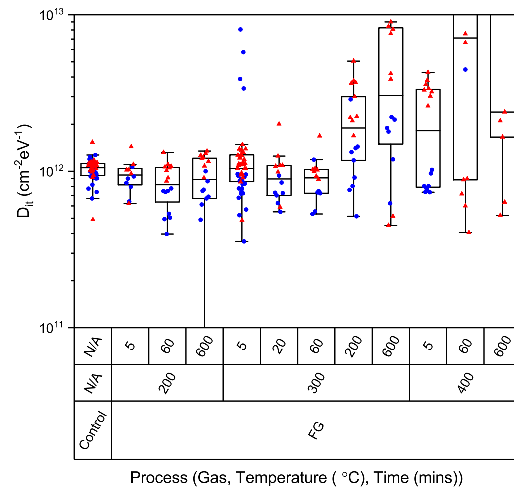
The distributions of minimum D_{it} for the N_2 gas processes are shown in figure 7.5a. As noted in previous sections, the material breakdown above 400°C affects the data extraction severely, shown here by an increase in average D_{it} and extreme increase in variability, at least an order of magnitude. It should also be noted, however, that such increase in D_{it} and variability begins for the 200 mins process at 300°C, with D_{it} increasing from 1.4×10^{12} cm^{-2}eV^{-1} for 1 hr at 300°C to 2.0×10^{12} cm^{-2}eV^{-1} for 200 mins at 300°C and the interquartile range increasing from $10^{0.15}$ to $10^{0.56}$. This supports the supposition from section 7.4 that the cumulative annealing dose causes deterioration above 1 hr at 300°C without the gross breakdown observed in section 7.3. The 100 hr, 200°C process also shows increased D_{it}, and as its interquartile range does not intersect that of the control sample, it can be concluded that this increase is significant.

Another observation to note from figure 7.5a, but also from figures 7.5b and 7.5c, is that, while the data from the Terman and conductance methods frequently overlap, the average D_{it} by the conductance method is slightly higher than using the Terman method. This may be related to the normalisation-induced upturn in conductance D_{it}, discussed in section 5.5, or due to the conductance method not capturing the same minimum as the Terman method, due to its limited energy range.

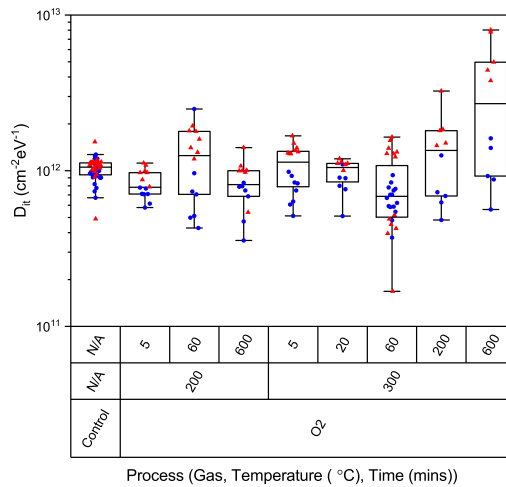
For the N_2 processes, some small improvements in D_{it} are observed for low



(a) N_2 anneal processes



(b) Forming gas anneal processes



(c) O_2 anneal processes

Figure 7.5: Distributions and variability of minimum interface-trapped charge for control and different anneal gas processes. Blue circles: D_{it} extracted by the Terman method, red triangles: D_{it} extracted by the conductance method. X-axes: top: anneal time (mins), middle: anneal temperature (°C), bottom: anneal gas

annealing doses: at 200°C up to 10 hrs and at 300°C for 5 mins. The lowest D_{it} for a N_2 process was 8.9×10^{11} cm^{-2}eV^{-1}, for 10 hrs at 200°C but the interquartile range of this sample intersects the control sample. This trend does not continue for the 100 hr, 200°C process and further study is recommended before concluding that this improvement is genuine and repeatable.

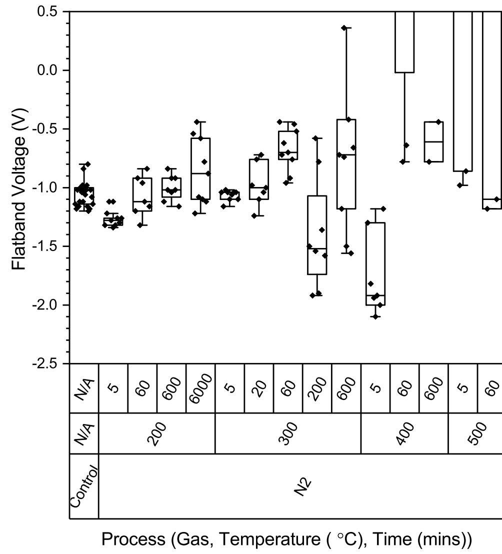
The distributions of minimum D_{it} for the forming gas and O_2 processes are shown in figures 7.5b and 7.5c, respectively. Similar, again, to all results discussed thus far, variability and average D_{it} increase for anneal dose above 1 hr at 300°C. For thermal doses below this, however, trends cannot be clearly observed. The forming gas processes have slightly lower D_{it} in this regime but, as with the N_2 processes, variability is sufficiently high and interquartile ranges intersect frequently enough that additional data must be gathered before conclusive improvements can be demonstrated.

Two samples underwent annealing in O_2 for 1 hr at 300°C. Both are displayed in the same cell in figure 7.5c - the Terman D_{it} distributions overlap but the conductance D_{it} presents two distinct distributions. One sample displayed significantly lower D_{it}, with an average of 5.6×10^{11} cm^{-2}eV^{-1} but this process could not be repeated for the second sample. This observation may be related to the high-performance crystalline native oxide reported by Punkkinen *et al.*[124] and Lång *et al.*[125]. This observation suggests that annealing may potentially offer a route to a similar high-performance native oxide but the inability to repeat the positive result suggests that, if such a native oxide is achievable, it is likely to be highly sensitive to process parameters and control.

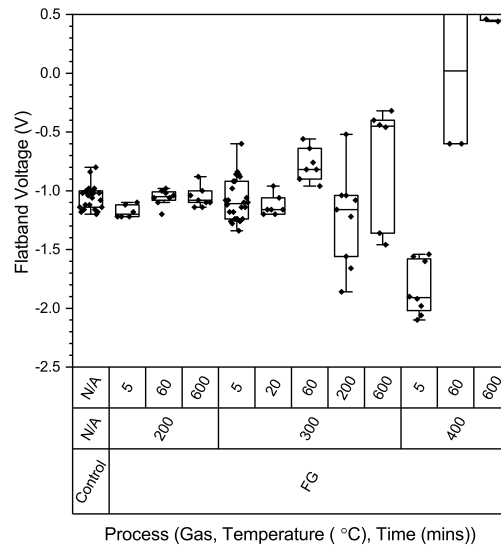
7.6 Flatband Voltage Response to Annealing

The distributions of flatband voltage for the N_2, forming gas and O_2 processes are shown in figures 7.6a, 7.6b and 7.6c, respectively. Trends are similarly difficult to observe in V_{FB} as in D_{it}: deterioration is still observed within the same time/temperature regions as discussed above, particularly for variability but the magnitude of the flatband voltage also increases for most processes between the optimum and gross breakdown. The 100 hr, 200°C anneal process, despite giving average V_{FB} of slightly decreased magnitude, gives significantly increased variability, suggesting that some deterioration may be occurring and the apparent improvement may not be stable and repeatable.

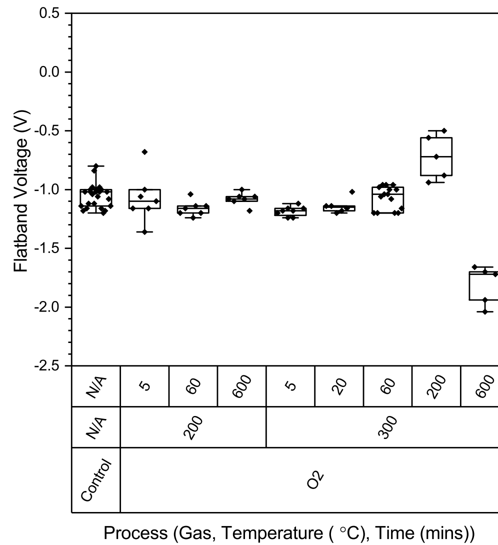
The optimum processes for V_{FB} are 1 hr at 300°C for the N_2 and forming gas processes and 200 mins at 300°C for the O_2 processes. These coincide with the



(a) N_2 anneal processes



(b) Forming gas anneal processes



(c) O_2 anneal processes

Figure 7.6: Distributions and variability of flatband voltage for control and different anneal gas processes. X-axes: top: anneal time (mins), middle: anneal temperature (°C), bottom: anneal gas

optima for V_H and, for the forming gas process, the region of potentially improved D_{it}. For these processes, the magnitude of V_{FB} is significantly reduced, with the interquartile range not intersecting that of the control sample or the sample with the next-shortest anneal time. The control sample had an average V_{FB} of -1.05 V and this improved to -0.68 V for the optimal N_2 process, -0.78 V for the optimal forming gas process and -0.72 for the optimal O_2 process. Similarly to V_H, the improvements in V_{FB} appears insensitive to anneal gas, implying, as discussed in section 7.4, that the chemical action of the gases are being inhibited and alternative annealing regimes may provide further insight and/or improvement.

7.7 Conclusion and Further Work

A range of anneal gases, temperatures and times have been studied as post-metallisation anneal processes. The devices and InSb material were found to break down when annealed at 400°C for 1 hr or more and at 500°C for any time. For low post-threshold doses, the classical C-V features break down and C-V response displays only strong frequency dispersion across all voltages and frequencies. For high post-threshold doses, the C-V response closely resembles p-type material, with increased frequency dispersion in accumulation. This behaviour is attributed to out-diffusion of antimony leaving vacancy sites which act as acceptors, producing a layer of p-type material. Transmission electron microscopy (TEM) samples were prepared and showed an interfacial layer in samples annealed above the breakdown threshold but additional characterisation at higher resolution is required to characterise the interfacial layer and diffusion.

Below the breakdown threshold, clear improvements have been demonstrated in V_H and V_{FB}. V_H was reduced from 1.38 V to 0.72 V and V_{FB} was improved from -1.05 V to -0.68 V. Smaller, marginally significant, improvements have been observed in D_{it}. The optimal processes observed in this study were 1 hr at 300°C in N_2, 1 hr at 300°C in forming gas and 200 mins at 300°C in O_2. Above these optima, all figures of merit showed deterioration in magnitude and/or variability for all figures of merit, despite remaining below the threshold for gross breakdown.

As the scope of this study was broad, a more detailed study would provide more accurate optimisation. Smaller increments in temperature and time would provide more accurate mapping of parameter space and larger sample size would provide more reliable comparison following data extraction.

Additional studies could also be performed into post-deposition annealing processes before metal deposition and into rapid thermal annealing. This study focused

on post-metallisation annealing for ease of fabrication but the e-beam deposition process may have introduced additional damage, obscuring the effects of annealing on the substrate and dielectric interface[88] - additional work on post-deposition annealing before metallisation and on annealing after thermal evaporation of metal may provide additional insight.

Rapid thermal annealing may produce significantly different results to the results presented here. This study demonstrated deterioration, correlating with total thermal dose, and insensitivity to anneal gas: rapid thermal annealing may offer routes to more energetic gas chemistry without causing gross breakdown of the material and interface.

Chapter 8

AlInSb Ternary Alloy

8.1 Introduction

The work presented in this thesis thus far has been performed on binary InSb. However, practical InSb-based structures include AlInSb as either its main constituent or as a confining layer and, in the applications of surface passivation and gate control, dielectrics will almost certainly be deposited onto ternary AlInSb, rather than binary InSb. To investigate the differences between InSb and AlInSb, and the role of aluminium on InSb-based surfaces/interfaces, a series of AlInSb layers of varying aluminium composition were prepared and investigated.

The preparation of AlInSb materials is limited by crystal growth techniques: ternary materials are not commercially prepared as bulk wafers and must be grown epitaxially. Within epitaxial growth, conventional limits of solubility and material quality are further limited by the matching of lattice constant to a substrate. Prospective substrates for the growth of AlInSb within this project are InSb and GaAs. InSb offers a large lattice constant and a small lattice mismatch, with the addition of Al producing a layer in tensile strain. By contrast, GaAs produces a large lattice mismatch and significant compressive strain for all AlInSb compositions but offers semi-insulating substrates - the use of semi-insulating substrates is common in practical devices[126][127]. An additional limitation is also present for AlInSb material: aluminium compounds, including AlSb, oxidise readily in ambient air and can experience far greater surface degradation than InSb surfaces. The limit for surface stability in AlInSb is approximately 20-25% Al.

Two sets of samples were prepared and studied. The first set aimed to investigate the effect of low Al composition (∼0.1%) in layers grown on InSb substrates, aiming to prevent lattice relaxation, the subsequent formation of crystal defects and their effect on device response. The second set aimed to investigate the effect of Al in

high composition AlInSb (the 1-20% range), including lattice relaxation but capable of covering a larger range of composition.

8.2 Strained AlInSb with Low Al Composition

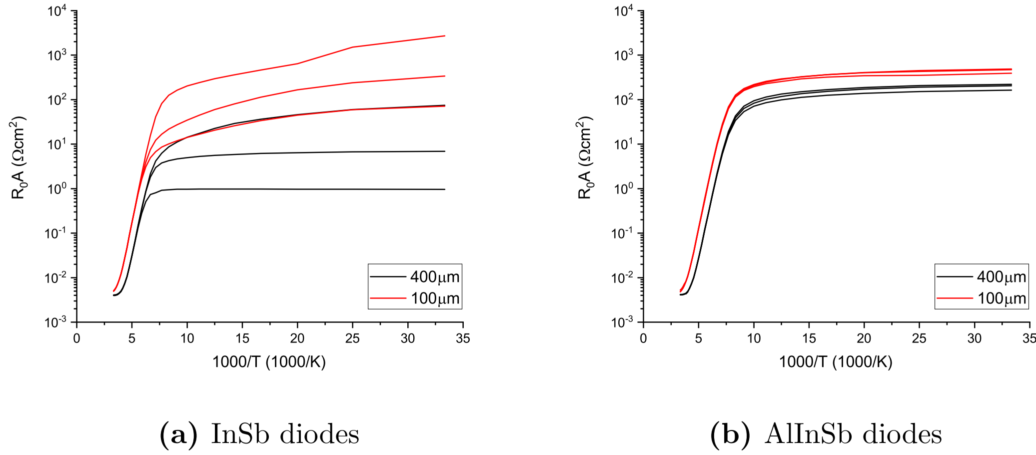
Two samples were prepared on InSb substrates. They were grown on p-type bulk InSb wafers with approximately 3×10^{13} Ge-doping, purchased from Wafer Technology limited, using a Veeco Gen II MBE reactor. The substrates received no cleaning before loading and underwent only thermal oxide desorption under an antimony overpressure before growth.

Two wafers underwent growth for MOSCAP devices: approximately 6.51 µm of undoped material grown directly onto the InSb substrate. Two further wafers underwent growth for p-i-n homostructure diode devices: 51 µm of Te-doped ($\sim1\times10^{18}$ n-type) material as a buffer and n-type contact, 11 µm of undoped material ($<1\times10^{16}$ n-type) as an active region and 0.51 µm of Be-doped ($\sim1\times10^{18}$ p-type) material as a top contact. The diode samples were prepared to extract background dopant concentration for use in analysis of MOSCAP devices.

For each layer structure, a control sample was grown with 0% Al composition (i.e. binary InSb) throughout and an AlInSb sample was grown with a target Al composition of 0.1%. This composition was not characterised or confirmed directly: the target was for finite Al composition of ∼0.1% without inducing sufficient strain for the material to relax. This low composition was unsuitable for direct characterisation: energy-dispersive x-ray spectroscopy (EDX), x-ray photoelectron spectroscopy (XPS) etc. lack sufficient sensitivity for constituents below ∼1%, no calibration standard was available for secondary ion mass spectroscopy (SIMS) and the strain/lattice mismatch was too low to resolve using x-ray diffraction (XRD). Atomic force microscopy (AFM) was used to investigate surface morphology and surface decoration of defect features.

8.2.1 Diode Characterisation (Dopant Concentration)

Diode characterisation was ultimately unsuitable for dopant extraction. As discussed below in section 8.3, Hall measurements of InSb on semi-insulating GaAs gave an average dopant concentration of 1.44×10^{15} cm^{-3} n-type, whereas the C-V characterisation gave average minimum dopant concentration of 4.6×10^{17} cm^{-3} for the InSb diodes and 3.4×10^{17} cm^{-3} for the $Al_{0.001}In_{0.999}Sb$ diodes. As the materials on InSb and GaAs were grown using similar growth conditions, current-voltage (I-V)



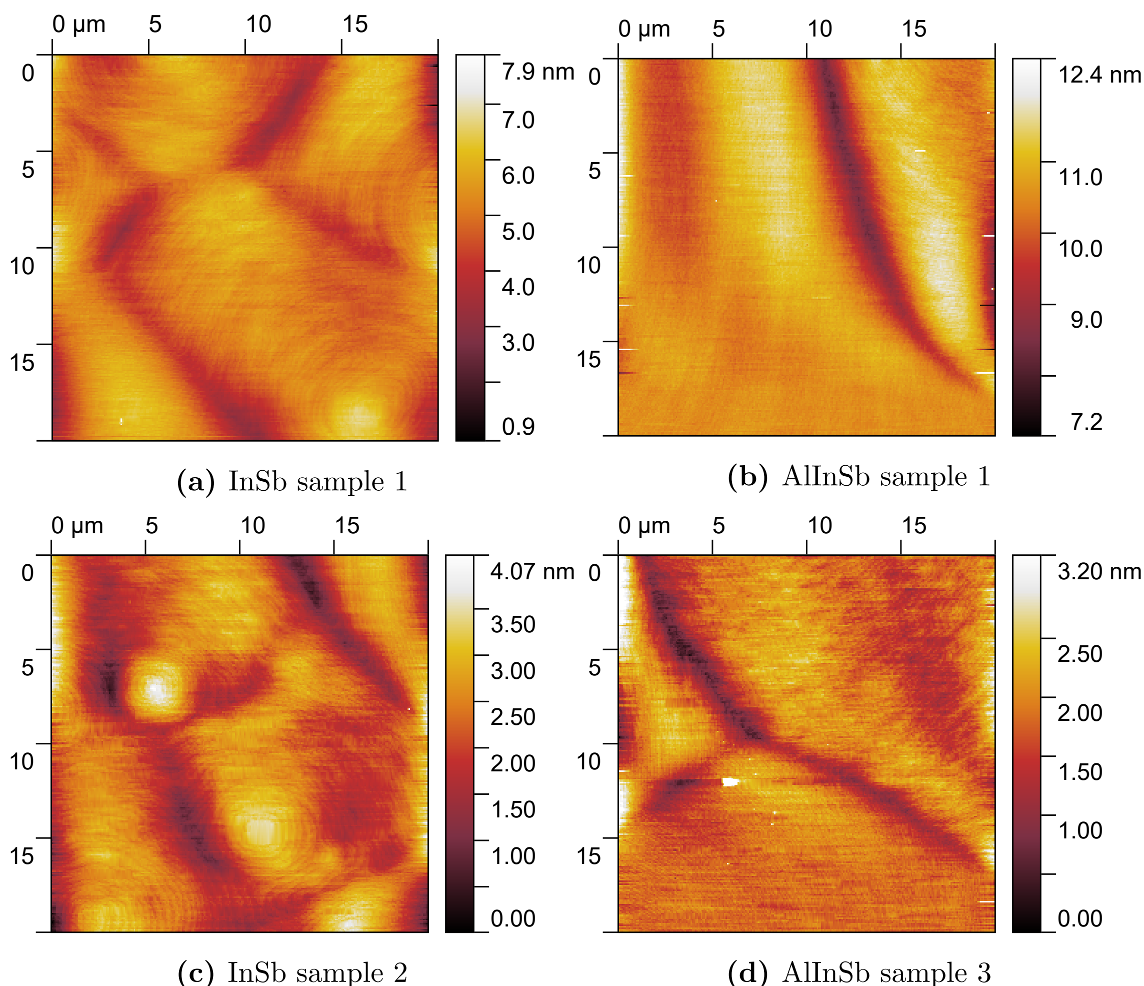
(a) InSb diodes **(b)** AlInSb diodes

Figure 8.1: Plots of R_0A against reciprocal temperature for InSb and AlInSb diodes. Note that the 400 μm devices were characterised for decreasing temperature and the 100 μm devices for increasing temperature

characterisation at variable temperature (I-V-T) was used to further investigate the diodes and benchmark them against historic devices.

When characterising InSb-based diodes, the preferred figure of merit is differential resistance at zero bias (R_0), and specifically zero-bias resistance multiplied by device area (R_0A, where A is the area of the cross-section which current flows through). A high R_0A is preferred. Plots of R_0A against reciprocal temperature are shown in figure 8.1 - the high-temperature region on the left, which appears approximately linear in figure 8.1, is diffusion-limited and the low-temperature region on the right, which appears approximately flat or 'turned over', is generation-recombination limited.

The average (arithmetic mean) maximum R_0A is 533 Ωcm^2 for the InSb devices and 323 Ωcm^2 for the $Al_{0.001}In_{0.999}Sb$ devices, at a temperature of 30 K. Historic values for comparable structures give an average R_0A of approximately 10^5 Ωcm^2 at 77 K[128][129][130]. The measured R_0A is approximately 3 orders of magnitude poorer then historic devices, indicating that fabrication issues - e.g. growth defects, impurities, process damage etc. - may be affecting devices. As these issues are likely to affect the C-V characterisation too, the dopant extraction is deemed to be unreliable and the Hall measurement data from the InSb sample on semi-insulating GaAs is taken instead.



(a) InSb sample 1

(b) AlInSb sample 1

(c) InSb sample 2

(d) AlInSb sample 3

Figure 8.2: AFM images from MOSCAP samples.

8.2.2 Atomic Force Microscopy Characterisation (Surface Defects)

AFM images were captured for the InSb and 0.1% AlInSb MOSCAP layers. The instrument used was a Park XE-100 AFM, the AFM tips were Pt-coated NSC-14 tips from MikroMasch and measurements were performed in contact mode. The scan area was 20 µm×20 µm and post-processing in the freeware package Gwyddion was used to align rows, subtract the background and remove 'scar' features from the scanning acquisition process. Four scans were taken for the InSb sample and two for the 0.1% AlInSb. A sample of AFM images are shown in figure 8.2.

The InSb sample shows clear 'hillock' features, with valley-like boundaries visible where features intersect. These may be induced by a 3-dimensional growth mode, or as surface decorations from material defects - possibly induced by incomplete desorption of native oxide prior to material growth. This would be consistent with the diode characterisation results shown in section 8.2.1.

In the AlInSb sample, there are no visible 'hillock' features but there are visible 'valley' boundaries between features. It is surmised that the AlInSb sample includes similar features to the InSb sample but with significantly increased size/reduced density. The average number of 'hillock' regions in a 20 µm×20 µm scan is 5.3 for the InSb sample and 2.5 for the AlInSb sample. As both samples were grown under identical conditions and nominally lattice matched/strained, this suggests that the two samples did not undergo identically ideal growth - one or both of the samples may include material defects and the AlInSb may be relaxed. This study is limited, however, by the number of measurements. To confirm this result, a larger number of scans should be taken, preferably over multiple samples and/or areas of the wafer.

8.3 Relaxed AlInSb with High Al Composition

Two samples were prepared on GaAs (limited by the end of the MBE growth campaign). They were grown on semi-insulating bulk GaAs wafers with a resistivity of $>10^7$ Ω cm, purchased from AXT Inc., using a Veeco Gen II MBE reactor. The substrates received no cleaning before loading and underwent a thermal oxide desorption before growth.

A scheme of buffer layers was grown to accommodate heteroepitaxy and lattice mismatch. A GaAs smoothing layer was grown, with a thickness of 200 nm, followed by a AlSb nucleation layer, with a thickness of 200 nm, to accommodate a large proportion of the lattice mismatch with a minimal density of mismatch-related defects. A thick layer of undoped target material, 51 µm was then grown to allow propagating defect features to meet and annihilate before propagating to the top of the structure.

Both layers were grown as MOSCAP layers. One sample of InSb was grown as a control and one AlInSb sample was grown, with an Al composition of 10%. The dopant concentration was determined by Hall measurement, as discussed in section 5.3.1: the InSb material had an average dopant concentration of 1.44×10^{15} cm^{-3} n-type and the $Al^{0.1}In_{0.9}Sb$ had an average dopant concentration of 1.40×10^{16} cm^{-3} n-type. The dopant concentration for InSb (1.44×10^{15} cm^{-3}) was also used for the InSb and $Al_{0.001}In_{0.999}Sb$ on InSb, under the assumption that neither the change of substrate or the addition of 0.1% Al would significantly affect the dopant concentration.

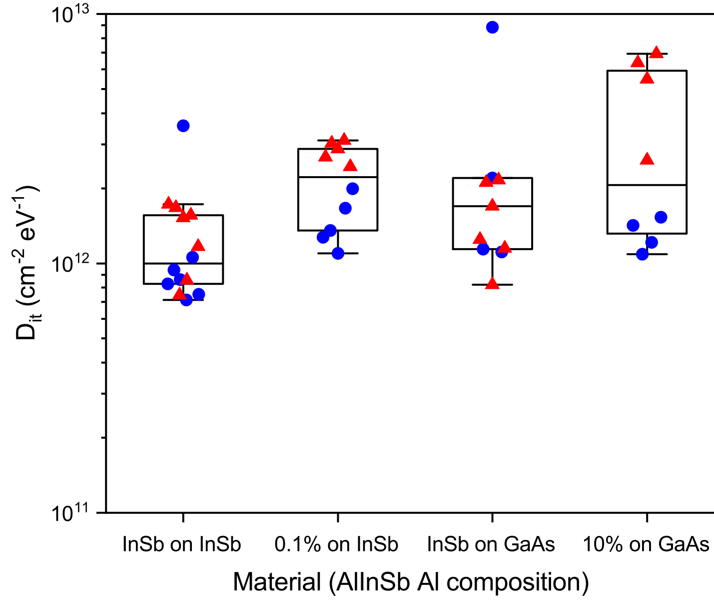


Figure 8.3: Distributions and variability of minimum interface-trapped charge for AlInSb and control samples. Blue circles: D_{it} extracted by the Terman method, red triangles: D_{it} extracted by the conductance method

8.4 AlInSb MOSCAP Devices

After growth, the MOSCAP samples received a 1 min oxide strip in HCl (1:5 37% HCl and deionised (DI) water) and nitrogen blow-dry before being promptly loaded into an Ultratech Fiji ALD reactor. They received 100 cycles (approximately 10 nm) of Al_2O_3 using trimethylaluminium (TMA) and water at 200°C as a thermal Al-first process. The samples were unloaded and promptly loaded into an SVS electron beam evaporator, where they received 1 µm of Al metal as a gate contact. After unloading, the samples were degreased using acetone and isopropanol and pattered using AZ 9260 photoresist as a mask and Microposit MF-319 photoresist developer (dilute tetramethyammonium hydroxide) as an etchant. The samples were diced for characterisation and characterised at a temperature of 80 K using a Leybold RDK 10-320 cryostat with a HP 4155C parameter analyser for I-V measurements and an Agilent E4980A LCR meter for C-V measurements, at frequencies between 1 kHz and 2 MHz. A process flow with additional details is included in appendix A.

The distributions for interface-trapped charge (D_{it}), flatband voltage (V_{FB}) and hysteresis voltage (V_H) are shown in figures 8.3, 8.4 and 8.5.

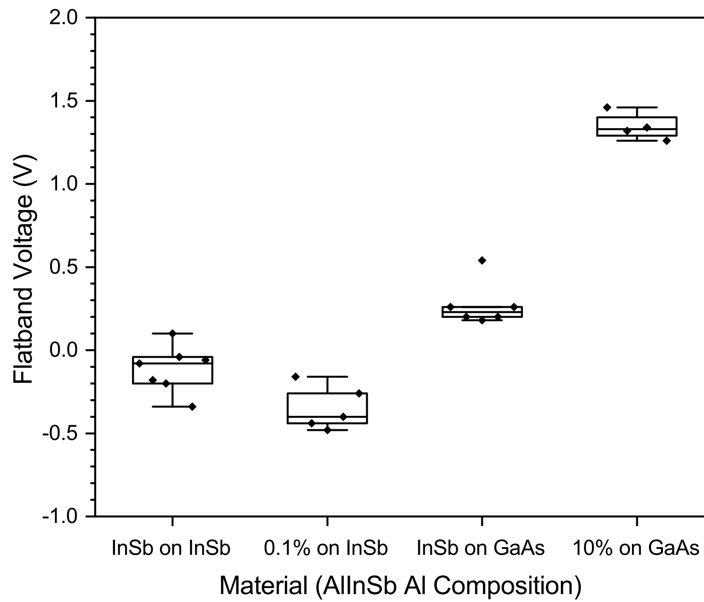


Figure 8.4: Distributions and variability of flatband voltage for AlInSb and control samples

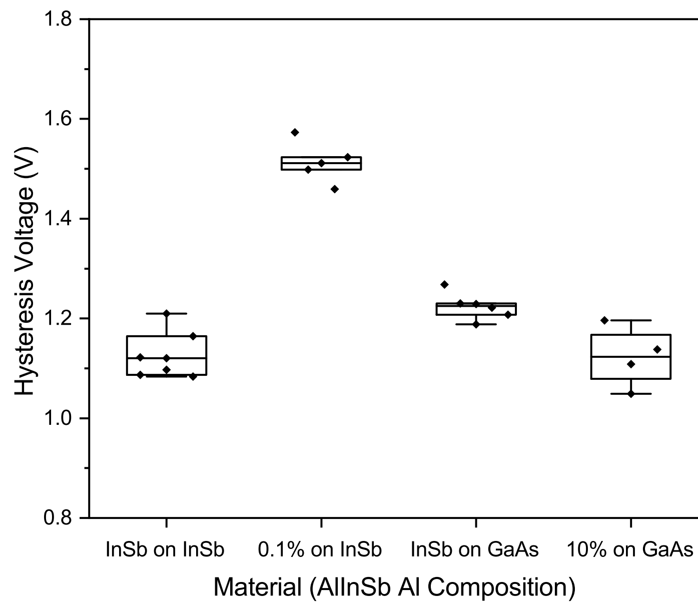


Figure 8.5: Distributions and variability of hysteresis voltage for AlInSb and control samples

8.4.1 Interface-trapped Charge in AlInSb Materials

For the D_{it} shown in figure 8.3, the lowest average D_{it}, 1.28×10^{12} cm^{-2}eV^{-1}, is obtained for InSb on InSb - the system least likely to have formed defects during the growth. Average D_{it} is slightly higher for InSb on GaAs - 2.25×10^{12} cm^{-2}eV^{-1} when an outlier is excluded - which could be attributed to growth defects from lattice mismatch and relaxation. It is similarly high for both AlInSb layers: 2.15×10^{12} cm^{-2}eV^{-1} for 0.1% Al on InSb and 3.33×10^{12} cm^{-2}eV^{-1} for 10% Al on GaAs. However, the number of devices characterised per sample is low (4-7) and the ranges and interquartile ranges intersect for all these samples, however, casting doubt onto the validity of comparisons.

Furthermore, discrepancies can be observed between the data extracted using the Terman and conductance methods: the conductance method gives higher D_{it} than the Terman method for the AlInSb samples and the 10% AlInSb on GaAs gives a discrepancy of 3.60×10^{12} cm^{-2}eV^{-1} between the two methods. This may be related to artefact features, as discussed in section 5.5, or the limited energy range sampled by the conductance method, as discussed in section 7.5 but, as the data from the Terman method shows minimal changes between materials, the conductance method may be capturing an additional effect that is not captured by the Terman method.

Overall, while the current data suggests that growth on mismatched substrates and inclusion of Al may increase D_{it}, the discrepancies between characterisation techniques and high variability relative to the small changes in average D_{it} indicate that further work is required before firm conclusions can be made.

8.4.2 Flatband Voltage in AlInSb Materials

Similarly to D_{it}, the smallest flatband voltage is obtained for InSb on InSb: -0.11 V. Growth on GaAs appears to incorporate fixed charge, resulting in the flatband voltage increasing to +0.27 V. The 10% AlInSb appears to incorporate significantly more fixed charge, shifting V_{FB} to +1.35 V. As the addition of Al to the bulk and interface seemingly results in additional fixed charge, it follows that the charge introduced by growing on GaAs and forming defects from the lattice mismatch would also shift V_{FB} by a smaller amount, as demonstrated by the data from the InSb on GaAs sample. Alternatively, the apparent shift in V_{FB} may be a consequence of the semiconductor work function changing as Al is added. Metal-semiconductor work function differences are not accounted for in analysis, and may be contributing to the observed shift in V_{FB}.

The 0.1% AlInSb sample on InSb also demonstrates a shift relative to the InSb

on InSb control, but in this case, the shift is negative. The cause for this is not immediately clear, and the shift is small enough that it borders on significance, but it may be related to the strain in the material. The samples grown on GaAs were in compressive strain and entirely relaxed, whereas the 0.1% AlInSb grown on InSb is in tensile strain. While the addition of strain may not account for a change in fixed charge, the discrepancy in feature size in the AFM images supports the supposition that the two samples grown on InSb are not identical - the 0.1% AlInSb may be partially relaxed. Relaxation may have introduced charge defects and these may have been negatively charged, as opposed to the positive charge apparent in the samples grown on GaAs. Alternatively, the features in the AFM images may indicate that the InSb on InSb contains defects from a different source (e.g. insufficient removal of the native oxide) that the incorporation of Al may have counteracted.

8.4.3 Hysteresis in AlInSb Materials

The 'optimal' InSb on InSb displays hysteresis voltage approximately in line with the 10% AlInSb on GaAs: 1.13 V and 1.12 V, respectively. The InSb on GaAs displays slightly higher hysteresis - 1.22 V - with significantly reduced variability, suggesting the shift is significant. If the increase relative to the InSb on InSb is attributed to growth defects and the propagation thereof causing slow trapping, then it follows that the addition of Al reduced hysteresis back to the minimum displayed by the InSb on InSb. This is consistent with the attribution of hysteresis to diffusion of substrate elements into the oxide (as discussed in section 2.7 - increased bond enthalpy inhibits diffusion) but inconsistent with the results demonstrated by the 0.1% AlInSb sample.

The 0.1% AlInSb sample displays significantly increased hysteresis: 1.51 V. This shift is significantly larger than the shifts between other samples and its source is not immediately apparent. As discussed in sections 8.2.2 and 8.4.2 above, some discrepancies between the InSb on InSb sample and the 0.1% AlInSb on InSb have been observed, predominantly in surface decoration, as shown in section 8.2.2, but section 8.4.2 also observes apparently contradictory trends between samples on InSb and samples on GaAs. Section 8.4.2 discusses two possible explanations: that the InSb on InSb sample includes growth defects that are reduced by the addition of Al and that the addition of Al induces sufficient tensile strain to cause partial relaxation and/or charged states to form. The second explanation is preferred for the V_H results: the offsetting of existing states by additional states is not conventionally discussed in the context of hysteresis states, whereas defect states from tensile strain

are likely to contribute towards trapping in hysteresis.

8.5 Conclusion and Further Work

A snapshot study into AlInSb-dielectric interfaces has been performed. Low Al incorporation in nominally lattice-matched material has produced changes in surface morphology, imaged by AFM, although further investigation is required to confirm this result. The addition of Al into both low-strain and relaxed material produced small increases in D_{it} but a larger sample size is needed to confirm the significance of these results. V_{FB} and V_H show contradictory results for AlInSb on InSb and on GaAs. The most likely source of these contradictory results is tensile strain in AlInSb on InSb, as opposed to the compressive strain in (Al)InSb on GaAs.

Further work is immediately recommended into wider Al compositions. A study covering 0% to 20% or 25% Al on GaAs would allow clearer identification of the role of Al and the trends associated with increasing Al composition. To further characterise the discrepancies between the samples grown on InSb and those grown on GaAs, a study into variable Al composition on InSb may enable distinction between Al-related effects and effects related to tensile strain, particularly if electrical measurements were complemented with AFM characterisation to track material defects and surface decorations.

Chapter 9

Alternative Dielectrics

9.1 Introduction

This thesis has so far focused exclusively on aluminium oxide as a dielectric. As discussed in section 2.2, aluminium oxide has shown good interfaces with III-V materials and low interface-trapped charge density (D_{it}) but its bulk properties, such as dielectric constant, compare unfavourably with other materials, such as hafnium oxide. Furthermore, the high hysteresis shown by devices in chapters 6, 7 and 8 has proven challenging to reduce and an assessment on whether alternative dielectrics could offer lower hysteresis could offer invaluable guidance in process development.

The deposition instrument used for this study - an Ultratech Fiji - was equipped with source materials for three metals and two co-reactants: trimethylaluminium (TMA) as an aluminium source; diethylzinc (DEZ) as a zinc source; tetrakis(dimethylamino)hafnium (TDMAH) as a hafnium source; water, O_2 plasma and ozone as oxygen sources and N_2 plasma as a nitrogen source. As aluminium oxide (Al_2O_3) has already been studied and zinc oxide (ZnO) is a semiconductor rather than a dielectric, recipes were sourced (from Veeco, on behalf of Ultratech) to deposit aluminium nitride (AlN) and hafnium oxide (HfO_2). While the recipes were not optimised for the specific ALD system, the deposited materials provided an additional snapshot study comparing AlN and HfO_2 to Al_2O_3.

9.2 Experimental Methodology

Material from two 2" (~50 mm) Te-doped n-type wafers of InSb with a carrier concentration of approximately 8×10^{14} cm^{-3} n-type was prepared. The wafers were cleaved into quarters and three quarters were taken for processing. The samples each received an oxide strip in HCl (1:5 37% HCl and deionised (DI) water) and

Table 9.1: ALD process parameters for Al2O$_3$, AlN and HfO$_2$

Dielectric	Metal Precursor Dose (s)	Metal Precursor Purge (s)	Co-reagent Dose (s)	Co-reagent Purge (s)	Plasma Power (W)
Al_2O_3	0.06	8	0.06	8	N/A
AlN	0.06	5	20	5	300
HfO_2	0.25	5	6	5	300

nitrogen blow-dry before being promptly loaded into an Ultratech Fiji ALD reactor. One sample was prepared as a control and underwent deposition of 100 cycles (approximately 10 nm) of Al_2O_3 using trimethylaluminium (TMA) and water at 200°C as a thermal Al-first process. Another sample received 200 cycles (approximately 10 nm, with roughly half the deposition rate of Al_2O_3) of AlN deposition using TMA and N_2 plasma at 250°C as a plasma Al-first process. The final sample received a TMA pretreatment of 10 cycles, followed by 100 cycles (approximately 10 nm) of HfO_2 using tetrakis(dimethylamino)hafnium (TDMAH) and O_2 plasma at 200°C as a plasma Hf-first process. This process was designed to ensure low DC leakage, following the leakage results in section 6.4, and to emulate Trinh *et al.*[38], which represents the best result found in the literature, as discussed in chapter 2 (section 2.2.4). The ALD process parameters are listed in table 9.1.

Following dielectric deposition, all samples were unloaded and transferred promptly to an SVS electron beam evaporator, where they received 1 µm of Al metal as a gate contact. After unloading, the samples were degreased using acetone and isopropanol and pattered using AZ 9260 photoresist as a mask and Microposit MF-319 photoresist developer (dilute tetramethyammonium hydroxide) as an etchant. The samples were diced for characterisation and characterised at a temperature of 80 K using a Leybold RDK 10-320 cryostat with a HP 4155C parameter analyser for I-V measurements and an Agilent E4980A LCR meter for C-V measurements, at frequencies between 1 kHz and 2 MHz.

9.3 Results and Discussion

The distributions for leakage current density (J_L) at -5 V (the maximum applied voltage), interface-trapped charge (D_{it}), flatband voltage (V_{FB}), hysteresis voltage (V_H) and frequency dispersion are shown in figures 9.2, 9.3, 9.4 and 9.5. The Terman and conductance D_{it} data is generally consistent, in contrast with the results in sections 7.5 and 8.4.1.

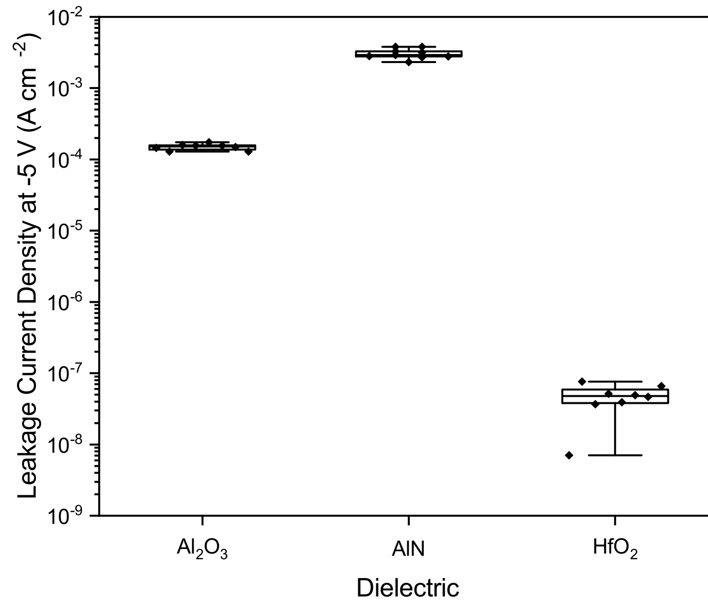


Figure 9.1: Distributions and variability of DC leakage current density at -5 V for different dielectrics

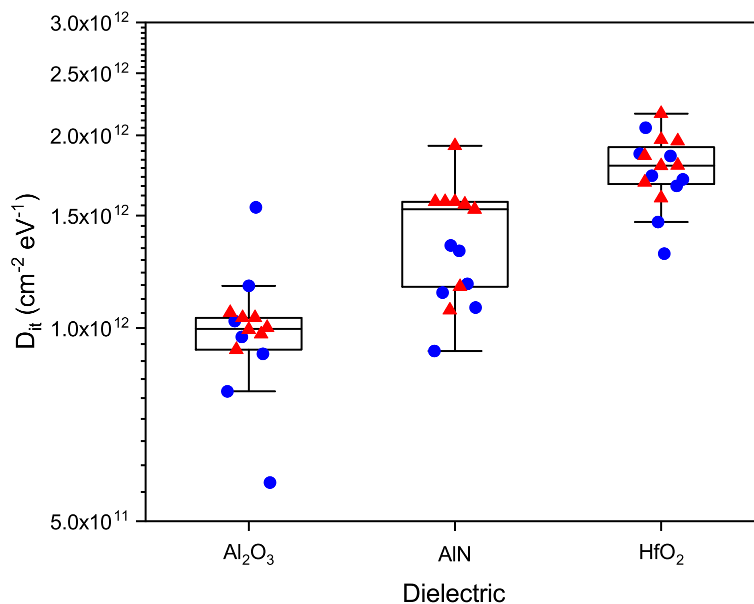


Figure 9.2: Distributions and variability of minimum interface-trapped charge for different dielectrics. Blue circles: D_{it} extracted by the Terman method, red triangles: D_{it} extracted by the conductance method

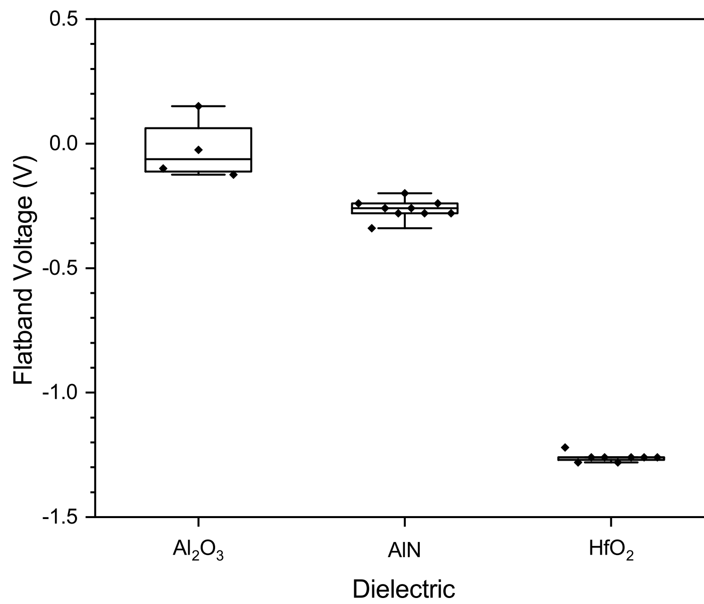


Figure 9.3: Distributions and variability of flatband voltage for different dielectrics

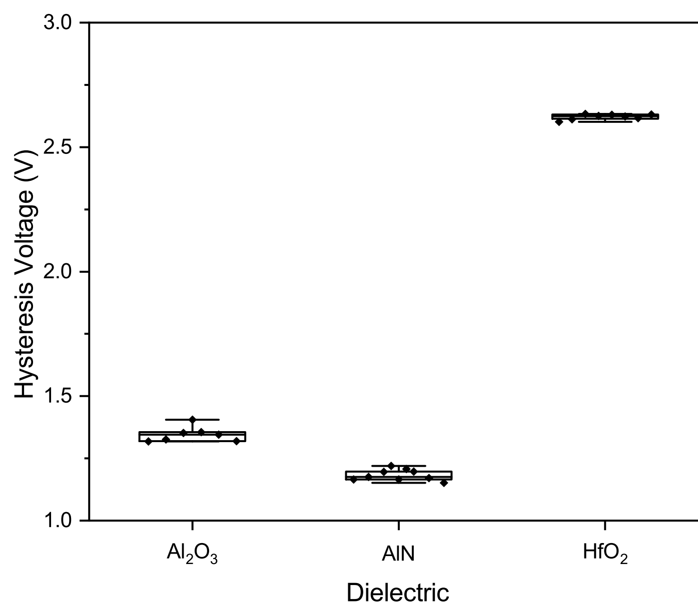


Figure 9.4: Distributions and variability of hysteresis voltage for different dielectrics

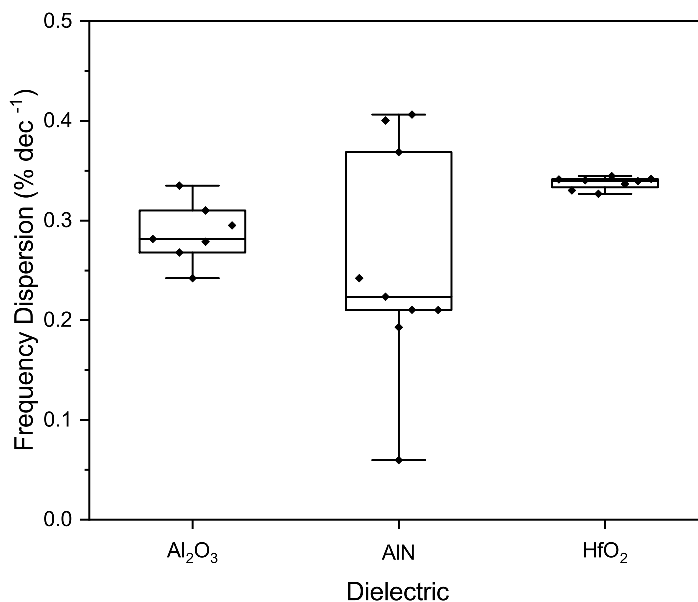


Figure 9.5: Distributions and variability of frequency dispersion for different dielectrics

9.3.1 Aluminium Nitride

When compared to Al_2O_3, AlN has noticeably increased J_L, from 1.5×10^{-4} A cm^{-2} to 3.1×10^{-3} A cm^{-2}. This is most likely be due to oxygen content in the dielectric, producing states in the oxide which form a leakage path. Despite precautions taken to reduce oxygen content - pre-conditioning the reaction chamber with a 20 nm layer of AlN to getter oxygen, waiting for the sample load lock to pump to good vacuum before loading and using an oxygen getter on the source N_2 - residual oxygen may have desorbed from existing oxides/deposits on the chamber wall, may have been present in precursors or gas lines or may have been sputtered from the quartz plasma tube. This may be reduced by further chamber/system conditioning, such as a bake out procedure, and/or by substituting the quartz plasma tube for an alumina tube, less susceptible to sputter damage.

When compared to Al_2O_3, AlN has slightly increased D_{it}, from 1.0×10^{12} cm^{-2}eV^{-1} to 1.4×10^{12} cm^{-2}eV^{-1}, when outliers are neglected. It is difficult to determine whether this change is significant, as the sample size is small for both processes, but the interquartile ranges of the two processes do not overlap, suggesting that the result is significant. Three outliers were observed in the AlN sample (not shown in figure 9.2), with an average of 2.2×10^{13} cm^{-2}eV^{-1}. The conductance method gives a slightly higher average D_{it} for the AlN sample than the Terman method - 1.5×10^{12} cm^{-2}eV^{-1} compared to 1.2×10^{12} cm^{-2}eV^{-1}, when Terman outliers are

neglected - but the data from the two methods overlaps significantly and additional data would be required to demonstrate that the methods are inconsistent.

When compared to Al_2O_3, AlN has a slightly greater V_{FB}, increased from -0.03 V to -0.26 V. The Al_2O_3 sample has a very small sample size, only 4 valid devices, but the ranges of the two datasets do not overlap. By contrast, V_H is improved in AlN compared to Al_2O_3, from 1.35 V to 1.18 V. The frequency dispersion results for the AlN sample are inconclusive: the 9 data points gathered are grouped in two regions, 3 data points are grouped with an average of 0.39 % dec^{-1}, 5 data points are grouped with an average of 0.22 % dec^{-1} and one outlier occurs at 0.06 % dec^{-1}. The largest group indicate decreased frequency dispersion compared to Al_2O_3 but further data must be gathered to reliably identify the 'true' average and distribution of frequency dispersion in AlN.

In chapter 2 (section 2.2.6), the properties of AlN were discussed in comparison to Al_2O_3. Krylov *et al.*[46] report reduced D_{it} for AlN on InGaAs, when compared to Al_2O_3, contradicting the results obtained here, but the results are not directly comparable. Krylov *et al.* performed all ALD processes at 300°C on InGaAs, eliminating the effect of temperature, but, for the results presented here, ALD was performed at 200°C for Al_2O_3 and at 250°C for AlN. Furthermore, it is demonstrated in chapter 6, section 6.3 that increasing the deposition temperature from 200°C to 250°C for InSb substrates results in increased D_{it} for otherwise identical processes. The D_{it} increase from increased temperature in chapter 6 was 2.0×10^{12} $cm^{-2}eV^{-1}$ - this is larger than the change between Al_2O_3 and AlN shown here, suggesting that the increase in D_{it} from increasing temperature may have been offset by a decrease from changing dielectric material.

The AlN displays greater flatband voltage and decreased hysteresis. Existing literature (Krylov *et al.*[46] but also Luc *et al.*[48]) states that AlN is susceptible to oxidation but indicates that it provides a superior diffusion barrier to Al_2O_3. It is possible that reduced diffusion resulted in decreased hysteresis (and the lower frequency dispersion in the largest group of values) but surface oxidation before gate metal deposition resulted in greater flatband voltage (introducing negative charge).

9.3.2 Hafnium Oxide

When compared to Al_2O_3, HfO_2 has significantly decreased J_L, from 1.5×10^{-4} A cm^{-2} to 4.7×10^{-8} A cm^{-2}. As discussed in section 6.4, this is likely to be due to increased density of the oxide film, compared to thermal processes. When comparing these results to Al_2O_3 and estimating whether like-for-like processes would offer similar leakage, the plasma HfO_2 at 200°C is approximately in line with the 100°C plasma

Al_2O_3 process demonstrated in section 6.4. This suggests that thermal HfO_2 should offer J_L in line with thermal Al_2O_3 and and suitable for further study.

When compared to Al_2O_3, HfO_2 has slightly increased D_{it}, from 1.0×10^{12} cm^{-2}eV^{-1} to 1.8×10^{12} cm^{-2}eV^{-1}. The only intersection between the two sample ranges is one outlier data point and the Terman and conductance methods are in good agreement. When V_{FB} and V_H are compared, a significant increase is observed in both parameters for the HfO_2 sample. The flatband voltage for the reverse voltage sweep is not shown but is unchanged between the Al_2O_3 and the HfO_2 - 1.33 V and 1.36 V, respectively - suggesting that the difference in forward V_{FB} and V_H may be due to 'slow' hystersis states only. The frequency dispersion is slightly increased for the HfO_2 sample, from 0.29 % dec^{-1} to 0.34 % dec^{-1}, and the ranges overlap by only one point.

Due to the TMA pretreatment and presumed interfacial layer (see Trinh *et al.*[38]), the observed increase in D_{it} is unexpected, as the high-quality interface should have been retained by the interfacial layer. This suggests that the details of the TMA treatment and thickness of the ensuing interfacial layer may still affect D_{it} and that further study into the number of TMA half-cycles and/or Al_2O_3 cycles may reveal an optimum interfacial process.

The increase in V_H is very large and striking. HfO_2 is assumed to offer a superior diffusion barrier compared to Al_2O_3, which would result in decreased hysteresis, rather than the observed increase. A possible cause of the increased hysteresis is the reduced deposition temperature compared with HfO_2 processes reported in the literature, and subsequent reduction in deposition energetics. In existing literature, the preferred deposition temperature for HfO_2 is generally 250°C[38][48][52][86] or higher[77][80][88][89] and the reduced deposition temperature of 200°C may have induced defect states capable of increasing hysteresis. Further study to establish the differences between thermal and plasma processes may provide additional insight.

9.4 Conclusion and Further Work

A brief comparison has been made between Al_2O_3, AlN and HfO_2 dielectrics on InSb. AlN gave increased J_L (probably due to oxygen content), slightly improved hysteresis and, while D_{it} increased slightly, this effect may be due to increased deposition temperature. The frequency dispersion results for AlN were inconclusive, with values grouping around 0.39 % dec^{-1} and 0.22 % dec^{-1}. HfO_2 gave significantly decreased J_L (probably as a result of the plasma deposition process), slightly increased D_{it} and frequency dispersion and significantly increased hysteresis. These changes,

particularly increased hysteresis, may be due to the reduced deposition temperature compared with the literature, as HfO_2 is commonly deposited at 250°C or higher, or may be related to the difference between thermal and plasma processes.

The immediate recommendation for further work is to generate a matrix of results which covers Al_2O_3, AlN and HfO_2 at a range of deposition temperatures and for both thermal and plasma processes. A like-for-like comparison may represent AlN and HfO_2 more fairly, separating the effects of temperature, dielectric and thermal/plasma deposition but also ensuring each dielectric can be demonstrated in ideal deposition conditions. An impediment to this study is that the standard recipes (provided by Veeco, on behalf of Ultratech) only detail AlN deposition using N_2 plasma at 250°C - further investigation may be necessary into whether AlN can be deposited at 200°C and into the optimal process for such a deposition. Additional dielectric materials might also be worth investigating, such as hafnium nitride, silicon dioxide (SiO_2), silicon nitride (Si_3N_4) etc.

Chapter 10

Conclusion and Recommendations for Further Work

Indium antimonide (InSb) is a narrow bandgap semiconductor material which shows great promise for mid-infrared emitters and detectors, ultra-high speed switching devices and emerging quantum technologies. Despite this promise, its application is hindered by lack of a suitable dielectric process for surface passivation and gate control.

10.1 Conclusions

A literature review has been performed and, based on review findings, a series of experimental studies have been performed. A modelling and analysis framework has been established and tailored to InSb. Experimental work has covered HCl wet pre-treatments, in-situ plasma pre-treatments, post-deposition annealing, AlInSb substrates and a range of deposited dielectrics.

10.1.1 Literature Review

Existing literature on narrow bandgap III-V interfaces focuses predominantly on $In_{0.53}Ga_{0.47}As$, occasionally on InAs and GaSb, rarely on InSb and barely ever on AlInSb. Previously-studied SiO_2 and Ga_2O_3/Gd_2O_3 have been eschewed recently in favour of Al_2O_3 and HfO_2, deposited by atomic layer deposition (ALD) - Al_2O_3 for its low density of interface traps (D_{it}) and HfO_2 for its high dielectric constant and resistance to diffusion. La_2O_3 and AlN have been investigated as an alternative route to low D_{it} but offer marginal benefit over Al_2O_3 interfaces. In addition to 'fast' traps (D_{it}), 'slow' traps can introduce hysteresis and frequency-dependent effects which

are similarly detrimental to practical devices and are as important as D_{it}, if not more so, in demonstrating high-quality dielectrics.

The preferred III-V wet treatments are sulphidation, HCl and, occasionally, ammonium hydroxide, although degradation has been observed in sulphidation treatments. Some gaseous precursors have demonstrated 'self-cleaning' effects and formed beneficial interfacial layers. Plasma pre-treatments have been demonstrated on III-V materials with dramatic improvements, particularly on GaSb and GaN where D_{it} is decreased by more than an order of magnitude. Post-deposition processes are difficult to compare to InSb, due to its low melting point and non-congruent transition at ~325°C, but may offer routes to decreased D_{it} and/or 'slow' traps. Characterisation methods have individual benefits and shortcomings and may offer more reliable characterisation when applied in parallel. AlInSb has rarely been studied but might offer lower hysteresis and/or D_{it} than pure InSb.

10.1.2 Modelling and Analysis

A modelling and analysis suite was built, optimised and verified. Peculiarities of III-V band structure - nonparabolicity in the conduction band minimum at the Γ point and contributions from higher minima at the L and X wavevectors - were accommodation in the model. These accommodations were verified using Moss-Burstein data from existing literature (Zawadzki[104]). Analysis produces several figures of merit, most notable interface-trapped charge density (D_{it}), flatband voltage (V_{FB}) and hysteresis voltage (V_H). A correction is required to extract C_{ox} from measured C-V data, using C_S values from the implemented model to correct for the effect of low carrier concentration.

High-field effects are exacerbated by the narrow bandgap of InSb and influence device performance and characterisation under commonly-used conditions that would be stable for materials with a wider bandgap. Zener tunnelling and impact ionisation across the depletion region were investigated and quantified, confirming that material with a carrier concentration greater than $\sim 10^{16}$ cm^{-3} will be affected by these phenomena. The effect of quantisation in the conduction band in high electric fields was investigated using a freeware Schrödinger-Poisson solver and its impact of accumulation capacitance and the new C_{ox} extraction method may necessitate further work.

10.1.3 Pre-treatments

A study was performed into HCl wet treatments and interfacial layers of $InCl_3$ produced by them. X-ray photoelectron spectroscopy (XPS) revealed that an $InCl_3$ layer forms only when the HCl is diluted in and rinsed with isopropanol (IPA) and that it desorbs most significantly between 200°C and 250°C. MOSCAPs were prepared using HCl-water and HCl-IPA processes with ALD depositions at 200°C and 250°C. The $InCl_3$ layer, produced by the HCl-IPA process, was associated with a V_{FB} shift of +0.79 V - a shift that was entirely eliminated by desorbing the layer with increased deposition temperature or by treating instead with HCl-water. It was found that any HCl treatment reduced V_H relative to the control, from 1.4 V to a minimum of 1.1 V, but other figures of merit were unaffected. The increased deposition temperature was associated with deterioration in all figures of merit. These results build on the findings in existing literature on XPS[65] and MOSCAPs[34], showing a clear connection between $InCl_3$ and V_{FB}.

Plasma pre-treatments with Ar and Ar/H_2 were generally associated with deterioration in all figures of merit but particularly increased DC leakage current. These results contradict results from other plasma processes, which demonstrate improved performance, particularly in D_{it}[79][82][83]. Within the experimental data, some discrepancies exist but they may be due to variable contamination between facilities. When a plasma-enhanced ALD process (using O_2 plasma as an oxygen precursor) performed at 100°C was compared to a thermal ALD process at 200°C, the plasma process offered a seemingly increased oxide density, a lower DC leakage, reduced D_{it}, reduced V_H and increased V_{FB} - further work must be done to isolate the effects of changing deposition temperature and ALD co-reactant

10.1.4 Annealing

A series of post-metallisation anneal processes were studied. Material breakdown was observed for anneal doses above 400°C, 5 mins, with transmission electron microscopy (TEM) showing the formation of interfacial layers and electrical characterisation showing the breakdown of classical features into frequency-dependent behaviour only, followed by an apparent change to p-type material.

Below the breakdown anneal dose, optima in D_{it}, V_{FB} and V_H were observed around 300°C, 1 hr for N_2, O_2 and forming gas anneal processes. The largest improvements were observed in V_H and V_{FB}, improving from 1.38 V to 0.72 V and from -1.05 V to -0.68 V, respectively, and smaller, marginally-significant, improvements were observed for D_{it}. For thermal doses above this optimum, the figures of merit

deteriorated by approximately a factor of 2 and/or the variability within samples increased similarly.

10.1.5 AlInSb

A snapshot study was performed on InSb and $Al_{0.1}In_{0.9}Sb$ as relaxed materials on GaAs substrates and on InSb and $Al_{0.001}In_{0.999}Sb$ as high quality/strained materials on InSb. Al composition was associated with increased D_{it} but contradictory results were observed for 10% Al composition on GaAs and for 0.1% Al composition on InSb. These results may be due to the difference in compressive and tensile strain for materials on GaAs and InSb, respectively. This explanation is supported by atomic force microscopy characterisation, which shows a contrast in surface feature size (assumed to be decorations from material defects) for InSb and $Al_{0.001}In_{0.999}Sb$ on InSb, suggesting that relaxation may have occurred in the $Al_{0.001}In_{0.999}Sb$.

10.1.6 Dielectrics

A brief study was performed to compare Al_2O_3, AlN and HfO_2 dielectrics. AlN gave slightly improved hysteresis and, while D_{it} increased slightly (from 1.0×10^{12} cm^{-2}eV^{-1} to 1.4×10^{12} cm^{-2}eV^{-1}), this effect may be due to increased deposition temperature: 250°C for AlN, compared to 200°C for Al_2O_3. The frequency dispersion results for AlN were inconclusive, with two groups of values around 0.39 % dec^{-1} and 0.22 % dec^{-1}. HfO_2 gave slightly increased D_{it} (from 1.0×10^{12} cm^{-2}eV^{-1} to 1.8×10^{12} cm^{-2}eV^{-1}) and frequency dispersion (from 0.29 % dec^{-1} to 0.34 % dec^{-1}) and significantly increased hysteresis (from 1.35 V to 2.62 V). This may be due to the deposition temperature of 200°C being unsuitable for HfO_2, as HfO_2 is commonly deposited at 250°C or higher. These results conflict with results in the existing literature, which show reduced diffusion in HfO_2, which should give reduced slow charge[38][39], and high-quality HfO_2-based dielectrics have been previously demonstrated for InSb[38]

10.2 Comparison to Existing Systems

For the InSb MOSCAPs studied in this thesis, the best D_{it} results are approximately 8×10^{11} cm^{-2}eV^{-1} and the best V_H results are approximately 0.7 V. A typical HfO_2-Si MOSCAP can be expected to have a minimum D_{it} of approximately 1×10^{11} cm^{-2}eV^{-1} and a V_H of less than 0.1 V[131], with state-of-the-art silicon systems likely offering slightly improved performance.

For D_{it}, the InSb technologies studied in this thesis are at least in-line with III-V technologies such as $In_{0.53}Ga_{0.47}As$ and GaSb, as summarised in appendix **??**. In particular, other III-V technologies show a discrepancy between characterisation using the Terman and conductance methods, with the Terman method reporting D_{it} values up to an order of magnitude greater than the conductance method, whereas the InSb devices characterised in this thesis show minimal discrepancy between the two methods. This gives increased confidence in the D_{it} results from InSb. The best InSb devices in this thesis are also within an order of magnitude of typical HfO_2-Si devices, suggesting InSb is close to competing with Si technologies for D_{it}. It must be noted, however, that the InSb devices in this thesis have only been characterised at a temperature of 80 K, and additional work to characterise InSb MOS technology at room temperature (using radio frequency techniques) may offer a different comparison.

For V_H, the InSb devices in this thesis are significantly lagging Si technology. While a like-for-like comparison - using the same oxide thickness, DC voltage range and temperature - is not possible using literature data, the devices in this thesis appear to have V_H more than an order of magnitude greater than Si technology. Reducing V_H must be a key objective if InSb technology is to compete with Si.

For V_{FB}, there is not a specific target for the value of V_{FB}. Rather, a technology must offer V_{FB} close to zero, to minimise transistor threshold voltage, and must offer manipulation to enable fine tuning and selection of depletion/enhancement mode device operation. The devices in this thesis have demonstrated both V_{FB} close to zero (e.g. sections 6.4 and 8.4) and V_{FB} manipulation using wet cleaning (section 6.3) and plasma processes (section 6.4). Further manipulation may be possible using other techniques (e.g. fluorine-doping of ALD films[132]) but the present state of the technology offers good control of V_{FB}.

10.3 Recommendations for Further Work

A series of further studies are suggested in sections 6.5, 7.7, 8.5 and 9.4. Most notably:

- Additional investigation into plasma treatments, using XPS and/or further exploration of ‘parameter space’, may identify the deterioration mechanisms.
- Additional investigation into thermal/plasma ALD processes at 100°C/200°C to isolate the effects of changing process temperature and co-reactant.

- Study into anneal treatments after deposition but before metallisation and comparison vs. post-metallisation processes.
- Study into rapid thermal annealing as a route to more effective chemical action, using increased temperature to increase gas energetics without exposing the material to large thermal doses.
- Study into a wider range of Al composition of AlInSb, using both GaAs and InSb substrates to isolate strain effects.
- Further investigation into deposition temperature/co-reactant effects for Al_2O_3, AlN and HfO_2, to isolate these effects from changes in dielectric material.

The work in this thesis has focused exclusively on n-type substrates. P-type InSb is not as readily available as n-type InSb and sample preparation may require epitaxial growth and fine-tuning of background doping and dopant flux to prevent high-field effects, as discussed in section 5.6. Untreated p-type InSb MOSCAPs, not shown in this thesis, have displayed very high frequency dispersion but may be improved by post-deposition annealing or other processes studied in this thesis.

In addition to specific studies on specific process elements, dielectric processes for InSb have yet to be integrated into practical devices. Gated MOSFET devices are a practical device structure that would be enabled by a high-quality dielectric process but conventional lateral MOSFET structures are unsuitable for InSb at room temperature. Gated quantum well devices, such as those presented by Ashley *et al.*[127] but with a MOS gate instead of a Schottky barrier gate, should offer effective modulation between on-state and off-state at room temperature and more useful transistor devices. An initial attempt to fabricate a quantum well MOSFET is included in appendix C but channel modulation was limited to only 14%. Further investigation into these results and structures may demonstrate a route to resolve this issue and produce practical and useful transistor devices. Such devices may be viable for commercialisation but would also be useful as a vehicle to study gate control for other applications (such as quantum devices).

An alternative practical device enhancement enabled by an effective dielectric process would be diode surface passivation. The dielectric process could be applied to planar samples following wet and dry etch processes to study the effect of etch-and-passivate processes on standard MOSCAP figures of merit: D_{it}, V_{FB}, V_H, frequency dispersion etc. The dielectric process could be applied directly to etched diode devices and standard diode figures of merit (e.g. differential resistance at zero bias, R_0, measured for a range of perimeter:area ratio), could be used to assess the

effectiveness of surface passivation directly. For low-damage processes, this may necessitate additional patterning of diode devices to raise the surface-to-volume ratio sufficiently to identify etch damage and the effect of passivation.

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Appendix A

MOSCAP Fabrication and Characterisation Process Flow

A.1 Introduction

This document details the full standard fabrication and test process for metal-oxide-semiconductor capacitor (MOSCAP) test devices. This process has been developed for indium antimonide (InSb) but can be applied to other materials (e.g. AlInSb, GaSb, GaInSb).

The process begins with a planar wafer. The process is written for bulk material but the mask set and process flow are suitable for epi material too. The wafer is first cleaned and a dielectric layer deposited. Gate metal is then deposited and a metal etch used to define gate metal pads. This mask provides some usable test structures without depositing ohmic contact metal. A post-deposition anneal is to be used as standard, once a suitable process is proven. Contact metal is deposited after annealing and a photoresist mask is used to both open up contact holes in any remaining oxide and pattern ohmic contact metal by lift-off. Gold is used in the ohmic contact and no post-metallisation annealing is performed. The wafer can then be diced and samples prepared for testing in the closed-cycle cryostat. A separate user manual is provided for operating the cryostat. figure A.1 shows the two MOSCAP designs in cross-section. The 'lateral' structure (left) relies on a series measurement of the MOSCAP pad and MOS field being dominated by the smaller MOSCAP pad. The 'ohmic' structure (right) uses an ohmic contact ring around the MOSCAP pad.

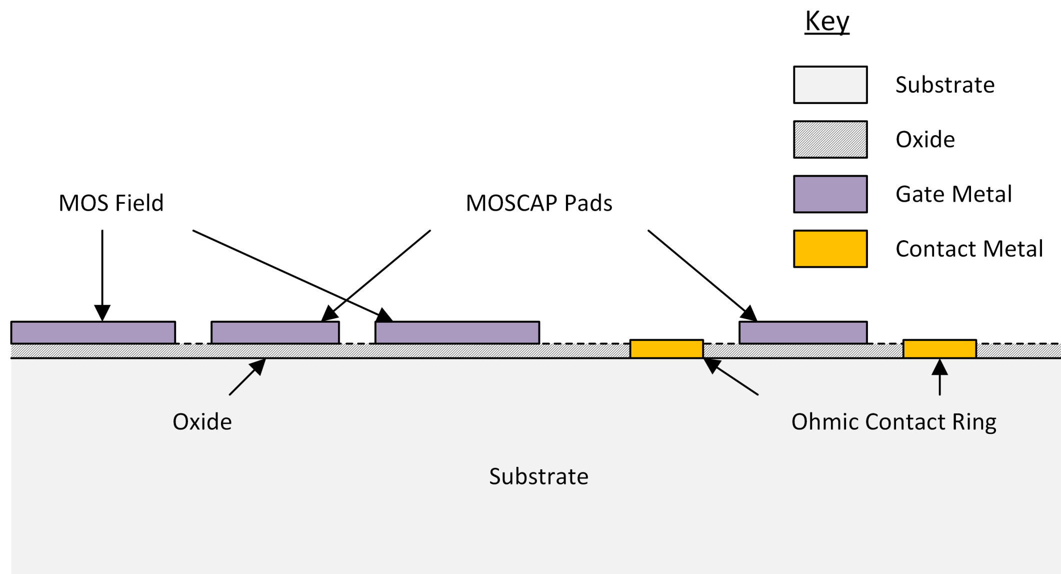


Figure A.1: Cross-section view of MOSCAP structures

A.2 Wafer Cleaning

If wafer is visibly contaminated, perform solvent clean.

a Soak in acetone for 20 seconds, wash with acetone bottle and transfer to IPA

b Soak in IPA for 20 seconds

c Blow dry using nitrogen gun

d Optical inspection for contamination

e Heat wafer on a pre-heated hot plate for 3 minutes at 110±5°C, cool to 21±2°C

Before dielectric deposition, perform acid clean. Prepare solution and measure witness sample (see section A.3 Dielectric Deposition) in advance and transfer to deposition chamber as quickly as possible to prevent re-oxidation of the surface.

a Measure 80 ml dilutant (water or IPA) into etch beaker

b Add 20 ml HCl into etch beaker

c Prepare rinse (use same as etch dilutant)

d Measure temperature

e Load sample(s) into etch basket and immerse

f Agitate samples moderately

g Etch for 30 seconds or until effervescence stops

h Remove basket, rinse and blow dry using nitrogen gun

i Load into deposition chamber immediately

A.3 Dielectric Deposition

The standard dielectric process is 10 nm of Al_2O_3 deposited by atomic layer deposition (ALD). Two variants of the process are used: one for the Oxford Instruments OpAL at the University of Liverpool and one for the Ultratech Fiji at the University of Warwick. Both processes include a silicon 'witness' sample for process monitoring and control.

A.3.1 University of Liverpool, Oxford Instruments OpAL

Before cleaning the wafer, prepare a silicon witness sample

a Cleave out small silicon piece (e.g. 1 cm square)

b Load onto ellipsometer

c Run measurement

d Save ellipsometry data

Perform standard cleaning procedure (see section A.2) on wafer, load and run.

a Open deposition chamber

b Load wafer and Si witness sample

c Close and pump chamber

d Run deposition recipe

e Once completed, unload wafer and Si witness sample

f Measure Si witness sample using ellipsometry. Use initial measurement as substrate to model deposited dielectric thickness

g Catalogue Si witness sample for future reference

A.3.2 University of Warwick, Ultratech Fiji

Before processing, ensure the ALD reactor is turned on and, before cleaning the process wafer, prepare a silicon witness sample

a Cleave out small silicon piece (e.g. 1 cm square)

b Ensure the ALD reactor is turned on, that the heaters are on and that they are at or close to their setpoints

c Check that the sample platten is in the load lock. If it is not, pump the load lock and transfer the platten

d Vent the chamber and load the Si witness sample. Close the lid to prevent particulates from entering the load lock

Once the witness sample and chamber are ready, perform standard cleaning procedure (see section A.2) on wafer, load and run.

a Load wafer, close the load lock and pump the load lock

b Once the pump procedure is complete, transfer the platten to the reactor chamber. Monitor the process through the load lock window to ensure the transfer does not fail

c Select and run the required recipe (e.g. 'Al2O3 200C - Thermal')

d When the process is nearing completion, run the calibration/baseline procedure on the Filmetrics interferometer

e Once completed, transfer platten back to load lock and unload wafer and Si witness sample

f Measure both the wafer and the Si witness sample using the Filmetrics interferometer and the appropriate model (e.g. 'Al2O3 on InSb'). Save the acquired spectra

A.4 Gate Metal Patterning

After dielectric deposition, deposit metal, spin on & pattern resist and use a metal etch to pattern the metal. The standard gate metal is 950 nm of aluminium, patterned using AZ 9260 photoresist and MF 319 developer as an etchant.

A.4.1 Metal Deposition

Before depositing metal, degrease the wafer to aid adhesion

a Soak in acetone for 20 seconds, wash with acetone bottle and transfer to IPA

b Soak in IPA for 20 seconds

c Blow dry using nitrogen gun

d Optical inspection for contamination

e Heat wafer on a pre-heated hot plate for 3 minutes at 110±5°C, cool to 21±2°C

Load promptly to the metal deposition tool.

a Load wafer into SVS E2000LL metal evaporator

b Deposit Al using recipe "Al950nm"

c On completion unload the wafer from the SVS E2000LL

A.4.2 Photoresist Patterning

For the standard Al etch in MF 319 solution, use AZ 9260 resist. Once the resist is deposited, do not remove the wafer from the yellow room until the etch is complete, as exposed AZ 9260 will still etch in MF 319 Resist: AZ 9260 Developer: AZ 726 MIF

a Heat wafer on a pre-heated hot plate for 3 minutes at 110±5°C, cool to 21±2°C

b Continue processing immediately

c Spin AZ 9260 resist on the Laurell spinner (300 rpm 5 s then 5000 rpm 60 s)

d Heat wafer on a pre-heated hot plate for 2 minutes at 110±5°C, cool to 21±2°C

e Rehydrate (19°C, 45% humidity) for 10 minutes

f Using the Karl Suss MA8 and mask labelled "Gate Metal" expose the wafer using recipe OV_AZ9260 (hard contact, 900 mJ/cm2)

g Develop for 3-4 minutes in AZ 726 developer

h Rinse in de-ionised water for 30 seconds

i Blow dry using nitrogen gun

Once developed, do not remove from the yellow room until after etching

A.4.3 Metal Etch

The standard etches for aluminium based on orthophosphoric acid react violently with the InSb substrate. As such, an alternative process based on MF 319 photoresist developer (∼2.3% tetramethylammonium hydroxide) was developed. As the solution has such a low concentration, the etch rate is very low.

a Decant MF 319 developer into suitable glassware. Petri dishes allow for several wafers/samples to be processed in parallel with small quantities of etchant

b Place wafer horizontally in etchant. Do not agitate

c Etch until the metal clears from unmasked areas (40-70 minutes)

d Remove from etchant, quench and rinse in DI water

e To remove the resist, soak the wafer in acetone for 20 seconds, spray with acetone bottle and transfer to fresh acetone then spray with acetone bottle and transfer to IPA

f Leave wafer to soak in IPA for 20 seconds

g Blow dry using nitrogen gun

h Inspect by eye for metal adhesion

Initialisation time: <5 mins
Etch rate: 30 nm/min
Selectivity: 3.3
Lateral etch rate: 0.17 μm/min
Lateral feature definition can be poor using a positive photoresist

A.5 Post-Deposition Annealing

This process stage is currently in prototype

a Set the anneal furnace to 250°C

b Turn on forming gas and turn off nitrogen

c Regulate the flow rate to 100 sccm

d Wait for the temperature to settle

e Load wafer into alumina boat

f Remove tube lid, load sample boat into middle of furnace (using glass rod) and replace tube lid

g Wait 10 minutes for the process to complete

h Unload sample boat (using glass rod) into larger alumina boat. Do not touch the sample boat directly, as it will be extremely hot.

i Place boats on a cool metal surface and wait 5 mins for the sample to return to room temperature

j Once all annealing processes have been completed, return the furnace to 300°C, turn on nitrogen and turn off forming gas

A.6 Contact Metal Patterning

One photolithography step is used to strip dielectric and deposit ohmic contact metal. The standard contact metal is 50/300 nm of Ti/Au, patterned using AZ 9260 photoresist lift-off

A.6.1 Photoresist Patterning

Resist: AZ 9260 Developer: AZ 726 MIF

a Heat wafer on a pre-heated hot plate for 3 minutes at 110±5°C, cool to 21±2°C

b Continue processing immediately

c Spin AZ 9260 resist on the Laurell spinner (300 rpm 5 s then 5000rpm 60s)

d Heat wafer on a pre-heated hot plate for 2 minutes at 110±5°C, cool to 21±2°C

e Rehydrate (19°C, 45% humidity) for 10 minutes

f Using the Karl Suss MA8 and mask labelled “Contact Metal” expose the wafer using recipe OV_AZ9260 (hard contact, 900 mJ/cm2)

g Develop for 3-4 minutes in AZ 726 developer

h Rinse in de-ionised water for 30 seconds

i Blow dry using nitrogen gun

A.6.2 Dielectric Etch

Dilute HF is used to etch the dielectric

a Prepare 100 ml of deionised water in a PTFE beaker

b Add 2 ml 50% concentrated hydrofluoric acid (HF), stir and leave to stand for 5 minutes

c Place wafer horizontally in basket and immerse in etchant for 30 seconds

d Remove basket from etch & quench in beaker of DI water. Immediately place beaker under running QPod and rinse for 30 seconds

e Blow dry using nitrogen gun

Initialisation time: <10 s
Etch rate: 2.0 nm/s for stoichiometric oxide, lower for Al-rich oxide

A.6.3 Metal Deposition

a Load wafer into SVS E2000LL metal evaporator

b Deposit Ti/Au using recipe "IBM TiAu (500-3000Å)"

c On completion unload the wafer from the SVS E2000LL

A.6.4 Lift-off

a Soak wafer in acetone for 30 minutes (19°C) followed by 30 seconds ultrasonic. If gate metal adhesion fails, stop ultrasonic process

b Spray wafer with acetone bottle and transfer to fresh acetone 20 seconds

c Spray with acetone bottle and transfer to IPA and soak for 20 seconds

d Blow dry with nitrogen gun

A.7 Dicing and Preparation for Characterisation

Electrical characterisation is currently performed using a closed-cycle cryostat system, where samples are wire bonded to a carrier PCB. The wafer must be diced, mounted to the PCB and devices bonded to pads on the PCB.

A.7.1 Dicing

Wafers are to be diced by cleaving, with slightly different procedures for GaAs and InSb substrates

a Ensure the equipment is ready: extracted bench, soft mat (cleanroom wipe), diamond scribe, soft pads (cut cleanroom wipe), glass slides and sample wafers

b Mark the boundaries between dies on the back face, using the diamond scribe. Lift the wafer by hand, not using tweezers, as required

c Place the wafer device side down on the mat

d Place a glass slide on the back side of the sample, using a soft pad for protection, and align with the cleave direction

e With the aid of the markers and glass slide, scribe along the cleave direction (between dies)

f For GaAs, sandwich the sample between glass slides (using soft pads for protection) and align the scribe with the edge of the glass slides. Press the suspended region of the wafer to cleave

g For InSb, press the sample into the soft mat with one finger either side of the scribe. If the sample does not cleave immediately, pull the sides apart

h Repeat as necessary until the wafer is diced

i Scribe the back side of each die with a unique ID

A.7.2 Mounting

Once the wafer has been diced, the dies must be mounted to sample carrier PCBs and wire bonded before loading into the closed-cycle cryostat for characterisation. As the MOSCAP devices are all top-to-top structures, insulating GE varnish is used for mounting.

a Ensure centre of carrier PCB is clean and clean with acetone/IPA/ethanol as required

b Apply a small blob of GE varnish to the PCB

c Place the sample onto the GE varnish

Table A.1: Wire bonding parameters

Gate Metal Bond	Contact Metal Bond	PCB Pad Bond
Force	2.5	3.5
Time	35	30
Power	2.1	1.0

d Use a foam-tipped swab to move the sample, spreading the GE varnish and setting the sample as flat as possible. Ensure that the sample edges do not contact the bond pads

e Leave to cure for at least 1 hour

A.7.3 Bonding

Bonding services in the School of Engineering are provided by Frank Courtney. Bond parameters are listed in table A.1.

After the devices are bonded, the PCB must be mounted to a copper carrier block using GE varnish.

a Ensure copper block is clean and clean with acetone/IPA/ethanol/HCl as required

b Apply a small blob of GE varnish to copper block

c Place the PCB onto the GE varnish

d Move and rotate the PCB, spreading the GE varnish and setting the PCB as flat as possible. Rotate the PCB slightly off-centre to aid demounting

e Repeat, if required, for an additional PCB on the reverse side of the copper block

f Leave to cure for at least 1 hour

A.7.4 De-mounting

After characterising the sample as described in section A.8 below, the PCB must be demounted from the copper block and the sample from the PCB. Before demounting, the wire bonds must be removed.

a Perform the bond removal under a magnifying lens for visibility

b Prepare a small ‘cleanroom wipe’ to deposit removed bond wires onto

c Find and prepare a pair of fine-tipped tweezers for bond removal

d Hold the sample under the magnifying lens

e Remove the wire bonds from the sample and deposit on the cleanroom wipe

f Once all bonds are removed, dispose of the cleanroom wipe in general waste

After the bond wires have been removed, the sample can be de-mounted.

a Find and prepare a petri dish and lid suitable for demounting (e.g. dedicated dishes to prevent cross-contamination with copper and/or de-mounting residues)

b Decant ethanol into the petri dish

c Immerse the copper block, PCB(s) and sample(s) in ethanol completely, decanting additional ethanol if needed

d Wait at least 1 min, then remove the PCB(s) from the copper block. Additional tools, e.g. old wafer tweezers or razor blades, can be inserted between the PCB and copper block for leverage

e Wipe the back of the PCB(s). Be aware that the softened GE varnish on the back can adhere to cleanroom wipes etc. and that ethanol evaporation at this stage can leave residues

f Remove the copper block from the ethanol and wipe away any remaining GE varnish using ethanol-soaked cleanroom wipes

g Blow dry the copper block using nitrogen gun

h Re-immerse the PCB(s) in ethanol. Where possible, place the PCB(s) such that both top and bottom sides are exposed to the ethanol

i Place the lid on the petri dish and leave overnight to soften/dissolve the GE varnish

j Remove the PCB(s) and spray gently with ethanol

k Remove the sample from the PCB. Sliding off with tweezers/razor blade can confirm the removal/softening of the GE varnish

l Blow dry the sample using nitrogen gun

m Wipe the PCB(s) clean using ethanol-soaked cleanroom wipes and blow dry using nitrogen gun

A.8 Cryogenic Electrical Characterisation

A closed-cycle cryostat is used for electrical characterisation. Refer to the user manual of the cryostat for detailed process instruction. Before loading, ensure you have a written or photographic map of the connections between devices and bond pads and a record of wafer name and die name/address.

A.8.1 Sample Loading and Cooling

Once the sample has been mounted and bonded, it must be loaded and cooled to characterisation temperature. Detailed instructions are available in the user manual of the cryostat and, as such, the processes below are outlined in brief.

a Vent and unload the cryostat, ensuring that the turbomolecular pump is off and decelerated to stationary before venting

b Load the copper block, connect the interface cable and place the shield, ensuring the cables are not snagged

c Seal the chamber and pump to high vacuum ($<10^{-4}$ mbar)

d Turn on the compressor and set the temperature controller to 80 K

e Wait for the temperature to settle (ensure the heater is turned on and the range set to ‘high’)

A.8.2 Current-Voltage (I-V) Measurement

A simple 2-terminal current-voltage (I-V) measurement is used as a quick screening stage. It assesses leakage in the dielectric’s weakest range and excessively leaky devices are discarded from subsequent characterisation.

a Connect SMU4 to the common field

b Connect SMUs 1-3 to MOSCAP devices

c Enter the measurement parameters listed in table A.2. Ensure the step voltage is entered as a negative number

Table A.2: I-V measurement parameters

Parameter	Value
Temperature	80 K
Start voltage	0 V
Stop voltage	-5 V
Step voltage	-10 mV
Compliance	100 mA
Integration time	Medium
Hold time	1 s
Delay time	0 s
Y-axis mapping	Logarithmic

d Enter the names of each device, following the convention outlined in figure A.2. Spaces and punctuation must match figure A.2 exactly

e Enter the destination folder. Subdirectories can be incorporated e.g. 'Oliver\2017 May Annealing 2\10min 200C'

f Run the measurement

g Devices which remain below 100 mA (the compliance limit) for all voltages are considered to have not broken down. Devices which reach 100 mA are considered to have broken down.

(a) For devices which have not broken down, record the maximum current and pass them to the next stage

(b) For devices which have broken down, record the voltage at which they broke down (reached 100 mA) and omit them from subsequent characterisation

h Repeat steps b-f for all devices

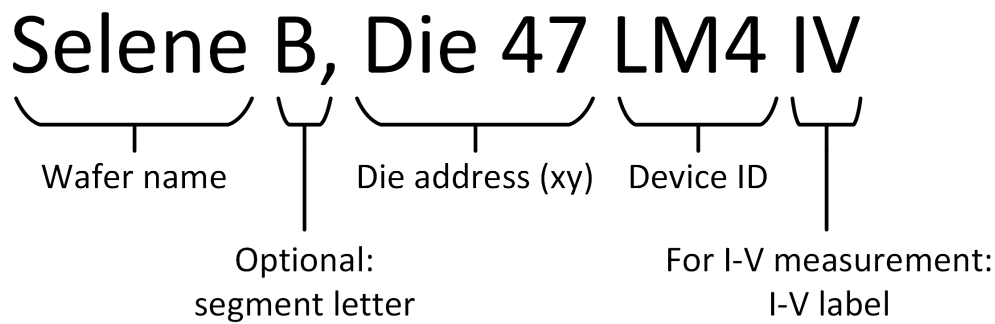


Figure A.2: File naming convention

A.8.3 Capacitance-Voltage (C-V) Measurement

A capacitance-voltage (C-V) measurement is used for standard MOSCAP characterisation. It takes longer to perform than the I-V measurement and is only performed on devices which pass the screening stage.

a Connect Lcur and Lpot to the common field or ohmic contact

b Connect Hcur and Hpot to the MOSCAP device

c Enter the measurement parameters listed in table A.3. Ensure the push switch controls for hysteresis and temperature control are set correctly

d Enter the name of the device, following the convention outlined in figure A.2. Spaces and punctuation must match figure A.2 exactly

e Enter the destination folder. Subdirectories can be incorporated e.g. ‘Oliver\2017 May Annealing 2\10min 200C’

f Check the frequency control is set to ‘list’ and the values match table A.4

g Run the measurement

h Repeat steps a-g for all valid devices

A.8.4 High Resolution C-V Measurement

Long-duration measurements with a large number of small frequency steps can show features that might be missed from a basic C-V measurement. The high resolution C-V measurement takes approximately 4 hours and should be run on one or two devices at the end of the measurement cycle. This procedure is in beta and feedback is welcome.

Table A.3: C-V measurement parameters

Parameter	Value
Temperature	80 K
Start voltage	-5 V
Stop voltage	+5 V
Number of steps	500
Oscillator level	20 mV
Integration time	Medium
Hold time	1 s
Delay time	0 s
Enable Temperature Sweep	Disabled
Enable Hysteresis Scan	Enabled

Table A.4: List of C-V probe frequencies

Frequency (Hz)
1k
5k
10k
40k
80k
100k
200k
400k
600k
800k
1M
2M

Table A.5: High resolution C-V measurement list of frequencies

Parameter	Start value	Stop value	Number of steps	Sweep mode
Frequency	20	2M	60	Logarithmic

a Select a device to run the high resolution measurement on:

(a) Larger devices can be measured with less noise at low frequencies. Select larger devices wherever possible

(b) Select a device which shows characteristic C-V features: high capacitance in accumulation at all frequencies, falling capacitance in depletion (around 0 V) at all frequencies, high capacitance in inversion at low frequency and low capacitance in inversion at high frequency

(c) The high resolution measurement extends to very low frequency and can be used to investigate peculiar features at low frequency which have not converged in the basic measurement

b Follow steps a-e in section A.8.3

c Change the integration time to ‘long’

d Set the frequency control to ‘range’ and enter the values in table A.5

e Optional: add a distinguishing label to the wafer name in the device name, e.g. ‘Selene B HR, Die 47 LM4’

f Run the measurement

A.8.5 Capacitance-Voltage-Temperature (C-V-T) Measurement

The closed-cycle cryostat is capable of automated measurements at arbitrary temperatures between 20 K and 330 K. Capacitance-voltage-temperature (C-V-T) measurements are not standard for MOSCAP characterisation and techniques to interpret the C-V-T data have not yet been developed but a procedure is detailed below for taking the measurements. The C-V-T measurement has an exceptionally long duration, greater than 12 hours.

a Select a well-performing device to run the C-V-T measurement on

b Follow steps a-e in section A.8.3

Table A.6: C-V-T measurement parameters

Parameter	Start value	Stop value	Number of steps	Sweep mode
Frequency	1k	1M	18	Logarithmic
Temperature	20	320	60	Linear

c Set the frequency and temperature control to ‘range’ and enter the values in table A.6

d Change the ‘Enable Temperature Sweep’ button to its positive state (enabled)

e Run the measurement

Appendix B

Literature Review Summary Table

Fabrication processes and key figures of merit from published III-V semiconductor-dielectric interfaces are summarised in table B.1 below.

Table B.1: Literature review summary

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Dep. Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Hong *et al.*[28]	1999	GaAs	Gd_2O_3 (crystalline)	E-beam evaporation	200-550°C	Arsenic stabilised 550°C	-	$\sim 10^{11}$ midgap	High-low	$\sim 10^{-8}$ Acm^{-2} at 1 $MVcm^{-1}$
Ye *et al.*[30]	2004	GaAs	Al_2O_3	ALD	300°C, N_2 carrier	-	O_2 anneal, 600°C, 60 s	6×10^{10}, 5×10^{11}	I-V hysteresis, g_m-f relationship	-
Hong *et al.*[19]	2007	GaAs	$Ga_2O_3(Gd_2O_3)$	E-beam evaporation	UHV	-	-	$\sim 10^{11}$ midgap	Terman (assumed)	-
Hong *et al.*[19]	2007	InGaAs	Al_2O_3	ALD	-	-	None	10^{12} midgap	Terman	$\sim 10^{-9}$ Acm^{-2} at 1 $MVcm^{-1}$

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Brammertz *et al.*[68]	2008	GaAs	Al_2O_3	ALD	300°C	HCl clean	FG, 380°C, 30 s	3×10^{12} near VB, $>10^{13}$ midgap, $\sim4\times10^{12}$ near CB	Conductance	-
Brammertz *et al.*[68]	2008	GaAs	Al_2O_3	ALD	300°C	Ammonium sulphide 5 mins	FG, 400°C, 30 min	1×10^{12} near VB, 8×10^{12} midgap, 3×10^{12} near CB	Conductance	-
Hou *et al.*[36]	2008	InSb	Al_2O_3	ALD	200°C	None	-	$\sim10^{12}$ (77 K)	NSCU CVC model	4×10^{-7} Acm^{-2} at 2 V
Hou *et al.*[36]	2008	InSb	Al_2O_3	ALD	200°C	TMA clean	-	$\sim10^{12}$ (77 K)	NSCU CVC model	10^{-8} Acm^{-2} at 2 V
Hou *et al.*[36]	2008	InSb	Al_2O_3	ALD	200°C	CP4A clean	-	$\sim10^{12}$ (77 K)	NSCU CVC model	10^{-8} Acm^{-2} at 2 V
Zhao *et al.*[33]	2009	InGaAs	Al_2O_3	ALD	-	HF clean	500°C	$>1.17\times10^{12}$	Conductance	-
Zhao *et al.*[33]	2009	InGaAs	HfO_2	ALD	-	HF clean	500°C	$>4.4\times10^{12}$	Conductance	-
Zhao *et al.*[33]	2009	InGaAs	$LaAlO_3$	ALD	-	HF clean	500°C	$>\sim2\times10^{12}$	Conductance	-
Trinh *et al.*[62]	2010	InAs	Al_2O_3	ALD	200°C	TMA clean	N_2, 400°C, 30 s	4×10^{12} midgap	Hill's method	$\sim10^{-8}$ Acm^{-2} at 1 $MVcm^{-1}$
Trinh *et al.*[62]	2010	InAs	Al_2O_3	ALD	200°C	Ammonium sulphide 20 min, TMA clean	N_2, 400°C, 30 s	2.5×10^{12} midgap	Hills method	$\sim10^{-8}$ Acm^{-2} at 1 $MVcm^{-1}$
Trinh *et al.*[62]	2010	InAs	Al_2O_3	ALD	200°C	HCl clean, TMA clean	N_2, 400°C, 30 s	2×10^{12} midgap	Hills method	$\sim10^{-10}$ Acm^{-2} at 1 $MVcm^{-1}$
Trinh *et al.*[87]	2010	InGaAs	Al_2O_3	ALD	300°C	Acetone & isopropanol only	N_2, 500°C, 10 min	2.5×10^{12}	Conductance	-
Trinh *et al.*[87]	2010	InGaAs	Al_2O_3	ALD	300°C	HCl & sulphidation	N_2, 500°C, 10 min	5×10^{11}	Conductance	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Trinh *et al.*[87]	2010	InGaAs	Al_2O_3	ALD	300°C	HCl & sulphidation	H_2, 500°C, 10 min	$<5\times10^{11}$	Conductance	-
Burek *et al.*[88]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl, TMA	Thermal evaporation	5.7×10^{12} midgap	Conductance	-
Burek *et al.*[88]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl, TMA	Thermal evaporation, FG, 400°C, 50 min	3.4×10^{12} midgap	Conductance	-
Burek *et al.*[88]	2011	InGaAs	HfO_2	MBD	400°C	Unclear	E-beam evaporation	1.1×10^{13} midgap	Conductance	-
Burek *et al.*[88]	2011	InGaAs	HfO_2	MBD	400°C	Unclear	E-beam evaporation, FG, 400°C, 50 min	$<5.2\times10^{12}$ midgap	Conductance	-
Carter *et al.*[81]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl	FG, 400°C, 1 min	4.6×10^{12} near CB	Conductance	-
Carter *et al.*[81]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl, TMA	FG, 400°C, 1 min	4.6×10^{12} near CB	Conductance	-
Carter *et al.*[81]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl, H plasma 100 W	FG, 400°C, 1 min	2.5×10^{12} near CB	Conductance	-
Carter *et al.*[81]	2011	InGaAs	Al_2O_3	ALD	300°C	HCl, H plasma 100 W & TMA	FG, 400°C, 1 min	1.7×10^{12} near CB	Conductance	-
Hwang *et al.*[77]	2011	InGaAs	HfO_2	MBD	400°C	As decapping, TMA 230°C 10 s	FG, 400°C, 50 min	6×10^{12} midgap	Terman	-
Liu *et al.*[78]	2011	InGaAs	Al_2O_3	'Molecular-atomic deposition' (N_2)	-	Sulphidation	N_2, 500°C, 3 min	1.3×10^{13}	Conductance (assumed)	-
Liu *et al.*[78]	2011	InGaAs	Al_2O_3	'Molecular-atomic deposition' (N_2)	-	Sulphidation, FG plasma	N_2, 500°C, 3 min	1.3×10^{12}	Conductance (assumed)	-
Liu *et al.*[78]	2011	InGaAs	Al_2O_3	'Molecular-atomic deposition' (FG)	-	Sulphidation, FG plasma	N_2, 500°C, 3 min	3.7×10^{11}	Conductance (assumed)	-
Nainani *et al.*[90]	2011	GaSb	Al_2O_3	ALD	300C	HCl	FG, 350°C, 30 min	3×10^{12} near VB, 3×10^{11} midgap, 1.1×10^{13} near CB	Conductance	-
Nainani *et al.*[90]	2011	GaSb	Al_2O_3	ALD	300°C	HCl	FG, 350°C, 30 min	3×10^{11} midgap	Conductance	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Paterson *et al.*[27]	2011	GaAs	$Gd_{0.25}Ga_{0.15}O_{0.6}$	MBD	UHV	-	-	2×10^{12} midgap, 10^{14} near CB	High-low & Terman	-
Paterson *et al.*[27]	2011	InGaAs	$Gd_{0.25}Ga_{0.15}O_{0.6}$	MBD	UHV	-	-	$\sim10^{14}$ midgap, $\sim10^{13}$ near CB, $\sim10^{14}$ in CB	High-low	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	300°C	650°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	2×10^{12} near VB	High-low	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	300°C	650°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	3.0×10^{13} near CB	Conductance	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	300°C	600°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	2×10^{12} near VB	High-low	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	300°C	600°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	2.0×10^{13} near CB	Conductance	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	200°C	600°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	2×10^{12} near VB	High-low	-
Xu *et al.*[75]	2011	GaSb	Al_2O_3	ALD	200°C	600°C activation anneal, HCl & ammonium hydroxide	N_2, 600°C, 30 s	1.5×10^{13} near CB	Conductance	-
Suzuki *et al.*[40]	2012	InGaAs	HfO_2 with Al_2O_3 IPL	ALD	250°C	Ammonium hydroxide & sulphidation	N_2, 400°C, 1 min	2×10^{12}	Conductance	-
Suzuki *et al.*[40]	2012	InGaAs	HfO_2	ALD	250°C	Ammonium hydroxide & sulphidation	N_2, 400°C, 1 min	2×10^{14}	Terman	-
Trinh *et al.*[89]	2012	InAs/InGaAs	HfO_2	MBD	300°C, UHV	HF & sulphidation	FG, 400°C, 5 min	1.02×10^{13}	Conductance	-
Trinh *et al.*[89]	2012	InAs/InGaAs	HfO_2	MBD	300°C, UHV	HF & sulphidation	FG, 450°C, 5 min	4.37×10^{12}	Conductance	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Trinh *et al.*[89]	2012	InAs/InGaAs	HfO_2	MBD	300°C, UHV	HF & sulphidation	FG, 500°C, 5 min	2.71×10^{12}	Conductance	-
Trinh *et al.*[89]	2012	InAs/InGaAs	HfO_2	MBD	300°C, UHV	HF & sulphidation	FG, 550°C, 5 min	5.33×10^{12}	Conductance	-
Wang *et al.*[37]	2012	GaSb p-type	$HfAlO_3$	ALD	200°C, Al-first	Acetone, methanol, isopropanol	None	4.0×10^{12} near VB, 5.5×10^{12} midgap	Conductance	-
Wang *et al.*[37]	2012	GaSb p-type	$HfAlO_3$	ALD	200°C, Hf-first	Acetone, methanol, isopropanol	None	4.0×10^{12} near VB, 4.5×10^{12} midgap	Conductance	-
Wang *et al.*[37]	2012	GaSb p-type	$HfAlO_3$	ALD	200°C, Al-first	Acetone, methanol, isopropanol	N_2, 600°C, 30 s	8.0×10^{12} near VB, 1.2×10^{13} midgap	Conductance	$\sim10^{-8}$ Acm^{-2} at 1 $MVcm^{-1}$
Wang *et al.*[37]	2012	GaSb p-type	$HfAlO_3$	ALD	200°C, Hf-first	Acetone, methanol, isopropanol	N_2, 600°C, 30 s	1.0×10^{13} near VB, 1.6×10^{13} midgap	Conductance	$\sim10^{-7}$ Acm^{-2} at 1 $MVcm^{-1}$
Chobpattana *et al.*[80]	2013	InGaAs	HfO_2 with Al_2O_3 IPL	ALD	300°C	HCl/HF, H plasma 100 W & TMA	FG, 400°C, 15 min	1×10^{13} midgap	Terman	-
Chobpattana *et al.*[80]	2013	InGaAs	HfO_2 with Al_2O_3 IPL	ALD	300°C	HCl/HF, N plasma 100 W & TMA	FG, 400°C, 15 min	2×10^{12} midgap	Terman	-
Chobpattana *et al.*[80]	2013	InGaAs	HfO_2	ALD	300°C	HCl/HF, H plasma 100 W & TMA	FG, 400°C, 15 min	9×10^{12} midgap	Terman	-
Chobpattana *et al.*[80]	2013	InGaAs	HfO_2	ALD	300°C	HCl/HF, N plasma 100 W & TMA	FG, 400°C, 15 min	2.5×10^{12} midgap	Terman	-
Trinh *et al.*[38]	2013	InSb	HfO_2 with Al_2O_3 IPL	ALD	250°C	HCl	N_2, 250°C, 30 s	6×10^{11} near CB	Conductance	-
Uddin *et al.*[99]	2013	InSb	Al_2O_3	ALD	130°C	None	None	1.6×10^{13} near VB	Gated Hall fitting	-
Uddin *et al.*[99]	2013	$Al_{0.1}In_{0.9}Sb$	Al_2O_3	ALD	130°C	None	None	2×10^{12} midgap	Gated Hall fitting	-
Uddin *et al.*[99]	2013	$Al_{0.1}In_{0.9}Sb$	Al_2O_3	ALD	130°C	None	None	1×10^{12} near CB	Gated Hall fitting	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Zadeh *et al.*[44]	2013	InGaAs	La_2O_3	Evaporation	-	HF & sulphidation	FG, TiN/W	4.6×10^{11}	Conductance	-
Zadeh *et al.*[44]	2013	InGaAs	La_2O_3	Evaporation	-	HF & sulphidation	FG, W	9.2×10^{12}	Conductance	-
Barth *et al.*[86]	2014	GaSb	HfO_2	ALD	250°C	HCl, TMA	FG, 350°C	5×10^{13} near VB	Terman	-
Barth *et al.*[86]	2014	GaSb	HfO_2	ALD	250°C	Solvent, H/Ar plasma 100 W, TMA	FG, 350°C	1×10^{14} near VB	Terman	-
Barth *et al.*[86]	2014	GaSb	HfO_2	ALD	250°C	HCl, H/Ar plasma 100 W, TMA	FG, 350°C	5×10^{13} near VB	Terman	-
Luc *et al.*[47]	2014	InGaAs n-type	Al_2O_3 with AlN IPL	PEALD	250°C	HCl	N_2, 450°C, 2 min	7.5×10^{12} midgap	Terman	10^{-9} Acm^{-2} at 2 V
Luc *et al.*[47]	2014	InGaAs p-type	Al_2O_3 with AlN IPL	PEALD	250°C	HCl	N_2, 450°C, 2 min	1.9×10^{12} midgap	Terman	10^{-9} Acm^{-2} at 2 V
Luc *et al.*[47]	2014	InGaAs n-type	Al_2O_3 with AlN IPL	PEALD	250°C	HCl	N_2, 450°C, 2 min	8×10^{11} midgap	Conductance	10^{-9} Acm^{-2} at 2 V
Luc *et al.*[47]	2014	InGaAs p-type	Al_2O_3 with AlN IPL	PEALD	250°C	HCl	N_2, 450°C, 2 min	4×10^{11} midgap	Conductance	10^{-9} Acm^{-2} at 2 V
Luc *et al.*[93]	2014	InGaAs	Al_2O_3	ALD	250°C	HCl, TMA	N_2, 400°C, 5 min	1.5×10^{12} near CB	Conductance	-
Luc *et al.*[93]	2014	InGaAs	Al_2O_3	ALD	250°C	HCl, TMA	FG, 400°C, 5 min	1.375×10^{12} near CB	Conductance	-
Peralagu *et al.*[70]	2014	GaSb	Al_2O_3	ALD	300°C	Sulphidation (1%)	None	4×10^{12} midgap	High-low	-
Chang *et al.*[45]	2015	InGaAs	La_2O_3	ALD	250°C	Sulphidation	N_2, 300°C, 1 min	3×10^{11}	Conductance	-
Chang *et al.*[45]	2015	InGaAs	Al_2O_3	ALD	250°C	Sulphidation	N_2, 300°C, 1 min	4×10^{12}	Conductance	-
Chang *et al.*[45]	2015	InGaAs	Al_2O_3/La_2O_3	ALD	250°C	Sulphidation	N_2, 300°C, 1 min	1.8×10^{11}	Conductance	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Cho *et al.*[84]	2015	GaN	Al_2O_3	ALD	200°C	Solvent	FG, 430°C, 30 min	6.8×10^{12} near CB	Conductance	-
Cho *et al.*[84]	2015	GaN	Al_2O_3	ALD	200°C	Solvent, Ar plasma 50 W	FG, 430°C, 30 min	5×1010 near CB	Conductance	-
Cho *et al.*[84]	2015	GaN	Al_2O_3	ALD	200°C	Solvent, Ar plasma 150 W	FG, 430°C, 30 min	2.1×10^{11} near CB	Conductance	-
Cho *et al.*[84]	2015	GaN	Al_2O_3	ALD	200°C	Solvent, Ar plasma 300 W	FG, 430°C, 30 min	2.3×10^{12} near CB	Conductance	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	H plasma 10 cycles	FG, 400°C, 15 min	3.8×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	H plasma 10 cycles	FG, 400°C, 15 min	1.4×10^{13}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	H plasma/TMA 2 cycles	FG, 400°C, 15 min	3.8×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	H plasma/TMA 2 cycles	FG, 400°C, 15 min	3.5×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	H plasma/TMA 5 cycles	FG, 400°C, 15 min	2.7×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	H plasma/TMA 5 cycles	FG, 400°C, 15 min	3.3×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	H plasma/TMA 10 cycles	FG, 400°C, 15 min	2.0×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	H plasma/TMA 10 cycles	FG, 400°C, 15 min	2.0×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	BOE	FG, 400°C, 15 min	2.9×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	BOE	FG, 400°C, 15 min	3.4×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	120°C	No BOE	FG, 400°C, 15 min	2.8×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (001)	HfO_2	ALD	300°C	No BOE	FG, 400°C, 15 min	3.4×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (110)	HfO_2	ALD	120°C	BOE	FG, 400°C, 15 min	2.8×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (110)	HfO_2	ALD	300°C	BOE	FG, 400°C, 15 min	3.2×10^{12}	Full interface state model	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Kent *et al.*[66]	2015	InGaAs (110)	HfO_2	ALD	120°C	No BOE	FG, 400°C, 15 min	2.8×10^{12}	Full interface state model	-
Kent *et al.*[66]	2015	InGaAs (110)	HfO_2	ALD	300°C	No BOE	FG, 400°C, 15 min	3.5×10^{12}	Full interface state model	-
Koh *et al.*[79]	2015	InGaAs	HfO_2 with Al_2O_3 IPL	ALD	-	HCl	None	9×10^{11} midgap	Conductance	-
Koh *et al.*[79]	2015	InGaAs	HfO_2 with Al_2O_3 IPL	ALD	-	HCl, Ar plasma 20 W	None	6×10^{11} midgap	Conductance	-
Luc *et al.*[48]	2015	InGaAs	Thick HfO_2 with AlN IPL	PEALD	250°C	HCl	FG, 450°C, 5 min	5.2×10^{12} midgap	Terman	10^{-9} Acm^{-2} at 2 V
Luc *et al.*[48]	2015	InGaAs	Thin HfO_2 with AlN IPL	PEALD	250°C	HCl	FG, 450°C, 5 min	5.3×10^{12} midgap	Terman	10^{-4} Acm^{-2} at 2 V
Luc *et al.*[48]	2015	InGaAs	Thin HfO_2 with AlN IPL	PEALD	250°C	HCl	PRP N_2/H_2; FG, 450°C, 5 min	3.1×10^{12} midgap	Terman	-
Luc *et al.*[48]	2015	InGaAs	Thin HfO_2 with AlN IPL	PEALD	250°C	HCl	PRP NH_3; FG, 450°C, 5 min	2.9×10^{12} midgap	Terman	-
Ruppalt *et al.*[82]	2015	GaSb	Al_2O_3	PEALD	150°C	None	FG, 350°C, 30 min	1×10^{14}	Terman	-
Ruppalt *et al.*[82]	2015	GaSb	Al_2O_3	PEALD	150°C	HCl	FG, 350°C, 30 min	1×10^{13}	Terman	-
Ruppalt *et al.*[82]	2015	GaSb	Al_2O_3	PEALD	150°C	N/H plasma 50 W 10 min 250°C	FG, 350°C, 30 min	1×10^{13}	Terman	-
Ruppalt *et al.*[82]	2015	GaSb	Al_2O_3	PEALD	150°C	N/H plasma 50 W 30 min 150°C	FG, 350°C, 30 min	2.5×10^{12}	Terman	-
Ruppalt *et al.*[82]	2015	GaSb	Al_2O_3	PEALD	150°C	N/H plasma 100 W 10 min 150°C	FG, 350°C, 30 min	3×10^{11}	Terman	-
Sakong *et al.*[73]	2015	GaN	Al_2O_3	ALD	-	None (dry etched)	N_2, 850°C, 30 s	2.8×10^{12}	High-low	-
Sakong *et al.*[73]	2015	GaN	Al_2O_3	ALD	-	Tetramethylammonium hydroxide	N_2, 850°C, 30 s	1.1×10^{11}	High-low	-

Work done by	Year	Substrate Material	Dielectric Material	Deposition Technique	Deposition Conditions	Pre-treatment	P-D Processing	D_{it} ($cm^{-1}eV^{-1}$)	D_{it} Extraction	J_L
Yi *et al.*[100]	2015	$Al_{0.09}In_{0.91}Sb$	HfO_2	ALD	175°C	-	-	8.4×10^{11}	Gated Hall fitting	-
Krylov *et al.*[46]	2016	InGaAs	Al_2O_3	ALD	300°C	Sulphuric & ammonium hydroxide	N_2, 300°C, 5 min	2.5×10^{12} midgap	Terman	-
Krylov *et al.*[46]	2016	InGaAs	Al_2O_3	ALD	300°C	Sulphuric & ammonium hydroxide	N_2, 400°C, 5 min	8.5×10^{12} midgap	Terman	-
Krylov *et al.*[46]	2016	InGaAs	AlN	ALD	300°C	Sulphuric & ammonium hydroxide	N_2, 300°C, 5 min	6.5×10^{12} midgap	Terman	-
Krylov *et al.*[46]	2016	InGaAs	AlN	ALD	300°C	Sulphuric & ammonium hydroxide	N_2, 400°C, 5 min	2.2×10^{12} midgap	Terman	-
Krylov *et al.*[46]	2016	InGaAs	AlN	PEALD	300°C	Sulphuric & ammonium hydroxide	N_2, 300°C, 5 min	1.8×10^{12} midgap	Terman	$\sim10^{-10}$ Acm^{-2} at 1 $MVcm^{-1}$
Krylov *et al.*[46]	2016	InGaAs	AlN	PEALD	300°C	Sulphuric & ammonium hydroxide	N_2, 400°C, 5 min	1.5×10^{12} midgap	Terman	$\sim10^{-10}$ Acm^{-2} at 1 $MVcm^{-1}$
Lechaux *et al.*[74]	2016	InGaAs	Al_2O_3	ALD	250°C	Ammonium hydroxide	None	6×10^{11}	Conductance	1×10^{-5} Acm^{-2} at 2 V
Lechaux *et al.*[74]	2016	InGaAs	Al_2O_3	ALD	250°C	Ammonium hydroxide	O_2 plasma	8×10^{11}	Conductance	1×10^{-5} Acm^{-2} at 2 V

Appendix C

Quantum Well MOSFET

C.1 Introduction

In an attempt to integrate dielectrics into practical device structures quantum well metal-oxide-semiconductor field effect transistors (QW-MOSFETs) were fabricated. Quantum well structures are preferred for narrow bandgap semiconductors[127][98][133]: encapsulating the narrow bandgap material (InSb) with a wide bandgap material (AlInSb) prevents leakage current through bulk narrow bandgap material at room temperature. Additionally, dopants can be deposited as an ultra-thin layer (a 'delta-doping' layer, of δ-doping layer) and, if grown in close proximity to the quantum well, the carriers can transfer into the well, enabling high carrier concentration without ionised dopant impurities and allowing effective carrier transport with mobility above bulk values.

Quantum well MESFET (metal-semiconductor field effect transistor) structures have been fabricated previously, but are limited by leakage current across the Schottky barrier[98]. This leakage can be significantly reduced using a metal-oxide-semiconductor gate structure. In an attempt to demonstrate a more practical vehicle for dielectric process development, particularly in the context of gate control, QW-MOSFET devices were fabricated by depositing gate dielectric, gate metal and source/drain contact metals onto an InSb/AlInSb quantum well structure. The devices showed minimal transistor-like behaviour, showing only linear response and ~10% modulation of drain current for ΔV_G=5 V.

C.2 Experimental Methodology

The InSb/AlInSb quantum well structure was grown on a 2" wafer of semi-insulating GaAs by the National Epitaxy Facility at the University of Sheffield. The layer

Table C.1: Quantum well structure layer specification

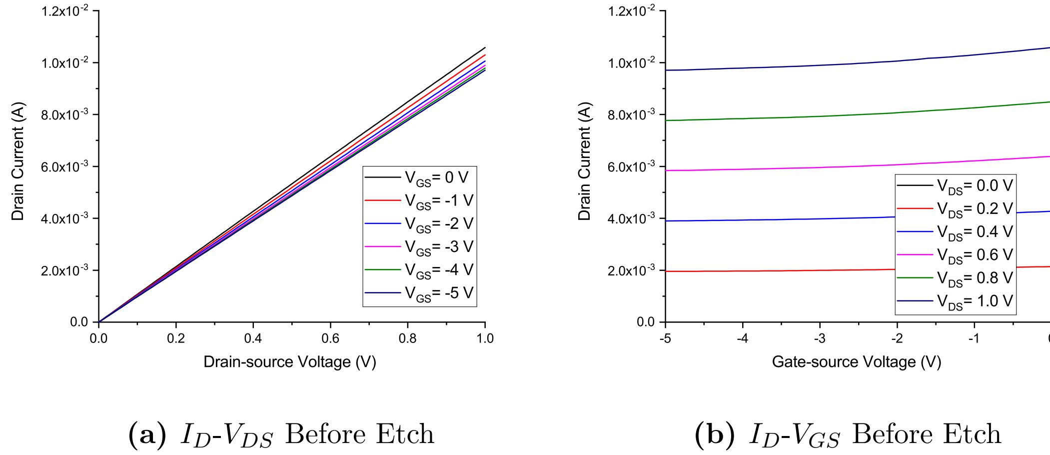
Layer	Material	Thickness (nm)	Doping
Top barrier	$Al_{0.15}In_{0.85}Sb$	25	Undoped
δ-doping	δ-doping	0.1	Te-doped n-type $5{\times}10^{11}$ cm^{-2}
Spacer	$Al_{0.15}In_{0.85}Sb$	25	Undoped
Quantum well	InSb	30	Undoped
Bottom barrier	$Al_{0.1}In_{0.9}Sb$	3000	Undoped
Buffer layer	AlSb	500	Undoped
Buffer layer	GaAs	200	Undoped

specification is given in table C.1 - 15% Al was used for the top barrier, 10% Al for the bottom barrier and a buffer layers of GaAs and AlSb were grown between the GaAs substrate and the bottom barrier. The material was characterised by Hall measurement at the University of Cardiff at a temperature of 3 K, giving an electron mobility of 240000 cm^{2}V^{-1}s^{-1} and a carrier density of $3.7{\times}10^{15}$ cm^{-2}.

A 1 cm square piece was cleaved from the wafer and processed at the University of Warwick. The sample was cleaned for 1 min in HCl-water (1:5 37% HCl and deionised (DI) water), loaded into an Ultratech Fiji and 100 cycles of Al_2O_3 deposited at 200°C as a thermal Al-first process. After unloading, the sample was transferred promptly to an SVS e-beam evaporator, where 1 µm of Al metal was deposited as a gate contact. The sample was then patterned using AZ 9260 photoresist as a mask and Microposit MF-319 photoresist developer (dilute tetramethyammonium hydroxide) as an etchant to give a gate contact, with a gate length of 170 µm. The sample was then annealed in O_2 at 300°C for 90 mins in a Carbolite tube furnace, with a gas flow of 100 sccm.

The pattern for the drain and source contacts was defined using AZ 9260 photoresist, with a contact width of 270 µm (equal to the effective gate width) and a separation of 10 µm between the gate and the source/drain. The sample was etched in dilute hydrofluoric acid (1:50 50% HF and DI water) for 30 s to remove any gate oxide from the source/drain areas before re-loading into the SVS e-beam evaporator. An ion beam mill was performed, followed by a 50 nm Ti adhesion layer and a 300 nm Au ohmic contact layer. A lift-off process was then performed by soaking the sample in acetone and using an ultrasonic cleaning/agitation process. The MOSFET gate and ohmic contact recipes were similar to those detailed in appendix A for MOSCAP devices.

After the gate, source and drain regions were defined, the sample was mounted to



(a) I_D-V_{DS} Before Etch **(b)** I_D-V_{GS} Before Etch

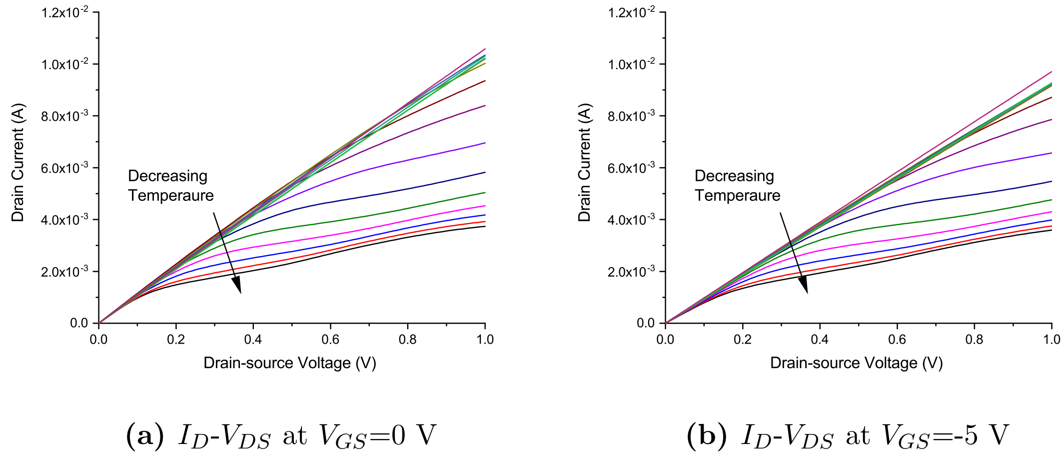
Figure C.1: QW-MOSFET current-voltage response for I_D-V_{DS} and I_D-V_{GS} at room temperature before etch isolation

a carrier PCB, wire bonded using Al wire, mounted onto a copper carrier block and loaded into a Leybold RDK 10-320 cryostat for low-temperature characterisation. The devices were characterised using a HP 4155C parameter analyser between temperatures of 20 K and 300 K. After characterisation, the sample was de-mounted using ethanol and cleaned using acetone and isopropanol. It was then patterned using AZ 9260 photoresist and etched in a mixture of lactic, nitric and hydrofluoric acid (100:16:4) for 4 mins to isolate the QW-MOSFET devices and eliminate conduction in the quantum well 'around' the MOSFET gate. After the photoresist was removed, the etch depth was measured as 5.8 µm using an Ambios XP100 stylus profilometer. The devices were then characterised at room temperature using an Agilent B1500A parameter analyser and a Wentworth manual probe station, using BeCu (beryllium-copper) probe needles.

C.3 Results and Discussion

Examples of measured drain characteristics and transfer characteristics are shown in figures C.1, C.2 and C.3.

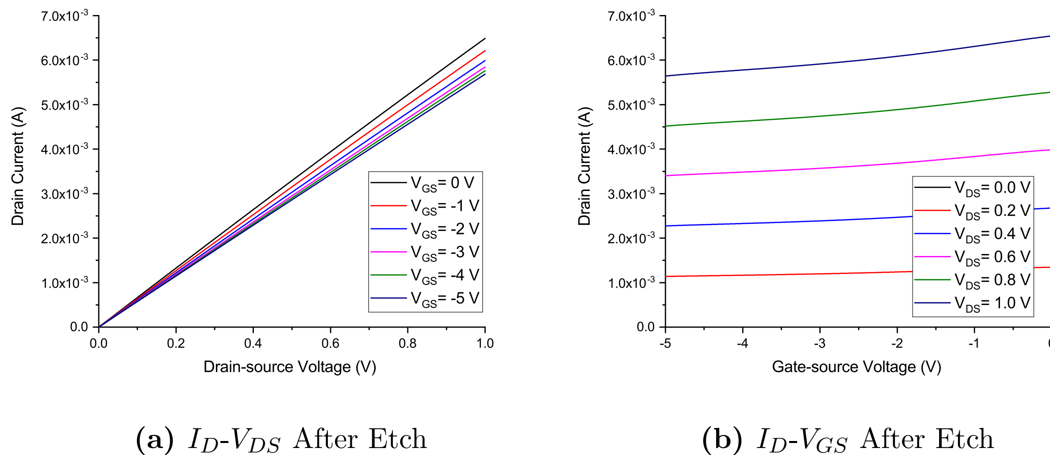
Characterised devices showed only linear characteristics at room temperature, with no saturation behaviour. The largest $\frac{I_{On}}{I_{Off}}$ (on/off ratio) observed at room temperature was 1.14 for a device after etching. The small modulation prevented meaningful evaluation of instantaneous transconductance but the total modulation at $V_{DS} = 0.1\ V$ (810 µA for 5 V) implies a transconductance (g_m) of 162 µS, or 953 µSmm^{-1}. $\frac{I_{On}}{I_{Off}}$ for cooled devices before etching is shown in figure C.4 - $\frac{I_{On}}{I_{Off}}$ was 1.09 at 300 K, rising to a maximum of 1.12 at 240 K before falling to a minimum of



(a) I_D-V_{DS} at V_{GS}=0 V

(b) I_D-V_{DS} at V_{GS}=-5 V

Figure C.2: QW-MOSFET I_D-V_{DS} response at variable temperature (20 K to 300 K) for V_{GS}=0 V and V_{GS}=-5 V



(a) I_D-V_{DS} After Etch

(b) I_D-V_{GS} After Etch

Figure C.3: QW-MOSFET current-voltage response for I_D-V_{DS} and I_D-V_{GS} at room temperature after etch isolation

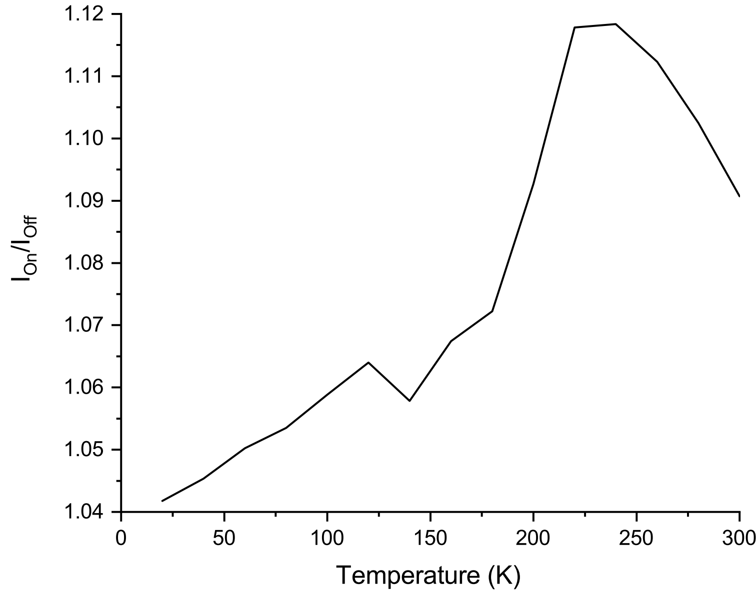


Figure C.4: $\frac{I_{On}}{I_{Off}}$ of QW-MOSFET devices for variable temperature

1.04 at 20 K.

As there is no saturation behaviour observed at room temperature, it is assumed that leakage is dominating the device response. This is supported by the apparent onset of FET-like saturation behaviour at low temperature shown in figure C.2, where leakage mechanisms freeze out. The leakage may be associated with the barrier layers and/or the remaining material at the periphery of the device (conduction ‘around’ the device).

The barrier material had not been characterised and the only Hall measurement performed on undoped (Al)InSb material grown at the National Epitaxy Facility was a single measurement on undoped $Al_{0.05}In_{0.95}Sb$. This measurement gave a carrier concentration of 9.91×10^{13} cm^{-3} p-type at 77 K (eliminating the minority electrons) and a mobility of 786 $cm^2V^{-1}s^{-1}$. These gave a conductivity of 12.5 mSm^{-1} and, assuming the $Al_{0.15}In_{0.85}Sb$ and $Al_{0.1}In_{0.9}Sb$ barrier materials are similar to the $Al_{0.05}In_{0.95}Sb$ Hall measurement, conduction through the barriers should be minimal.

The sheet resistance of the quantum well was calculated using equation C.1. In this instance, N_D is the carrier concentration per unit area, not per unit volume.

$$R_S = \frac{1}{N_D q \mu_e} \tag{C.1}$$

The width of the remaining material and the length between source and drain contacts were measured to be 18.3 µm and 190 µm, respectively, using an optical

microscope. These values gave the resistance of the quantum well in the remaining material to be 0.073 Ω using the maximum low temperature mobility and 0.25 Ω using a mobility of 70000 $cm^2V^{-1}s^{-1}$, a typical room temperature value for high-mobility material on a GaAs substrate. The device leakage is most likely to be caused by the remaining material - to resolve this in future work, the isolation etch should be performed before depositing the gate. The gate can then exceed the dimensions of the etched mesa and 'run down the side' of the device, preventing and non-depleted conduction paths from remaining after fabrication.

In addition to leakage, a significant series resistance is observed in both characterisation rigs. The series resistance is approximately 166 Ω (calculated from a sample device for V_D between 0 V and 100 mV) but the source of this resistance is unclear. As the source/drain contact recipe has not been optimised, this may have introduced additional series resistance but it is unlikely to account for such a large value. Additional investigation using the transfer length method (TLM) and/or Hall bar structures may offer additional insight into series resistance.

C.4 Analysis, Modelling and Discussion

The drain current (I_D) for a conventional MOSFET in its linear region can be predicted using equation C.2 (from Sze[12]), where W and L are the gate width and length, μ is the channel mobility, C_{ox} is the oxide capacitance, V_G is the gate voltage, V_T is the threshold voltage and V_D is the drain voltage. Transconductance can be determined by dividing both sides by $(V_G - V_T)$.

$$I_D = \frac{W}{L}\mu C_{ox}(V_G - V_T)V_D \tag{C.2}$$

The gate width and length are 270 µm and 170 µm, respectively, and the average C_{ox} observed for InSb MOSCAPs fabricated alongside the QW-MOSFETs was 5.7×10^{-7} Fcm^{-2}. Threshold voltage can be predicted using equation C.3 (from Sze[12]), where V_{FB} is the flatband voltage, φ_b is the electrostatic potential in the bulk substrate, ϵ_{semi} is the absolute permittivity of the semiconductor, q is the electron charge and N_I is the dopant concentration.

$$V_T = V_{FB} + 2\varphi_b + \frac{\sqrt{2\epsilon_{semi} q N_I (2\varphi_b)}}{C_{ox}} \tag{C.3}$$

The average V_{FB} for the InSb MOSCAPs was -1.16 V - this is taken as a first

approximation of the V_{FB} for the MOSFETs, although results in section 8.4 suggest the V_{FB} for the top $Al_{0.15}In_{0.85}Sb$ layer may be shifted in the positive direction. The bulk electrical potential, φ_b, was calculated to be 0.1704 eV for the $Al_{0.1}In_{0.9}Sb$ bottom barrier, acting as the substrate, and the relative permittivity of $Al_{0.15}In_{0.85}Sb$ was calculated to be approximately 15.28, using the one-dimensional electrostatic model and ternary material models detailed in chapter 4. The dopant concentration is assumed to be dominated by the barrier and the previously-discussed value of 9.91×10^{13} cm^{-3} was used. Using these values, V_T is calculated to be -0.81 V.

This value is then substituted into equation C.2, taking V_G=0.0 V and V_D=1.0 V to obtain a value for maximum drain current and g_m (assuming operation in the linear region). When the channel mobility is taken as the maximum Hall mobility of 240000 cm^{2}V^{-1}s^{-1}, $I_{D,max}$ is calculated to be 0.18 A and g_m to be 0.22 S, or 1.28 Smm−1. When a reduced channel mobility of 1000 cm^{2}V^{-1}s^{-1} is used, $I_{D,max}$ drops to 7.36×10^{-4} A and g_m to 910 µS, or 5.4 mSmm^{-1}. These results suggest that, assuming the oxide capacitance extraction is reliable, the effective channel mobility is more than two orders of magnitude lower than the measured Hall mobility and has a value of 178 cm^{2}V^{-1}s^{-1}.

To assess saturation behaviour, equation C.4 (also taken from Sze[12]) can be used to calculate saturation current, where m is a function of dopant concentration which approaches 0.5 for low dopant concentration (assumed here for the barrier material).

$$I_{D,sat} = \frac{mW}{L}\mu C_{ox}(V_G - V_T)^2 \tag{C.4}$$

Using equation C.4, $I_{D,sat}$ for V_G-0.0 V is calculated to be 0.07 A for the maximum Hall mobility, 2.98×10^{-4} A for the reduced mobility of 1000 cm^{2}V^{-1}s^{-1} and 5.3×10^{-5} A for the extracted value of 178 cm^{2}V^{-1}s^{-1}. Saturation behaviour is not observed in measured devices but is likely to be lost in the case of excessive leakage.

C.5 Conclusion

Quantum well MOSFET devices were fabricated to demonstrate gate control but minimal channel modulation was observed, even when devices were cooled. High leakage was observed at all stages, probably due to material remaining at the periphery of the device after the isolation etch, and a large series resistance was also measured. Calculations for conventional MOSFETs predicted higher modulation than observed and saturation currents significantly below the measured current,

even for a V_G of -5 V. The 'true' MOSFET behaviour is likely to be obscured by the leakage. Modification to the fabrication process - performing the isolation etch before gate deposition, allowing the gate to overlap the mesa edge - should eliminate the leakage and enable the device to be effectively characterised and the series resistance issue to be investigated and resolved.