

# A Defects' based model on the Barrier Height behaviour in 3C-SiC-on-Si Schottky Barrier Diodes

Arvanitopoulos, A., Antoniou, M., Jennings, M., Perkins, S., Gyftakis, K. N., Mawby, P. A. & Lophitis, N.

Author post-print (accepted) deposited by Coventry University's Repository

## Original citation & hyperlink:

Arvanitopoulos, A, Antoniou, M, Jennings, M, Perkins, S, Gyftakis, KN, Mawby, PA & Lophitis, N 2019, 'A Defects' based model on the Barrier Height behaviour in 3C-SiC-on-Si Schottky Barrier Diodes' IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. (In-press), pp. (In-press).

<https://dx.doi.org/10.1109/JESTPE.2019.2942714>

DOI 10.1109/JESTPE.2019.2942714

ISSN 2168-6777

ESSN 2168-6785

Publisher: IEEE

**© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.**

**Copyright © and Moral Rights are retained by the author(s) and/ or other copyright owners. A copy can be downloaded for personal non-commercial research or study, without prior permission or charge. This item cannot be reproduced or quoted extensively from without first obtaining permission in writing from the copyright holder(s). The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the copyright holders.**

**This document is the author's post-print version, incorporating any revisions agreed during the peer-review process. Some differences between the published version and this version may remain and you are advised to consult the published version if you wish to cite from it.**

# A Defects'-based model on the Barrier Height behaviour in 3C-SiC-on-Si Schottky Barrier Diodes

A. Arvanitopoulos, M. Antoniou, M. R. Jennings, S. Perkins, K. N. Gyftakis, P. Mawby, N. Lophitis

**Abstract**—3C-Silicon Carbide (3C-SiC) Schottky Barrier Diodes on Silicon (Si) substrates (3C-SiC-on-Si) have been found to suffer of excessive sub-threshold current, despite the superior electrical properties of 3C-SiC. In turn, that is one of the factors deterring the commercialization of this technology. The forward Current-Voltage (I-V) characteristics in these devices carry considerable information about the material quality. In this context, an advanced Technology Computer Aided Design (TCAD) model is proposed and validated with measurements obtained from a fabricated and characterized Platinum/3C-SiC-on-Si Schottky Barrier Diode with scope to shed light in the physical carrier transport mechanisms, the impact of traps and their characteristics on the actual device performance. The model includes defects originating from both the Schottky contact and the hetero-interface of 3C-SiC with Si, which allows the investigation of their impact on the magnification of the sub-threshold current. Further, the simulation results and measured data allowed for the identification of additional distributions of interfacial states, the effect of which is linked to the observed non-uniformities of the Barrier Height value. A comprehensive characterization of the defects affecting the carrier transport mechanisms of the investigated 3C-SiC-on-Si power diode is thus achieved and the proposed TCAD model is able to accurately predict the device current both during forward and reverse bias conditions.

**Index Terms**—3C-SiC-on-Si, Band diagram, Cubic SiC, Inhomogeneous, SBD, SBH, Schottky Barrier Height, Semiconductor device modelling, Silicon Carbide, TCAD, Traps

## I. INTRODUCTION

SILICON CARBIDE (SiC) is a very promising material due to its wide bandgap (WBG) properties and has the potential to replace Silicon (Si) in various power electronic applications [1], [2]. The 3C-SiC is the only cubic polytype of Silicon Carbide, also found in literature as  $\beta$ -SiC [3]. Other major SiC polytypes, like 4H- and 6H-SiC, feature a hexagonal structure which introduces anisotropies in their electrical properties and are generally grouped as  $\alpha$ -SiC. Notably, power devices based on 3C-SiC inherit these isotropic electrical characteristics owned

to its cubic structure [4]. Such isotropic behaviour, mainly on the mobility and the impact ionization of carriers, is of significant importance for power devices [5]. Additionally, the cubic SiC features a slightly smaller energy bandgap ( $E_g$ ) compared to 4H-SiC which stands as a remarkable benefit for Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) by energetically locating the SiO<sub>2</sub>/3C-SiC interfacial traps in the Conduction band of 3C-SiC and in turn, resulting in a largely improved channel mobility [6]–[8]. Therefore, 3C-SiC MOSFETs are expected to have remarkably reduced conduction losses and increased reliability. Furthermore, 3C-SiC has the ability to be grown on cheap Si substrates (3C-SiC-on-Si) [9]. This allows large area wafers of material to be obtained and the cost for power devices fabrication to be reduced. Hence, 3C-SiC-on-Si power devices offer a cost-effective high performance wide bandgap technology platform where the improved devices performance, including high temperature operation, faster switching and lower losses can translate in a new generation, high performance and compact power electronics converters and accelerate the replacement of Si technology. The 3C-SiC-on-Si Schottky Barrier Diode (SBD) is a great candidate device because it combines the superior WBG material properties of SiC with the properties of SBDs such as negligible reverse recovery, low switching losses and high operating temperatures. But so far the formation of a reliable pure Schottky contact on SiC has been proved a rather challenging task, mainly suffering from high reverse leakage current [10].

The observed high leakage could be attributed to traps in bulk or at the interface between the metal and the semiconductor. Some of which could originate at the hetero-interface between Si and 3C-SiC e.g. induced by the lattice mismatch between the two materials [9], [11]. The presence of these defects and the high leakage is considered a bottleneck, hindering the commercialization of this technology [12]–[14]. Recent developments in the hetero-epitaxy process [15]–[18] suggest that 3C-SiC epi-layers with low bulk defect densities can soon

<sup>†</sup>This paper was submitted for review on the 10th of June 2019 and accepted on the 6<sup>th</sup> of September 2019.

A. Arvanitopoulos, S. Perkins and N. Lophitis are with the Institute for Future Transport and Cities and Faculty of EEC at Coventry University, Coventry, UK (e-mail: [arvanita@uni.coventry.ac.uk](mailto:arvanita@uni.coventry.ac.uk), [perkin19@coventry.ac.uk](mailto:perkin19@coventry.ac.uk), [n.lophitis@cantab.net](mailto:n.lophitis@cantab.net)).

M. Antoniou and P. Mawby was with the School of Engineering, University of Warwick, Coventry, UK (e-mail: [marina.antoniou@warwick.ac.uk](mailto:marina.antoniou@warwick.ac.uk), [p.a.mawby@warwick.ac.uk](mailto:p.a.mawby@warwick.ac.uk)).

M. R. Jennings is with the College of Engineering, Swansea University, Swansea, UK (e-mail: [m.r.jennings@swansea.ac.uk](mailto:m.r.jennings@swansea.ac.uk)).

K. N. Gyftakis is with the School of Engineering, The University of Edinburgh, Edinburgh, UK, (e-mail: [k.n.gyftakis@ieee.org](mailto:k.n.gyftakis@ieee.org)).

be obtained yet a better understanding of the causes of this leaky behaviour is needed as well as the location and type of defects and traps. A SBD is indeed an ideal test device for the study of the carrier transport mechanisms in any semiconductor material, the related physics and the impact of traps on the aforementioned. An appropriate model which can include those would allow to each a deep level of understanding of these complex phenomena and would stand out as a significant milestone for the creation of accurate designs which could in turn suppress the currently observed excessive leakage and sub-threshold current levels [19]–[21].

However, interfaces formed when SiC is brought into contact with metals, are rather complex carriers' transport systems [22]. The Schottky-Mott rule [23] is hardly ever observed in experiments, because it omits the impact of interface states and charges on the actual Schottky barrier height (SBH). Additionally, evidences of SBH inhomogeneity [24], discourage the adaptation of the Fermi Level ( $E_F$ ) pinning mechanism in explaining why the Schottky-Mott theory lacks in accuracy.

The inhomogeneity of the Schottky contacts has been widely investigated for the SiC SBDs. Non-uniform properties of the SBH create the conditions for an increased leakage current and a reduced blocking voltage value [25]. In [26]–[28], such variations in performance have been attributed to the existence of a Gaussian distribution for the SBH values around a mean value. Another simplistic approach suggests two independent Schottky barrier heights in parallel [29]–[31] to express the resultant current. Inhomogeneous Schottky contacts have also been described by the Tung's model [32], [33]. According to this model, spatially no uniformities of the barrier height are related to potential fluctuations at the Schottky interface forming patches. The patches dimensions are comparable with the space charge region width. Therefore, in low forward bias conditions the conducting low barrier patches have their current laterally pinched-off. Nonetheless, this fitting model is not applicable for diodes with significant degree of non-ideality ( $\eta > 1.21$ ) [30]. Furthermore, the physical interpretation of these fitting parameters remains mainly unanswered [34].

Interestingly, it has been shown that the inhomogeneity of the SBHs can be linked with the presence of defects of various origins, including both the materials and the devices [35]–[40]. In [41], defect clusters spatially located near the Schottky interface were responsible for the formation of partial low-barrier patches. Different SiC SBDs have been characterized in [42], with the existence of varying degrees of deep levels were identified as the cause for the observed differences in the leakage current. However, the physical mechanisms of these traps' influence on the barrier height of SiC SBDs are still mostly unclear.

In this paper, a model is developed based on interfacial traps, which obey conditional trapping / de-trapping rules, to describe the behaviour of the SBH in Schottky Metal/3C-SiC-on-Si interfaces. Advanced Technology Computer Aided Design (TCAD) is utilized along with measurements from a fabricated and characterized vertical 3C-SiC-on-Si SBD [43], to establish a deeply physical method, which allowed to link the non-

uniformities of the SBH with the impact of traps. Thereafter, a comprehensive model is suggested to accurately describe the observed excessive leakage currents in both forward and reverse operations. The model is built upon the presence of trap states at the Schottky interface and the physics, governing their effect on the carrier transport mechanisms, are revealed. It is, therefore, considerably more accurate to existing models, especially when the  $\eta$  value of SBDs exceeds unity.

According to the proposed TCAD model, the interfacial traps' dynamics can introduce a non-uniform distribution of the electric field at the surface of the Schottky contact. Such condition, is likely to enhance mechanisms like the image force lowering of the SBH, Field Emission (FE) or quantum barrier tunnelling mechanism and Trap-Assisted Tunnelling (TAT). This can significantly modify the number of carriers having the required kinetic energy to cross the barrier and, in turn, strongly affects the sub-threshold current. Moreover, in the post-threshold region, the forward current mainly depends on Thermionic Emission (TE) theory and is directly affected by the discrete bulk deep levels. Consequently, in this paper a complex contribution is modelled, that indirectly influences the barrier height and the resistivity, in accurately reproducing the sub-threshold, the on-state and the leakage current obtained by measurements.

The rest of this work is organized as follows. In section II, the physics-based theory of the proposed TCAD model is presented. In section III, the model is applied and validated utilizing measurements from a 3C-SiC-on-Si SBD. Finally, in section IV the conclusions of this work are presented.

## II. SUGGESTED MODEL FOR THE SUB-THRESHOLD CURRENT WITH THE IMPACT OF THE SCHOTTKY INTERFACE STATES

The terms defect, trap and state are referenced throughout this paper. A 'defect' is a generic term used to reference material anomalies responsible for the formation of traps. The term 'trap' specifically refers to the energy level that exists due to a defect of the crystal lattice and is able to conditionally capture charge carriers, temporarily or permanently. Traps can be of donor and/or acceptor type. The term 'state' indicates a trap spatially located at the Metal/Semiconductor interface demonstrating donor-like and/or acceptor-like behaviour.

### A. Linking the Interface states with a Uniform behaviour of the Schottky Barrier Height of the Schottky contact

In 3C-SiC SBDs the TE theory predicts a low sub-threshold current in forward bias. For each temperature value, only a fraction of majority carriers from the tail of the resulting occupation distribution features enough energy to overcome the Schottky barrier. However, elevated sub-threshold current levels are usually observed in fabricated devices. The main reason for this is the combined effect of both the Schottky interface and the bulk 3C-SiC defects. For a given temperature, the kinetic energy of the majority carriers remains unaltered and so does the shape of the occupation distribution in the conduction band. Thus, the observed high level of the sub-threshold current indicates that the presence of traps should introduce an effect on the potential energy at the interface

affecting the SBH value. This essentially modifies the ratio between the number of majority carriers able to cross the barrier and their total population at a specific temperature in the occupation distribution. Therefore, a TCAD model is proposed to imitate the impact of the traps and states existing in a 3C-SiC-on-Si SBD on the SBH value and, in turn, the overall electrical performance.

For the rest of this work, we assume n-type 3C-SiC-on-Si material and, thus, electrons as the majority carriers. The authors previously reported on the parameters and physical models of the bulk 3C-SiC aiming for representative TCAD modelling and simulation [44]. Utilizing this material physical model, the occupation distribution of electrons in the conduction band ( $E_C$ ) of the 3C-SiC is illustrated in Fig. 1.

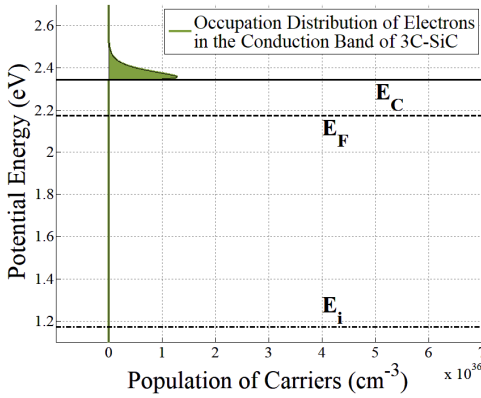


Fig. 1 The occupation distribution of the electrons in the  $E_C$  of 3C-SiC as resulted from the multiplication of the probability of occupation of state (Fermi-Dirac distribution) with the number of available Density of States in this band [44]. The calculations refer to a  $1.5 \times 10^{16} \text{cm}^{-3}$  n-type doped material and  $T = 300\text{K}$ . The zero potential energy in this illustration corresponds to the valence band ( $E_V$ ) of 3C-SiC.

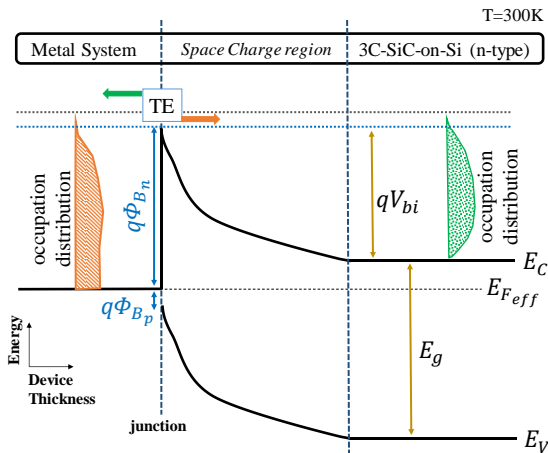


Fig. 2 For a defect-free Metal/3C-SiC-on-Si interface in Equilibrium and for a specific temperature, the TE predicts a small amount of carriers from the 3C-SiC occupation distribution in the  $E_C$  to be able to cross the barrier.

With the suggested TCAD model, the sub-threshold region of the forward log(I)-V characteristics of a SBD is utilized as a starting point. This region has been linked with the quality of the material [45], allowing therefore, for the various trap distributions to be identified. The identified traps can act either as recombination or generation centres depending on the bias conditions. An illustration of the band diagrams for a 3C-SiC-

on-Si SBD is shown in Fig. 2 for the case where no interfacial defects are considered. The TE theory predicts a specific amount of majority carriers from the occupation distribution, having the required energy, to flow to the metal side.

In equilibrium this current is balanced by the occupation distributions at the conduction bands of each system. Nonetheless, the existence of states at the Schottky interface disrupts this thermal equilibrium condition.

In this sub-section, we assume the Schottky interface to feature a trap profile comprising donor and/or acceptor-like states. Each type of these interfacial states is considered to have a continuous energetic distribution over a specific range of energies. The neutrality level ( $E_0$ ) level separates the acceptor from the donor levels. Traps energetically located below the  $E_F$  are more likely to carry an electron. On the contrary, the ones above the  $E_F$  are more likely to carry a hole. The acceptor traps carrying a hole are neutral, whilst they become charged (negatively) after capturing an electron. Similarly, donor traps carrying an electron are neutral unless they are occupied by a hole which makes them charged (positively). Hence, the fixed position of the traps'  $E_0$  and the position of the  $E_F$ , which varies with the applied voltage [46], essentially determine whether there exists additional charge and of what polarity at the Schottky interface.

Fig. 3, illustrates a case where the interface traps' profile consists of a continuous band of donor-like states. The donor states energetically above the  $E_F$  can become occupied forming a positive charge at the interface, the Schottky barrier becomes thinner and an effective built-in potential ( $V_{bi}^{eff}$ ) is formed. The difference between the actual built-in potential ( $V_{bi}$ ) and the  $V_{bi}^{eff}$ , can be seen in Fig. 3 as delta ( $\delta$ ). Notably,  $V_{bi}^{eff}$  depends directly on the quantity of ionized occupied states. Under zero bias there exists an increased quantity of majority carriers crossing the barrier because of Thermionic Field Emission (TFE). Field Emission (FE) current is also present and its importance depends on the concentration of these states.

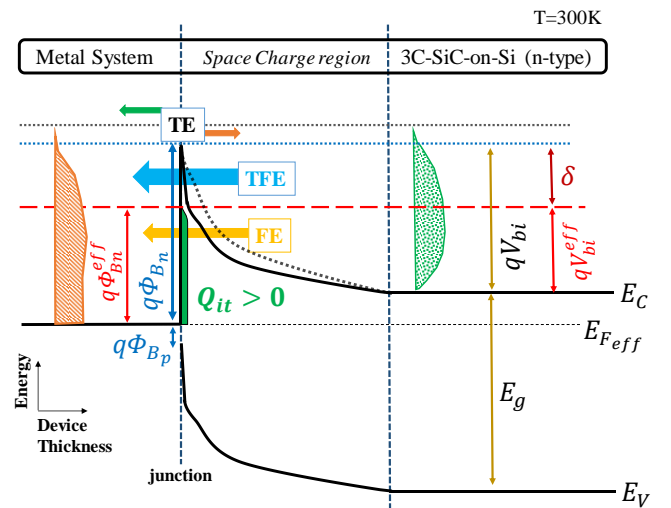


Fig. 3 Interfacial donor-like states can modify the equilibrium conditions enabling a greater portion of the electrons' occupation distribution to cross the barrier, thus resulting in more current in early forward bias. The dotted  $E_C$  represents the initial bending due to the depletion region without any effect from interfacial states.

The application of small forward bias ( $V_f$ ) moves all bands, including  $E_F$  upwards. This upward movement of  $E_F$  reduces the quantity of occupied donor-like states. Consequently, the positive charge at the interface reduces which in turn decreases  $\delta$ , although both  $V_{bi}$  and  $V_{bi}^{eff}$  decrease due to the  $V_f$ . The overall result is a significantly increased TE and at the same time a reduction of the TFE.

In the case the traps' profile consists of a continuous band of interfacial acceptor-like states with an energetic distribution covering a wide range above and below the  $E_F$ , then the states above the  $E_F$  are not occupied and thus they won't contribute at all to the current at the equilibrium condition. Similarly, although the acceptor-like states that lay below the  $E_F$  are highly likely to be occupied, their effect would be an increment of the SBH [47], which in turn would further limit the already small percentage of electrons that were allowed to cross the barrier with TE from the tail of their occupation distribution. The large concentration of the occupied acceptor-like states would degenerate the initial Metal/n-type 3C-SiC-on-Si with the emulated negative charge. Hence, although the barrier increases, this increment should feature a very thin triangular shape due to band bending. Therefore, the limited TE will be balanced by the TFE. Moreover, the recombination with Trap-Assisted Tunnelling will not be favoured due to the energetic positions of these states below the relative position of the  $E_F$  at the Schottky interface. For these positions in the energy axes, the barrier separating the activated acceptor-like states and the occupation distribution is relatively thick. In consequence, both direct (FE) and indirect tunnelling (TAT) would have a negligible contribution.

In Fig. 4, a scenario is illustrated where the interfacial traps' profile features a distribution of acceptor-like states closer to the  $E_C$  and a distribution of donor-like states below the  $E_0$ . At zero bias the position of the  $E_F$  at the interface in this case also determines a positive charge, however less compared to the one formed in Fig. 3. In turn, the induced  $\delta$  value and the amount of electrons able to transport with TFE will decrease.

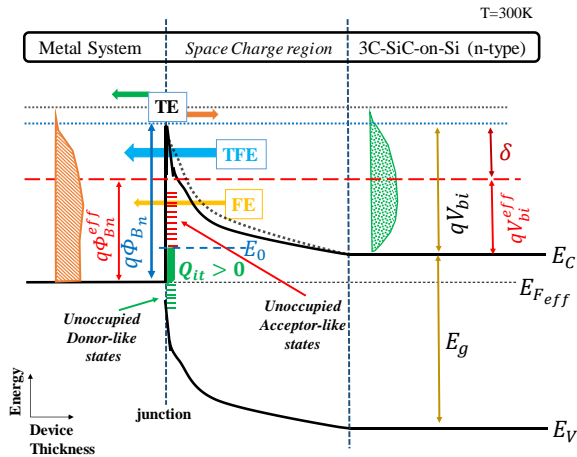


Fig. 4 At the Metal/3C-SiC-on-Si interface both donor and acceptor-like states exist separated by the notation of the neutrality level. In equilibrium the  $E_F$  determines a positive charge due to the donor-like states still energetically remaining above this level. The dotted  $E_C$  represents the initial bending due to the depletion region without any effect from interfacial states. Red states resemble acceptors and green resembles donor traps.

Fig. 5 depicts the same traps distribution but at higher forward bias, whilst  $V_f < V_{bi}$ . The relative position of the  $E_F$  at the Schottky interface moves upwards and under these conditions the acceptor-like states energetically located below the  $E_F$  can become occupied i.e. forming a negative charge.  $V_{bi}^{eff}$  becomes larger than the  $V_{bi}$  near the interface,  $\delta$  becomes negative and the charge causes the bands to bend and to form a “thin triangular shaped” region located at higher energies than the original barrier. In consequence, the effective barrier height increases. The contribution of TFE is sufficient through this thin region, although reduced compared to the previous bias condition in Fig. 4.

It is thus interesting to note the impact of bias condition on the effective built in potential as described in Fig. 4 and Fig. 5 where the interfacial traps' profile features a distribution of acceptor-like states closer to the  $E_C$  and a distribution of donor-like states below the  $E_0$ . The type of charged states and their strength changes with bias which directly affects the TFE current element. The FE in both these bias cases remain less important whereas the TE eventually becomes the dominating factor but only when the bias approach the  $V_{bi}$ .

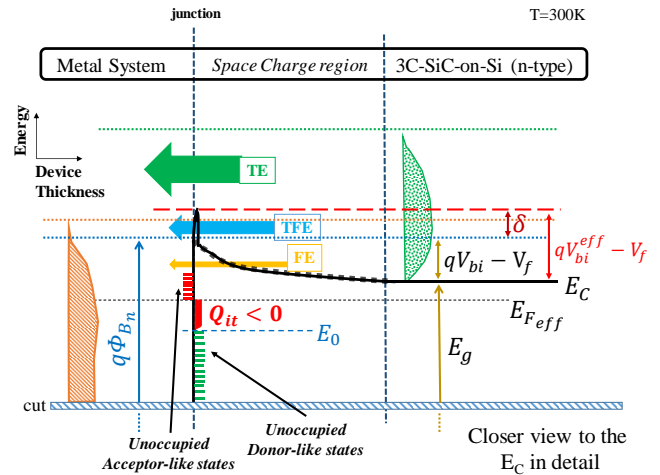


Fig. 5 At the Metal/3C-SiC-on-Si interface both donor and acceptor-like states exist separated by the notation of the neutrality level. The application of forward bias forces the  $E_F$  to move upwards. This alters the condition illustrated in Fig. 4 and acceptor-like traps now become ionized, thus highly likely to be occupied by an electron. This can balance the previously strong effect the charged donor-like states introduced to the barrier height.

Moreover, the presence of states in all aforementioned scenarios, i.e. in Fig. 3, Fig. 4, Fig. 5, can stimulate TAT too. The impact of forward bias on TAT is explained as follows. The Fermi level and the bands of the semiconductor move further up increasing their energy. Electrons tend to move from a higher  $E_F$  level to a lower  $E_F$  level side, thus, in these conditions they favour a move from the semiconductor to the Metal ( $E_F^{3C-SiC} > E_F^{Metal}$ ). Donor-like interfacial states above the  $E_F$  are able to release majority carriers to the Metal side (capture a hole). Thus, electrons in the occupation distribution of the n-type 3C-SiC-on-Si conduction band that are energetically located lower than the formed  $V_{bi}^{eff}$ , is now very likely to be captured from the ionized (occupied by holes) interfacial donor-states giving rise to TAT recombination. In addition, the donor-

like states can become positively charged, as described earlier, and induce band bending which further encourages the TAT mechanism. Similarly, acceptor-like states below  $E_F$ , absorb majority carriers in the vicinity of the interface from the semiconductor side. In this condition, they are able to capture holes from the Metal side, i.e. resembling the completion of a TAT recombination process. However, the TAT recombination originating from acceptor-like states below the  $E_F$  can be less intense compared to an equivalent case with donor-like states above the  $E_F$ . That is because tunnelling in the latter takes place at a lower energy where a higher part of the occupation distribution meets the correct energy requirement.

Therefore, the donor-like interfacial states contribute to the current by enhancing both the TFE and the indirect TAT recombination, whilst the acceptor-like ones mainly affect the TAT recombination processes. In both cases the resultant carriers' flow adds to the TE and shapes the sub-threshold current of the power diode.

In the extreme case of the presence of amphoteric interfacial traps [48], [49], then we have states at the same energy which can behave both as acceptors and donors. This is illustrated in Fig. 6. Depending on the forward bias level, positive charge, from the occupied donor-like states, is compensated by negative charge, originating from the occupied acceptor-like states. Accordingly, this can alter the contribution of the TFE, FE and TAT recombination to the resultant current.

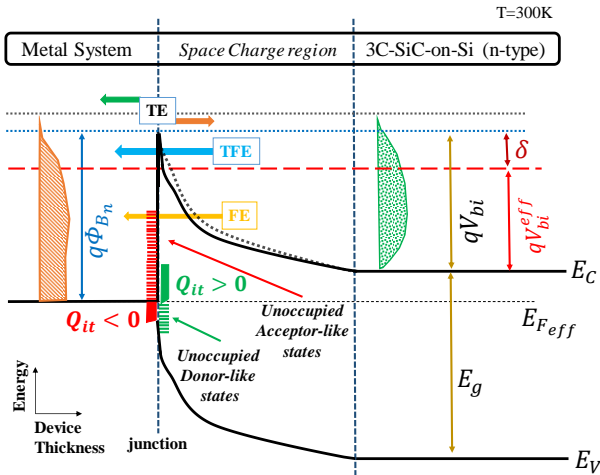


Fig. 6 Amphoteric interfacial traps at the Metal/3C-SiC-on-Si increase the complexity of the modelled effect on the SBH, by counterbalancing their influence, but also offer more degrees of freedom in matching characterized diodes. The dotted  $E_C$  represents the initial bending due to the depletion region without any effect from interfacial states.

Summarizing, the exact I-V relationship and the amount of majority carriers flowing towards the metal side, whilst in the sub-threshold region at every bias condition, is directly affected by the exact interface traps' profile. We argue that a spatially uniform distribution of this traps' profile along all the Schottky contact essentially defines a uniform behaviour of the SBH for this contact. Thereafter, this uniform behaviour can be disrupted by the introduction of multiple additional trap profiles featuring different spatial properties along the Schottky contact.

### B. Modelling the Non-Uniformities of the Schottky Barrier Height

Non-uniformities of the SBH can be modelled by defining multiple interfacial trap profiles which must act in patches at different locations on the Schottky contact. This is illustrated on the same band diagram in Fig. 7. The solid line resembles what could be a "patch region one", whilst the dashed one resembles what could be a "patch region two". In "patch region two" the profile of the states can be similar to what is described in Fig. 3– for simplicity we will refer to it as "profile A". In the "patch region one" there can exist "profile A" but also "profile B". The traps' "profile B" can introduce different states' distributions of a different neutrality level. In the scenario of Fig. 7, trap "profile B" consists of donor-like states close to the  $E_C$ . The  $Q_{itA}$  corresponds to the charged donor-like states from the "profile A". On the other hand, the  $Q_{itB}$  corresponds to additional charged donor-like states contained in the "profile B", which is energetically expanding in a narrower band of energies. This emulates a lower SBH value on the Schottky contact for the "patch region one" compared to the "patch region two" in which only the trap "profile A" applies. As with previous cases, the application of bias, strongly affects which one of those two trap profiles, and thus patches, will be more active. For  $V_f \ll V_{bi}$ , in "patch region one", both donor-like state distributions form a positive charge, creating enhanced electric field conditions at the interface. In turn, the TFE, FE and TAT recombination become more dominant compared to the rest of the contact area. Consequently, the  $\delta'$  becomes larger for "patch region one" ( $\delta' > \delta$ ), indicating a smaller  $V_{bi}^{eff}|_{A,B}$ , and thus a smaller SBH value, as shown in Fig. 7. With the applied forward bias increasing, both  $Q_{itA}$  and  $Q_{itB}$  reduce. Beyond a specific bias level, the  $E_F$  will eventually overcome the shallowest donor-like energy level of the interfacial trap "profile B" and the  $Q_{itB}$  will become zero. Thereafter, only the "profile A" will affect the carriers' transport, thus determining a larger effective built-in potential ( $V_{bi}^{eff}|_A$ ). In turn, the TAT recombination will reduce, resulting in a different  $\eta$  value, closer to unity. In consequence, the sub-threshold region of the log(I)-V curve will feature two different slopes. Likewise, even more complex curves of the sub-threshold current, can be associated with the presence and contribution of even more complex states profiles and patches at the Schottky interface.

The spatial information of any additional traps' profile, that accounts for a localized non-uniformity of the SBH, remains arbitrary and can be adjusted given the actual states distribution for each Schottky contact. Thus, it is assumed that any patch definition will expand within a particular percentage of the total Schottky contact area. Currently, it is not possible to determine the exact location and the dimensions of the patch, responsible for the inhomogeneity, within the Schottky active area. Given the accurate TCAD model of the diode and the utilization of the area factor, the percentage of the actual active area over which the additional trap-profile spatially expands should be decided with simulations.

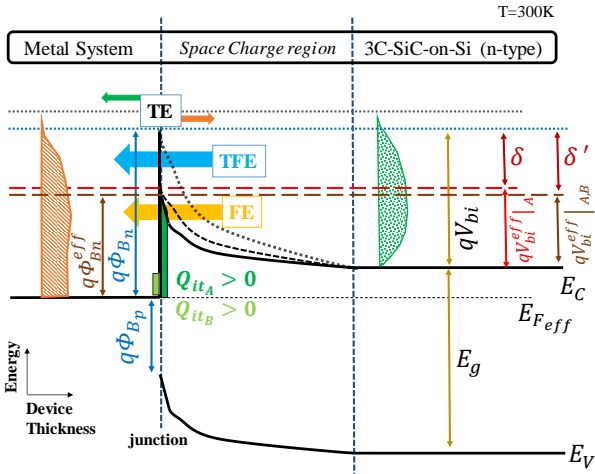


Fig. 7 Non-uniformities of the SBH resembled on the same band diagram. Two interfacial trap profiles, A and B, featuring different donor-like state distributions are able to model a first patch region (solid  $E_C$ ). The dashed  $E_C$  corresponds to the effect induced considering only the trap profile A, which is a similar case to the one shown in Fig. 3 and can resemble a second patch. The dotted  $E_C$  represents a case without any effect from interfacial states.

### III. ATTRIBUTING THE SUB-THRESHOLD CURRENT TO THE INTERFACIAL STATES – CASE STUDY

#### A. The 3C-SiC-on-Si Schottky Barrier Diode TCAD modelling methodology

The vertical power SBD, considered in this work, features cylindrical contacts and its fabrication was reported in [43]. The Schottky interface was formed from the evaporation of Platinum (Pt) on a  $4\mu\text{m}$  thick non-freestanding drift layer of 3C-SiC material, epitaxially grown on Si. The area of the Schottky contact is smaller than that of the back Titanium (Ti) ohmic one in order to deal with parasitic capacitance elements of the device [50]. Consequently, a fraction of 3C-SiC surface is exposed on the top. A buffer layer of  $1\mu\text{m}$  is included resulting in a punch-through design. The Si substrate is approximately  $500\mu\text{m}$  thick [51], whilst all the layers are Nitrogen (N) doped. The design details can be identified in the device cross-sectional view illustrated in Fig. 8.

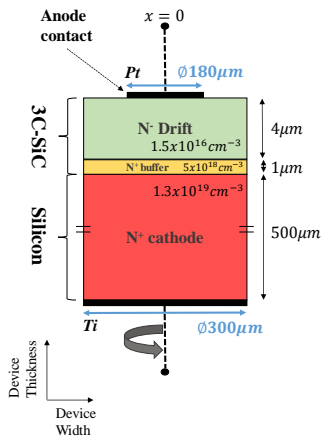


Fig. 8 The TCAD simulated cylindrical asymmetric SBD structure based on an isotope 3C-SiC on Si hetero-interface.

The annealing process for contact smoothing eventually forms Platinum Silicides (PtSi) [47]. The work function of PtSi is still greater than the electron affinity of the n-doped cubic SiC

( $\Phi_{PtSi} > X_{3C}$ ). This indicates that, after contact, majority electrons flow from the semiconductor to the metal to reach equilibrium. This flow lowers the potential energy of the bands at the 3C-SiC side. The SBH, or metal-semiconductor work function ( $\Phi_B$ ), formed governs the current transport in the SBD.

The band diagram of the investigated SBD is illustrated in Fig. 9. The work function of thin PtSi,  $q\Phi_{PtSi} = 4.98\text{ eV}$  [52] and the validated bulk 3C-SiC parameters [44], [53], listed in Table I, have been employed in the calculations. For the accurate representation of the  $E_F$  in the bulk, the band gap narrowing phenomenon has been considered in the calculations in (1), where,  $n_0$  is the equilibrium concentration of majority electrons at  $T = 300\text{K}$ . The band diagram assists in identifying the relative position of the  $E_F$  at the Schottky interface, which is a crucial information for the discussed model.

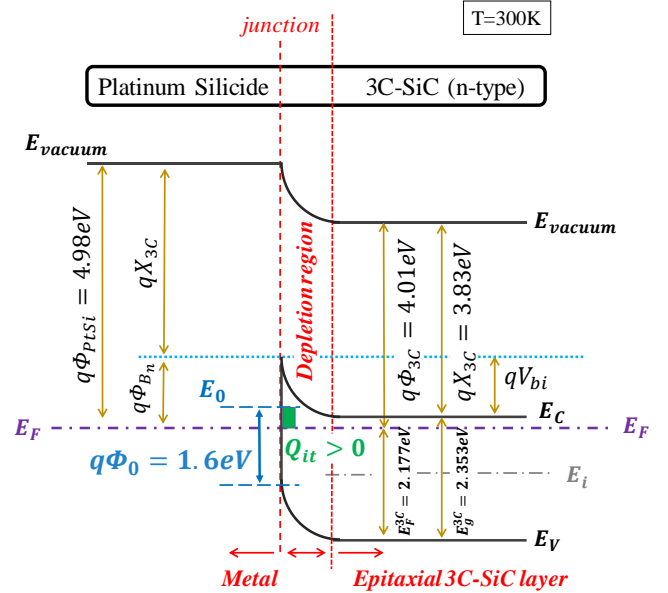


Fig. 9 The band-diagram of the Schottky contact between n-type 3C-SiC-on-Si and thin PtSi. The interfacial traps' Profile A, in Table II, and the position of the  $E_F$  decide the formed positive interface charge.

Table I  
Basic parameters of bulk 3C-SiC for the Band Diagram

Parameter	Bulk 3C-SiC
Bandgap ( $E_g$ ) at $T=300\text{K}$ [eV]	2.353
Intrinsic carrier concentration ( $n_i$ ) [ $\text{cm}^{-3}$ ]	0.2285
Electron affinity [eV]	3.83

$$n_0 = n_i \exp\left(\frac{E_F - E_g/2}{kT}\right) \quad (1)$$

#### B. The suggested model on the sub-threshold current assuming a spatially Uniform SBH behaviour

Synopsys Sentaurus Structure Editor [54] and Synopsys Sentaurus Device [55] were utilized to simulate the two dimensional model of the SBD depicted in Fig. 8 with the application of a proper area factor value. The design methodology includes an initial simulation without the inclusion of any bulk or interfacial trap profiles in order to obtain the sub-threshold current as predicted from the Thermionic Emission (TE) only. Thereafter, the comparison

between the obtained  $\log(I)$ - $V$  and the measurements assists in deciding which case of interfacial trap distributions, from the ones described in Section II, is more likely to cause the differentiations between the simulated and the observed current. The band diagram of the diode largely assists towards this direction because it contains critical information, i.e. the position of the  $E_F$ . Utilizing the information of the relative position of the  $E_F$  at the Schottky interface and the selected case of the traps' profile, the distribution properties of the donor and/or acceptor-like states within this trap profile are roughly estimated. The mean and sigma values of these Gaussian distributions are set in such a way so that the neutrality level can be determined. Thus, the  $E_0$  is not defined in the simulations, rather it arises as the energy level that separates the two Gaussian distributions of the interfacial traps' profile. Finally, the concentration and the exact range of energies for each state type are identified through extensive simulations and comparison to the experimental results.

According to the suggested model in this work, a trap profile is considered featuring states with a continuous band of energies at the PtSi / 3C-SiC-on-Si interface. Focusing on the sub-threshold current measurements of the investigated diode, subsequent TCAD simulations were carried out to identify the distributions of these interfacial states. The best match between measurements and simulations was obtained with the introduction of a traps' profile with both donor and acceptor-like distributions (Profile A), resembling the case illustrated in Fig. 4, and properties as listed in Table II. The result, which compares the measurements with the simulations considering uniform SBH behaviour, is shown at the end of this sub-section.

Table II  
Identified Defects in the investigated 3C-SiC-on-Si SBD

Traps' Description	Type	Concentration	Energetic Distribution
<i>Schottky interfacial states resulting in a specific effect on the SBH (Profile A)</i>	Donor	$6 \times 10^{12} \text{ cm}^{-2}$	Gaussian $E_{Mid}^{from E_V} = 0.8 \text{ eV}$ , $E_{Sig} = 0.8 \text{ eV}$
	Acceptor	$5 \times 10^{12} \text{ cm}^{-2}$	Gaussian $E_{Mid}^{from E_C} = 0.4 \text{ eV}$ , $E_{Sig} = 0.4 \text{ eV}$
<i>Bulk deep levels due to 3C-SiC/Si hetero-interface</i>	Acceptor	$1.5 \times 10^{16} \text{ cm}^{-3}$	Single Level Activation Energy [56]: $E_{from E_V} = 0.5 \text{ eV}$

The simulations revealed that the  $E_0$ , separating the two distributions of the traps' Profile A, should be energetically considered above the  $E_F$  in equilibrium, as illustrated in Fig. 10. The notation  $\Phi_0$  is used to identify the neutrality level in respect to the valence band ( $E_V$ ). This implies that a positive charge is formed at the Schottky interface due to occupied interfacial donor-like deep levels, as shown in Fig. 9.

The characterized states, in Profile A, are coupled with the Schottky contact through a calibrated nonlocal TAT model [57]. The values of the parameters for this model were fine-tuned for 3C-SiC, as shown in Table III, to achieve the best match to the experimental data [43]. The tunnelling mass of

electrons is a dimensionless property of the material that forms the tunnelling barrier, whereas the prefactor ( $g_C$ ) refers to the ratio between the effective [58] and the free electrons Richardson constant [59].

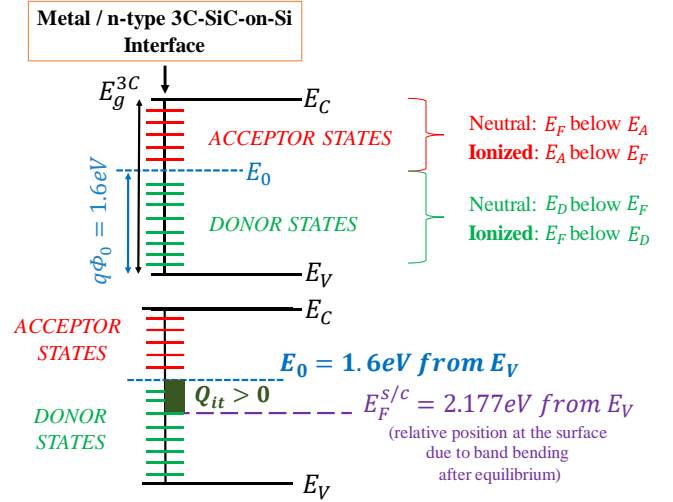


Fig. 10 The continuous band of donor and acceptor states in conjunction to the assumed position of the  $E_0$  and the calculated position of the  $E_F$  for the n-type 3C-SiC-on-Si produces a positive charge at the Schottky interface while in equilibrium. The energies of the acceptor and donor states are indicated as  $E_A$  and  $E_D$  correspondingly.

Table III  
Mobility and Tunnelling parameters

Parameter	3C-SiC	
	electrons	holes
Mobility [ $\text{cm}^2/\text{Vs}$ ]	650	50
Tunnelling mass [in units of $m_0$ ]	0.05	0.05
Interface prefactor ( $g_C$ )	$1 \times 10^{-3}$	$0.66 \times 10^{-2}$

Further, to accurately emulate the on-state performance, the influence of bulk acceptor traps was also required in the simulations. These deep levels, originating from the 3C-SiC/Si hetero-junction region, are modelled to spatially distribute in a uniform manner throughout the 3C-SiC epilayer. The properties of the bulk traps are given in Table II. Such bulk traps affect the majority carriers' transport by capturing and releasing electrons, which decreases their mobility and, in turn, increases the simulated on-resistance. The defects generated at the hetero-interface of 3C-SiC to Si, are mainly attributed to the out-diffusion of Si from the substrate in order to contribute to the formation of the overlying SiC layer [15]. To the credit of this work, the TCAD simulation results are in line with reported observations for the 3C-SiC, which consider the Silicon vacancy ( $V_{Si}$ ) to act as a deep acceptor level [60]. Moreover, the observed simulated behaviour of the introduced deep levels originating from the 3C-SiC/Si hetero-interface resembles the presence of Stacking faults (SFs). The SFs in 3C-SiC are highly electrically active also causing scattering of electrons especially in n-type materials [61]. This source of increased resistivity is the main cause for power device degradation. More specifically, the accumulated N at such crystallographic defects create preferable paths for the current to flow in 3C-SiC [62].

All the identified defects (interfacial traps' Profile A and bulk traps), affect the carrier transport and accordingly the shape of



the SBD log(I)-V curve. Simulation results in Fig. 11 give an insight of how the presence of these defects impacts the current mechanisms, which are subsequently activated. In particular, in curve 1 only the TE is activated in the simulations of the power device. In curve 2, the inclusion of the interfacial traps' Profile A does not have a strong contribution in the sub-threshold current unless additional interacting mechanisms are involved to describe its effect on the SBH. The deep level bulk acceptor traps mainly affect the post-threshold part of the I-V characteristic by draining majority carriers and, thus, limiting the on-state current level. In curve 3, the image force lowering, due to the depletion region charge and the charged donor-like interface states, signifies the contribution of the TFE current. This results in more carriers crossing the barrier for the same potential energy and temperature. In curve 4, the barrier tunnelling mechanism is activated to account for the FE of electrons. Finally, in curve 5, the calibrated non-local TAT model accommodates for the indirect tunnelling of electrons through the identified interfacial states of Profile A.

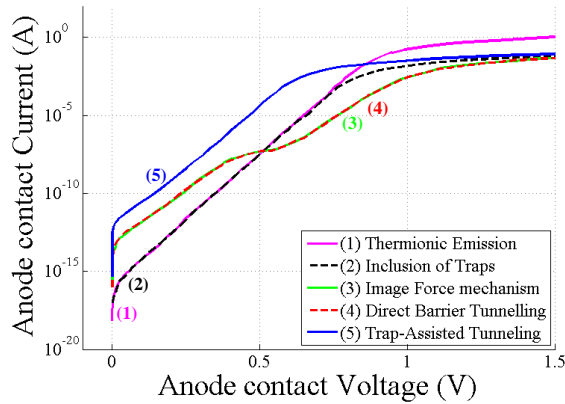


Fig. 11 The combined contribution of the identified traps in Table II and their effect on the majority carriers' transport after TCAD simulations of the investigated 3C-SiC-on-Si SBD.

Interestingly, the simulations in Fig. 11 indicate an almost negligible contribution of the FE mechanism to the sub-threshold current. In fact, the specification of the interfacial states distributions is responsible for this behaviour. The positive charge formed due to the portion of the donor-like states that become occupied is relatively small. Thus, the resultant band bending induced by this charge is not significant and the barrier shape does not get thin enough to strengthen the FE of the majority carriers. At the same time, the occurred band bending encourages TAT by moving the occupation distribution of electrons closer to the interfacial states. If the distribution of the interfacial states featured only donor-like traps as shown in Fig. 3, then the FE element of the total current would be greater at the expense of the TAT element. Comparing the curve 1, in Fig. 11, to the final simulated forward bias log(I)-V curve of the SBD in Fig. 12, it is clear that the sub-threshold current is a representative indicator of the semiconductor material quality in 3C-SiC-on-Si.

The proposed TCAD model, with the inclusion of the identified defects in Table II, is able to replicate accurately both the forward and the reverse electrical performance of the SBD. A very good match between the simulations and the

measurements is obtained, as shown in Fig. 12 and Fig. 13.

Notably, the effect of the interfacial traps' Profile A, in Table II, suggests a specific behaviour of the SBH. Although this simulated behaviour is in agreement with the forward experimental data, it is still weak in accurately predicting the sub-threshold current for early forward bias conditions, as seen in Fig. 12.

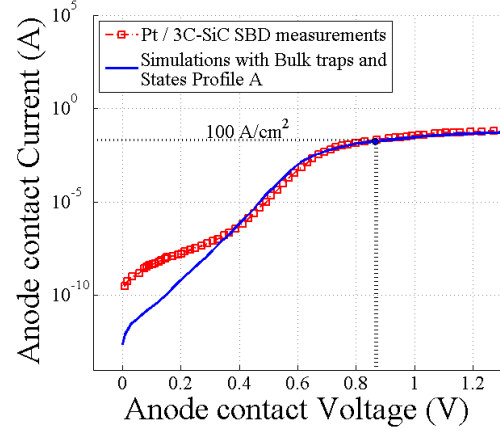


Fig. 12 The TCAD simulated log(I)-V characteristics of the investigated Pt / 3C-SiC-on-Si SBD after the inclusion of the traps in Table II is in a very good agreement to the experimental data [43].

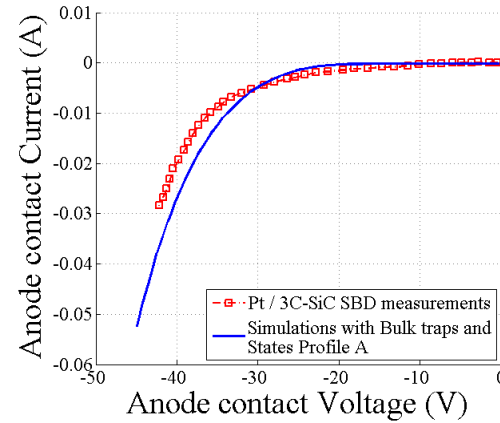


Fig. 13 The reverse characteristics can also be accurately predicted with the inclusion of the traps in Table II.

### C. Expanding the suggested model to accommodate for the Inhomogeneous features of the investigated Schottky contact

It is reasonable to argue that the Schottky interface in SiC won't feature uniform properties in the lateral direction [63]–[68]. In the case of the investigated SBD, the small mismatch observed in the early forward bias stages in Fig. 12, can be attributed to such a SBH inhomogeneity.

To model this in the simulations, a patch region on the Schottky contact is assumed to feature a second profile of interfacial states, additive to the existing Profile A. Within this small part of the contact, the added profile should consist of a donor-like states' distribution energetically located above the relative position of the  $E_F$  at the Schottky interface. This will directly link their impact only to a limited set of early forward bias values; this corresponds to the simulated forward bias log(I)-V region featuring the mismatch with the measurements. The concentration of these added donor-like states should be

higher than the one defined in the previously identified Profile A, in order to ensure an elevated sub-threshold current. As long as the  $E_F$  is below these states, the likelihood of their switching between the unoccupied and the charged state is high. Further, energetically above these extra donor-like states, an additional acceptors' distribution succeeds, also with a higher concentration compared to the corresponding one in the Profile A. This will balance the sub-threshold current, after a specific value of the forward bias, by locally increasing the resistance. Thus, a trade-off is formed between these two new concentration values. These additional interfacial distributions of states are grouped together, in Table IV, as Profile B and their properties were determined through simulations. The patch region, where both traps' Profile A and B apply gives accurate result when it covers 30% of the total Schottky contact. Essentially, this patch region describes the non-uniformity of the SBH. The addition of the interfacial traps' Profile B in the TCAD model and its supplementary effect on the electrons' transport mechanisms, results in simulations that can accurately predict the sub-threshold and the on-state electrical performance. This is shown in Fig. 14.

Table IV  
Additional Interfacial Trap profile to model the SBH Inhomogeneity

Traps' Description	Type	Concentration	Distributions	
			Energetic	Spatial
Schottky interfacial states to model a Non-Uniform SBH value (Profile B)	Donor	$4 \times 10^{19} \text{ cm}^{-3}$	Gaussian $E_{Mid}^{from Ev} = 1 \text{ eV}$ $E_{Sig} = 0.3 \text{ eV}$	Covering 30% of the Schottky contact in the «Device Width» axis
	Acceptor	$2 \times 10^{18} \text{ cm}^{-3}$	Gaussian $E_{Mid}^{from Ev} = 1.7 \text{ eV}$ $E_{Sig} = 0.4 \text{ eV}$	

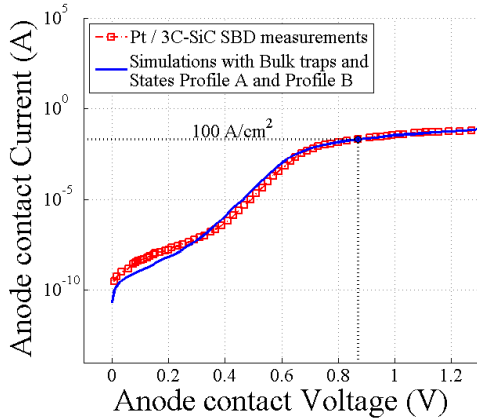


Fig. 14 The inclusion of the interfacial states' Profile B, which acts as additive to the states' Profile A, makes the suggested TCAD model able to predict the observed non-uniformity of the SBH in the lowest part of the measured log(I)-V characteristics of the SBD [43]. The traps' Profile B is described in Table IV.

Moreover, as shown in Fig. 15, the assumed patch region on the simulated Schottky contact does not influence the very good prediction of the reverse performance, obtained previously in Fig. 13. In reverse bias, the main contribution on the current is due to TAT generation processes through the ionized donor-like states. With the increased reverse bias, the relative position of the  $E_F$  in Fig. 10 will energetically drop lower, for all the

Schottky contact, and more interfacial donor-like states will become occupied by a hole. Further, the electrons will now favour a move from the Metal side to the semiconductor side ( $E_F^{Metal} > E_F^{3C-SiC}$ ). The generation process is then realized with these occupied states firstly emitting the captured hole to the  $E_V^{Metal}$  and then emitting the trapped electron to the  $E_C^{3C-SiC}$ . This two-step process depends on the concentration of the interfacial donor-like states which were energetically located below the  $E_F$  in equilibrium. The specifications of the additional trap Profile B, in Table IV, will not entail any change to the concentration of these traps, therefore, the Fig. 13 and Fig. 15 are almost identical.

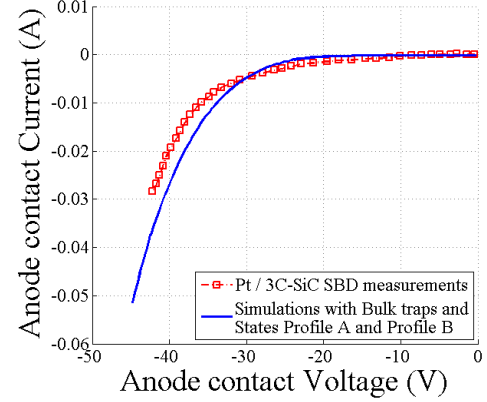


Fig. 15 The inclusion of the additional interfacial states' Profile B in Table IV, does not disrupt the donor-like state distribution below the  $E_F$ , as defined in the traps' Profile A in Table II, thus the generation current in reverse bias will remain mainly unaltered.

When all the identified defects, as described in Table II and Table IV, are included in the TCAD model, the simulation results are in excellent agreement with the measurements regarding both the forward (sub-threshold, on-state) and reverse bias conditions. Comprehensively, the final matching is also illustrated in Fig. 16 in the linear scale.

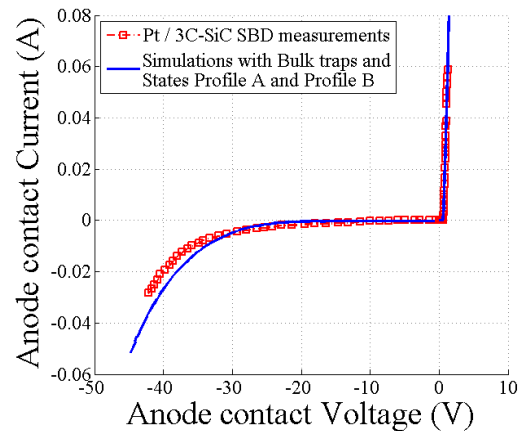


Fig. 16 The predicted I-V from the proposed model in this work, and the measurements [43] indicate that the identified defects accurately describe the net electrical performance of the diode.

#### IV. CONCLUSIONS

In this paper, the development of a highly accurate and deeply physical model is proposed to describe the non-ideal behaviour of the SBH in SBDs due to the presence of defects.

To validate the model, the experimental performance of a fabricated 3C-SiC-on-Si SBD is used. Various combinations and cases of traps were regarded and their sub-sequent effect on the carrier transport mechanisms were thoroughly presented, analysed and illustrated. As the sub-threshold region of the  $\log(I)$ - $V$  measurements carries considerable information relevant to these defects, it is exploited in identifying their properties. According to the proposed model, an interfacial traps' profile is initially considered by modelling both donor-like and acceptor-like states. Each state type features its own energetic distribution and concentration. It has been shown that the specifications of a single interfacial traps' profile, spatially expanding over the total active area, determines a certain SBH behaviour owned to the effect of these traps on the carrier transport mechanisms. By modelling the additional traps profiles which are spatially present over parts of the Schottky interface, it has been achieved for the first time to model the observed inhomogeneity of the SBH and to explain the physics behind it. In consequence, the suggested model is able to sufficiently predict complex sub-threshold leakage current – voltage relationships by appropriately characterizing these trap profiles. This can be considered an advantage over the Tung's model, which can also be utilized to describe non-uniform Schottky contacts, but its application is delimited by the ideality factor value of the diode.

The way the determined defects affect the carrier transport mechanisms has also been analysed, with the role of the Schottky interfacial states on the TAT generation and recombination current revealed to depend on the bias condition. Since both the sub-threshold and the leakage current of the SBD can be accurately described and explained by the model, the quality of the Schottky contact (in terms of the presence of states) can be evaluated and understood. The on-state has been found to be mainly affected by bulk deep levels. In this work these deep levels have been characterized as  $V_{Si}$  acceptor type in the 3C-SiC epilayer. These defects are due to the out-diffusion of Si originating from the hetero-interface between the 3C-SiC and the substrate. Finally, potential similarities of the modelled bulk traps, to the reported electrical behaviour of SFs in 3C-SiC is encouraging and requires further investigation.

In conclusion, the TCAD model, with the inclusion of the identified interfacial trap profiles and bulk deep levels, allowed for an excellent prediction of the total electrical performance of the investigated 3C-SiC-on-Si SBD. Indeed, the simulation results, presented in this work, are in excellent agreement with the measurements for both the forward and the reverse bias. The ability to analyse and model such complex behaviour enables the optimization of fabrication strategies that would allow the reduction/elimination of interfacial states but also the design of device structures which could mitigate from those. Finally, it should be highlighted that the suggested model is not limited only to 3C-SiC-on-Si substrate diodes, rather it can be applied to any SBD, enabling for the identification of the defects (both Schottky interface states and bulk traps) and their sub-sequent effect on the electrical performance of the power diode. To also highlight the ability of the model to work when strong non-idealities exists and to provide the relevant physical insight of

the underlying causes of those, where other models, e.g. Tung's model, do not work.

## REFERENCES

- [1] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017. doi:10.1109/TIE.2017.2652401
- [2] Y. K. Sharma, "Introductory Chapter: Need of SiC Devices in Power Electronics - A Beginning of New Era in Power Industry," in *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*, Y. K. Sharma, Ed. IntechOpen, 2018, pp. 1–16
- [3] H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies," *J. Appl. Phys.*, vol. 76, no. 3, pp. 1363–1398, 1994. doi:10.1063/1.358463
- [4] F. Ciobanu, G. Pensl, H. Nagasawa, A. Schöner, S. Dimitrijević, K. Y. Cheong, V. V. Afanas'ev, and G. Wagner, "Traps at the Interface of 3C-SiC/SiO<sub>2</sub>-MOS-Structures," *Mater. Sci. Forum*, vol. 433–436, no. Table 1, pp. 551–554, 2003. doi:10.4028/www.scientific.net/MSF.433-436.551
- [5] A. A. Lebedev, S. P. Lebedev, V. Y. Davydov, S. N. Novikov, and Y. N. Makarov, "Growth and investigation SiC based heterostructures," in *15th Biennial Baltic Electronics Conference (BEC)*, 2016. doi:10.1109/BEC.2016.7743717, pp. 5–6
- [6] M. Krieger, G. Pensl, M. Bakowski, and A. Schöner, "Hall Effect in the Channel of 3C-SiC MOSFETs," *Mater. Sci. Forum*, vol. 485, pp. 441–444, 2005. doi:10.4028/www.scientific.net/MSF.483-485.441
- [7] K. K. Lee, Y. Ishida, T. Ohshima, K. Kojima, Y. Tanaka, T. Takahashi, H. Okumura, K. Arai, and T. Kamiya, "N-Channel MOSFETs Fabricated on Homoepitaxy-Grown 3C-SiC Films," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 466–468, 2003
- [8] T. O. Hshima, K. K. Lee, Y. Ishida, K. Kojima, Y. Tanaka, T. Takahashi, M. Yoshikawa, H. Okumura, K. Arai, and T. Kamiya, "The Electrical Characteristics of Metal-Oxide-Semiconductor Field Effect Transistors Fabricated on Cubic Silicon Carbide," *Jpn. J. Appl. Phys.*, vol. 42, 2003. doi:10.1143/JJAP.42.L625
- [9] G. Ferro, "3C-SiC Heteroepitaxial Growth on Silicon: The Quest for Holy Grail," *Crit. Rev. Solid State Mater. Sci.*, vol. 40, no. 1, pp. 56–76, 2015. doi:10.1080/10408436.2014.940440
- [10] F. Roccaforte, F. Giannazzo, V. Raineri, F. Roccaforte, F. Giannazzo, and V. R. Nanoscale, "Nanoscale transport properties at silicon carbide interfaces," *J. Appl. Phys.*, vol. 43, 2011
- [11] P. Hens, G. Wagner, A. Hölzling, R. Hock, and P. Wellmann, "Dependence of the seed layer quality on different temperature ramp-up conditions for 3C-SiC hetero-epitaxy on Si (100)," *Thin Solid Films*, vol. 522, pp. 2–6, 2012. doi:10.1016/j.tsf.2011.10.177
- [12] A. Stefanskiy, Ł. Starzak, and A. Napieralski, "Silicon Carbide Power Electronics for Electric Vehicles," *2015 Tenth Int. Conf. Ecol. Veh. Renew. Energies*, pp. 1–9, 2015. doi:10.1109/EVER.2015.7138047
- [13] G. Colston, S. D. Rhead, V. A. Shah, O. J. Newell, I. P. Dolbnya, D. R. Leadley, and M. Myronov, "Mapping the strain and tilt of a suspended 3C-SiC membrane through micro X-ray diffraction," *Mater. Des.*, vol. 103, pp. 244–248, 2016. doi:10.1016/j.matdes.2016.04.078
- [14] Y. Li, Z. Zhao, L. Yu, Y. Wang, Z. Yin, Z. Li, and P. Han, "Heteroepitaxial 3C-SiC on Si (100) with flow-modulated carbonization process conditions," *J. Cryst. Growth*, vol. 506, no. September 2018, pp. 114–116, 2019. doi:10.1016/j.jcrysgro.2018.09.037
- [15] F. La Via, A. Severino, R. Anzalone, C. Bongiorno, G. Litrico, M. Maureri, M. Schoeler, P. Schuh, and P. Wellmann, "From thin film to bulk 3C-SiC growth: Understanding the mechanism of defects reduction," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 57–68, 2018. doi:10.1016/j.mssp.2017.12.012
- [16] H. Nagasawa, K. Yagi, T. Kawahara, and N. Hatta, "Reducing Planar Defects in 3C-SiC," *Chem. Vap. Depos.*, vol. 12, pp. 502–508, 2006. doi:10.1002/cvde.200506466
- [17] D. Chaussende, F. Mercier, A. Boule, F. Conchon, and M. Soueidan, "Prospects for 3C-SiC bulk crystal growth," vol. 310, pp. 976–981, 2008. doi:10.1016/j.jcrysgro.2007.11.140
- [18] R. Anzalone, C. Locke, J. Carballo, N. Piluso, A. Severino, G. D. Arrigo, A. A. Volinsky, F. La Via, and S. E. Sadow, "Growth rate effect on 3C-SiC film residual stress on (100) Si substrates," vol. 648, pp. 143–146,

2010. doi:10.4028/www.scientific.net/MSF.645-648.143
- [19] J. Eriksson, M. H. Weng, F. Roccaforte, F. Giannazzo, S. Leone, and V. Raineri, "Toward an ideal Schottky barrier on 3C-SiC," *Appl. Phys. Lett.*, vol. 95, no. 8, 2009. doi:10.1063/1.3211965
- [20] S. Roy, C. Jacob, and S. Basu, "Current transport properties of Pd/3C-SiC Schottky junctions with planar and vertical structures," *Solid State Sci.*, vol. 6, no. 4, pp. 377–382, 2004. doi:10.1016/j.solidstatesciences.2004.01.003
- [21] J. Komiya, Y. Abe, S. Suzuki, T. Kita, and H. Nakanishi, "Schottky diode characteristics of 3C-SiC grown on a Si substrate by vapor phase epitaxy," *J. Cryst. Growth*, vol. 275, no. 1–2, pp. 1001–1006, 2005. doi:10.1016/j.jcrysgro.2004.11.155
- [22] D. K. Schroder, "Carrier Lifetimes in Silicon," vol. 44, no. 1, pp. 160–170, 1997
- [23] W. Monch, "On the physics of metal-semiconductor interfaces," *Reports Prog. Phys.*, vol. 53, no. 3, pp. 221–278, Mar. 1990. doi:10.1088/0034-4885/53/3/001
- [24] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Appl. Phys. Rev.*, vol. 1, no. 011304, 2014. doi:10.1063/1.4858400
- [25] R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," *Phys. Rev. B*, vol. 45, no. 23, pp. 13509–13523, 1992. doi:10.1103/PhysRevB.45.13509
- [26] V. Kumar, A. S. Maan, and J. Akhtar, "Barrier height inhomogeneities induced anomaly in thermal sensitivity of Ni/4H-SiC Schottky diode temperature sensor," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 32, no. 4, p. 041203, 2014. doi:10.1116/1.4884756
- [27] M. E. Aydin, N. Yildirim, and A. Türüt, "Temperature-dependent behavior of Ni/4H-nSiC Schottky contacts," *J. Appl. Phys.*, vol. 102, no. 4, 2007. doi:10.1063/1.2769284
- [28] G. S. Chung, K. S. Kim, and F. Yakuphanoglu, "Electrical characterization of Au/3C-SiC/n-Si/Al Schottky junction," *J. Alloys Compd.*, vol. 507, no. 2, pp. 508–512, 2010. doi:10.1016/j.jallcom.2010.08.004
- [29] J. H. Werner and H. H. Güttler, "Barrier inhomogeneities at Schottky contacts," *J. Appl. Phys.*, vol. 69, no. 3, pp. 1522–1533, 1991. doi:10.1063/1.347243
- [30] S. U. Omar, T. S. Sudarshan, T. A. Rana, H. Song, and M. V. S. Chandrashekar, "Large barrier, highly uniform and reproducible Ni-Si/4H-SiC forward Schottky diode characteristics: Testing the limits of Tung's model," *J. Phys. D: Appl. Phys.*, vol. 47, no. 29, 2014. doi:10.1088/0022-3727/47/29/295102
- [31] J. L. Li, Y. Li, L. Wang, Y. Xu, F. Yan, P. Han, and X. L. Ji, "Influence of deep defects on electrical properties of Ni/4H-SiC Schottky diode," *Chinese Phys. B*, vol. 28, no. 2, 2019. doi:10.1088/1674-1056/28/2/027303
- [32] R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," *Phys. Rev. B*, vol. 45, no. 23, pp. 13509–13523, 1992
- [33] J. P. Sullivan, R. T. Tung, M. R. Pinto, and W. R. Graham, "Electron transport of inhomogeneous Schottky barriers: A numerical study," *J. Appl. Phys.*, vol. 70, no. 12, pp. 7403–7424, 1991. doi:10.1063/1.349737
- [34] P. M. Gammon, A. Pérez-Tomás, V. A. Shah, O. Vavasour, E. Donchev, J. S. Pang, M. Myronov, C. A. Fisher, M. R. Jennings, D. R. Leadley, and P. A. Mawby, "Modelling the inhomogeneous SiC Schottky interface," *J. Appl. Phys.*, vol. 114, no. 22, 2013. doi:10.1063/1.4842096
- [35] F. La Via, M. Camarda, and A. La Magna, "Mechanisms of growth and defect properties of epitaxial SiC," *Appl. Phys. Rev.*, vol. 1, no. 3, 2014. doi:10.1063/1.4890974
- [36] Y. Yamamoto, S. Harada, K. Seki, A. Horio, T. Mitsuhashi, D. Koike, M. Tagawa, and T. Ujihara, "Low-dislocation-density 4H-SiC crystal growth utilizing dislocation conversion during solution method," *Appl. Phys. Express*, vol. 7, no. 6, 2014. doi:10.7567/APEX.7.065501
- [37] M. Benamara, M. Anani, B. Akkal, and Z. Benamara, "Ni/SiC-6H Schottky Barrier Diode interfacial states characterization related to temperature," *J. Alloys Compd.*, vol. 603, pp. 197–201, 2014. doi:10.1016/j.jallcom.2014.02.177
- [38] K. Y. Lee and Y. H. Huang, "An investigation on barrier inhomogeneities of 4H-SiC Schottky barrier diodes induced by surface morphology and traps," *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 694–699, 2012. doi:10.1109/TED.2011.2181391
- [39] T. Katsuno, Y. Watanabe, H. Fujiwara, M. Konishi, H. Naruoka, J. Morimoto, T. Morino, and T. Endo, "Analysis of surface morphology at leakage current sources of 4H-SiC Schottky barrier diodes," *Appl. Phys. Lett.*, vol. 98, no. 22, pp. 2–5, 2011. doi:10.1063/1.3597413
- [40] K. Y. Lee and M. A. Capano, "The correlation of surface defects and reverse breakdown of 4H-SiC Schottky barrier diodes," *J. Electron. Mater.*, vol. 36, no. 4, pp. 272–276, 2007. doi:10.1007/s11664-006-0075-3
- [41] D. J. Ewing, L. M. Porter, Q. Wahab, X. Ma, T. S. Sudharshan, S. Tumakha, M. Gao, and L. J. Brillson, "Inhomogeneities in Ni/4H-SiC Schottky barriers: Localized Fermi-level pinning by defect states," *J. Appl. Phys.*, vol. 101, no. 11, 2007. doi:10.1063/1.2745436
- [42] K. C. Mandal, S. K. Chaudhuri, K. V. Nguyen, and M. A. Mannan, "Correlation of deep levels with detector performance in 4H-SiC epitaxial schottky barrier alpha detectors," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 2338–2344, 2014. doi:10.1109/TNS.2014.2335736
- [43] P. Shenoy, A. Moki, B. J. Baliga, D. Alok, K. Wongchotigul, and M. Spencer, "Vertical Schottky barrier diodes on 3C-SiC grown on Si," in *Proceedings of 1994 IEEE International Electron Devices Meeting*, 1994. doi:10.1109/IEDM.1994.383380, pp. 411–414
- [44] A. Arvanitopoulos, N. Lophitis, K. N. Gyftakis, S. Perkins, and M. Antoniou, "Validated physical models and parameters of bulk 3C-SiC aiming for credible technology computer aided design (TCAD) simulation," *Semicond. Sci. Technol.*, vol. 32, no. 10, p. 104009, 2017. doi:10.1088/1361-6641/aa856b
- [45] M. Mandurrino, G. Verzellesi, M. Goano, M. E. Vallone, F. Bertazzi, G. Ghione, M. Meneghini, G. Meneghesso, and E. Zanoni, "Trap-assisted tunneling in InGaN/GaN LEDs: Experiments and physics-based simulation," *Proc. Int. Conf. Numer. Simul. Optoelectron. Devices, NUSOD*, pp. 13–14, 2014. doi:10.1109/NUSOD.2014.6935332
- [46] B. Asllani, M. Berthou, D. Tournier, P. Brosselard, and P. Godignon, "Modeling of Inhomogeneous 4H-SiC Schottky and JBS Diodes in a Wide Temperature Range," *Mater. Sci. Forum*, vol. 858, pp. 741–744, 2016
- [47] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer, 2008
- [48] M. Walters, "Radiation-Induced Neutral Electron Trap Generation in Electrically Biased Insulated Gate Field Effect Transistor Gate Insulators," *J. Electrochem. Soc.*, vol. 138, no. 9, p. 2756, 1991. doi:10.1149/1.2086050
- [49] F. Jazaeri, C. M. Zhang, A. Pezzotta, and C. Enz, "Charge-based modeling of radiation damage in symmetric double-gate MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 6, no. 1, pp. 85–94, 2018. doi:10.1109/JEDS.2017.2772346
- [50] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New York: Wiley, 2006
- [51] C. M. Su, M. Wuttig, A. Fekade, and M. Spencer, "Elastic and anelastic properties of chemical vapor deposited epitaxial 3C-SiC," *J. Appl. Phys.*, vol. 77, no. 11, pp. 5611–5615, 1995. doi:10.1063/1.359551
- [52] T. J. Drummond, "Work Functions of the Transition Metals and Metal Silicides," Albuquerque, 1999
- [53] N. Lophitis, A. Arvanitopoulos, S. Perkins, and M. Antoniou, "TCAD Device Modelling and Simulation of Wide Bandgap Power Semiconductors," in *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*, Y. K. Sharma, Ed. Rijeka: InTech, 2018
- [54] Synopsys, "Sentaurus TM Structure Editor User Guide.," 2017
- [55] Synopsys, "Sentaurus TM Device User Guide.," 2017
- [56] H. Itoh, A. Kawasuso, T. Ohshima, M. Yoshikawa, I. Nashiyama, S. Tanigawa, S. Misawa, H. Okumura, and S. Yoshida, "Intrinsic Defects in Cubic Silicon Carbide," *Phys. Status Solidi*, vol. 162, no. 1, pp. 173–198, 1997
- [57] A. Schenk, "A model for the field and temperature dependence of Shockley-Read-Hall lifetimes in silicon," *Solid State Electron.*, vol. 35, no. 11, pp. 1585–1596, 1992. doi:10.1016/0038-1101(92)90184-E
- [58] N. Tōyama, "Effective Richardson constant of sputtered PtSi Schottky contacts," *J. Appl. Phys.*, vol. 64, no. 1988, 1988. doi:10.1063/1.341634
- [59] V. Saxena, J. Nong Su, and A. J. Steckl, "High-Voltage Ni – and Pt – SiC Schottky Diodes Utilizing Metal Field Plate Termination," vol. 46, no. 3, pp. 456–464, 1999
- [60] L. Wenchang, Z. Kaiming, and X. Xide, "An electronic structure study of single native defects in beta-SiC," *J. Phys. Condens. Matter*, vol. 5, no. 7, pp. 891–898, Feb. 1993. doi:10.1088/0953-8984/5/7/016
- [61] I. Deretzis, M. Camarda, F. La Via, and A. La Magna, "Electron backscattering from stacking faults in SiC by means of ab initio quantum transport calculations," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 85, no. 23, 2012. doi:10.1103/PhysRevB.85.235310
- [62] X. Song, J. F. Michaud, F. Cayrel, M. Zielinski, M. Portail, T. Chassagne, E. Collard, and D. Alquier, "Evidence of electrical activity of extended defects in 3C-SiC grown on Si," *Appl. Phys. Lett.*, vol. 96,

- no. 14, pp. 1–4, 2010. doi:10.1063/1.3383233
- [63] G. Pristavu, G. Brezeanu, M. Badila, R. Pascu, M. Danila, and P. Godignon, “A model to non-uniform Ni Schottky contact on SiC annealed at elevated temperatures,” *Appl. Phys. Lett.*, vol. 106, 2015. doi:10.1063/1.4923468
- [64] A. F. Hamida, Z. Ouenoughi, A. Sellai, R. Weiss, and H. Ryssel, “Barrier inhomogeneities of tungsten Schottky diodes on 4H-SiC,” *Semicond. Sci. Technol.*, vol. 23, 2008. doi:10.1088/0268-1242/23/4/045005
- [65] S. Roy, C. Jacob, and S. Basu, “Current transport properties of Pd / 3C – SiC Schottky junctions with planar and vertical structures,” *Solid State Sci.*, vol. 6, pp. 377–382, 2004. doi:10.1016/j.solidstatesciences.2004.01.003
- [66] L. Boussouar, Z. Ouenoughi, N. Rouag, A. Sellai, R. Weiss, and H. Ryssel, “Investigation of barrier inhomogeneities in Mo / 4H – SiC Schottky diodes,” *Microelectron. Eng.*, vol. 88, no. 6, pp. 969–975, 2011. doi:10.1016/j.mee.2010.12.070
- [67] S. Kyoung, E. Jung, and M. Young, “Post-annealing processes to improve inhomogeneity of Schottky barrier height in Ti / Al 4H-SiC Schottky barrier diode,” *Microelectron. Eng.*, vol. 154, pp. 69–73, 2016. doi:10.1016/j.mee.2016.01.013
- [68] F. Giannazzo, F. Roccaforte, S. F. Liotta, and V. Raineri, “Two Dimensional Imaging of the Laterally Inhomogeneous Au / 4H-SiC Schottky Barrier by Conductive Atomic Force Microscopy,” *Mater. Sci. Forum*, vol. 557, pp. 545–548, 2007. doi:10.4028/www.scientific.net/MSF.556-557.545



**Arvanitopoulos E. Anastasios** was born in Patras, Greece, in May 1985. He received the Diploma in Electrical and Computer Engineering from the University of Patras, Greece in 2011. Since October of 2016 he has been a Ph.D. Candidate at the Research

Institute for Future Transport and Cities, Coventry University, UK. His research is focused on Wide Bandgap (WBG) power semiconductor devices for high performance electronics in Electric Vehicles (EVs). Of his particular interest is the physical modelling of WBG semiconductor materials and devices aiming to accurately simulate the effect of defects in the device operation.



**Marina Antoniou** received the B.A. and M. Eng. degrees in electrical and information engineering from the University of Cambridge (Trinity College), Cambridge, U.K., and the Ph.D. degree in electrical engineering from Cambridge. She was a Junior Research Fellow in Selwyn College, Cambridge, U.K. She is

currently an Associate Professor at the University of Warwick and is also affiliated with the U.K. Power Electronics Centre. Her research interests include power electronics and high voltage power semiconductor devices.



**Mike R. Jennings** received his BEng degree in Electronics with Communications from the University of Wales, Swansea, UK in 2003. The BEng incorporated a second year (exchange program) of study in the USA, where he studied at Union College, Schenectady, NY. His interest in semiconductor

device modelling, processing and characterisation led him to

undertake a PhD, in the field of silicon carbide (SiC) power electronics at the University of Warwick, UK. During his PhD he has won travel scholarships from the IEE (Hudswell Bequest Fellowship) and Welsh Livery Guild for electrical engineering research purposes. The scholarships obtained allowed him to visit Rensselaer Polytechnic Institute, NY, USA in 2005. He successfully defended his PhD, entitled "Novel Contact Formation for 4H-SiC Power Devices" in 2008. In 2009 Mike was awarded a Science City Research Alliance (SCRA) Fellowship, sponsored by the European Regional Development Fund (ERDF) and Advantage West Midlands (AWM). The focus of his research within this remit was the "Development of SiC Devices". His current research topics include high voltage bipolar devices (PiN diodes and Thyristors) in SiC, novel gate oxidation processes for Field Effect Transistors (FET) and 3C-SiC (cubic) growth above direct wafer bonded Si/SiC structures. Mike continues to work on the above topics as an active member of the Systems and Process Engineering Centre within the College of Engineering, Swansea University. He is a lecturer on numerous electrical engineering courses including IC design and power semiconductor devices.



**Samuel Perkins** was born in Norwich in the United Kingdom, on September 17<sup>th</sup>, 1993. He received his B.Eng. and MRes degrees from Coventry University, Coventry, in 2017. Currently he is pursuing his PhD degree at Coventry University. His research is focused on Wide Bandgap (WBG) power semiconductor devices for Ultra High

Voltage applications. Of his particular interest is the physical modelling of WBG semiconductor materials and characterisation of 4H-SiC n-IGBTs for Ultra High Voltage applications.



**Konstantinos N. Gyftakis (M'11)** was born in Patras, Greece, in May 1984. He received the Diploma in Electrical and Computer Engineering from the University of Patras, Patras, Greece in 2010. He pursued a Ph.D in the same institution in the area of electrical machines condition monitoring and fault diagnosis (2010-2014). Then he worked as a Post-Doctoral

Research Assistant in the Dept. of Engineering Science, University of Oxford, UK (2014-2015). Then he worked as Lecturer (2015-2018) and Senior Lecturer (2018-2019) in the School of Computing, Electronics and Mathematics and as an Associate with the Research Institute for Future Transport and Cities, Coventry University, UK. Additionally, since 2016 he has been a member of the “Centro de Investigação em Sistemas Electromecatrónicos” (CISE), Portugal. Since 2019 he has been a Lecturer in Electrical Machines, University of Edinburgh, UK. He has authored/co-authored more than 70 papers in international scientific journals and conferences and a chapter for the book: “Diagnosis and Fault Tolerance of Electrical Machines, Power Electronics and Drives”, IET, 2018.



**Philip Mawby** (S'85–M'86–SM'01) received the B.Sc. and Ph.D. degrees in electronic and electrical engineering from the University of Leeds, Leeds, U.K., in 1983 and 1987, respectively. His Ph.D. was focused on GaAs/AlGaAs heterojunction bipolar transistors for high-power radio frequency applications at the

GEC Hirst Research Centre, Wembley, U.K. In 2005, he joined the University of Warwick, Coventry, U.K., as the Chair of Power Electronics. He was also with the University of Wales, Swansea, U.K., for 19 years and held the Royal Academy of Engineering Chair for power electronics, where he established the Power Electronics Design Center. He has been internationally recognized in the area of power electronics and power device research. He was also involved in the development of device simulation algorithms, as well as optoelectronic and quantum-based device structures. He has authored or coauthored more than 100 journal and conference papers. His current research interests include materials for new power devices and modeling of power devices and circuits. Prof. Mawby has been involved in many international conference committees, including the ISPSD, EPE, and the ESSDERC. He is a Chartered Engineer, a Fellow of the IET, and a Fellow of the Institute Physics. He is a Distinguished Lecturer for the IEEE Electron Devices Society.



**Neophytos Lophitis** received the B.A. and M.Eng. degrees in 2009 and the Ph.D. degree in Power Devices in 2014, all from the University of Cambridge. Then he worked as a Research Associate in Power at the University of Cambridge (2014-15)

and as a consultant for Power Microelectronics companies

(2013-15). He joined Coventry University in 2015 where he is currently an Assistant Professor of Electrical Engineering at the School of Computing, Electronics & Mathematics and the research Institute for Future Transport and Cities. Since 2015 he has also been a member of the “High Voltage Microelectronics Laboratory” at the University of Cambridge, UK. Neophytos is also affiliated with the U.K. Power Electronics Centre and the European Centre for Power Electronics. His research includes optimization, design, degradation and reliability of high voltage microelectronic devices and electrical energy storage and conversion systems. He authored/co-authored more than 45 scientific manuscripts, including one book chapter for the book: “Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications”, IntechOpen, 2018.