On the robustness of ultra-high voltage 4H-SiC IGBTs with an optimized retrograde p-well

Tiwari, AK, Perkins, S, Lophitis, N, Antoniou, M, Trajkovic, T & Udrea, F

Original citation & hyperlink:
Tiwari, AK, Perkins, S, Lophitis, N, Antoniou, M, Trajkovic, T & Udrea, F 2019, On the robustness of ultra-high voltage 4H-SiC IGBTs with an optimized retrograde p-well. in 12th IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives (SDEMPED 2019). IEEE, IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives, Toulouse, France, 27/08/19
https://dx.doi.org/10.1109/DEMPED.2019.8864804

DOI 10.1109/DEMPED.2019.8864804

Publisher: IEEE

On the robustness of ultra-high voltage 4H-SiC IGBTs with an optimized retrograde p-well

Amit K. Tiwari, M. Antoniou, S. Perkin, N. Lophitis, T. Trajkovic and F. Udrea

***Abstract* — The robustness of ultra-high voltage (>10kV) SiC IGBTs comprising of an optimized retrograde p-well is investigated. Under extensive TCAD simulations, we show that in addition to offering a robust control on threshold voltage and eliminating punch-through, the retrograde is highly effective in terms of reducing the stress on the gate oxide of ultra-high voltage SiC IGBTs. We show that a 10 kV SiC IGBT comprising of the retrograde p-well exhibits a much-reduced peak electric field in the gate oxide when compared with the counterpart comprising of a conventional p-well. Using an optimized retrograde p-well with depth as shallow as 1 µm, the peak electric field in the gate oxide of a 10kV rated SiC IGBT can be reduced to below 2 MV.cm^{-1}, a prerequisite to achieve a high-degree of reliability in high-voltage power devices. We therefore propose that the retrograde p-well is highly promising for the development of >10kV SiC IGBTs.**

***Index Terms* — *SiC IGBT, Ultra-high voltage, Oxide breakdown, Retrograde p-well, Threshold voltage, Punch-through*.**

I. Introduction

In recent years, SiC has attracted considerable interest for the development of IGBTs to achieve the most optimum trade-off between the conduction and switching losses in ultra-high voltage (>10kV) class of applications, most notably, HVDC and Smart Grid [1-3]. The research has witnessed significant momentum and the first generation SiC IGBTs in the voltage range 10kV-30kV have been reported by a number of researchers [4-10]. Notable milestones in the area include the development of 10kV p-IGBT by Zhang *et al.* (2005), 10kV n-IGBT by Wang *et al.* (2005), 15 kV n- & p-IGBTs by Ryu *et al.* (2012), and 27 kV n-IGBT by Brunt *et al.* (2015) [7-10].

Although the presence of a stable native oxide (SiO_2) of SiC, which can be thermally grown to be used as a gate dielectric, has played a key role in advancing the ultra-high IGBT technology, it has also posed considerable reliability and stability challenges [11-13]. A robust high-voltage and low-to-medium frequency (a few Hz to 1 kHz) switching operation against a number of overload operational conditions, such as those encountered in ultra-high voltage modulated power converters and Marx generators, is highly desirable from SiC IGBTs [14, 15].

SiC exhibits a high critical electric field of 3-5 MV.cm^{-1}, which is ten times higher than that Si and is also much higher than that of SiO_2 [10]. However, its native oxide, SiO_2, has a lower dielectric constant of 3.9, nearly two and a half times lower than 10 of SiC. In accordance with Gauss law, the product of the relative dielectric constant and the normal electric field of SiO_2 and SiC material must be constant at their interface, *i.e.*, $\kappa_{SiC}.E_{SiC} = \kappa_{SiO2}.E_{SiO2}$, employing that at a given voltage, the effective electric field in SiO_2 is 2.5 times higher than that in SiC. To keep the electric field in the gate oxide below the safe operating limit of 2 MV.cm^{-1} to avoid its premature electrical breakdown, the electric field in SiC at the interface should not exceed 0.8 MV.cm^{-1}. This restricts the device designer to fully exploit the benefits of superior material properties of SiC.

High-κ dielectrics are proposed to improve the performance of SiC power devices at high-voltages [17-20]. However, due to significant lattice mismatch, high-quality

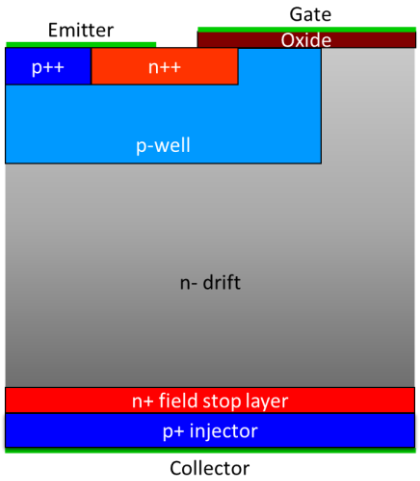


Fig. 1. An n-channel DMOS SiC IGBT test cell

A portion of this work was supported by the EPSRC's Centre for Power Electronics under Underpinning Power Electronics (UPE) 2: Switch Optimization Theme (Ref. EP/R00448X/1).

A. K. Tiwari (akt40@cam.ac.uk), T. Trajkovic (tt208@cam.ac.uk) and F. Udrea (fu10000@cam.ac.uk) are with Department of Engineering, University of Cambridge, Cambridge, CB2 1PZ, U.K.

M. Antoniou (marina.antoniou@warwick.ac.uk) is with Department of Engineering, University of Warwick, Coventry, CV4 7AL, Coventry, UK.

S. Perkin (perkin19@uni.coventry.ac.uk) and N. Lophitis (ac0473@coventry.ac.uk) is with Faculty of Engineering, Environment and Computing, Coventry University, CV1 2JH, Coventry, UK.

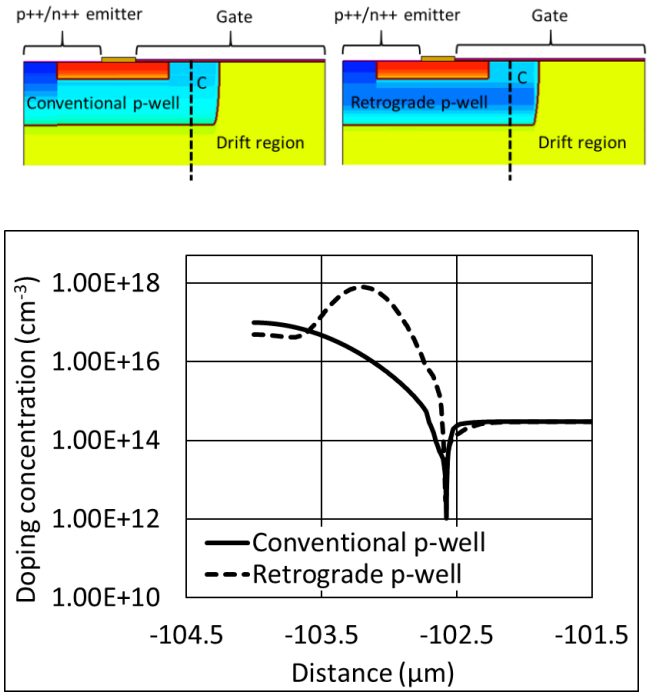


Fig. 2. Doping profiles for conventional and retrograde p-wells.

dielectric/SiC interfaces are particularly challenging to achieve in practice, often exhibiting a high density of defects (>10^{11} $eV^{-1}.cm^{-2}$) [19, 20], which ultimately lead to poor channel mobilities.

In the backdrop of limited compatibility with typical mass manufacturing and relatively smaller band offsets at the high-κ/SiC interface, the direct integration of high-κ dielectrics in SiC MOS technology has not been smooth. Multilayer stacks comprising of an ultra-thin (1-3nm) interfacial layer of SiO_2 and thick (30-50nm) high-κ dielectrics, which utilize a low thermal budget, are proposed to obtain high-quality

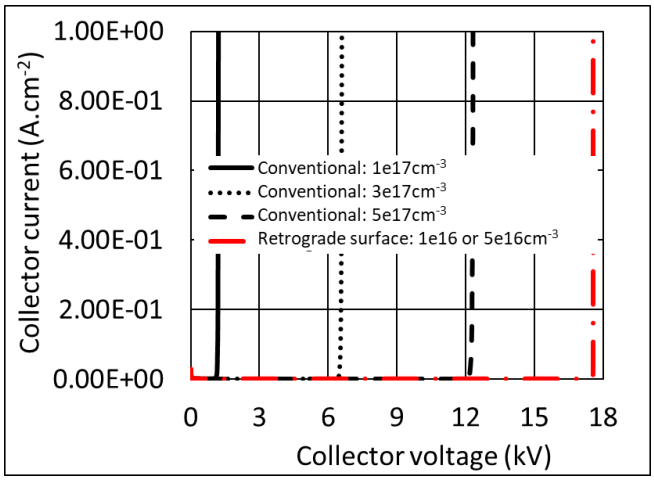


Fig. 3. Depiction of punch-through in an ultra-high voltage SiC IGBT with conventional and retrograde p-well.

interfaces, leading to improved channel mobilities >100 $cm^2.V^{-1}.s^{-1}$ [21, 22]. However, there is little available on the robustness of such stacks during high-voltage operation.

Whilst efforts are continued to increase the impact of high-κ dielectrics, significant improvements in terms of shielding the gate oxide from the high electric field can be achieved with the help of an enhanced IGBT design. In this paper, we report on improving the robustness of ultra-high voltage class of SiC IGBT using an innovative retrograde p-well.

We further compare the performance of SiC IGBTs comprising of an optimized retrograde p-well with that of a counterpart utilizing a conventional p-well. We show that in addition to offering a robust control on the gate threshold voltage (V_T) and eliminating punch-through, the retrograde p-well is key to achieve a much-reduced peak electric field in the gate oxide.

II. Device Structure and Methodology

As shown in Fig. 1, an n-channel DMOS IGBT structure is used to examine the robustness of a 10-12 kV SiC IGBT. The SiC IGBT test cell, a punch through design, consists of a p^+ injector, n^+ field-stop/buffer epilayer and n^- drift epilayer.

To have a high-degree of carrier injection, p^{++} injector consists of a doping density of 1×10^{19} cm^{-3}. A doping concentration of 1×10^{18} cm^{-3} is utilized for the n^+ buffer, which is adequate to stop the electric field reaching the injector. The doping concentration and thickness of drift epilayer are 3×10^{14} cm^{-3} and 120 µm, respectively, resulting in a theoretical breakdown voltage in excess of 15kV.

The retrograde p-well differs with a conventional p-well mainly in the manner the doping concentration is varied with the depth. In a conventional approach, the peak doping concentration of 1×10^{17} cm^{-3} lies mostly at the surface or in the sub-surface region of p-well, which then decreases with the depth.

In contrast, in the retrograde approach, the doping near the surface of the p-well, also referred as the sub-surface region, is kept low (~10^{16} cm^{-3}), which gradually increases up to 1×10^{18}-5×10^{18} cm^{-3} and then decreases with the depth. The variation in the doping concentration with the depth for a conventional and retrograde p-well is illustrated in Fig. 2.

The low-doping region near the surface of retrograde p-well is typically 0.2-0.3 µm deep, whilst the remaining depth of ~0.4-0.6 µm is dedicated to a high-doping concentration, typically higher than $1\times10^{18}cm^{-3}$. Extensive details regarding the design-optimization of retrograde p-well are described in our previous work [23].

An electron lifetime of 2.5 µs is utilized in simulations. The hole lifetime is considered to be the $1/5^{th}$ of that of electron lifetime. Furthermore, breakdown characteristics are obtained using a background carrier concentration of 1×10^{9} cm^{-3}.

The Okuto-Crowell model is used to calculate impact ionization as a function of electric field in 4H-SiC. Doping

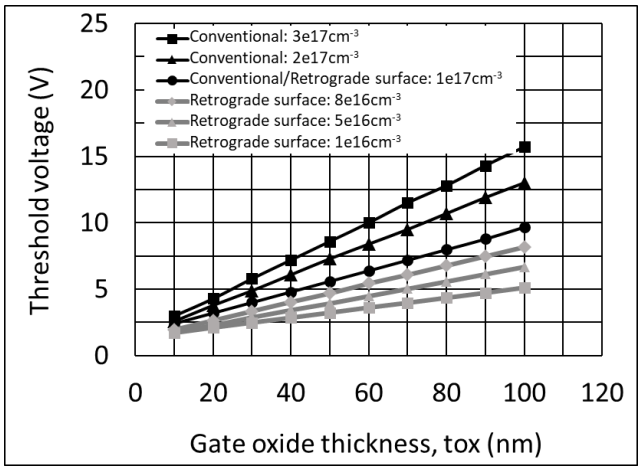


Fig. 4. IGBT threshold voltage as a function of the gate oxide thickness upon p-well utilizing conventional and retrograde doping profiles.

and temperature dependency of carrier mobility is modelled using the Caughey-Thomas model. The lifetimes of carriers are modeled as a product of a doping-dependent, field-dependent and temperature-dependent factors, as embedded in Scharfetter model utilizing Shockley-Read-Hall (SRH) recombination mechanism.

The dependency of energy bandgap upon both temperature and doping is considered. Simulations also include the incomplete ionization of dopants in 4H-SiC. The donor trap of Nitrogen is considered to be located at 0.0709 eV with respect to the conduction band and the acceptor trap of Aluminum is considered to be located at 0.265 eV with respect to the valance band. Extensive details regarding physics models and parameters used in simulations of 4H-SiC IGBTs can be found in our previous work [24-25].

III. Elimination of Punch-Through

As shown in Fig. 3, a 10-12kV SiC IGBT comprising of a conventional p-well of depth ~1.0 µm and doping concentrations of 1×10^{17} and 3×10^{17} cm^{-3} exhibits a premature rise in the collector current at ~1 kV and ~6 kV, respectively. We found that a shallow conventional p-well (<1 µm) with low doping concentrations (<3×10^{17} cm^{-3}) depletes completely much before reaching 10 kV and thus let the collector current conduct through it. A completely depleted p-well means no gate control on the IGBT current.

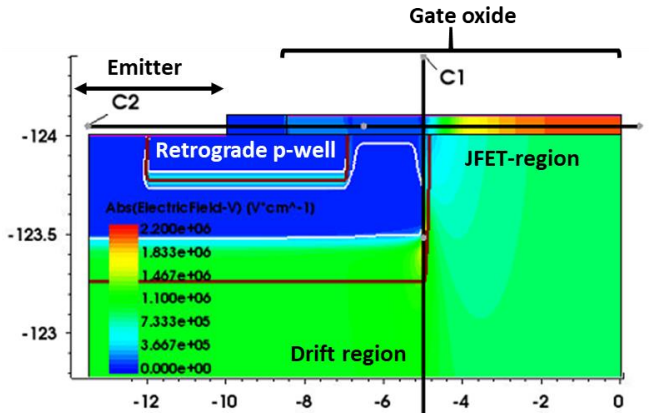
For low p-well doping concentrations, for example, 1×10^{17} cm^{-3}, a deep (>2 µm) conventional p-well can be envisaged to help with the elimination of punch-through in ultra-high voltage IGBTs. However, deep ion-implantation in SiC are particularly challenging, requiring energies in excess of 3 MeV to reach a depth of 2.0 µm. Such high energies not only increase the cost but also cause significant damage to the surface. Ion-implants in SiC are generally limited to a maximum depth of 1.5 µm, which is not enough to avoid punch-through if a lowly doped conventional p-well is used.

The punch-through is less of an issue for SiC IGBT with retrograde p-well since the doping concentration at its bottom is very high, typically, ~$10^{18}$$cm^{-3}$, ensuring only partial depletion at high-voltages. The retrograde p-well effectively eliminates the punch through and a sharp breakdown occurs at a theoretically value of 16-17 kV.

The breakdown characteristics remains unaffected by the change in the sub-surface doping concentration of the retrograde p-well. Furthermore, it is important to note that without affecting the IGBT breakdown characteristics, the retrograde p-well can be made as shallow as 0.6-0.8 µm, a depth that is achievable with only 700-800 keV implants.

IV. Control on Gate Threshold Voltage

In an effort to eliminate punch through and to reduce the requirement of deep implants, a high doping concentration in the conventional p-well is not recommend since it significantly increases V_T. Importantly, if a higher doping



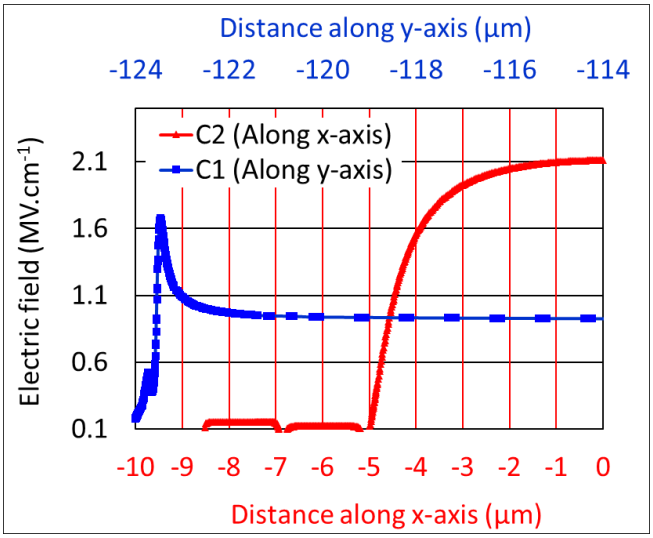


Fig. 5. Electric field variation along different cutlines, C1 and C2, in a SiC IGBT at 10kV. The maximum field region is lying at the top of the middle of JFET region.

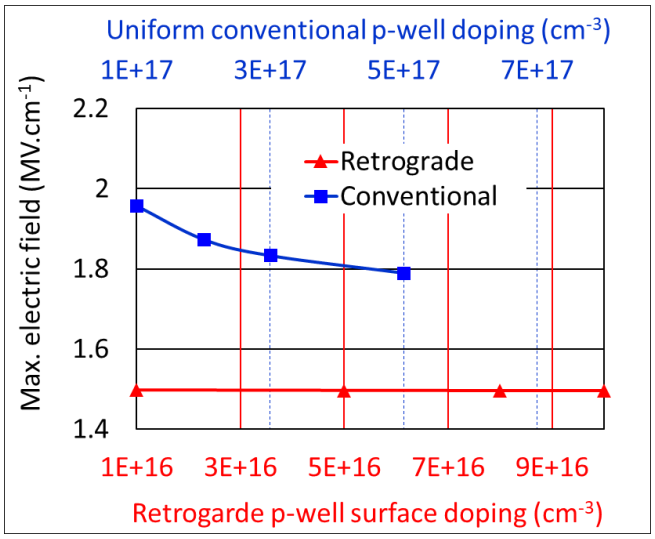


Fig. 6. The maximum electric field in the gate oxide as a function of doping concentration in underlying uniformly doped conventional p-well and at the sub-surface region of retrograde p-well. Electric field values correspond to the collector voltage of 10 kV under no gate bias. Both conventional and retrograde p-wells have the same depth of ~2.8 µm deep, while the oxide thickness is fixed at 50 nm.

concentration is utilized, an increase in V_T should not be compensated at the cost of sacrificing the gate oxide thickness, as it leads to significantly reliability issues during operation at high voltages.

The retrograde p-well offers a robust solution to IGBT gate threshold voltage control by effectively decoupling the blocking ability from the doping of the sub-surface region. As shown in Fig. 4, a 10-12 kV SiC IGBT comprising of retrograde p-well yields V_T between 5-7 V for the gate oxide as thick as 100 nm. If required, the gate oxide thicker than 100 nm can be utilized by further reducing the doping at the surface of the retrograde p-well. For example, for the surface doping of 1×10^{16} cm^{-3}, V_T of SiC IGBT with 100nm gate oxide is calculated to be only 5 V and a 150nm thick SiO_2 can be utilized without increasing V_T beyond 7 V.

To have V_T in similar range, i.e., 5-7 V, using a conventional p-well with doping concentration of 1×10^{17} cm^{-3}, one would have to consider significantly thinner gate oxide, i.e., 40-50 nm, which is likely to suffer from poor quality issues and hence could pose significant reliability challenges. It is worth mentioning here that the heavily doped bottom of retrograde p-well has no role to play in V_T control.

Furthermore, although as such there is no restriction on the magnitude of sub-surface doping of the retrograde p-well, V_T shift may not be significant even if a very low doping concentration is utilized. For example, for one order change in the magnitude of sub-surface doping concentration, i.e., 1×10^{16} to 1×10^{15} cm^{-3}, V_T shifts by only 0.5 V.

Nevertheless, in a scenario, where, there are stringent operational requirements and several processing constraints in terms of the V_T window, ion-implantation depth and oxide thickness, the retrograde p-well is highly relevant to the ultra-high voltage SiC IGBT technology, outperforming a conventional p-well. The retrograde p-well can further assist with the SiC MOS technology by tackling with low channel mobility issue. As previously reported by Kimoto *et al.* and Ortiz *et al.*, a low doping concentration, preferably ~1×10^{16} cm^{-3}, at SiC/SiO2 is desirable in order to enhance channel mobility from ~10 cm^2.V^{-1}.s^{-1} to >120 cm^2.V^{-1}.s^{-1}. In

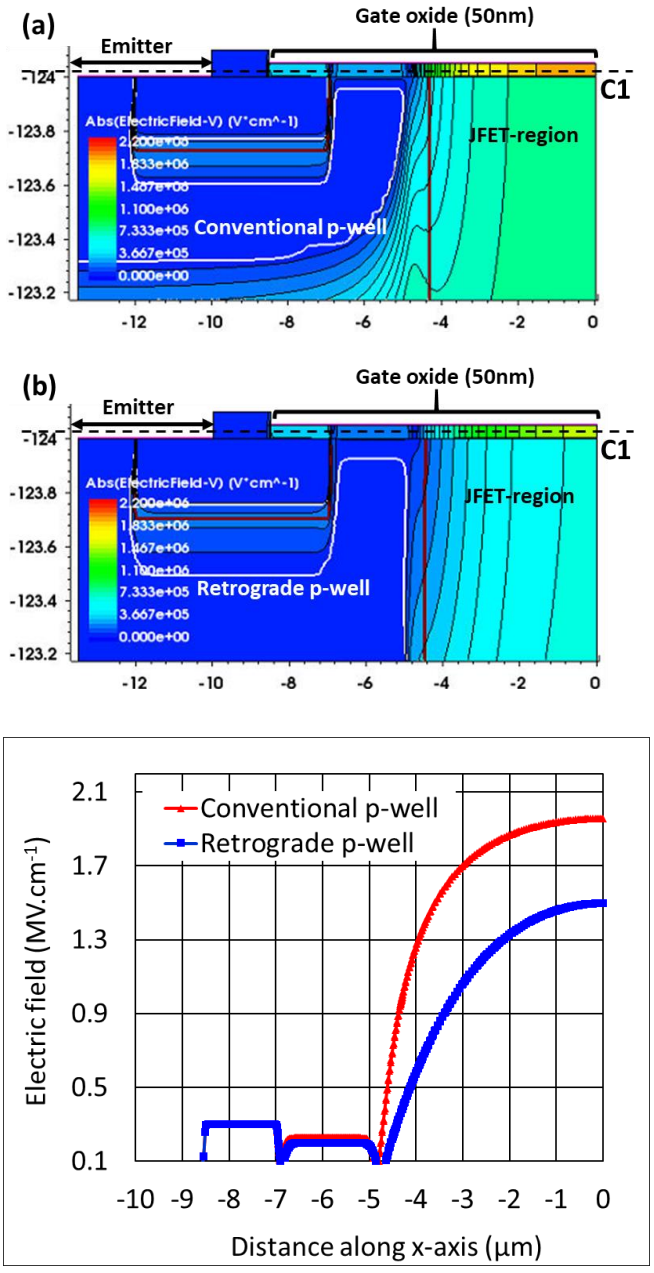


Fig. 7. Electric field profiles at 10kV in a SiC IGBTs with fixed 50 nm thick gate oxide on (a) a conventional p-well and (b) a retrograde p-well. The maximum electric field in the gate oxide (along cut line C1) typically lies in the middle of JFET region, i.e., at '0' of the test cell used in simulations. The retrograde p-well surface has a doping density of 5×10^{16} cm^{-3} and conventional p-well is uniformly doped with 1×10^{17} cm^{-3}. Both p-wells are ~2.5 µm deep.

high-voltage power devices, punch-through is likely to be an issue for conventional p-well consisting of low-doping concentration. However, by adapting the retrograde p-well approach, a substantial reduction (~1×10^{16} cm^{-3}) in the doping at the MOS interface is achievable.

V. Impact upon Peak Electric Field in Gate Oxide

We further examine the peak electric fields within high-voltage SiC IGBT structures. As shown in Fig. 5, a SiC IGBT exhibits high magnitude electric field predominantly in two regions, being in the gate oxide on top of the JFET region and at the bottom of p-well. In the present context, the latter is of least concern since the IGBT test-cell used in simulations consists of specifications, i.e., drift region thickness 120 µm and doping concentration 1×10^{14} cm^{-3}, which yield a breakdown voltage of >15 kV. This means the peak electric field in this region at the rated voltage of 10 kV will be much lower than the critical field limit of 3MV.cm^{-1}.

We have therefore put our emphasis mainly upon the peak electric field in gate region consisting of SiO_2. Since the retrograde and conventional approaches utilize different p-well depths to achieve a 10 kV IGBT, a direct comparison between the electric field profiles of both approaches is not feasible. For example, to have a 10 kV SiC IGBT, an implant depth of only 0.6-0.8 µm is required when the retrograde p-well is utilized, whereas if a conventional approach is adopted, the p-well will have to be substantially deep, i.e. >2 µm. The comparison is further complicated by difference in the magnitude of doping concentrations of conventional and retrograde approaches.

For the sack of comparison, we compare the peak oxide electric field when both the retrograde and conventional p-wells have the same depths. For our analysis, we choose the conventional p-well to be deep enough (~2.5 µm) to reach

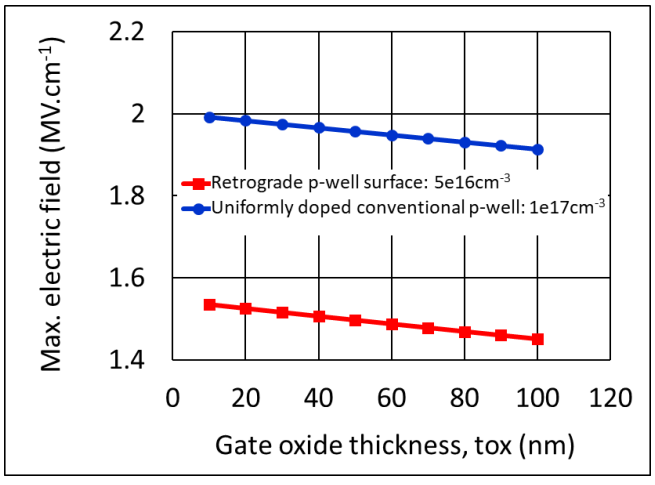


Fig. 8. The maximum electric field in the gate oxide as a function of its thickness. Electric field values correspond to the collector voltage of 10 kV under no gate bias. Details regarding conventional and retrograde p-wells are akin to those mentioned in Fig. 6.

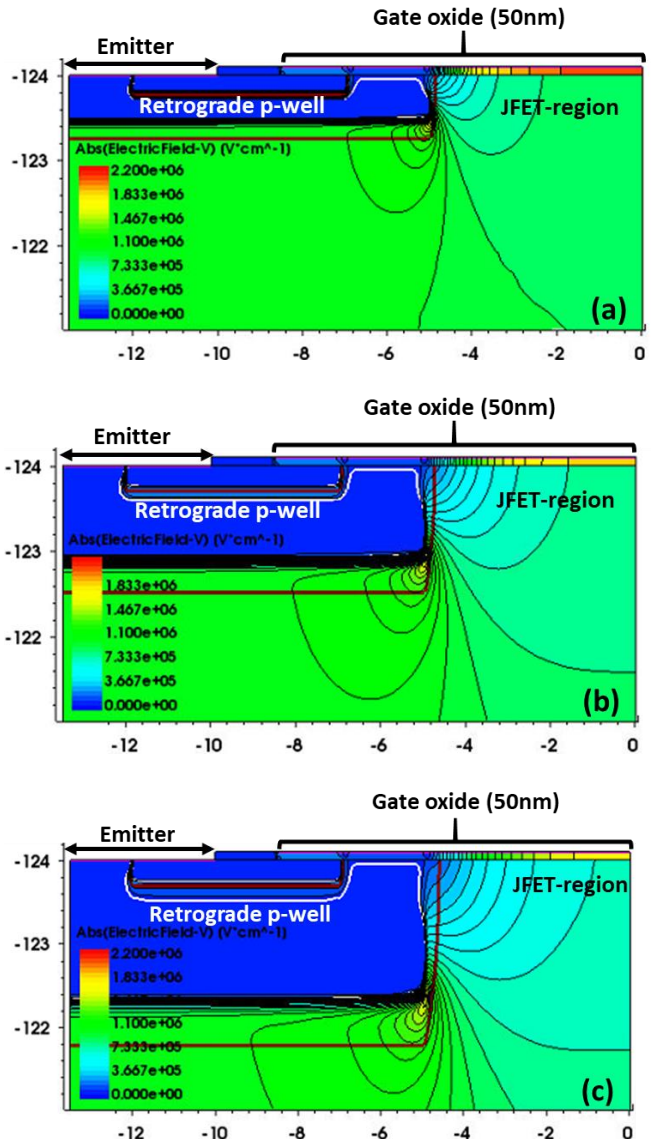


Fig. 9. Electric field profiles at 10kV in a SiC IGBTs when the retrograde p-well depth is (a) 0.7-0.8 µm, (b) 1.4-1.5 µm and (c) 2.0-2.2 µm. The oxide thickness is fixed at 100 nm and the retrograde p-well surface has a doping concentration of 5×10^{16} cm^{-3}, which are yielding a V_T of 7V.

10 kV and then utilize the same depth to simulate the retrograde p-well.

One can choose the retrograde p-well depth of 0.6-0.8 µm as the reference depth. However, a conventional p-well with this depth is not adequate to yield a 10 kV blocking capability, leading to significant punch through at low voltages. As a result, the comparison will be feasible at only low voltages, <1 kV.

We have examined the effect of doping concentration of both approaches and the gate oxide thickness upon the peak electric field. As shown in Fig. 6, we note that the magnitude of peak/maximum electric field in the gate oxide remains unperturbed with the change in doping concentration at the

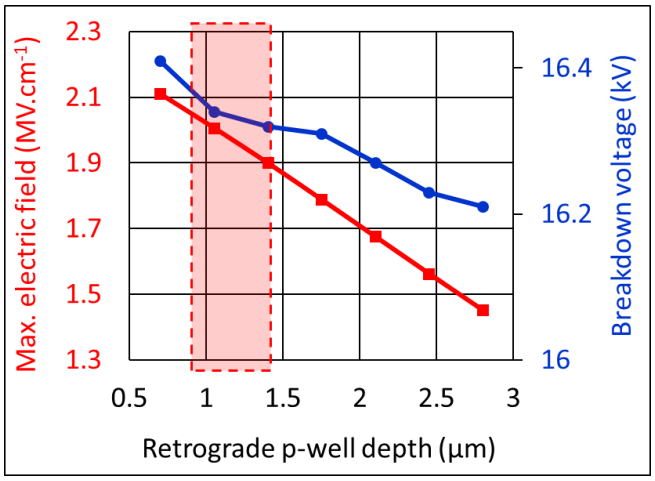


Fig. 10. Variation in the maximum electric field in the gate oxide and breakdown voltage as a function retrograde p-well depth. Electric field values correspond to the collector voltage of 10 kV under no gate bias. The gate oxide is 100nm thick and the sub-surface doping is 5×10^{16} cm^{-3}. The dotted rectangle is an indicator of the implant energy range of 800 keV-2MeV that is required to achieve the depth in the range 0.9-1.4 µm.

surface of retrograde p-well. In contrast, for a conventional p-well, the peak electric field in the gate oxide decreases with increase in the doping concentration of underlying conventional p-well. Of particular importance is a much-reduced magnitude of peak electric field in the gate oxide when deposited upon the retrograde p-well.

A comparison between the electric field profiles of SiC IGBT with conventional and retrograde p-wells is further illustrated in Fig. 7. A deep retrograde p-well, which consists of a heavily doped bottom (~10^{18} cm^{-3}) depletes partially at 10 kV and results in a much-reduced electric field in the JFET region when compared with that of a conventional p-well, which has a relatively lower doping density of 1×10^{17} cm^{-3} and thus exhibiting a greater degree of depletion. As explained using Gauss law, a lower electric field in the JFET region reflects in pro-rata reduction in electric field in the gate oxide lying on top of the JFET region.

As shown in Fig. 8, a further reduction in the peak electric field can be achieved with relative ease by increasing the thickness of gate oxide. For 100nm thick oxide on the retrograde p-well, the peak electric field is lying below 1.5 $MV.cm^{-1}$, which is particularly beneficial to enhance the long-term robustness of power devices.

In the case of conventional p-well, the peak electric field has also reduced with the oxide thickness. However, it remains ~25% higher in comparison to that of the retrograde p-well. Furthermore, a 100 nm thick gate oxide on a conventional p-well with doping density of $1\times10^{17}cm^{-3}$ means a V_T of ~10V. The doping of the underlying surface of retrograde p-well has little effect upon the peak electric field, and thus it can be lowered further using a lower surface doping, which will allow even thicker oxide deposition for the similar V_T.

A deep p-well, either retrograde or conventional, can help with minimizing the electric field in the JFET region and thus in the gate oxide retrospectively. For example, as depicted Fig. 9, the peak electric field in JFET region reduced significantly with the retrograde p-well depth. However, a deep p-well is not easy to realize in practice.

Having asserted that the retrograde p-well is superior to conventional p-well, we have further optimized the retrograde p-well to obtain an optimum depth, typically shallower than 1.5 µm, so that it can be realized using low energy implants whilst ensuring the peak electric field in the gate oxide remains below 2$MV.cm^{-1}$ and V_T within 7 V. Fig. 10 shows the reduction in the peak electric field in the gate oxide as a function of the retrograde p-well depth.

We note that for the sub-surface doping of 5×10^{16} cm^{-3} and an oxide thickness of 100nm, which yield a V_T of ~7V, the retrograde p-well with depth of 1.2 µm is adequate to retain the peak electric field below 2$MV.cm^{-1}$ in the gate oxide. Upon utilizing an even reduced sub-surface doping concentration of 1×10^{16} cm^{-3} and an oxide thickness of 150nm, which also yield a V_T of 7V, one can utilize a shallower retrograde p-well of 0.9 µm, being both depths well within 2 MV implantation energies.

It is worth mentioning that the edges of retrograde p-well are lowly doped (of the order of $10^{17}cm^{-3}$) and the high doping region is kept away from the corner, which generally experiences the most significant electric field crowding in a vertical power device. Additionally, the curvature of corner is reduced to minimize electric field crowding and hence impact ionization by forming a softer junction at the bottom. Such design features avoid degradation of the IGBT blocking voltage when the peak doping concentration and the depth of the retrograde p-well increases. It is evident that there is not much degradation in the breakdown voltage when the depth of retrograde p-well is increased.

VI. Conclusion

In conclusion, we showed that the retrograde p-well is offering a robust solution to V_T control, whilst eliminating punch-through. We further showed that using the retrograde p-well, a peak electric field <2 $MV.cm^{-1}$ is feasible in the gate oxide of a 10kV SiC without exceeding its V_T beyond 7 V and utilizing costly deep implantations.

We find that the sub-surface doping concentration of 1×10^{16} -5×10^{16} cm^{-3} for the retrograde p-well and oxide thickness of 100-150 nm are the most optimum combination for 10 kV rated SiC IGBTs, requiring a shallow implant of depth of <1.2 µm and retaining V_T and the gate oxide peak electric field below 7 V and 2 $MV.cm^{-1}$, respectively. We therefore propose the optimized retrograde p-well is highly desirable to enhance the robustness of ultra-high voltage class of SiC IGBTs, further minimizing processing challenges and development cost substantially.

REFERENCES

[1] J. Wang, A. Q. Huang, W. Sung, Y. LIU, and B. J. Baliga, "Smart grid technologies", IEEE Industrial Electronics Magazine, vol. 3, no. 2, pp. 16-23, June 2009.

[2] J. W. Palmour, J. Q. Zhang, M. K. Das, R. Callanan, A. K. Agarwal, D. E. Grider, "SiC power devices for smart grid systems", In proceedings of IEEE International Power Electronics Conference, pp. 1006-1013, August 2010.

[3] L. Cheng, J. W. Palmour, A. K. Agarwal, S. T. Allen, E. V. Brunt, G. Y. Wang, V. Pala, W. J. Sung, A. Q. Huang, M. J. O'Loughlin, A. A. Burk, D. E. Grider, and C. Scozzie, "Strategic overview of high-voltage SiC power device development aiming at global energy savings" Mater. Sci. Forum, vols. 778-780, pp. 1089-1095, February 2014.

[4] K. Fukuda, D. Okamoto, M. Okamoto, T. Deguchi, T. Mizushima, K. Takenaka, H. Fujisawa, S. Harada, Y. Tanaka, Y. Yonezawa, T. Kato, S. Katakami, M. Arai, M. Takei, S. Matsunaga, K. Takao, T. Shinohe, T. Izumi, T. Hayashi, S. Ogata, K. Asano, H. Okumura, and T. Kimoto, "Development of ultrahigh-voltage SiC devices", IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 396-404, 2015.

[5] N. Iwamuro and T. Laska, "IGBT history, state-of-the-art, and future prospects" IEEE Trans. on Electron Devices, vol. 64, no. 3, pp. 741-752, March 2017.

[6] M. Rahimo, P. Streit, A. Kopta, U. Schlapbach, S. Eicher, and S. Linder, "The status of IGBTs and IGCTs rated over 8kV", In proceedings of PCIM Europe, pp. 1-6, 2003.

[7] Q. Zhang, H-R. Chang, M. Gomez, C. Bui, E. Hanna, J. A. Higgins, T. Isaacs-Smith, and J. R. Williams, "10kV trench gate IGBTs on 4H-SiC", in Proceedings of 17th IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 303–306, May 2005.

[8] X. Wang, and James A. Cooper, High-voltage n-channel IGBTs on free-standing 4H-SiC epilayers, IEEE Trans. on Electron Devices, vol. 57, no. 2, pp. 511-515, Feb. 2005.

[9] S. H. Ryu, L. Cheng, S. Dhar, C. Capell, C. Jonas, J. Clayton, M. Donofrio, M. J. O'Loughlin, A. A. Burk, A. K. Agarwal, J. W. Palmour, "Development of 15 kV 4H-SiC IGBTs", Mater. Sci. Forum, vol. 717–720, pp. 1135-1138, May 2012.

[10] E. V. Brunt, L. Cheng, M. J. O'Loughlin, J. Richmond, V. Pala, J. W. Palmour, C. W. Tipton, C. Scozzie, "27 kV, 20 A 4H-SiC n-IGBTs", Mater. Sci. Forum, vol. 821–823, pp. 847-850, June 2015.

[11] T. Kimoto, J. A. Cooper, "Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications", John Wiley & Sons, Nov. 2014.

[12] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation", IEEE Trans. on Power Electronics, vol. 30, no. 5, pp.2445-2455, May 2015.

[13] A. Fayyaz, and A. Castellazzi, "High temperature pulsed-gate robustness testing of SiC power MOSFETs" Microelectronics Reliability, vol. 55, no. 9-10, pp. 1724-1728, August 2015.

[14] A. Kadavelugu, S. Bhattacharya, S. H. Ryu, E. V. Brunt, D. Grider, A. Agarwal, S. Leslie, "Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters", IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2528-2535, October 2013.

[15] M. Hinojosa, H. O'Brien, E. V. Brunt, A. Ogunniyi, and C. Scozzie, "Solid-state Marx generator with 24 KV 4H-SIC IGBTs." In proceedings of IEEE Pulsed Power Conference (PPC), pp. 1-5, October 2015.

[16] B. J. Baliga, "Silicon carbide power devices" World scientific, 2006.

[17] M. Nawaz, "On the evaluation of gate dielectrics for 4H-SiC based power MOSFETs", Active and Passive Electronic Components, 2015.

[18] S. K. Gupta, J. Singh, and J. Akhtar, "Materials and processing for gate dielectrics on silicon carbide (SiC) surface" In Physics and Technology of Silicon Carbide Devices, Intech- Open Access Publisher, October 2012.

[19] V. V. Afanas'ev, A. Stesmans, F. Chen, S. A. Campbell, and R. Smith, "HfO2-based insulating stacks on 4H–SiC (0001)", Appl. Phys. Letts., vol. 82, no. 6, pp. 922-924, February 2003.

[20] R. Mahapatra, N. Poolamai, S. Chattopadhyay, N. G. Wright, Amit K. Chakraborty, K. S. Coleman, P. G. Coleman, and C. P. Burrows, "Characterization of thermally oxidized Ti⁄ SiO2 gate dielectric stacks on 4H–SiC substrate", Appl. Phys. Lett., vol. 88, no. 7, pp. 072910 1-3, February 2006.

[21] F. Arith, J. Urresti, K. Vasilevskiy, S. Olsen, N. Wright, and A. O'Neill, "Increased Mobility in Enhancement Mode 4H-SiC MOSFET Using a Thin SiO2/Al2O3 Gate Stack", IEEE Electron Device Letts., vol. 39, no. 4, pp. 564-567, April 2018.

[22] J. Urresti, F. Arith, K. Vassilevski, A. K. Tiwari, S. Olsen, N. G. Wright, and A. G. O'Neill, "High-Mobility SiC MOSFETs Using a Thin-SiO2/Al2O3 Gate Stack, " Mater. Sci Forum, vol. 924, pp. 494-497, July 2018.

[23] Amit K. Tiwari, M. Antoniou, T. Trajkovic, S. Perkins, N. Lophitis, F. Udrea, "Performance improvement of >10kV SiC IGBTs with retrograde p-well", Mater. Sci Forum (2018) (in press).

[24] S. Perkins, M. Antoniou, Amit K. Tiwari, A. Arvanitopoulos, T. Trajkovic, F. Udrea, N. Lophitis, ">10kV 4H-SiC n-IGBTs for Elevated Temperature Environments", In proceedings of International Seminar on Power Semiconductors (ISPS), August 2018.

[25] N. Lophitis, A. Arvanitopoulos, S. Perkins, M. Antoniou, "TCAD device modelling and simulation of wide bandgap power semiconductors", InTech– Open Access Publisher, pp. 17-44, February 2018.