Drift-diffusion and hydrodynamic modeling of current collapse in GaN HEMTs for RF power application

Faramehr, S., Kalna, K. & Igic, P.

Drift-Diffusion and Hydro-Dynamic Modelling of Current Collapse in GaN HEMTs for RF Power Application

Soroush Faramehr, Karol Kalna and Petar Igić

Electronic System Design Centre (ESDC), College of Engineering, Swansea Universtiy, Singleton Park, Swansea, SA2 8PP, Wales, United Kingdom.

E-mail: 476599@swansea.ac.uk, K.Kalna@swansea.ac.uk and P.Igic@swansea.ac.uk

Abstract. Current collapse due to the trapping/de-trapping of the carriers at the surface and in the bulk of a 0.25 μm gate length AlGaN/GaN high electron mobility transistor (HEMT) is investigated using 2D Technology Computer Aided Design (TCAD) transient simulations. Gate and drain pulse techniques are used to study the dynamic picture of trapping and de-trapping of carriers within drift-diffusion and hydrodynamic transport models. In addition, coupled electrical and thermal simulations are performed to model the energy exchange of the carriers with the lattice and to predict electron temperature in the channel. It is found that current degradation upon electrical stress is due to two different types of traps, donor-like traps and acceptor-like traps, respectively. The collapse next to 5% and 75% was observed for bulk and surface traps, respectively. The combined effect of surface and bulk traps on current transient characteristics has been investigated and simulations are in a very good qualitative agreement with the experimental observations.

1. Introduction

Gallium Nitride (GaN) based High Electron Mobility Transistors (HEMTs) are attracting attention for power electronics, microwave amplifiers, radio frequency and switching applications due to unique properties of III-V materials [1], [2], [3]. GaN properties such as spontaneous and piezoelectric polarizations resulting in two-dimensional electron gas (2DEG) with densities above 10^{13} cm^{-2}, relatively high mobility (up to 2000 cm^{2}V^{-1}s^{-1}), a large energy band gap (3.4 eV), a good thermal conductivity (160 WK^{-1}m^{-1}) ensuring good heat dissipation, and a very high breakdown field (3500 kV/cm) make it an ideal candidate for all devices requiring fast carrier transport with high breakdown. Recently, a record for the current gain cutoff frequency (f_T) of 370 GHz has been achieved in a 30 nm gate-length GaN HEMT with extrinsic transconductance ($g_{m.ext}$) of 650 mS/mm, maximum drain current density (I_D) of 1.5 A/mm, on/off current ratio of 10^6, and on-resistance of 0.78 Ω.mm [4]. Singisetti *et al* (2012). [5] have demonstrated on-resistance record of 0.66 Ω.mm in a 115 nm gate length GaN HEMT with current gain cutoff frequency (f_T) of 122 GHz, peak transconductance (g_m) of 510 mS/mm, on/off current ratio of 2.2×10^5, and maximum I_D of 1.15 A/mm. Despite the fact that GaN HEMTs have achieved an excellent performance, the main challenge remains to sustain reliability and stability of the device performance [6], [7]. The excellent performance of HEMTs is not always reproducible due to the existence of defects and/or trap centers in a device structure. Traps in GaN HEMTs can cause transient instabilities [8], persistent photoconductivity [9], and current collapse [10], [11] resulting in degradation of the device performance. To achieve reliability and stability of GaN HEMTs, understanding of the failure mechanisms is vital. Among failure mechanisms, a current collapse is the most critical issue. The current collapse is defined as a temporary reduction of the drain current after application of a high voltage [12]. It has been widely observed that recovery time of this phenomenon has a very slow nature in the range of seconds or even a few days [13], [14]. Under DC bias measurements, the current collapse manifests itself as a reduction in drain current [15], while in RF applications this phenomenon limits RF performance [16]. There are two widely accepted explanations for current collapse: surface-trapping and bulk-trapping limiting the output power density and switching characteristics.

Surface-trapping, which can be viewed as a virtual gate, depletes the 2DEG under the drain side of the gate caused by an increase of the parasitic negative sheet charge at the surface leading to extension of the gate depletion region and subsequent current collapse [13]. Bulk-trapping modifies the charge distribution at the device layers resulting in the change of electron density in 2DEG [17].

Recently, numerous experimental techniques have been used to identify and localize the traps such as deep-level transient spectroscopy (DLTS) [18], and gate-lag and drain-lag measurements [19], [20]. However, as existing techniques are insufficient and discriminate in long-term experiments, there is no direct information and no widely-accepted explanation for nature of the traps. Consequently, numerical simulations are necessary to be carried out in order to provide a detailed understanding of behavior and nature of the traps [21].

To investigate the role of surface and bulk traps, two-dimensional (2D) simulations of an $Al_{0.28}Ga_{0.72}N$/GaN HEMT were performed using Atlas simulation toolbox by Silvaco [22]. Since hot electrons play a key role in bulk trapping [23], hydrodynamic (HD) transport model is employed to study the effect of hot electrons on the device performance. Previous studies focused on effect of traps using DC simulations [23], and transient simulations of drain-lag and current collapse [24]. Recently, Zhang *et al* (2013). [25] investigated only the influence of the interface acceptor-like traps on the transient response of GaN HEMTs. However, some of the important factors such as hot electrons, self-heating related to thermal effects, long-term transient analysis or the effect of trapping of hot electrons on the drain current in regions not in vicinity of the gate have been neglected in the latter and in the previous works.

This work has two main aims: firstly, to provide a comprehensive review of the major reliability issues in GaN HEMT device technology related to power applications and, secondly, to report novel advances for the reliability issues. These advances include: an investigation of the virtual gate profile at device surface (at the source and drain sides of the gate) leading to a conclusion that the gate-lag measurements of GaN HEMTs exhibit the impact of both bulk and surface traps (this is contradictory to the previous works [24], [25]); in-depth analysis of the gate-lag measurements; and, finally, insight into a dynamical behavior of regions under the gate during electrical stress at low and high drain biases. To achieve all these, we have used the HD and drift-diffusion (DD) transport models coupled with thermal modeling [26]. The both transport models are meticulously calibrated against experimental I_D-V_{DS} characteristics of the 0.25 μm gate length AlGaN/GaN HEMT. Based on this accurate calibration, a long-term transient analysis technique with an acceptable simulation run-time is developed to investigate the above listed phenomena causing the current collapse.

2. Basic device structure and simulation model

A cross-section of the simulated 0.25 μm gate length AlGaN/GaN HEMT is illustrated in figure 1. The barrier, the buffer and the substrate thicknesses are 21 nm, 1.9 μm and 300 μm, and the source-to-gate and the gate-to-drain separations are 1.25 μm and 2.50 μm, respectively. The device has a very similar asymmetric geometry to the recently reported normally ON (V_{th}=-3.75 V) AlGaN/GaN HEMT for RF power applications with a gate length of 0.5 μm and an aluminium mole fraction of x=0.26 providing a maximum output current of I_{Dmax}=7.3 A/mm at V_{GS}=1 V and V_{DS}=6 V [27].

The wurtzite phase of GaN HEMT possesses spontaneous and piezoelectric polarizations. III-V nitrides have a spontaneous polarization due to an intrinsic asymmetry of bonding at equilibrium. Moreover, the growth of AlGaN on GaN results in tensile strain and piezoelectric polarizations [28]. The spontaneous (SP) and piezoelectric (PZ) polarizations, a coupling between mechanical and electrical properties, induces a bound sheet charge at the interface serving as a device channel. The net polarization is then calculated as:

$$P_{SP}(x) = (-0.052 \cdot x - 0.029) \, [C/m^2] \tag{1}$$

$$P_{PZ}(x) = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) [C/m^2] \tag{2}$$

where C_{13} and C_{33} denote the elastic constants, e_{31} and e_{33} the piezoelectric constants, and a and a_0 the lengths along the hexagonal crystallographic edge [29]. The following relations are used for the lattice, elastic, and piezoelectric constants:

$$a_0(x) = (-0.077x + 3.189) \times 10^{-10} \, [m] \tag{3}$$

$$C_{13} = (5x + 103) \, [GPa] \tag{4}$$

$$C_{33} = (-32x + 405) \, [GPa] \tag{5}$$

$$e_{33}(x) = (0.73x + 0.73) \ [C \ m^{-2}] \tag{6}$$

$$e_{31}(x) = (-0.11x - 0.49) \ [C \ m^{-2}] \tag{7}$$

where x corresponds to the mole fraction of the relevant layers. The SP and PZ polarizations are taken into account by a net polarization charge of $\sigma_{Pol} = +1.15 \times 10^{13}$ cm^{-2} at the interface and by equal but opposite sign at the surface.

The device dimensions on a micrometer scale suggest that a DD transport model is sufficient [30] to describe the operation of a GaN HEMT. However, non-local transport effects such as local carrier temperature and carrier energy distribution are evidently affecting the device operations [6]. Therefore, we have also employed a HD transport model using the energy balance approach [31], [32]. The relations between carrier energy flux densities and carrier current densities in the HD are given by [33]:
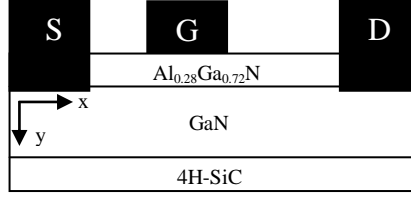

Figure 1. Cross-section of the simulated 0.25 μm gate length GaN HEMT.

$$div \ \overrightarrow{S_n} = \nabla \left(\frac{E_C}{q} - \psi \right) \overrightarrow{J_n} - \frac{3k_B}{2} \left(\frac{\partial(nT_n)}{\partial t} + RT_n + n\frac{T_n - T_L}{\tau_n} \right) \tag{8}$$

$$div \ \overrightarrow{S_p} = \nabla \left(\frac{E_V}{q} - \psi \right) \overrightarrow{J_p} - \frac{3k_B}{2} \left(\frac{\partial(pT_p)}{\partial t} + RT_p + p\frac{T_p - T_L}{\tau_p} \right) \tag{9}$$

where $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the carrier current densities, n and p are the electron and hole concentrations respectively, E_C and E_V are conduction and valence band energies, ψ is the electrostatic potential, K_B is the Boltzmann constant, $T_{n,p}$ are carrier temperatures, $\overrightarrow{S_n}$ and $\overrightarrow{S_p}$ are the electron and hole energy flux densities, R is the available net recombination rate using Shockley-Read-Hall (SRH) model.

Eqs. (8) and (9) involve terms expressing electron and hole energy density loss rates in which heated carriers exchange energy with lattice through recombination and generation processes given by:

$$W_{n,p} = -\frac{3k_B}{2} \left(RT_{n,p} + n\frac{T_{n,p} - T_L}{\tau_{n,p}} \right) \tag{10}$$

where W_n and W_p are energy loss rate of electrons and holes, τ_n and τ_p are electron and hole relaxation times, respectively, all given in Table 1, and T_L is the lattice temperature.

The electrical behaviour of GaN HEMTs is also strongly dependent on the channel temperature [26], [34] significantly modifying output characteristics thus thermal simulations should be coupled with electrical one. The lattice temperature is computed using thermal model at each point of the device [26] and the following heat flow equation is solved in all regions:

$$div \ S_L = -\rho_L c_L \frac{\partial T_L}{\partial t} + H \tag{11}$$

$$S_L = -k_l \nabla T_L \tag{12}$$

$$H = \frac{3k_B}{2} \left(n\frac{T_n - T_L}{\tau_n} + p\frac{T_p - T_L}{\tau_p} \right) + R(E_C - E_V) \tag{13}$$

$$k(T_L) = k_{300} \times \left(\frac{T_L}{300 \ K} \right)^{\alpha} \tag{14}$$

where S_L is the heat flow density, ρ_L is the mass density, c_L is the heat capacitance, H is the heat generation term, k_l is the thermal conductivity, k_{300} is the thermal conductivity at room temperature and α is the coefficient of temperature dependence of thermal conductivity [33].The thermal

conductivity constant (k_{300}) and its coefficient (α) are material quality dependant [35] and given in Table 1. In thermal simulations, Dirichlet boundary conditions are applied [22].

The current collapse in GaN HEMTs has been widely explained by the trapping and de-trapping phenomena. During the operation, electric field present in the device induces defects in its structure [36]. The defects alter the output power density and limit the switching properties of the device [37], [38]. The electrically active defects act as traps with the associated energies in the bandgap and exchange charge within conduction and valence bands through recombination. The charge caused by trapping/de-trapping processes can be added to overall charge as:

$$Q_T = q(N_{tD}^+ - N_{tA}^-) \tag{15}$$

where N_{tD}^+ and N_{tA}^- are the densities of ionized donor and acceptor traps [22], respectively. N_{tD}^+ and N_{tA}^- are dependent on the trap density and probability of ionization as:

$$N_{tD}^+ = \text{Density} \times F_{tD} \tag{16}$$

$$N_{ta}^- = \text{Density} \times F_{tA} \tag{17}$$

where F_{tD} and F_{tA} are the probability of ionization for donor traps and acceptor traps [22], respectively, given by:

$$F_{tA} = \frac{v_n \varphi_n \times n + e_{pA}}{v_n \varphi_n \times n + v_p \varphi_p \times p + e_{nA} + e_{pA}} \tag{18}$$

$$F_{tD} = \frac{v_p \varphi_p \times p + e_{nD}}{v_n \varphi_n \times n + v_p \varphi_p \times p + e_{nD} + e_{pD}} \tag{19}$$

where φ_n and φ_p are the electron and hole capture cross sections, v_n and v_p are the carrier thermal velocities, e_{nA} and e_{pA} are the electron and hole emission rates for acceptor traps, and e_{nD} and e_{pD} are the electron and hole emission rates for donor traps, respectively.

Table 1
Room-temperature values for III-Vs material adopted in the simulations [29], [35]

Material Properties	GaN	AlN
Bandgap	3.4 eV	6.2 eV
Electron capture cross-section	1×10^{-15} cm^2	1×10^{-15} cm^2
Electron relaxation time	0.1 ps	0.1 ps
Hole relaxation time	0.1 ps	0.1 ps
Electron saturation velocity	1.8×10^7 cm/s	2.16×10^7 cm/s
Thermal conductivity	130 W/m K	285 W/m K
Coefficient of temperature dependence of thermal conductivity α	-0.43	-1.57
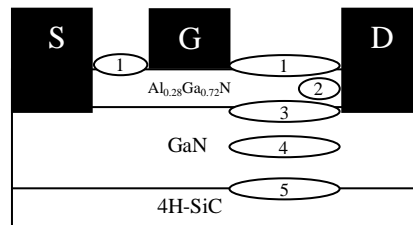
Figure 2. Possible trap locations in GaN HEMTs.

Figure 2 illustrates the location of the traps in a typical GaN HEMT [29]. The possible locations are: 1. interface of semiconductor and dielectric, 2. barrier, 3. interface of barrier and channel, 4. buffer, and 5. interface of substrate and buffer [19].

Empty acceptor traps can capture electrons/emit holes referred to as a trapping. When they are occupied, acceptor traps can also emit electrons or capture holes in a process called a de-trapping.

Similarly, donor traps are neutral when filled with electrons (empty with holes) and positively charged when empty with electrons (filled with holes). Empty donor traps can capture electrons/emit holes during the trapping process. Finally, occupied donor traps can emit electrons/capture holes referred to as a de-trapping (see Table 2).

Table 2
Scheme of trapping/de-trapping processes

Trap Types	DONOR-LIKE	ACCEPTOR-LIKE
Empty Trap Process	Positively Charged Trapping	Neutral Trapping
Occupied Trap Process	Neutral De-Trapping	Negatively Charged De-Trapping

To study surface related current collapse, donor-like traps are uniformly distributed within 5 Å [30], [39] from the surface over access regions with a density of $N_T^{AlGaN} = 5.75 \times 10^{21}$ cm^{-3} [39]. The donor-like traps are located at $E_T\text{-}E_V = 0.1$ eV, 0.2 eV, 0.25 eV, 0.3 eV and 0.4 eV [30], [39] with the electron and hole capture cross sections of $\sigma_n = \sigma_p = 1 \times 10^{-19} cm^2$ [39]. To investigate bulk related current collapse, acceptor-type traps are uniformly distributed in the AlGaN and GaN layers with a density of $N_T^{AlGaN} = 5 \times 10^{16}$ cm^{-3} and $N_T^{GaN} = 2.5 \times 10^{16}$ cm^{-3} and energetically located at $E_C - E_T = 2.2$ eV [24] and $E_C - E_T = 1.8$ eV [40], respectively.

3. Model calibration

Quantum effects due to carrier confinement associated with variation of potential is taken into account by a density gradient (DG) approach. Figure 3 compares electron density across the channel obtained from classical against the DG approach. This quantum correction mimics the penetration of the electron wave function from the channel into the barrier and buffer layers.
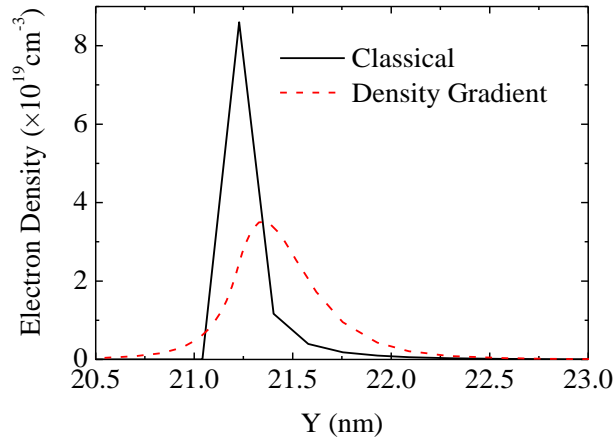
Figure 3. Cross-section of electron density at the drain side of the gate when all contacts are grounded. Solid line illustrates the classical quantum model while dashed line shows the DG quantum model.

Figure 4 compares output characteristics of the GaN HEMT simulated by the DD and HD transport models using DG quantum correction against pulsed experimental measurements with large pulse-off/pulse-on time ration to avoid self-heating effects. All HD simulation results show negative differential conductance (NDC), while DD simulation results display no NDC, but the formation of a potential barrier at the drain side of the gate is consistent with NDC observed in the HD simulations [23]. This calibration of the HD and DD simulations is at heart of our further investigations. The HD transport model is employed to study the trapping and de-trapping processes inside the device resulting in hot-spots and a creation of surface pits [41]. However, the DD transport model is sufficient to investigate the current collapse phenomenon resulting from surface traps [30], [39] because dramatic changes of electron and lattice temperatures inside of the device have no much effect on temperature at the surface which is close to room temperature.
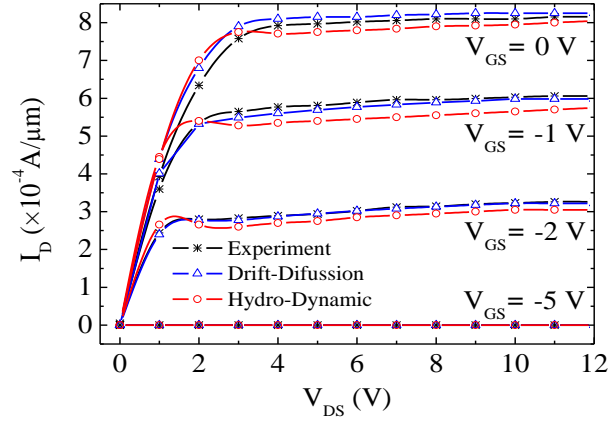
Figure 4. I_D-V_{DS} **characteristics at** V_{GS}=-5 V, -2 V, -1 V and 0 V comparing the HD (circles) including bulk traps at energy levels of 2.2 eV and 1.8 eV in AlGaN and GaN layers, respectively, and the DD simulations (triangles) including surface traps at energy level of 0.25 eV to experimental data (crosses). Since the self-heating is not observed in experiment, it is excluded from the calibration.

4. Transient simulation of trapping

4.1. Surface Traps

To study surface traps, drain voltage is kept constant and gate bias is ramped up from off state (V_{GS}=-5 V) to on state (V_{GS}=0 V) in t=1 ns using gate-lag technique. The term "gate-lag" refers to the transient response of the drain current when gate-source voltage is pulsed.
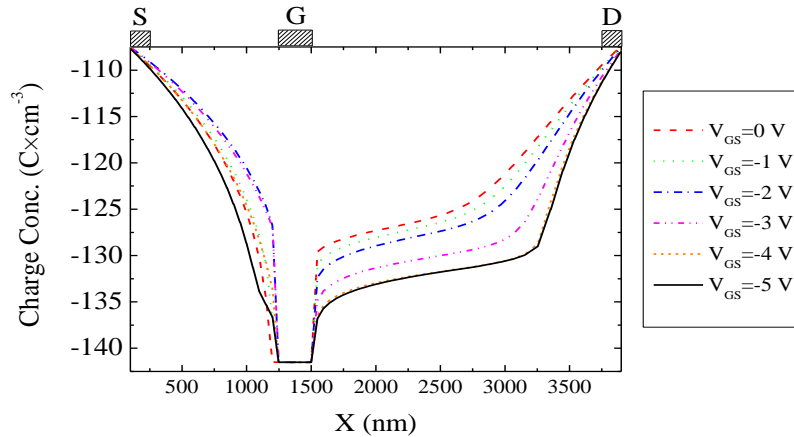

Figure 5. Extracted charge density at the surface of the GaN HEMT at V_{DS}=12 V and V_{GS}=0, -1 V, -2 V, -3 V, -4 V and -5 V.
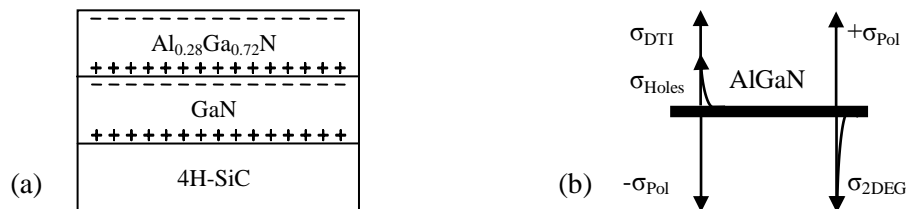

Figure 6. (a) Scheme of polarization charge components . **(b)** scheme of space charge components in a GaN HEMT. σ_{DTI} is the charge due to ionization of donor-like traps at the surface, σ_{Holes} is the charge resulting from hole accumulation at the surface, $\pm\sigma_{Pol}$ is the polarization charge, and σ_{2DEG} is the charge of two-dimensional electron gas.

Surface-related drain current collapse is attributed to "virtual gate" on the access region between the gate and the drain. When device is switched off abruptly, the virtual gate depletes regions under the drain side of the gate through the trapped charge at the surface. The trapped charge is due to tunneling of electrons from the gate to the regions next to the drain side of the gate moving by a hopping

mechanism at the surface (see figure 5) [30]. At low gate biases, a more negative charge is accumulated at the surface on the drain side of the gate. In contrast, the source side of the gate, due to a different bias compared to the drain, has a different conduction and valence band profiles. As the gate bias is increased to V_{GS}=-2 V and beyond, the Fermi level starts to be pinned close to and then above the energy level of donor traps at the surface. The energy position of the donor traps close to Fermi level leads to negligible generation of electrons, as they cannot acquire enough energy to ionize. Consequently, the ionization rate of donor traps is reduced lowering a generation of holes and reducing the positive charge coming from the holes at the surface.

At equilibrium, the charge neutrality requires number of electrons in the 2DEG to be equal to the number of ionized donor-like traps at the surface in the absence of any doping in AlGaN layer. In other words, there is a number of holes at the surface of the structure which can participate in trapping and de-trapping processes by capturing and releasing the electrons [see figures 6(a) and 6(b)]. As a consequence, any modification to the positive charge at the surface leads to a change in 2DEG density and thus in a drain current. The positive charge is provided by ionization of donor-like traps (in dependence on applied bias) which are the source of electrons in AlGaN/GaN HEMTs [42], holes at the surface (resulting from negative polarization charge), or by both [30].

When the device is switched off at V_{GS}=-5 V, electrons start to tunnel from the gate to the channel and access regions reducing the positive charge at the surface. Consequently, due to trapped charge at regions close to the gate, the 2DEG gets depleted. In the presence of the donor-like traps, the virtual gate behavior becomes the function of net capture and emission rates of the carriers. This behavior corresponds to the delayed drain current switching called the current collapse seen as ΔI in figure 7. Traps with energy level at E_T=0.25 eV [39] show a good agreement with experimental results (compare figure 4 at V_{GS}=0 V and V_{DS}=12 V to figure 7 with energy level at 0.25 eV). Traps with the energy levels close to valence band are mostly neutral and the negative surface charge due to polarization charge is at a maximum level (see figure 7 where $\Delta I_{0.1} < \Delta I_{0.4}$). However, traps with higher energy levels reduce the net negative charge given by $\sigma_{Net} = -\sigma_{Polarization} + \sigma_{DTI} + \sigma_{Holes}$ [39] at the surface consequently increasing electron density of 2DEG resulting in an increase of the drain current where σ_{DTI} is the charge due to ionization of donor-like traps at the surface.
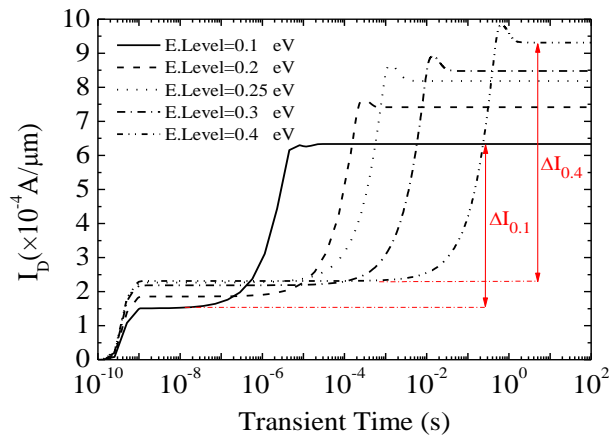
Figure 7. Transient response of drain current (log scale) to a V_{GS} ramp up pulse at V_{DS}=12 V and V_{GS}=-5 V to V_{GS}=0 V due to surface traps to different energetic positions of the donor-like traps with respect to valence band position using the DD transport model at T=300 K.

The effect of surface traps on instability issues have been investigated in great details in the literature and, for example, a very detailed study looking at the current collapse due to donor-like surface traps have been given by Meneghesso *et al* (2004) [30] and Tirado *et al* (2006). [39]. Furthermore, recent publications presenting power HEMT devices suggest that advanced surface passivation techniques employing various dielectrics, such as the thin HfO$_2$ layer, are very effective in relieving the current collapse issue in power HEMTs by reducing the density of surface traps [43], [44] and [45]. The reports also suggest that two HEMTs manufactured at the same time employing same processes on two different types of commercial substrates could have significantly different current collapse properties [44]. These have been linked to the inherent bulk trap profiles present in the substrates.

Bearing in mind that future power HEMT devices could use a bulk region as alternative current paths [46], device designers would need to have detailed understanding of bulk trapping mechanisms and their effect on power device electric properties. In what follows, bulk trapping has been investigated in great details.

4.2. Bulk Traps

Pulsed *I-V* set-up is normally performed in the sub-microsecond range [47]. Using drain-lag technique, the gate voltage is kept constant and drain voltage is ramped up or down. The term "drain-lag" describes the transient response of the drain current when drain-source voltage is pulsed. When a drain voltage is increased from V_{DS}=0.1 V to V_{DS}=12 V during the ramp time of t=1 μs, electrons in the channel regions next to the drain-side edge of the gate will be significantly heated up to T_e=6740 K (see figure 8) when gaining a very large kinetic energy of approximately 0.9 eV [48] spreading further away from the channel into AlGaN and GaN layers. However, this large kinetic electron energy will not be efficiently transferred to the lattice (energy of polar optical phonon in GaN is 91.2 meV and in AlN 99.2 meV) resulting in creation of a hot spot close to the gate expanding toward drain at increasing drain bias and an increase of the lattice temperature to around T_L=590 K (assuming an initial lattice temperature of T=300 K) as observed in the comprehensive thermal HD modeling of the device (see figure 9).
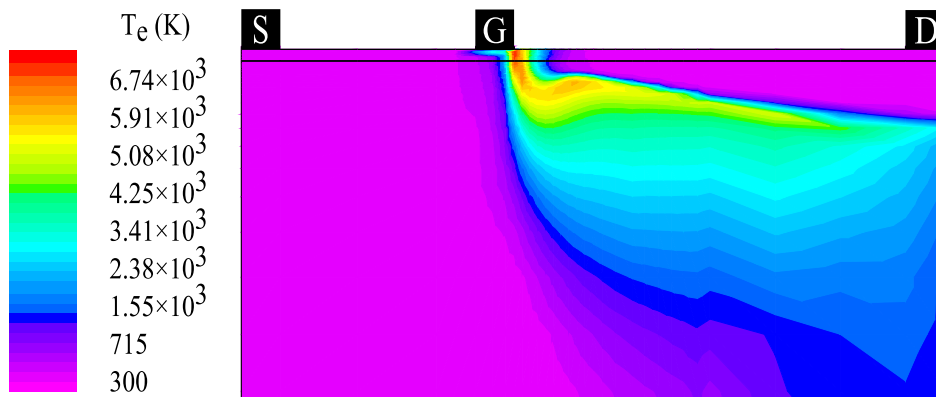

Figure 8. Distribution of electron temperature under the gate in the device at V_{DS} = 12 V and V_{GS} = 0 V.
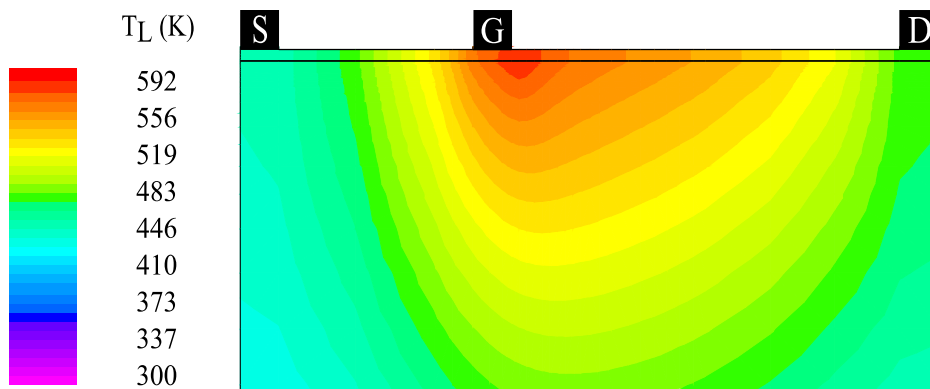

Figure 9. Distribution of lattice temperature in the device at V_{DS} = 12 V and V_{GS} = 0 V.

In the presence of the acceptor-like traps, hot electrons can recombine with the traps as illustrated in figure 10 by a sharp current decline resulting from change in electron capture and emission rates of trapping and de-trapping processes. These processes lead to a modification in charge distribution in the device due to addition/removal of the trapped charge. Acceptor-like traps close to the channel get filled with electrons quickly during electrical stress, while deep traps require more time and hotter electrons. After electrical stress, some of the filled traps start emitting electrons. Since the electrons liberated through de-trapping process aim for the lowest possible energy states, these emitted electrons return to the channel thus reducing a net capture rate of the device (see figure 11). Simulation results

show the recovery time of $t_{\text{recovery}} = 10^3$ s which is in a good agreement with the experimental results by Joh *et al* (2012) [12].

The strength of trapping and de-trapping processes changes in time and one could be dominant. When the drain is ramped up, the trapping process becomes dominant while, after electrical stress, the de-trapping process starts to increase from its initial value till equilibrium is reached. Finally, this dynamic process reaches a new steady-state and the drain current is stabilized.
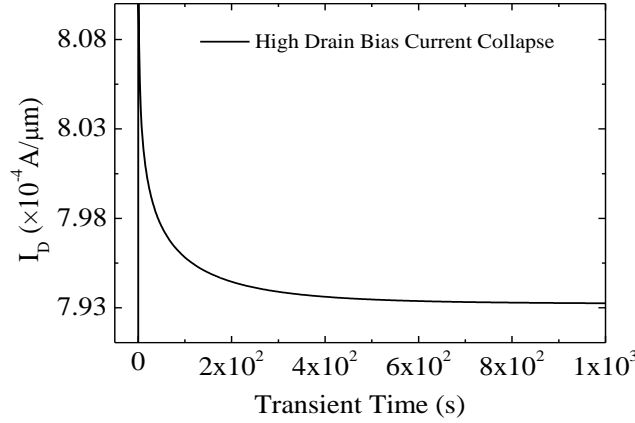
Figure 10. Transient response of drain current (expanded plot) due to bulk traps to a V_{DS} ramp-up pulse at V_{GS}=0 V and V_{DS}=0.1 V to V_{DS}=12 V using the HD transport model.
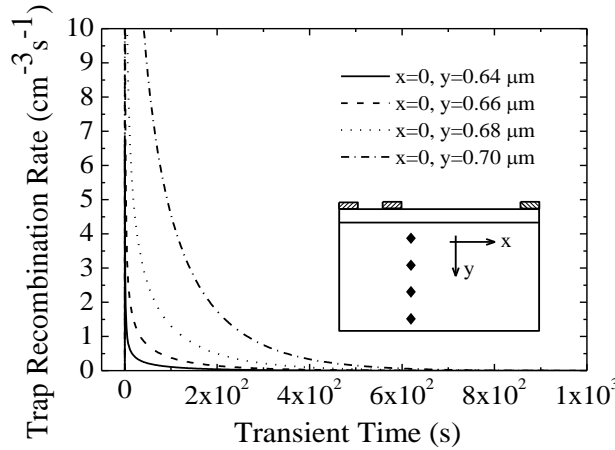

Figure 11. A V_{DS} ramp-up trap electron capture rate along the *y*-direction; inset shows the schematic of the device showing the locations (♦) where recombination rates were probed. X=0 µm is set to be at the drain side of the gate.

Figure 11 illustrates the normalized trap recombination rate which is governed by electron capture rate against time. To provide a better insight into the trapping and de-trapping processes, we probe the recombination rate at four positions under the drain side of the gate. The regions close to the gate reach the equilibrium faster than the regions far from the gate as the trapped electrons far from the gate have a higher kinetic energy. Consequently, these electrons require more time to relax and to return to the channel in comparison to the trapped electrons in regions close to the gate. This behavior clearly shows the importance of the trapped electrons not at the vicinity of the gate which has been ignored in some previous works [24].

Figures 12(a) and 12(b) show the simulated transient response to a V_{DS} ramped down from V_{DS}=12 V to V_{DS}=0.1 V at V_{GS} = 0 V where the recovery time shows a good agreement with the experimental work by DasGupa *et al* (2012) [49]. At V_{DS}=12 V, a number of traps are filled with electrons and the net trapped charge is at maximum level in the device (see figure 13). After applying electrical stress, the system of trapping and de-trapping finds itself far from equilibrium conditions as the previous

filling mechanism has being interrupted. Consequently, filled traps start emitting electrons (see figure 14). This behavior corresponds to the reduction of trapped charge and modification of charge distribution in the device. Consequently, the number of the electrons in the channel is significantly increased resulting in increase in the drain current. When the drain voltage is pulsed down, the de-trapping process becomes dominant as observed in experiment [49].
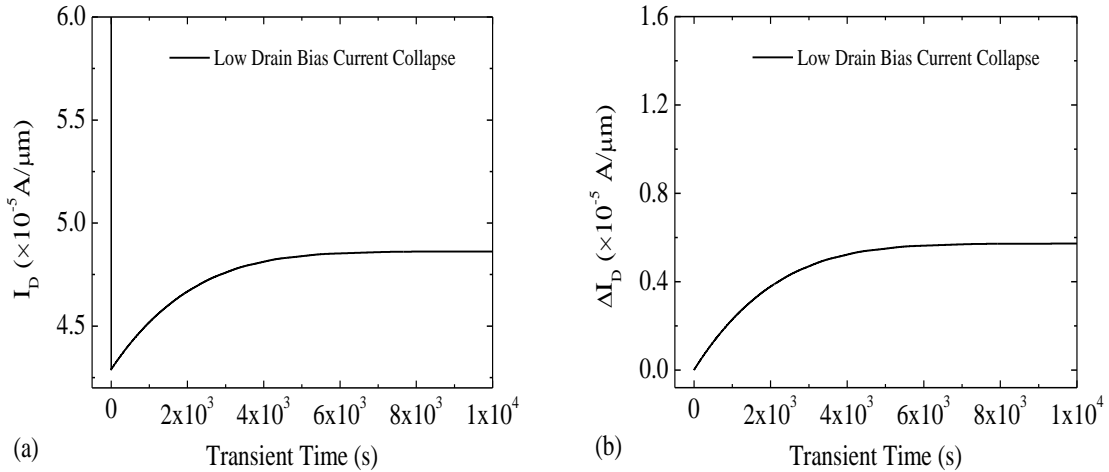
Figure 12. (a) Transient response of drain current (expanded plot) due to bulk traps to a V_{DS} ramp-down at V_{GS}=0 V and V_{DS}=12 V to V_{DS}=0.1 V using the HD transport model. (b) Transient response of drain current due to bulk traps to a V_{DS} ramp-down at V_{GS}=0 V and V_{DS}=12 V to V_{DS}=0.1 V using the HD transport model when current is defined as: $\Delta I_D(t) = I_D(t) - I_D(0)$ where $I_D(0)$ is the current at the first recorded instant of de-trapping [49].
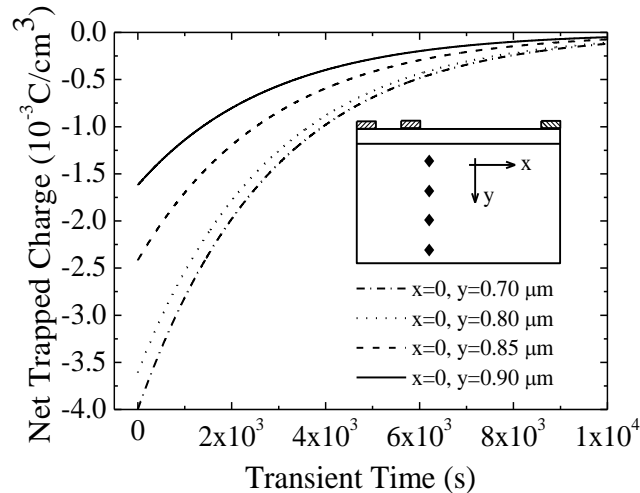
Figure 13. A V_{DS} ramp-down trap net trapped charge density as a function of y-direction at V_{DS}=12 V and V_{GS}=0 V; inset shows the schematic of the device showing the locations (♦) where net trapped charge was probed.

Figure 14 represents a normalized trap recombination rate governed by the electron emission rate in four different positions under the gate. The regions far from the gate reach equilibrium faster than the regions close to the gate. The electrons in the regions far from the gate have a larger kinetic energy and will relax to the lowest possible energy state faster than the electrons with a smaller kinetic energy.

Figure 15 shows the current collapse as a function of drain bias. At a large drain bias, the electron trapping is intensified resulting in enhanced current collapse. This increase in the current collapse is due to higher kinetic energy the electrons have gained from the large applied voltage. The higher energy leads to the increase in trapping as a larger number of electrons spreads from the channel to barrier and buffer and more traps are occupied. On the other hand, at a low drain bias, the hot electron effects are negligible resulting in a smaller current collapse.
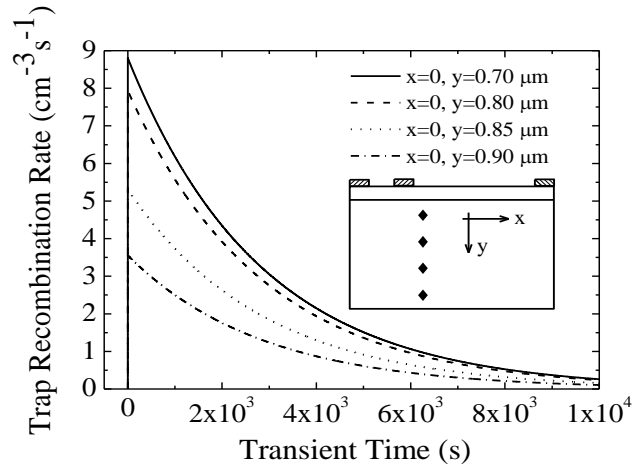
Figure 14. A V_{DS} pulse-down trap electron emission rate as a function of the *y*-direction; inset shows the schematic of the device showing the locations (♦) where recombination rates were probed.
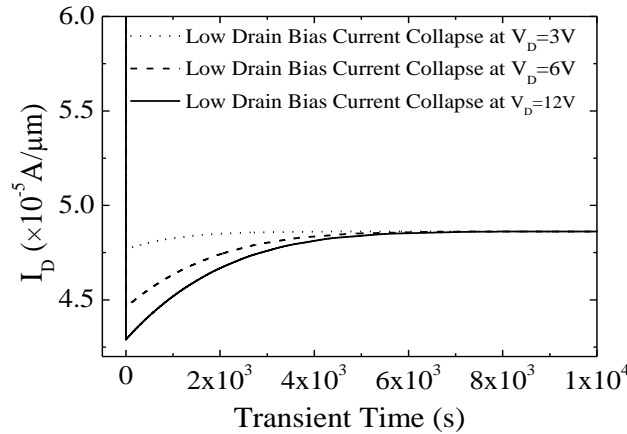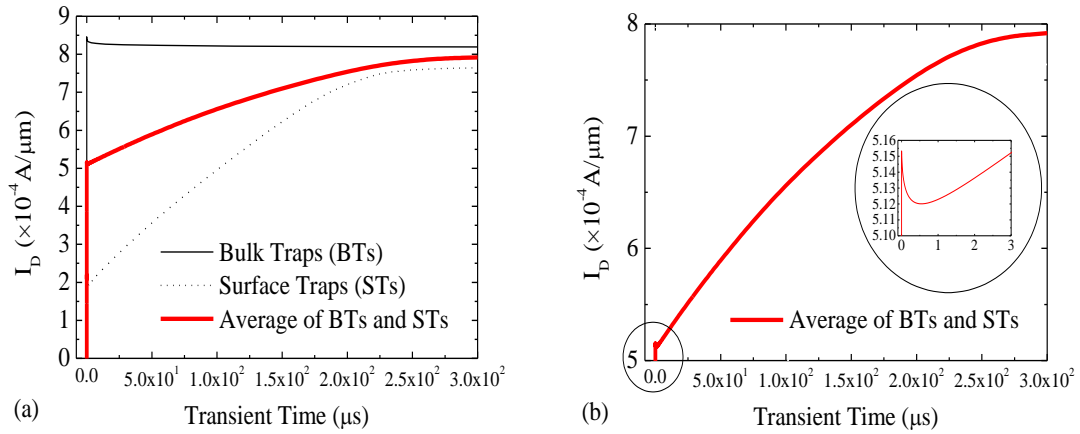

Figure 15. Transient response of drain current (expanded plot) due to bulk traps to a V_{DS} ramp-down at V_{GS}=0 V and V_{DS}=12 V, 6 V and 3 V to V_{DS}=0.1 V using the HD transport model.

Using the HD transport model and the gate-lag technique, transient simulations are performed to investigate the effect of acceptor-like traps in the bulk on output characteristics of the device. The simulations focus on the transition period between the off- and on-states to highlight the transient response. When the system of trapping and de-trapping is at equilibrium off-state (V_{GS}=-5 V and V_{DS}=12 V) and a single gate-ramp up pulse is applied to the system (a ramp-up pulse from V_{GS}=-5 V to V_{GS}=0 V in *t*=1 ns at V_{DS}=12 V), the current collapse is observed. At V_{GS}=-5 V, regions under the gate become depleted from electrons and trapping and de-trapping rates are negligible. When the device is switched on by ramping up from V_{GS}=-5 V to V_{GS}=0 V, electrons acquire enough energy to get captured by acceptor-like traps in the bulk. Later on, the filled traps start to emit electrons and the emission rate begins to increase. The emitted electrons from the acceptor-like traps start to return to the channel stabilizing the drain current and reaching a new equilibrium between trapping and de-trapping mechanisms [see bulk traps in figure 16(a)]. Analogously, the DD transport model and the gate-lag technique are used to study the effect of surface traps on output characteristics of the device. At V_{GS}=-5 V, the "virtual gate" resulting from the trapped charge at the surface depletes regions under the drain side of the gate. When the device is switched on by a ramp-up pulse from V_{GS}=-5 V to V_{GS}=0 V in *t*=1 ns at V_{DS}=12 V, in the presence of donor-like traps, the behavior of the device becomes the function of the net capture and emission rates of the carriers leading to a slow transition in the output

current between the end of electrical stress and steady state, i.e. current collapse occurs [see surface traps in figure 16(a)].

The recovery in the drain current during the gate-lag measurements (due to de-trapping) is mostly explained by donor-like traps at the surface [30], [39]. This effect can be also modeled individually assuming either non-uniform acceptor-like trap distribution at the vicinity of the gate [50] or interface acceptor-like traps [25]. The current collapse observed in experiments [6], [25] can be then explained by averaging between surface and acceptor traps in the device as illustrated in figure 16(a). This suggests that the transient behavior due to gate-lag technique observed in the experiments cannot be assigned to just one type of traps located at the interface [25]. Moreover, the spike seen in the experiments is not due to measurement circuit switching imperfection, but due to the bulk trapping [see figure 16(b)].

Figure 16. Transient response of drain current due to bulk traps (BTs) obtained from HD transport model and surface traps (STs) at energy level=0.2 eV to a V_{GS} ramp-up from -5 V to 0 V (a gate lag technique) and V_{DS}=12 V using the DD transport model. (a) The combine current resulting from the bulk and surface traps under the same bias conditions as seen in experiment [6], [25]. (b) The extended plot of the combine current to clarify the spike at the beginning of the transition due to the bulk traps (see enlargement in the inset).

5. Conclusion

The surface and the bulk trapping transient simulations affecting performance of AlGaN/GaN HEMTs were studied using 2D DD and HD transport models including thermal coupling using Atlas simulation toolbox by Silvaco [22]. The both transport models were calibrated against output characteristics of the 0.25 μm gate length AlGaN/GaN HEMT. Firstly, the gate-lag technique was employed to study a dynamic nature of capture and emission rates of the surface traps. Secondly, the drain-lag techniques were used to investigate the behavior of the traps in the barrier and buffer layers of the device. Later, the gate-lag technique was also employed to investigate traps in the barrier/buffer layers.

It has been observed that the convergence and simulation run-time become more critical when the HD transport model is employed. In addition, a more complex mesh profile is necessary for a faster convergence when using the HD transport model. Therefore, the DD model is preferable over the HD model if non-local effects such as carrier temperature can be neglected. Finally, the electrical model coupled with the thermal model has been found to be essential for investigations of the current collapse.

Using the DD transport model and the gate-lag technique, we have investigated a virtual gate profile at the source and drain sides of the gate. We have found that the profile at the source side of gate exhibits a transient behavior when Fermi level pins around the donor trap energy at the surface but this has a negligible effect on output characteristics of the device. When using the HD model, we observed that electron temperature can increase up to about T_e=6740 K at V_{GS}=0 V and V_{DS}=12 V. The high electron temperature leads to creation of a hot spot with the lattice temperature of T_L=592 K at the vicinity of the gate spreading toward the drain which can result in the generation of defects by piezoelectric stress [12] or generation of dislocations [51]. This can seriously damage device integrity and trigger the onset of breakdown [41]. This is due to a large kinetic energy of electrons ($E{\approx}0.9$ eV for T_e=6740 K)

in the channel, but depends also on the 2DEG density, i.e., under the same bias conditions, the 2DEG with a lower electron density can acquire a larger energy intensifying the current collapse.

To evaluate the influence of the traps on the drain current, simulations have been performed for surface and bulk traps individually using the drain-lag technique. The initial current collapse due to the existence of the donor-like traps at the surface results in the increase of the drain current over recovery time by 75 %. However, the current dispersion related to bulk effects resulting from the acceptor-like traps in the bulk leads to reduction of the drain current by about 5 % over time. Drain-lag simulation results for the bulk traps shows a good agreement of recovery times with experimental results [12], [49] where the recovery times are $t=10^3$ s and $t=10^4$ s for high and low drain biases, respectively.

Our modeling of the gate-lag technique provides a detailed insight into the experimental behavior since the effects of surface and bulk traps cannot be decoupled. We have found that while the bulk traps are responsible for the initial spike for the current collapse during gate-lag measurement, the later current recovery observed in experiment is entirely due to the surface traps. However, the interface traps play only a minor role in trapping and de-trapping processes over time. This suggests that a surface passivation can be employed to mitigate the current collapse.

Acknowledgment

References
[1] Zhang N, Mehrotra V, Chandrasekaran S, Moran B, Shen L, Mishra U, Etzkorn E and Clarke D 2003 Large area GaN HEMT power devices for power electronic applications: switching and temperature characteristics, *Power Elec. Spec. Conf.* **1** 233-37

[2] Wu Y F, Keller B P, Keller S, Kapolnek D, Kozodoy P, Denbaars S P, and Mishra U K 1997 High power AlGaN/GaN HEMTs for microwave applications *Solid-St. Electron.* **41** 1569-74

[3] Hodge M D, Ventury R, Shealy J and Adams R 2011 A Robust AlGaN/GaN HEMT technology for RF switching applications, *Proc. Compound. Semicond. Integ. Circ. Symp.* 1-4

[4] Yue Y, Hu Z, Guo J, Sensale-Rodriguez B, Li G, Wang R, Faria F, Fang T, Song B, Gao X, Guo S, Kosel T, Snider G, Fay P, Jena D and Xing H 2012 InAlN/AlN/GaN HEMTs with regrown ohmic contacts and *fT* of 370 GHz *IEEE Electron Device Lett.*, **33** 988-90

[5] Singisetti U, Wong M H, Speck J S and Mishra U K 2012 Enhancement-mode N-polar GaN MOS-HFET with 5-nm GaN channel, 510-mS/mm g_m, and 0.66-Ω · mm R_{on}, *IEEE Electron Device Lett.* **33** 26-28

[6] Meneghesso G, Verzellesi G, Danesin F, Rampazzo F, Zanon F, Tazzoli A, Meneghini M and Zanoni E 2008 Reliability of GaN high-hlectron mobility transistors: State of the Art and Perspectives *IEEE Trans. Device Matter. Rel.* **8** 332-43

[7] Klein P B, Binari S C, Ikossi K, Wickenden A E, Koleske D D and Henry R L 2001 Effect of deep traps on sheet charge in AlGaN/GaN high electron mobility transistors *Electronics Letts.* **37** 1550-51

[8] Thesis T N and Wright S L 1986 Origin of residual persistent photoconductivity in selectively doped GaAs/Al$_x$Ga$_{1-x}$As heterojunctions *Appl. Phys. Lett.* **48** 1374-76

[9] Hirsch M T, Wolk J A, Walukiewicz W and Haller E E 1997 Persistent photoconductivity in n-type GaN, *Appl. Phys. Lett.* **71** 1098-00

[10] Binari S C, Kruppa W, Dietrich H B, Kelner G, Wickenden A E and Freitas Jr J A 1997 Fabrication and characterization of GaN FETs *Solid-St. Electron.* **41** 1549-54

[11] Binari S C, Ikossi K, Roussos J A, Kruppa W, Park D, Dietrich H B, Koleske D D, Wickenden A E, and Henry R L 2001 Trapping effects and microwave power performance in AlGaN/GaN HEMTs *IEEE Trans. Electron. Devices* **48** 465-71

[12] Joh J and del Alamo J A 2011 A current-transient methodology for trap analysis for GaN high electron mobility transistors *IEEE Trans. Electron Devices* **58** 132-40

[13] Ventury R, Zhang N Q, Keller S, and Mishra U K 2001 The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs *IEEE Trans. Electron Devices* **48** 560-66

[14] Koley G, Tilak V, Eastman L F, and Spencer M G 2003 Slow transients observed in AlGAN/GaN HFETs: Effects of SiN$_x$ passivation and UV illumination *IEEE Trans. Electron Devices* **50** 886-93

[15] Faramehr S, Kalna K, and Igić P 2012 Simulation of current collapse in the 0.25 gate length Al$_{0.28}$Ga$_{0.72}$N/GaN HEMT *Proc. Int. Conf. Microelec. (Miel)* 233-36

[16] Pavlidis D, Valizadeh P and Hsu S H 2005 AlGaN/GaN high electron mobility transistor (HEMT) reliability *Proc. GaAs Symp.* 265–68

[17] Faramehr S, Igić P and Kalna K 2012 TCAD modelling of current dispersion in a 0.25 μm gate length GaN HEMT *Proc. Int. Conf. Adv. Semicond. Microelec. (ASDAM)*

[18] Chini A, Lecce V Di, Esposto M, Meneghesso G, Zanoni E 2009 RF degradation of GaN HEMTs and its correlation with DC stress and I-DLTS measurements, *Proc. Eur. Microwave Integ. Circ. (EuMIC)*132-35

[19] Binari S C, Klein P B, and Kazior T E 2002 Trapping effects in GaNand SiC microwave FETs *Proc. IEEE* **90** 1048–58

[20] Mizutani T, Ohno Y, Akita M, Kishimoto S and Maezawa K 2003 A study on current collapse in AlGaN/GaN HEMTs induced by bias stress *IEEE Trans. Electron Devices* **50** 2015–20

[21] Ťapajna M, Simms R J T, Pei Y, Mishra U K, and Kuball M 2010 Integrated optical and electrical analysis: identifying location and properties of traps in AlGaN/GaN HEMTs during electrical stress *IEEE Electron Device Letts.* **31** 662-64

[22] Silvaco, inc. 2012 *Atlas user manual* (Santa Clara: Silvaco Inc.)

[23] Braga N, Mickevicius R, Gaska R, Hu X, Shur M S, Khan M A, Simin G and Yang J 2004 Simulation of hot electrons and quantum effects in AlGaN/GaN heterostructure field effect transistors *J. Appl. Phys.* **95** 6409-13

[24] Hu W D, Chen X S, Yin F, Zhang J B and Lu W 2009 Two-dimensional transient simulations of drain lag and current collapse in GaN-based high-electron-mobility transistors, *J. Appl. Phys.* **105** 0845021-27

[25] Zhang W, Zhang Y, Mao W, Ma X H, Zhang J C and Hao Y 2013 Influence of the interface acceptor-like traps on the transient response of AlGaN/GaN HEMTs *IEEE Electron Device Lett.* **34** 45-47

[26] Benbakhti B, Soltani A, Kalna K, Rousseau M and De Jaeger J C 2009 Effects of self-heating on performance degradation in AlGaN/GaN-based devices *IEEE Trans. Electron Devices* **56** 2178-85

[27] Marcon D, Viaene J, Vanaverbeke F, Kang X, Lenci S, Stoffels S, Venegas R, Srivastava P and Decoutere S 2012 GaN-on-Si HEMTs for 50 V RF Applications *Proc. Eur. Microwave Integ. Circ. Conf.* (EuMIC) 325-28

[28] Mishra U K, Parikh P and Wu Yi F 2002 AlGaN/GaN HEMTs-an overview of device operation and application *Proc. IEEE* **90** 1022-31

[29] Quay R 2008 *Gallium nitride electronics* ed R Hull *et al* (Leipzig: Springer)

[30] Meneghesso G, Verzellesi G, Pierobon R, Rampazzo F, Chini A, Mishra U K, Canali C and Zanoni E 2004 Surface-related drain current dispersion effects in AlGaN–GaN HEMTs*", IEEE Trans. Electron Devices* **51** 1554-1561

[31] Stratton R 1962 Diffusion of hot and cold electrons in semiconductor barrier *Phys. Rev.* **126** 2002-14

[32] Stratton R 1972 Semiconductor current-flow equations (diffusion and degeneracy) *IEEE Trans. Electron Devices* **19** 1288-92

[33] Palankovski V and Quay R 2004 Analysis and simulation of heterostructure devices ed S Selberherr (Wien: Springer-Verlag)

[34] Joh J, del Alamo J A, Chowdhury U, Chou T M, Tserng H Q and Jimenez J L 2009 Measurement of channel temperature in GaN high-electron mobility transistors *IEEE Trans. Electron Devices* **56** 2895-00

[35] Vitanov S, Palanovski V, Maroldt S and Quay R 2009 High-temperature modelling of AlGaN/GaN HEMTs *Solid-State Electronics* **54** 1105-12

[36] Joh J and del Alamo J A 2006 Mechanisms for electrical degradation of GaN high-electron mobility transistors *IEDM Tech. Dig.* 415-18

[37] Joh J and del Alamo J A 2011 A current-transient methodology for trap analysis for GaN high electron mobility transistors *IEEE Trans. Electron Devices* **58** 132-40

[38] Koudymov A, Simin G, Khan M A, Tarakji A, Gaska R and Shur M S 2003 Dynamic current-voltage characteristics of III-N HFETs *IEEE Electron Device Lett.* **24** 680-82

[39] Tirado J M, Sanchez-Rojas J L and Izpura J I 2006 Simulation of surface state effects in the transient response on AlGaN/GaN HEMT and GaN MESFET devices *Semicond. Sci. Technol.* **21** 1150-59

[40] Klein P B, Binari S C, Ikossi-Anastasiu K, Wickenden A E, Koleske D D, Henry R L and Katzer D S 2001 Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy *Appl. Phys Lett.* **79** 3527-29

[41] Bajo M M, Hodges C, Uren M J and Kuball M 2012 On the link between electroluminescence, gate current leakage, and surface defeats in AlGaN/GaN high electron mobility transistors upon off-state stress *Appl. Phys. Lett.* **101** 0335081-84

[42] Ibbetson J P, Fini P T, Ness K D, DenBaars S P, Speck J S and Mishra U K 2000 Polarization effects, surface states, and the source of the electrons in AlGaN-GaN heterostructure field effect transistors *Appl. Phys. Lett.* **77** 250-52

[43] Fontsere A, Perez-Tomas A, Banu V, Godignon P, Milan J, Vleeschouwer H De, Parsey J M and Moens P 2012 A HfO_2 based 800V/300°C Au-free AlGaN/GaN-on-Si HEMT Technology *Proc. Int. Symp. Power Semicond. Devices (ISPSD)* 37-40

[44] Hwang I, Choi H, Lee J W, Choi H S, Kim J, Ha J, Um C Y, Hwang S K, Kim J Oh J Y, Shin J K, Park Y, Chung U In, Yoo In K, and Kim K 2012 1.6kV, 2.9 mΩ cm^2 normally-off p-GaN HEMT device *Proc. Int. Symp. Power Semicon. Devices (ISPSD)* 41-44

[45] Li Z, Waldron J, Dayal R, Parsa L, Hella M and Chow T P 2012 High voltage normally-off GaN MOSC-HEMTs on silicon substrate for power Switching Applications *Proc. Int. Symp. Power Semicond. Devices (ISPSD)* 45-48

[46] Mishra U K 2010 AlGaN/GaN transistors for power electronics 2010, *IEDM* 13.2.1-4

[47] Joh J, del Alamo J A and Jimenez J 2008 A simple current collapse measurement technique for GaN high-electron mobility transistors *IEEE Electron Device Lett.* **29** 665-67

[48] Rousseau M, Soltani A and De Jaeger J C 2012 Efficient physical-thermal model for thermal effects in AlGaN/GaN high electron mobility transistors *Appl. Phys. Lett.* **101** 1221011-3

[49] DasGupa S, Sun M, Armstrong A, Kaplar R J, Marinella M J, Stanley J B, Atcitty S and Palacios T 2012 Slow detrapping transients due to gate and drain bias stress in high breakdown voltage AlGaN/GaN HEMTs *IEEE Trans. Electron Devices* **8** 2115-22

[50] Braga N, Mickevicius R, Gaska R, Shur M S, Khan M A and G Simin 2004 Simulation of gate lag and current collapse in gallium nitride field-effect transistors *Appl. Phys. Lett.* **85** 4780-82

[51] Ťapajna M, Kaun S W, Wong M H, Gao F, Palacios T, Mishra U K, Speck J S, and Kuball M 2011 Influence of threading dislocation density on early degradation in AlGaN/GaN high electron mobility transistors, Appl. Phys. Lett. **99**, 223501