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Microarticle

Characterising lateral capacitance of MNOSFET with localised trapped charge in nitride layer

A.E. Atamuratov[a], Z.A. Atamuratova[a], A. Yusupov[a], A. Ghani[b,*]

[a] Department of Physics, Urgench State University, Urgench, Uzbekistan
[b] School of Computing, Electronics and Mathematics, Coventry University, Coventry, CV1 5FB, UK

ABSTRACT

This paper discusses the limitations of scanning microscope to read localised charge and proposes a viable solution. A 2D simulation and characterisation of the capacitance-voltage (C-V) characteristics of the lateral source-base transition of metal-nitride-oxide-semiconductor field effect transistor (MNOSFET) with charge trapped in nitride layer is presented. It is shown that C-V dependence is changed after trapping the localised charge in nitride layer. The change depends on position of the localised trapped charge. An n-channel transistor is considered with acceptor concentration in base of 10^{16} cm^{-3}. By localising a charge bit with linear size of 80 nm in nitride layer, it is observed that capacitance jump in C-V dependence starts at some bias voltage applied to the source-base transition. This voltage depends on the position of charge bit. This dependence can be used in determining the charge bit position in the nitride layer along channel. To the best of the author's knowledge, it is one of the most efficient methods in scanning localised charge.

Introduction

In determining dopant profiles in ion implanted semiconductors, mapping of defect distribution and reading of data in non-volatile memory elements can be achieved by using scanning microscopy. For example, the localised charge as a bit information trapped in silicon nitride film of rotating nitride-oxide-semiconductor (NOS) disk is detected by the effect which the charges have on the capacitance of depletion layer [1]. As stated in [2] that in order to register charge bit with scanning capacitance microscopy, electrostatic force microscopy is used for extracting data about localised potential and surface capacitance of semiconductor [3]. In [4] atomic force microscope (AFM) is used to write and read information bit with linear size of 40 nm. The scanning microscopy has high spatial resolution but its use is limited in applications related with scan or reading speed. It is mainly because the scan rate is limited by the feedback response time. Secondly, scanning microscopes have expensive and complex electromechanical components to move either tip or sample and optical systems (laser, photodetector) for registration.

While using scanning microscope, the measurements are usually taken at the surface of non-coated sample. In this work, it is investigated whether it is possible to read localised charge (charge bit) trapped in MNOSFET by non-destructive method, without using the movable probe, rather by applying scanning voltage to source-base (or drain-base) transition which allows to reach enough scan rate to read data. By applying sawtooth sweep voltage, the scan rate becomes dependent on the period of sawtooth voltage. Similarly, by increasing the bias voltage applied to source-drain transition, the width of depletion layer is increased too. Hence, the transition capacitance decreases inversely to the width and directly to the area of transition. The trapped localised charge should also affect the width of depletion layer and correspondingly the capacitance of the transition in dependence on position. If the dependence is known by measuring the change of capacitance, it is possible to estimate charge bit position. Therefore, sawtooth scan voltage may be used as scanning to read bit information in the form of localised charge trapped in silicon nitride layer. In this case, the channel of transistor can be considered as word line in random access read-only non-volatile memory element. Hence, considering 2D simulations is enough and expedient for this case.

Structure and simulations

The main purpose of this work is to investigate dependency between lateral position along channel of localised charge bit trapped in silicon nitride layer and capacitance C_{sb} of the source-base transition. In this work only localisation of one charge bit is considered whereas localisation of two charge bits and their spatial resolution will be considered in the following work. The position of localised charge is determined by distance L between source and the center of localised charge (Fig. 1). The localised charge bit is modelled as uniform charge area in silicon nitride layer with linear size 80 nm lengthways channel which is available for silicon nitride layer [2]. Whereas the volume density of the charge is $8 \cdot 10^{18}$ cm^{-3} for charged area which is comparable with a reported value of the trap density in silicon nitride [2].

* Corresponding author.

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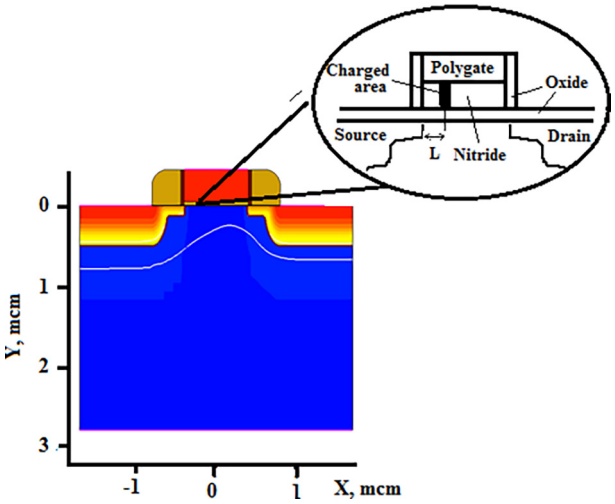

Fig.1. The simulated MNOSFET structure. At insertion, charged area and distance L between source and center of charged area is shown.

A 2D simulation is performed by using a commercial device simulator TCAD Sentaurus. The linear size of the transistor channel have submicron scale, therefore, drift-diffusion model was used for mobility. The Shockley-Read-Hall recombination, the high field saturation model for velocity and influence of normal component of field was accounted for in this model. The C-V dependence is simulated by using small signal AC analysis at 1 MHz. An n-channel silicon MNOSFET (Fig. 1) is simulated, where source and drain areas were doped by Arsenic with Gaussian profile and maximal concentration 10^{20} cm^{-3}. A silicon base (substrate) was doped uniformly by boron with concentration 10^{16} cm^{-3}. Length of polysilicon gate is 800 nm. The insulating layer consists of SiO_2 with thickness 3 nm covered by silicon nitride layer with thickness 50 nm. Simulation of the C-V dependence of source-base transition is performed by using small-signal AC analysis at 1 MHz.

Simulation results

It has been investigated and shown that the influence of the localised charge trapped in insulating layer on capacitance of source-drain transition depends on parameters and position of the charge [5,6]. It is caused by the influence of the charge to geometry of the transition depletion layer. In [2] it is shown that by applying voltage to MNOS structure, it is possible to embed in a silicon nitride layer a localised charge with minimal linear size 75 nm, caused by the charge tunnelling through oxide layer. In retrospect, the influence of the positive localised charge with linear size 80 nm to C-V dependence of source-base transition is considered in this work.

The simulation results show the capacitance in C-V dependence of transition have jumping behaviour started at bias voltage V_{jump}. Whereas V_{jump} depends on position of the localised charge relative to source (Fig. 2a). Position of the localised charge L is determined as distance between source and center of the charge (Fig. 1). Appreciable changes of capacitance are observed in the range of L from 75 nm up to 300 nm which covers approximately half of the distance between source and drain. In (Fig. 2b), C-V dependence for L = 300 nm is shown with higher resolution.

In order to determine the jump voltage V_{jump}, it is expedient to calculate the derivative of the change of the capacitance with respect to the bias voltage V_{bias} d(ΔC)/dV. In the dependence d(ΔC)/dV vs. V_{bias} the V_{jump} correspond to maximum of d(ΔC)/dV. Simulation results for different L shows that V_{jump} strongly depends on position of the charge bit (Fig. 3) and that V_{jump} monotonously decreased by increasing the distance L.

It is evident that capacitance changes at trapping the localised

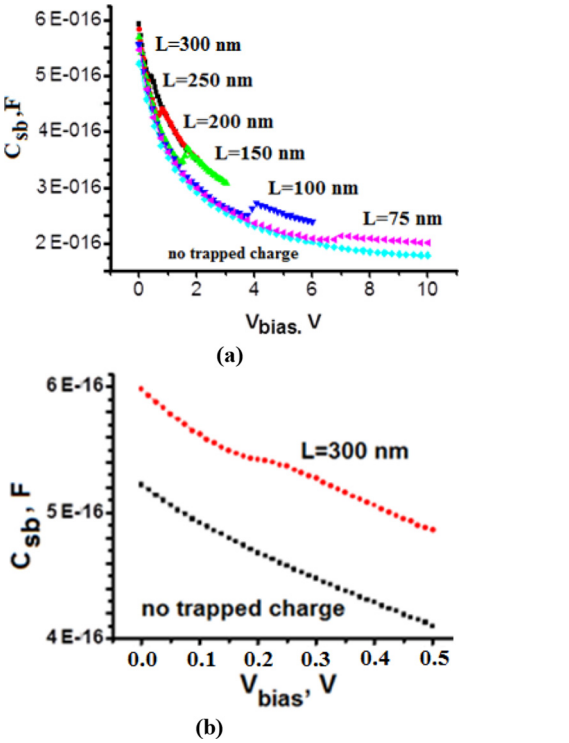

Fig. 2. (a) C-V dependence of the source-base transition without and with localised charge embedded in silicon nitride layer of MNOSFET on the different distance L from the source. (b) C-V dependence of the source-base transition without and with localised charge embedded in silicon nitride layer of MNOSFET on the distance L = 300 nm from the source.

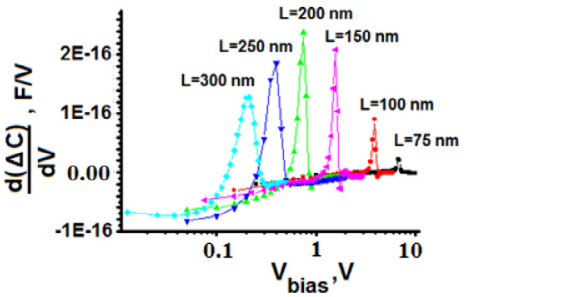

Fig. 3. d(ΔC)/dV for different L of the embedded localised charge.

charge in nitride layer is linked with changes of the carrier distribution in semiconductor base is caused by trapped charges. The change of the carrier distribution results due to the change in the width of depletion layer which consequently changes the capacitance of the source-base transition. Simulated V_{jump} − L dependence can be used to read the charge bit or to determine the position of localised charge trapped in silicon nitride layer of MNOSFET.

In embedding the localised charge, the changes of carrier distribution is mainly observed at depth no more than 300 nm. The analysis shows that the capacitance jump (Fig. 2a) is observed at trapping of the localised charge at bias voltage is caused by appropriate changing of carrier distribution near semiconductor surface. In Fig. 4, it is shown that the transition borders in base side appropriate to bias voltage near V_{jump} and L = 200 nm. Transition border is determined as geometric set of points in base at which concentrations of electrons and holes are equal. At the insertion in Fig. 4 the C-V dependence for L = 200 nm is shown with V_{jump} equals to 0.75 V. Transition borders are appropriate to cases with bias voltages in range between 0.4 and 1.1 V which captures the jump voltage 0.75 V. If the transition capacitance is considered in a flat capacitor approach, the capacitance should decrease

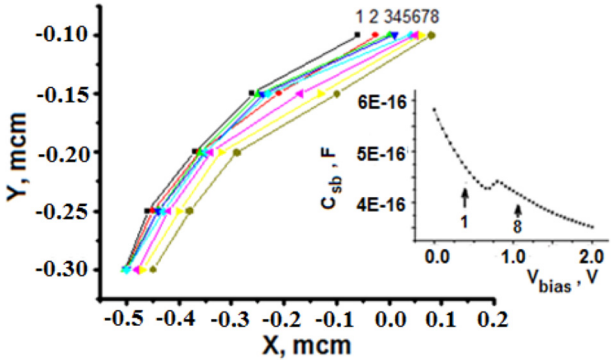

Fig. 4. Transition borders in base side at bias voltages between 0.4 and 1.1 V: 1–0.4 V, 2–0.5 V, 3–0.6 V, 4–0.7 V, 5–0.8 V, 6–0.9 V, 7–1.0 V, 8–1.1 V. Insertion shows C-V dependence for source-base transition and it is indicated that jump area caused by the localised charge trapped in distance L = 200 nm from the source. X is counted from the centre of channel and Y is counted from the surface of semiconductor base (see Fig. 1).

with increase in bias voltage. The decrease of capacitance is linked with increase in the width of depletion layer. In Fig. 4 the increase of the width is reflected by displacing the transition border to the right. However, by increasing the bias voltages from 0.6 V up to 0.8 V, transition border at depth up to 200 nm is abnormally displaced to the left. Therefore at these bias voltages the width of depletion layer is decreased and the capacitance is increased as shown in Fig. 4 insertion. The results of this work can serve as the basis for developing a method nitride layer of MNOSFET.

In this letter, it is proposed to use sweep voltage instead of scanning tip which allows to ensure much higher speed of scanning.

Conclusion

A new method has been proposed where by changing the position of embedded localised charge in silicon nitride layer of MNOSFET, it is possible to manipulate carrier distribution near semiconductor surface. The results of this work can serve as the basis for developing an alternative method to identify position of the charge bit along channel, trapped in the nitride layer of MNOSFET. It allows to manipulate the width of lateral source-base (or drain-base) transition and as a consequence the capacitance of the transition. The main features of the influence of the charge bit to C-V dependence of the lateral transition is the jump of capacitance at defined bias voltage V_{jump}. This effect can be used to read the bit information stored in the form of localised charge embedded in silicon nitride of MNOSFET, scanning by bias voltage. At considered MNOSFET parameters proposed in this method, it is possible to identify the position of the charge. We envisage number of applications based on this method including but not limited to the study of surface morphology of various matters and building microcircuits on computer chips.

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References

[1] Iwamura S, Nishida Y, Hashimoto K. Rotating MNOS disk memory device. IEEE Trans Electron Dev 1981;28(7):854–60.
[2] Barrett RC, Quate CF. Charge storage in a nitride oxide silicon medium by scanning capacitance microscopy. J Appl Phys 1991;70(5):2725–33. https://doi.org/10.1063/1.349388.
[3] Girard P. Electrostatic force microscopy: principles and some applications to semiconductors. Nanotechnology 2001;12(4):485–90.
[4] Shi H, Hong S, Moon J, Jeon JU. Read/write mechanisms and data storage system using atomic force microscopy and mems technology. Ultramicroscopy 2002;91(1–4):103–10.
[5] Atamuratov AE, et al. Influence of the field of the Built_in oxide charge on the lateral C-V dependence of the MOSFET. Dokl Phys 2010;55(2):52–4.
[6] Atamuratov AE, et al. The lateral capacitance of nanometer MNOSFET with a single charge trapped in oxide layer or at SiO_2-Si_3N_4 interface. Nanosystems 2015;6(6):837–42.