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Abstract: This paper presents a new topology of single phase Cascaded Multilevel Inverter (CMLI). The proposed topology offers an optimised DC source utilisation, reduced switch count and curtailment of active switches in the conduction path for minimising power losses. It can produce almost twice the number of output voltage steps in comparison to the Cascaded H-bridge, hence named Level-doubling architecture, and can be operated as both symmetric and asymmetric CMLI. Identical modules of proposed CMLI precludes requirement of variety of semiconductors and provides ease for spare management. Modular design also facilitates mass production and enhances system reliability. Furthermore, the proposed topology can be easily extended to High Voltage (HV) applications. The proposed design is tested for its practicability by simulations in MATLAB/Simulink and results are verified by experimental set up of a scaled prototype single-phase model.

1. Introduction

In recent years, there has been tremendous interest in the development of new structures for Multilevel Inverter (MLI). The primary aim of these efforts is to minimise inverter hardware and enhancement of power quality [1]. Reduction in component count directly influences the inverter efficiency, as few semiconductors (Insulated Gate Bipolar Transistor (IGBTs)) means small power loss in terms of both on-state and switching power losses. Historically, MLI was introduced to cope with the difficulty of designing conventional 2-level inverters for Medium Voltage (MV) (more than 1kV e.g., 2.3 kV, 3.3 kV, 4.16kV, 6kV and 6.6 kV) and high-power applications due to limited voltage and power ratings of available semiconductors [2,3].

Some basic topologies of MLI are termed as Diode Clamped (DCMLI), Flying Capacitor (FCMLI) and Cascaded (CMLI) [4]. The main advantage of DCMLI is that it requires only one dc input source, and through a string of capacitors and clamping diodes, large number of voltage steps/levels are synthesised to form an output voltage close to sine wave. By doing so, a single dc source is optimally utilised in DCMLI. However, large number of capacitors and clamping diodes along with semiconductor switches increases the cost and lowers down the efficiency. Despite that, DCMLI is industry standard for MV AC Motor drives [5,6] mainly due to its single dc source requirement. On the other hand, CMLI has least components count but it works only with multiple dc sources. An interesting feature of CMLI is that it can be formed by variety of structures. Therefore large number of topologies for CMLI have been presented in recent years focusing on reduction of semiconductors [7]. However less attention has been given to reduce input dc sources. It is noteworthy that these expensive dc sources are usually in the form of dc batteries, photovoltaic (PV) arrays, fuel cells, or multi-winding transformers with rectifiers.

Another advantage of CMLI is its modularity of structure, which provides fault tolerant operation. Therefore, any faulty module can be quickly bypassed and later replaced with spare modules. This ensures service continuity and minimises production down time. Spare management becomes easy if all modules are symmetric or identical i.e.,

of similar structure containing equally rated IGBTs. Moreover, when all input dc sources are also equal in terms of their voltage magnitude, it is customary to term it as symmetric MLI. In symmetric CMLI, there are as many input dc sources required as the number of steps per quarter cycle of inverter output voltage. For achieving high power quality (less harmonic distortion), greater number of levels must be formed, which in turn increases the number of dc sources. Similarly, asymmetric structure in which dc sources are of unequal magnitudes, such as binary or trinary CMLI does resolve this issue and minimises the number of dc sources but it introduces variety of semiconductor ratings, unequal dc sources magnitudes and unequal power sharing among the sources. This also requires complex charge balancing schemes [8]. In this way, advantages of symmetric structure are lost and it poses problems for stock management of variety of IGBTs and dc sources. This approach does not support customer requirement who would like to arrange components spares of one type only. Besides these conventional topologies, many hybrid topologies, which are essentially the combination of conventional topologies, have also been proposed for performance improvement of MLI [9-11].

In view of advantages of symmetric CMLI, this paper proposes new structures for a single phase nearly-symmetric CMLI, which requires less hardware components in comparison to the conventional Cascaded H-bridge (CHB) and many other topologies. It significantly minimises the number of input dc sources, while maintaining the benefits of symmetric CMLI such as modularity, reliability, simple control, and supportive structure for easy stock management.

The paper is organised as follows: section-2 gives an account of basic MLI structures and some recently reported topologies; section-3 presents proposed CMLI structures, their algorithms, and working principle is explained in this section. In section-4, a comparative study of the proposed inverter with CHB and some recently proposed topologies is presented, while section-5 presents simulation and hardware results for design validation of proposed inverter.

2. Existing CMLI Topologies

Since inception of CHB topology, design aspects of MLIs have been thoroughly investigated. Over the years, there have been large contributions by inverter designers towards bringing improvements in MLI designs, especially in cascaded topology [12-21]. Many of the presented cascaded topologies have their basic structure based on half-bridge cells. For example, in [12] cascaded half bridge structure has been proposed for level generation and a full bridge inverter for polarity reversal. In [17], this structure is extended for HV applications. However, this topology places switches of every module in the path of current flow, and therefore conduction power loss increases in direct proportion to the number of cascaded modules. In [15] the architecture has been modified in level generator by proposing IGBT-diode combination. This led to reduction in driver circuitry but still the number of switches in the conduction path is on higher side. Moreover, voltage spikes distort output levels when power is delivered to an inductive load. Topology proposed in [16] does minimise switch count but dc sources must be arranged alternately with opposite polarity. This brings complexity in structure for manufacturing. Moreover, replacement of defective modules may be erroneous. It also suffers from the presence of large number of switches in the conduction path, and therefore puts greater cooling requirement for the inverter. Many topologies, such as proposed in this paper employ bidirectional switches with the capability to block voltages in both directions. Topology proposed in [18] employs both unidirectional and bi-directional switches for power flow from serially connected dc sources. This structure reduces the total number of conducting switches at any instant, however topology proposed in this paper would result this count even lesser. To minimise the number of input dc sources, asymmetric MLI (ACMLI) topologies have also been presented. However, asymmetric structure has unequal power sharing among input dc sources. Therefore, in an asymmetric structure the number of varieties of dc sources should be kept minimum.

Literature review indicates that MLI technology has witnessed remarkable developments in the last two decades. However, there is still an interest in optimising this technology. One way to achieve this is through hybridisation to overcome their shortcomings and making them more suitable to specific applications. In this paper, a derived topology of CMLI with minimum variety is proposed, which is close to symmetric structure to avail benefits of symmetry. In addition, the proposed structure provides reduced switch count, minimises number of dc sources, and reduces the maximum number of conducting switches at any instant.

3. Proposed cascaded inverter topology

3.1. Architecture of proposed MLI

The basic architecture is developed in two stages: the level generating stage, where input dc sources are cascaded via semiconductors, and the load side H-bridge, which is used for polarity reversal (see Fig. 1). For single phase inverter of basic architecture, $n - 1$ bidirectional switches are required. An IGBT with anti-parallel diode provides bidirectional current flow but it cannot block voltage in both directions.
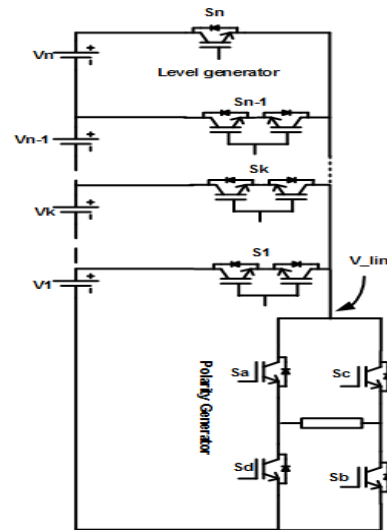

Fig.1 *Basic architecture*

For instance, if all switches in Fig.1 are single IGBTs with anti-parallel diode, and when switch S_2 is turned on, then voltage $V_1 + V_2$ will appear as dc link voltage and forward bias the anti-parallel diode of lower stage switch S_1, thus causing a short circuit across V_2. Therefore, switches S_1 to S_{n-1} must be able to block voltage in both directions. Hence this architecture requires bidirectional switches in stage1 to stage $n - 1$. However, in the n_{th} stage a unidirectional switch can be used since there is no upper stage source for it. In this regard, the basic architecture has one less IGBT than the topology proposed in [19]. A bidirectional switch can be formed with two IGBTs in common emitter configuration with their gates connected together, as has been used in earlier topologies as well [14], [18]. The power section contains an H-bridge to deliver ac power to the load. It is also used to produce 0-level in the output multilevel waveform.

For symmetric inverter, the input dc voltage magnitudes, and the number of output levels are given by (1) and (2)

$$V_i = V_{dc} \quad ; i = 1,2..n \qquad (1)$$
$$N_{step} = 2n + 1 \qquad (2)$$

In the present structure of Fig.1, the MLI can work only as symmetric MLI with fewer output levels. However, a structural change can enhance the output levels. For this purpose, two IGBTs of bidirectional switch S_1 are relocated such that one of them (S_{1c}) is used to connect, and the other one (S_{1b}) to bypass the first dc source (see Fig.2).
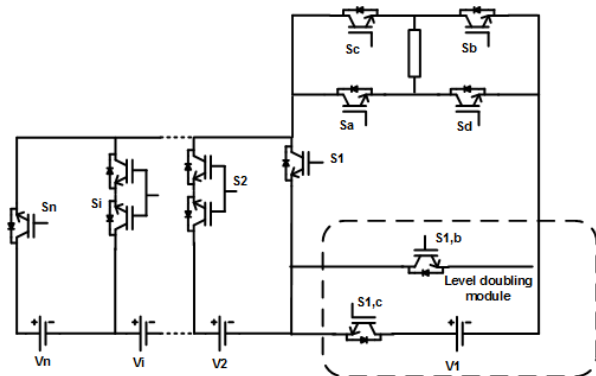

Fig.2 *Proposed level doubling architecture*

Therefore, this reorientation of switches forms a half-bridge cell within the structure. As found in the literature, such as [9,13], the level-enhancement to some basic topology is achieved by adding a half-bridge cell which requires two additional IGBTs and an extra voltage source. However, structural modification precluded the necessity of any extra half-bridge cell; rather the hardware is only reconfigured for level-enhancement. To achieve level-doubling, the first dc source voltage magnitude is also adjusted in a definite relation with the other dc sources. However, one IGBT (S_1) is also required to be placed for bypassing the sub-multilevel stage V_2 to V_n. The switch count therefore remains equal to as in [19] but with definite value additions as described is Section 3.1.2. With this configuration, the proposed architecture can function in both symmetric and asymmetric modes.

3.1.1 Parameters: To achieve higher power-quality the inverter output levels must be increased. So, for level doubling (LD) proposed architecture, the dc source magnitudes are established by equation (3)

$$V_i = \begin{cases} 2^{i-1}V_{dc} \; ; \; i = 1 \\ 2^{(i-j)}V_{dc} \; ; i = 2,3,4 \dots, j = i - 1 \end{cases} \quad (3)$$

The dc link voltage established by the level generator is given by (4)

$$V_{link} = \sum_{i=1,2\dots}^{n} V_i \quad (4)$$

Whereas the maximum output voltage magnitude expressed as a function of dc sources $'n'$ is given by (5)

$$V_{0,max} = (2n - 1)V_{dc} \quad (5)$$

The blocking voltage rating V_B of IGBTs plays important role in the overall cost of inverter. For the proposed architecture, the blocking voltage of base unit IGBTs is limited to V_{dc}. The maximum blocking voltage across IGBTs in sub-multilevel lower-half section switches $(\frac{n-1}{2})_l$ is obtained when maximum link voltage is established by turning on switch $S_{1,c}$ and S_n; while for upper-half section switches $(\frac{n-1}{2})_u$, the condition is that $S_{1,c}$ and S_1 are on, and dc link voltage is equal to V_{dc}. It turns out that switch pairs of identical blocking voltages exist in the sub-multilevel unit, such as

$$\begin{aligned} V_{B,S1} &= V_{B,Sn} = 2(n-1)V_{dc} \\ V_{B,S2} &= V_{B,Sn-1} = 2(n-2)V_{dc} \\ V_{B,S3} &= V_{B,Sn-2} = 2(n-3)V_{dc} \\ \vdots \quad & \quad \vdots \quad \quad \vdots \\ \vdots \quad & \quad \vdots \quad \quad \vdots \\ V_{B,\left(\frac{n-1}{2}\right)_{l,j}} &= V_{B,\left(\frac{n-1}{2}\right)_{u,k}}; \\ j &= 1,2,3 \dots. \quad k = n, n-1, n-2, \dots. \quad (6) \end{aligned}$$

IGBTs of polarity generator H-bridge must bear a voltage stress of maximum dc link voltage. The blocking voltage of polarity generator switches is given by (7)

$$V_{B, Polarity} = 4(2n - 1)V_{dc} \quad (7)$$

The total blocking voltage of inverter is, therefore obtained as (8).

TBV

$$= \begin{cases} 3(3n-1)V_{dc} + 4 \sum_{j=1,2,3}^{\frac{n-1}{2}} (n-j)V_{dc} \; ; if \; n \; is \; odd \\ 2(4n-1)V_{dc} + 4 \sum_{j=1,2,3}^{n/2} (n-j)V_{dc} \; ; \; if \; n \; is \; even \end{cases} \quad (8)$$

To minimise variety of switches of different blocking voltages in the sub-multilevel section, it is recommended to keep $'n'$ to a small value. For example, if $= 5$, there will be 2 switch pairs in the range of 1:2 voltage ratings ratio and the variety is limited to 2. Interestingly, the cost of an IGBT of double-voltage and a current rating is even lesser than half-voltage rated IGBT [21]. It follows that IGBT S_n rating can be applied to all switches in the sub-multilevel stages when n is kept small. Then the sub-multilevel section will also consist of identical switches. However, due to higher total blocking voltage rating, such deigns are suitable for low voltage, high power-quality applications as well [22]. Furthermore, the structure can be extended for high voltage applications as described in Sec.3.1.4.

For the proposed topology, the total number of output levels is related with the input dc sources 'n' as given in (9)

$$N_{steps} = 4n - 1 \quad (9)$$

Comparing (2) and (9), it is clear that the proposed architecture would provide almost double number of levels compared with the basic architecture and therefore, is the recommended design. It may be mentioned that the sub-multilevel topology presented in [19] can achieve level enhancement by increasing the cascaded stages or when several inverters are connected in series resulting in a cascaded expansion. However, in the proposed LD sub-multilevel topology this is achieved without resorting to cascaded expansion. Moreover, the proposed LD topology can also be placed in cascaded fashion to increase its voltage ratings to HV range.

Now it can be observed that with dc source magnitudes as calculated in (3), the LD topology produces output levels at discrete intervals. If the inverter has j stages of sub-multilevel module having n_j number of dc sources, and is in series with LD base module, then the number of levels N_{steps} produced by the inverter can also be calculated by (10)

$$N_{steps} = 4n_{j-1} + 7 \quad ; n_{j-1} = j - 1 \quad (10)$$

The number of IGBTs (taking one bidirectional switch equivalent to two IGBTs) is given by (11)

$$N_{IGBT} = 2n + 4 \quad (11)$$

Due to bidirectional switches, number of switches (and gate drivers) are less than the number of IGBTs as given by (12)

$$N_{dri.} = N_{sw.} = n + 6 \quad (12)$$

3

Table 1 Generalised switch states for proposed architecture shown in Fig.2

State (i)	$S_1 S_{1b} S_{1c}$ $S_2 S_3 .. S_k ..$ $S_{n-1} S_n$	V_{link}	$S_a S_b$ $S_c S_d$	V_{out}
1	10100..0..00	V1	1010	0
2	10100..0..00	V1	1100	$+V_{dc}$
3	01010..0..00	V2	1100	$+2V_{dc}$
4	00110..0..00	V1+V2	1100	$+3V_{dc}$
5	0101..0..001	V1+V2+ V3	1100	$+4V_{dc}$
:	:	:	:	:
2n	10000..0..10	$\sum_{i=1}^{n} V_i$	1100	$+(2n-1)V_{dc}$
:	:	:	:	:
4n	10000..0..01	V1	0011	$-V_{dc}$
:	:	:	:	:
5n +1	10000..0..10	$\sum_{i=1}^{n} V_i$	0011	$-(2n-1)Vdc$

Table 2 Switch states for 11-level Inverter of Proposed MLI shown in Fig.3

State	Level	$S_1 S_{1b} S_{1c}$ $S_2 S_{13}$	$S_a S_b$ $S_c S_d$	V_{link}	V_{out}
1	0	10100	1010	V1	0
2	+1	10100	1100	V1	$+V_{dc}$
3	+2	01010	1100	V2	$+2V_{dc}$
4	+3	00110	1100	V1+V2	$+3V_{dc}$
5	+4	01011	1100	V2+V3	$+4V_{dc}$
6	+5	00101	1100	V1+V2+V3	$+5V_{dc}$
7 - 11	4 - 0	:	:	:	$+4V_{dc}..0$
12	−1	10100	0011	V1	$-V_{dc}$
13	−2	01010	0011	V2	$-2V_{dc}$
14	−3	00110	0011	V1+V2	$-3V_{dc}$
15	−4	01011	0011	V2+V3	$-4V_{dc}$
16	−5	00101	0011	V1+V2+V3	$-5V_{dc}$

Table-1 presents switch states of semiconductors to achieve maximum positive and negative levels for the proposed inverter with 'n' number of dc sources. Whereas switch 'ON/OFF' states are represented by '1' and '0' respectively.

3.1.2 Working principle: working modes are explained with the help of a single-phase inverter composed of a base unit and sub-multilevel module with a total of three cascaded sources (see Fig. 3). Table 1 is reconstructed as Table 2 by substituting n=3 and switch combinations for 11 levels are presented in it. In Fig. 3, the active switches and current path is shown in thick black lines. The inverter produces 0 output in mode-1 (see Fig. 3(a)), positive levels in mode-2 (Fig. 3 (b) and (c)), and negative levels in mode-3 (Fig. 3(d)). For generating '0' level, any level produced by level generator is nullified by switching either both upper or both lower switches of H-bridge (see Fig. 3(a)). As shown in Fig. 3(b), switch S_{1c}, S_1 are active for generation of positive level-1; Level 2 is produced by bypassing base module, and switches S_2 and S_{1b} conduct for this level (see Fig.3c). The polarity of these levels is determined by position of H-bridge switch pairs. Either switch pair $S_a S_b$ (mode-2) or $S_c S_d$ (mode-3) may be active at a time. Moreover, $S_a S_d$ and $S_b S_c$ cannot conduct simultaneously, and must be triggered by complimentary logic to avoid short circuit across dc link. Hence 11 levels can be generated by following the switch combinations presented in Table 2.

3.1.3 Voltage balancing of dc sources: As the duty cycle of all source-connecting switches is not equal, the input dc sources in any MLI experience unequal charge-discharge periods. This leads to quicker discharge for the source which is on for greater time than the other sources, and voltage magnitudes of dc sources cannot maintain their stated values. This voltage unbalance problem is classically addressed by switching pattern swapping which requires redundant states[8].These redundant switch states are available when proposed MLI works in symmetric mode i.e., when all dc sources are of equal magnitudes V_{dc} and voltage balancing can be achieved. In the level-doubling mode, the proposed MLI however has limited redundant switch states but has redundancy in three-phase configuration. Therefore, for single phase, the input sources should be regulated dc sources. For this purpose, a possible configuration is to charge dc batteries through PV modules and Maximum Power Point Tracking (MPPT) charge controller. However, for unregulated dc sources, some redundancies can also be introduced for voltage balancing, if the LD module (see Fig.2) is formed by an H-bridge. But this approach will increase the switch count and therefore, as a result there is a trade-off between voltage balancing and switch count.

3.1.4 Extension of Topology for high voltage applications: As stated, the proposed topology in the present form is more
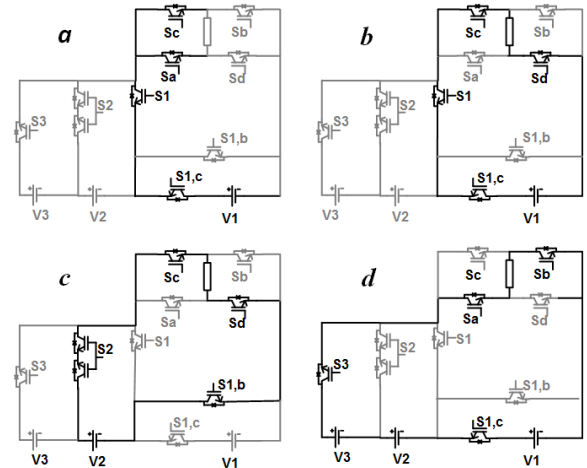

Fig. 3 *Working modes of 11-level inverter LD architecture and power flow shown in dark black line for*
a Mode-1,0 level
b Mode 2, +Vdc
c Mode 2, +2Vdc
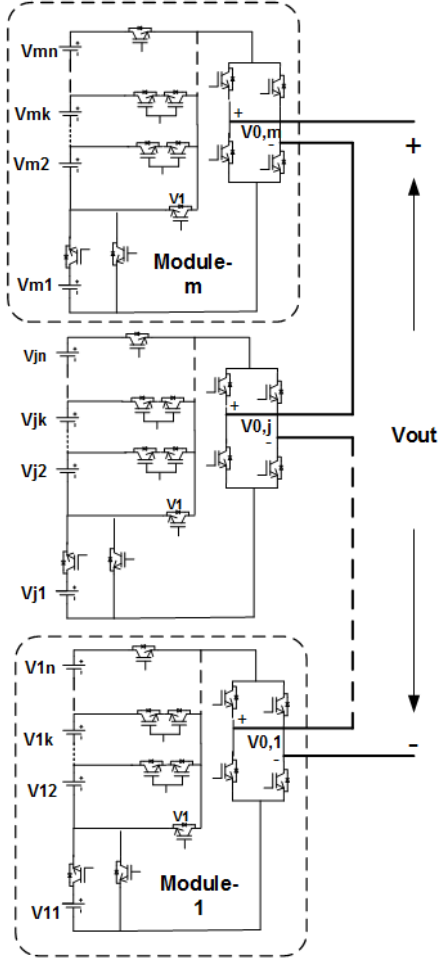*d* Mode 3, -5Vdc

Fig. 4 *Cascaded expansion of proposed topology for HV applications*

suitable for low voltage, high power-quality applications. For applications such as distributed generation, microgrid interface and MV ac motor drives, the converter voltage rating must be enhanced. By utilising cascaded expansion approach, the proposed topology can be made suitable for MV and HV applications as well. Fig.4 elaborates the concept in which proposed MLI shown in Fig.2 has been placed as a single module and several such modules are serially connected to extend converter voltage rating. In addition, redundant switch states are also available in this cascaded expansion. For achieving higher number of levels and output voltage magnitude, following Algorithms are proposed:

Algo-1: For all modules to be identical, the dc source voltage magnitudes, number of levels and total output voltage is established by (13), (14) and (15) respectively.

$$V_{1,j} = V_{dc} ; \quad V_{2,j} = V_{kj} = 2V_{dc} ;$$
$$j = 1,2..m \quad ; k = 2,3,..n \qquad (13)$$
$$N_{steps} = 4mn - 2m + 1 \qquad (14)$$
$$V_{0,max} = m(2n - 1)V_{dc} \qquad (15)$$

This proposed cascaded expansion is compared with the topology presented in [19]. For example, considering a configuration of three cascaded sub-modules ($m = 3$), each

having three sources ($n = 3$), then Algo-1 would produce 31 output levels for the Proposed topology. The topology presented in [19] being symmetric must have all dc sources of equal magnitude in a sub-module. Therefore, to apply Algo-1 i.e., for all identical sub-modules, the dc source magnitudes are given as $V_{im} = V_{dc}$, i=1,2,3 and m=1,2,3 then it follows the topology [19] would be able to produce only 19 levels.

Algo-2: In this configuration, all modules except the first module are similar. Module-2 to Module-m has dc sources of double magnitude than the sources of Module-1. Thus, a partially symmetric inverter structure is obtained by following set of equations:

$$V_{1,1} = V_{dc} ; \quad V_{k1} = 2V_{dc} \quad ; k = 2,3,..n \qquad (16)$$
$$V_{1j} = 2 V_{1,1}; \quad V_{kj} = 2V_{k1} ; j = 2,3 ...m ;$$
$$k = 2,3,..n \qquad (17)$$

$$N_{steps} = 8mn - 4m - 4n + 3 \qquad (18)$$
$$V_{0,max} = (2m - 1)(2n - 1)V_{dc} \qquad (19)$$

Algo-3: Another possible configuration is to double the voltage magnitude of k_{th} source of j_{th} module with respect to its preceding module. Thus, the inverter has asymmetric structure.

$$V_{1,1} = V_{dc} ; \quad V_{k1} = 2V_{dc} \quad ; k = 2,3,..n \qquad (20)$$
$$V_{kj} = 2V_{ki} ; k = 1,2,..n ; j = 2,..m; \quad i = j - 1 \qquad (21)$$

$$N_{steps} = (4n - 1) + \sum_{i=1}^{m-1} 2^i(4n - 2) \qquad (22)$$
$$V_{0,max} = (2^m - 1)(2n - 1)V_{dc} \qquad (23)$$

Hence, it may be concluded that for a configuration of three modules ($m = 3$) and three sources per module ($n = 3$), Algo-3 will generate the highest converter rating of $35V_{dc}$ with 71 levels because of its asymmetric configuration; Algo-2 will produce $25V_{dc}$ with 51 levels, and with Algo-1 the converter rating will extend to $15V_{dc}$, with 31 levels. However, Algo-2 will yield almost symmetric converter (providing modularity) of extended voltage rating without increasing the semiconductor ratings, and therefore it is the preferred configuration for HV applications.

4. Comparative analysis of proposed and existing topologies

The significance of any design could be gauged only by a relative performance comparison. Therefore, to ascertain the effectiveness of a topology, various parameters related to cost, efficiency and power quality are usually considered. Fig. 5 demonstrates such comparison of proposed inverter architecture with existing LD and some symmetric topologies. Comparative state of various parameters such as required number of IGBTs (N_{IGBT}), number of dc sources (N_{DC}), and number of drivers ($N_{drivers}$), versus output levels generated by the inverter (N_{steps}) are presented in a graphical form in this Figure.
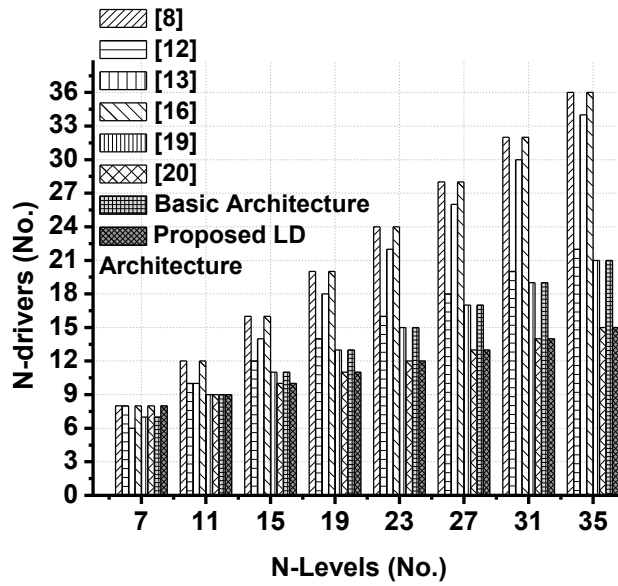
As shown in Fig.5(a), the required number of IGBTs for producing a given number of levels is minimum for proposed LD architecture compared with other LD topologies [8,13,16,19,20]. It may be mentioned that
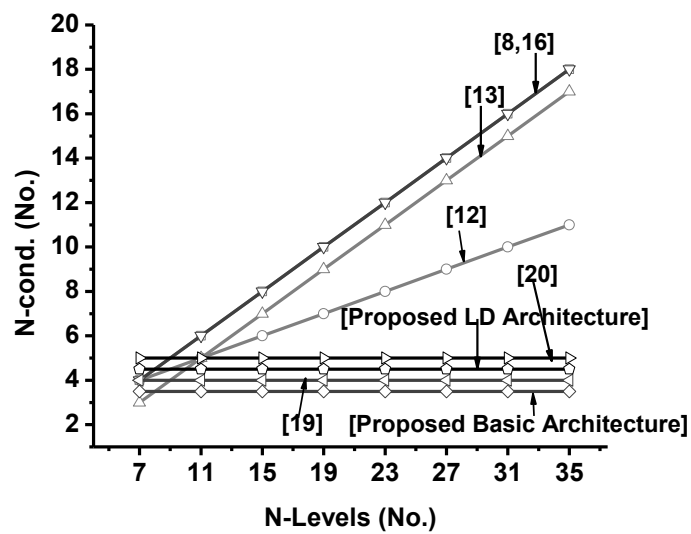
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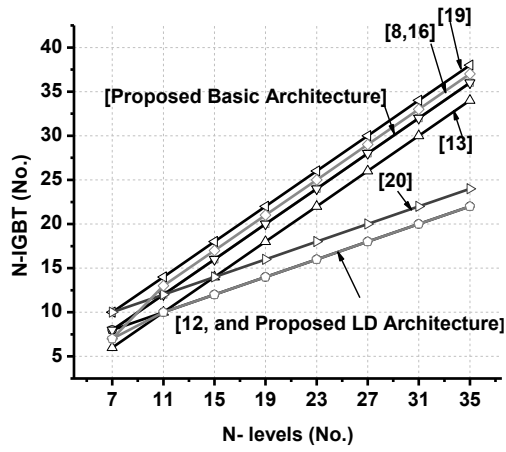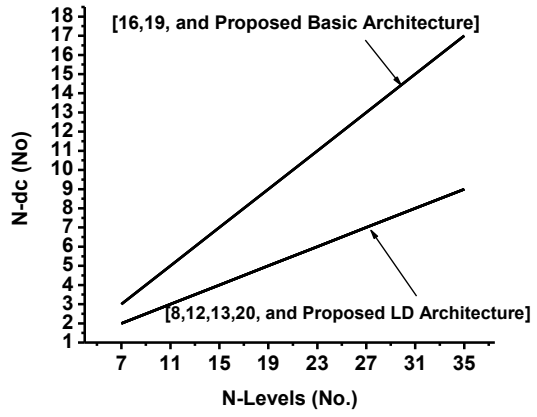
Fig.5 *Comparison of components requirement versus output levels*
a IGBT switches
b Gate drivers
c DC sources requirement
d Max. conducting devices Versus cascaded sources

topology presented in [12] if used as LD topology would also require equal number of IGBTs, but greater number of gate drivers, which incurs higher conduction losses. Fig. 5(b) shows minimum requirement of gate drivers (and number of switches) for the proposed LD topology than other topologies. It may be mentioned that topology presented in [20] has equal number of gate drivers but greater number of IGBTs are required for it, and it has higher conduction losses than proposed LD topology (see Fig. 5(c)). Fig. 5(d) manifests minimum requirements of dc sources for proposed LD architecture in comparison with Basic Architecture and some symmetric topologies such as given in [16,19]. Hence, for generating specific number of output levels, other topologies would require greater number of semiconductors, gate drivers and conducting switches compared to the proposed design. The proposed LD topology can therefore be said to have combined several superior attributes in a single package.

Another comparison can be made with respect to voltage stresses borne by each component. By considering a case of four cascaded sources ($n = 4$) for the proposed LD Architecture, with voltage magnitudes ratio of 1:2 ($V_1 = \frac{1}{2}V_{dc}$ and $V_2 = V_3 = V_4 = 1V_{dc}$, the maximum blocking voltage of individual switches then turns out to be: $V_{B,S1c} = V_{B,S1b} = \frac{1}{2}V_{dc}$; $V_{BS1} = V_{B,S4} = 3V_{dc}$; $V_{B,S2} = V_{B,S3} = 2V_{dc}$ and each polarity generator switch bears $3.5V_{dc}$. This makes a total of TBV value of $25V_{dc}$. If we compare the level-doubling (asymmetric) topology presented in [20] with the same voltage source magnitudes will have higher total standing voltage of $35V_{dc}$ due to two extra switches placed in the H-bridge. On the other hand, in symmetric sub-multilevel inverter presented in [19] with equal dc source magnitudes (V_1 to $V_4 = 1V_{dc}$), the total voltage stress will be a little higher at the value of $26V_{dc}$ but it can produce about 50% less levels. However, CHB based LD topology [13] results in minimum value of TBV i.e., $13V_{dc}$. This is an advantage of classical CHB, but it suffers due to the highest switch count.

In accordance with eq. (3) and (8), it may be noted that proposed LD Architecture would not produce all even and odd levels in succession. However, it should not be considered a demerit as reduced component count and higher number of levels generated by the topology will improve power quality of inverter at reduced cost. This advantage therefore offsets any limitation of the proposed topology. Moreover, the proposed LD architecture achieves double number of levels by addition of a single IGBT in the basic architecture, while this level doubling is achieved at the expense of two IGBTs and an extra voltage source in topology proposed in [13]. In some topologies, such as [9], higher number of steps are formed by source voltage distribution in capacitors, which improves the power quality but capacitors do not provide active power, and as a result inverter power rating does not enhance. However, the topology presented here does not require capacitors at all; rather separate dc sources are used to improve both power quality and inverter power rating. Fig. 5(d) shows a comparison between the proposed Basic Architecture and some symmetric topologies [16,19] with the proposed LD topology with respect to the requirement of dc sources for producing a specific number of levels. Like other level-doubling topologies, the proposed LD architecture also employs much lesser number of dc sources to produce same

number of levels. Hence, it can be said that dc sources are optimally utilised with the proposed LD Architecture. Another important feature of proposed topology is the count of maximum number of conducting switches at any instant. This parameter has great influence on average power loss and efficiency of inverter. In the proposed Basic- Architecture the maximum number of conducting switches varies between 3 to 4, and in proposed LD architecture, the maximum number of conducting switches varies between 4 and 5 (as described in the following section), see Fig. 5(c), irrespective of the number of cascaded stages. Hence, on-state power losses remain constant even if the inverter is designed for large number of cascaded stages.

4.1 Power loss and efficiency calculations

For efficiency calculation, power loss in semiconductors during ON-state and switching transition must be determined. This is done in the following sections for level and polarity generator. For the sake of comparison, these losses are also calculated for conventional CHB topology. In the proposed LD architecture of Fig. 2, according to switch states of Table-1, only one switch in the sub-multilevel cell is required to be ON at any instant, irrespective of the number of cascaded stages. For a conducting bidirectional switch (S_2 or S_3 ... or S_{n-1}), two devices are considered for loss calculations. In the base unit of half-bridge cell, only one switch (S_{1b} or S_{1c})is ON at any instant. Thus, at maximum, 3 devices can conduct simultaneously in the level generating part. The polarity generator switch pair (S_aS_b or S_cS_d) are required to be ON at any instant. This accounts for, at most, 5 devices to be in conducting state at any instant. It may be pointed out that in several other topologies such as proposed in [8,12,13,15,16], the current must flow through at least one device in each cascaded stage in the level generating part. Therefore, in these topologies conduction power losses increase linearly with the number of cascaded sources. Using reference [18], the power loss is calculated in the next section.

4.1.1 Conduction loss in proposed MLI:
The instantaneous on-state power loss is calculated as given in (24)

$$P_{cond} = V_{on}(t).i(t) \qquad (24)$$

Where $V_{on}(t)$ represents the on-state voltage drop across the device and $i(t)$ is the instantaneous current through it. The general expression for conduction loss through a transistor and a diode is given in (25) and (26)

$$P_{cond.T.}(t) = [V_{on,T} + R_T.i^\beta(t)].i(t) \quad (25)$$
$$P_{cond.,D}(t) = [V_{,onD} + R_D.i(t)].i(t) \quad (26)$$

In these equations, $V_{on,T}$, $V_{,onD}$ are on-state voltage drops across transistor and diode, which is typically less than 3 volts for IGBT. R_T and R_D represent equivalent resistances of transistor and diode respectively, β is a constant, which depends on transistor specification.

The average conduction power loss for a bidirectional switch is given by (27) (see at bottom of the next page). For inductive load, the current is assumed to be sinusoidal as expressed in (28) (see at the bottom), where I_m represents peak load current. In a unidirectional switch, transistor

conducts for the interval $\emptyset \leq wt \leq \pi + \emptyset$,while its anti-parallel diode conducts for $0 \leq wt \leq \emptyset$, where $\emptyset$ is the load impedance angle. Conduction power loss in a unidirectional switch is therefore given by (29) (see at the bottom). In the architecture shown in Fig. 2, the maximum number of conducting switches cannot be more than 5; including 3 unidirectional switches (one in level generator S_{1b} or S_{1c} ,and two in polarity generator $S_a S_b$ or $S_c S_d$) and one bidirectional switch (equivalent to two unidirectional switches S_2 or S_3 ... or S_{n-1}) in the level generator. Therefore, the maximum conduction power loss is calculated from eq. (30).

$$P_{c,max.} = 3P_{c,uni.} + 1P_{c,bid.} \qquad (30)$$

Since eq. (30) is independent of $'n'$, it follows that conduction power loss remains constant irrespective of the number of cascaded stages. This advantage is not available in various topologies, and therefore for proposed topology efficiency does not decrease when number of cascaded stages in sub-multilevel unit are increased. Therefore, cooling requirements of inverter do not increase when it is designed for higher levels.

4.1.2 Conduction power loss in conventional cascaded H-bridge topology: In conventional CHB topology, two unidirectional switches conduct in each cascaded cell. Therefore, for n-number of cascaded cells, the conduction power loss is given by eq. (31) (see at the bottom), which shows the conduction loss in classical cascaded H-bridge topology varies linearly with the number of cascaded cells $(2n)$ and causes much greater conduction losses and reduced

efficiency when it is designed for higher levels.

4.1.3 Switching power loss comparison: Switching power loss occurs in semiconductors during both turn-on and turn-off events. During these transitions, finite values of current and voltage-drop occurs across a switch causing loss of energy in the switch. Therefore, total switching power loss in the proposed multilevel inverter needs to be investigated. For calculation of switching losses, linear approximation for voltage and current transition is assumed. Turn-off is characterised by a delay time t_{off}, measured from the instant of removal of gate voltage, as V_{CE} persists for a while until V_{GE} falls completely. The switching power loss can be determined as a function of switching frequency, so that energy loss during IGBT turn-off and turn-on can be calculated by eq. (32) and (33) (see at the bottom), where V_T is the off-state voltage of IGBT. Thus, the switching power loss of K_{th} switch for a single On-OFF transition is given by (34)

$$P_{sw,k} = \left(E_{on,k} + E_{off,k}\right)f \qquad (34)$$

If a switch makes $N_{on,k}$ and $N_{off,k}$ transitions in a half cycle, then total switching power loss of the level generator switches is given in eq. (35)

$$P_{sw,L} = 2f \left(\sum_{k=1}^{N_{IGBT}} N_{on,k}E_{on,k} + \sum_{k=1}^{N_{IGBT}} N_{off,k}E_{off,k} \right) (35)$$

Each pair of IGBTs in the polarity generator H-bridge also turn-on and off once in each cycle. Therefore, switching power loss in H-bridge is given by (36).

$$P_{sw,H} = 2f\left(E_{on} + E_{off}\right) = \tfrac{1}{3}fIV_T\left(t_{on} + t_{off}\right) \quad (36)$$

$$P_{c,bid.} = \frac{1}{\pi} \int_0^\pi \left[V_{on,T} + R_T. i^\beta(t) + V_{on,D} + R_D. i(t)\right] i(t)\, d(\omega t)$$

$$P_{c,bid.} = \frac{2}{\pi} I_m \left(V_{on,T} + V_{on,D}\right) + \frac{R_D I_m^2}{2} + \frac{R_T I_m^{\beta+1}}{\pi} \int_0^\pi \sin^{\beta+1}(\omega t)\, d(\omega t) \qquad (27)$$

$$i(t) = I_m \sin(\omega t) \qquad (28)$$

$$P_{c,uni.} = \frac{1}{\pi} \left[\int_0^\emptyset \left[V_{on,D} + R_D. i(t)\right] + \int_\emptyset^\pi \left[V_{on,T} + R_T. i^\beta(t)\right] i(t)\, d(\omega t)\right.$$

$$P_{c,uni.} = \frac{1}{\pi} \left[V_{on,D}I_m(1 - \cos\emptyset) + \frac{R_D I_m^2}{4}(2\emptyset - \sin 2\emptyset) + V_{on,T}I_m(1 + \cos\emptyset)\right.$$

$$\left. + R_T I_m^{\beta+1} \int_\emptyset^\pi \sin^{\beta+1}(\omega t)\, d(\omega t)\right] \qquad (29)$$

$$P_{cond,CHB} = 2nP_{c,uni.} = \frac{2(n)}{\pi} \left[\begin{array}{c} V_D I_m(1 - \cos\emptyset) + \dfrac{R_D I_m^2}{4}(2\emptyset - \sin 2\emptyset) \\[2mm] + V_T I_m(1 + \cos\emptyset) + R_T I_m^{\beta+1} \displaystyle\int_\emptyset^\pi \sin^{\beta+1}(\omega t)\, d(\omega t) \end{array} \right] \qquad (31)$$

$$E_{off,sw} = \int_0^{t_{off}} v(t)\, i(t)\, dt = \int_0^{t_{off}} \left|\left(\frac{V_T}{t_{off}}t\right)\left(-\frac{(t - t_{off})}{t_{off}}\right)I\right| dt = \frac{IV_T}{6}t_{off} \qquad (32)$$

$$E_{ON,sw} = \int_0^{t_{on}} v(t)\, i(t)\, dt = \int_0^{t_{on}} \left|\left(\frac{V_T}{t_{on}}t\right)\left(-\frac{(t - t_{on})}{t_{on}}\right)I\right| dt = \frac{IV_T}{6}t_{on} \qquad (33)$$

Hence, total switching power loss in the inverter is calculated as (37)

$$P_{sw,} = P_{sw,L} + P_{sw,H} \qquad (37)$$

From (32) and (33), it can be observed that switching power loss depends on the blocking voltage (V_T) of switches also. In CHB the blocking voltage of each switch is limited to cell input voltage. This is the biggest advantage of CHB. For proposed topology, the approach to minimise blocking voltage and maintaining symmetry of module, as discussed in section 3.1.1, also become relevant in this context. Moreover, the proposed topology requires very few IGBTs as compared to CHB, and therefore despite increase of switching losses due to higher blocking voltages, small switch count subsides this limitation.

5. Design validation

To validate proper functioning of proposed topology, two approaches have been used in this paper. In the first approach, working principle is authenticated by simulations in *MATLAB/Simulink*, followed by measurements taken on hardware setup.

5.1 Simulation results

Numerous techniques have been developed for generating multilevel waveforms of low harmonic contents [23]. Among these techniques, fundamental switching frequency technique is recommended for the proposed topology. It may be mentioned that other switching techniques, such as Multicarrier Pulse Width Modulation (MC PWM), Space Vector Modulation (SVM), and Nearest Level Modulation are also helpful in minimising undesirable high frequency content in inverter output, termed as harmonics. For the same purpose, at fundamental frequency, selective harmonic elimination (SHE) algorithm may be applied to determine the accurate switching angles which would remove some of the low order harmonics [24]. Fundamental switching frequency method is based on the fact that an N-level stepped wave form can be synthesised by (N-1) phase shifted square waves. The phase angles of these waves play very important role in the generation of harmonics. Taking advantage of quarter wave symmetry of sine wave, these switching angles are required to be calculated only for the first quarter of the cycle.

The instantaneous voltage of synthesised multilevel output is given by (38), where k represents the number of
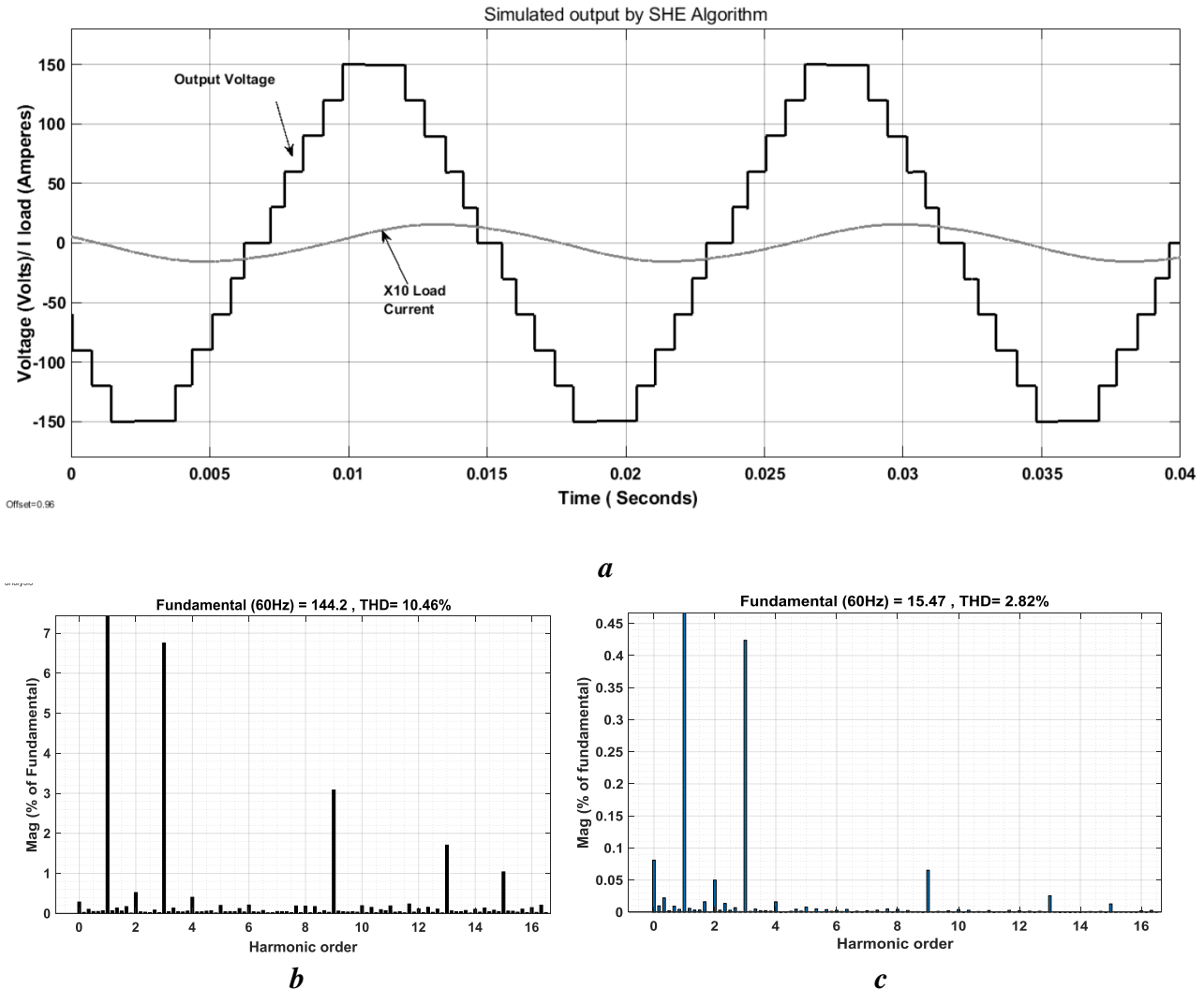

a

b

c

Fig. 6 *Simulation results using SHE Algorithm*
a 11-level output voltage and load current
b Load voltage and its THD analysis
c Load current and its THD analysis

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steps and thus the switching angles, and 'h' represents the order of harmonics.

$$V_0(\omega t) = \frac{4V_{dc}}{\pi} \sum_{h=1,3..}^{\infty} \sum_{i=1}^{k} Cos\,(h\,Cos\,\alpha_i) \frac{\sin h\omega t}{h} \quad (38)$$

One measure of power quality of any inverter is the Total Harmonic Distortion (THD) which is given by the ratio of root mean square (RMS) value of all harmonics to the fundamental component (V_1), as given by (39)

$$\%THD = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \cdots}}{V_1} \times 100 \quad (39)$$

To generate an 11-level output through proposed LD architecture, three dc sources of 30V, 60V, 60V are used in the Simulink model. The single-phase inverter architecture shown in Fig. 3 is simulated in *MATLAB/Simulink* environment with highly inductive load (R=55Ω, L=200mH, Ø=54°, P. F = 0.58 lagging). For synthesising multilevel output, the phase angles of shifted square waves are calculated iteratively in Mathcad software. It may be mentioned that for five levels (excluding 0 level) quarter wave,

five switching angles are required to be determined, which are found as $\alpha_1 = 6.36°; \alpha_2 = 15.06°; \alpha_3 = 23.54°; \alpha_4 = 37.24°$ and $\alpha_{5=} 58.15°$ for modulation index of 0.85. Fig.6 shows the simulation results for 11 level output voltage and load current (amplified by a factor of 10 for better visibility). It may be observed that the current waveform is lagging. The power quality of the output voltage and current is evaluated by determining voltage THD and current THD values using FFT analysis in Powergui. Simulation results show voltage THD of 10.46%, fundamental voltage magnitude (V_1, rms) of 102 volts, while current THD value is found to be 3.13%. As can be seen, the load current is almost a pure sine wave because load inductance works as low pass filter and greatly suppresses the high order harmonics. To substantiate this finding, voltage and current THD values are obtained with different loads of various power factors ranging between 0 (pure inductive) to 1.0 (pure resistive). Table 3 lists the simulation results, which shows that the current THD values are decreased when load inductance is increased. Voltage THD, on the other hand, remains constant and is independent of the load power factor. Hence, to decrease voltage THD, the number of output levels must be increased.
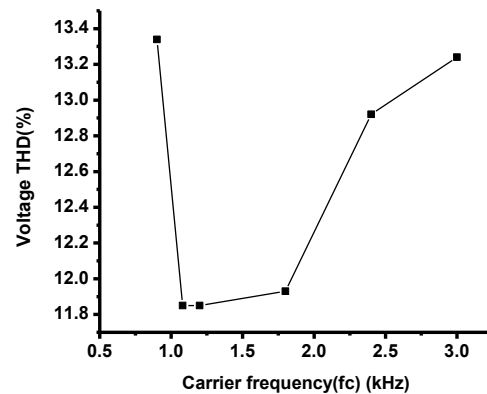
To compare the power quality obtained by a high frequency PWM technique, the simulation is again performed
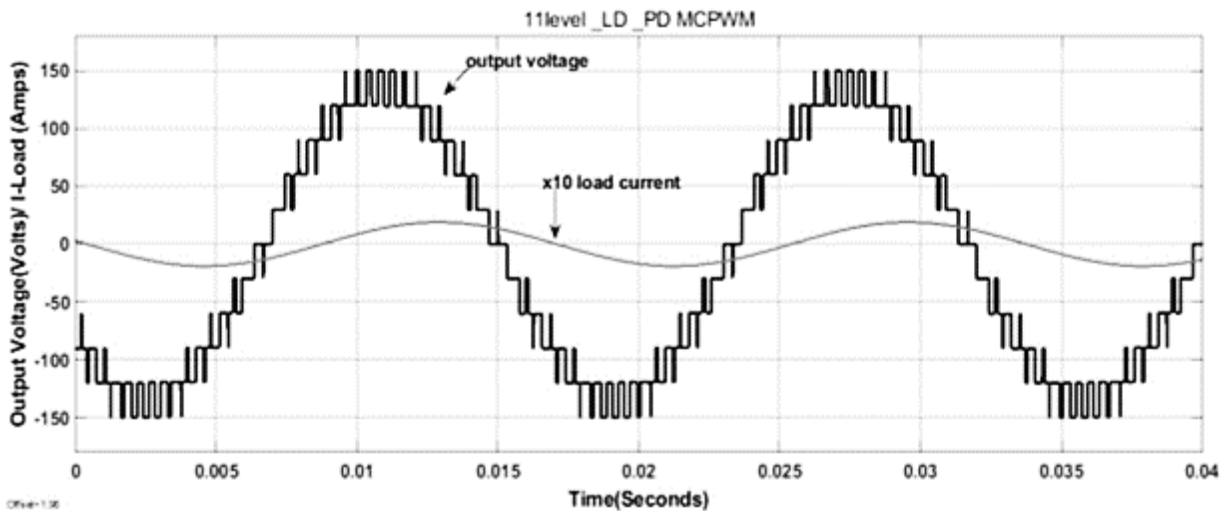
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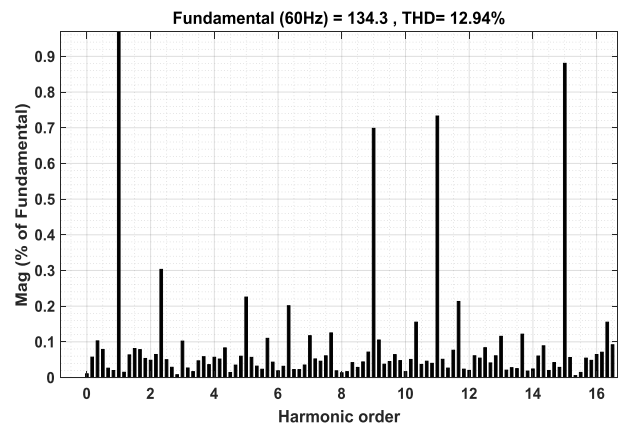
b

c

Fig. 7 *Simulation results using PDMCPWM Method*
a 11-level PWM output voltage and load current
b Load voltage and its THD analysis
c Voltage THD variation with carrier frequency

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Table 3 Variation of voltage and current THD with load power factor

R (Ω)	L (mH)	Phase Angle (degrees)	Power Factor	%V THD	%I THD
0	600	90	0	10.75	2.42
150	600	66.15	0.404	10.75	2.74
150	400	45.15	0.705	10.75	3.13
150	200	26.68	0.89	10.75	4.35
200	0	0	1.0	10.75	10.75

Table 4 Parameters of experimental work

Notation	Parameter	Value	Characteristics
$V_{dc,1}$	dc voltage Source-1	30 Volts	input
$V_{dc,2}$	dc voltage Source-2	60 Volts	input
$V_{dc,3}$	dc voltage Source-3	60 Volts	input
$I_{dc,1}$	Source-1 dc current	0.5A	measured
$I_{dc,2}$	Source-2 dc current	0.95A	measured
$I_{dc,3}$	Source-3 dc current	0.38A	measured
L	Load inductance	200mH	set value
R	Load Resistance	55Ω	set value
V_{Load}	Load Voltage True RMS	99.3 Volts	output measured
I_{Load}	Load current True RMS	1.067A	output measured
%V-THD	Voltage THD	6.9	quality measure

using Phase Disposition (PD MCPWM) technique. Fig. 7(a) presents the simulated output voltage and current waveform while Fig. 7(b) shows the %THD value and Harmonic profile for the output voltage. The simulation is repeatedly performed at various carrier frequencies and Fig 7(c) shows the relationship between output voltage %THD and carrier frequency. It is observed that voltage THD is affected by carrier frequency; at higher carrier frequencies the low order harmonics are greatly mitigated and harmonics are shifted to the higher frequency band, where they can be filtered by a small size filter. For this particular case PDPWM gives a minimum THD value and higher peak fundamental output voltage at carrier frequency of 1.2kHz. However, comparing with the fundamental switching modulation (SHE), the ON-OFF transitions for switches S_{1b}, S_{1c} and S_4 are doubled and therefore, enhance switching power losses. Therefore, fundamental switching frequency method is preferable from the perspective of power losses and efficiency.

5.2 Hardware results

Practical implementation of the proposed LD architecture is realised by a scaled hardware laboratory setup. Fig.8 shows the schematics and hardware setup. In this prototype, the modules of 11-level proposed multilevel inverter utilized 10 Power MOSFET (IRF BG30) as switching elements while the input voltage and RL load of same magnitudes as used in the simulations model are employed. Power supply GW Instek GPS 3303 is used for providing three regulated input dc sources. The switching angles calculated by SHE Algorithm
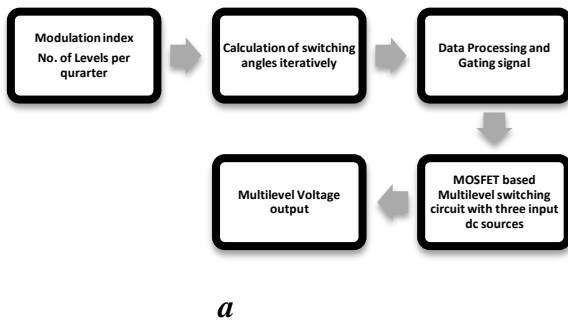
are stored in a lookup table and gate signals are produced with Atmel ATMega 16A Microcontroller board. The MOSFET switches receives gate signals through 9 gate drivers (TLP250). The output waveforms are observed on a 100MHz GW Instek Digital Storage Oscilloscope. The output voltage signal is measured across the MLI output terminals with oscilloscope channel-1 set to 1V/div., and differential probe at x50 scale. The load current is measured at channel-2(20mV/div.) with a GW Instek current probe GCP100 set at 10mV/A. Power quality measurements are also carried out by Power and Harmonic Analyzer Lutron DW 6095. Table-4 lists the parameters used in the experimental work.
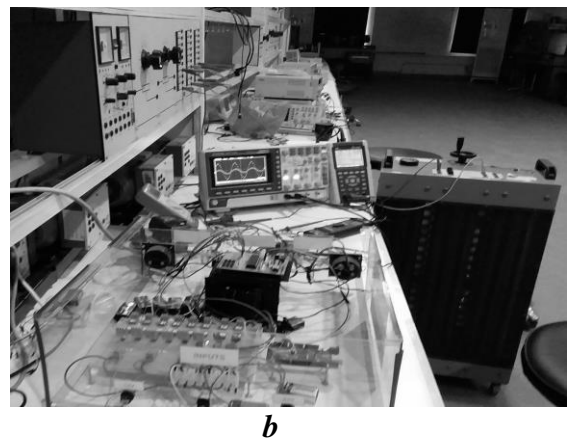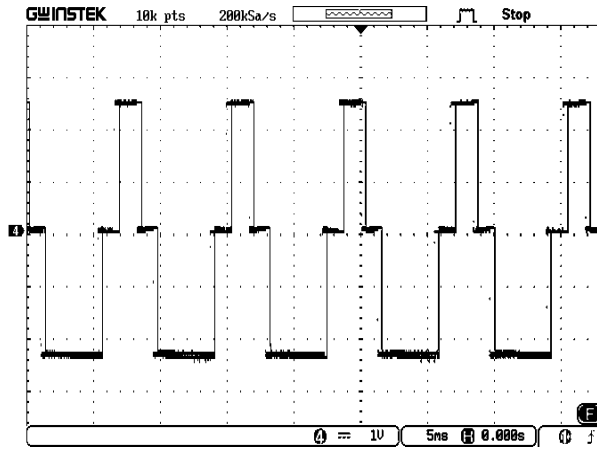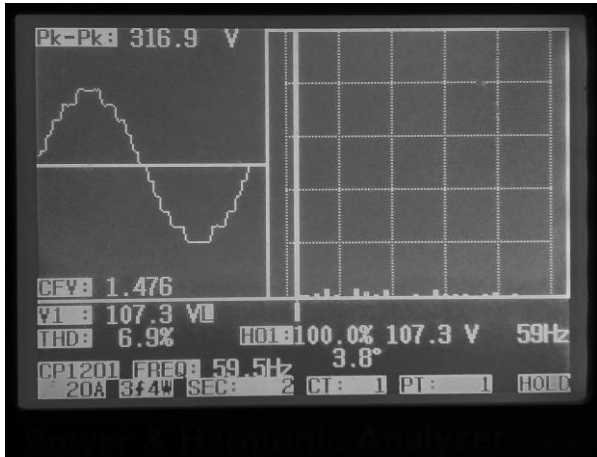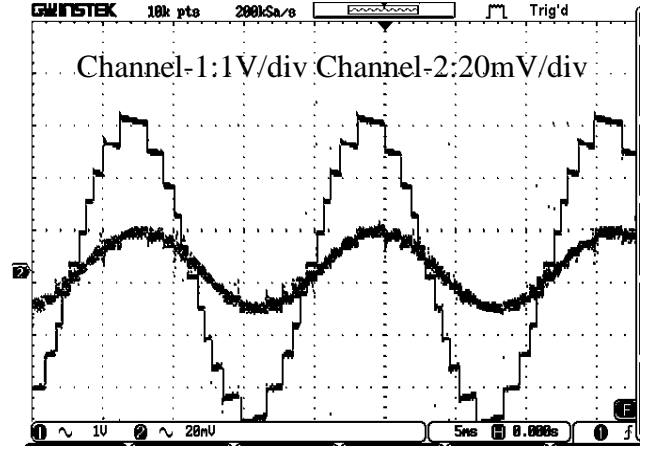

a

b

Fig. 8 *Hardware implementation*
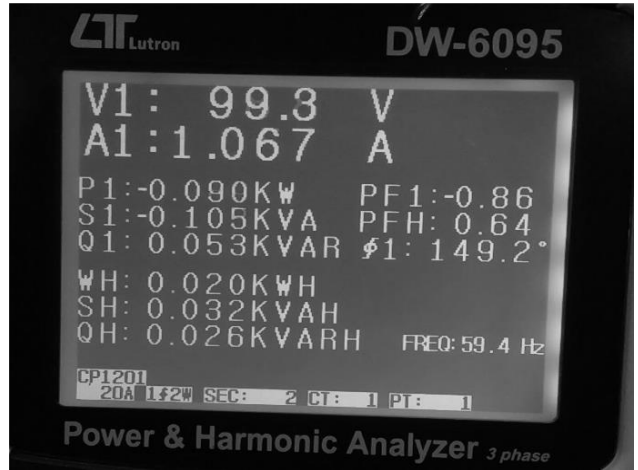*a* Schematics
b The hardware setup

a

c   *d*

Fig. 9 *Hardware results for 11-level inverter of proposed LD architecture*
a Blocking voltage across bidirectional switch S2 at 1V/div. 1:20 differential probe setting
b 11-level output voltage and current waveform
c Plot of harmonic profile and voltage THD by Power Analyser
d Fundamental Power output measured with the Power and Harmonic Analyser

The experimental results are presented in Fig. 9 (a) to 9 (d). As shown in Fig 9(a), switch S_2 blocked voltage of both positive and negative polarity, this validates the selection of a bidirectional switch for S_2 position. The hardware setup also successfully produced 11-level output voltage waveform with maximum level of ±150V. Due to load inductance, the load current is sinusoidal with a magnitude of 1.067A(rms). Thus, the output voltage and current signals obtained in the experimental setup also conform to the simulation results. The load consumed 0.09kW which was only limited due to the current rating of available inductors. The power however can be scaled up with higher rated load inductor and resistor. As shown in Fig. 9 (c, d), the measured values from Power and Harmonic Analyser are obtained as follows: fundamental output power 0.09 kW, and voltage THD 6.9%. The input dc power is given by the sum of power output of three input dc sources, which are measured as P1=15W, P2=57W, and P3=22.8W. Therefore, the efficiency $(\eta = P_{out}/P_{in})$ of the proposed inverter is evaluated as 95 % which is comparable with the 11-level Inverter reported in [25]. Hence, the simulation results and measured values both confirm the practicability of the proposed LD MLI architecture.

6. Conclusion

In this research work, a novel level-doubling topology of cascaded Multilevel Inverter is presented. The proposed architecture showcases many advantages in a single package; such as reduced requirements of IGBTs and gate drivers. Furthermore, it curtails conduction power losses by placing lesser number of switches in the current path compared with earlier LD topologies, hence results in increased efficiency. Although the proposed topology is asymmetric by definition, but the recommended approach for selection of IGBTs in its sub-modules give it a symmetric structure. When all IGBTs are of equal rating, spare management for the end user becomes easier. This characteristic cannot be utilized with asymmetric converters designs. Moreover, design of base cell and sub-multilevel cell is independent of each other and despite different switching duties, effective cooling system for each module can be designed separately. In addition, cascaded expansion also provides a compatibility with HV system. For this domain of operation, three algorithms have

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been proposed for enhancing power quality with small hardware requirements.

Hence, proposed topology has superior attributes comparing with conventional and a number of existing topologies. These include minimum switch-count, optimal utilisation of sources, and higher number of levels besides maintaining the modularity. In addition, a fixed number of minimum devices in current path results in reduced conduction power losses and therefore high efficiency of inverter. The topology is suitable for low and medium voltage, high power-quality applications, while cascaded expansion can increase its output voltage ratings and enables it to operate in HV systems as well.

7. Acknowledgement

8. References

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