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Carrier Transport mechanisms contributing to the sub-threshold current in 3C-SiC-on-Si Schottky Barrier Diodes

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***Abstract*—3C-Silicon Carbide (3C-SiC) Schottky Barrier Diodes on silicon (Si) substrates (3C-SiC-on-Si) seem not to comply with the superior wide band gap expectations in terms of excessive measured sub-threshold current. In turn, that is one of the factors which deters their commercialization. Interestingly, the forward biased part of the Current-Voltage (I-V) characteristics in these devices carries considerable information about the material quality. In this context, an advanced Technology Computer Aided Design (TCAD) model for a vertical Platinum/3C-SiC Schottky power diode is created and validated with measured data. The model includes defects originating from both the Schottky contact and the hetero-interface of 3C-SiC with Si which allows the investigation of their impact on the magnification of the sub-threshold current. For this, barrier lowering, quantum field emission and trap assisted tunneling of majority carriers need to be considered at the non-ideal Schottky interface. The simulation results and measured data allowed for the comprehensive characterization of the defects affecting the carrier transport mechanisms of the forward biased 3C-SiC on Si power rectifier for the first time.**

Keywords*—*3C-SiC; band diagram; carrier transport; defects; heteroepitaxy; Schottky interface; SBD; TCAD; unipolar;

I. INTRODUCTION

3C- Silicon Carbide (SiC) on Silicon (Si) power devices can experience high subthreshold current [1]. This is attributed to the lattice and thermal mismatches of the Si substrate with the 3C-SiC, resulting in epitaxial layers rich in deep levels [2], [3]. Crystallographic defects originating from the SiC-Si hetero-interface propagate far through the grown epi-layers [4], [5]. For this purpose, extensive research effort is undergoing in order to lower the density of crystallographic defects in 3C-SiC hetero-epitaxy [6], [7].

Further, apart from the bulk defects originating from the hetero-interface; interfacial traps also play a significant role in the cubic SiC. Interfaces formed when two materials are brought into contact, are rather complex carriers' transport systems [8].

Forming a reliable Schottky contact on 3C-SiC has indeed been proved a rather challenging task [9]. The presence of a high density of material defects, degenerates the contact and ohmic rather than rectifying behavior is exhibited [10]. Particularly, in 3C-SiC Schottky Barrier Diodes (SBDs) the Thermionic Emission (TE) theory predicts a low leakage current in forward bias. This expectation is owed to the low intrinsic carrier concentration property of the wide band gap (WBG) SiC material. Nonetheless, elevated sub-threshold current levels are usually observed in fabricated devices. The main reason for this is the combined effect of both the Schottky interface and the bulk 3C-SiC defects.

The dangling bonds formed due to the loss of semiconductor surface crystal periodicity interact with the deposited metal and result in a charge at the Schottky metal – 3C-SiC interface. The characterization of this charge depends on the relative Fermi level (E_F) position; a sensitive information that can be extracted from the band diagram of the power device. As a result, the surface charge dynamically changes with the forward bias and is likely to emulate reverse bias conditions enhancing the image force lowering of the SBH. This phenomenon significantly modifies the number of carriers having the required kinetic energy to cross the barrier. In addition, the temperature insensitive field emission or quantum barrier tunneling mechanism affects the majority carrier transport. Eventually, the invoked mechanisms raise the probability of trap-assisted tunneling in 3C-SiC Schottky interfaces for the sub-threshold bias region. In the post-threshold region, the forward current mainly depends on TE theory and is directly affected by the discrete bulk deep levels. It is therefore, of great significance to model the non-ideal behavior in these systems towards understanding the forward bias carrier transport.

The authors previously reported on the parameters and physical models of the bulk 3C-SiC aiming for credible Technology Computer Aided Design (TCAD) modeling and simulation but did not include the effect of non-idealities [11], [12]. This work focuses on investigating the sub-threshold current-voltage (I-V) characteristics of a 3C-SiC on Si SBD which indirectly signifies the actual material quality [13]. An advanced TCAD model is developed to investigate the carrier transport mechanisms, how they are affected by possible energy levels and how they alter the subthreshold current. By including these mechanisms in the model, excellent matching with the experimental measurements has been achieved.

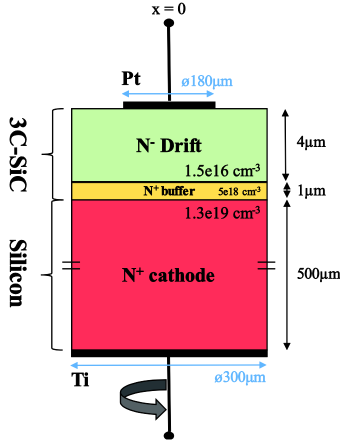

Fig. 1. The TCAD simulated cylindrical asymmetric SBD structure based on an isotype 3C-SiC on Si hetero-interface.

This work is organized as follows. In section II, a detailed model of a vertical SBD based on 3C-SiC on Si is described for TCAD simulations. Further, the non-idealities affecting carrier transport in forward biased SBDs are discussed. In section III, TCAD simulation results are reported and evaluated, pointing out the contribution of bulk and interfacial defects to the I-V characteristics. In section IV the conclusions of this work are summarized.

II. The Non-Ideal 3C-SiC Schottky Contact

A. *The 3C-SiC vertical Schottky Barrier Diode*

The vertical power SBD, considered in this work, features cylindrical contacts and its fabrication was reported in [14]. The Schottky interface was formed from the evaporation of Platinum (Pt) on a 4µm thick non-freestanding drift layer of 3C-SiC material, epitaxialy grown on Si. The area of the Schottky contact is smaller than that of the back Titanium (Ti) ohmic one in order to deal with parasitic capacitance elements of the device [15]. Consequently, a fraction of 3C-SiC surface is exposed on the top. A passivation step is not reported in [14], hence dangling bonds are likely to exist. A buffer layer of 1µm is included resulting in a punch-through design. The Si substrate is approximately 500µm thick [16], whilst all the layers are Nitrogen (N) doped. This indicates a n-type drift layer and thus electrons are the majority carriers. The design details can be identified in the device cross-sectional view illustrated in Fig. 1.

B. *The non-ideal Schottky interface with 3C-SiC*

The work function of Pt is greater than the electron affinity of the n-doped cubic SiC ($\Phi_m > X_{3C}$), indicating that electrons flow from the semiconductor to the metal after contact, until equilibrium is achieved. This flow lowers the potential energy of the bands at the 3C-SiC side. The SBH, or metal-semiconductor work function $\left(\Phi_{B_n}\right)$, formed governs the current transport in the SBD.

The large work function of Pt foresees a reduced subthreshold current. Nonetheless, the annealing process for contact smoothing forms Platinum Silicides (PtSi) [17]. The Schottky contact under investigation is formed from the deposition of 2000 angstrom of metal [14]. It can therefore be assumed that during fabrication, a thin PtSi film was formed. The band diagram of Fig. 2 illustrates the considered SBD based on validated bulk 3C-SiC parameter values [11] and the work function of thin PtSi, $q\Phi_{PtSi} = 4.98\, eV$ [18]. The Table I lists the most significant parameters of 3C-SiC employed in the band diagram. For accurate interpretation, the band gap narrowing phenomenon has been considered in the calculations for the relative position of the E_F in (1), where, n_0 is the equilibrium concentration of majority electrons at $T = 300K$.

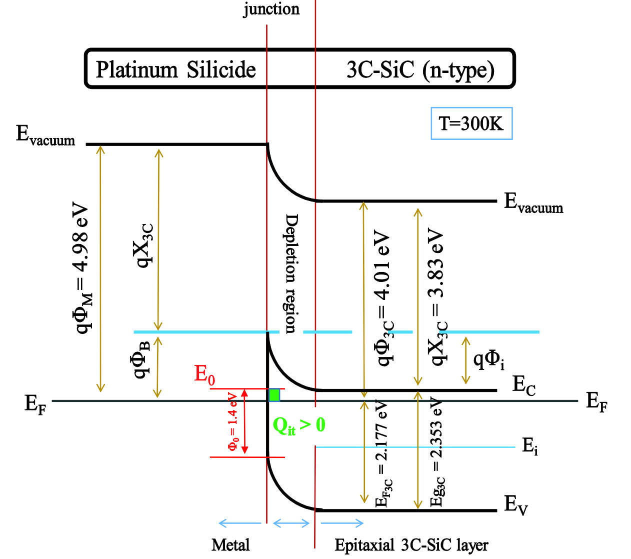

Fig. 2. The band-diagram of the Schottky contact between n-type 3C-SiC and thin PtSi. The non-ideal case is illustrated in which the position of the neutrality level decides the formed interface charge.

$$n_0 = n_i exp\left(\frac{E_F - E_g/2}{kT}\right) \tag{1}$$

Table I: Basic parameters for bulk SiC adopted.

Parameter	Bulk 3C-SiC
Bandgap (E_g) at T=300K [eV]	2.353
Intrinsic carrier concentration (n_i) [cm^{-3}]	0.2285
Electron affinity [eV]	3.83

To derive a more informative band-diagram the interfacial non-idealities should be incorporated. Even after the cleaning processes, dangling bonds exposed at the surface of the 3C-SiC lead to the formation of energy levels. Taking into consideration that the occurred traps are very close to each other; their interactions result in a continuous band of energies at the PtSi / 3C-SiC interface. The formed traps at the interface include both donors and acceptors, as shown in Fig. 3. The notation Φ_0 is used to identify the neutrality level (E_0) in respect to the valence band (E_V). This level separates the acceptor from the donor deep levels at the Schottky interface and is considered material-specific. Traps energetically located above the E_F are more likely to be occupied by an electron. On the contrary, the

ones below the E_F are more likely to be un-occupied by an electron. The acceptor traps carrying a hole are neutrals, whilst they become ionized after capturing an electron featuring a negative charge. Similarly, unless they are occupied by a hole carrying positive charge, donor traps are neutral. Hence, the position of the traps' E_0 determines the Schottky interface charge.

The SBH derived by the Schottky-Mott rule [19] ignores the effect of supplementary electronic states (such as those described in the previous paragraph) at the interface able to absorb charges. In fact, in the presence of high density of interface states in real power SBD devices, the Bardeen's limit delimits the effective barrier height $\left(\Phi_{B_n}^{eff}\right)$ [19]. The presence of charged interface states can lead to a local increase of the electric field at the interface. Subsequently, phenomena like image force lowering and quantum wave function effects are enhanced. For accurate 3C-SiC SBDs simulation results, therefore, these phenomena need to be considered.

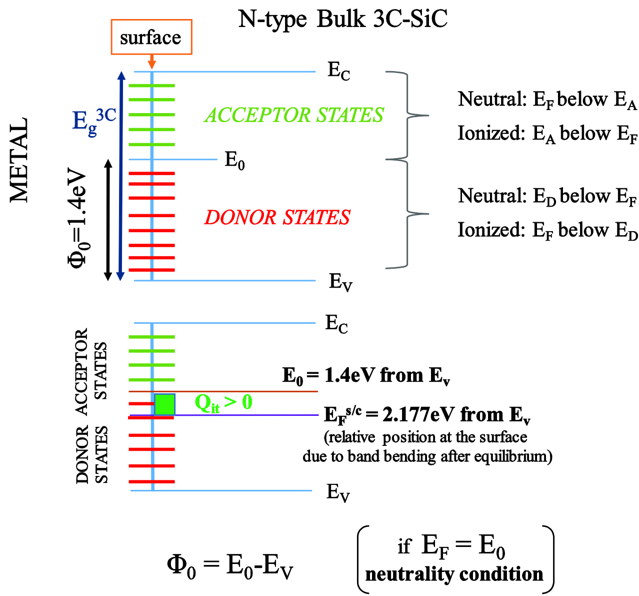

Fig. 3. The continuous band of donor and acceptor traps in conjunction to the assumed position of the neutrality level produces a positive charge at the Schottky interface in equilibrium.

C. Carrier Transport in forward biased non-ideal SBDs

Carriers' transport in a 3C-SiC Schottky interface occurs as a combinational effect of both the potential and the kinetic energy of the carriers. The first one refers to the power device system, whilst the latter one relates to the temperature. For a given temperature, the kinetic energy of the carriers defines the shape of the occupation distribution of electrons in the conduction band (E_C).

According to the TE theory in (2), at each temperature only a fraction of electrons from the tail of the resulting occupation distribution features enough energy to overcome the barrier. In equilibrium the same number of electrons realizes the opposite transition; thus, the net current is zero. The application of forward bias changes the potential energy of the system by moving the bands at the n-type 3C-SiC side upwards. This allows a greater portion of electrons to flow over the barrier disrupting the equilibrium conditions.

In the forward biased log(I) vs V plot of the vertical power diode in Fig. 1, two main regions can be recognized.

$$I = AA^*T^2 e^{-\frac{q\Phi_B}{kT}}\left(e^{\frac{(qV-Ir_s)}{\eta kT}}-1\right) = I_s\left(e^{\frac{(qV-Ir_s)}{\eta kT}}-1\right) \qquad (2)$$

When the supplied voltage is greater than the build-in potential (Φ_i) formed at the abrupt Schottky junction in Fig. 2, the on-state of the device is mainly affected from the bulk 3C-SiC defects. Describing the on-state behavior of the power diode [15], the value of the series resistance (r_s) is modified accordingly. In addition, the E_C offset of the isotype hetero-interface is too small compared to the bias level and thus its contribution is negligible. On the other hand, at the sub-threshold region the saturation current (I_s) dominates. The measured leakage current however, is of orders of magnitude greater than the theoretical expected from the TE expression (2) [14]. Although, the ideality factor (η) incorporates patches that lead to inhomogeneous SBH [15], still, the interfacial defects have a great contribution to the investigated diode current.

III. Results

Synopsys Sentaurus Structure Editor [20] and Synopsys Sentaurus Device [21] is utilized to simulate the modelled SBD depicted in Fig.1. To achieve the best matching to the measurements, a gradual incorporation of the traps and the previously discussed phenomena, related to the non-ideal SBD, took place with subsequent TCAD simulations. In this sense, the impact each phenomenon introduced on the sub-threshold region of the I-V could be examined. The lack of a passivation layer at the fabricated device is considered in this work, by defining a thin layer of fixed positive charges at the exposed 3C-SiC surface of the device with a uniform spatial distribution.

At the Schottky interface, surface defects are introduced with the assumption that the E_0 is above the E_F in equilibrium, as illustrated in Fig.3. This implies that a positive surface charge is apparent due to ionized interfacial donor deep levels, which acts as an additive to the depletion region charge. Each surface defect type is defined with a Gaussian energetic distribution, covering all the bandgap portion that corresponds to it. In other words, both deep and shallow levels are formatted and taken into account. These traps are coupled with the Schottky contact through a calibrated nonlocal trap-assisted tunneling model [22]. The values of the parameters for this model where fine-tuned for 3C-SiC, as shown in Table II, to achieve the best match to the experimental data. From Table II, the tunneling mass of electrons is a dimensionless property of the material that forms the tunneling barrier, whereas the prefactor (g_C) refers to the ratio between the effective [23] and the free electrons Richardson constant [24].

As can be seen in Fig.4 and Fig.5 the near defect-free parameters of 3C-SiC fail to predict the high subthreshold current observed in the fabricated device. With the inclusion of deep levels and the development of a realistic and process informed TCAD model for SBDs, which accounts for defects

in the epi layer, the hetero-interface between Si and SiC and the states at the proximity of the Schottky contact a good prediction is achieved.

Table II: Mobility and Tunneling parameters.

Parameter	3C-SiC	
	electrons	holes
Mobility [cm^2/Vs]	650	50
Tunneling mass [in units of m_0]	0.05	0.05
Interface prefactor (g_C)	$1x10^{-3}$	$0.66x10^{-2}$

The performed simulations presented in Fig. 4 give an insight of how the discussed physical phenomena affect the sub-threshold carrier transport and accordingly the shape of the power SBD log(I)-V curve. In particular, in curve 1 only thermionic emission is activated in the simulations of the power device. In curve 2 the inclusion of traps, according to Table III, does not have a strong contribution in the sub-threshold current unless additional interacting mechanisms are involved like the image force lowering in curve 3. As a matter of fact, the formatted positive charge at the interface enhances this mechanism observed as a barrier lowering. This results in more carriers crossing the barrier for the same potential energy and temperature.

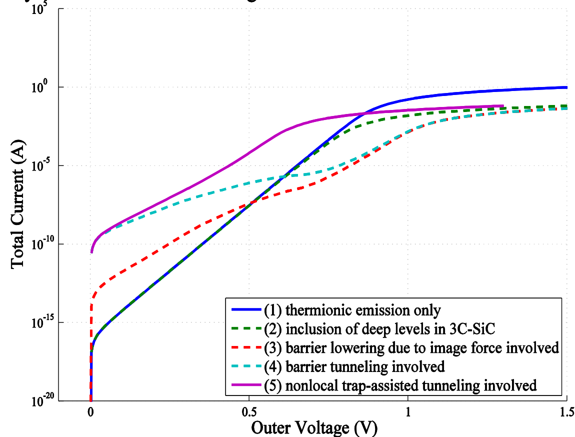

Fig.4: The combined contribution of deep levels and the additional device-specific phenomena considered in this work, in the majority carrier transport from TCAD simulations.

In curve 4 of Fig. 4, the ability of carriers for field emission have a strong impact in the sub-threshold region by increasing the current, especially while the V_F is still low. Majority carriers with insufficient kinetic energy to cross the barrier are now able to achieve a quantum tunneling transition from the 3C-SiC to the metal system. The more the positive interfacial charge formed, according to Fig. 3, the greater the induced electric field at the Schottky interface. Although the device is in low forward bias, this condition causes essential band bending emulating a reverse bias environment. The triangular-like potential barrier, seen in Fig. 2, becomes thinner raising the likelihood of the field emission mechanism. Trap-assisted tunneling in curve 5 shifts the V_{th} to the left as more electrons are now able to approach the barrier causing further lowering that increases the sub-threshold current.

Considering the contribution of all the discussed carrier transport phenomena in the sub-threshold region, the matching to the experimental data is very good. Comparing the curve 1 in Fig.4 to the final simulated forward bias log(I)-V curve of the SBD in Fig. 5, it is apparent that the sub-threshold current is a representative indicator of the semiconductor material quality in 3C-SiC.

Table III: Characterization of utilized traps.

Trap specification	Type		Concentration	
Traps due to not passivated 3C-SiC surface [cm^{-3}]	Fixed charges		$5x10^{18}$	
Schottky interface defects [cm^{-2}]	Acceptor	Donor	$5x10^{12}$	$1x10^{13}$
Bulk deep levels due to 3C-SiC/Si [cm^{-3}]	Acceptor		$1.5x10^{16}$	

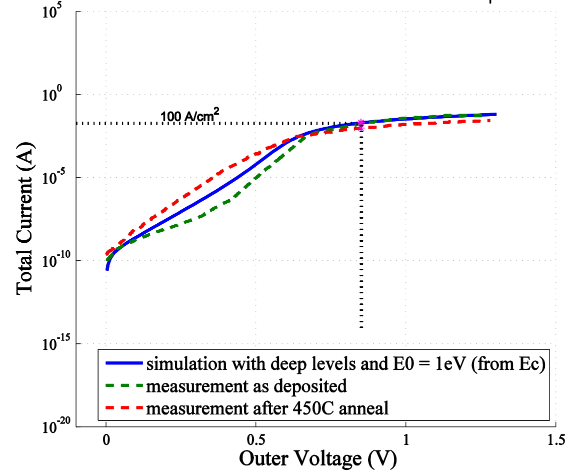

Fig.5: The TCAD simulated I-V characteristics from the investigated non-ideal Schottky Pt / 3C-SiC contact along with the effect from the bulk deep levels due to the 3C-SiC on Si hetero-interface are in excellent agreement to experimental data.

Deep levels originating from the 3C-SiC/Si heterojunction region are modelled to spatially distribute in a uniform manner throughout the 3C-SiC part. In the high current region of the log(I)-V plot, the majority carriers are able to transport from the semiconductor to the metal side readily. Deep level acceptor traps mainly affect this post-threshold part of the I-V characteristic by draining majority carriers and thus limiting the on-state current level. If donor traps are assumed, the excess contribution of majority carriers is compensated by the decrement of electrons mobility due to scattering effects and the post-threshold current level remains almost unaltered. The simulation results, therefore, indicate the latter should be of acceptor type.

According to the literature, the defects generated at the hetero-interface of 3C-SiC to Si, are mainly attributed to the out-diffusion of Si from the substrate in order to contribute to the formation of the overlying SiC layer [25]. To the credit of

this work, the TCAD simulation results are in line with reported observations which consider the Silicon vacancy (V_{Si}) to act as a deep acceptor level [26].

Moreover, the observed simulated behavior of the introduced deep levels originating from the 3C-SiC/Si hetero-interface resembles the presence of Stacking faults (SFs). The SFs in 3C-SiC are highly electrically active also causing scattering of electrons especially in n-type materials [27]. This source of increased resistivity is the main cause for power device degradation. More specifically, the accumulated Nitrogen at such crystallographic defects create preferable paths for the current to flow in 3C-SiC [28]. Further simulations should be carried out to adequately model SFs towards gaining a comprehensive picture.

IV. Conclusions

The TCAD simulations of the investigated 3C-SiC on Si vertical SBD revealed that the first part of the log(I)-V curve is due to the Fermi-level pinning from the effect of the formed interface charge. This phenomenon deviates from the ideal Schottky–Mott behavior and thus an independency on the SBH is indicated. In addition, the tunneling parameters were fine-tuned for the Schottky contacts on 3C-SiC. The characterization of the deep levels by determining the type, densities and distributions of both interfacial and bulk defects led to an excellent matching between simulations and experimental data of the sub-threshold current in the forward biased SBD. Further, the bulk acceptor-like 3C-SiC defects originating from the hetero-interface with Si where identified from literature as V_{Si}. Finally, potential similarities of the modelled bulk traps, originating from the hetero-interface, to the reported behavior of SFs in 3C-SiC is encouraging and needs further investigation.

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