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The Stripe Fortified GCT: A new GCT design for maximizing the controllable current

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***Abstract*—In this paper we introduce a new GCT design, namely the Stripe Fortified GCT, for the purpose of maximizing the controllable current by optimizing the current flow path in the device during turn-off. The main design of the new device along with variants are introduced. The MCC performance of this novel structure is assessed with a developed two dimensional model for full wafer simulations. Our results show that this new design is a very good candidate for increasing the MCC to values more than 5000A.**

I. INTRODUCTION

The Integrated Gate Commutated Thyristors (IGCTs) feature the most competitive trade-offs in the very high power range of the Power Semiconductor Device spectrum. At high current densities, they offer excellent reliability, low conduction losses and large utilization of silicon area [1]. IGCTs also meet the device requirements of high-power converters for DC distribution systems; which are required to handle an increasing share of renewable power [2]. An increase in the power handling capability from one single device would mean a significant reduction in the cost of power conversion in large renewable power generation sites such as offshore wind-farms. For achieving this it is required to increase the GCT's current handling capability even further.

It is possible to increase the Maximum Controllable Current (MCC) by optimising the current flow in the device while it is turning off. The cathode/p-base junction needs to be maintained reverse biased to prevent electron emission. The considerable flow of holes in the close proximity of cathode/p-base junction creates a lateral voltage drop which forward biases the centre of the junction. The aforementioned phenomena ultimately cause re-triggering of the thyristor n-p-n-p structure resulting in the catastrophic failure of the semiconductor device [3]. By providing a more favourable path for the holes trying to reach the gate metallisation well before approaching the proximity of the cathode junction the maximum turn-off current can be increased. The concept of improving the current controllability by better control on the current flow during turn-off is also utilised in the High Power Technology (HPT) GCT [4] where more than 5000A have been reported [5]. This paper introduces the Stripe Fortified GCT, a new device design with increased Maximum Controllable Current.

II. MODELLING THE GCT

A standard 91mm device is shown in Figure 1. It consists of more than 2700 long and narrow cathode fingers surrounded by a gate metallisation. These cathode fingers are distributed in concentric rings (10 in our case) and the gate metallisation in the area between the fingers of ring 5 and ring 6 makes the annular gate contact terminal of the device. They are shorted together by the pole pieces of the press pack housing. An IGCT is the result of the combination of the GCT with its Gate Unit (GU). In order to simulate the behaviour of such a device in dynamic conditions, the interaction between neighbouring regions in the wafer needs to be taken into account.

The developed complete mixed mode model for MCC simulations with the gate unit and the external circuit is shown in Figure 2. It resembles the operation of the GCT with high degree of accuracy in inverter circuits and choppers. It has a di/dt limiting inductor and an over voltage clamp but no dV/dt snubbers. The Device Under Test (DUT) is a GCT model which consists of ten individual, physically defined, two dimensional Finite Element Method (FEM) GCT structures.

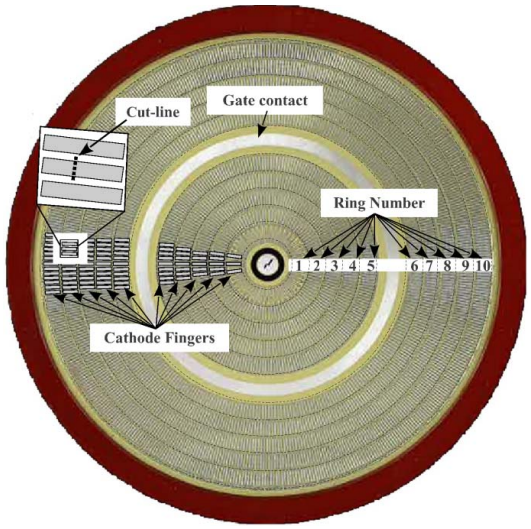


Figure 1. Top view of a typical 91mm wafer Gate Commutated Thyristor with cathode segments arranged in 10 concentric rings and the gate contact placed between Ring 5 and Ring 6. The cut-line refers to Figure 3.

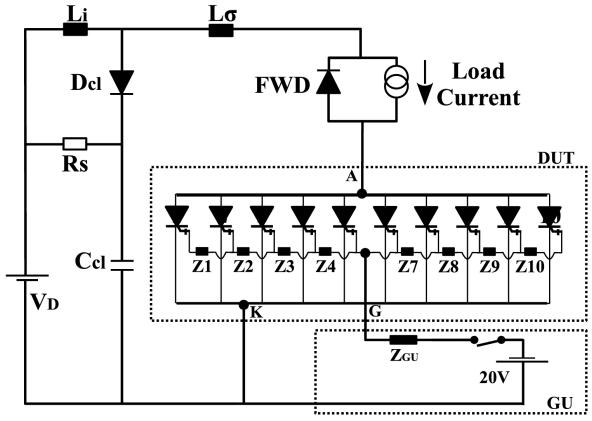


Figure 2. The complete mixed mode model for MCC simulations with the gate unit and the external circuit (Li=2μH, Ccl=10μF, Lσ=0.3μH).

GCT	Impedance (Z)		Active Area [%]
	R [mΩ]	L [nH]	
1	0.39	0.46	3.5
2	0.28	0.62	4.2
3	0.21	0.73	5.5
4	0.17	1.54	6.8
5	-	-	8.2
6	-	-	11.8
7	0.10	0.77	13
8	0.09	0.42	14
9	0.08	0.34	16
10	0.07	0.34	17
GU	0.08	2.15	-

Table 1. Model specific values of the impedance and the active area of every ring.

Each one of them represents one of the ten ring regions of the GCT wafer shown in Figure 1 and has been attributed the approximate active area of the equivalent ring it represents. The gate contact metallisation imposes a distribution of uneven gate inductive loading on the device which alters the current distribution during turn-off. This is modelled by the interconnection of the 2D FEM structures via a SPICE network of impedances (Z1, Z2, ... Z10). The inductance distribution has been derived in [10] whereas the resistance distribution has been evaluated after direct calculation by us. The model specific values are shown in Table 1. Our mixed mode model of interconnected physically defined GCT cells can capture the turn-off failure which makes it ideal for wafer level MCC studies. Similar mixed mode two dimensional models for full wafer devices have also been used for MCC studies [6].

III. Novel Cell Design

The cell structure and the doping design of the proposed Stripe Fortified GCT is depicted in Figure 3. A similar design (but not the same) with a buried high p concentration exists in Gate Turn Off (GTO) thyristors [7, 8]. In this case, the p base is made lowly doped (therefore highly resistive) to achieve high cathode/gate breakdown voltage and the p+ buried layer inside the p base (underneath the gate) aims to restore the

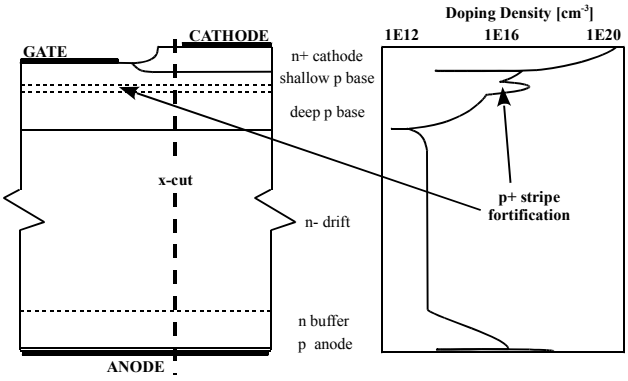


Figure 3. The Stripe Fortified GCT - cell structure and doping design along the cut-line shown in Figure 1.

lateral resistance of this region. The increase in the cathode/gate breakdown aims to mitigate early design limitations of the gate unit in GTOs whereas the decrease of the p base resistance under the gate aims to improve the Safe Operating Area (SOA). The Stripe Fortified GCT is structurally identical to the conventional GCT – also in the p base – with an additional p+ layer positioned 30μm away from the gate electrode; the exact position of the stripe can vary however. The peak concentration of this extra layer is $1x10^{17}cm^{-3}$ and it is approximately 10μm wide. In this paper, various stripe configuration not limited solely to the region under the gate are investigated. Alternative designs where the stripe is discontinued (placed only beneath the gate or the cathode region) have also been considered.

IV. Methodology and Results

A conventional reference design (marked as Ref. in Figure 4 and Figure 5) is first optimized for high MCC, then the stripe fortified GCT (stripe added on the conventional Ref. design) with variants have been studied. The procedure for the determination of the MCC, requires many mixed mode simulations due to the fact that one simulation can only predict

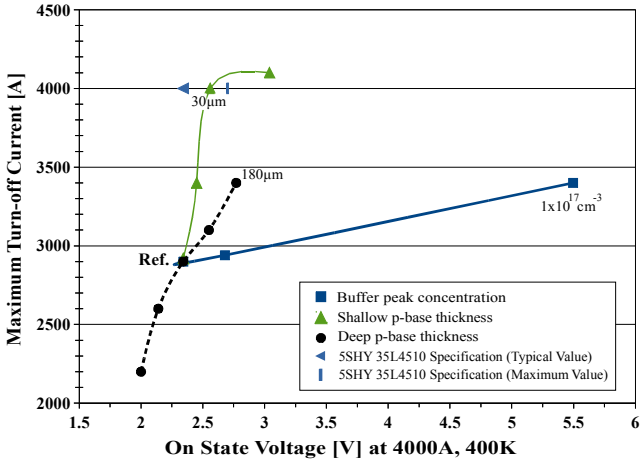


Figure 4. Optimization curves – Last pass turn-off current as a function of the on state voltage drop at 4000A, 400K. - Ref.: shallow p-base of 20μm thickness and $1x10^{17}cm^{-3}$ peak concentration, 140μm deep p-base thickness and $1x10^{16}cm^{-3}$ buffer peak concentration.

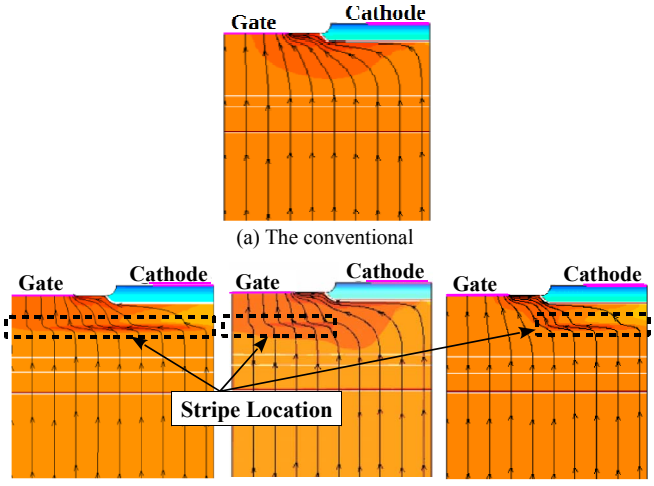
whether the device is able to switch off or not. Initially the DC link voltage (V_D) is fixed to the normal working voltage of 2800V and the temperature (T_J) to 400K. The circuit components are kept constant and the device is set to turn off a certain current. Every successful turn-off is followed by another turn-off simulation with increased current until a failure is recorded. The conditions for considering a turn-off to be successful are those described in [4]:

Successful turn-off: A turn-off is considered to be successful when the anode current reduces to the blocking leakage value right after the tail phase.

Failure to turn-off: The GCT is considered to have failed to turn off when during the anode voltage rise period one or more cathode fingers start conducting more than 10% of the on-state anode current value.

The optimization curves are shown in Figure 4. The reference conventional (Ref.) design gives an MCC at 2900A. When optimized for high MCC, the conventional design achieves about 4000A which matches the specifications of 5SHY35L4510 [9], a 91mm conventional GCT.

In order to assess the effectiveness of the proposed structures in providing a secondary path for the current during turn-off, single cell turn-off simulations have been performed. The MCC simulations have a considerably larger footprint in computational resources when compared to single cell single turn-off simulations. It is therefore useful to use the current flow-lines and the current density contour maps as a mean to provide a simpler and faster approach in assessing how effective the proposed designs can be. The current density contours with stream traces for the most important stripe design variants are compared with the conventional in Figure 5. The Stripe Fortified (Figure 5b) and the Stripe Fortified Cathode (Figure 5d) GCT show a considerable reduction in the local current density underneath the cathode junction. The Stripe Fortified Gate (Figure 5c) on the other hand does not



(a) The conventional

(b) Stripe Fortified (c) Stripe Fortified Gate (d) Stripe Fortified Cathode

Figure 5. Total current density: contours and stream traces during turn-off

seem to alter the current flow under the cathode. As shown, the stripe demonstrates a considerable effectiveness in providing an alternative path for the current by guiding the carriers towards the gate metallisation before reaching the proximity of the cathode. A similar reduction in the current density under the cathode has also been identified in HPT GCTs where improved controllability has been achieved [4, 5].

The conclusive MCC results with respect to the on-state voltage drop are depicted in Figure 6. **The Stripe Fortified Gate** does not present any significant improvement in the controllable current which is consistent with the current contours and the current flow lines of Figure 5c. This design fails to reduce the current density underneath the centre of the cathode which leaves the device sensitive to a parasitic latch-

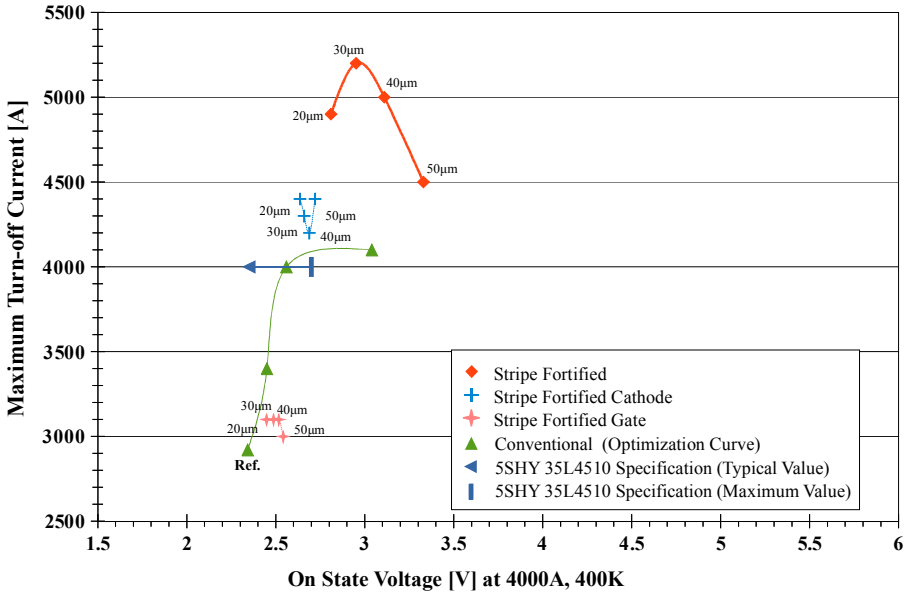


Figure 6. Simulation Results: The Maximum Controllable Current versus the on-state voltage drop for the reference conventional design, the proposed Stripe Fortified GCT and variants.

up [3]. The **Stripe Fortified Cathode** design gives an MCC limit of 4200-4400A and there is very little change in the maximum turn-off current with respect to the vertical position of the stripe. The current contours and flow lines for this design are shown in Figure 5d. **The Stripe Fortified design** (stripe is continuous) demonstrates the most promising performance with MCC ranging from a minimum of 4500A to a maximum of 5200A. The current contours and current flow lines are shown in Figure 5b. As shown, the vertical position of the stripe strongly affects the current controllability. The stripe is very effective when it is positioned between 20-40μm from the gate surface. If positioned more deeply or closely to the surface the improvement in the MCC is only marginal.

V. DISCUSSION

The manufacturing of such a highly doped region deep in the silicon is not apparent. An easy solution to this problem is to epitaxially grow the top side of the GCT similarly to what has been done for the fabrication of Static Induction Thyristors, Static Induction Transistors and the Buried Gate GTOs [11, 12, 13]. When considering the current process used in the fabrication of the state-of-the-art GCT devices, epitaxial growth is not the most preferable fabrication method however. An alternative method is the Ultra-High Energy Boron Implantation where implantation of boron with energies between 2.5MeV and 25MeV can be achieved to give p-regions as deep as 40μm similarly to what has been demonstrated in [14] and [15].

The proposed Stripe Fortified design for GCT demonstrates a considerable improvement in current controllability. During turn-off, the stripe provides an alternative highly conductive path for the holes to reach the gate electrode. This alternative path, being at a distance from the cathode junction, results in a considerable reduction in the current density underneath the centre of the n+ emitter. As a result, a higher conduction current is required to cause the cathode to re-trigger parasitically while turning off [3]. Nevertheless not all stripe designs are effective; there exists a performance difference between continuous and discontinued stripe designs for example. Also the results show clearly that the stripe is effective in averting the device from re-triggering only when it is placed within the p-base region underneath the cathode (e.g. the "Stripe Fortified Cathode" and the "Stripe Fortified" variants). This result differs from the observations made for the GTO thyristor in [7] for which the stripe was restricted to the gate region.

Another design parameter that affects both the current controllability but also the on-state losses is the vertical position of the stripe. A deeper stripe results in a linear increase in the on-state losses. This is not the case for the current controllability however. A shallow stripe becomes less effective, because its doping becomes comparable to the background p-base doping, whereas a very deep stripe becomes ineffective because the carriers can escape this narrow path more easily. Therefore there exists an optimum position for the stripe which has been found to be at around 30μm where the MCC is maximized and Stripe Fortified GCT is predicted to achieve 5200A.

VI. CONCLUSIONS

In this paper a novel GCT design is presented, namely the Stripe Fortified GCT. Variants of the main proposed structure are also discussed. The MCC performance of this design is assessed with a developed two dimensional model for full wafer simulations which was initially used to optimize a reference GCT for Maximum Controllable Current. The simulation results show that the Stripe GCT is a very promising candidate for lifting the MCC to values more than 5000A.

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