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A Comprehensive Comparison of the Static Performance of Commercial GaN-on-Si Devices

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***Abstract*—Gallium Nitride (GaN) based devices on Silicon (Si) substrates (GaN-on-Si) promise unmatched performance at low cost. Despite this theoretical promise, the lattice and thermal conductivity mismatch between the GaN and Si has obstructed the realization of reliable electrically graded high voltage devices. Recently, a small number of manufacturers have claimed the successful development of such devices. Panasonic and Transphorm among a few others have also made their devices available in the open market. The commercial availability of these devices, (something common only for mature technologies), proves the remarkable progress that has been achieved. In this paper, a comprehensive and experimentally derived comparison of the static performance is made between the 600 V Panasonic PGA26C09DV Gate Injected Transistor (GIT) and the 600 V Transphorm cascode TO-220 series devices. The Si 650 V Infineon SPA15N60C3 Super-Junction (S-J) provides a reference with Si technology. The Panasonic devices feature a p-GaN layer which makes them one of the first Enhancement mode (E-mode) GaN power devices on the market, whereas the Transphorm devices are Depletion-mode (D-mode) High Electron Mobility Transistors (HEMTs) cascaded with a low voltage (LV) Si Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Despite the Panasonic and Transphorm devices being examples of GaN-on-Si aiming for the same applications, the measurements and analysis shows that their performance is very different.**

Keywords— B1505A, cascode GaN, E-mode, GaN HEMT, power devices, static performance.

I. INTRODUCTION

Within the last few years GaN HEMT devices have demonstrated remarkable achievements [1]–[4], however, conventional GaN HEMTs are inherently D-mode devices. This has presented significant complications in system designs and requires complex safety measures to prevent situations like shoot-through failures occurring [5]. Therefore, the desire to overcome these issues has led to the development of several E-mode devices reported in [6]. In this paper we will discuss two of the most promising types of devices, the p-GaN layer GaN GIT and the cascode GaN HEMT [7]. The circuit schematics for these devices are shown in Fig. 1.

The principle difference between the two different devices is how they achieve normally-off operation. Panasonic GITs are fundamentally E-mode devices, by utilizing a p-doped GaN layer beneath the gate they have successfully shifted the potential across the channel under the gate [8] shown in Fig. 2. There is an additional p-GaN region adjacent to the drain. This acts to detrap trapped electrons and therefore, prevent current collapse [9]. In contrast, Transphorm have cascaded a D-mode HEMT device with a E-mode LV Si MOSFET to produce a composite E-mode device [10].

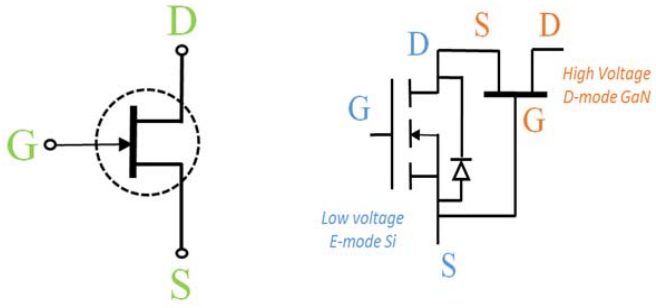

Fig. 1 Topology of the Panasonic GaN based GIT (left) and the Transphorm cascode GaN HEMT (right).

The considerable difference in device technology has posed many unique challenges for each type of GaN device, for instance, [6] has reported system design complications associated with the low threshold of p-GaN layer GaN GIT. In contrast; [11], [12] have discussed the limitations associated with the parasitics of the package in GaN cascode devices.

After several years of development Panasonic launched the TO-220 600 V PGA26C09DV p-GaN layer GaN-on-Si GIT in 2013[13]. In the meantime, Transphorm published the first qualified JEDEC data relating to the GaN-on-Si cascode-package in February 2013 [14]. Subsequently, the first generation of commercialized TO-220 600 V GaN-on-Si cascode package power devices was introduced in 2015. Panasonic and Transphorm have both developed devices that compete in the same voltage class as highlighted in Table 1.

TABLE 1. TESTED DEVICES

Manufacturer	Type of Device	Power Device Model	Rated class	No. of Devices
Transphorm	*Cascode*	*TPH3202PS*	*600V/9A*	*10*
Transphorm	*Cascode*	*TPH3206PD*	*600V/17A*	*10*
Panasonic	*P-GaN*	*PGA26C09DV*	*600V/15A*	*2*
Infineon	*S-J*	*SPA15N60C3*	*650V/15A*	*3*

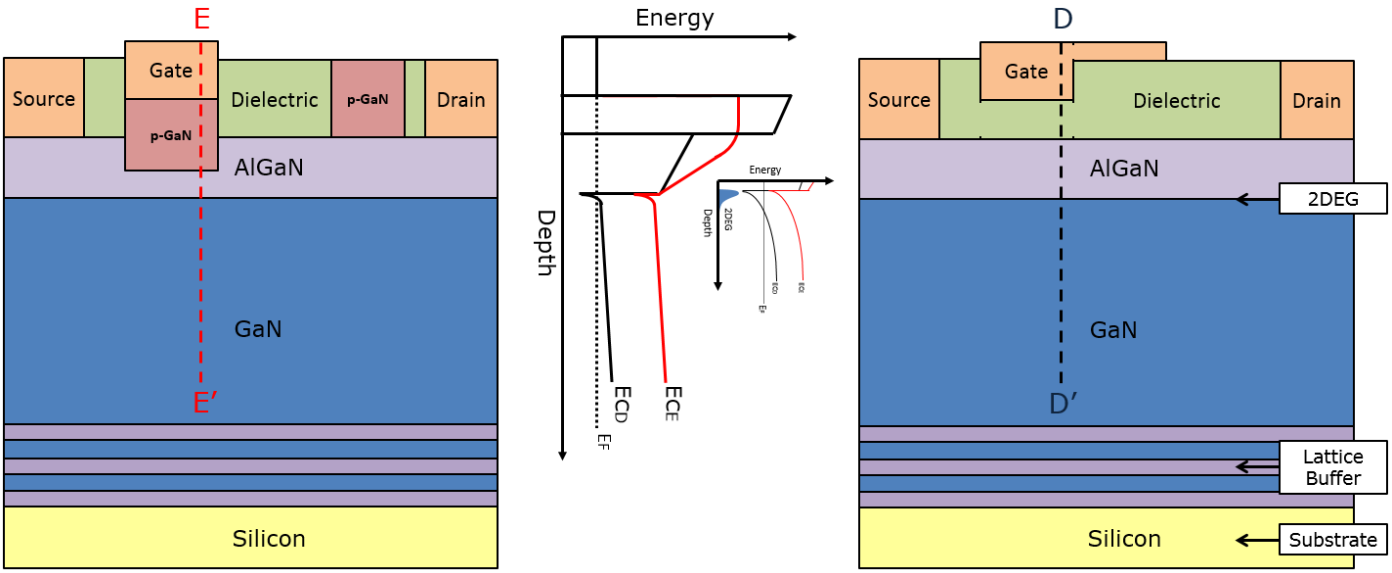

Fig. 2 Schematic Cross Sectional View and Band Diagram of (left) GaN Hybrid Drain (HD) GIT and (right) GaN D-mode HEMT in Cascode Topology

Although, the performance of cascode HEMTs has been reported in [10], [13], [14] and of p-GaN GIT devices in [9], [13], [16], few works have been produced directly comparing the two, let alone with the state of the art Si technology. Therefore, in this paper, we analyse an Infineon Si S-J MOSFET, the Transphorm cascode GaN HEMT and the Panasonic p-GaN layer GaN GIT, providing information on application suitability and evaluating the characteristics of these devices.

The remaining parts of this work are arranged as follows; in section II, the methodology and experimental setup is defined. In section III, the static characteristics are presented and analyzed. Finally, in section IV the conclusions are presented.

II. Methodology

The specific models evaluated and compared in this paper are shown in Table 1.

Experimental Setup

Devices were measured at a constant temperature of 300 K, using the Keysight B1505A Power Device Analyzer [17] [18]. The devices were inserted into the 500 Amp Ultra-High Current 3-pin inline package socket module on the N1265A Ultra-High Current Expander/Fixture which was connected to the B1505A Power Device Analyzer. For capacitance measurements the N1260, High Voltage Bias was used. Cable parasitics were limited through calibrations and appropriate cable selection. The junction temperature (T_j) of the Device Under Test (DUT) was monitored every 2 seconds using a thermocouple attached to the device's heat sink, applying the assumption that the temperature at the heat sink is the same as the device's T_j. Fig 3 displays the B1505A oscilloscope view. This was used to verify the measurement window (red), pulse period, pulse width, voltage and current.

Furthermore, it should be noted that a 100 Ω resistor was connected to the gate to minimize the overshoot oscillations and encourage steady state operation at the measurement window.

If not specified, devices were tested using the parameters provided by their respective datasheet [19]–[21]. In addition, throughout the experiments pulsed measurements were used to limit the self-heating effect on the devices.

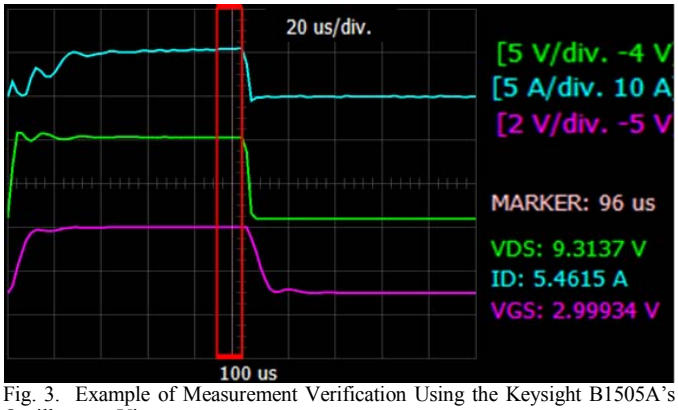

Fig. 3. Example of Measurement Verification Using the Keysight B1505A's Oscilloscope View.

Fig 4 displays the Keysight B1505A Power Device Analyzer, the N1265 Ultra-High Current Expander/Fixture, the N1260 High Voltage Bias Tee and the 500 Amp Ultra-High Current 3-pin inline package socket module. With this equipment the forward (I_{ds}-V_{ds}), reverse (I_{ds}-V_{ds}), transfer (I_{ds}-V_{gs}), on-state resistance (R_{ON}), Capacitance-Voltage (C-V) and breakdown voltage (BVDSS) measurements were performed. Throughout the paper, I_{ds} denotes the drain-source current, V_{ds} the drain-source voltage and V_{gs} the gate-source voltage.

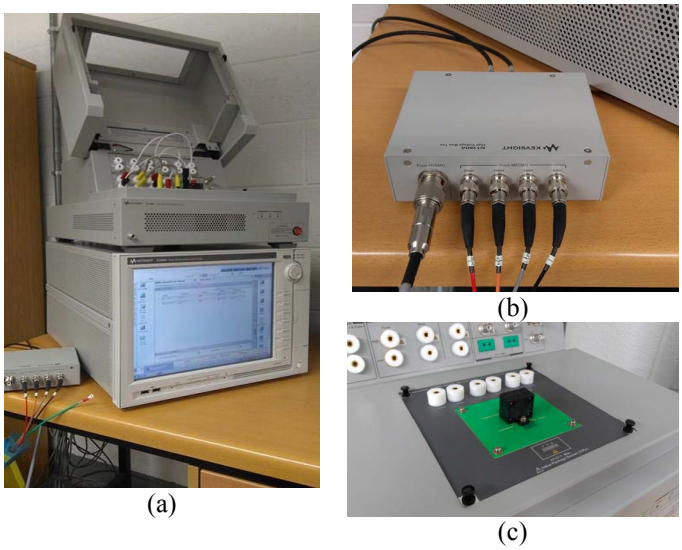

Fig. 4. (a) The Keysight B1505A Power Device Analyzer and N1265 Ultra High Current Expander/Fixture. (b) The N1260 High Voltage Bias Tee. (c) The 500 Amp Ultra-High Current 3-Pin Inline Package Socket Module.

III. Experimental Results and Analysis

A. Forward I-V Characterisitcs

Table 2 summarises the parameters used to perform the measurements of the pulsed forward I_{ds}-V_{ds} characteristics.

TABLE 2. FORWARD I_{DS}-V_{DS} EXPERIMENTAL PARAMETERS

Device	V_{gs} (V)	Step (mV)	V_{ds} (V)	Step (mV)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	*0-10*	*1000*	*0-10*	*100*	*100*	*1*
PGA26C09DV	*0-4.5*	*500*	*0-10*	*100*	*100*	*1*
TPH3202PS	*0-10*	*1000*	*0-10*	*100*	*100*	*1*
TPH3206PD	*0-10*	*1000*	*0-10*	*100*	*100*	*1*

Fig 5 displays the pulsed forward (I_{ds}-V_{ds}) characteristics of the SPA15N60C3 S-J (a), the PGA26C09DV GIT (b), TPH3202PS (c) and TPH3206PD (d) GaN HEMTs.

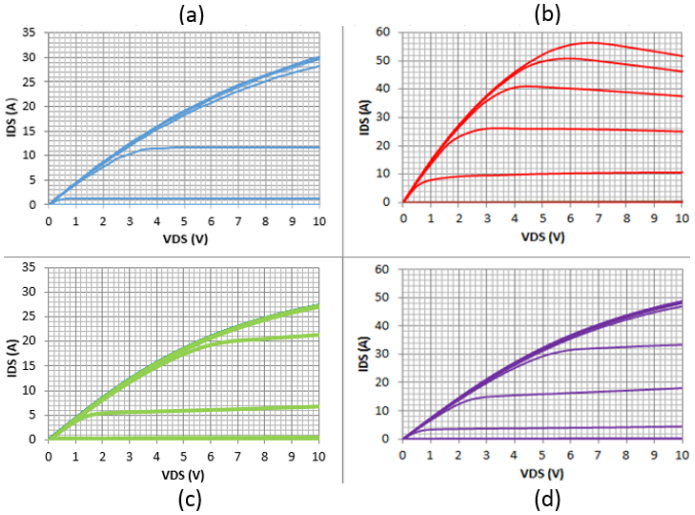

Fig 5. Forward I_{ds}-V_{ds} Characteristics

The measured I_{ds}-V_{ds} characteristics for the Transphorm TPH3202PS and TPH3206PD display a considerable difference with the manufacturer's datasheet [20], [21]. They experienced a saturation of I_{ds} 44 A at V_{gs} 7 – 10 V. In contrast, the datasheet states that the device should have an I_{ds} of + 80 A for a V_{gs} of 10. The Transphorm TPH3206PD measurements match the experimental and simulated results of [12]. In addition, these agree with the experimental I-V characterisation of a Transphorm TPH3206PD in [22]. The Panasonic PGA26C09DV shows superior I_{ds}-V_{ds} characteristics compared the similarly rated Transphorm TPH3206PD and Si SPA15N60C3 S-J device.

B. Reverse I-V Characterisitcs

Table 3 summarises the experimental parameters for the pulsed reverse I_{ds}-V_{ds} characteristics.

TABLE 3. REVERSE I_{DS}-V_{DS} EXPERIMENTAL PARAMETERS

Device	V_{gs} (V)	Step (mV)	V_{ds} (V)	Step (mV)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	*0-10*	*1000*	*0-(-10)*	*100*	*100*	*1*
PGA26C09DV	*0-4.5*	*500*	*0-(-10)*	*100*	*100*	*1*
TPH3202PS	*0-10*	*1000*	*0-(-10)*	*100*	*100*	*1*
TPH3206PD	*0-10*	*1000*	*0-(-10)*	*100*	*100*	*1*

Fig 6 displays the pulsed reverse (I_{ds}-V_{ds}) characteristics of the SPA15N60C3 S-J (a), the PGA26C09DV GIT (b), TPH3202PS (c) and TPH3206PD (d) GaN HEMTs.

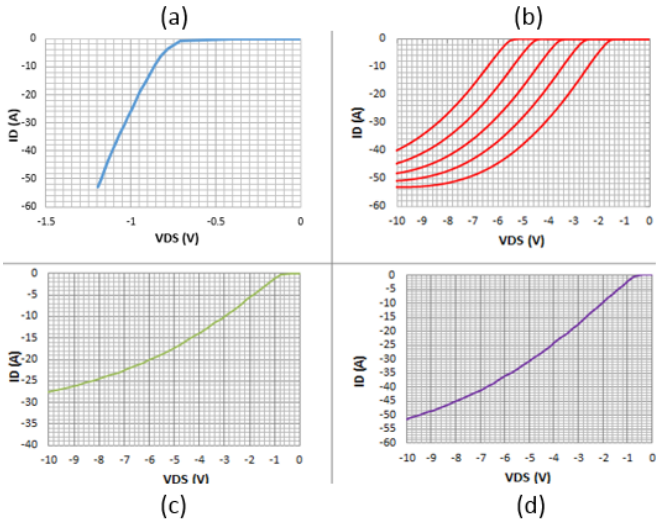

Fig 6. Reverse I_{ds}-V_{ds} Characteristics

GaN HEMTs do not have a body diode [6] this is also the case for the Panasonic GIT (see diagram of Fig. 1). With the absence of an anti-parallel body diode, reverse conduction is possible if the drain voltage falls below the sum of the gate potential and the threshold voltage. This method of reverse conduction is reverse-recovery free which makes it ideal for applications like half-bridge and full-bridge converters [23]. In

contrast, the Infineon S-J and Transphorm cascode HEMTs have an antiparallel body diode.

C. Transfer Characterisitcs

Table 4 summarises the experimental parameters for the transfer characteristics I_{ds}-V_{gs}.

TABLE 4. I_{DS}-V_{GS} EXPERIMENTAL PARAMETERS

Device	V_{gs} (V)	Step (mV)	V_{ds} (V)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	*0-10*	*1000*	*10*	*100*	*1*
PGA26C09DV	*0-4.5*	*500*	*10*	*100*	*1*
TPH3202PS	*0-10*	*1000*	*10*	*100*	*1*
TPH3206PD	*0-10*	*1000*	*10*	*100*	*1*

Fig 7 displays the pulsed (I_{ds}-V_{gs}) transfer characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs.

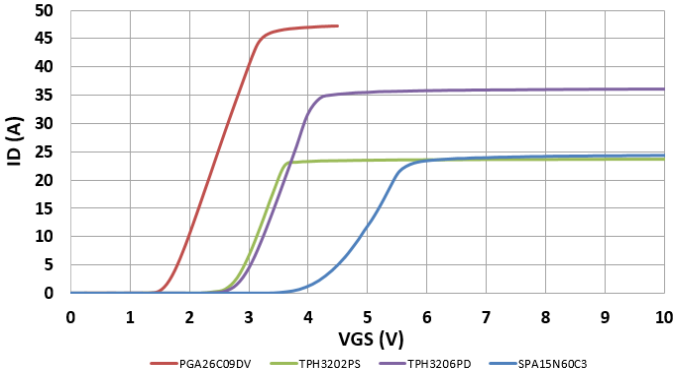

Fig 7. I_{ds}-V_{gs} Transfer Characteristics.

The device threshold voltages (V_{TH}) were obtained using the method of linear extrapolation of I_{ds}-V_{gs} curves [24]. The transfer characteristics corroborate with the typical properties of naturally E-mode HEMT devices with relatively low gate V_{TH} reported by [6]. The Panasonic PGA26C09DV has a gate V_{TH} of 1.2 V compared to the Transphorm TPH302PS and TPH3206PD's 2.5 V_{TH}. This greater V_{TH} can be attributed to Transphorm's use of the cascaded LV Si MOSFET illustrated in Fig 1. The LV Si MOSFET is arranged to drive the GaN device, therefore, it will determine the overall device's V_{TH}. Contrary to this, the PGA26C09DV is driven solely by the p-gate.

In addition, according to the datasheet, the maximum operation V_{gs} for the Panasonic PGA26C09DV is relatively low at 4.5 V. It has been reported that large gate voltages in GITs by even small amounts may lead to device failure [12]. However, we experimented with gate voltages well above 10 V and found no device failures. On the contrary, Transphorm's TPH3202PS and TPH3206PD devices are capable of withstanding gate voltages up to 18 V according to their respective datasheets. This is because of the LV Si MOSFET driving the composite device. The higher gate breakdown voltage allows a certain degree of freedom to use traditional Si MOSFET drivers and lessen the complexity of system safeguards to prevent the premature failure of the power device. Furthermore, although temperature has not been considered in these experiments, real application may induce small V_{TH} shifts which can render the device uncontrollable or to behave in a non-desirable manner.

D. On Resistance Measurements

Table 5 summarises the experimental parameters for the pulsed forward R_{on}-I_{ds} characteristics.

TABLE 5. R_{ON} EXPERIMENTAL PARAMETERS

Device	V_{gs} (V)	I_{ds} (A)	Step (mA)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	*4.5*	*1-44*	*100*	*100*	*1*
PGA26C09DV	*2.5*	*1-45*	*100*	*100*	*1*
TPH3202PS	*4.5*	*1-24*	*100*	*100*	*1*
TPH3206PD	*4.5*	*1-36*	*100*	*100*	*1*

Fig 8 displays the forward pulsed R_{on} vs I_{ds} characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs.

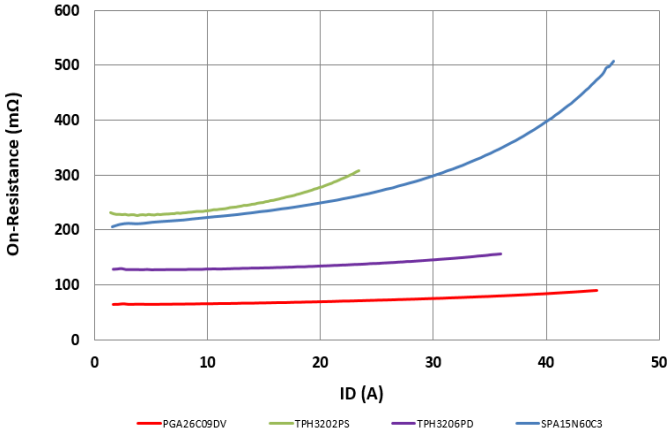

Fig 8. Forward R_{on}-I_{ds} Characteristics.

The Panasonic PGA26C09DV has a significantly lower R_{on} than the Transphorm devices. In addition, compared to the state-state-of-the-art Si MOSFET technology the PGA26C09DV has one thirteenth of the On Resistance, Gate Charge ($R_{on}Q_q$) [25], which is an important for fast switching. The Transphorm devices still display impressive R_{on} values when compared to similarly rated Si technology [14].

Reportedly, 10% of the resistance in the cascode devices can be contributed to LV Si MOSFET to GaN HEMT connection [10]. Recently a wire bond-less package for a cascode GaN HEMT has been presented in [26]. This may further reduce the R_{on} and provide more reliable operation without wire bond lift-off failures and smaller parasitics. However, even with this reduction in parasitics attributed to the LV Si MOSFET to GaN HEMT bond wires, the

PGA26C09DV still displays considerably lower R_{on}. Achieving this lower R_{on} has significant impacts in the overall system in terms of efficiency and power loss for power supply system's as reported by [27].

E. C-V Measurements

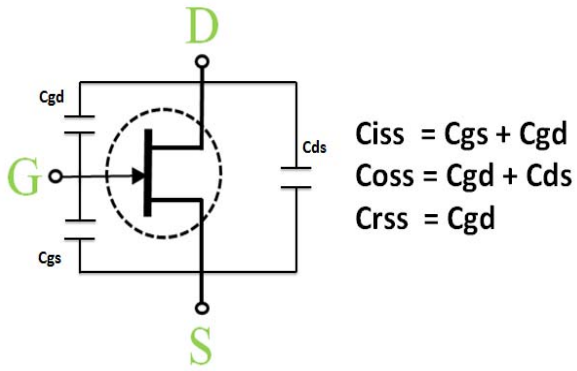

Fig 10. Equivalent Capacitance Diagram for the E-mode GaN GIT displaying the Output Capacitance (Coss), Input Capacitance (Ciss) and Reverse Capacitance (Crss) Components

Table 6 summarises the experimental parameters for the C-V measurements.

TABLE 6. C-V EXPERIMENTAL PARAMETERS

Device	V_{ds} (V)	Step (V)	Frequency (MHz)
SPA15N60C3	*0.1-650*	*0.65*	*1*
PGA26C09DV	*0.1-650*	*0.65*	*1*
TPH3202PS	*0.1-650*	*0.65*	*1*
TPH3206PD	*0.1-650*	*0.65*	*1*

Fig 11 displays the Coss, Ciss and Crss measurements of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs.

The Panasonic PGA26C09DV device has significantly lower Coss, Ciss and Crss values than the two Transphorm devices. This is attributed to the overall design of the device. For switching applications, it is highly desirable to have low Ciss. Turn-on/Turn-off delays are proportional to the devices Ciss, increasing this time will prevent high speed switching capabilities. For the Transphorm cascode device, the Ciss is dominated by the LV Si MOSFET, however, driver loss is less significant for High Voltage (HV) applications. In the cascode devices Coss is dominated by HV Metal Insulated Semiconductor Field Effect Transistors D-(MISFETs), which is promising due to D-MISFETs intrinsic low output capacitance property [28]. The cascode Gate to Drain Capacitance (Cgd), which determines major switching losses, is mainly composed of HV D-MISFET's the Drain to Source capacitance (Cds), the LV Si FET's Cgd/Coss ratio and Zener diode capacitance. In this case, the HV D-MISFET, LV Si FET and Zener diode need to be carefully designed to achieve an optimized Cgd for the cascode device to ensure high switching capabilities as device size and transconductance play a role in this. It should be noted that we did not measure the gate charge (Qq). The Transphorm TPH3202PS has higher capacitance values than the TPH3206PD device.

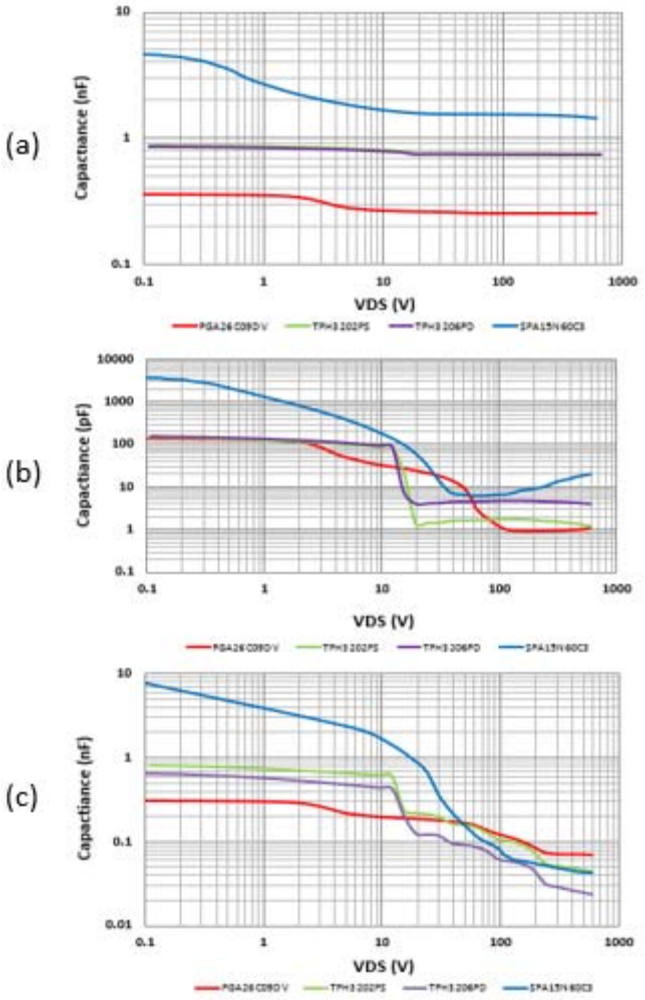

Fig 11. Coss (a), Ciss (b) and Crss (c) Measurements.

F. BVDSS Measurments

Table 7 summarises the experimental parameters for the BVDSS measurements.

TABLE 7. BVDSS EXPERIMENTAL PARAMETERS

Device	V_{gs} (V)	V_{ds} (V)	Step (V)	Max I_{ds} (µA)
SPA15N60C3	***0***	***0-1000***	***1***	***100***
PGA26C09DV	***0***	***0-1000***	***1***	***100***
TPH3202PS	***0***	***0-1000***	***1***	***100***
TPH3206PD	***0***	***0-1000***	***1***	***100***

Fig 8 displays the BVDSS characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs. The measurements shown are for new devices with multiple devices tested. All these waveform experience some level of noise contributed by the limitations of the measurement equipment.

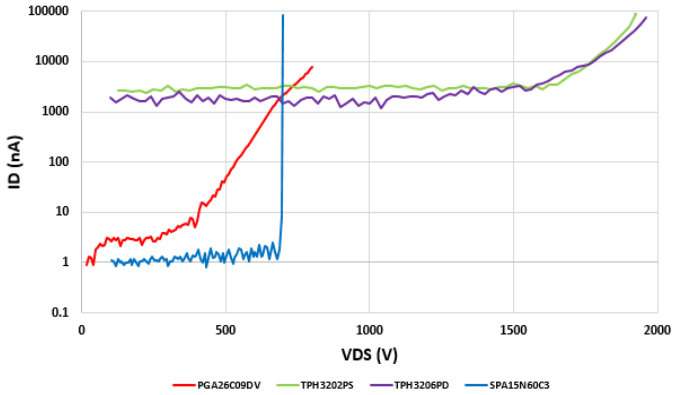

Fig 12. BVDSS Measurements

The Panasonic PGA26C09DV GIT has a drain leakage current a magnitude lower than the Transphorm devices and a breakdown voltage of approximately 750 V. Both Transphorm devices display similar drain leakage currents and breakdown voltages in the region of 1850 V. GaN has a critical electric field of 3.3 MV [29]. This high critical electric field allows large avalanche breakdown voltages.

Each of the Transphorm devices tested had over a 250% greater breakdown voltage than the maximum V_{DS} value. The reason for this is in HEMT devices it is not the semiconductor that limits the voltage blocking capability. Indeed, HEMT devices do not fail by avalanche induced breakdown. Instead, they primarily fail because of Time Dependent Dielectric Breakdown (TDDB) [30]. Transphorm have, therefore, designed these devices to withstand three times the amount of rated V_{ds} so to ensure that premature device failures because of dielectric breakdown will not occur under normal operating conditions [31]. However, motivation for this over-engineering may possibly be the need to pass the reliability tests.

IV. Further Considerations for Industrial Applications

The Si S-J has been proven to be reliable, cost effective and efficient. This has yet to be confirmed for WBG devices. In addition, WBG devices experience different failure modes in comparison to Silicon ones. Current reliability validation is performed through avalanche specific tests. As mentioned before, GaN devices experience dielectric breakdown. Therefore, application relevant testing approaches have been suggested by [32] to provide greater indications of device performance. That being said, the static characterization that is reported in this paper provides an indication about how the performance of the devices and how technologies compare. It also highlights potential issues and limitations. Understanding and determining those performance limits, is essential for the design of efficient and reliable converters.

Due to the characteristics of E-mode GaN HEMTs, specialized gate drivers and careful drive techniques need to be utilized when they are included in a system. As of yet these specialized gate drivers have not been proven to be reliable. Texas Instrument's LM5114 gate driver is designed to drive individual GaN devices but it cannot provide signal isolation [33]. Fig 13 displays the topology for a simple boost converter using a LM5114 Single 7.6-A peak current low-side gate driver. The GIT device is highly susceptible to the noise induced by the system's parasitics. The consequences of this scenario may produce catastrophic results unless steps are taken to minimize the effect of this parasitic interference. For example, efficient design for the PCB layout can be performed in which the inductance and distance between the GIT and the driver is minimal.

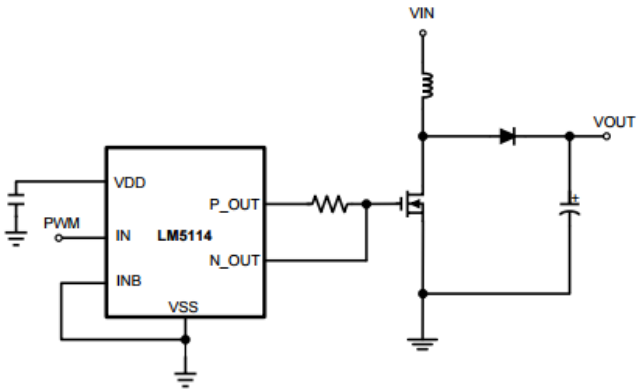

Fig. 13. Topology For a Simple Boost Converter Using an LM5114 Single 7.6-A Peak Current Low-Side Gate Driver [34]

In contrast, D-mode GaN cascode HEMTs do not need specialized gate drivers because they are driven by traditional Si FET technology. However, although the GaN cascode HEMT only requires traditional Si gate drivers the device experiences insufficient slew control. In addition, the LV Si MOSFET faces avalanche failure due to the static voltage sharing [35]. Low avalanching voltages could be solved by replacing the LV Si MOSFET with a HV Si MOSFET. However, a HV Si MOSFET would increase the specific R_{on}-I_{ds} for the device and increase the power loss of this device. In addition, would require the GaN's gate-source capabilities to be raised accordingly.

Also it should be noted that due to the high frequency capabilities of GaN devices and large stray inductance present in the package of GaN devices, there is extreme challenge in the optimal package configuration. These stray inductances in traditional device packages such as the TO-220 have prevented the exploitation of the full switching capability of GaN devices. The stray inductances also increase the losses in dynamic operations because of the increased switching times [36].

Therefore, GaN device manufacturers are packaging GaN-on-Si in low inductance or optimized package configurations. Transphorm have taken special consideration in designing devices with effective terminal configurations. For TO-220 packages the terminal layout is Gate-Source-Drain (GSD) as opposed to the conventional Gate-Drain-Source (GDS) power terminal layout. The terminal configuration is designed to minimize the Gate-Source driving loop parasitic inductance and to isolate the driving loop from the power loop, minimizing noise [37].

V. CONCULSIONS AND FUTURE WORK

In this paper, the static performance at 300 K of commercial GaN-on-Si devices was determined experimentally. Two different GaN-on-Si technologies, the E-mode GIT from Panasonic and D-mode cascaded HEMT from Transphorm, were characterized and benchmarked against a Si S-J MOSFET.

Experimental results in this paper have demonstrated a high variation in the performance of the Transphorm devices compared to their respective datasheets. Further, the Transphorm devices did not break until about 1850 V, despite being rated at 600 V. This corresponds to approximately 250% over-engineering on this device's maximum voltage rating.

Comparing the GaN-on-Si devices, the Panasonic PGA26C09DV has a lower leakage current for voltages up to 600V, where the breakdown was observed as expected. The C-V measurements indicated that the Panasonic device is faster, which can be expected, being a purely GaN based device compared to the cascade configuration. The Panasonic GIT also featured a lower R_{ON} too. However, the Transform device has a higher threshold voltage, which is desirable. In relation to the Si S-J, both GaN-on-Si technologies displayed impressive results. The GaN GIT device, outperformed the Si S-J in terms of R_{ON} and displayed interesting I-V characteristics. The two Transphorm devices also performed respectively well, with the TPH3206PD displaying similar R_{ON} values. The Si S-J displayed lower leakage currents than the both the GaN-on-Si technologies at 300 K. This however, may change with higher operation temperatures, as GaN has a wider band gap energy. High temperature static measurements will therefore, be need to assess the performance of these devices.

Each device presents unique advantages that suit different applications. It can be concluded that the Panasonic device is more suited to applications where switching and efficiency are high priorities. On the other hand, Transphorm devices suit applications where spike voltages and greater gate control is desired. It should also be stated that although GaN-on-Si offers unmatched performance capabilities, modern Si S-J MOSFETs are still competitive and capable of outperforming GaN technology in certain properties.

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