Endurance improvement of more than five orders in Ge_xSe_{1-x} OTS selectors by using a novel refreshing program scheme

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Abstract -- Selector device is critical in high-density cross-point resistive switching memory arrays for suppressing the sneak leakage current path. Ge_xSe_{1-x} based ovonic threshold switch (OTS) selectors have recently demonstrated strong performance with high on-state current, nonlinearity and endurance. Detailed study of its reliability is still lacking and the understanding on the responsible mechanisms is limited. *In this work, for the first time, the endurance degradation mechanism of Ge-rich* Ge_xSe_{1-x} *OTS is identified. Accumulation of slow defects that remain delocalized at off-state and GeSe segregation/crystallization during cycling lead to the recoverable and non-recoverable leakage current, respectively.* ***Most importantly,*** *a refreshing program scheme is developed to recover and prevent the OTS degradation and the endurance can be therefore improved by more than five orders without adding additional material elements or process steps.*

I. Introduction

Selector device is the key element for high-density storage class memory (SCM) using resistive switching device in a large 1S1R cross-point array to suppress the sneak leakage paths [1-4] (Fig.1a &b). Ge_xSe_{1-x} selector devices have been reported recently with high on-state current density, thermal stability, endurance, and low off-state leakage current [5-8]. We have also reported on its switching and relaxation mechanisms with both atomistic simulation and experimental evidence [7-10]. Detailed study on its reliability and degradation mechanisms is still lacking, and the understanding is limited, such as on the increase of leakage current in endurance tests [8,11]. ***In this work****, for the first time, an overall picture is obtained for the defects and mechanisms responsible for switching, relaxation and endurance degradation in Ge-rich* Ge_xSe_{1-x} *OTS selector. The accumulation of slow defects that remain delocalized at off-state and the GeSe segregation/crystallization during cycling lead to recoverable and non-recoverable leakage current increase, respectively.* ***Most importantly,*** *based on this understanding, an optimal refreshing program scheme using the reverse pulse or at higher temperatures is developed to recover and prevent the OTS degradation, and the endurance can be improved by more than five orders without adding additional material elements or process steps (Fig.18).*

II. Device and switching/relaxation mechanism

Devices used: Amorphous Ge_xSe_{1-x} films are prepared by room temperature physical vapor deposition (PVD) (Fig.2a) [7-8]. TiN/ Ge_xSe_{1-x}/TiN selector device (x=40%) is integrated in a 300 mm process flow, using a pillar (TiN) bottom electrode that defines the device size down to 50 nm. A Ge_xSe_{1-x} chalcogenide films control from 20 nm down to 5 nm thickness was achieved and passivated with a low-temperature BEOL process. A triangle pulse is used to record the bias and current during the switching (Fig.2b&c).

Switching mechanism: As reported in our previous atomistic simulation and experiment work [9-10], OTS volatile switching in Ge-rich Ge_xSe_{1-x} is based on the modulation of electronic structure of mis-coordinated amorphous Ge-Ge bonds as tail states (Fig.3a). In this work, *ab initio* calculation reveals that the high electric field at V_{th} and the charge injection to CB lead to the Ge-Ge bond over-coordinated, thus transitioned from the ground state to the excited state (Fig.3b) with a much reduced mobility gap (Fig.4a). This is equivalent to delocalization in space and reduction of energy level as illustrated in Fig.4b, so that a conductive percolation filament is formed and can be retained at the low E_{on}, allowing a high I_{on}. Vice versa for the switch-off when E_{on} is further reduced to V_{hd}, where fast defect localization leads to a much weaker filament and much smaller I_{off} [9,10]. The filamentary switching in OTS is supported by the area-independence of both on and off currents [9,10] and the stochastic Weibull distributions of t-on & t-off [10].

Relaxation at off-state was also observed [10]. In this work, we report, for the first time, that after the switching-off, V_{th} gradually increases with the OTS floating time and eventually returns to the value of the first-fire (FF) voltage (V_{FF}) in a fresh OTS after a long relaxation period (Fig.5a). This complete V_{th} relaxation is caused by the localization of ALL slow delocalized defects that remained in the filament at switch-off, as illustrated in Fig.5b.

III. Endurance degradation and the mechanism

***I_{leak}* increase with cycling** is observed at off-state during the endurance test (Fig.6a), which overwhelms the characteristics of OTS switching eventually after 1M cycles. This is confirmed by the DC I-V measured at off-state (Fig.6b), as I_{leak} is very low in a fresh device and increases after the FF, and it keeps increasing during the cycling. The I_{leak} increase is found insensitive to pulse amplitudes (Fig.7a) and durations (Fig.7b), suggesting that the degradation is mainly dependent on the number of switch cycles.

Excitation energy (Ea) of off-state current is measured to further investigate the mechanisms using the Arrhenius plot. Ea at off-state both in a fresh device and after FF (Fig. 8a @1V) and at on-state (Fig. 8b @3V) are measured and compared in Fig. 8c. Ea reduces from 0.43 eV in a fresh device to 0.3 eV after the FF, and to -0.005 eV at on-state. This can be explained by the switching and relaxation process (Fig.9a-c). The defects in a fresh device are localized and at above the electrode's Fermi level with a high energy barrier of 0.43 eV, leading to very low leakage via Poole-Frenkel tunneling. When they are delocalized at switch-on, a filament is formed with ohmic-like conduction via defect-to-defect (DTD) tunneling. Once the bias is further reduced to reach V_{hd}, the fast defects are localized during switch-off, but the slow defects remain delocalized and retain a weaker filament and I_{off} at off-state, which is due to a DTD energy barrier (Ea = 0.3 eV) higher than that at on-state, caused by the larger distance between these slow defects remaining in the filament.

During cycling, Ea of I_{leak} reduces gradually from 0.3 eV to 0.05 eV, while I_{leak} increases and V_{th} reduces (Figs.10a-b). It may be explained by the accumulation of additional defects (Fig.10c),

i.e., the number of slow defects that remain delocalized at off-state increases during cycling, leading to the lower tunneling barriers between defects, hence I_{leak} increases and V_{th} reduces. Based on this understanding/presumption, novel recovery methods will be explored in attempt to localize these additional slow defects either by a reverse-bias pulse or at a higher temperature, which may facilitate the OTS recovery, as investigated in detail below.

IV. Endurance recovery and degradation mechanism

Recovery methods: (a) One reverse-bias pulse is applied to each OTS, after 1k, 100k, and 1M cycles, respectively (**Fig.11a-d**). There is a small I_{leak} increase observed in the OTS after 1k cycles, as also confirmed by DC measurement (**Fig.11e**), and the reverse pulse can recover both V_{th} and I_{leak} to the value before the cycling, agreeing with that in the relaxation test without cycling (**Fig.5**), supporting that additional delocalized slow defects accumulated during cycling are localized (**Fig.10**). In the OTS after 100k cycles, I_{leak} increases clearly, and the reverse pulse can only partially recover the device. In OTS after 1M cycles, however, I_{leak} increase is prominent and OTS cannot be recovered by one reverse pulse. ***(b) Higher temperature*** at 125ºC to 250ºC can also reduce I_{leak} after 6k cycles (**Fig.12**), but it needs 8 hours at above 200ºC to recover the OTS. The above recovery results are, to certain extent, similar to the relaxation behavior observed in OTS device without cycling (**Fig.13a&b**), where the reverse bias and higher temperatures can also accelerate the localization-induced relaxation, leading to the higher V_{th} in the subsequent switch-on. This suggests that the localization of the slow defects contributes to both the OTS recovery in early cycles and the relaxation after a single switching event. The non-recoverable degradation in later cycles (**Fig.11c&d**), however, needs to be further examined.

Mechanism of non-recoverable degradation: TEM of the OTS before and after 1M cycles are compared in **Fig.14 (a-b)**. The fresh OTS device has uniform and amorphous Ge_xSe_{1-x} layer but it becomes non-uniform, partially crystalized and porous after 1M cycles showing element segregation in the chalcogenide layer, which may lead to the non-recoverable I_{leak} [11].

To further clarify the root cause of non-recoverable I_{leak} degradation, TEM of two OTS devices at different cycles after applying one reverse pulse in each device are compared in **Fig.15 (a-b)**. In the OTS after 5k cycles followed by a reverse pulse, the Ge_xSe_{1-x} layer is amorphous and the OTS is recoverable (**Fig.15a**), suggesting the localization of slow defects dominates the recovery. This is further supported by the observation that the I_{leak} and V_{th} of OTS after 4k cycles can fully recover to the I_{off} and V_{FF} of a fresh device after floating for 40 days (**Fig.16a-b**), similar to that of the long relaxation, confirming that the recovery is also originated from the localization of the accumulated slow defects (**Fig.16e**).

In OTS after 1M cycles followed by one reverse pulse (**Fig.15b**), Ge_xSe_{1-x} layer is similar to that without applying the reverse pulse (**Fig.14b**), and it is partially crystallized with high Ge content at the bottom, leading to non-recoverable OTS degradation. This is confirmed in **Fig.16c-d**, as the OTS after 1M cycles cannot be recovered after floating for 45days, supporting GeSe segregation /crystallization is the main cause of degradation (**Fig.16e**).

V. Optimal refreshing scheme for endurance improvement

Optimal refreshing pulse conditions are investigated to improve the endurance performance. The ratio of forward switching and reverse recovery pulses is an important criterion, as the selector needs to be switched on/off during the read operations, which occurs more often than the write/erase of the RRAM. It is found a ratio of 5k:1 between the forward and reverse pulses is optimal for avoiding excessive I_{leak} (**Fig.17a**). This is confirmed by the TEM (**Fig.15c**), as Ge_xSe_{1-x} layer remain amorphous after 1M cycles with the negative pulses applied in every 5k cycles, suppressing the excessive I_{leak}. A reverse bias higher than -5 V will lead to additional I_{leak} increase (**Fig.17b**), hence -4 V is chosen to minimize the advert degradation effects.

Endurance improvement: OTS endurance can be improved by more than five orders after inserting a reverse recovery pulse of -4 V for every 5k cycles of forward switching at 5 V at room temperature (**Fig.18**). This reverse pulse refreshing scheme combined with switching cycling at 125ºC can further improve the endurance by more than six orders to reach beyond 10^{10} cycles (limited by test instrument), thanks to the combined recovery effects of the reverse pulse and a higher temperature, making it well suitable for embedded applications. *It should be emphasized that this significant endurance improvement has been achieved without adding any additional material elements or process steps.*

Mechanism of preventing degradation: Non-recoverable degradation can be attributed to ionic movements of Ge and Se towards opposite directions under the forward switching pulse [12,13]. The ionic movements can aggregate and eventually lead to GeSe segregation and crystallization after a large number of switching cycles (**Fig.16e**). A reverse pulse in every 5k cycles can push these ions back and stop its aggregation, which is similar to that observed in PCRAM devices [12,13]. Ti contamination in the chalcogenide layer has also been observed in OTS endurance tests and attributed as the cause of degradation [11]. Ti has also been observed in the devices in this work after 1M cycles both with and without applying the refreshing scheme, hence its role for causing degradation may not be dominant and needs further investigation. It should also be noted that the full applicability of this work to other OTS materials is to be further examined in future work.

VI. Conclusions

Endurance recovery and degradation mechanism of Ge-rich Ge_xSe_{1-x} OTS is investigated. For the first time, the accumulation of delocalized slow defects & GeSe segregation/crystallization are identified as causes for recoverable and non-recoverable leakage current increase at off-state during the cycling, respectively. Most importantly, based on this understanding, it is found that the slow defects can be localized to recover the OTS by either a reverse pulse or at higher temperature, and the GeSe segregation/ crystallization can be prevented by inserting a reverse pulse in every 5k cycles. An optimal refreshing scheme is designed that can improve the endurance by more than five orders at room temperature. It can be further improved to more than six orders at 125ºC, without adding additional elements or process steps.

Reference

[1] G. W. Burr, J. Vac. Sci. Technol., 2014; [2] L. Zhang, et al, IEDM 2014; [3] W. Chen, et al, EDL, 2016; [4] Jo et al, IEDM 2014; [5] H.Y. Cheng, et al, IEDM 2017; [6] Y. Koo, et al, VLSI 2016; [7] B. Govoreanu, et al, VLSI 2017; [8] N. S. Avasarala, et al, VLSI 2018; [9] S. Clima, et al, IEDM 2017; [10] Z. Chai et al, VLSI 2019. [11] A. Verdy et al, IRPS 2018. [12] S Nam et al, ESS Letters 2009. [13] L. Goux et al, TED 2009.

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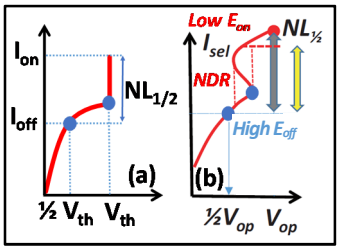


Fig.1 (a) Selectors must have high I_{on} and I_{on}/I_{off} ratio (non-linearity, $NL_{1/2}$). (b) Its negative differential resistance (NDR) leads to high E_{off} and low E_{on} in OTS when it is in series with a resistive-switching device (voltage-divider rule).

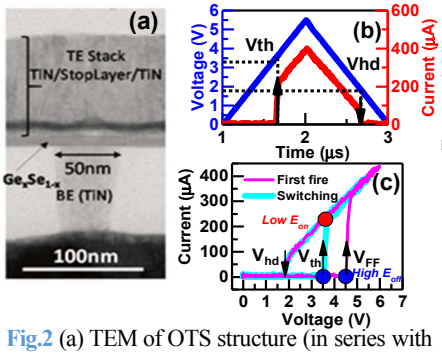


Fig.2 (a) TEM of OTS structure (in series with a resistor R=13kΩ). (b) Triangle voltage pulse & I-t. (c) I-V of volatile switching (1S1R).

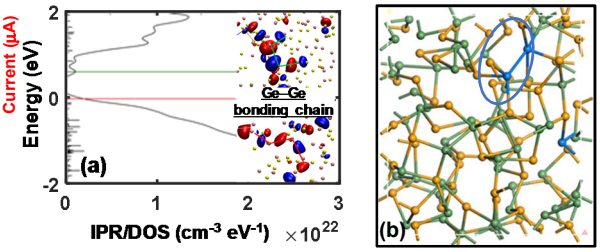


Fig.3 (a) Simulation of mobility gap tail states formed by Ge-Ge bonds and the consequential defect chain at conduction/valence band edges [9]. (b) Atomic calculation with *ab initio* molecular dynamics shows Ge-Ge (●) enters the "excited" state at high field upon charge injection, which cause over-coordinated Ge-Ge bond (●), acquires a narrower mobility band gap (as shown in Fig.4a).

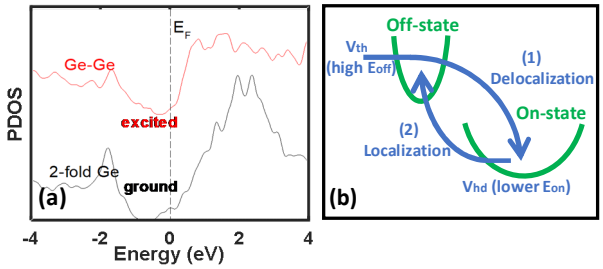


Fig.4 (a) *ab initio* molecular dynamics calculations show that the "excited" Ge-Ge bond acquires a much narrower mobility gap, equivalent to (b) defect delocalization at V_{th} (high E_{off}), as transition -ed to a larger defect physical size and lower energy level, and the opposite localization at V_{hd} (further decreased E_{on}). This type of illustration will be used in Figs.9 &10 for easier demonstration.

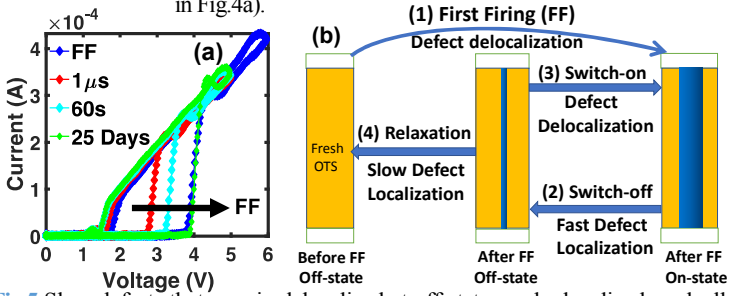


Fig.5 Slow defects that remain delocalized at off-state can be localized gradually during relaxation, and become fully localized eventually, returning to fresh OTS device after a long period, so that the V_{th} value return to V_{FF}. (b) Illustration of filament formation/enhancement/weakening process during (1) FF, (2) switch–off, (3) switch-on, and (4) relaxation towards fresh state in OTS.

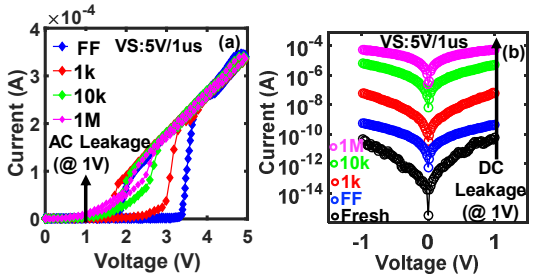


Fig.6 (a) Observation of the leakage current increasing during AC cycling. Volatile switching (VS) is entirely overwhelmed by I_{leak} after 1M cycles. (b) I_{leak} increase with cycling is confirmed by DC I-V measurement.

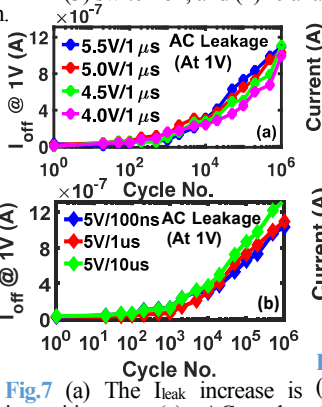


Fig.7 (a) The I_{leak} increase is insensitive to (a) AC pulse amplitudes and (b) durations.

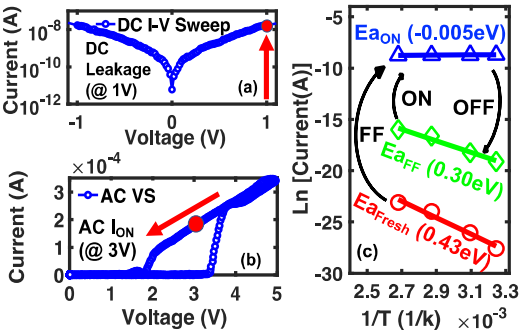


Fig.8 (a) DC Off-state current is measured at 1 V. (b) AC on-state current is measured at 3 V during down-sweep (c) ***Ea*** is measured by the Arrhenius plot in fresh device, after FF, and at on-state, respectively.

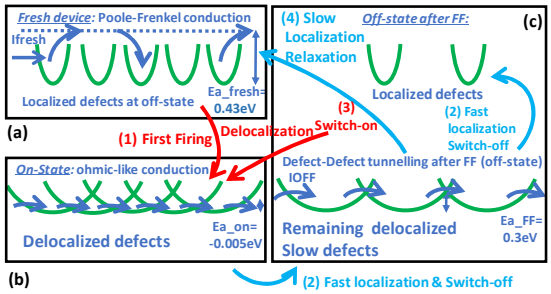
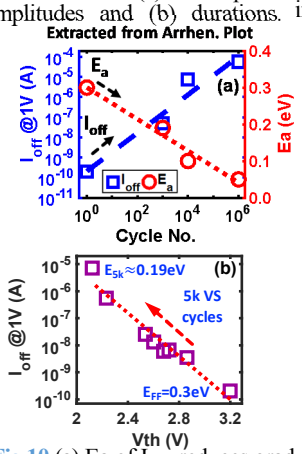


Fig.9 Illustration of the switching and relaxation process. (a) a very small off-state current in a fresh device. (b) high on-state current after FF (1) and switch-on (3) due to filament formation/enhancement. (c) the larger off-state current after switch-off than that in the fresh OTS is due to the remaining delocalized slow defects in the filament. Fast and slow defect localization lead to switch-off (2) and relaxation (4), respectively.



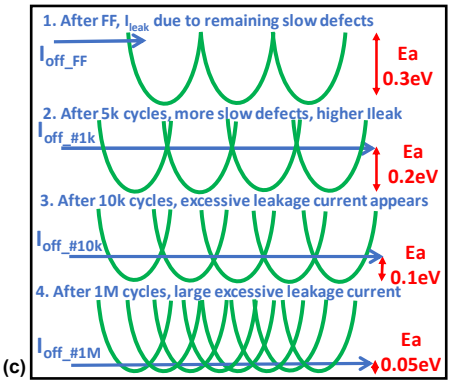


Fig.10 (a) Ea of I_{leak} reduces gradually during cycling, associated with I_{leak} increase. (b) Correlation between V_{th} reduction, Ea reduction, and the I_{leak} increase within 5k cycles. (c) This may be explained by the gradual accumulation of additional slow defects remaining delocalized at off-state during cycling, leading to the shorter distance and lower tunneling barriers between defects and hence the higher I_{leak} and lower V_{th} in following switching.

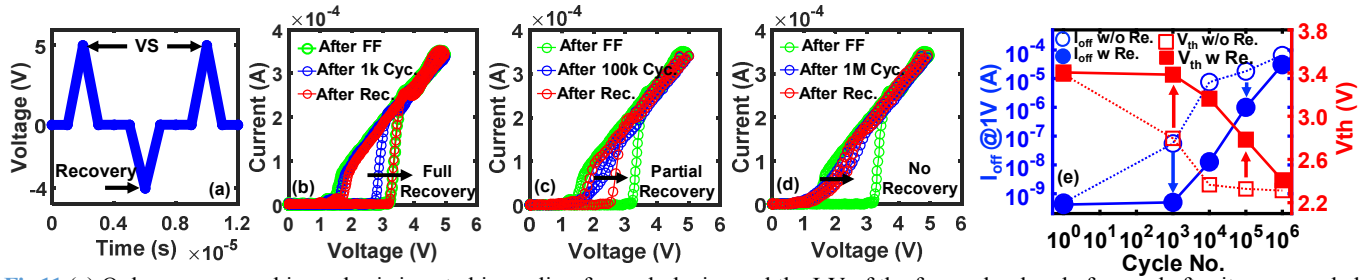


Fig.11 (a) Only one reverse-bias pulse is inserted in cycling for each device and the I-V of the forward pulses before and after it are recorded and compared. (b) Small I_{leak} increase is observed after 1k cycles, and the reverse pulse recovers V_{th} and I_{off} to that before the cycling, shown in (e). (c) For 100k cycles, I_{leak} increases clearly, and the reverse pulse can only partially recover OTS. (d) For 1M cycles, however, I_{leak} increase is prominent and OTS cannot be recovered by one reverse pulse. (e) Comparison of V_{th} and I_{leak} in (b-d) by DC measurement before and after the reverse pulse.

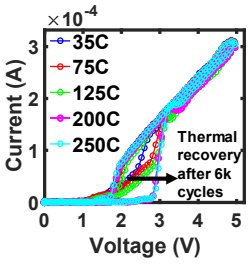
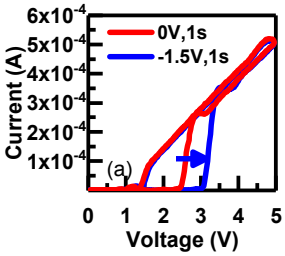


Fig.12 HT: 75ºC to 250ºC can reduce I_{leak} after 6k cycles, but it needs 8 hours at above 200ºC to recover the OTS.



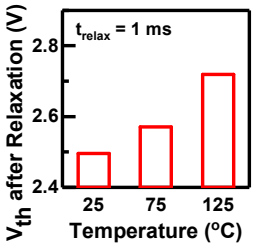


Fig.13 The V_{th} relaxation of OTS after a single switching (floating at off-state without cycling) can also be accelerated by both (a) reverse bias, and (b) higher temperature.

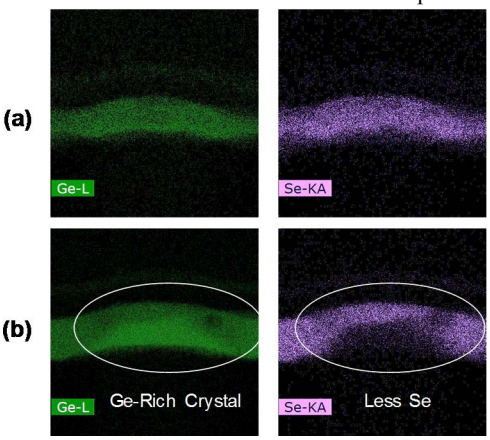


Fig.14 TEM of OTS before and after 1M cycles without applying the reverse pulse. (a) Uniform, amorphous Ge_xSe_{1-x} layer in fresh devices (above). (b) It becomes non-uniform, partially crystallized and porous in cycled device with Ge-Se segregation (below).

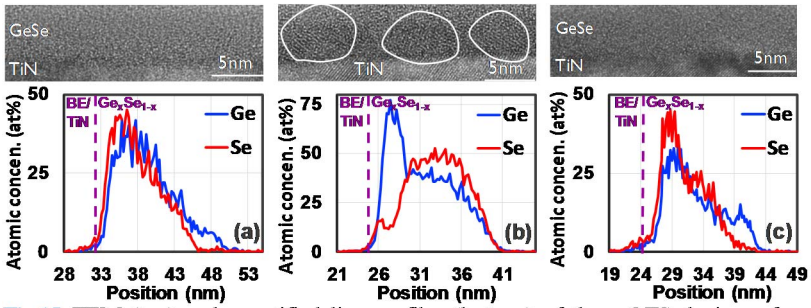


Fig.15 TEM (top) and quantified line profiles (bottom) of three OTS devices after applying reverse recovery pulse. (a) OTS after 5k cycles followed by one reverse pulse (left), corresponding to Fig.11(b). GeSe layer is mainly amorphous but less uniform, the OTS is recovered. (b) OTS after 1M cycles followed by one reverse pulse (middle), corresponding to Fig.11(d). GeSe layer is partial crystalline with high Ge content at bottom, similar to Fig.14(b). OTS cannot be recovered. (c) OTS after reverse pulse is applied in every 5k cycles for 1M cycles in total (right). GeSe layer is mainly amorphous but less uniform, similar to Fig. 15(a). OTS is recovered and the degradation is prevented.

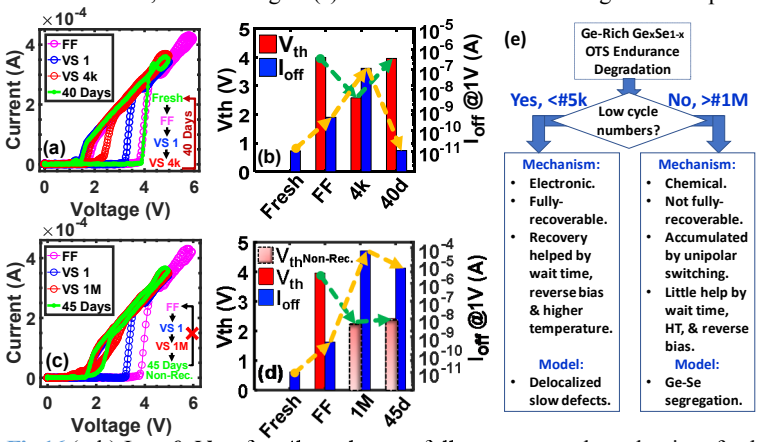


Fig.16 (a-b) I_{leak} & V_{th} after 4k cycles can fully recover to the value in a fresh device after floating for 40 days, but (c-d) it cannot recover after 1M cycles.(e) Illustration of the recovery mechanism due to localization of slow defects in (a-b) in early cycles and unrecoverable degradation mechanism in (c-d) after 1M cycles due to GeSe segregation and material crystallization, respectively.

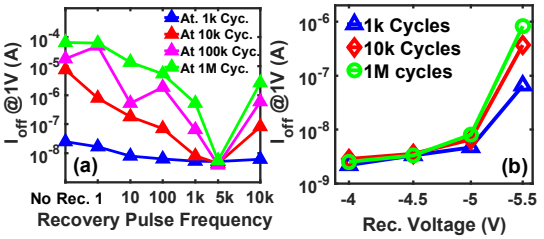


Fig.17 Leakage current with different recovery pulse conditions (a) with different ratios between forward-switching and reverse-recovery pulses. (b) with different reverse pulse amplitudes. The -4V/1us reverse pulse in every 5k forward-bias volatile switching cycles (5V/1us) provide the minimum degradation for up to 1M cycles.

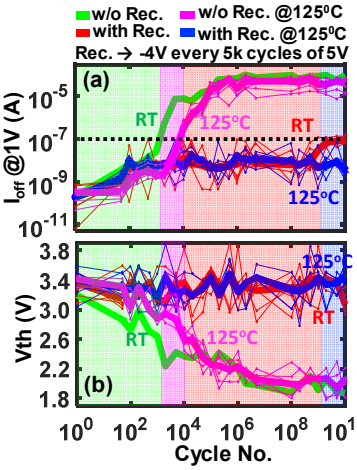


Fig.18 Comparison of (a) DC I_{leak} and (b) V_{th} during cycling without recovery vs. with the optimal recovery scheme, and at RT vs 125ºC. The OTS endurance improves by more than five orders at RT, and operates without degradation for 10^9 cycles. At 125ºC, the OTS operates with no degradation beyond 10^{10} cycles (instrument limit). V_{th} is measured at 100 µA. I_{off}=10^{-7}A (@1V) is used as the criterion of degradation. The max. I_{off} is limited by R_{series}.