This is the author's version of an article that has been published in this journal. Changes were made to this version by the publisher prior to publication. The final version is available at http://dx.doi.org/10.1109/TMTT.2019.2914106

Analog Gross Fault Identification in RF Circuits using Neural Models and Constrained Parameter Extraction

Andrés Viveros-Wacher, José E. Rayas-Sánchez, and Zabdiel Brito-Brito

***Abstract*— The demand and relevance of efficient analog fault diagnosis methods for modern RF and microwave integrated circuits increases with the growing need and complexity of analog and mixed-signal circuitry. The well-established digital fault diagnosis methods are insufficient for analog circuitry due to the intrinsic complexity in analog faults and their corresponding identification process. In this work, we present an artificial neural network (ANN) modeling approach to efficiently emulate the injection of analog faults in RF circuits. The resulting meta-model is used for fault identification by applying an optimization-based process using a constrained parameter extraction formulation. A generalized neural modeling formulation to include auxiliary measurements in the circuit is proposed. This generalized formulation significantly increases the uniqueness of the faults identification process. The proposed methodology is illustrated by two faulty analog circuits: a CMOS RF voltage amplifier and a reconfigurable bandpass microstrip filter.**

***Index Terms*— Analog faults, artificial neural network, gross faults, fault identification, fault injection, parameter extraction.**

I. Introduction

THE GROWING utilization of analog and mixed signal integrated circuits (IC) has increased the demand not only of fault tolerant techniques but also of fault detection and isolation [1]. While fault diagnosis techniques for digital circuits are mature and well established, those for analog circuits are still under development, facing significant technical challenges. This is mainly due to three key points [2]-[4]: a) there are not only two possible signal values, but in principle an infinite number of possible values; b) the timing characteristics of signals are not discrete, but continuous; and 3) the failure mode does not necessarily propagate to the output pins of the circuit.

Analog faults can be classified as catastrophic (or gross) faults and parametric (or soft) faults [5]. Gross faults are typically caused by structural deformities, such as open and short circuits, while parametric faults are generally caused by variations of component parameter values outside of their tolerance range. Prior work has used these two types of basic fault models and pursued a fault injection methodology to capture the circuit behavior under faulty conditions [5], [6].

Among machine learning techniques for knowledge-based fault diagnosis, those that exploit artificial neural networks (ANN) have become the most extensively used approaches for fault diagnosis of many types of systems, including analog circuits [7]-[12]. Machine learning-based techniques in current literature are mostly centered in trying to generate a fault dictionary to detect a predetermined k-number of faults [13], [14], extracting features from circuital measurements, and modeling a binary-encoded set of failure modes [15]-[17]. Most of this prior work focuses on the utilization of neural networks as classifiers, to distinguish between faulty and non-faulty responses [18]-[21]. Other works have used the wavelet transform in pre-processing methods to improve not only the detection but also the isolation of faults [22], [23], namely, the localization of the specific faulty circuit component. However, they require large and complex neural networks as well as significant pre-processing procedures to achieve the correct identification.

Optimization algorithms have also been extensively used in conjunction with neural networks for fault diagnosis, such as genetic algorithms [24]-[26], particle swarm optimization [27], [28], simulated annealing [29], and even hybrid methods [30] and other novel algorithms [31]. However, most of the prior work applies those algorithms to reduce the training time, to improve the accuracy of the model, or to efficiently select the input features to model, while still employing fault dictionaries as means of identifying faults within the circuit.

This paper proposes using a simple artificial neural network (classical 3-layer perceptron) to model the effects of injecting gross faults to the circuit under diagnosis. This neural model is used to learn the relationship between a faulty circuit set of responses (ANN outputs) and the origin of the failure (ANN inputs). Once the ANN is trained, it is used for fault identification and isolation through a simple yet efficient optimization process based on a constrained parameter extraction formulation, reproducing the faulty circuit responses by extracting by optimization the inputs of the already trained

Manuscript received Oct 31, 2018; revised March 25, 2019; accepted Month DD, YYYY.
This work was supported through a CONACYT scholarship (*Consejo Nacional de Ciencia y Tecnología,* Mexican Government).
This paper is an expanded version from the IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization, August 8–10, 2018, Reykjavik, Iceland.
(Corresponding author: J. E. Rayas-Sánchez.)
A. Viveros-Wacher is with Intel Corp., Zapopan, 45109 Mexico (e-mail: andres.viveros.wacher@intel.com).
J. E. Rayas-Sánchez and Z. Brito-Brito are with the Department of Electronics, Systems, and Informatics, ITESO – The Jesuit University of Guadalajara, Tlaquepaque, Jalisco, 45604 Mexico (e-mail: erayas@iteso.mx, zabdiel@iteso.mx).
Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.
Digital Object Identifier XXXXXXXXXXXXX

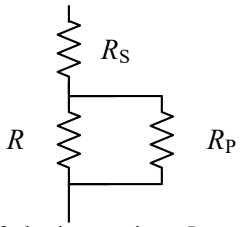

Fig. 1. Two possible faults in a resistor R: an open modeled with a resistance in series (R_S) or a short modeled with a resistance in parallel (R_P).

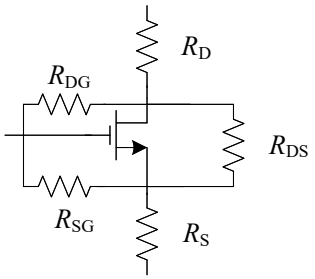

Fig. 2. Five possible faults in a transistor, modeled with opens on the drain (R_D) and source (R_S) terminals, and shorts between each pair of terminals (R_{DS}, R_{DG} and R_{SG}). Taken from [32].

ANN model. Our methodology is illustrated by a classical CMOS negative feedback RF voltage amplifier, as well as by a reconfigurable microstrip bandpass filter able to switch between WiFi and UMTS transmit band standards.

The present article expands our work in [32] by incorporating the following aspects: a) we make a more detailed review of the literature on machine learning techniques for analog fault identification; b) we present a more comprehensive description of analog fault models to further clarify the context of our contribution; c) we present a generalized formulation for our fault identification neural model, by incorporating auxiliary (internal) responses of the circuit under diagnosis, in order to improve the uniqueness of the predicted fault identification; and d) we include an additional RF and microwave circuit example, namely, a reconfigurable microstrip bandpass filter, to showcase the improved method for fault identification.

The rest of this paper is organized as follows: Section II describes the analog fault models used in this work. Section III describes the ANN-based fault modeling approach. Section IV presents the parameter extraction formulation for fault identification. Sections V and VI present the fault identification problem and results for two circuit examples. Finally, Section VII concludes our work.

II. Analog Fault Models

Analog fault models aim at exposing the circuit under diagnosis to: a) a catastrophic failure, where the circuit cannot operate; b) a performance degradation, where the circuit still works but the performance is lower than its specification; and c) an acceptable performance, despite having the faults. The classification of fault models can be composed of gross fault models, which emulate open and short circuits within the main circuit topology, and parametric fault models, which emulate a variation in a circuit component outside of its tolerable range.

In this work, we focus on employing gross fault models. Opens are modeled by using a high enough value of a serial ideal lumped resistance, while shorts are modeled by using a small enough value of a parallel ideal lumped resistance. Fig. 1 shows how fault models are employed within a resistor. A similar approach is followed when fault models are injected on any given circuit component with two terminals, such as capacitors, inductors or diodes. Fig. 2 shows how gross faults are injected in a transistor. An open fault is injected on each terminal (excepting the gate for the case of a CMOS transistor), while a short is injected between each pair of terminals. Given that the faults are analog, their values could take in theory an infinite number of possible values. However, a nominal value is chosen so that we guarantee that the desired effect is generated. In this work, the nominal values for the faults are in the order of MΩ for opens and mΩ for shorts.

We inject faults on each component of interest in a parametrized manner, in such a way that each fault can be individually activated and have a specific resistive value. When faults are not active, the value used for opens is in the order of mΩ and for shorts is in the order of MΩ. In this way, we guarantee that under no-fault conditions, the fault-injected circuit behaves as the original circuit.

III. Analog Faults Neural Modeling

A. Neural Model Formulation

We define the vector of ANN inputs, $\boldsymbol{x}$, as follows: x_1 represents the location of the fault, or in other words, the component where the fault is injected during simulation; x_2 represents the possible fault in each component: 1-2 for two-terminal components corresponding to R_S and R_P (see Fig. 1), or 1-5 for CMOS transistors corresponding to R_D, R_S, R_{DS}, R_{DG} and R_{SG} (see Fig. 2); and x_3 represents the amount of deviation from the nominal fault value. In this work, we employ a reduced range from −5% to +5% for x_3, which is a reasonable manufacturing tolerance. As an initial approach, we aim to neuro-model the behavior of the circuit when injecting a single fault at a time.

The output for the ANN model actually represents the deviation of the circuit responses from a no-failure condition. In [32], the identification of faults was achieved through observing the output responses of the circuit under test related to its main specifications (i.e., the responses of interest), and comparing them against those of a faultless scenario. However, a certain subset of faults can yield similar or even exactly the same output responses of the circuit. This directly impacts on the decision of our proposal to identify the fault, yielding to non-uniqueness issues in the extraction of the failure cause. To overcome this issue, in this work we propose the use of auxiliary responses other than those used as specified output responses. These auxiliary responses may include internal responses of the circuit (measured at topologically internal nodes, branches, or ports), or other overall performance metrics (input impedances, cutoff frequencies, etc.). These additional measurements are not directly related to the main

specifications of the circuit, but are extremely useful to uniquely identify the failing component in the circuit and its kind of failure. Moreover, obtaining these additional responses practically does not increase the overall computational cost, since no additional simulations are implied.

We aim to neuro-model a matrix of response deviations $\boldsymbol{R} \in \Re^{m\times n}$, where m is the number of simulated responses, including the output specification-related measurements, as well as the auxiliary internal measurements, and n is the number of components for a given response, e. g., the real and imaginary parts of the voltage gain of an amplifier, or the magnitude and phase of an S-parameter, etc. In this manner, the matrix of response deviations to be modeled is represented by

$$\boldsymbol{R} = \begin{bmatrix} \sum_i^N \left(\boldsymbol{R}_{11,i} - \boldsymbol{R}_{11,i}^{\mathrm{nf}} \right) & \cdots & \sum_i^N \left(\boldsymbol{R}_{1n,i} - \boldsymbol{R}_{1n,i}^{\mathrm{nf}} \right) \\ \vdots & \ddots & \vdots \\ \sum_i^N \left(\boldsymbol{R}_{m1,i} - \boldsymbol{R}_{m1,i}^{\mathrm{nf}} \right) & \cdots & \sum_i^N \left(\boldsymbol{R}_{mn,i} - \boldsymbol{R}_{mn,i}^{\mathrm{nf}} \right) \end{bmatrix} \quad (1)$$

where N is the number of frequency points at which the response is sampled, and $R^{\mathrm{nf}}{}_{mn}$ is the m,n^{th} response when no faults are injected.

B. ANN Characteristics and Training

As mentioned before, we select a simple 3-layer perceptron for the topology of our ANN. The ANN is implemented and trained using the Matlab neural network toolbox. We select the Bayesian regularization algorithm for training, and use 1,000 base points generated using the Sobol pseudo-random sequence to sample the selected solution space as uniformly as possible [33] but limiting the total amount of learning and testing data. Out of the total number of base points, 70% are selected for learning and 30% are selected for testing. The algorithm used for training increases the number of neurons in the hidden layer, h, until the generalization performance deteriorates (similarly to [34]), or until the learning and testing errors are below 1%,

$$\begin{aligned} &(e_{\mathrm{t\_old}} < e_{\mathrm{t\_new}} \wedge e_{\mathrm{t\_new}} > e_{\mathrm{l\_new}}) \vee \\ &(e_{\mathrm{t\_new}} < 1\% \wedge e_{\mathrm{l\_new}} < 1\%) \end{aligned} \quad (2)$$

where $e_{\mathrm{t\_old}}$ is the testing error at the previous iteration and $e_{\mathrm{t\_new}}$ and $e_{\mathrm{l\_new}}$ are the testing and learning errors, respectively, at the current iteration. Each error is calculated as the Frobenius norm of the difference between the ANN output and the circuit output. Once the ANN is trained, we test it using 100 extra base points not used during training. The output from the ANN model is compared against actual circuit simulated responses to calculate the model maximum relative error.

IV. Fault Identification by Parameter Extraction

Here we exploit parameter extraction (PE) as an optimization problem that aims at minimizing the difference between a target response and the system response being optimized [35]–[38]; in [35] it is explained how PE can be problematic and subject to multiple local minima. In our work, we aim at finding the input values $\boldsymbol{x}$ of the ANN model that minimize the difference between the actual deviated responses of a faulty circuit, calculated in (1) and treated as the target, and the ANN output. The optimization procedure is implemented by solving

$$\boldsymbol{z}^* = \arg\min_{\boldsymbol{z}} \left\| \boldsymbol{R}(\boldsymbol{z}) - \boldsymbol{R}^{\mathrm{t}} \right\|_1 \quad (3)$$

where $\boldsymbol{R}(\boldsymbol{z})$ is the ANN model output and $\boldsymbol{R}^{\mathrm{t}}$ is the target output. In our case, (3) is solved by using the Nelder-Mead method. The Manhattan norm used in (3) averages all errors across the frequency sweep; it can be replaced by the Huber formulation [39] in cases where both large and small differences between $\boldsymbol{R}(\boldsymbol{z})$ and $\boldsymbol{R}^{\mathrm{t}}$ appear throughout the frequency points, to further improve the PE solution. In order to keep $\boldsymbol{x}$, the ANN inputs, within feasible values during the optimization iterations, we use box constraints defined as

$$\boldsymbol{x} = \begin{bmatrix} x_1^{\mathrm{lb}} + \left(x_1^{\mathrm{ub}} - x_1^{\mathrm{lb}}\right)(\sin z_1)^2 \\ x_2^{\mathrm{lb}} + \left(x_2^{\mathrm{ub}} - x_2^{\mathrm{lb}}\right)(\sin z_2)^2 \\ \sin z_3 \end{bmatrix} \quad (4)$$

where $x_1{}^{\mathrm{lb}}$ and $x_1{}^{\mathrm{ub}}$ are the selected lower and upper values, respectively, corresponding to the minimum and maximum values of x_1 when the ANN was trained. Similarly, $x_2{}^{\mathrm{lb}}$ and $x_2{}^{\mathrm{ub}}$ correspond to the upper and lower values for x_2. Notice that the optimal values of x_1 and x_2 should be both integer numbers; however, we solve (3) by letting the optimization process to run on continuous values for z_1 and z_2, rounding to the nearest integer the optimal final values found for x_1 and x_2.

Given the typically expected high number of local minima, we use a statistical PE algorithm, where the starting point of the optimization procedure is slightly perturbed each time the normalized difference between the optimal ANN response and the target response is larger than a desired value, $\varepsilon_{\mathrm{PE}}$. In our case, the value selected is $\varepsilon_{\mathrm{PE}} = 10^{-5}$.

V. Example 1: CMOS Negative Feedback RF Voltage Amplifier

A. Circuit Description

The first circuit example to illustrate our fault injection and identification procedure is the classical CMOS negative feedback RF voltage amplifier depicted in Fig. 3, which uses an external series-parallel ideal feedback network formed by R_1 and R_2. Its nominal voltage gain is shown in Fig. 4.

B. Analog Faults Injected

We inject an open to the drain and source pins of each CMOS transistor, and a short between each pair of transistor nodes. When faults are not active, the value used for opens is 1 mΩ and for shorts is 200 MΩ. In this way, we guarantee that under no-fault conditions, the fault-injected circuit behaves as the original circuit, as it is confirmed in Fig. 4.

C. Faults Neural Model and Training

In this particular example, the matrix of response deviations $\boldsymbol{R} \in \Re^{1\times 2}$ for the neural model (ANN outputs), is defined as

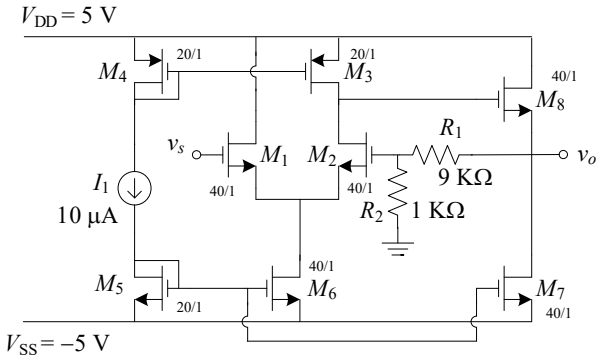

Fig. 3. Original CMOS negative feedback RF voltage amplifier. Taken from [32].

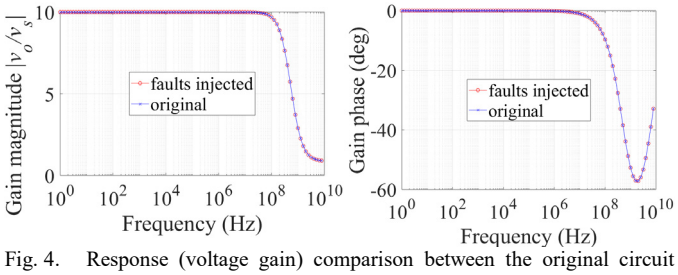

Fig. 4. Response (voltage gain) comparison between the original circuit and the fault-injected circuit with all faults inactive. Taken from [32].

$$\boldsymbol{R} = \left[\begin{array}{l} \sum_{i}^{N} \left(\mathrm{Re}\left\{ Av_i \right\} - \mathrm{Re}\left\{ Av_i^{\mathrm{nf}} \right\} \right) \\ \sum_{i}^{N} \left(\mathrm{Im}\left\{ Av_i \right\} - \mathrm{Im}\left\{ Av_i^{\mathrm{nf}} \right\} \right) \end{array} \right]^{\mathrm{T}} \quad (5)$$

where Av^{nf} is the complex amplifier voltage gain when no faults are injected, Av is the complex voltage gain with the injected fault, and N is the number of sampled frequency points. Following the ANN training algorithm described in Section III.B, the final value of the number of neurons in the hidden layer is h = 21, as seen in Fig. 5, and the maximum relative testing error measured with the 100 extra base points is 0.00635%.

D. Parameter Extraction to Faults Identification

To validate the effectiveness of our proposal, we select a random fault as target, and followed the PE procedure described in Section IV, where the values for upper and lower bounds for the box constraints in (4) are x_1^{lb} = 1 and x_1^{ub} = 8

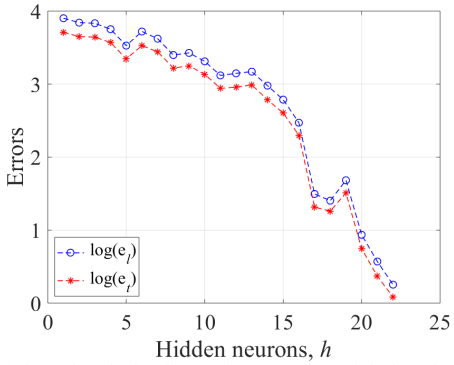

Fig. 5. Training the fault diagnosis neural model for the CMOS RF amplifier: ANN performance while increasing h, the number of neurons in the hidden layer. Taken from [32].

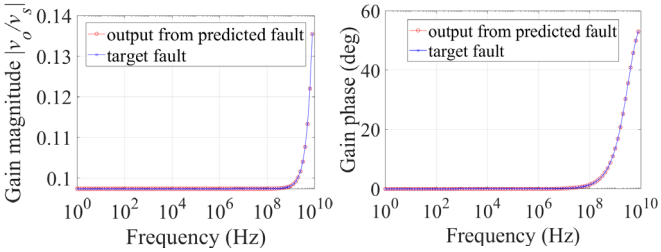

Fig. 6. Comparison between the circuit responses of the CMOS RF amplifier at a predicted fault and those at the actual fault injected (gain magnitude and phase). Taken from [32].

for x_1 and x_2^{lb} = 1 and x_2^{ub} = 5 for x_2 (see Fig. 3).

The values of $\boldsymbol{x}$ for the actual faults are [2 3 0.1498%]$^{\mathrm{T}}$. The resulting values of $\boldsymbol{x}$ match exactly on x_1 and x_2, thus the fault location within the circuit and the fault type (one out of five possible faults) are identified precisely on each case. There is, however, a slight variation between the predicted (0.02967%) and the actual value in the variable corresponding to the deviation from the nominal fault value, x_3. Nevertheless, the simulated responses from the circuit with the identified fault closely resemble the responses with the original injected fault, as shown in Fig. 6.

VI. Example 2: Reconfigurable Microstrip Bandpass Filter

A. Circuit Description

The second circuit example is a reconfigurable microstrip

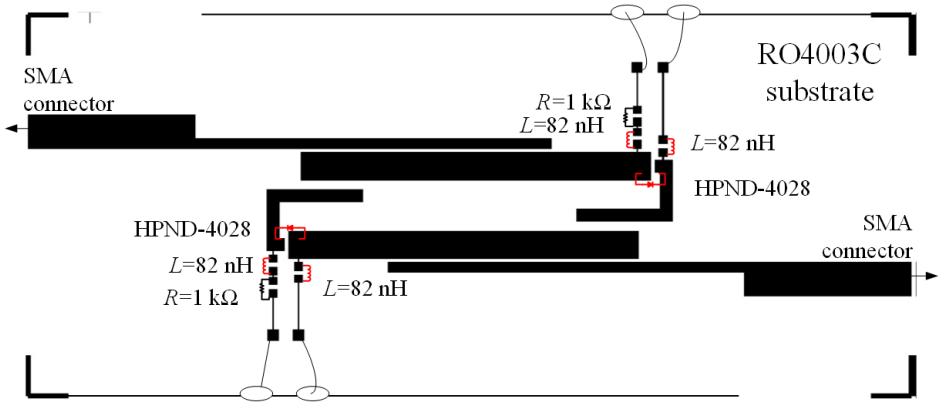

Fig. 7. Reconfigurable microstrip bandpass filter topology. Taken from [40]. Highlighting (in red) the components where faults are injected.

bandpass filter able to switch between WiFi and UMTS transmit band standards [40]. When in WiFi mode, the filter center frequency is 2.44 GHz with a bandwidth of 80 MHz, and in UMTS mode, the center frequency is 1.955 GHz with a 140 MHz bandwidth. The circuit is implemented in Keysight ADS making use of co-simulation. In other words, the EM simulation was performed beforehand in Momentum and its results are stored and used in ADS. As seen in Fig. 7, the circuit uses two PIN diodes to switch between WiFi and UMTS states and four RF choke inductors.

B. Analog Faults Injected

We inject an open fault model and a short fault model on each inductor and diode of the circuit in its UMTS state. In this example, each fault is also activated individually in a parametrized manner. When inactive, the open fault value is 1 mΩ and the short fault value is 1 MΩ. When all faults are inactive, the circuit behaves as the original circuit, as expected (see Fig. 8). The responses of interest of the circuit are the return loss (S_{11}) and the insertion loss (S_{21}).

C. Faults Neural Model and Training

The inputs selected for the ANN model are the fault location (x_1) from out of the 6 selected circuit elements, the fault type (x_2), meaning whether the injected fault is an open or a short, and the fault value (x_3) which relates to the deviation from the nominal value of the fault. The output for the ANN model is the deviation of the circuit responses from a no-fault condition. In this case, apart from using the return and insertion losses to calculate this deviation, we treat each fault location as a port, and use each S-parameter as auxiliary information to improve the uniqueness in identification process during the parameter extraction process. In order to insert a port on each fault location, the ADS schematic is modified in such a way that the actual inductors and diodes are removed, and the port is assigned a complex impedance corresponding to the impedance of the replaced circuit element, as shown in Fig. 9.

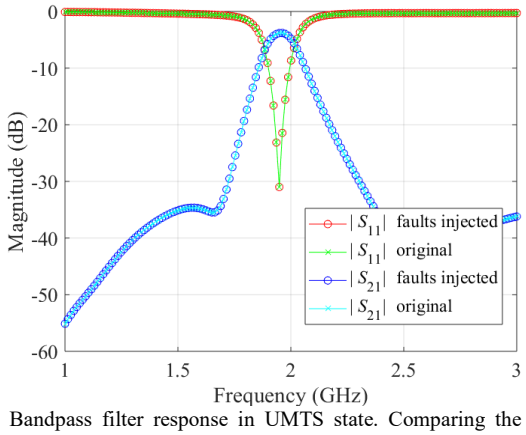

Fig. 8. Bandpass filter response in UMTS state. Comparing the original circuit and the fault-injected circuit with all faults inactive.

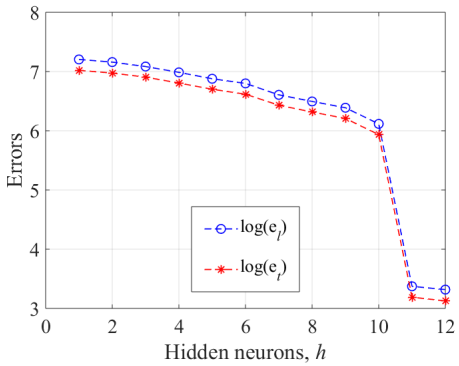

Fig. 10. Training the fault diagnosis neural model for the bandpass microstrip filter: ANN performance while increasing h, the number of neurons on the hidden layer.

In this case, the selected matrix of response deviations, $\boldsymbol{R} \in \Re^{64\times 2}$, includes the magnitude and phase of the 64 S-parameters for the complete circuit (S_{11}, S_{12}, …, S_{88}), as follows:

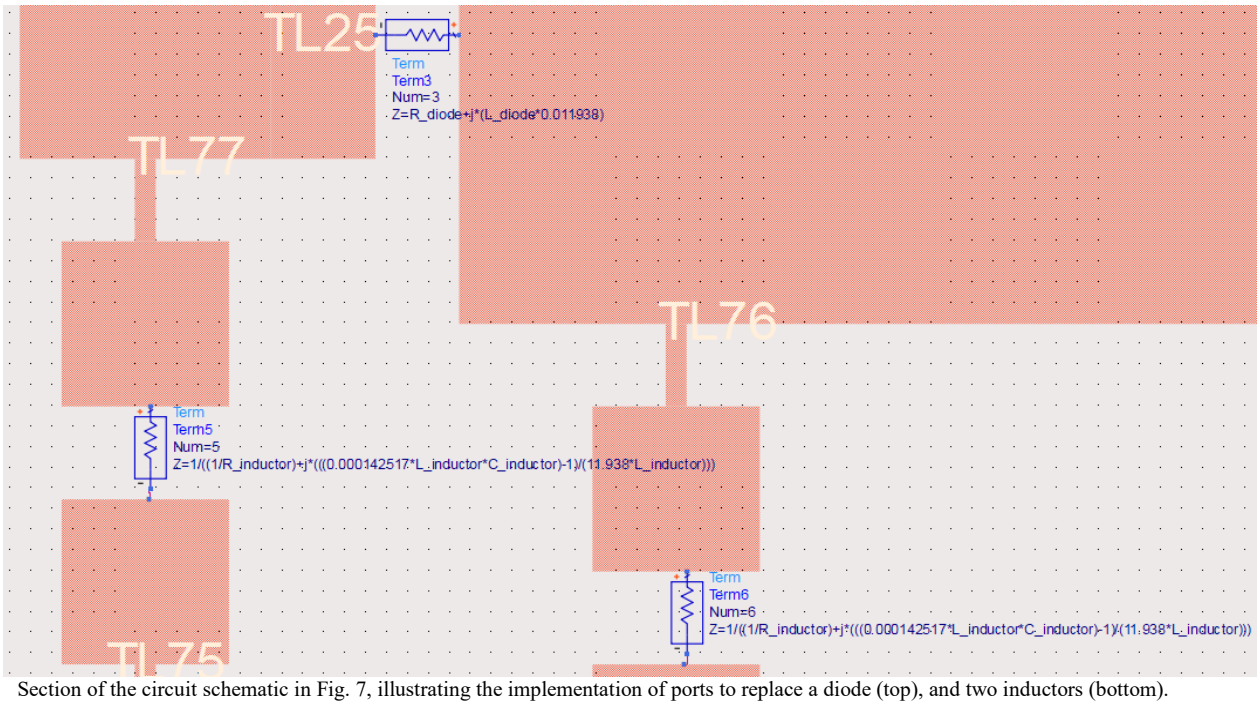

Fig. 9. Section of the circuit schematic in Fig. 7, illustrating the implementation of ports to replace a diode (top), and two inductors (bottom).

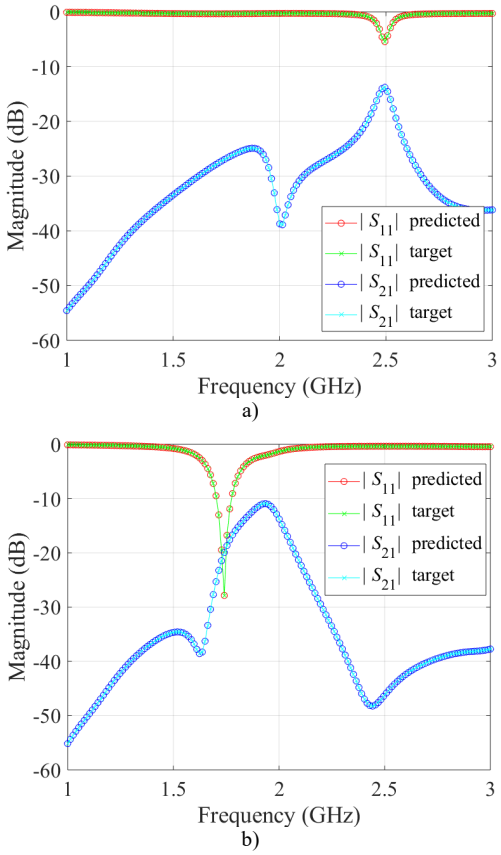

Fig. 11. Comparison between the circuit responses for the RF bandpass microstrip filter at predicted faults and those at: a) the first actual fault injected, and b) the second actual fault injected.

$$\boldsymbol{R} = \begin{bmatrix} \sum_{i}^{N}\left(\left|S_{11}\right| - \left|S_{11}^{\mathrm{nf}}\right|\right) & \sum_{i}^{N}\left(\arg\left(S_{11}\right) - \arg\left(S_{11}^{\mathrm{nf}}\right)\right) \\ \vdots & \vdots \\ \sum_{i}^{N}\left(\left|S_{88}\right| - \left|S_{88}^{\mathrm{nf}}\right|\right) & \sum_{i}^{N}\left(\arg\left(S_{88}\right) - \arg\left(S_{88}^{\mathrm{nf}}\right)\right) \end{bmatrix} \quad (6)$$

We also select a 3-layer perceptron for our ANN, and increase the number of neurons in the hidden layer, h, until the generalization performance deteriorates, or until the learning and testing errors are below 0.1%. In this example, the final value of h is 11, as seen in Fig. 10. The final performance of the ANN shows a maximum relative testing error of 0.007917%.

D. Parameter Extraction to Faults Identification

To validate our proposal, we select two random faults as targets (not seen during training). The values of $\boldsymbol{x}$ for the first actual fault are $[5\ \ 1\ \ 0.016231\%]^{\mathrm{T}}$ and the predicted fault, following the PE process, is $[5\ \ 1\ \ 0.0373\%]^{\mathrm{T}}$. As in the previous example, the fault type and location are accurately identified, with a small error in the actual variable deviation. Additionally, the simulated responses of the circuit with the predicted fault closely reproduce the responses with the actual fault, as confirmed in Fig. 11.a. As an additional validation point, we use a second actual fault at $\boldsymbol{x} = [3\ \ 2\ \ -0.05445\%]^{\mathrm{T}}$, for which the corresponding predicted fault, following the PE process, is $[3\ \ 2\ \ -0.02897\%]^{\mathrm{T}}$. Fig. 11.b shows the comparison between the circuit responses with the second target fault and the predicted fault. A similar performance was observed at other random faults testing points.

VII. Conclusions

An analog gross fault diagnosis method based on artificial neural networks (ANN) and constrained parameter extraction was proposed in this paper. It employs a generalized formulation to increase the uniqueness of the predicted faults, by incorporating auxiliary information from internal nodes within the circuit topology. Our method was illustrated by injecting analog gross faults in two circuit examples: a classical CMOS RF negative feedback amplifier and a reconfigurable bandpass microstrip filter. The gross faults were modeled as resistances with a high enough value in series to cause an open circuit and with a low enough value in parallel to cause a short circuit. The ANN was then used as a metamodel, with an extremely low computational cost, to automatically identify faults through a constrained statistical parameter extraction process. Following this process, we were able to properly identify the actual injected faults in both circuits.

References

[1] Z. Gao, C. Cecati, and S. X. Ding, "A survey of fault diagnosis and fault-tolerant techniques—Part I: Fault diagnosis with model-based and signal-based approaches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3757-3767, Jun. 2015.

[2] J. W. Bandler and A. E. Salama, "Fault diagnosis of analog circuits," *Proc. IEEE*, vol. 73, no. 8, pp. 1279-1325, Aug. 1985.

[3] P. Kabisatpathy, A. Barua, and S. Sinha, *Fault Diagnosis of Analog Integrated Circuits*, New York, NY: Springer, 2005.

[4] R. Liu, *Testing and Diagnosis of Analog Circuits and Systems*. New York: Van Nostrand Reinhold, 1991.

[5] D. Bhatta, I. Mukhopadhyay, S. Natarajan, P. Goteti, and B. Xue, "Framework for analog test coverage," in *Int. Symp. Quality Electronic Design* (*ISQED*), Santa Clara, CA, Mar. 2013, pp. 468-475.

[6] M. B. Yelten, S. Natarajan, B. Xue, and P. Goteti, "Scalable and efficient analog parametric fault identification," in *IEEE/ACM Int. Conf. Computer-Aided Design* (*ICCAD*), San Jose, CA, Nov. 2013, pp. 387-392.

[7] L. Chunlai, Z. Xianshuang, and Gudake, "A survey of online fault diagnosis for PV module based on BP neural network," in *Int. Conf. Smart City and Systems Engineering* (*ICSCSE*), Hunan, China, Nov. 2016, pp. 483-486.

[8] K. Madani, "A survey of artificial neural networks based fault detection and fault diagnosis techniques," in *Int. Joint Conf. Neural Networks* (*IJCNN*), Washington, DC, Jul. 1999, pp. 3442-3446.

[9] H. Ma, D. Xu, and Y-S. Lee, "Fault diagnosis of power electronic circuits based on neural network and waveform analysis," in *Proc. of the IEEE Int. Conf. Power Electronics and Drive Systems* (*PEDS-1999*), Hong Kong, Jul. 1999, pp. 234-237.

[10] S. Yang, W. Li, and C. Wang, "The intelligent fault diagnosis of wind turbine gearbox based on artificial neural network," in *Int. Conf. Condition Monitoring Diagnosis*, Beijing, Apr. 2008, pp. 1327-1330.

[11] H. A. Talebi and K. Khorasani, "A neural network-based actuator gain fault detection and isolation strategy for nonlinear systems," in *IEEE Conf. Decision Control*, New Orleans, LA, Dec. 2007, pp. 2614-2619.

[12] J-Z. He, Z-H. Zhou, X-R. Yin, and S-F. Chen, "Using neural networks for fault diagnosis," in *Proc. Int. Joint Conf. Neural Networks* (*IJCNN*), Como, Italy, Jul. 2000, pp. 217-220.

[13] Q. Haini, X. Weisheng and Y. Youling, "Design of neural network output layer in fault diagnosis of analog circuit," in *Int. Conf. Electronic*

Measurement Instruments, Xi'an, China, Aug. 2007, pp. 3-639-3-642.
[14] D. Ying and H. Yigang, "On the application of artificial neural networks to fault diagnosis in analog circuits with tolerances," in *Proc. Int. Conf. Signal Processing World Computer Cong.*, Beijing, China, Aug. 2000, pp. 1639-1642 vol.3.
[15] H. Yuan, G. Chen, S. Shi, and H. Chen, "Research on fault diagnosis in analog circuit based on wavelet-neural network," in *World Cong. Intelligent Control Automat.*, Dalian, China, Jun. 2006, pp. 2659-2662.
[16] B. Zhang, R. Xu, X. Yin and Z. Gao, "Research on fault diagnosis for rail vehicle compartment of LED lighting system of analog circuit based on WP-EE and BP neural network," in *Chinese Control Decision Conf. (CCDC)*, Yinchuan, China, May 2016, pp. 2989-2993.
[17] Z. Xue, Y. Li and Y. Cao, "Simulation of improved BP algorithm in the fault diagnosis of analog circuit," in *Int. Conf. Electrical and Control Eng.*, Yichang, China, Sept. 2011, pp. 3148-3150.
[18] S. Chakrabarty, V. Rajan, J. Ying, M. Mansjur, K. Pattipati, and S. Deb, "A virtual test-bench for analog circuit testability analysis and fault diagnosis," in *Proc. IEEE Syst. Readiness Tech. Conf. Test Technology for the 21st Century*, Salt Lake City, UT, Aug. 1998, pp. 337-352.
[19] D. Grzechca and J. Rutkowski, "Use of neural network and fuzzy logic to time domain analog tasting," in *Proc. Int. Conf. Neural Inform. Processing*, 2002. ICONIP '02, Nov. 2002, vol. 5, pp. 2601-2604.
[20] Z. R. Yang, M. Zwolinski, C. D. Chalk, and A. C. Williams, "Applying a robust heteroscedastic probabilistic neural network to analog fault detection and classification," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 142-151, Jan. 2000.
[21] V. Rajan, Jie Yang, S. Chakrabarty, and K. Pattipati, "Machine learning algorithms for fault diagnosis in analog circuits," in *IEEE Int. Conf. Syst., Man Cybernet.*, San Diego, CA, Oct. 1998, vol. 2, pp. 1874-1879.
[22] S. Guoming, L. Qi, L. Gang, J. Shuyan, and W. Houjun, "Analog circuit fault diagnosis using wavelet feature optimization approach," in *IEEE Int. Conf. Electronic Meas. & Instruments* (*ICEMI*), Qingdao, Jul. 2015, pp. 119-124.
[23] M. Li, Y. He, L. Yuan, and M. Li, "Fault diagnosis of analog circuit based on wavelet neural networks and chaos differential evolution algorithm," in *Int. Conf. Electrical and Control Eng.*, Wuhan, Nov. 2010, pp. 986-989.
[24] X. Li, Y. Zhang, S. Wang, and G. Zhai, "Analog circuits fault diagnosis by GA-RBF neural network and virtual instruments," in *Int. Symp. on Instrumentation & Measurement, Sensor Network and Automation (IMSNA)*, Sanya, China, Aug. 2012, pp. 236-239.
[25] G. Liang and Y. He, "A fault identification approach for analog circuits using fuzzy neural network mixed with genetic algorithms," in *Proc. IEEE Int. Conf. on Robotics, Intelligent Systems and Signal Processing*, Changsha, Hunan, China, Oct. 2003, pp. 1267-1272 vol.2.
[26] H. Li and Y. Zhang, "An algorithm of soft fault diagnosis for analog circuit based on the optimized SVM by GA," in *Int. Conf. Electronic Meas. & Instruments*, Beijing, China, Aug. 2009, pp. 4-1023-4-1027.
[27] J. Tang, Y. Shi and D. Jiang, "Analog Circuit Fault Diagnosis with Hybrid PSO-SVM," in *IEEE Circuits and Systems Int. Conf. Testing and Diagnosis*, Chengdu, China, Apr. 2009, pp. 1-5.
[28] Y. Ming, "Application of particle swarm optimization and RBF neural network in fault diagnosis of analogue circuits," in *Int. Symp. Intelligent Informat. Technol. Applic.*, Shanghai, China, Nov. 2009, pp. 176-178.
[29] D. Grzechca, "Simulated annealing with artificial neural network fitness function for ECG amplifier testing," in *European Conf. Circuit Theory and Design (ECCTD)*, Linkoping, Sweden, Aug. 2011, pp. 49-52.
[30] L. Haijun, F. Yao, X. Zhicheng and Z. Xuhui, "The study about feature selection of analog circuit fault diagnosis based on annealing genetic hybrid algorithm," in *Int. Forum Strategic Technology (IFOST)*, Tomsk, Russia, Sept. 2012, pp. 1-4.
[31] D. Binu and B. S. Kariyappa, "RideNN: a new rider optimization algorithm-based neural network for fault diagnosis in analog circuits," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 1, pp. 2-26, Jan 2019.
[32] A. Viveros-Wacher and J. E. Rayas-Sánchez, "Analog fault identification in RF circuits using artificial neural networks and constrained parameter extraction," in *IEEE MTT-S Int. Conf. Num. EM Mutiphysics Modeling Opt. (NEMO-2018)*, Reykjavik, Iceland, Aug. 2018, pp. 1-3.
[33] I. M. Sobol, "On the distribution of points in a cube and the approximate evaluation of integrals," *U.S.S.R. Computational Mathematics and Mathematical Physics*, vol. 7, pp. 86-112, 1967.
[34] J. E. Rayas-Sánchez and V. Gutiérrez-Ayala, "EM-based Monte Carlo analysis and yield prediction of microwave circuits using linear-input neural-output space mapping," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 12, pp. 4528-4537, Dec. 2006.
[35] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development and engineering applications," *IEEE Microw. Magazine*, vol. 17, no. 4, pp. 64-76, Apr. 2016.
[36] M. H. Bakr, J. W. Bandler, and N. Georgieva, "An aggressive approach to parameter extraction," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 12, pp. 2428-2439, Dec. 1999.
[37] S. Koziel, J. W. Bandler, and Q. S. Cheng, "Adaptively constrained parameter extraction for robust space mapping optimization of microwave circuits," in *2010 IEEE MTT-S Int. Microw. Symp.*, Anaheim, CA, 2010, pp. 205-208.
[38] S. Koziel, J. W. Bandler, and Q. S. Cheng, "Constrained parameter extraction for microwave design optimisation using implicit space mapping," *IET Microwaves, Antennas & Propagation*, vol. 5, no. 10, pp. 1156-1163, July 2011.
[39] J. W. Bandler, S. H. Chen, R. M. Biernacki, L. Gao, K. Madsen, and H. Yu, "Huber optimization of circuits: a robust approach," *IEEE Trans. on Microw. Theory Techn.*, vol. 41, no. 12, pp. 2279-2287, Dec. 1993.
[40] Z. Brito-Brito, I. Llamas-Garro, G. Navarro-Munoz, J. Perruisseau-Carrier, and L. Pradell, "UMTS-WiFi switchable bandpass filter," in *2009 European Microw. Conf. (EuMC)*, Rome, 2009, pp. 125-128.

Andres Viveros-Wacher was born in Mexico City, Mexico in 1986. He received the B.Sc. in electronic engineering from the National Autonomous University of Mexico (UNAM), Mexico City, Mexico in 2010 and the M.Sc. in microelectronics systems from the University of Bristol, Bristol, U.K. in 2011. He is currently pursuing the Ph.D. degree in engineering sciences at the Department of Electronics, Systems, and Informatics, ITESO–The Jesuit University of Guadalajara.

Since 2012, he is an analog validation engineer at Intel Corp. His current research interests include design of experiments, optimization methods for high-speed I/O, surrogate-based optimization and analog fault modeling and diagnosis methods.

José Ernesto Rayas-Sánchez received the B.Sc. degree in electronics engineering from ITESO–The Jesuit University of Guadalajara, Mexico, the M.Sc. degree in electrical engineering from Monterrey Tec (ITESM), Monterrey, Mexico, and the Ph.D. degree in electrical engineering from McMaster University, Ontario, Canada.

He is currently a *Profesor Numerario* (Hons.) with ITESO–The Jesuit University of Guadalajara, where he is Chair of the Doctoral Program in Engineering Sciences. He currently leads the Research Group on Computer-Aided Engineering of Circuits and Systems with ITESO–The Jesuit University of Guadalajara. His research focuses on computer-aided and knowledge-based modeling, design and optimization of high-frequency electronic circuits and devices (including RF, microwave, and wireless circuits).

Dr. Rayas-Sánchez is Chair of the Technical Committee on Computer Aided Design (MTT-1) of the IEEE Microwave Theory and Techniques Society (MTT-S). He is member of the Technical Program Reviewers Committee of the IEEE MTT-S International Microwave Symposium (IMS). He serves as reviewer for the following publications: IEEE Transactions on Microwave Theory and Techniques, IEEE Microwave and Wireless Components Letters, IEEE Antennas and Wireless Propagation Letters, IET Microwaves, Antennas & Propagation Journal, International Journal on Numerical Modelling (Wiley) and International Journal of RF and Microwave Computer-Aided Engineering (Wiley). Since 2013, he is IEEE MTT-S Regional Coordinator for Latin America. He was the General Chair of the First IEEE MTT-S Int. Microwave Workshop Series in Region 9 (IMWS2009-R9) on Signal Integrity and High-Speed Interconnects (Guadalajara, Mexico, Feb. 2009), as well as the General Chair of the First

IEEE MTT-S Latin America Microwave Conference (LAMC-2016, Puerto Vallarta, Mexico, Dec. 2016).

Zabdiel Brito-Brito received the B.Sc. degree in Communications and Electronics Engineering, and the M.Sc. degree in Electronics Engineering from the National Polytechnic Institute (IPN), Mexico, in 2001 and 2003, respectively, and received the PhD. degree in Communications and Signal Theory at the Technical University of Catalonia (UPC), Barcelona, Spain, in 2010.

He is currently a full Professor with ITESO– The Jesuit University of Guadalajara, where he is the academic program administrator of the Master's Degree in Electronics Design and of the Systems in Chip Design Specialization. He is a member of the Research Group on Computer-Aided Engineering of Circuits and Systems with ITESO–The Jesuit University of Guadalajara. His research focuses on Microwave, RF and Wireless tunable systems using solid state and MEMS devices and also on methods and techniques for computer-aided and knowledge-based modeling.

Dr. Brito-Brito serves as reviewer for the IEEE Transactions on Antennas and Propagation. Since 2019, he is the IEEE Guadalajara Section Secretary. He was the IEEE MTT-S Guadalajara Chapter Chair from 2015 to 2018, as well as the Financial Chair of the First IEEE MTT-S Latin America Microwave Conference (LAMC-2016, Puerto Vallarta, Mexico, Dec. 2016).