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# Analog Fault Identification in RF Circuits using Artificial Neural Networks and Constrained Parameter Extraction

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***Abstract* — The increase of analog and mixed-signal circuitry in modern RF and microwave integrated circuits demands for improved analog fault diagnosis methods. While digital fault diagnosis is well established, the analog counterpart is relatively much less mature due to the intrinsic complexity in analog faults and their corresponding identification. In this work, we present an artificial neural network (ANN) modeling approach to efficiently emulate the injection of analog faults in RF circuits. The resulting meta-model is used for fault identification by applying an optimization-based process using a constrained parameter extraction formulation. The proposed methodology is illustrated by a faulty analog CMOS RF circuit.**

***Index Terms* — analog faults, artificial neural network, gross faults, fault injection, fault identification, parameter extraction.**

## I. Introduction

The growing need of analog and mixed signal integrated circuits (IC) has increased the demand not only of fault tolerance but also of fault detection and isolation [1]. While fault diagnosis techniques for digital circuits are mature and well established, those for analog circuits are still relatively unexplored. This is mainly due to three key points [2]-[4]: a) there are not only two possible signal values, but in principle an infinite number of possible values; b) the timing characteristics of signals are not discrete, but continuous; and 3) the failure mode does not necessarily propagate to the output pins of the circuit.

Analog faults are categorized as catastrophic (or gross) faults and parametric (or soft) faults [5]. Gross faults are typically caused by structural deformities, such as open and short circuits, while parametric faults are generally caused by variations of component parameters outside of their tolerance range. Prior work has used these two types of basic fault models and pursued a fault injection methodology to capture the circuit behavior under faulty conditions [5], [6].

On the other hand, as one of the knowledge-based fault diagnosis methods, machine learning techniques that exploit the use of neural networks have become the most extensively used method for fault diagnosis of many types of systems, including analog circuits [7]-[12]. Most of the previous work focuses on the usage of neural networks as classifiers, to distinguish only between faulty and non-faulty responses [13]-[16]. Other works have used the wavelet transform as pre-processing methods to improve not only the detection but also the isolation of faults [17], [18], namely, the localization of the specific faulty circuit component. However, they require complex neural networks as well as prior processing methods to achieve correct identification. This paper proposes using a simple artificial neural network (ANN) to model the effects of injecting gross faults to the circuit under diagnosis. Once the ANN is trained, it is used for fault identification through a simple yet efficient optimization process based on constrained parameter extraction, reproducing a faulty circuit response by optimizing the already trained ANN model inputs. A classical RF CMOS feedback amplifier illustrates our methodology.

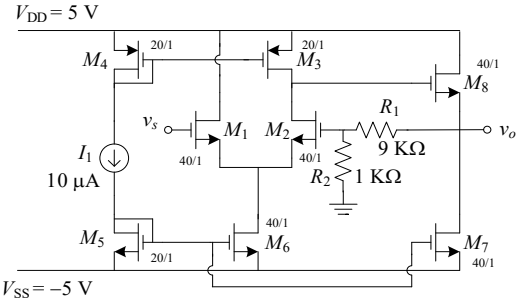


Fig. 1. Original negative feedback CMOS RF amplifier.

## II. Analog Fault Models

Analog fault models aim at exposing the circuit under diagnosis to: a) a catastrophic failure, where the circuit cannot operate; b) a performance degradation, where the circuit still works but the performance is lower than its specification; and c) an acceptable performance, despite having the faults. This work employs gross fault models that emulate open and short circuits within the main circuit topology. Opens are modeled by using a high enough value of a serial resistance, while shorts are modeled by using a small enough value of a parallel resistance. The nominal values chosen for the faults in this work are 200 MΩ for opens and 1 mΩ for shorts.

## III. Analog Fault Injection on a Circuit Example

The circuit selected for fault injection is a classical CMOS negative feedback RF amplifier depicted Fig. 1, whose nominal voltage gain is shown in Fig. 2.

We inject an open to the drain and source pins of each transistor, and a short between each pair of transistor nodes, in a parametrized manner, in such a way that each fault can be individually activated and have a specific resistive value. When faults are not active, the value used for opens is 1 mΩ

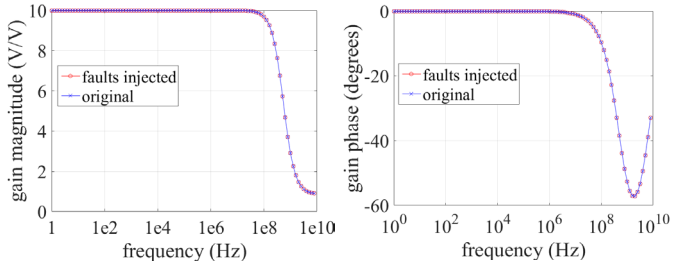


Fig. 2. Response (voltage gain) comparison between the original circuit and the fault-injected circuit with all faults inactive.

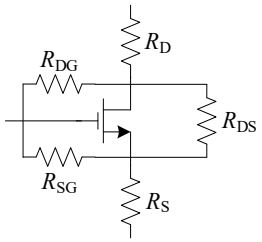


Fig. 3. Five possible faults in a transistor, modeled with opens on the drain ($R_D$) and source ($R_S$) terminals, and shorts between each pair of terminals ($R_{DS}$, $R_{DG}$ and $R_{SG}$).

and for shorts is 200 MΩ. In this way, we guarantee that under no-fault conditions, the fault-injected circuit behaves as the original circuit, as it is confirmed in Fig. 2.

## IV. Artificial Neural Network Modeling

### A. Problem Definition

As an initial approach, we aim to neuro-model the behavior of the circuit when injecting a single fault at a time. We define the vector of ANN inputs, $\boldsymbol{x}$, as follows: $x_1$ represents the location of the fault, from one out of 8 transistors; $x_2$ represents one out of the 5 possible faults for each transistor ($R_D$, $R_S$, $R_{DS}$, $R_{DG}$ and $R_{SG}$), as seen in Fig. 3; and $x_3$ represents the amount of deviation from the nominal fault value. Given that the faults are analog, their values could take in theory an infinite number of possible values. However, for this work we employ a reduced range from −5% to +5% for $x_3$, which is a reasonable manufacturing tolerance.

The output $\boldsymbol{R} \in \Re^m$ for the ANN model, is defined as

$$\boldsymbol{R} = \begin{bmatrix} \sum_i^N \left( \mathrm{Re}\{Av_i\} - \mathrm{Re}\{Av_i^{\mathrm{nf}}\} \right) \\ \sum_i^N \left( \mathrm{Im}\{Av_i\} - \mathrm{Im}\{Av_i^{\mathrm{nf}}\} \right) \end{bmatrix} \quad (1)$$

where $Av^{\mathrm{nf}}$ is the complex amplifier voltage gain when no faults are injected, $Av$ is the gain with the injected fault, and $N$ is the number of sampled frequency points. In other words, the neuro-modeled output represents the deviation of the circuit voltage gain from a no-failure condition.

### B. ANN Characteristics

We select a 3-layer perceptron for the topology of our ANN. The ANN is implemented and trained using the Matlab neural network toolbox. We select the Bayesian regularization algorithm for training, and use 1,000 base points generated using the Sobol pseudo-random sequence to sample the selected solution space as uniformly as possible [19]. Out of the total number of base points, 70% are selected for learning and 30% are selected for testing. The algorithm used for training increases the number of neurons in the hidden layer, $h$, until the generalization performance deteriorates (similarly to [20]), or until the learning and testing errors are below 1%,

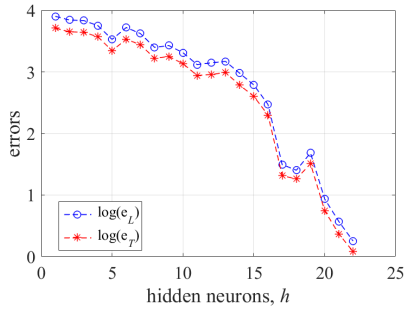


Fig. 4. ANN performance while increasing $h$, the number of neurons in the hidden layer.

$$\begin{aligned} &(e_{\mathrm{t\_old}} < e_{\mathrm{t\_new}} \wedge e_{\mathrm{t\_new}} > e_{\mathrm{l\_new}}) \vee \\ &(e_{\mathrm{t\_new}} < 1\% \wedge e_{\mathrm{l\_new}} < 1\%) \end{aligned} \quad (2)$$

where $e_{\mathrm{t\_old}}$ is the testing error at the previous iteration and $e_{\mathrm{t\_new}}$ and $e_{\mathrm{l\_new}}$ are the testing and learning errors, respectively, at the current iteration. The ANN performance while increasing $h$ is seen in Fig. 4. The final value of $h$ is 21.

Once the ANN is trained, we test it using 100 extra base points not used during training. The output from the ANN model is compared against actual circuit (SPICE) simulations. The ANN can closely predicts the circuit faulty response, with around 0.00635% of maximum relative error.

## V. Fault Identification by Parameter Extraction

Here we exploit parameter extraction (PE) as an optimization problem that aims at minimizing the difference between a target response and the system response being optimized [21]. In our work, we aim at finding the input values $\boldsymbol{x}$ of the ANN model that minimize the difference between the objective function value of a faulty circuit, calculated in (1) and treated as the target, and the ANN output. The optimization procedure is executed by solving

$$\boldsymbol{z}^* = \arg\min_{\boldsymbol{z}} \left\| \boldsymbol{R}(\boldsymbol{z}) - \boldsymbol{R}^t \right\|_1 \quad (3)$$

where $\boldsymbol{R}(\boldsymbol{z})$ is the ANN model output and $\boldsymbol{R}^{\mathrm{t}}$ is the target output. In our case, (3) is solved by using the Nelder-Mead method. In order to keep $\boldsymbol{x}$, the ANN inputs, within feasible values during the optimization iterations, we use box constraints defined as

$$\boldsymbol{x} = \begin{bmatrix} x_1^{\mathrm{lb}} + \left(x_1^{\mathrm{ub}} - x_1^{\mathrm{lb}}\right)(\sin z_1)^2 \\ x_2^{\mathrm{lb}} + \left(x_2^{\mathrm{ub}} - x_2^{\mathrm{lb}}\right)(\sin z_2)^2 \\ \sin z_3 \end{bmatrix} \quad (4)$$

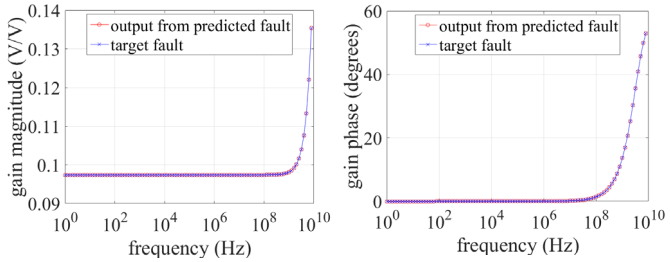

Fig. 5. Comparison between the circuit responses at predicted fault and those at the actual fault injected (gain magnitude and phase).

where $x_1^{lb} = 1$ and $x_2^{ub} = 8$ are the selected lower and upper values, respectively. Similarly, $x_1^{lb} = 1$ and $x_2^{ub} = 5$ correspond to the upper and lower values for $x_2$.

Given the expected high number of local minima, and to overcome the issue of different faults yielding a similar response, we use a statistical PE algorithm, where the starting point of the optimization procedure is slightly perturbed each time the normalized difference between the optimal ANN response and the target response is larger than a desired value, $\varepsilon_{PE}$. In our case, the value selected is $\varepsilon_{PE} = 1\times10^{-5}$.

### C. Fault Identification Results

To validate the effectiveness of our proposal, we select a random fault as target, and followed the PE procedure. The values of $\boldsymbol{x}$ for the actual faults are [2 3 0.1498%]. The resulting values of $\boldsymbol{x}$ match exactly on $x_1$ and $x_2$, thus the fault location within the circuit and the fault type (one out of five possible faults) are identified precisely on each case. There is, however, a slight variation between the predicted (0.02967%) and the actual value in the variable corresponding to the deviation from the nominal fault value, $x_3$. Nevertheless, the simulated outputs from the circuit with the identified fault closely resemble the outputs with the original injected fault, as shown in Fig. 5. This consistency was verified for other 5 cases of different injected faults, observing a similar behavior.

## VI. Conclusion

An analog gross fault diagnosis method based on artificial neural networks and constrained parameter extraction was proposed in this paper. Our method was illustrated by injecting analog gross faults in a CMOS RF negative feedback amplifier. The gross faults were modeled as resistances with a high enough value in series to cause an open circuit and with a low enough value in parallel to cause a short circuit. The ANN reached the desired learning and generalization performance using 21 neurons at the hidden layer. The ANN was then used as a metamodel, with an extremely low computational cost, to automatically identify faults through a statistical constrained parameter extraction process. Following this process, we were able to properly identify the actual injected faults.

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