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Optimizing Phase Settings of High-Frequency Voltage Regulators for Power Delivery Applications

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***Abstract* — Every new computer server introduced to the market aims at delivering the best tradeoff between performance and power consumption. This goal is crucial in the case of servers for cloud computing hardware infrastructure. In this context, power delivery (PD) experts are adopting higher frequency switching voltage regulators (VR) to reduce platform's cost as well as total cost of ownership (TCO). Because of this fact, the real estate of components, such as voltage regulators and output inductors, is shrinking as VR frequency increases. As a consequence, achieving the best performance of the VR implies looking into phase shedding schemes, as well as EM coupled inductor design, among other techniques, to mitigate power losses. This paper focuses on the study of the best angle arrangement possible for high frequency VR applications, by exploring angle settings under light load scenarios, aiming to minimize VR's power loss and output's voltage ripple.**

***Index Terms* — high frequency switching, multiphase voltage regulator, optimization, phase configuration, power loss reduction, ripple reduction.**

I. Introduction

As customers demand for better power efficiency and performance from server computers, every new CPU server generation faces more challenges to meet such demands. In recent years, power delivery (PD) engineers have come across with several strategies, such as multiphase voltage regulators (VR) [1,2] to improve transient responses and reduce power losses and ripple, coupled inductors [3,4] to enhance efficiency, high-frequency (HF) switching voltage regulators [5-7] for fast transient performance, phase shedding schemes [8,9] for better efficiency at lighter loads, etc.

VR designs are rapidly moving to adopt HF switching implementations to reduce real estate space as well as platform's bill of materials (BOM) cost. This trend imposes the need to deal with electromagnetic (EM) coupling due to proximity of components, especially for the output inductors. This paper focuses on the optimization of phase configurations to mitigate power losses and reduce output voltage ripple for HF switching VR applications for server computers. To illustrate the proposed approach, we consider a 4-phase VR under light load conditions, however, our technique can be extended to larger number of phases.

The rest of the paper is organized as follows. In Section II, we review the methodology employed in the laboratory to set the best phase settings based on power loss and ripple measurements. Section III goes over a simulation tool developed in-house to approximate the results measured in the laboratory, facilitating phase exploration studies. Section IV shows a comparison between the results obtained in the laboratory and the simulation. To speed up our design process, we explore in Section V some optimization techniques to find the optimal phase recipe aiming at reducing power loss and ripple metrics. Finally, Section VI presents our conclusions.

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II. Finding Phase Configuration in the Laboratory

Measuring in a reliable manner the losses through different phase configurations in the laboratory, requires to maintain some variables controlled besides the load and the VR itself. The input voltage V_{in} and output voltage V_{out} are fixed to nominal settings. Also, a stable feedback configuration is used and the loading current I_{load} is fixed, while temperature of the VR is controlled and set to 25 °C.

Measurements include the input power P_{in} and the output voltage ripple V_{ripple}, since our goal is to minimize the power loss P_{loss} with the smallest V_{ripple}. For this experiment, we can calculate the output power P_{out} considering that both I_{load} and V_{out} are fixed. From here, it is enough to measure P_{in} to calculate the efficiency η as well as the power loss P_{loss}.

The angle resolution is limited by the VR's registers that configure the delays between the different phases of the output inductors (see Fig. 1). We define the number of possible

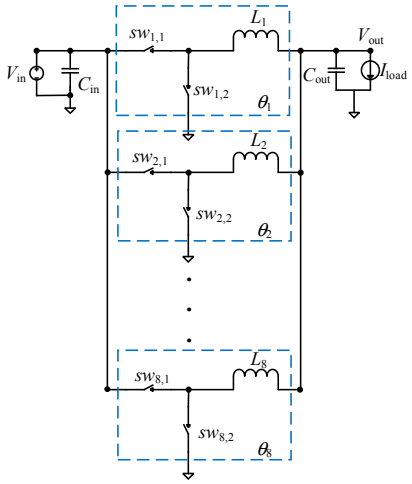

Fig. 1. Multiphase Buck converter: 8-phase representation with ideal switches for each output inductor.

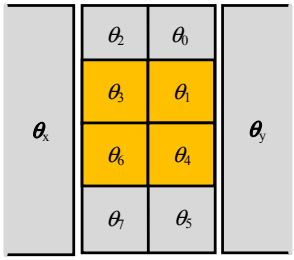

Fig. 2. Visual representation of an embedded package inductor hocked to the high-frequency switching VR. Orange boxes represent the output inductors enabled for this study. θ_2, θ_0, θ_7, and θ_5 are kept fixed. Vectors $\boldsymbol{\theta}_x$ and $\boldsymbol{\theta}_y$ denote close neighboring output inductors.

discrete angle values per output inductor as N_a. Then, the number of possible angle configurations N_{cfg} grows exponentially with the output inductors:

$$N_{cfg} = N_a{}^N \tag{1}$$

where N is the number of output inductors of the VR.

For instance, if we have eight available output inductors (as in Fig. 1) with four possible angles per inductor, then $N = 8$ and $N_a = 4$, yielding $N_{cfg} = 4^8 = 65{,}536$ possible phase configurations. It is possible to simplify the problem by fixing one phase (*e.g.*, $\theta_1 = 0°$) to reduce the number of possible configurations to $N_{cfg} = 4^7 = 16{,}384$. In our case, we selected only four out of the eight output inductors, as illustrated in Fig. 2, keeping the rest fixed.

The pseudo code employed to sweep N different output inductors with N_a different angle configurations per output inductor is shown in Fig. 3.

III. Simulation Approach for Phase Configurations

To obtain an accurate output inductor model, the embedded package output inductor and its power distribution network (PDN) are modeled in a 3D field solver[1] [7]. Our main interest focuses on characterizing the output inductor, for which we can extract the L, R, and C parasitic elements, as well as the inductor's coupling factor (k), from the corresponding S-parameters.

These S-parameters are then loaded into our in-house simulation tool to perform P_{loss} and V_{ripple} calculations. This is done by means of injecting DC and AC components at the input of the inductors given a configuration of V_{in}, V_{out}, f_{sw}, I_{load}, C_{in}, C_{out}, and $\boldsymbol{\theta}$, where $\boldsymbol{\theta} = [\theta_1\ \theta_2\ \ldots\ \theta_8]^T$ is the vector of available phases, f_{sw} is VR's operating switching frequency, C_{in} is the input's filter capacitance and, C_{out} is the capacitance at the load. Finally, we set I_{load} under light load conditions, while V_{in} and switching transistors are assumed to be ideal components, as illustrated on Fig. 1. We are interested in performing the phase configuration study under light load conditions, since these conditions represent the largest AC loss contribution due to the switches and inductors, yielding to more heat dissipation and a more expensive thermal design.

```
set VR to NominalVoltage
set Iload to ConstantCurrent
set N to NumberofOutputInductor
set Na to NumberofAngleConfigurations
set AnglesList to [0, (360/Na), (2*360/Na), …, ((Na−1)*360/Na)]
set θ1 to 0
for each AngleValue2 in AnglesList
  set AngleValue2 to θ2
  for each AngleValue3 in AnglesList
    set AngleValue3 to θ3
      ⋮
      for each AngleValueN in AnglesList
        set AngleValueN to θN
        measure Vripple , Pin
        store Vripple, Pin in Results[AngleValue2, AngleValue3, …,AngleValueN]
      end loop
    ⋮
  end loop
end loop
```

Fig. 3. Pseudo code implemented in the laboratory to measure V_{ripple} and P_{loss} sweeping different phase angle configurations.

There will be certain behaviors that will not be captured during simulation, such as PWM glitches and power losses at the switches. However, power losses on the switches are independent from $\boldsymbol{\theta}$. Hence, by neglecting the contribution of the PWM glitches on V_{ripple}, we can approximately set our two main performance parameters of interest as functions of phase configuration variations, *i.e.*, $V_{ripple} = f(\boldsymbol{\theta})$ and $P_{loss} = g(\boldsymbol{\theta})$.

IV. Validating the Simulation Approach by Laboratory Measurements

Here we compare normalized simulation results versus laboratory measurements on a realistic environment (eight core Xeon® CPU). Normalized 3D plots of V_{ripple} and P_{loss} are shown in Fig. 4. These plots are obtained from the laboratory and by using our in-house simulation tool predicting the behavior of the high frequency VR. For the sake of visual

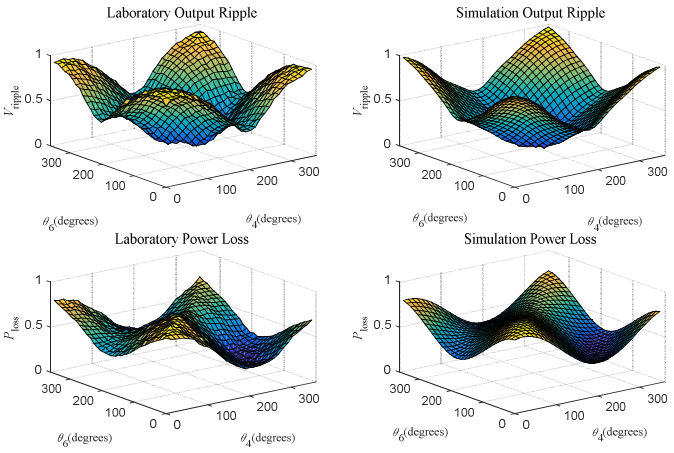

Fig. 4. 3D plots for normalized V_{ripple} (top) and P_{loss} (bottom), sweeping two phases in the laboratory (left side) and in the simulation model (right side).

[1] PowerSI 3D-EM v17.0.0.12061.80497, Cadence Design Systems, Inc., San José, CA, 2016.

clarity, we fix $\theta_1 = 0°$ and $\theta_3 = 0°$ for V_{ripple}, and $\theta_1 = 0°$ and $\theta_3 = 67°$ for P_{loss} (see Fig. 2). It is seen from Fig. 4 that the simulation model approximates with quite acceptable accuracy the behavior of the actual physical platform. While, the relative errors of our simulation model with respect to laboratory measurements are less than 20% for V_{ripple}, and less than 15% for P_{loss}.

V. Finding the Best Phase Configuration by Numerical Optimization

As observed in Fig. 4, phase configuration can greatly impact both V_{ripple} and P_{loss}. Given the multiplicity of available angle combinations and the dimensionality of the spatial configuration on converter's inductors, a practical approach lies in the implementation of optimization techniques. Since this problem requires the simultaneous minimization of two functions, here we propose a *minimax* formulation, which is described up next.

A. Power Loss and Output Ripple Error Function

We define maximum acceptable values for P_{loss} and V_{ripple}, denoted as $P_{lossmax}$ and $V_{ripplemax}$. Then, error functions are defined as

$$e_{Vripple}(\boldsymbol{x}) = \left(V_{ripple}(\boldsymbol{x})/V_{ripple\max}\right) - 1 \quad (2)$$

$$e_{Ploss}(\boldsymbol{x}) = \left(P_{Ploss}(\boldsymbol{x})/P_{loss\max}\right) - 1 \quad (3)$$

where vector $\boldsymbol{x}$ contains the current phase configuration, $e_{Vripple}(\boldsymbol{x})$ is the error function value for the current $V_{ripple}(\boldsymbol{x})$, while $e_{Ploss}(\boldsymbol{x})$ is the error function value for the current $P_{loss}(\boldsymbol{x})$.

The values selected for $V_{ripplemax}$ and $P_{lossmax}$ are defined to achieve an overall CPU efficiency enhancement of at least 0.5 %. Even though, this increase in efficiency can be regarded as a small enhancement, in practice it can greatly reduce the thermal impact on the CPU, by up to 5 °C, which has a very significant impact for cloud computing servers.

B. Optimization Problem Formulation

The optimization problem is formulated to find the argument that minimizes with respect to $\boldsymbol{x}$ the maximum error function value for V_{ripple} and P_{loss}:

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \quad (4)$$

$$u(\boldsymbol{x}) = \max\{e_{Vripple}(\boldsymbol{x}), e_{Ploss}(\boldsymbol{x})\} \quad (5)$$

where $\boldsymbol{x}^*$ is the optimal phase configuration found, and the corresponding minima values of V_{ripple} and P_{loss} are denoted as $V_{ripple}{}^*$ and $P_{loss}{}^*$. If $u(\boldsymbol{x}^*) < 0$ we guarantee that both V_{ripple} and P_{loss} at $\boldsymbol{x}^*$ are below their maximum acceptable values at the optimal phase configuration found. However, if $u(\boldsymbol{x}^*) > 0$, at least one of these performance responses is exceeding its maximum value.

C. Implementing Optimization Flow

We solve optimization problem (4)-(5), with error functions defined by (2)-(3), using two different optimization algorithms, both available in MATLAB[2] optimization toolbox. In the first case we use the sequential quadratic programing (SQP) algorithm based on the Broyden-Fletcher-Goldfarb-Shano (BFGS) formula [10]. SQP is a powerful algorithm suitable for nonlinear programming and continuous problems; it is a gradient-based deterministic method and requires an initial guess or starting point $\boldsymbol{x}^{(0)}$. In the second case, we use the genetic algorithm (GA), which in principle is a global optimization random population search method (no gradients required), suitable for a discrete solution space.

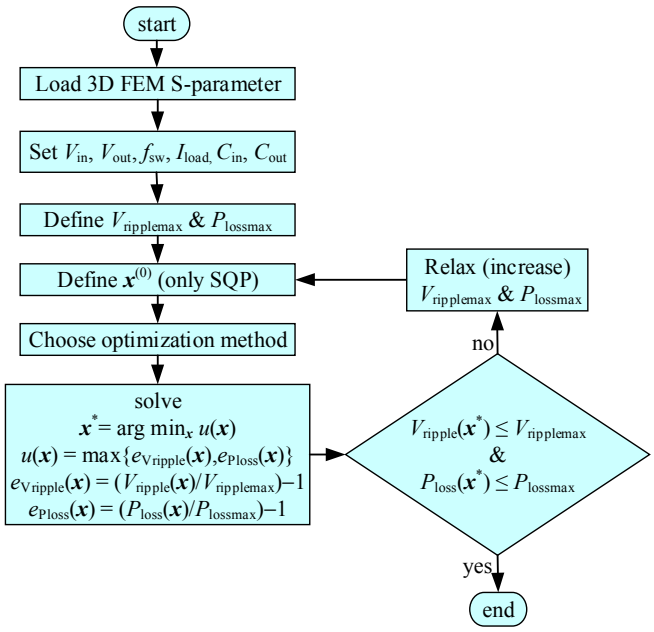

Fig. 5. Optimization flow to obtain the best phase angle recipe while minimizing V_{ripple} and P_{loss} from a high-frequency switching VR.

Up next, we enlist a summary of the optimization flow we followed (see Fig. 5):

a. Load S-parameters from 3D FEM solver.
b. Set converter's operating conditions (V_{in}, V_{out}, f_{sw}, I_{load}, C_{in}, C_{out}).
c. Define $V_{ripplemax}$ and $P_{lossmax}$, such that CPU's overall efficiency improves by at least 0.5 %.
d. For the case of SQP, define an initial guess for phase configuration $\boldsymbol{x}^{(0)}$ to calculate the initial errors.
e. Choose one of the two optimization algorithms.
f. Apply the selected optimization algorithm to solve (4). For the case of GA, the solution space is restricted to discrete angle steps. In the case of SQP, optimization is conducted over a continuous design space.
g. Test if $V_{ripple}(\boldsymbol{x}^*)$ and $P_{loss}(x^*)$ meet $V_{ripplemax}$ and $P_{lossmax}$. If not, relax $V_{ripplemax}$ and $P_{lossmax}$, and repeat the process from d.

D. Optimization Results

[2] MATLAB, Version R2015a, The MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2006.

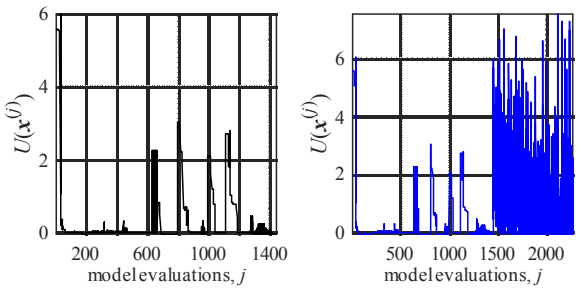

Fig. 6. Evolution of the objective function during optimization using: a) SQP with a bad starting point; and b) GA.

Since our simulation model is very fast, the aforementioned algorithms were run 100 times total, 50 times using SQP (with different starting points) and 50 times with the GA, registering each time the optimal values for P_{loss} and V_{ripple}. To simplify our study (see Section II), instead of analyzing four phases at a time, we maintained one of the phases fixed ($\theta_1 = 0°$). In the case of GA, 100% of the optimized angle results landed at the same angle configuration (see normalized P_{loss} and V_{ripple} results in Table I). Although there is no mathematical proof that shows this result is the global minimum, by "eye inspection" in the laboratory, we confirmed the optimal solution found by GA corresponds to the best one identified by exploring the entire solution space as illustrated in Fig. 4.

Results from Table I confirm that SQP can reach either a local or the global minimum. Most of the times (70%) we run SQP landed at the same solution (after rounding) found by GA, while 30% of the times landed at a local minimum.

The number of objective function evaluations during optimization is also a figure of merit. For the case of GA, it required an average of 2,250 objective function evaluations. Even though this number is large, it is still significantly smaller than the 16,384 measurements needed to sweep the entire solution space in the laboratory (see Section II). In contrast, using SQP with random initial angles, it required an average of 406 function evaluations, confirming that SQP is much faster than GA, but less reliable to find the global minimum, as expected.

Finally, Fig. 6 shows the evolution of the objective function U during optimization for two particular cases. Fig. 6a shows the behavior of SQP when a very bad starting point is selected, which makes it comparable in computational cost to GA. Fig. 6b confirms that GA yields larger oscillations of U during optimization than SQP due to its random population-based nature.

VI. Conclusions

We optimized phase configurations of a HF switching VR for PD CPU server applications. Our work covered several aspects to obtain the phase configuration. In the first aspect, we described how to estimate P_{loss} and V_{ripple} of the physical CPU. On the second aspect, we modeled the output inductor and the behavior of the VR, to calculate P_{loss} and V_{ripple}. We validated our simulation model by comparing versus laboratory measurements under a simplified multiphase scenario, showing good agreement. Finally, we implemented numerical optimization techniques in the simulation space. As a result, we identified faster the best phase configuration, decreasing P_{loss} and V_{ripple}. This effort helped us to reduce the thermal stress on the physical chip. Furthermore, this work can be extended to more complex scenarios, where more interactions between different voltage domains play a significant role defining the best phase configuration.

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TABLE I

NORMALIZED POWER LOSS AND OUTPUT RIPPLE AT OPTIMAL SOLUTIONS

Opt. Method	$\boldsymbol{x}^*$ (degrees)	$u(\boldsymbol{x}^*)$	$P_{\text{loss}}(\boldsymbol{x}^*)$	$V_{\text{ripple}}(\boldsymbol{x}^*)$
GA	$[0.00 \;\; 180.00 \;\; 180.00]^T$	-31.432×10^{-3}	7.386×10^{-7}	0.0298
SQP (70% times)	$[0.41 \;\; 180.15 \;\; 180.35]^T$	-31.431×10^{-3}	3.024×10^{-6}	0.297
SQP (30% times)	$[307.13 \;\; 132.66 \;\; 156.71]^T$	-16.692×10^{-3}	98.073×10^{-3}	0.0661