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Design of Experiments Implementation towards Optimization of Power Distribution Networks

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***Abstract*— Modern computer servers require cutting edge technologies to meet their expected high performance. Among several relevant disciplines, power delivery (PD) is a key player in this regard. Efficient and reliable statistical methods to reduce cost while keeping adequate server's performance are highly demanded from the PD perspective. This paper addresses a feasible statistical methodology based on design of experiments (DoE) for evaluating platform's power delivery ingredients. Our methodology explores voltage regulator's intrinsic parameters, compensation networks, non-linear compensation parameters, and the amount of bulk capacitors. Our statistical approach aims at identifying those variables with the largest impact on computer server's PD performance, as well as optimizing them at the system level while achieving cost reduction.**

Keywords*— *design of experiments; laboratory correlation; power delivery simulation; statistics control; voltage regulator

I. Introduction

Server's performance imposes severe demands for higher bandwidths, low cost power solutions, and high computing performance. Thus, modern computer servers require cutting edge technologies to meet all the above expectations. In this regard, power delivery (PD) requires some tradeoff decisions to select an adequate voltage regulator, a suitable and affordable decoupling solution, and a robust stack up design to handle sharp load current demands, while keeping silicon under expected performance.

Several authors have explored different PD methodologies, such as establishing target impedance across a wide frequency range to select the decoupling capacitor solutions needed by the power distribution network (PDN) [1, 2], as well as time domain approaches [3] and jitter analysis [4, 5] for estimating voltage drop and voltage margins to come up with robust design solutions.

Industrial PD design is still considered an "art"; as it is a heavily heuristic process and very dependent on engineer's expertise. Identifying which variables are most impactful to the PDN space is a highly complex task, usually performed in practice by parametric sweeps, exhaustive enumeration, and engineering knowledge and experience. To the best of our knowledge, formal statistical methodologies based on design of experiments (DoE) for the optimization of the PDN have never been reported. Our contribution in this papers aims at filling that gap. In particular, our paper focuses on solving computer server´s PD system by optimizing voltage regulator´s (VR) tuning parameters as well as its bulk capacitors solution.

In Section II, we conceptually describe how design of experiments (DoE) can be exploited to develop PD behavioral models. Section III presents a DoE simulation approach identifying the most important variables impacting the whole VR solution. Section III follows the same DoE methodology but as applied to the physical VR implementation incorporating laboratory measurements. Section IV makes a comparison between both scenarios, simulation and physical implementation, with the aim of performing system optimization using response surface methods (RSM). Finally, Section V makes conclusions from the experimental work, and sets future directions to improve PD design.

II. Modeling Power Delivery by DoE

DoE has been adopted in some disciplines closely related to PDN design, such as I/O's electrical validation and verification [6] and signal integrity (SI) analysis [7, 8], where designers statistically assess cases to find the best channel configuration with the best equalization recipe to avoid loss of information from one buffer to another. However, PD has not taken full advantage of such methodologies.

Similarly to the SI and electrical validation realm, PD designers are looking for the best power channel's recipe capable to maintain its voltage level within expected ratings

under any loading circumstance. PD engineers typically require complex and detailed PDN simulation models to predict with sufficient accuracy the power channel's behavior, which makes simulation very computationally intensive, taking up to several days to obtain a PDN behavior.

From the above perspective, classical parametric sweeps and exhaustive enumeration are usually prohibitive. Here we propose using advanced DoE techniques, such as fractional factorial design (FFD) [9], Taguchi, etc., that can reduce significantly the amount of simulations needed, enabling PD engineers to efficiently identify the most impactful variables within the PDN. In DoE, the objective is to efficiently obtain a behavioral model for a certain output of interest, such it describes with sufficient accuracy the actual system's behavior. This behavioral approximation is typically implemented by a linear regression model

$$y(\boldsymbol{x}) = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 + \ldots + \varepsilon \qquad (1)$$

where $y(\boldsymbol{x})$ is system's output of interest, β's are parameters to be determined during the DoE analysis, x_1, x_2, etc., are the model variables that represent the selected system factors *A*, *B*, etc., and ε is the statistical error. Variables x_1 and x_2 are defined in a coded scale from −1 to +1 (low and high corner levels, respectively, for *A* and *B*), and x_1x_2 represents the interaction between x_1 and x_2.

III. DoE for Power Delivery: Simulation Approach

To illustrate our methodology, we select a similar VR design to that one in [10] as the test vehicle to meet some voltage requirements: silicon's V_{min} = 1.5 V and V_{max} = 2 V, under any loading condition (*di*/*dt*).

Based on the VR design described in [10], parameters investigated in the simulation are given in Table I. We consider not only intrinsic VR compensation parameters but also some VR-external factors. For the first set, we focus our study on the proportional-integral-derivative (PID) controller's variables (k_i, k_d, k_p), non-linear coefficients (*NL-C*), adaptive transient response (*ATR*), and auto-phasing schemes enabling and disabling VR's phases at some point in time (A_{Ph}). On the second set we consider the quantity of bulk capacitors (*BlkC*) and the slew rate (*SR*) (here defined as the *di*/*dt* slope of the transition from minimum current (I_{min}) to maximum current (I_{max})).

TABLE I. Variables used to Build the FFD for Simulation Scenario

Factor	Equivalent Variable	(−1)	(+1)
$A = (x_1)$	k_p	100	250
$B = (x_2)$	k_d	250	450
$C = (x_3)$	k_i	100	250
$D = (x_4)$	k_{fp}	100	250
$E = (x_5)$	A_{Ph}	no	yes
$F = (x_6)$	*NL-C*	no	yes
$G = (x_7)$	*ATR*	no	yes
$H = (x_8)$	*BlkC*	29%	100%
$J = (x_9)$	*SR* (1-1000 A/µs)	slow	fast

From Table I, there are nine factors to investigate, requiring a total of $2^9 = 512$ simulations to find system's most significant factors. However, we use the FFD technique to reduce the number of simulations by "confounding" some of these factors.

Returning to our simulation's test bench scenario, we selected a $2_{IV}^{(9-4)} = 32$ experiments. We use resolution *IV* since it suitable for designs in which none of the main effects is an alias of another main effect or neither two factor interactions, but two factor interactions are aliases between them. Typically, it receives the name of "confusion of factors". Additionally, we use a factorial $2^{(9-4)}$ because only five of the main factors are not confounded, and they correspond to Yates order for generating the test bench, while the remaining four factors are generated by the following confounded factors [9]: $F = \pm BCDE$, $G = \pm ACDE$, $H = \pm ABDE$, and $J = \pm ABCE$.

We use only time domain simulations in SIMetrix/Simplis[2] simulator to obtain test bench results under different VR and PD settings. Once results are collected, an analysis of variance (ANOVA) is performed to get some linear regression equations at the output of interest including its effects. The, from Pareto's analysis, it is possible to identify what variables are more important and hence simplify the equations obtained from ANOVA, yielding

$$V_{min} \approx 0.960 + 0.001722 x_2 \qquad (2)$$

$$V_{max} \approx 2.791 - 0.0026 x_2 - 0.0806 x_8 \qquad (3)$$

It is interesting to note that both model equations are depending on a derivative parameter ($x_2 = k_d$), while V_{max} adds one more dependency with the quantity of bulk capacitors (x_8 = *BlkC*).

IV. DoE for Power Delivery: Physical Approach

Based on our findings obtained in Section III, a laboratory verification with the same PD design on a physical platform implementation is conducted to validate if the dependencies are the same. Since the physical VR module has more factors available for configuration, we focus our interest on those factors similar to the ones used in the simulation approach. Table II shows the codification for each factor.

Following exactly the same DoE procedure used in Section II, the resulting model equations describing system's behavior for Vmin and Vmax are:

$$V_{min} \approx 1.3676 + 0.001826 x_8 \qquad (4)$$

$$V_{max} \approx 2.019 - 0.000047 x_1 - 0.000297 x_2 \qquad (5)$$

[2]SIMetrix/Simplis 7.20e (x64), Copyright © 2014 Simplis Technologies Ltd, 78 Chapel Street, Thatcham, Berkshire, RG18 4QN, UK, http://www.simetrix.co.uk/site/index.html

TABLE II. VARIABLES USED TO BUILD THE FFD FOR PHYSICAL IMPLEMENTATION

Factor	Equivalent Variable	(–1)	(+1)
$A = (x_1)$	k_p	100	250
$B = (x_2)$	k_d	250	450
$C = (x_3)$	k_i	100	250
$D = (x_4)$	k_{fp}	100	250
$E = (x_5)$	ATR_{h1}	no	yes
$F = (x_6)$	ATR_{h2}	no	yes
$G = (x_7)$	ATR_{kp}	0	56
$H = (x_8)$	K_{j_atrl}	0	56
$J = (x_9)$	*BlkC*	29%	100%
$K = (x_{10})$	*SR* (1-1000 A/µs)	slow	fast

where $x_8 = k_{\text{j\_atrl}}$ is one of the non-linear factors, while from PID's side, some compensation factors like $x_1 = k_\text{p}$ and $x_2 = k_\text{d}$ resulted meaningful. It should be highlighted that the quantity of bulk capacitors is not too relevant among the factors of the physical implementation. This fact indicates that it would be possible to look into a favorable scenario that reduces the quantity of capacitors needed. To validate that, we expanded our model to incorporate this additional factor, as follows

$$V_{\text{min}} \approx 1.3676 + 0.001826x_8 + 0.0198e^{-6}x_9 \quad (6)$$

$$V_{\text{max}} \approx 2.019 - 0.000047x_1 - 0.000297x_2 + 0.0091e^{-6}x_9 \quad (7)$$

It is seen that this new DoE model is now dependent on the number of bulk capacitors, x_9.

V. SYSTEM OPTIMIZATION: SIMULATION AND LABORATORY

In the previous two sections we described the methodology to find the most significant factors of a PD system for both scenarios: simulation and its physical implementation. As it is observed that there are some coincidences and discrepancies on the model equations obtained from the simulation and laboratory measurements.

Both scenarios indicate that a good PID compensation recipe is needed (k_p and k_d resulted significant factors), while the laboratory approach added one more non-linear parameter that needs fine tuning ($k_{\text{j\_atrl}}$). Also, in the case of the laboratory, the quantity of bulk capacitors was initially not too relevant, indicating a great opportunity to reduce costs. We adjusted our DoE linear regression model to include bulk capacitors as one more factor to consider in the physical PD optimization.

To optimize power delivery's system response from simulation and from the laboratory, we solve an optimization problem that minimizes a suitable objective function $u(\boldsymbol{x})$ with respect to variables $\boldsymbol{x}$, exploiting our response surface model $y(\boldsymbol{x})$ [9] (see flow diagram in Fig. 1), as follows:

$$\boldsymbol{x}^* = arg\ min_x\ u(\boldsymbol{x}) \quad (8)$$

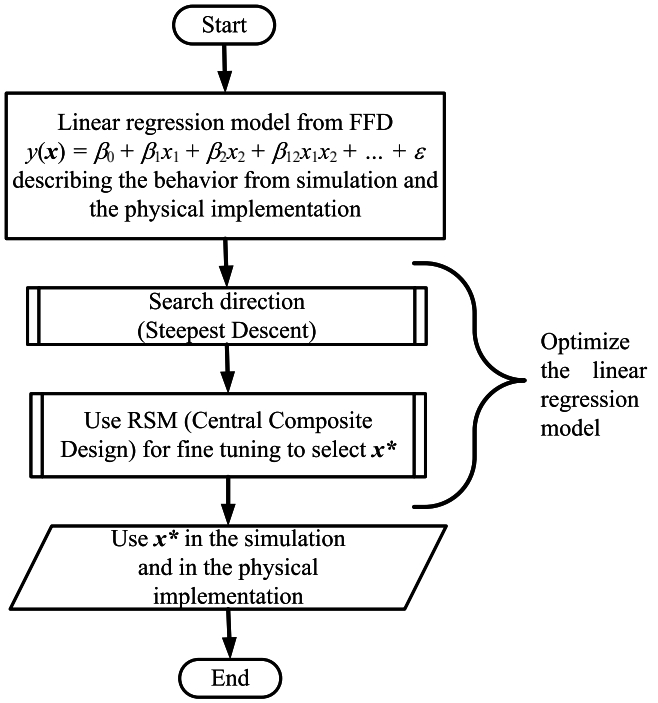

Fig. 1. Flow diagram illustrating the sequence followed in the implementation of RSM optimization technique.

$$u(\boldsymbol{x}) = [V_{\text{min}} - y(\boldsymbol{x})] + [y(\boldsymbol{x}) - V_{\text{max}}] \quad (9)$$

Central composite design (CCD) [9] is one of various RSM techniques. CCD consists on a factorial design 2^k or a FFD with n_F runs, 2^k axial runs or star and n_c central runs. The fundamental deployment of a CCD is based on sequential experimentation, *i.e.*, it is used a 2^k design to adjust the first order model. Since such model usually presents lack of adjustment, then, axial runs are added to incorporate some quadratic terms in the model. In this work we selected CCD as the method to develop the RSM models.

From Fig. 1, the first optimization step uses steepest descent to establish the direction that maximizes the system. Finally, the second step consists on applying the CCD technique to enhance the model around the optimal solution.

Table III, summarizes results before and after optimization for both scenarios (PD simulation and physical PD implementation). As it is observed in Table III, physical power delivery implementation needs 14% more capacitors than the simulation, although, still making feasible a 29% reduction of capacitors needed. Both scenarios (simulation and physical implementation) are evaluated under fast SR conditions before and after optimization.

From Table III, it is clear that silicon's V_{min} and V_{max} requirements are met, although, we need to ensure these results are valid from the VR's perspective. To ensure whether these results meet VR's voltage boundaries, it is needed to estimate maximum and minimum VR output voltage allowed.

The following equations estimate these requirements:

TABLE III. DOE RESULTING VOLTAGE LEVELS AND PEAK TO PEAK COMPARISON FOR SIMULATION AND PHYSICAL IMPLEMENTATION SCENARIOS BEFORE AND AFTER OPTIMIZATION

Environment's scenario		k_p	k_d	$kj_{\_atrl}$	*BlkC*	*SR*	V_{min} (V)	V_{max} (V)	Peak to peak (mV)
Simulation	before	135	330	N/A	100%	fast	1.64	1.85	209.95
	after	135	275	N/A	57%	fast	1.57	1.89	313.80
Laboratory	before	180	420	0	100%	fast	1.62	1.82	196.80
	after	124	450	38.5	71%	fast	1.58	1.88	300.00

$$VR_{\text{minb}} = V_{\text{nom}} - (I_{\text{max}} * LL) - VR_{\text{AC\_DC}} \quad (10)$$

$$VR_{\text{maxb}} = V_{\text{nom}} + (I_{\text{max}} * LL) + VR_{\text{AC\_DC}} \quad (11)$$

where VR_{minb} and VR_{maxb} are VR output voltage boundaries, V_{nom} is the nominal voltage given for the power rail's channel, Imax is the maximum current load, *LL* is the load line or equivalent resistance seeing by the system[3], and $VR_{\text{AC\_DC}}$ is the AC plus DC tolerance the VR can support, for this particular case ±22 mV. Using (11) and (12), the calculated output voltage boundaries are VR_{minb} = 1.58 V and VR_{maxb} = 1.98 V. Hence, from Table III, it is observed that the optimization results are marginally meeting minimum and maximum VR's voltage boundaries.

VI. CONCLUSION

DoE proved to be an effective technique to find the most significant factors for PD analysis and design, as well as to perform PDN optimization. Our simulations and physical laboratory measurements showed sufficiently good agreement for the optimized PDN. With this methodology, it is possible to reduce costs, since, from our physical platform implementation it was possible to remove 29% of the capacitors at the expense of a finding better VR's tuning recipe. As further step, a detailed DoE study on the frequency domain is desirable to ensure acceptable VR's stability criteria and bandwidth. Finally, more computationally efficient optimization techniques, such as those based on space mapping approaches, will be addressed in future work to enhance our power delivery design process.

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[3] The specific values of V_{nom}, I_{max}, and *LL*, are proprietary information from Intel Corporation.