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# Optimization of cylindrical textile organic field effect transistors using TCAD simulation tool

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**Abstract.** We used a commercial TCAD tool in order to simulate a cylindrical Textile Organic Field Effect Transistor (TOFET) and study the impact of different critical region sizes in its electrical characteristics. The simulation was based on models and parameters similar to those of previous simulations in Organic Thin Film Transistors. We have seen that it is potentially feasible to build transistors which can operate in low voltages by using typical materials. Even if some of the selected typical materials have to be replaced by others more suitable for practical use in the textile industry, the simulation is a good starting point for estimating the device typical operation and parameters. By optimizing critical region sizes of the device we conclude that the device should have an active layer thickness below 100 nm, channel length around 10µm and gate oxide thickness as small as possible (300 nm or less), in order to have optimum transistor performance.

## 1. Introduction

Previous research works in the area of electronic textiles have proved the possibility to construct Textile Organic Field Effect Transistors (TOFETs). More specifically, fibre-based transistors can be fabricated by applying different material layers on conventional textile fibres [4-8]. In our work we tried to simulate and evaluate the performance of a cylindrical fibre-based transistor by using a TCAD modelling - simulation tool [9]. Although the simulation of planar OTFT (Organic Thin Film Transistor) has been thoroughly studied [1-3], the literature regarding simulation of cylindrical fiber-based TOFET is still poor. Simulations are expected to give more ideal results, regarding the electrical characteristics (figure of merits) of the electronic devices, when compared with the real devices measured in the laboratory. However, simulation can be a very helpful tool for designing, predicting the performance and optimizing the device prior its construction in the laboratory, thus, facilitating the setting of targets that potentially can be achieved in the laboratory.

Our target was initially to achieve a “functional” (reliable and fast) simulation of the cylindrical TOFET, in order to evaluate the peculiarities, difficulties and restrictions of the simulation, and subsequently to examine, in a semi - theoretical approach, the feasibility to fabricate a TOFET operating under low voltages, which is extremely important for future applications in electronic wearable textiles.

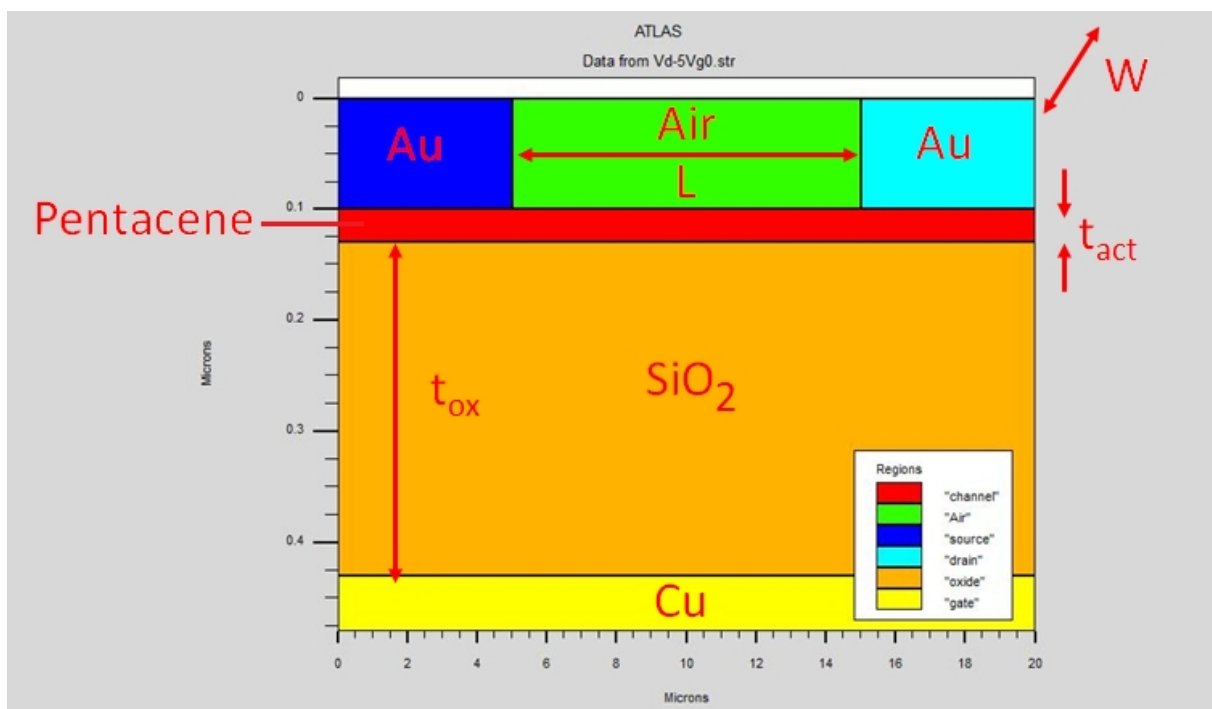


## 2. Simulated Devices

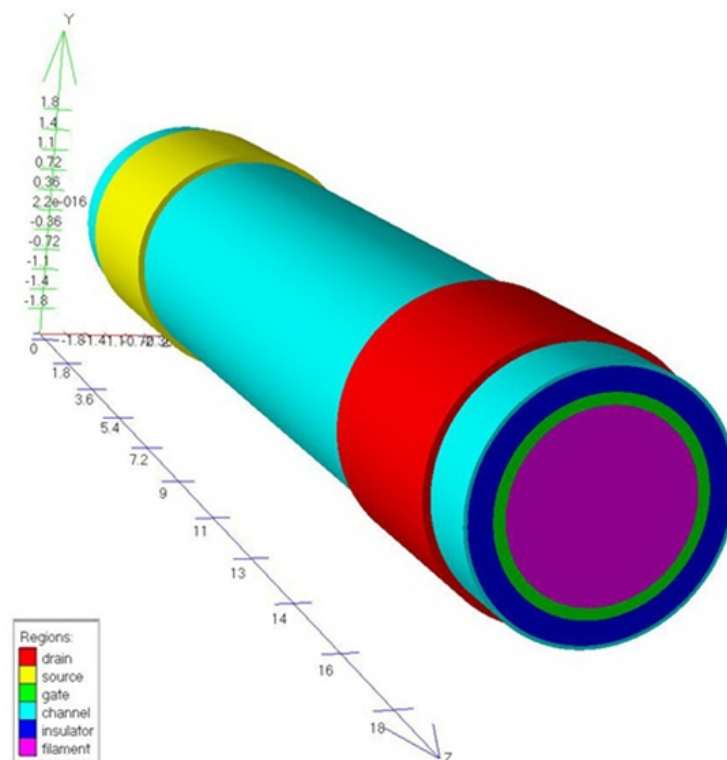
Regarding the materials used in the simulations, for the gate we considered a textile fiber coated with a layer of Copper. Alternatively, it could be used as coating layer of another highly conductive metal such as aluminum or a pure metallic stainless steel fibre [4,6,8]. For a fully organic device, textile the fiber can be coated with a layer of highly conductive polymer such as PEDOT:PSS [5,7]. For the dielectric material we considered a thin layer of Silicon oxide which can be deposited on the previous layer in order to encapsulate the gate [4,6]. Although silicon oxide due to its stiffness is not ideal for textile transistors, we have selected it because it is the typical gate dielectric used in semiconductors and hence was considered as more reliable for our first simulations approach. However, it can be replaced by other flexible organic materials with similar dielectric constants, such as Poly-ethylene therephtalate [5], PVP (Poly vinyl phenol) [3,6] and Polyimide [3,8]. For the active layer (semiconductive material) we selected Pentacene, mainly due to its relatively high mobility and its broad acceptance in the construction of organic devices [2-5,8]. Finally, for the source and drain contacts we selected Gold, which is the most commonly used in the implementations textile transistor in the laboratory [4-8]. For a fully organic device, gold can be replaced by a conductive polymer such as PEDOT:PSS [8].

Initially, we simulated a typical 2D top-contacted-bottom-gate OTFT (figure 1) in accordance with previous research works [10-14] and with characteristics (critical region sizes and materials) resembling the textile organic cylindrical transistors of our interest.

The structural parameters (critical region sizes) we considered for the initial 2D device, were, channel width  $W = 120 \mu\text{m}$ , channel length  $L = 10 \mu\text{m}$ , oxide thickness  $t_{\text{ox}} = 300 \text{ nm}$  and active layer thickness  $t_{\text{act}} = 50 \text{ nm}$ . For the 3D cylindrical TOFET the channel width depends on its radius ( $W \approx 2\pi R$ ), thus by considering a radius of  $20 \mu\text{m}$  the channel width is about  $125 \mu\text{m}$ , which is close to the channel width of the 2D device, while all the other critical region sizes are same to the 2D device.



**Figure 1.** 2D top-contacted-bottom-gate OTFT.



**Figure 2.** 3D cylindrical TOFET.

The organic material has a relatively high band gap of about 2.25 eV, a fact that makes the simulations more laborious and creates the need to use a higher level of bits, such as 90 or 128 bits, in order to achieve accuracy. In our simulations we set the affinity of the organic layer to 2.49 eV.

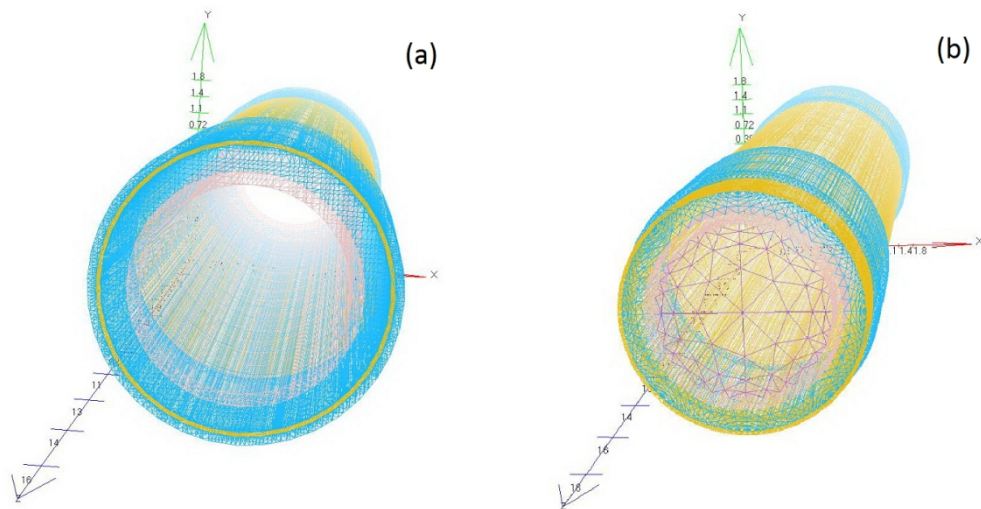
The simulations carried out in the 2D model are very fast (about 90 minutes for each device, estimating typical input and output characteristics), while the 3D simulations exhibit difficulties.

In order to have the best possible results, we utilized two different models for the construction of the 3D-meshes. The first one was implemented in the DEVEDIT subprogram of the ATLAS tool and is based in orthogonal coordinates (figure 3a), while the second one was implemented directly in the ATLAS tool and is based in cylindrical coordinates (figure 3b). In both cases simulations are conducted by ATLAS. In many cases the simulations stopped after several cut-backs, without reaching to a result. Although we expected better performance in the meshes constructed by ATLAS, because cylindrical coordinates fit perfect to the cylindrical geometry of the TOFET, the DEVEDIT's meshes were actually more effective, with less failures in finishing the simulations.

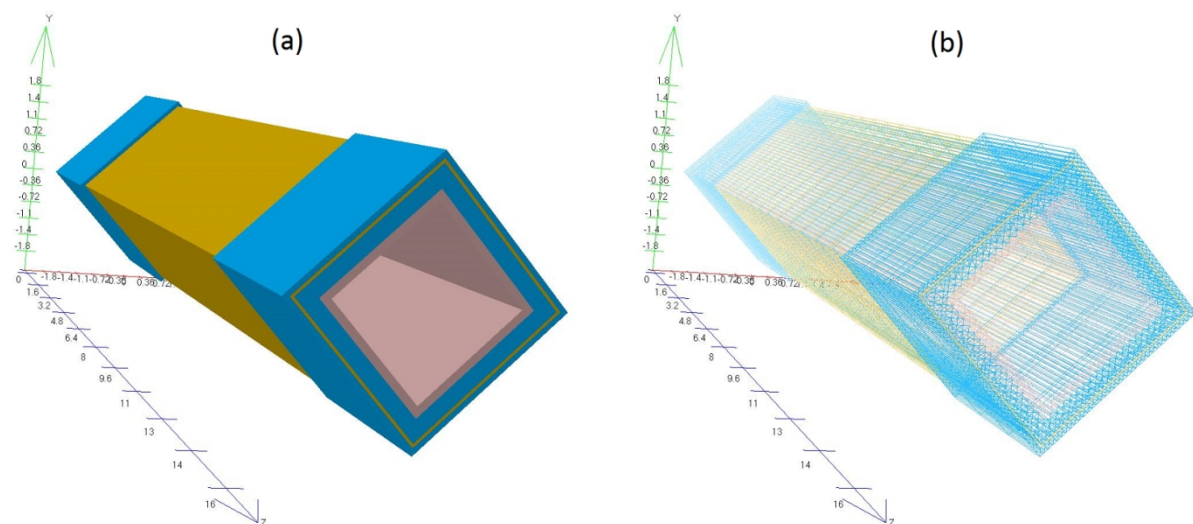
Usually the maximum number of nodes in a simulated device mesh is about 200000, while 25 to 40 planes are enough.

In the particular case of cylindrical TOFETs, the difference in the size magnitude of the core fibre radius ( $\sim\mu\text{m}$ ) and the layer's thicknesses ( $\sim\text{nm}$ ) created difficulties in the mesh construction of the devices, since best accuracy was required only in the very thin critical regions, such as the active channel and the gate oxide, and not in the entire volume of the simulated device which also includes the very large space occupied by the fibre. For this reason, we have also tested simulation scenarios by assuming the textile fiber as a cylindrical vacuum (figure 3a), confirming that it does not affect the final results and thus can be applied for practical reasons in order to speed up the simulation computing cycles.

We also simulated an orthogonal GAA (gate-all-around) 3D nanowire transistor (figure 4) and gradually transit it to a cylindrical one in order to see possible improvements in the electrical behavior.



**Figure 3.** Different mesh approaches of the 3-D cylindrical TOFET a) using DEVEDIT (Orthogonal coordinates) – hollow in the center and b) using ATLAS (cylindrical coordinates).



**Figure 4.** Orthogonal 3D nanowire transistor (Gate All Around – GAA) created in DEVEDIT, rectangular structure of the TOFET: (a) solid view, (b) mesh view.

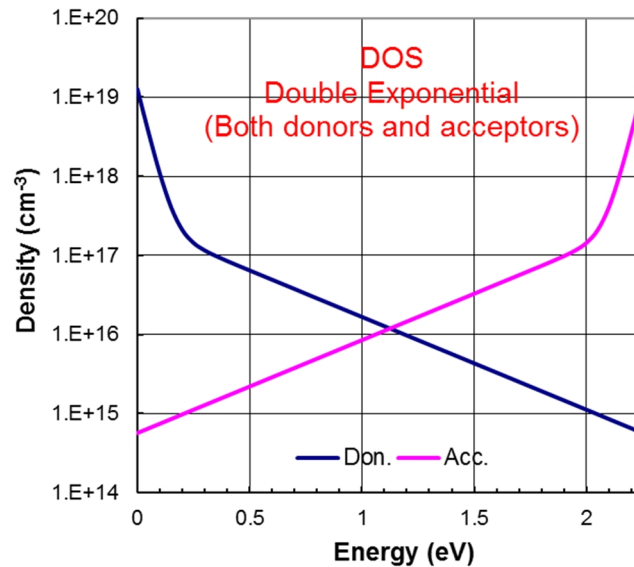
### 3. Models considered in the simulation

The Poisson's equation, carrier continuity equations and the drift-diffusion transport equations were concurrently solved in the simulation. Langevin recombination rate is also included in the carrier continuity equations [9].

A double exponential density of states distribution (DOS) in the organic layer is assumed using the parameters  $N_{TD} = 1.25 \cdot 10^{19} \text{ cm}^{-3} \text{ eV}^{-1}$ ,  $kT_{TD} = 0.038 \text{ eV}$  (tail states) and  $N_{DD} = 2.5 \cdot 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ ,  $kT_{DD} = 0.37 \text{ eV}$  (deep states), as depicted in figure 5.

We have also considered -in some cases- fixed interface charges in the organic layer – oxide interface having densities up to  $10^{12} \text{ cm}^{-2}$ .

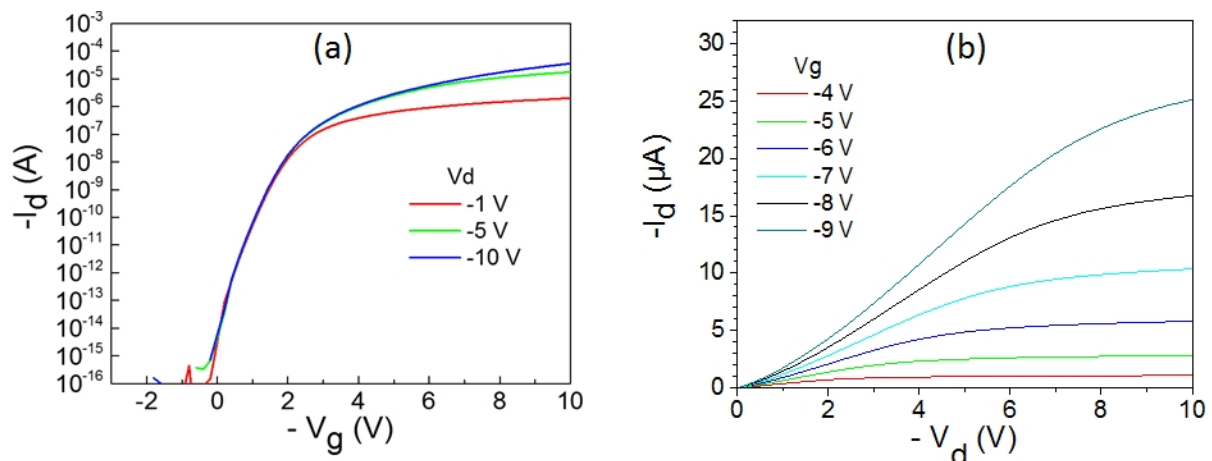
The Poole-Frenkel model has been used for the mobility estimation, which takes into account the electric field dependency of the mobility (parameters  $\text{hopp.beta}=1.5$   $\text{hopp.gamma}=5E7$   $\text{hopp.v0}=1E11$ ) [9]. The low field electron mobility is set to  $1 \text{ cm}^2/(\text{Vs})$ .



**Figure 5.** Double exponential DOS of the TOFET, both for donors and acceptors.

#### 4. Typical results

The electrical behavior of the aforementioned device ( $W = 120 \mu\text{m}$ ,  $L = 10 \mu\text{m}$ ,  $t_{\text{ox}} = 300 \text{ nm}$ ,  $t_{\text{act}} = 50 \text{ nm}$ ), restricted to voltages less than 10 V, is presented in figures 6a (input characteristics) and 6b (output characteristics). Analyzing the input characteristics we estimated (for this device) the values of the threshold voltage  $V_{\text{th}} = 2.33 \text{ V}$ , the subthreshold slope  $SS = 297 \text{ mV/dec}$ , the on-current  $I_{\text{on}} = 3.5 \cdot 10^{-5} \text{ A}$  and the off-current  $I_{\text{off}} = 5.9 \cdot 10^{-15} \text{ A}$ . The  $I_{\text{on}}/I_{\text{off}}$  ratio is about  $6 \cdot 10^9$ , while the maximum transconductance is  $g_{\text{m-max}} = 12.4 \mu\text{S}$ .



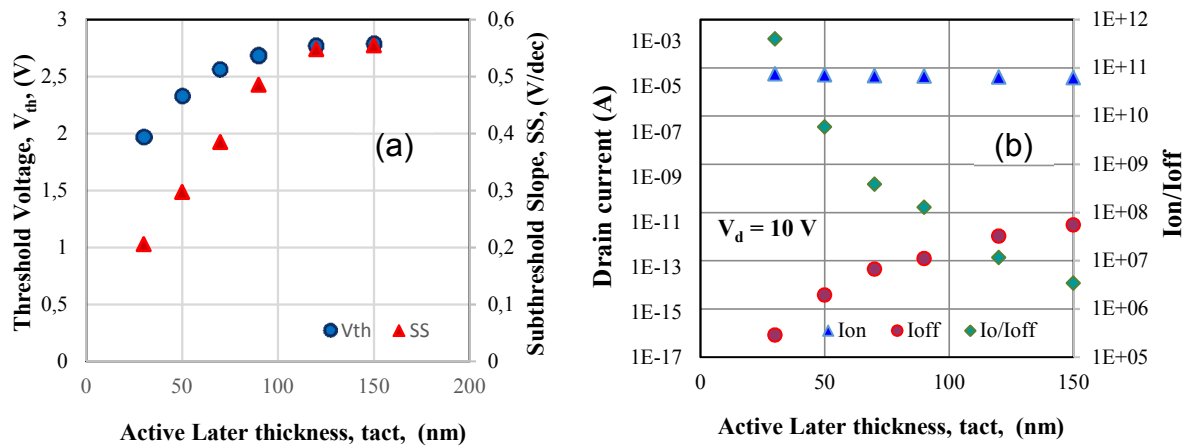
**Figure 6.** Typical Input (a) and output (b) characteristics of the TOFET.

#### 5. Device optimization

The influence of the critical region sizes and construction parameters in the performance of the simulated device has been studied, by simulating devices which differ in these characteristics and comparing their performance by means of figures of merit for the devices.

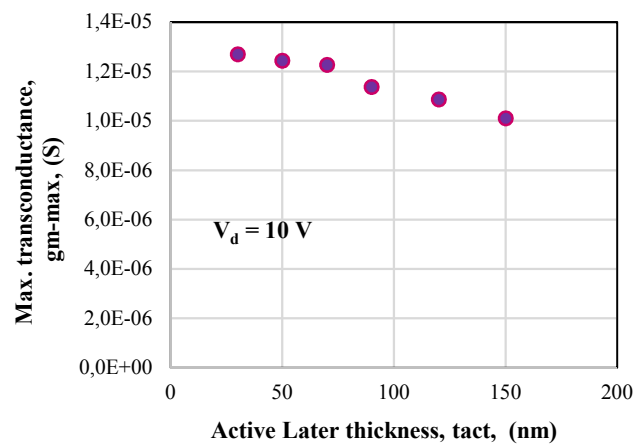
In respect to the active layer thickness  $t_{\text{act}}$ , we observe that smaller  $t_{\text{act}}$  results in smaller threshold voltage ( $V_{\text{th}}$ ) and subthreshold slope (SS). For  $t_{\text{act}}$  larger than 100 nm there is no significant change in both parameters (figure 7a). The on-current remains about the same, whilst there is a great change in

the off-current with significant impact in their ratio  $I_{on}/I_{off}$ . The  $I_{on}$  and  $I_{off}$  are defined as the drain currents at  $V_g$  equal to -10 and 0 V respectively at high  $V_d$  (-10 V). We observe that  $I_{on}/I_{off}$  ratio becomes better for smaller active layer thickness (figure 7b).



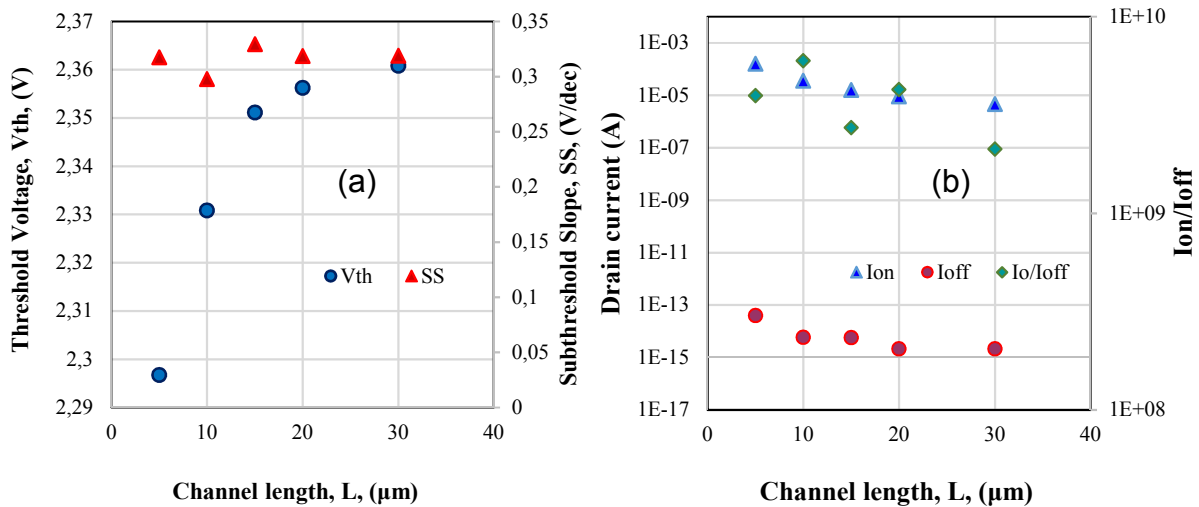
**Figure 7.** (a) Threshold voltage and Subthreshold slope versus  $t_{act}$ , (b) On-current, off-current and their ratio versus  $t_{act}$ .

Maximum transconductance is improved in lower  $t_{act}$ , with optimum performance observed in  $t_{act}$  smaller than 100 nm (figure 8).

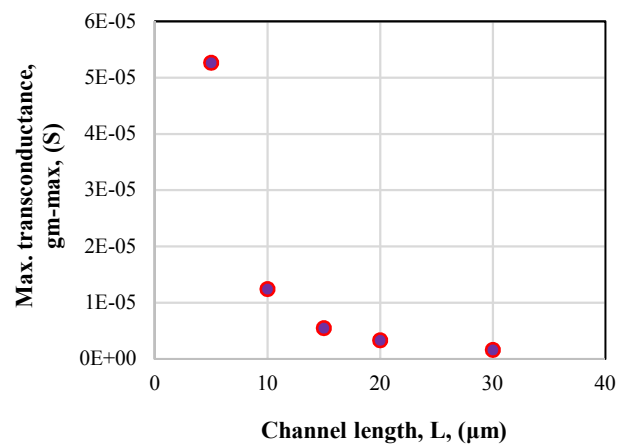


**Figure 8.** Maximum transconductance versus  $t_{act}$ .

By changing the channel length  $L$ , we observe that within the range of 5-30  $\mu\text{m}$ , the SS remains about at 300 mV/decade, and there is a relatively small change in  $V_{th}$  (figure 9a). The currents  $I_{on}$ ,  $I_{off}$  and their ratio become higher as  $L$  gets smaller (figure 9b). Maximum transconductance gets significantly higher as  $L$  gets smaller (figure 10).



**Figure 9.** (a) Threshold voltage and Subthreshold slope versus channel length  $L$ , (b) On-current, off-current and their ratio, versus channel length  $L$ .

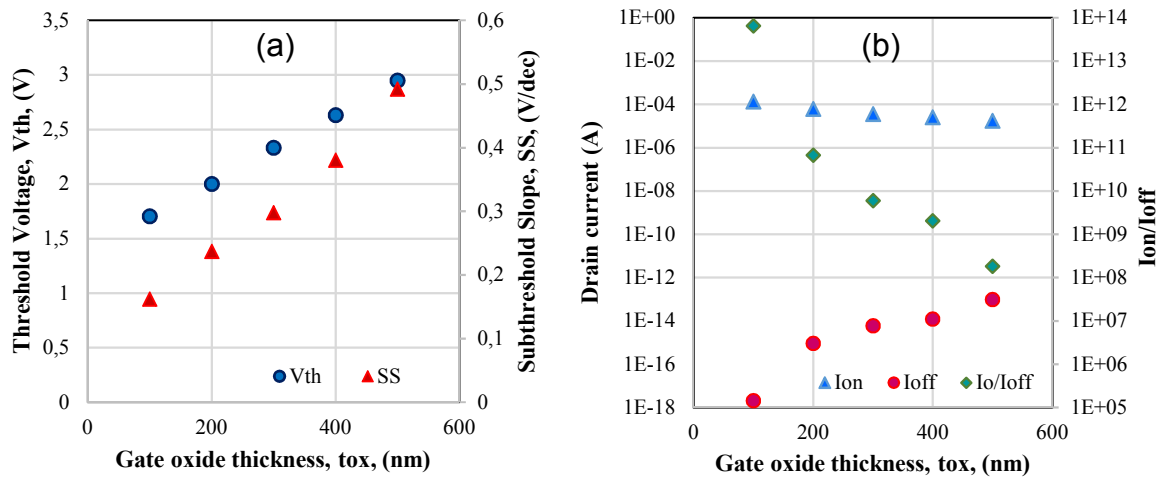


**Figure 10.** Maximum transconductance versus channel length  $L$ .

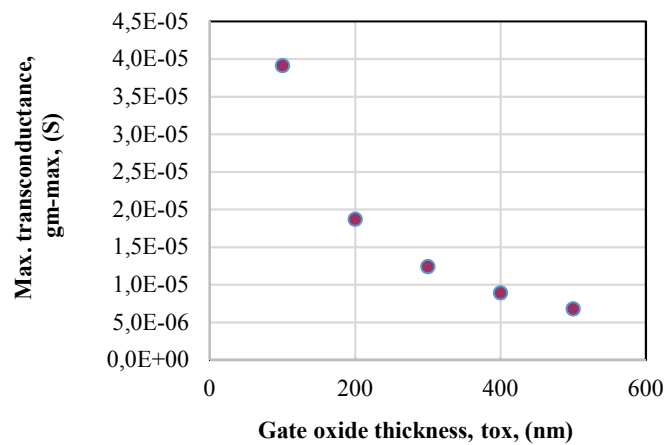
Regarding the oxide layer thickness  $t_{ox}$ , we observe a linear trend in both  $V_{th}$  and  $SS$  for  $t_{ox}$  between 100 nm and 500 nm (figure 11a). Considering  $I_{on}$ ,  $I_{off}$  currents and their ratio, obviously the devices perform better at smaller  $t_{ox}$  (figure 11b), and the same happens with the maximum transconductance  $g_{m-max}$  (figure 12).

We also examined the influence of different metal gates (figure 13a) and the existence of interface charges to the (figure 13b) input characteristics of the devices. Both metal gate work function and the interface charges (between the channel and the insulator) affect directly the threshold voltage, and subsequently the rest of the electrical characteristics of the devices.

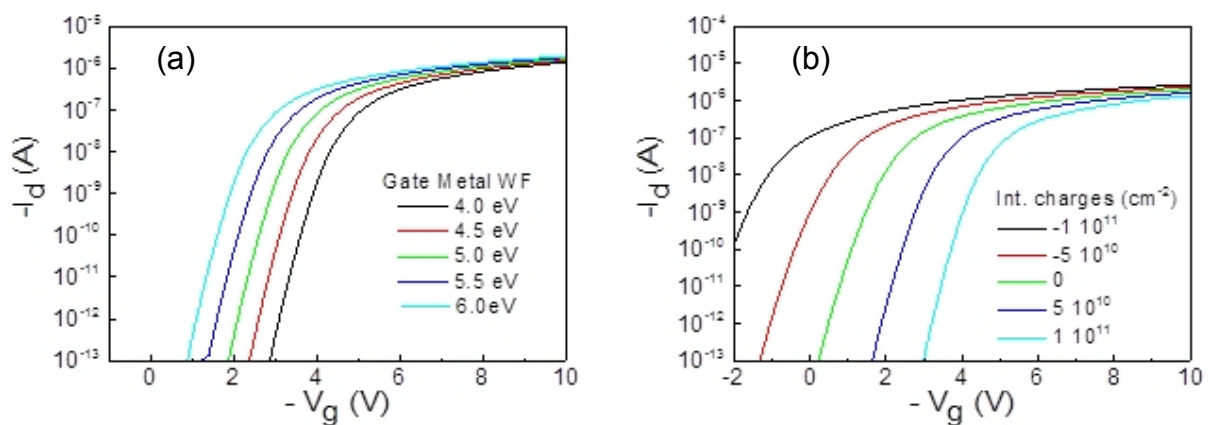




**Figure 11.** (a) Threshold voltage and Subthreshold slope and (b) on-current, off-current and their ratio (at  $V_d = -10$  V), versus oxide thickness  $t_{ox}$ .



**Figure 12.** Maximum transconductance versus oxide thickness  $t_{ox}$ .



**Figure 13.** (a) Metal gate work function, (b) Interface charges

## 6. Conclusions

We have initially estimated the device's performance in a "best case scenario" prediction of quality TOFETs which can be fabricated in the near future assuming typical values and parameters. Further improvement has been achieved by optimizing critical region sizes of the device such as channel width, channel length, gate oxide thickness and active layer thickness. For best electrical performance we concluded that the device should have an active layer thickness below 100 nm and gate oxide thickness as small as possible (300 nm or less). A channel length around 10 $\mu$ m is optimal, but even larger transistors will have fairly good performance, which is convenient for textile constructions. Most important, all these devices will be able to operate under 10 V, which is the operational voltage limit we set -considering power supply and human safety issues- as suitable for potential wearable textile applications.

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