IMPLEMENTATION OF HARRIS CORNER DETECTOR ON FPGA

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An appreciation to all who made this possible
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ABSTRACT

Harris Corner Detector (HCD) algorithm is widely used in many applications of image processing. Its performance with noisy images exceeds many other methods, in terms of accuracy and stability. Various methods are used to compare images and detect moving objects such as block matching but these methods are slow and have less accuracy. Moreover, the implementation of HCD has been proven to be computationally intensive, therefore, real-time streaming is difficult to achieve with sequential software implementation. This report presents the hardware implementation of HCD using Field-Programmable Gate Array (FPGA). The targeted board for the design is DE2-115 FPGA development board with an Altera Cyclone IV device. The architecture was tested using a SystemVerilog test-bench, enveloped by a MATLAB test-bench. The accuracy of the results obtained was tested visually and compared with the results of the same algorithm implemented in MATLAB. A maximum operational frequency of 170 MHz was achieved. The system uses 40% of the board's logic elements. Resource utilization and timing performance are considerably balanced compared to recent works.

ABSTRAK

Algoritma Harris Corner Detector (HCD) digunakan secara meluas untuk aplikasi pemprosesan imej. Prestasinya untuk imej hingar melebihi kebanyakan kaedah yang lain, dari segi ketepatan dan kestabilan. Pelbagai kaedah digunakan untuk membandingkan imej dan mengesan pergerakan objek seperti pemadanan blok tetapi kaedah-kaedah tersebut adalah perlahan dan kurang tepat. Selain itu, pelaksanaan HCD terbukti memerlukan proses pengkomputeran yang intensif, maka strim dalam masa nyata adalah sukar untuk dicapai dengan pelaksanaan perisian secara berjujukan. Laporan ini membentangkan pelaksanaan perkakasan HCD menggunakan *Field-Programmable Gate Array* (FPGA). Papan litar yang disasarkan untuk reka bentuk HCD adalah papan pembangunan FPGA DE2-115 dengan peranti Cyclone IV Altera. Senibina ini telah diuji menggunakan penanda aras SystemVerilog, dengan dikelubungi oleh penanda aras MATLAB. Kejituan dalam keputusan yang diperolehi telah diuji secara visual dan dibandingkan dengan keputusan algoritma yang sama yang dilaksanakan dalam MATLAB. Frekuensi pengendalian maksimum 170 MHz telah dicapai. Sistem ini menggunakan 40% unsur logic papan . Penggunaan sumber dan prestasi pemasaan adalah lebih jauh seimbang berbanding pelaksanaan yang terkini.

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LIST OF ABBREVIATIONS

HCD	-	Harris Corner Detector
NMS	-	Non-Maximum Suppression
ROI	-	Region of Interest
DFG	-	Dataflow Graph
HDL	-	Hardware Description Language
RTL	-	Register Transfer Level
RAM	-	Random Access Memory
FPGA	-	Field Programmable Gate Array
ANMS	-	Adaptive Non-Maximum Suppression

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CHAPTER 1

INTRODUCTION

1.1 Background

The main overall goal of computer vision is to model and imitate the visual system of the human through computer software and hardware at different levels. The replication of human visual system on computational platform has proven to be problematic and challenging. Computer vision is the field of reconstructing the 3D world from 2D images and computer graphics is pursuing the opposite direction by designing 2D images to simulate the 3D world. However, 3D details are lost during image transformation from 3D world to 2D images which lead to difficulties in analysis of image processing. Image processing is in the middle connecting the computer vision and computer graphics [1].

High-level computer vision tasks and systems like motion estimation rely on the extraction of low-level processes such as image features, interest point and corner detection which represent a small portion of image pixels [2, 3]. Interest points retain similar characteristics even after image transformation, which has to be robustly detected [4]. Image features are used in many applications such as object recognition. The performance of such applications relies on robustness and efficiency on the low-level processes. Corners are intuitively distinguishable features; they represent sudden change of intensity levels in more than one direction on the image [5]. A corner detector should satisfy the performance requirements of real-time video streaming applications.

Harris corner detector algorithm in [6] is widely used in many applications of image processing. Its performance with noisy images exceeds many other methods, in terms of accuracy and stability, such as SUSAN and Minimum Intensity Change (MIC) [5]. Despite their inherent differences, the computation is similar for most interest point detectors where window-based image processing operators are applied locally on every image position. This makes the extraction process computationally intensive. High-speed corner detection is in high demand for computer vision systems in applications such as motion detection and object recognition [7]. This report presents the hardware implementation of Harris corner detector algorithm on Field Programmable Gate Array (FPGA).

1.2 Motivation

There are some methods used for corner detection to find corners in images. However, the performance of these methods is low especially when implementing noisy images. The implementation of Harris corner detector has been proven to be computationally intensive. Therefore, real-time streaming is difficult to achieve with sequential software implementation. This work proposes a Harris corner detector hardware implementation with high throughput and accuracy to find the corners in an input image using FPGA.

1.3 Objectives

The aim of this work is to present the design and implementation of Harris corner detector on FPGA. To achieve this aim, some objectives must be accomplished:

1. To design hardware blocks of the system.
2. To apply pipelining to increase throughput.
3. To optimize for resource utilization, throughput and latency.
4. To verify and visually compare the result with MATLAB.

1.4 Scopes

The scope of this research is limited to the design and implementation of Harris corner detector on FPGA. The targeted FPGA board is Terasic DE2-115 Development Kit and the input image is limited to 256x256 gray scale image. Software used in this project are MATLAB, Quartus II and ModelSim.

1.5 Report Outline

Chapter 1 introduces the background of Harris corner detector. Chapter 2 explains the literature review and the related work of Harris corner detector which has been done prior to this work. Chapter 3 describes the methodology and design of the proposed hardware architecture of Harris corner detector. Each stage of the hardware implementation is explained. Chapter 4 discusses the result of the hardware implementation compared to MATLAB and the analysis of the result. Chapter 5 summarizes the project report and proposes recommendations for future work.

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