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From the organic thin film transistor to the 3-D textile organic cylindrical transistors – perspectives, expectations and predictions

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Abstract. In this paper we examine the possibility to simulate and study the behaviour of a fiber-based Textile Transistor in a commercial TCAD system. We also examine the capability of such transistors to operate in sufficiently low voltages, aiming to the potential realization of low-voltage wearable textiles in the future. We have seen that it is potentially feasible to build transistors which can operate in low voltages by using typical materials. Even if some of the selected typical materials have to be replaced by others more suitable for practical use in the textile industry, the simulation is a good starting point for estimating the device typical operation and parameters.

1. Introduction

The ultimate target for the electronic textiles of the future is the complete integration of electronic components and circuits into fibers and textile structures. Expectedly, the leading electronic component in this research area of electronic textiles is the OFET (Organic Field Effect Transistor). Following the tradition of naming each transistor type with an acronym, we introduced the acronym TOFET (Textile Organic Field Effect Transistor) for those OFETs that are fabricated by using a textile structure. Although the modelling and simulation of planar OTFT (Organic Thin Film Transistor) have been thoroughly studied and well established in the current literature [1-3], the simulation of cylindrical fiber-based TOFET is still a challenging task. Our research focuses in the TCAD modelling and simulation of a cylindrical fiber-based TOFET, which potentially can be integrated into a textile woven structure as suggested in numerous references [4-8].

Simulation scenarios have been performed in a commercial TCAD (Silvaco-ATLAS) tool [9]. The simulation model is based in a cylindrical structure, which has been successfully applied and well described in previous research works [4-8].

The gate is either a metallic fiber, such as aluminum and stainless steel [4,6,8] or an organic textile fiber coated with a layer of metal or highly conductive polymer, such as PEDOT:PSS [5,7]. In our model we selected the case of a textile fiber coated with a layer of copper. The material of the textile fiber can theoretically be of any type and does not really affect the characteristics of the simulated TOFET. We have also tested simulation scenarios by assuming the textile fiber as a cylindrical

vacuum, confirming that this assumption does not affect the final results and can be applied for practical reasons in order to speed up the simulation computing cycles.

For the dielectric material we considered a thin layer of Silicon oxide which can be deposited to encapsulate the gate [4,6]. Due to its stiffness silicon oxide is not an ideal dielectric for textile transistors and can be replaced by other flexible organic materials with similar dielectric constants, such as Poly-ethylene therephtalate [5], PVP (Poly vinyl phenol) [3,6] and Polyimide [3,8]. However, in our simulation we used silicon dioxide since it is a typical gate dielectric used in semiconductors.

For the active layer (semiconductor) we selected Pentacene, mainly due to its (relatively) high mobility and its broad acceptance in the construction of organic devices [2-5,8]. The Pentacene layer can be applied by thermal evaporation as described in numerus papers [4-6,8].

Finally, for the source and drain contacts we have used Gold, which is the most commonly reported in textile transistor implementations [4-8]. Generally, the source and drain contacts are formed by depositing metals or conductive polymers on the active layer, by means of evaporation or soft lithography techniques. A conductive polymer that could replace gold is PEDOT:PSS [8].

2. Simulations

Initially, we confirmed previous results by simulating OTFTs (figure 1) with characteristics (critical region sizes and materials) resembling the textile organic cylindrical transistors of our interest (displayed in figure 2). The simulation is based on models, parameters and measurements similar to those of previous simulations in OTFTs [10-14]. More specifically, the Poisson's equation, carrier continuity equations and the drift-diffusion transport equations were concurrently solved in the simulation. Langevin recombination rate is also included in recombination terms in the carrier continuity equations [9]. A double exponential density of states distribution (DOS) in the organic layer is assumed using the parameters $N_{TD} = 1.25 \ 10^{19} \ cm^{-3} \ eV^{-1}$, $kT_{TD} = 0.038$ eV (tail states) and $N_{DD} = 2.5 \ 10^{17} \ cm^{-3}eV^{-1}$, $kT_{DD} = 0.37$ eV (deep states). We have also considered –in some cases- fixed interface charges in the organic layer – oxide interface having densities about $10^{12} \ cm^{-2}$. The Poole-Frenkel model has been used for the mobility estimation, which takes into account the electric field dependency of the mobility (parameters hopp.beta=1.5 hopp.gamma=5E7 hopp.v0=1E11) [9]. The low field electron mobility is set to 1 cm^2/(Vs).

The initial device we considered had the following structural parameters: W = 120 μm (channel width), L = 10 μm (channel length), $t_{ox} = 300$ nm (oxide thickness) and $t_{act} = 50$ nm (active layer thickness).
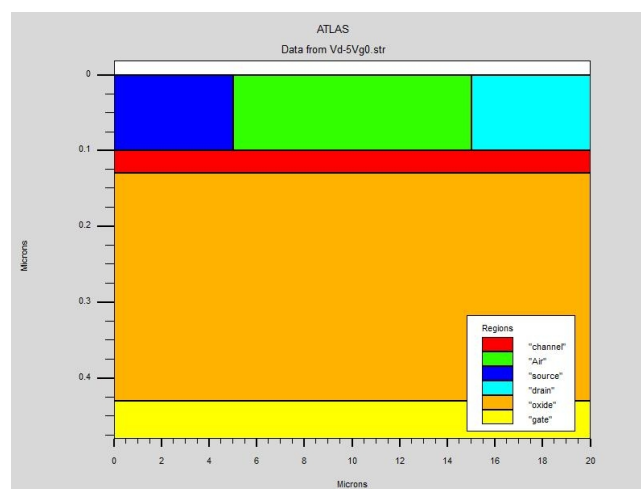

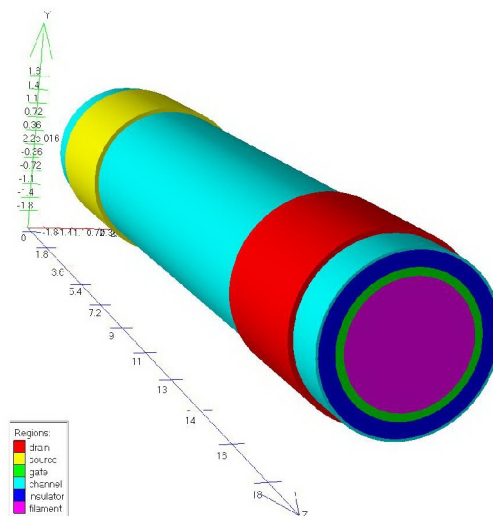**Figure 1.** The bottom-gate OTFT architecture, used for the simulations.

Figure 2. A 3-D view of the cylindrical TOFET, resembling the TFET.

The organic material has a relatively high band gap (2.25 eV), a fact that makes accurate simulations more laborious and probably a higher level of bits is needed in the simulations (such as 90 or 128 bits) to guarantee this. The affinity of the organic layer was set to 2.49 eV.

The simulations carried out in 2D were very fast (about 90 minutes for each device, estimating typical input and output characteristics), while the 3D simulations had difficulties. The difference in the size magnitude of the yarn radius (~μm) and the layer's thicknesses (~nm) created difficulties in the mesh construction of the devices, when trying to obtain relatively good accuracy in all cases, whilst best accuracy was required only in critical regions such as the active channel and the gate oxide.

In order to have the best possible results we considered two different (3D) meshes, one using the DEVEDIT subprogram and one implementing the device within ATLAS. In both cases simulations are conducted by ATLAS. In many cases the simulations stopped after several cut-backs of the simulator and no results were achieved. We expected to have better results in the meshes constructed by ATLAS, because we were able to design it using cylindrical coordinates (figure 3b), which fits perfect to the geometry of the TOFET. However the DEVEDIT's meshes were more effective (less cases that stopped without finishing the simulations – thus without results). We tried also to gradually transit from the orthogonal 3D nanowire transistor (figure 4) to the cylindrical one and see the possible improvements in their electrical behaviour.
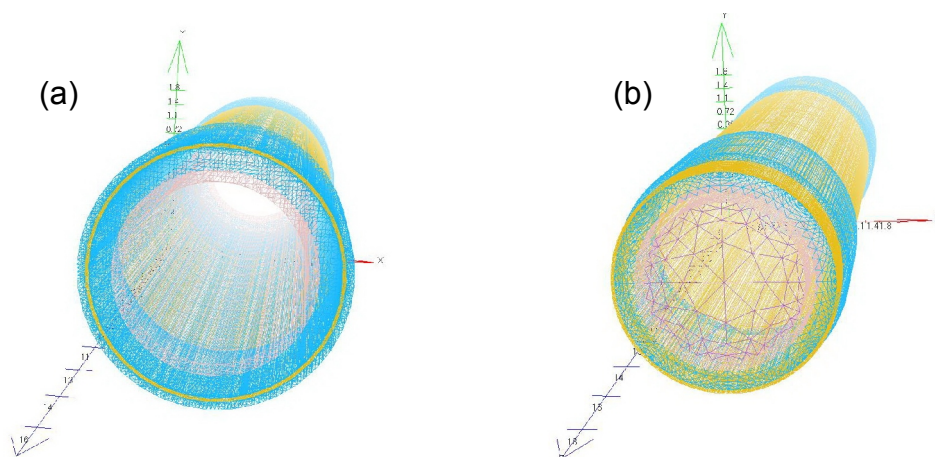

Figure 3. Different mesh approaches of the 3-D cylindrical TOFET a) using DEVEDIT (Orthogonal coordinates) – hollow in the centre and b) using ATLAS (cylindrical coordinates).
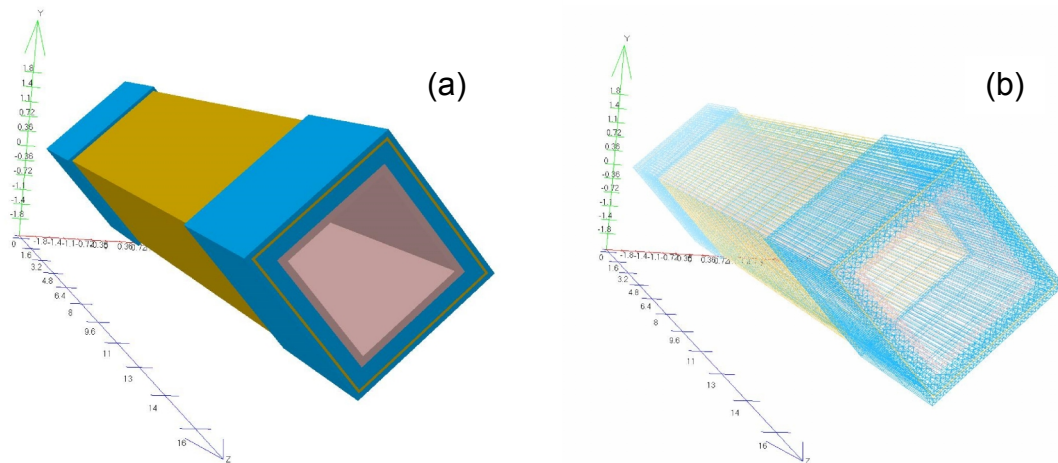
Figure 4. Rectangular structure of the TOFET (a), showing also the mesh used (b), created in DEVEDIT.

3. Results and discussion

We restricted our simulations up to voltages of 10 V, to examine the possibility to use the device in practical wearable textile applications. In figure 5a we can see the input characteristics of the OTFT (drain current I_d versus gate voltage V_g) with dimensions W = 120 μm, L = 10 μm, t_{ox} = 300 nm and t_{act} = 50 nm. In figure 5b we can see the output characteristic of the device (drain current I_d versus drain voltage V_d) for the same device.
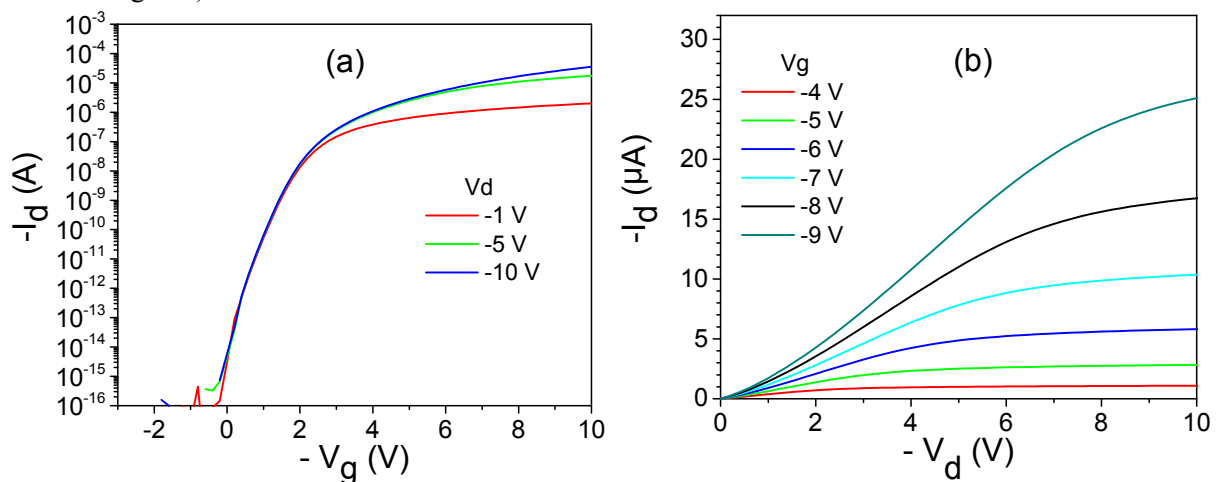

Figure 5. Input (a) and output (b) characteristics of the OTFT.

The device, as described in more details in reference [15], has a threshold voltage V_t = 2.33 V, subthreshold slope SS = 297 mV/dec, on-current I_{on}= 3.5 10^{-5} A, off- current I_{off} =5.9 10^{-15} A (both at V_d=-10 V) and an Ion/Ioff ratio about 6 10^9, while the maximum transconductance is g_{m-max} = 12.4 μS. Comparison with the 3D TOFET only shows a (small) improvement in favour of the 3D nanodevice – as expected – since the cylindrical structure has better electrostatic control, thus better electrical characteristics of the device. For example the equivalent TOFET has SS = 280 mV/dec and I_{on}/I_{off} = 8 10^9.

4. Conclusions

By using typical values for the device simulation of the TOFET, we have estimated the device's performance in a "best case scenario" prediction of quality TOFETs which can be fabricated in the

near future. These devices will be able to operate under 10 V, which is the operational voltage limit we consider as suitable for potential wearable textile applications. We have omitted in our simulation effects such as surface roughness of the layers, interface charges and high series resistances in the devices. Thus, the simulation seems to be optimistic though still realistic. Furthermore, possible improvements can trade off for the "optimistic assumptions" and even improve the total electrical behaviour of the devices. Such improvements would be a better effective mobility in the devices – we used 1 cm^2/V/s, while higher values have been reported (about 5 cm^2/V/s), in high quality transistors using also pentacene. Another possibility is to use thinner gate dielectrics, or even high-k materials. Moreover, the structure could change, by adding another gate between Source and Drain, making it a double-gate device.

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