Journal of Applied Physics

Exploring conductivity in *ex-situ* doped Si thin films as thickness approaches 5 nm

Cite as: J. Appl. Phys. **125**, 225709 (2019); https://doi.org/10.1063/1.5098307
Submitted: 01 April 2019 . Accepted: 01 June 2019 . Published Online: 14 June 2019

John MacHale, Fintan Meaney, Noel Kennedy, Luke Eaton, Gioele Mirabelli, Mary White, Kevin Thomas, Emanuele Pelucchi, Dirch Hjorth Petersen, Rong Lin, Nikolay Petkov, James Connolly, Chris Hatem, Farzan Gity, Lida Ansari, Brenda Long, and Ray Duffy

Journal of Applied Physics ARTICLE scitation.org/journal/jap

Exploring conductivity in *ex-situ* doped Si thin films as thickness approaches 5 nm

Cite as: J. Appl. Phys. **125**, 225709 (2019); doi: 10.1063/1.5098307
Submitted: 1 April 2019 · Accepted: 1 June 2019 ·
Published Online: 14 June 2019

John MacHale,[1,a)] Fintan Meaney,[1] Noel Kennedy,[2] Luke Eaton,[2] Gioele Mirabelli,[1] Mary White,[1] Kevin Thomas,[1] Emanuele Pelucchi,[1] Dirch Hjorth Petersen,[3] Rong Lin,[4] Nikolay Petkov,[5] James Connolly,[6] Chris Hatem,[7] Farzan Gity,[1] Lida Ansari,[1] Brenda Long,[1,2] and Ray Duffy[1,a)]

AFFILIATIONS

[1]Tyndall National Institute, University College Cork, Lee Maltings, Cork T12 R5CP, Ireland
[2]School of Chemistry, University College Cork, Cork T12 K8AF, Ireland
[3]Department of Physics, Technical University of Denmark, Fysikvej, Bld. 307, DK-2800 Kongens Lyngby, Denmark
[4]CAPRES—A KLA Company, Scion-DTU, Bld. 373, DK-2800 Kongens Lyngby, Denmark
[5]Cork Institute of Technology, Bishopstown, Cork T12 P928, Ireland
[6]Applied Materials, Lee Maltings, Cork T12 R5CP, Ireland
[7]Applied Materials, Gloucester, Massachusetts 01930, USA

[a)]**Authors to whom correspondence should be addressed:** john.machale@tyndall.ie and ray.duffy@tyndall.ie

ABSTRACT

Silicon (Si) has been scaled below 10 nm in multigate and silicon-on-insulator (SOI) device technologies, but clearly Si thickness cannot be reduced indefinitely, as we will run out of atoms eventually. As thickness approaches 5 nm, surfaces and interfaces will significantly impact the electrical behavior of Si, and surface physics cannot be discounted. Below that, bulk material properties will be altered considerably in the few-monolayer limit. One of the most basic defining properties of a semiconductor is its conductivity. To improve conductivity, while inducing a channel by appropriate biasing, it is necessary to define an accurate impurity doping strategy to reduce parasitic resistance. In this paper, we investigated the changing electrical conductivity of SOI films as a function of the Si thickness, in the range of 3–66 nm. SOI films were *ex situ* doped using three different approaches: liquid/vapor phase monolayer doping of phosphorus using allyldiphenylphosphine, gas-phase doping of arsenic using arsine (AsH_3), and room-temperature beam-line ion implantation of phosphorus. The circular transfer length method and micro-four-point probe measurements were used to determine the resistivity of the Si films, mitigating the contribution from contact resistance. The resistivity of the Si films was observed to increase with decreasing Si film thickness below 20 nm, with a dramatic increase observed for a Si thickness at 4.5 nm. This may drastically impact the number of parallel conduction paths (i.e., nanowires) required in gate-all-around devices. Density functional theory modeling indicates that the surface of the Si film with a thickness of 4.5 nm is energetically more favorable for the dopant atom compared to the core of the film.

I. INTRODUCTION

The semiconductor industry has been based on Si device scaling for many decades. The motivation for scaling Si is well known, as the reduced dimensions can lead to increased field-effect transistor (FET) device (logic) performance with lower power consumption, thereby enabling a vast array of consumer electronic products. While other materials such as Ge, III-Vs, and 2D materials have threatened to replace Si in FET device channels,[1–3] it remains at the core of modern digital logic transistors and circuits.

Si has been scaled below 10 nm in multigate[4,5] and silicon-on-insulator (SOI) device technologies,[6,7] but its thickness cannot be reduced indefinitely and larger surface-to-bulk ratios will impact the behavior of Si. In general, surface physics cannot be discounted as thickness approaches 5 nm.[8] It is known that effects must be considered at these scales such as carrier surface scattering, dielectric screening,[9] interface states,[10] as well as decreased doping efficiency,[11] increased dopant trapping,[12] and an increase in Si bandgap.[13] If not properly controlled, or at least understood, these

factors may inhibit proper semiconductor operation. A systematic experimental study of conductivity vs Si thickness is still lacking, particularly in relation to conventional and nonconventional *ex situ* doping techniques.

It is the aim of this work to systematically apply three different *ex situ* doping techniques to SOI samples with thicknesses ranging from 3 nm to 66 nm. These doping techniques are based on ion implant,[14] liquid/vapor-source in-diffusion,[15,16] and gas-source in-diffusion[17] and are verified on bulk Si samples in parallel. Conductivity is primarily determined by electrical testing of transfer length method structures and verified by a micro-four-point probe (μ4PP).

II. EXPERIMENTAL

Figure 1 is a summary of the process sequence used to fabricate and dope the SOI samples with a range of different Si film thicknesses. SOI wafers with nominally undoped 66 nm of Si on top of 145 nm of buried oxide were used as the starting point to obtain the required ultrathin Si films.

To prepare the SOI samples with the required range of different Si thicknesses, the SOI wafers with a starting Si film thickness of 66 nm were subjected to an oxidation/oxide strip process. This oxidation/stripping process works by consuming the top-most Si to form SiO_2, which is then stripped away, effectively thinning down the Si layer. The SOI wafers were thinned by a combination of dry thermal oxidation and ozone cleaning in order to remove controlled amounts of Si uniformly from the surface of the SOI layer. The oxidation was performed in a Thermco 9000 series horizontal furnace at 1000 °C. The ozone cleaning was done with the help of a Semitool Spray Acid Tool (SAT) using ozone gas, hydrofluoric acid (HF) acid, and ammonium hydroxide to clean the wafer before oxidation. Each cycle resulted in the removal of around 10 Å. The Si thickness was measured after each step using a Nanospec 3000 noncontact spectral reflectometry tool by means of refractive index. The wafers were then laser-diced into 10 mm by 10 mm chips. We performed atomic force microscopy (AFM) analysis of the surfaces of the different Si thicknesses used in this study. Multiple sites were measured per sample to generate a reliable average. Considering the full sample set, the surface roughness varied between 0.165 and 0.259 nm with no obvious trend as a function of Si thickness. The Si films are continuous in all cases. Overall, the surface roughness does not appear to vary significantly as the Si thickness on the SOI samples is scaled.

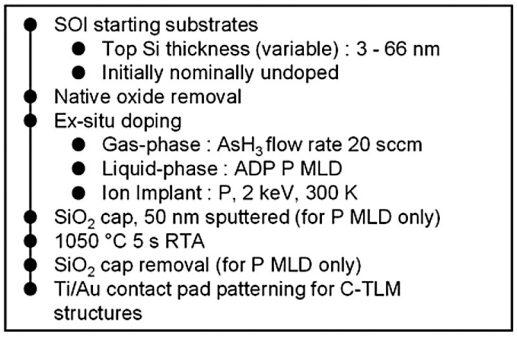

FIG. 1. The process flow for the fabrication, doping, and metal contacting of the different Si film thicknesses used for this work.

Dopant impurities were then introduced to the samples via one of the three following methods; liquid/vapor-source monolayer doping (MLD) of phosphorus,[15] gas-source in-diffusion of arsenic,[17] or beam-line ion implantation of phosphorus.

MLD of phosphorus:[15] All chemicals purchased from Sigma-Aldrich were of reagent grade and used as received. The SOI samples were initially sonicated in Milli-Q deionized water for 10 min and dried under a stream of nitrogen gas to remove any debris from the laser dicing process. The samples were then sonicated in acetone (≥99.8%), dipped in isopropyl alcohol (IPA) (99.9%), and then dried using nitrogen gas. A 10 s, 2% hydrofluoric acid dip was used to remove native oxide and to provide a H-terminated surface suitable for the ensuing hydrosilylation reaction. After H-termination, samples were quickly placed into a reaction flask under nitrogen on a Schlenk line. A 0.1M solution of allyldiphenylphosphine (ADP) (95%) in mesitylene (98%) was then degassed and transferred to the reaction flask. The reaction flask was heated to 180 °C for 3 h to allow for monolayer formation. Samples were then removed from the reaction flask and sonicated in IPA for 1 min before being dried in a stream of nitrogen to remove any physisorbed molecules.

Gas-source in-diffusion of arsenic:[17] Gas-phase doping of the SOI samples was carried out using a conventional metalorganic vapor phase epitaxy (MOVPE) rf-induction heated, horizontal reactor system, at a pressure of 700 Torr, with carrier gas Pd-diffuser purified hydrogen at a flow rate of 16 standard liters per minute (SLM). AsH_3 gas was used as the n-dopant source and was of the highest purity available commercially. The samples were heated on a graphite susceptor under hydrogen gas from 20 °C to 600 °C over a period of 260 s. At this temperature, AsH_3 dopant gas was supplied into the reactor at a controlled flow rate of 20 sccm (or 8.9×10^{-4} mole/min) and sample heating continued over a further 540 s to a process temperature of 850 °C. These conditions were then held for 120 s after which time the heating was switched off and samples allowed to cool under hydrogen and AsH_3. At a sample temperature of 600 °C (after 300 s), the AsH_3 dopant gas was switched out of the reactor and the samples were allowed to cool to room temperature under hydrogen.

Ion implantation of phosphorus: As a benchmark, some devices received a P 1×10^{15} cm^{-2} 2 keV 7° beam-line ion implant, performed at room temperature.

For each doping method, all samples were processed with a rapid thermal anneal (RTA) at 1050 °C for 5 s in N_2 after the introduction of the impurity atoms. For the phosphorus liquid/vapor MLD-doped samples, a protective SiO_2 cap was deposited after the reaction. This SiO_2 cap was used to prevent the dopant-containing molecules from evaporating from the surface. This protective cap was removed after the annealing process.[15]

In order to evaluate dopant incorporation, a nominally undoped bulk Si sample was included alongside the SOI samples for each doping method. These bulk samples were used to determine the active doping concentration vs Si depth using electrochemical capacitance voltage (ECV) measurements. The ECV measurements were performed using a WEP CVP21 wafer profiler

with an area size of 1.13 mm^2. ECV profilers extract an error with every data point in the curve. For the data presented here, the errors do not exceed 20%. As doping concentration axes are plotted in a log-scale, these errors are relatively small and do not affect the overall conclusions of this work.

To perform the electrical characterization of the doped Si films, the circular transfer length method (C-TLM) was used.[18] This method is used to measure the resistance between electrodes placed on a material at different distances apart in order to account for contact resistance by extrapolation. Optical lithography, metal evaporation, and lift-off were used to define repeated sets of 10 concentric circular electrode pairs consisting of 90 nm Au on top of a 10 nm Ti adhesion layer. These electrode pairs had a fixed internal electrode radius of 25 μm, as shown in Fig. 2(b). The inter-electrode separation ranged from 130 μm for the widest pair down to 3 μm for the narrowest pair. Electrode diameter and separation were verified by scanning electron microscopy (SEM) using a JEOL JSF 7500. Unlike its linear counterpart (TLM), the circular transfer length method has the advantage of requiring lithography for metal deposition only, without the need for extra geometrical etching of the material under test,[18] and also does not suffer from the same current crowding and current spreading issues.[19]

Electrical measurements were performed using an Agilent B1500 parameter analyzer, in a Cascade manual probe system under ambient conditions. The outer (shared) electrode was set to 0 V, and the bias voltage was applied to each inner electrode. The voltage was swept from −1 V to +1 V in 40 mV increments, with 127 points of integration used for each current reading. For each Si thickness, 4–6 sets of 10 C-TLM electrodes were measured to assess the resistivity of the material. The resistance of each concentric electrode pair was determined by taking an average of all of the single point resistances for each measurement point within a single current/voltage sweep,

$$R = \frac{1}{n}\sum_{x=1}^{n}\frac{V_x}{I_x}. \tag{1}$$

Resistance was then plotted against electrode separation as shown in Fig. 2. In order to account correctly for the contact resistance of the system, the resistance data from the C-TLM electrodes were fit to an equivalent linear TLM model.[18] This linear correction was performed by dividing the measured resistance values by a correction factor c, calculated as follows: [18]

$$c = \frac{r_1}{s} \times \ln\left(1 + \frac{s}{r_1}\right). \tag{2}$$

Here, c is the correction factor, r_1 is the radius of the inner electrode, and s is the separation between the inner electrode and the outer electrode. From the corrected C-TLM resistance data, the electrodes' geometries, and the known Si film thickness, the material resistivity was determined.

Figure 2 is a representative plot of Si film resistance vs electrode separation generated by C-TLM measurement on a 66 nm thick Si film. The circles represent the measured resistance and the diamonds represent the "linearized" resistance data, which is

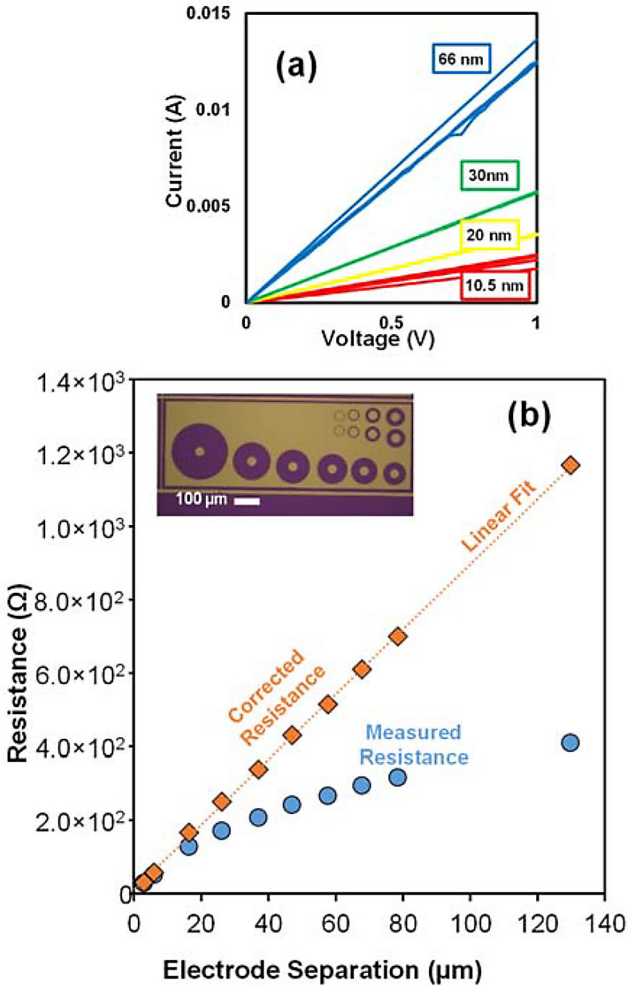

FIG. 2. (a) Representative I-V data for the different SOI thicknesses of the gas-doped samples. These data are all taken from the electrode pairs with 130 μm separation from each SOI thickness, respectively. (b) Resistance vs electrode separation for a 66 nm thick, liquid MLD P-doped Si film showing the measured resistance (blue circles) and the corrected resistance (orange diamonds). The dotted line is a linear fit to the corrected resistance, with an R^2 value of 0.9996. Inset: An optical image of a set of 10 C-TLM electrodes. The shared outer electrode was set at 0 V, while the bias was applied to the center electrodes, respectively, for each measurement.

transformed to account for the circular geometry of the C-TLM electrode structures.[18] The characteristic resistivity ρ for each C-TLM data set is determined by the following relationship:

$$\rho = \frac{dR}{ds} \times 2\pi r_1 \times d, \tag{3}$$

where ρ is the resistivity, $\frac{dR}{ds}$ is the slope of the corrected resistance R vs electrode separation s, r_1 is the radius of the inner electrode ($2\pi r_1$ is the "contact area"), and d is the thickness of the Si film.

The thickness of each Si film was verified by Cross-sectional Transmission Electron Microscopy (XTEM) or by scanning electron microscopy using a JEOL JSF 7500. XTEM was carried out using the JEOL 2100 high-resolution TEM (HRTEM) operated at 200 kV. Cross-section samples were prepared by focused ion beam etching using a FEI's Dual Beam Helios Nanolab system.

μ4PP measurements were performed with vibration tolerant microelectrodes[20] using the CAPRES MicroRSP-M200. The Si microelectrodes were Ni coated, and the nominal contact force of each cantilever electrode was approximately 5 μN. The measurements were performed with lock-in technique using 13 Hz and a measurement current in the range 2–50 μA. Dual configuration sheet resistance R_S was calculated using van der Pauw-like geometry correction.[21,22] Five sheet resistance measurements were performed on each sample, and the resistivity was calculated as the product of the mean sheet resistance and the Si thickness, $\rho = R_S \times d$. Our motivation to use both μ4PP and C-TLM electrical test was to double-check our electrical data, using 2 separate characterization techniques.

Electronic structure calculations were performed within the framework of density functional theory (DFT) as implemented in the Atomistix ToolKit.[23] The local-density approximation (LDA) for the exchange-correlation (XC) potential[24] and norm conserving pseudopotentials were used. Numerical atomic orbital basis set s3p3d1 was used for Si, and for the hydrogen terminations, s2p2 basis set was considered.[25–27] All structural relaxation was performed with the maximum force of less than 0.02 eV Å^{-1}. The energy cutoff was set to 180 Ry.

III. RESULTS AND DISCUSSION

A. Electrical analysis

The goal of this work was to investigate the relationship between decreasing film thickness and increased resistivity for Si films in the range of 66 nm down to 3 nm. For the ultrathin films (3 nm, 4.5 nm, and 10.5 nm), TEM imaging was necessary to gauge the film thickness accurately. Figure 3 shows representative cross-section TEM images of the three thinnest Si films that were used.

For each doping technique, the active concentration of dopant atoms was assessed using ECV measurements. Figure 4 shows the active dopant concentration vs Si depth for liquid and vapor MLD, gas-doped, and ion implant-doped Si. For these data, a bulk Si sample was included with the SOI samples during each respective doping step. Note that the active concentration achieved here could be improved upon by using a faster ramp rate RTA tool. In this case, the RTA tool has relatively slow ramp rates resulting in high thermal budget and thus too much diffusion. With faster ramp rate annealing tools, diffusion can be controlled such that the maximum active concentration is higher close to the surface. Work is ongoing in this regard and will be reported on in the future.

Furthermore, in Fig. 4, we observe that the ion implant process produces the most incorporated dopant, as the dose is proportional to the integrated area under the curve of the doping profile. The AsH_3 process achieves a high surface concentration, around 10^{20} cm^{-3} which appears promising. The MLD profiles peak at approximately 2×10^{19} cm^{-3} and innovative work is currently ongoing to increase that value. From the data in Fig. 4, we

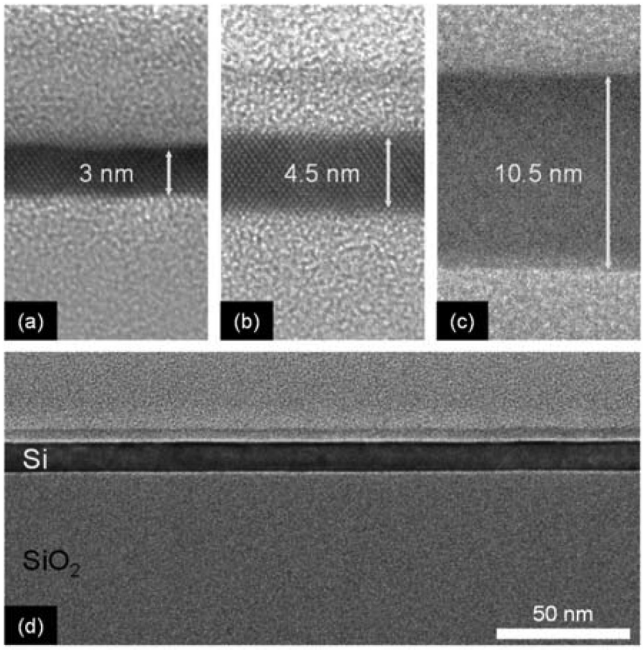

FIG. 3. (a)–(c) Representative TEM images of Si (SOI) films thinned down to different thicknesses via oxidation/oxide stripping. (d) shows a wider view of the 10.5 nm Si film.

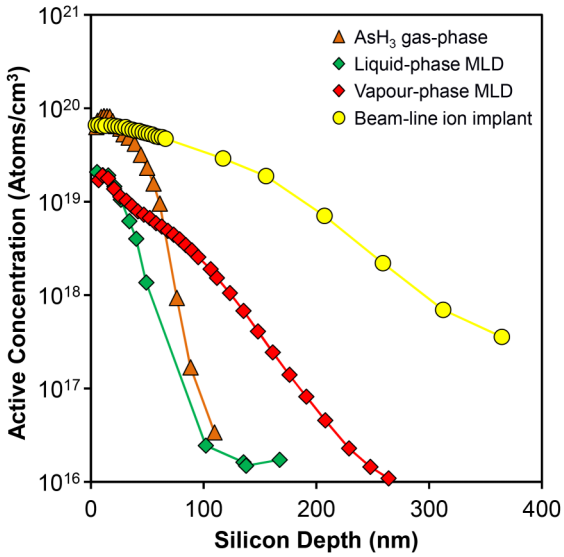

FIG. 4. ECV data showing the active dopant concentration profile vs depth for the bulk Si sample included with each doping run. The figure shows doping concentration for the gas-source (AsH_3) arsenic doping, the liquid-phase MLD phosphorus doping, vapor-phase MLD phosphorus doping, and beam-line ion implant doping processes.

would expect the best electrical conductivity in thin films doped by the ion implant or AsH_3 process.

Figure 5 shows the resistivity for Si films for the four doping processes. Theoretical active concentration contour lines have been added Fig. 5 to indicate the effective level of dopant activation. For the in-diffusion based doping processes, ρ starts to degrade already at 20 nm thicknesses. At 4.5 nm, the data points are off the y-axis scale but are in the $10^{11}\,\Omega$ nm range. The best doping process here was the ion implantation which started to see degradation in conductivity, by 2 orders of magnitude, at a Si thickness of 4.5 nm.

Figure 6 contains the raw data from which the ρ values were extracted and are included here to give extra understanding into the experimental trends. In the figure, representative resistance vs electrode separation is plotted for 5 thicknesses of SOI, for the vapor MLD-doped SOI samples, and for the beam-line ion implanted SOI. The SOI films with thicknesses of 66 nm, 30 nm, and 20 nm had current/voltage characteristics that showed the expected linear relationship over the range of ±1 V. A representative set of I-V characteristics for the arsenic-doped (AsH_3) SOI was seen back in Fig. 2(a). These thickest 4 out of the 7 tested Si thicknesses conducted electrical current consistently in all cases, from which a meaningful resistivity value could ultimately be extracted, i.e., the measured resistance scaled appropriately with electrode separation distance. The I-V measurements for the 3 nm and 4.5 nm thick Si films were either more resistive than allowed measureable current at the applied voltage ($<\pm 5\times10^{-13}$ A at ±1 V), or the measured resistance did not scale reliably with electrode spacing, according to the C-TLM model. In fact, the current conduction in the 3 nm films was so poor that the data could not be reasonably included in Fig. 5. Moreover, the plots in Fig. 6

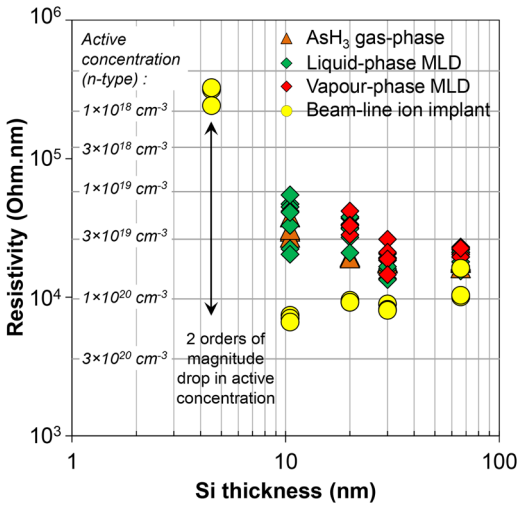

FIG. 5. Resistivity vs SOI thickness for the gas-phase (AsH_3) arsenic, vapor-phase MLD phosphorus, liquid-phase MLD phosphorus, and beam-line ion implant doping processes. The resistivity appears to increase at and below an SOI thickness of 20 nm and significantly at and below 10.5 nm for the nonimplant doping processes. No meaningful current was measureable for SOI thicknesses of film with Si thickness = 3 nm (not shown).

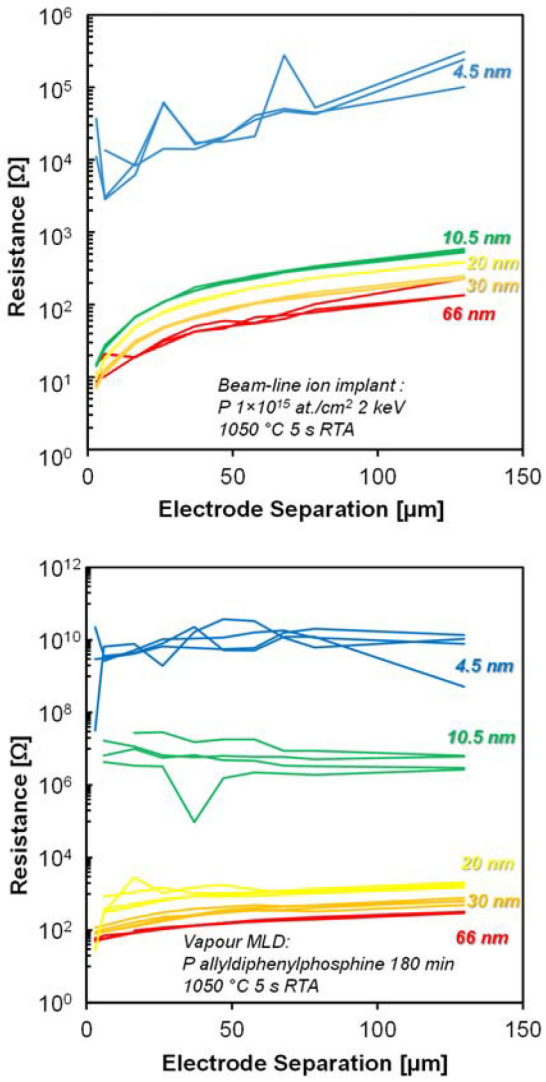

FIG. 6. Resistance plotted vs electrode separation for 5 thicknesses of SOI. Data were measured from the vapor MLD-doped SOI samples (bottom) and data from the beam-line ion implanted SOI (top).

emphasize how rapidly and dramatically resistance degrades with Si thickness for the nonion implanted cases. The ion implant example shows a tight distribution of curves for most Si thicknesses, it is only at 4.5 nm we see an obvious deviation, and then it is a 2 orders of magnitude degradation. For the MLD data, resistance shoots up rapidly, already 4 orders of magnitude at 10.5 nm, and by 8 orders of magnitude at 4.5 nm, which clearly is a problem for fabricating devices at these dimensions. From these data in Figs. 5 and 6, one can conclude that ion implant is currently the best choice for *ex situ* doping of thin Si films.

The increased resistivity for the ultrathin Si films could be attributed to a number of factors including increased surface

scattering effects due to the higher surface-to-volume ratio that naturally presents itself at the few-atom thickness scale, as well as potentially poor dopant incorporation and poor dopant activation. Atomic scale thickness variation has also been demonstrated to influence carrier mobility in ultrathin-body metal-oxide-semiconductor field efffect transistors (MOSFETs).[28] The comprehensive work of Granzner *et al.*, which reviews and compares the available empircal data,[29] suggests that nanowires with dimensions in the few-nanometer scale exhibit reduced effective electron mobility. However, the study shows that experimentally, this mobility reduction has been found to "kick in" at higher critical dimensions than theoretically predicted by the effects of phonon scattering and surface roughness. The implication here is that a number of different factors may be at play which contribute to the overall increased effective resistivity of the material.

There is a strong agreement between the electrical data captured by C-TLM and the μ4PP method. For two doping methods, namely, phosphorus MLD and AsH_3 gas doping, identical sample sets were processed, one of which was analyzed by μ4PP while the other received the usual C-TLM processing and characterization. Figure 7 shows resistivity data from the two extraction methods. For both doping processes, the comparison is good as the trends are well-reproduced. In effect, the μ4PP characterization validated the C-TLM approach.

Interestingly, we can also see in Fig. 7, with a smaller range on the y-axis than before, that the resistivity increases in the MLD case for the 66 nm Si thickness. This is related to the lower dose of dopant incorporation with this process, compared to the AsH_3 process, seen previously back in Fig. 4. This lower dose means that process cannot fully dope the thicker film effectively and hence the resistivity increases. The resistivity increase at smaller dimensions was as seen and discussed before in relation to Fig. 5.

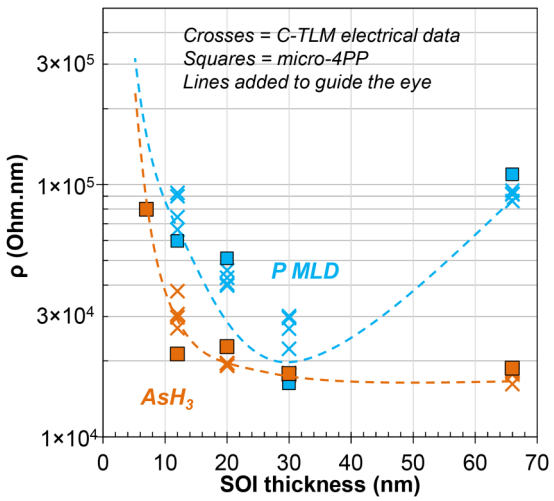

FIG. 7. Resistivity vs SOI thickness for the liquid MLD phosphorus and gas-phase (AsH_3) arsenic doping processes. In this sample subset, the aim was to benchmark ρ extracted by C-TLM measurements with that from μ4PP. For the 2 different doping processes, the comparison is good as the trends are well-reproduced. The conclusions from both sets of data are the same.

B. Implications for gate-all-around devices

The increased effective material resistivity that was observed for the ultrathin SOI films has concerning implications for device performance in future technology nodes. In the best case scenario from our available data, the resistivity of the 4.5 nm film was 2 orders of magnitude higher than the resistivity at 10.5 nm and above. As the dimensions shrink to the sub-10 nm regime for nanowire and fin-type devices, this increased resistivity will need to be accounted for if sufficient drive currents are to be maintained at a given supply voltage. This modification can be done by increasing device cross-sectional area (in the case of source/drain regions of nanowire devices), by increasing channel width (to decrease channel resistance), or by having multiple fin/nanowires in parallel. Obviously, none of these scenarios are desirable for the down-scaling of device size and area footprint.

The implication of increasing resistivity with scaled Si thickness is now discussed with respect to device technology incorporating gate-all-around nanowires and epi raised source/drains. It should be stated up front that the dimensions in the following calculations are indicative and representative of a modern or future device technology. These numbers will change from technology to technology depending on the application (e.g., high performance or low power logic devices) and will also depend on the specific targets and metrics of different chip makers in this space.

Assuming current flows in parallel paths through parallel nanowires, the total parasitic resistance (R_{TOTAL}) associated with the current through Si consists of that from the raised source and drain epi ($R_{SOURCE\ epi}$, $R_{DRAIN\ epi}$) plus that from the parallel resistances in the nanowires. This is shown schematically in Fig. 8(a). So,

$$R_{TOTAL} = R_{SOURCE\ epi} + (R_{NANOWIRE\ (1)} \parallel R_{NANOWIRE\ (2)} \parallel \cdots \parallel R_{NANOWIRE\ (n)}) + R_{DRAIN\ epi}, \tag{4}$$

assuming there are n nanowires in parallel, and $R_{NANOWIRE}$ is the resistance of an individual nanowire and $R_{NANOWIRES}$ is the lumped resistance of all the nanowires together. Resolving the resistance from just the nanowires, we can use the formula

$$\frac{1}{R_{NANOWIRES}} = \frac{1}{R_{NANOWIRE\ (1)}} + \frac{1}{R_{NANOWIRE\ (2)}} + \cdots + \frac{1}{R_{NANOWIRE\ (n)}}. \tag{5}$$

Assuming all parallel nanowires are equal simplifies the equation

$$\frac{1}{R_{NANOWIRES}} = \frac{n}{R_{NANOWIRE}} \tag{6}$$

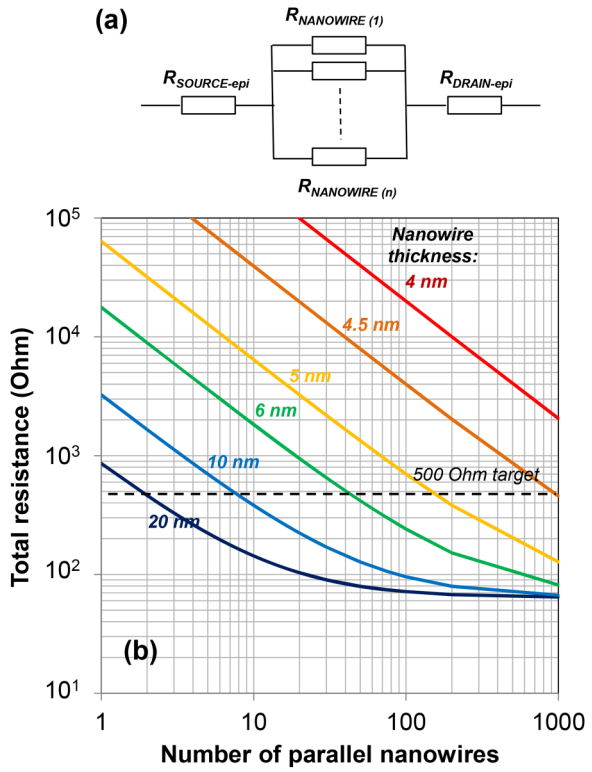

FIG. 8. Total parasitic resistance associated with current flow in Si through raised source drain epi, and parallel current path nanowires using the ρ values from the ion implanted samples. Total resistance is reduced by adding more nanowires in parallel. Reduced Si thickness around 5 nm greatly increases total resistance and thus requires more parallel nanowires to achieve a total resistance target.

and so

$$R_{NANOWIRES} = \frac{R_{NANOWIRE}}{n}. \tag{7}$$

Equation (4) then simplifies down to

$$R_{TOTAL} = 2R_{SOURCE/DRAIN\ epi} + \frac{R_{NANOWIRE}}{n}. \tag{8}$$

This formula is implemented in Fig. 8(b) assuming the following well-known relationship between Si resistivity (ρ) and resistance (R):

$$R = \rho\frac{L}{A}, \tag{9}$$

where L is the length in the direction of current flow and A is the cross-sectional area perpendicular to the current flow. For this representative discussion, we assume $L = 100$ nm on each side for the raised source drain epi and a radius of 100 nm. In order to simplify the discussion, we assume that the epi produces an approximately circular cross section perpendicular to the direction of current flow. For the nanowires, L is assumed to be 25 nm, which is representative of gate length in a modern technology, and radius of the nanowire is a variable. The nanowires are assumed to have a circular cross section perpendicular to the direction of current flow and the current is assumed to flow throughout the nanowires. Of course, this is a simplification as the cross-sectional area (A) will be different depending on whether the current is in an inversion-mode or accumulation mode. Here, we use the best experimental conductivity results, the ion implanted values of ρ vs Si thickness according to Fig. 5, using a fitted trend line to the data.

From Fig. 8(b), we can see that total resistance is reduced by adding more nanowires in parallel. Reducing Si thickness to around 5 nm greatly increases total resistance and thus requires more parallel nanowires to achieve a total resistance target. For the sake of discussion, we have a 500 Ω target, based on flowing 2 mA at a 1 V supply voltage. In that case, $R_{TOTAL} = 500\ \Omega$ is achieved for 20, 10, 6, 5, and 4.5 nm diameter nanowire devices consisting of 2, 7, 40, 130, and 800 nanowires in parallel. Having >100 parallel nanowires is a huge technological challenge and is unlikely to be a practical solution. This analysis suggests the solution may not lie in increasing the number of parallel conduction paths. Pioneering solutions for reducing resistivity in scaled Si structures may exist in the fields of proximity doping, where charge is induced from materials on the surface without embedding an impurity dopant atom in the Si crystal itself, and in novel Si surface passivation techniques, and thus increased efforts in these areas are needed for better conduction in 5 nm thick Si.

C. Modeling for physical understanding

To understand the behavior of a dopant in ultrathin Si films, the electronic structure of an ~4.5 nm thin film along [100] crystallographic orientation is studied using *ab initio* calculations by altering the location of dopants in three different scenarios. In the first scenario, a Si atom is substitutionally replaced by a phosphorus atom on the surface with the dangling bonds. In the second scenario, a Si atom is substitutionally replaced by a phosphorus atom on the core of the film. In the last scenario, a Si atom is substitutionally replaced by a phosphorus atom "close to" the surface and is surrounded only by Si atoms. In this set of simulations, the size of the supercells is large enough to supress the phosphorus donor electron from its periodic image, although it does not isolate the donor electron. Dangling bonds on the surface of the films are saturated by hydrogen atoms for obtaining the stable minimum energy. There is one single dopant in the supercell with ~400 Si atoms which corresponds to $\sim 1.3 \times 10^{20}\ cm^{-3}$ doping concentration. Common XC functionals used in the DFT calculations typically underestimate the bandgap energies. To improve the electronic structure description for the relaxed DFT/LDA geometries, a more accurate estimate of the bandgap energies is made using a metageneralized gradient approximation (meta-GGA) XC functional. If properly calibrated, meta-GGA has been demonstrated to provide bandgap energies comparable to experimental values for many semiconductors as demonstrated in the original formulation of the method.[30] Meta-GGA also provides an improved description for the bulk and 2D electronic structure.[31]

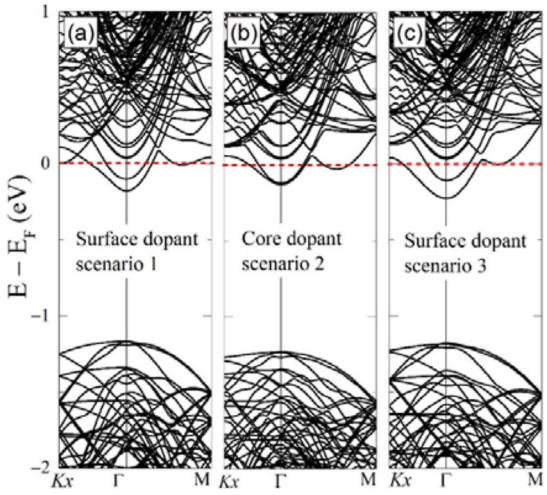

FIG. 9. Band structure of Si thin films along [100] orientation and with a thickness of 4.5 nm doped with phosphorus for (a) surface dopant bonded to H, (b) core dopant, and (c) surface dopant bonded to 4 neighbor Si atoms. Energies are referenced to the Fermi level (red dashed line).

Band structures of phosphorus doped Si thin films as a function of location are presented in Fig. 9 where energies are referenced to the Fermi level. As can be seen from the band structures, the dopant bands are not flat for this doping concentration which could imply that the donor electron is not isolated. It is worth mentioning that Si thin films with thickness below 4.5 nm are turned into direct bandgap. From system energy calculations, the film with surface dopant, i.e., scenario 1, is energetically more favorable. This is followed by surface dopant of scenario 3 and finally by the core dopant (scenario 2). These results suggest that the surface of the Si film with a thickness of 4.5 nm is energetically more favorable for the phosphorus dopant atom compared to the core of the film.

The implication of these results is that surfaces and interfaces interfere with effective doping in Si thin films and devices. As we scale dimensions, there is a greater device structure surface to volume ratio, and so the greater the influence of the surface and interface effects on dopant behavior, and ultimately the ability to *ex situ* dope these materials.

IV. CONCLUSIONS

In this work, we investigated the changing conductivity of ultrathin SOI films as the Si thickness was scaled from 66 nm down to 3 nm. Dopant impurities were introduced to the SOI samples by different doping techniques, namely, MLD of phosphorus, gas-source (Arsine) deposition of arsenic, and beam-line ion implantation of phosphorus. Material resistivity was observed to increase as the Si thickness was scaled below 20 nm, increasing significantly at 10.5 nm. At and below a Si film thickness of 4.5 nm, we observed a loss of consistently measureable resistance and an absence of the consistent scaling of resistance vs electrode separation predicted by the theory of the C-TLM. While it is evident that the material resistivity of SOI films increases with reduced film thickness, the lack of information on the true doping concentration profile for the first few nanometers prevents us from assigning the precise cause to one phenomenon or another. The effective resistivity used in this work is derived from the measured resistance and sample geometry, whereas in reality the actual material resistivity may not necessarily be constant with depth into the SOI film. As such, it is unclear as to whether the observed resistivity change is due to geometrical/quantum phenomena or is in fact due to the challenges associated with creating an optimal doping profile vs depth. Future characterization of the near-surface doping profile would provide a clearer indication of the true cause of the increased material resistivity. Ultimately, the results presented here shed light on some of the future roadblocks that must be overcome to push beyond the current limits of ultrathin SOI as a technology.

The overall implication of this study is that achieving conductivity in 5 nm Si films is not trivial. This may be due to a number of physical effects related to the reduced Si dimensions, but this also highlights the problems associated with *ex situ* doping of thin Si films. In-diffusion techniques suffer more as there is a surface barrier to overcome in order to enter Si, while ions can always be implanted beyond the surface into the target. Pioneering solutions may exist in the fields of proximity doping and novel surface passivation techniques, and thus increased efforts in these areas are needed for better conduction in 5 nm thick Si.

ACKNOWLEDGMENTS

This work is supported by Enterprise Ireland through Project No. IP-2017-0605, by the European Union's Horizon 2020 Research and Innovation programme via the ASCENT Access Network (Grant Agreement No. 654384), and through the European Regional Development Fund (ERDF) under Ireland's European Structural and Investment Funds Programmes 2014–2020. L. Ansari and F. Gity would like to acknowledge the SFI/HEA Irish Centre for High-End Computing (ICHEC) for the provision of computational facilities and support.

REFERENCES

[1]C. C. Sun, R. R. Liang, L. B. Liu, J. Wang, and J. Xu, Appl. Phys. Lett. **107**(13), 132105 (2015).
[2]V. Djara, L. Czornomaz, V. Deshpande, N. Daix, E. Uccelli, D. Caimi, M. Sousa, and J. Fompeyrine, Solid State Electron. **115**, 103 (2016).
[3]H. Liu and P. D. D. Ye, IEEE Electron Device Lett. **33**(4), 546 (2012).
[4]M. J. H. Van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, and R. J. P. Lander, in *Digest of Technical Papers—Symposium on VLSI Technology* (IEEE, 2007), p. 110.
[5]A. Veloso, G. Hellings, M. J. Cho, E. Simoen, K. Devriendt, V. Paraschiv, E. Vecchio, Z. Tao, J. J. Versluijs, L. Souriau, H. Dekkers, S. Brus, J. Geypen, P. Lagrain, H. Bender, G. Eneman, P. Matagne, A. De Keersgieter, W. Fang, N. Collaert, and A. Thean, paper presented at the 2015 Symposium on VLSI Technology (VLSI Technology), 2015.
[6]J. P. Colinge, Solid State Electron. **48**(6), 897 (2004).
[7]H. K. Lim and J. G. Fossum, IEEE Trans. Electron Devices **30**(10), 1244 (1983).
[8]See http://www.itrs2.net/ for semiconductor technology trends and projections.

[9]M. Diarra, Y. M. Niquet, C. Delerue, and G. Allan, Phys. Rev. B **75**(4), 045301 (2007).
[10]M. T. Bjork, H. Schmid, J. Knoch, H. Riel, and W. Riess, Nat. Nanotechnol. **4**(2), 103 (2009).
[11]T. L. Chan, M. L. Tiago, E. Kaxiras, and J. R. Chelikowsky, Nano Lett. **8**(2), 596 (2008).
[12]M. V. Fernández-Serra, C. Adessi, and X. Blase, Phys. Rev. Lett. **96**(16), 166805 (2006).
[13]L. Lin, Z. Li, J. Feng, and Z. Zhang, Phys. Chem. Chem. Phys. **15**(16), 6063 (2013).
[14]R. W. Hamm and M. E. Hamm, *Industrial Accelerators and Their Applications* (World Scientific Publishing Co., 2012), p. 1.
[15]N. Kennedy, R. Duffy, L. Eaton, D. O'Connell, S. Monaghan, S. Garvey, J. Connolly, C. Hatem, J. D. Holmes, and B. Long, Beilstein J. Nanotechnol. **9**, 2106 (2018).
[16]R. Duffy, A. Ricchio, R. Murphy, G. Maxwell, R. Murphy, G. Piaszenski, N. Petkov, A. Hydes, D. O'Connell, C. Lyons, N. Kennedy, B. Sheehan, M. Schmidt, F. Crupi, J. D. Holmes, P. K. Hurley, J. Connolly, C. Hatem, and B. Long, J. Appl. Phys. **123**(12), 125701 (2018).
[17]R. Duffy, K. Thomas, E. Galluccio, G. Mirabelli, M. Sultan, N. Kennedy, N. Petkov, G. Maxwell, A. Hydes, D. O'Connell, C. Lyons, B. Sheehan, M. Schmidt, J. D. Holmes, P. K. Hurley, E. Pelucchi, J. Connolly, C. Hatem, and B. Long, J. Appl. Phys. **124**(4), 045703 (2018).
[18]J. H. Klootwijk and C. E. Timmering, in *Merits and Limitations of Circular TLM Structures for Contact Resistance Determination for Novel III-V HBTs* (IEEE International Conference on Microelectronic Test Structures, 2004), p. 247.
[19]G. K. Reeves and H. B. Harrison, IEEE Electron Device Lett. **3**(5), 111 (1982).
[20]K. G. Kalhauge, H. H. Henrichsen, F. Wang, O. Hansen, and D. H. Petersen, J. Micromech. Microeng. **28**(9), 095010 (2018).
[21]R. Rymaszewski, J. Phys. E **2**(2), 170 (1969).
[22]S. Thorsteinsson, F. Wang, D. H. Petersen, T. M. Hansen, D. Kjær, R. Lin, J.-Y. Kim, P. F. Nielsen, and O. Hansen, Rev. Sci. Instrum. **80**(5), 053902 (2009).
[23]See https://www.synopsys.com/silicon/quantumatk.html for details.
[24]J. P. Perdew and A. Zunger, Phys. Rev. B **23**(10), 5048 (1981).
[25]T. Ozaki and H. Kino, Phys. Rev. B Condens. Matter Mater. Phys. **69**(19), 195113 (2004).
[26]D. Sharma, L. Ansari, B. Feldman, M. Iakovidis, J. C. Greer, and G. Fagas, J. Appl. Phys. **113**(20), 203708 (2013).
[27]L. Ansari, B. Feldman, G. Fagas, C. M. Lacambra, M. G. Haverty, K. J. Kuhn, S. Shankar, and J. C. Greer, IEEE Trans. Nanotechnol. **12**(6), 1075 (2013).
[28]K. Uchida, H. Watanabe, J. Koga, A. Kinoshita, and S. Takagi, in *Experimental Study on Carrier Transport Mechanism in Ultrathin-Body SOI MOSFETs* (IEEE, 2003), p. 8.
[29]R. Granzner, V. M. Polyakov, C. Schippel, and F. Schwierz, IEEE Trans. Electron Devices **61**(11), 3601 (2014).
[30]F. Tran and P. Blaha, Phys. Rev. Lett. **102**(22), 226401 (2009).
[31]J. C. Greer, A. Blom, and L. Ansari, J. Phys. Condens. Matter **30**(41), 414003 (2018).