

# Design and Improvement a High Speed and Low Power 8/9 Frequency Divider with TSPC Dynamic Logic

\*ALI RAHNEMAEI

\*\*FARNOOD KHOSHNEVIS

\*ALIREZA MOHAMMADNIA

\*ADEL AKBARIMAJD

\* Azad university of Ardebil, Germe Unit, P.O.BOX: 56146-467, Ardebil, IRAN

\*\* Southern unit of Azad university of Tehran, Tehran, IRAN

*Abstract* - A low power and high speed 8/9 CMOS programmable dynamic frequency divider has been designed. It contains a control bit by which can obtain 1/9 and 1/8 input frequency in output. In spite of the variations in size and structure of circuit, the 53% improvement in power dissipation has been achieved. Power dissipation about 1.6 mw in a 2.78 GHz Frequency Rate, 2.5 volt power supply circuit is verified by HSPICE simulation.

*Keywords*- Dynamic logic, Frequency divider, Frequency synthesizer, TSPC technique, LAN

## 1. Introduction

Frequency synthesizer is one of the most important blocks in communication receivers and transmitters [1-2]. A frequency synthesizer must be very accurate, low cost, low silicon area and low power dissipation. Figure 1 shows a structure of frequency synthesizer that includes PFD (phase-Frequency detector), CP (charge pump), LP (loop filter), VCO (Voltage Controlled Oscillator) and frequency divider. In the most of the frequency synthesizers a PLL is employed. Adoption of dynamic dividers in PLL allows reducing the considerable power consumption in forGiga Hertz applications [3-5]. In such circuits the dynamic latches are used because they are high speed and more compact in comparrison with static latches. TSPC (true single phase clock) technique can be utilized for avoiding the SKEW problem. In TSPC only one clock is employed for dynamic latch drivers [6]. In the rest of this paper we will employ a TSPC mechanism to design and improvement a high speed and low power ÷8/9 CMOS.

## 2. A 8/9 frequency divider structure

Figure 2 shows the general structure of a 8/9 frequency divider which includes a 2/3 divider, two ÷2 dividers and a 4-input OR gate. One of the inputs of OR gate is

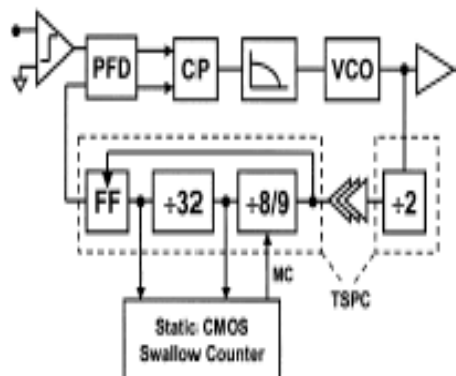


Fig.1. Structure of frequency synthesizer

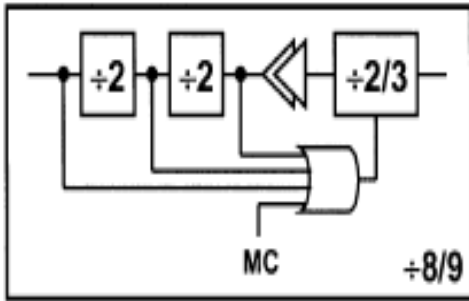


Fig.2. General structure of a 8/9 frequency divider

connected to output of  $\div 2/3$  block, two other inputs are connected to outputs of  $\div 2$  blocks. The forth pin MC is a control bit. When  $MC=0$  output of  $\div 2/3$  divider is one-third of input signal frequency and then the output of 8/9 frequency divider is one-ninth if input signal frequency. When  $MC=1$  the output of  $\div 2/3$  divider is half of signal frequency then the output of 8/9 frequency divider equal  $1/8$  input signal frequency.

It is better to employ asynchrony structure for frequency divider to obtain low power dissipation and reduce number of blocks that operate in high frequency [7-8].

### 3. Circuit Design

By comparison between dynamic structures

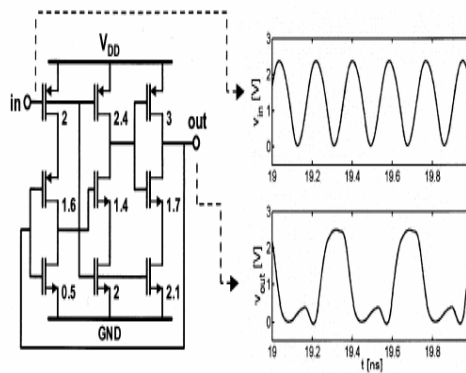


Fig.4. A 1/2 M-TSPC logic divider

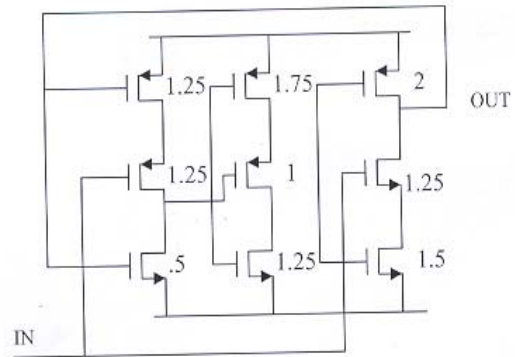


Fig.3. A 1/2 TSPC logic divider

and others structures such that SCL (source coupled transistor logic) one can yield into a result that dynamic structures have lower consumption power because of their compact organization and reduced number of transistors which result in low capacitive load [9]. For example a  $\div 2$  divider with SCL technique has 18 transistors which occupies more silicon area and makes its layout very difficult.

For designing  $\div 2$  frequency divider we can use two techniques: TSPC circuits in Figure 3 and M-TSPC (modified TSPC) in Figure 4. The speed of circuit may be increased by employed technique. For the comparison purposes we can use a 1/2 E-TSPC frequency divider instead of M-TSPC (see Figure 5).

Although accumulation of MOS transistors – which reduces the switching speed of circuit in high frequency applications – is avoided in this technique, but the power consumption

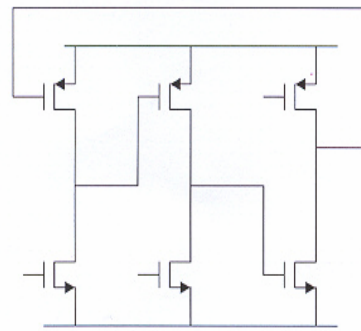


Fig.5. A 1/2 E-TSPC logic divider

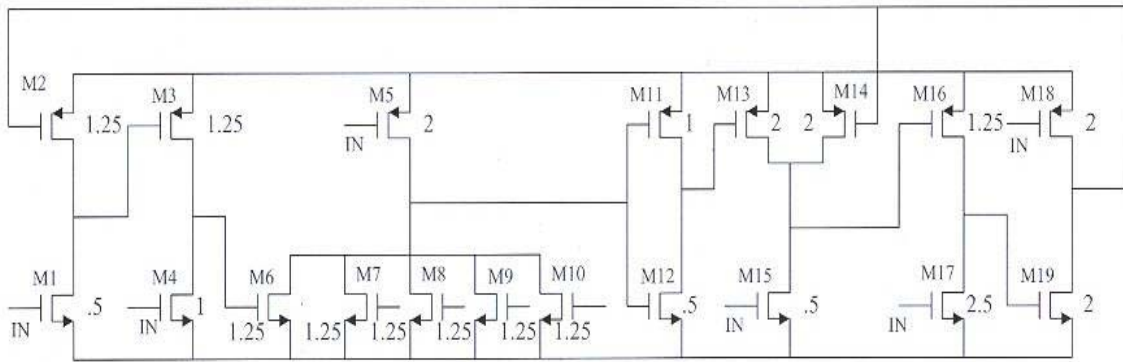


Fig.6. A 2/3 divider using E-TSPC technique

is higher than the circuits in Figure 3 and Figure 4. Both of TSPC and M-TSPC circuits suffer because of output node hazardous discharging problem [10]. For solution this problem we can insert a simple inverter in output of any TSPC and m-TSPC flip-flops and we can design a flip-flap with inversion output. As another solution we can insert a simple inverter in output of flip-flaps. Relating to importance of reducing the delay time of this stage, W/L inverter and buffer of the circuit must be optimized carefully.

Figure 6 shows the internal circuit of 2/3 blocks which uses E-TSPC technique for reducing the number of transistors to improve

switching performance and frequency operation.

The transistors M7, M8, M9, and M10 are inserted to 2/3 divider block to make the 4-input OR of circuit. MC control bit is connected to the gate of M7 and output of 2/3 block is fed back to the gate of M8; the gate of M9 is connected to first output of 1/2 block. Figure 7 shows total circuit of 8/9 frequency divider and sizing of all transistors.

When  $MC=0$ , the output frequency divider is one-ninth of input signal frequency and when  $MC=V_{CC}$ , the output frequency divider is one-eighth of input signal frequency divider.

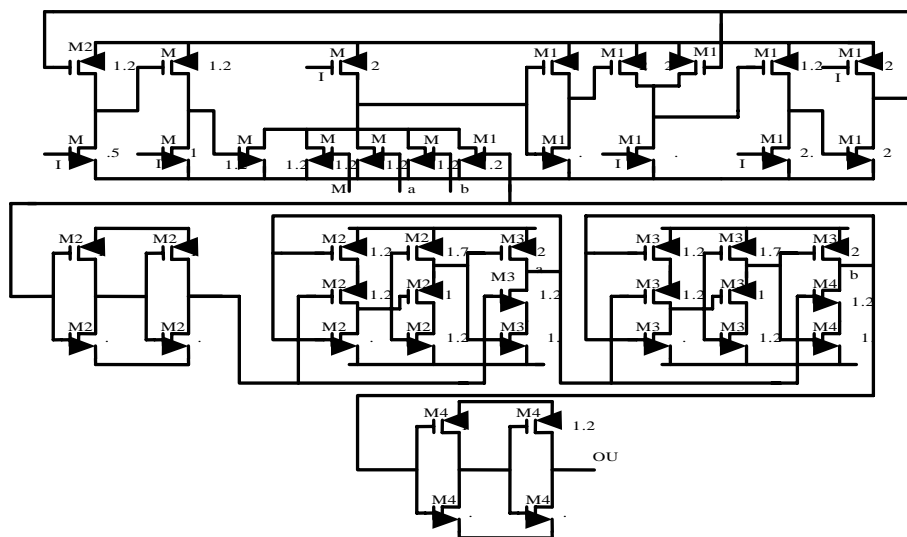


Fig.7. Total circuit of 8/9 frequency divider and sizing of transistors

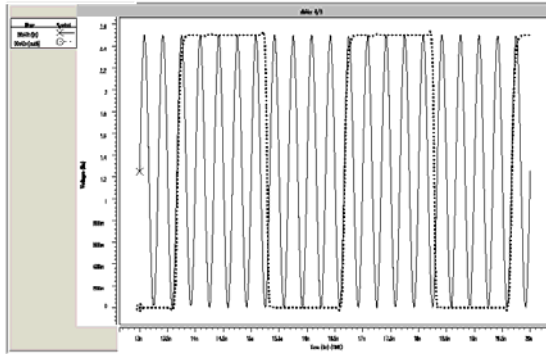


Fig.8. Input and output signals for frequency divider with TSPC technique

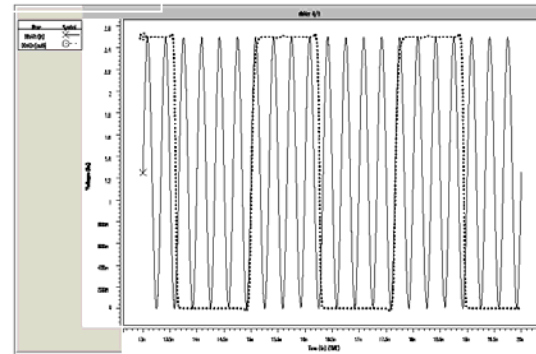


Fig.9. Input and output signals for frequency divider with E-TSPC technique

#### 4. Simulation results

The proposed circuit is simulated by HSPICE with  $0.25\mu\text{m}$  CMOS parameters. The results of simulation for frequency divider with TSPC technique (Figure2) and frequency divider with E-TSPC technique (Figure3) are shown in Figures 8 and 9 respectively. It is clear that the power dissipation of E-TSPC technique is  $374.937\mu\text{w}$  and for TSPC technique is  $129.297\mu\text{w}$  which is  $245.64\mu\text{w}$  greater than power dissipation of E-TSPC technique. So, insertion circuit of E-TSPC technique in main frequency synthesizer circuit causes decreasing the power dissipation.

When  $MC=0$  and output frequency is one-ninth of input signal frequency, by HSPICE simulation we can observe that the total power dissipation is  $1.6871\text{mw}$  and when  $MC=V_{CC}$  and output frequency in one-eightieth of input signal frequency, total power dissipation is  $1.7035\text{mw}$  (see Figures 8 and 9).

#### 5. Conclusions

In this paper a  $8/9$  frequency divider was designed in  $0.25\mu\text{m}$  CMOS which can be programmed with MC control bit. We used TSPC technique which needs only one clock to obtain a compact, high speed and low static power dissipation. By suitable selection of  $1/2$  frequency divider structure and suitable selection of WIL transistor sizes we could obtain  $1.7\text{mw}$  in power dissipation.

#### References

- [1] S. Pellerano, S. Levantino, "A  $13.5\text{-mw}$   $5\text{-GHz}$  Frequency Synthesizer With Dynamic-Logic Frequency Divider", IEEE, vol. 32, no.2, pp.378-383,2004.
- [2] S.Pellerano, S.Levantino, C.Samori,And .Lacaita, "A  $13.5\text{mW}$   $5\text{-GHz}$  Frequency Synthesizer With Dynamic-Logic Frequency Divider" IEEE J. Solid-State Circuits, vol. 39, pp. 378–383, Feb. 2004.
- [3] C. M. Hung and K. K. O, "A fully ntegrated  $1.5\text{-V}$   $5.5\text{-GHz}$  CMOS phase-locked loop," IEEE Jur. Solid-State Circuits, vol. 37, pp. 521–525, Apr. 2002.
- [4] B. U. H. Klepser, M. Scholz, and J. J. Kucera, "A  $5.7\text{-GHz}$  HiPerLAN SiGe BiCMOS voltage-controlled oscillator and phase-locked-loop frequency synthesizer," in Radio-Frequency Integrated Circuits Symp. Dig., Phoenix, AZ, May 2001, pp. 61–64.
- [5] H. R. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injected-locked frequency divider for a  $5\text{-GHz}$  wireless LAN receiver," IEEE J. Solid-State Circuits, vol. 35, pp. 780–787, May 2000.
- [6] M. Zargari et al., "A  $5\text{-GHz}$  CMOS transceiver for IEEE 802.11a wireless LAN systems," IEEE J. Solid-State Circuits, vol. 37, pp.1688–1694, Dec. 2002.
- [7] T. Schwanenberger, M. Ipek, S. Roth, and H. Schemmann, "A multistandard single-chip transceiver covering  $5.15$  to  $5.85\text{GHz}$ ," in IEEE Int.Solid-State Circuits

- Conf. Dig. Tech. Papers, Feb. 2003, pp. 350–351.
- [8] N. Krishnapura and P. R. Kinget, “A 5.3-GHz programmable divider for HiPerLAN in 0.25- $\mu$ m CMOS,” IEEE J. Solid State Circuits, vol. 35, pp. 1019–1024, July 2000.
- [9] J. Yuan and C. Svensson, “High-speed CMOS circuit technique,” IEEE J. Solid-State Circuits, vol. 24, pp. 62–70, Feb. 1989.
- [10] J. M. Hsu, G. K. Dehng, C. Y. Yang, C. Y. Yang, and S. I. Liu, “Lowvoltage CMOS frequency synthesizer for ERMES pager application,” IEEE J. Solid-State Circuits, vol. 48, pp. 826–834, Sept. 2001.