Thyristor/Diode-Bypassed Sub-Module Power-Groups for Improved Efficiency in Modular Multilevel Converters

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Thyristor/Diode-Bypassed Sub-Module Power-Groups for Improved Efficiency in Modular Multilevel Converters

Paul D. Judge, *Member, IEEE,* Michael M.C. Merlin, *Member, IEEE,* Tim C. Green, *Senior Member, IEEE,* David R. Trainer and Konstantin Vershinin *Member, IEEE*.

***Abstract*—The half-bridge Modular Multilevel Converter (MMC) is a Voltage Source Converter (VSC) with high efficiency, controllability and modularity. The topology is weak to DC side faults unless bipolar sub-modules are used, but this results in decreased efficiency. Power-Groups (PGs), a thyristor augmented multilevel structure, have been proposed as a way to reduce the power-loss increase arising from achieving DC-fault-tolerance. This paper investigates whether the PG concept can also achieve significant efficiency improvements in VSCs that are not required to be DC fault tolerant. A Single Sub-Module Voltage (SSMV) method of controlling the turn-on/turn-off of the thyristor assembly within each PG structure is presented and the differences with the previously detailed Dual Sub-Module Voltage (DSMV) technique are described. Two thyristor-based PG structures for use in non-DC-fault-tolerant MMCs are proposed, one using SSMV and the other using DSMV. A comparison is made considering the required semiconductor device count, the impact on thyristor snubber design, and the overall power-losses achieved. A further, simplified, variant using a diode bypassed PG structure is presented which results in power-loss reductions during rectifier mode only. Results show that power-loss reductions of ∼20-25% can be achieved by using the proposed PG structures to augment a half-bridge MMC.**

***Index Terms*—AC-DC Power Conversion, Converters, HVDC Converters, HVDC Transmission, Thyristor Converters, Thyristor Applications.**

I. Introduction

The Half-Bridge (HB) Modular Multilevel Converter (MMC) is now the conventional topology used for Voltage Source Converter (VSC) based HVDC systems and is offered by several manufacturers. The topology offers low-losses, high controllability, high quality current waveforms, and its modular construction offers simplified expansion to higher voltage ratings [1]. The HB-MMC offered a generation leap in terms of efficiency over previous iterations of 2- and 3-level VSCs for HVDC applications, with an approximate 40% reduction in overall converter losses [2]. However, the power losses are still a very significant component of the lifetime cost of the equipment and there is strong pressure to reduce those power losses. Since its introduction, work on improving the efficiency the MMC has mostly addressed those derivatives of the MMC topology which are designed to be capable of preventing AC side contribution to DC-side faults [3]–[9]. Preventing this fault current contribution requires a sufficient number of bipolar sub-modules (SMs) be included in the design, which necessitates placing more IGBTs in the conduction path, resulting in lower power efficiencies.

There has been relatively little research directed at improving the efficiency of the HB-MMC. The work that has been reported focuses mostly on alternative semiconductor devices, or modifications to the control strategy. In [7] the authors investigate several SM topologies, and compare expected losses when using IGBTs and IGCTs as the switching devices within the converter. In [10] the authors present an investigation into the potential of future SiC JFET switching devices to improve the efficiency of MMC converters. Some works have looked at modifying the circulating current flowing within the MMC in order to reduce losses by taking advantage of the superior conduction characteristics of the anti-parallel diodes within each IGBT module [11], [12]. Other research effort has also been placed into SM balancing techniques that allow for reduced switching losses within the converter, whilst also achieving low deviation in capacitor voltages [13]–[15].

Power-Groups (PGs) [16], [17] are modular structures of series connected sub-modules, with a low-loss parallel bypass branch containing a thyristor assembly, comprised of an anti-parallel connection of series thyristors, and a series inductance used to limit dI/dt and dV/dt stresses. By series connecting PGs together a multilevel converter valve could be constructed and that valve used in any modular multilevel converter topology. The SMs in each PG can be used to generate a voltage output when the thyristors are in a blocked state, as well as to actively control the turn on/off of the thyristors as required. This allows the bypass branch of each PG to be utilized independent of the state of the other PGs within the valve. When the SMs in an individual PG are not required to generate part of the overall valve voltage waveform, the thyristors within that PG can be used conduct current. Because thyristors are available with significantly higher voltage and current ratings than IGBTs, as well as having superior conduction characteristics, the conduction power-loss within the thyristor bypass branch of each PG is significantly lower than the SM branch. If the thyristor bypass branches within each PG in the multilevel valve are used for a significant

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fraction of the period, then useful efficiency gains during normal operation can be made. This concept is illustrated in Fig. 1, with three PGs connected in series (Note that the inclusion of the commutation inductors within the PG does not alleviate the requirement for external inductors within the converter for current control purposes). The original aim of the PG proposal was to achieve high efficiency VSCs that are also tolerant to DC faults. In [17], a PG augmented Hybrid MMC [4] was found to have power losses in the region of 0.4% of rated power, and a PG augmented variant of the Extended-Overlap Alternate Arm Converter [18]–[20] was found to achieve power losses in the region of 0.3% of rated power. These values should be compared to power losses in the region of 0.45% of rated power for the HB-MMC and 0.58% of rated power for the Hybrid MMC.

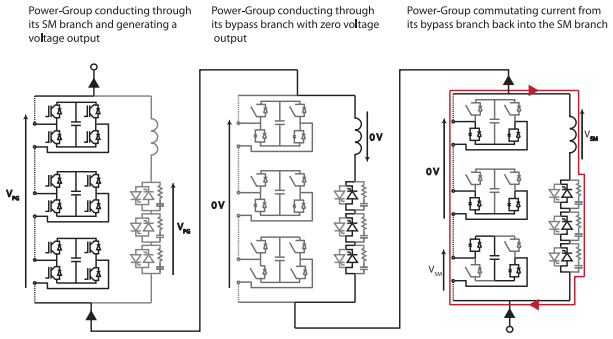

Fig. 1. Illustrative example showing three full-bridge SM Power-Groups connected in series, each of which is in a different conductive state.

The PG structures examined in [16], [17] focused exclusively on PG variants that included sufficient negative voltage capability from their SMs to facilitate DC fault tolerance. The purpose of this paper is to establish how effective PG augmentation is in reducing power losses in non-DC-fault-tolerant MMCs. The approach is to undertake a converter design and perform detailed simulations of a case-study converter. The submodules will be predominantly HB, i.e., a small number of bipolar SMs are employed to commutate the thyristors but not a sufficient number to control current flow with no DC bus voltage present. The paper is structured as follows: Section II examines the design of PG structures for use in a non-DC-fault-tolerant MMCs. A method for controlling the turn-on/turn-off of the PG bypass thyristor branch within each PG using a single SM voltage is described. The impacts of this method on the sizing of the PG commutating inductance, the magnitude of the PG thyristor turn-off losses, and the design of the PG thyristor snubber are investigated. A comparison between PG augmented MMCs using two different turn-off strategies/PG designs is then discussed. Section III then examines a PG design in which the thyristor assembly within the bypass branch of each PG is replaced with an upwards-facing diodes. This simplifies the design and control of the PG, but limits the use of the bypass branch to rectifying operation only. A new hybrid turn-on/turn-off method for this diode bypassed PG is also described. Conclusions are then drawn in Section IV.

II. Power-Groups for Non-Fault Tolerant Modular Multilevel Converters

In PGs, the commutation of the current between the SM branch and the thyristor bypass branch is controlled using voltages generated by the SM branch. The magnitude of the commutating voltage employed was found to have a strong impact on both the size of the commutating inductor required within each PG and the magnitude of the losses incurred within the thyristors during turn-off. A Dual SM Voltage (DSMV) technique was devised that used the bipolar output voltage of FB-SMs to create small differential voltages between SM with slightly different capacitor voltages and apply this as the commutating voltage for the thyristor [17]. This was found to result in lower turn-off losses within the thyristor valve, as well as a reduction in the the required size of commutation inductor. The specification of the PG design in [17], as well as the devices used within simulations are given in Table. I.

TABLE I
Power-Group Specification

Number of sub-modules per power-group	8
Number of thyristors	6 (arranged in anti-parallel with 3 devices in series)
Nominal sub-module voltage	1800 V
Nominal power-group voltage	14.4 kV
DC current rating	1500 A
IGBT used	Infineon FZ1500R33HE3 - 3300 V 1500 A
Thyristor used	Infineon T2871N - 8000 V 2600 A
Thyristor turn-off time (t_q)	550 μs
Hold-off time applied to thyristor valve ($t_{hold-off}$)	1000 μs

In [17], the requirement to achieve DC-fault-tolerance meant FB-SM were required to be included within the design. Two PG structures were considered, one containing solely FB-SMs and one a 50:50 split of FB and HB-SMs. In both cases, DSMV could be readily implemented as sufficient FB-SMs were already present in the PG to create the required differential voltages. For a PG designed to be used in a non-DC-fault-tolerant converter, i.e., not capable of generating enough negative voltage to oppose the flow of AC fault current during a DC side fault, the sole purpose of the FB-SM's negative voltage capability is to generate the commutation voltages required during turn-on or turn-off of the thyristors. The required number of FB-SMs (or similar bipolar SM type) is therefore solely dependent on the thyristor turn-off strategy that is employed. In this section, a comparison is made between PG augmented MMC designs that utilize the DSMV technique proposed in [17], and designs that use a Single SM Voltage (SSMV) to control the turn-on/turn-off of the thyristors within each PG. The proposed procedure to perform this controlled commutation using a single SM is given in the following subsection. The two PG designs are illustrated in Fig. 2.

A. Single SM Voltage Generation

This subsection describes the proposed method for controlling the turn on/off of the thyristors within a PG, using a Single SM Voltage (SSMV). The proposed method is illustrated in the sub-figures of Fig. 3. Each sub-figure has, below, an accompanying paragraph describing in detail the relevant state of the commutation process. The descriptions are given assuming the upwards-facing thyristors are to be triggered on

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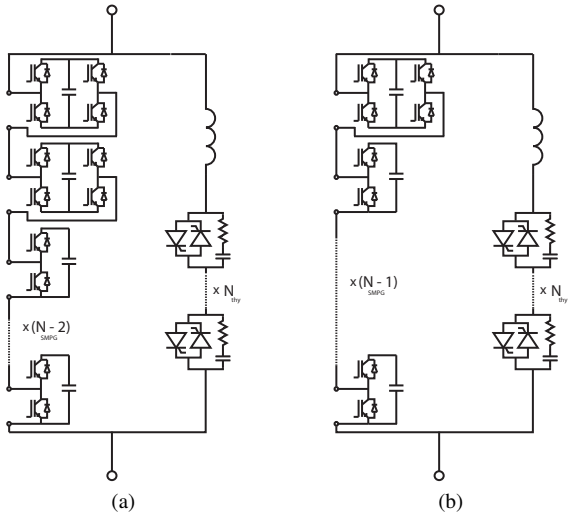

Fig. 2. Proposed thyristor bypassed power-group structures for non-DC-fault-tolerant converters. (a) Thyristor bypassed HB-PG with dual FB-SMs for turn-off control. (b) Thyristor bypassed HB-PG with single FB-SM for turn-off control.

and then later commutated off. The same process can mostly (with some differences discussed in the below subsections) be applied to the downwards-facing thyristors, with an inversion in the polarity of the voltages generated. The commutation inductor size used in the simulations results presented was selected as 200 μH. This choice was made to limit the initial di/dt through the thyristors at turn-on to 10 $A/\mu s$, assuming the use of SMs with nominal voltages in the region of 2000 V.

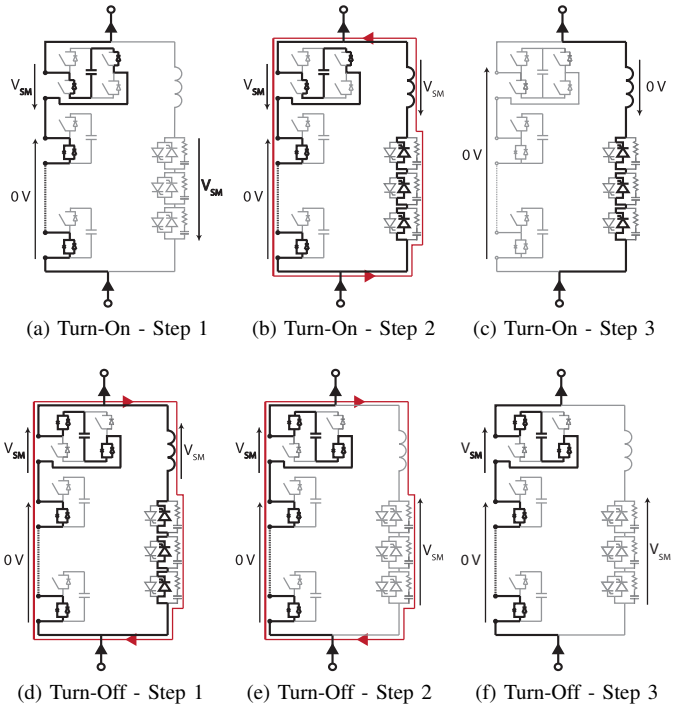

Fig. 3. Turn-on/turn-off control of PG thyristors using a single SM voltage (SSMV) to generate the commutation voltage - Black lines indicate that current is being conducted, grey indicates that there it is not. Red lines show circulating currents within the PG, forcing current into/out of the thyristor branch.

Prior to the thyristor turn-on, the arm current flows solely through the SM branch, with the thyristors in a blocking state. The SMs within the PG are available for the converters current controller to use.

a) Turn-on - Step 1: The FB-SM (a HB-SM could potentially be used in the case of firing the downwards facing thyristor) is set to a blocked state, all other SMs within the stack are set to generate zero volts. The blocked SM outputs a voltage which opposes the flow of the arm current. This voltage is such that it forward biases the thyristors to be fired. The blocked SM's capacitor voltage will increase during this time as it is conducting the arm current. To limit the magnitude of this voltage rise it is desirable that there would be as little delay as possible from this step until the thyristor firing pulse is sent.

b) Turn-on - Step 2: A triggering pulse is sent to the upwards facing thyristors. The forward voltage placed across it by the blocked FB-SM collapses and now appears across the commutating inductance. The current in the thyristors increases at a rate determined by the magnitude of the voltage imposed by the blocked FB-SM and the commutating inductance.

c) Turn-on - Step 3: The arm current fully commutates into the thyristor branch. The blocked FB-SM effectively open-circuits the current path through the SM branch and outputs zero volts.

A SPICE simulation of the proposed turn-on procedure is shown in Fig. 4. The time period 50-100 μs corresponds to step 1, where one of the SMs is first blocked, with all other SMs within the PG set to a bypass state. The blocked FB-SM outputs a voltage which opposes the flow of current through the SM branch, forward biasing the thyristors that are to be triggered. At t=100 μs the thyristors are sent a triggering pulse (step 2). The voltage across the thyristors collapses, and appears across the commutating inductance, driving a circulating current around the PG which forces the arm current into the thyristor branch. The di/dt at the start of turn-on is limited to ~ 10 $A/\mu s$, which increases significantly once the inductor is driven into saturation. The average di/dt for the process is ~ 30 $A/\mu s$, which is an order of magnitude below the specified critical di/dt limit of the thyristors (300 $A/\mu s$). Once the current is fully commutated from the SM branch it may conduct through the thyristors for a significant portion of a fundamental cycle (step 3).

To turn-off the PG thyristors using a single FB-SM, the following procedure is proposed:

d) Turn-off - Step 1: One SM is actively switched so that a reverse voltage is applied across the thyristors and commutating inductance. If the arm current is flowing in a downwards direction, this action must be performed by the FB-SM within the PG. If the current is flowing in an upwards directions, any of the SMs within the PG could be used. In both cases the polarity of the arm current and voltage to be generated results in the capacitor of the SM used to carry out this step being discharged. A circulating current is driven around the PG which commutates the current from the thyristors. The other SMs are kept in a bypass state. The thyristor current crosses zero as the stored charge within the thyristor is recovered.

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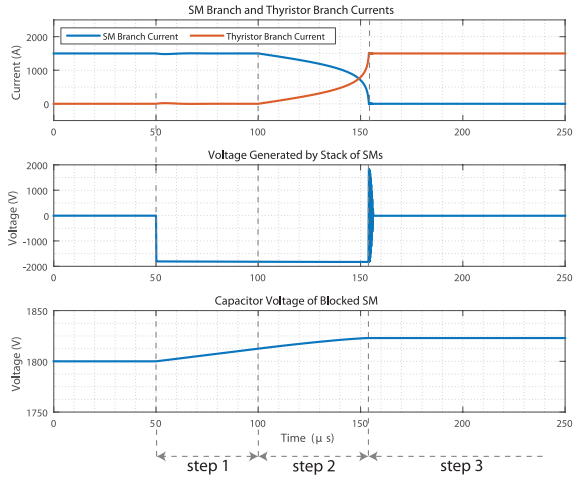

Fig. 4. Overall PG turn-on process when using a full SM voltage to generate the commutating voltage. Commutating inductor is a 200 μH saturable inductor with a 500 A saturation characteristic.

e) Turn-Off - Step 2: The thyristor junction recovers its reverse voltage blocking capability and the commutating voltage provided by the SM is now imposed across the thyristors, resulting in reverse-recovery losses.

f) Turn-off - Step 3: The reverse recovery current from the thyristors decays to zero as the stored charge is recovered. The arm current is then solely conducting in the SMs. If the arm current is flowing in an upwards direction the duty of which SM within the stack is used to hold the thyristors reverse biased could be rotated so as to limit the deviation of SM voltages from each other. If the arm current is flowing in a downwards direction however, only the FB-SM may be used, as holding the thyristors that had been conducting reverse-biased in this case requires a negative voltage to be applied. The maximum change in the FB-SM capacitor voltage (ΔV_c) in this case, during this step, can be approximated using (1), where C is the SM capacitor size and $t_{hold-off}$ is the hold-off time applied to the PG thyristors. For the considered converter designs given in Table. III, and assuming the FB-SM capacitor size is the same HB-SMs, this results in a ΔV_c of approximately 150 V, or $\sim 8\%$ the nominal SM capacitor voltage. It should be noted that this process always results in a decrease in the FB-SM capacitor voltage, which eliminates the potential for the turn-off procedure to result in an SM over-voltage event. The FB-SM capacitor size could potentially be increased to limit the magnitude of this discharge, however simulation results (shown in Fig. 7) indicate that SM balancing algorithms, which can act when the PG is not utilising its bypass thyristors, are sufficient to prevent the FB-SM from running away in terms of voltage from the other SMs within the PG.

$$\Delta V_c = \frac{\hat{I_{arm}} t_{hold-off}}{C} \tag{1}$$

After the turn-off procedure (which could take up to 1 ms due to the t_q value of the thyristor) has completed the thyristors have regained their forward voltage blocking ability, and the PG becomes free to use its SMs to generate a voltage output.

A SPICE simulation of the SSMV turn-off procedure, with varying arm current magnitudes, is shown in Fig. 5. A saturable inductor was used instead of a linear inductor since this would achieve a considerable volume saving while still adequately controlling commutation. Initially, the current is conducted by the thyristor branch. At t=100 μs (step 1) a reverse voltage is applied across the commutating inductor and thyristors by switching one of the SMs (SM 1) within the PG. The current in the thyristor branch is forced through zero and goes negative as the thyristors stored charge is recovered. Between t=160-195 μs (step 2), depending on the arm current magnitude, the thyristors regain their reverse voltage blocking capability. A t=350 μs the thyristor fully recovers (step 3). At t=400 μs the SM used to keep the thyristors reverse biased is changed to another SM (SM 2) and SM 1 is switched to bypass at this point. As noted in the previous section, this rotation in duty can only occur if the current was flowing through the upwards facing thyristors. The thyristors are held reverse-biased in this manner for the remainder of the hold-off time (1 ms in the given design), which must be sufficiently greater than the turn-off time of the thyristors (550 μs for the chosen devices). The overall power-loss incurred in the PG thyristors, including losses within the snubber network, varies from 13.25 J at 300 A to 22.66 J at 1500 A arm current magnitude.

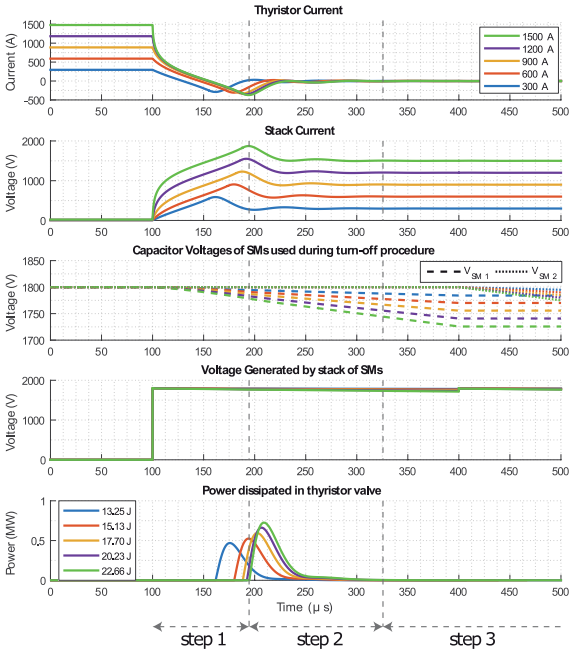

Fig. 5. Thyristor turn-off procedure using single sub-module voltage (SSMV). The 200 μH inductor in series with the thyristors is modeled with a 500 A saturation characteristic. turn-off losses for each case are given in the last sub-plot.

B. Impact on Snubber Design

As discussed in [17], PGs require a snubber network to be placed across the thyristor assembly to limit the dV/dt stress imposed across the thyristors by the switching actions of the SMs in the parallel branch. As discussed in the previous

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subsection, thyristors are normally forward biased by a voltage created by a SM prior to triggering to ensure reliable turn-on. This results in the snubber capacitors being discharged into the thyristor through the snubber resistor at turn-on. The snubber resistor must therefore also be sized to limit the peak discharge current into the device [21]. For a given target peak discharge current magnitude the minimum resistor size that can be used is therefore dependent on the voltage that is placed across the thyristor prior to firing, which in turn is determined by the turn-on/turn-off method employed. If DSMV is used, this results in voltages in the region of $\sim$ 66 V (200 V overall split between 3 thyristors in series) being placed across each thyristor, while SSMV results in voltages in the region of 600 V (2000 V overall split between 3 thyristors in series) being placed across each thyristor. To limit the peak discharge current to a value in the region of 100 A results in minimum resistor values of $\sim 0.6\ \Omega$ and $6\ \Omega$ respectively.

A comparison of snubber designs for PG designs using DSMV (using $L = 30\ \mu H$ as discussed in [17]) and SSMV (using $L = 200\ \mu H$ as discussed at the start of this section), showing variation in the critical design considerations (settling time, peak current draw, peak dV/dt stress and energy loss per SM switching event) is given in Fig. 6. A dV/dt design limit of 600 $\frac{V}{\mu S}$ across the thyristor assembly is considered as this an order of magnitude below the critical dV/dt limit of the devices considered. For PG designs with a 30 μH inductor, this requirement limits the practical R and C choices, and results in the most optimal snubber designs having losses in the region of 0.1 J per SM switching event. For the $200\mu H$ inductor the target dV/dt limit is easily achievable across a wider range of R and C values, allowing snubber losses to be reduced by an order of magnitude to $\sim$0.01 J per SM switching event.

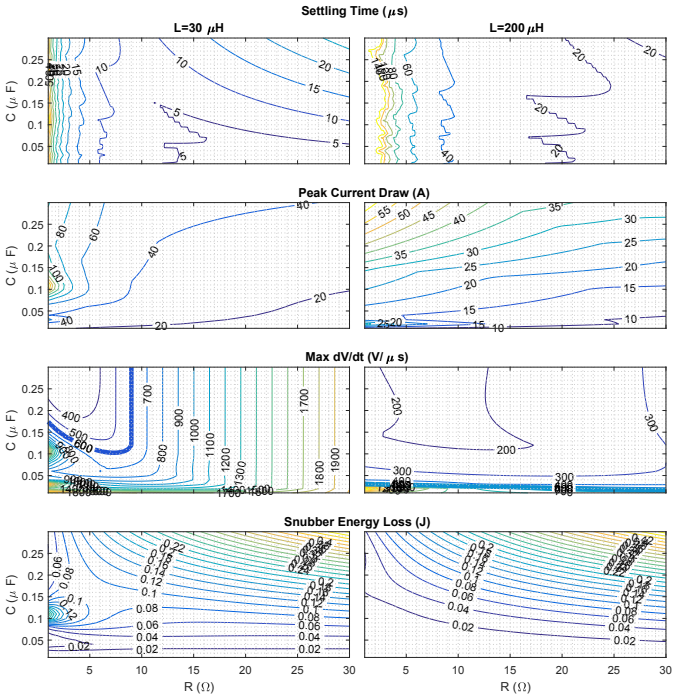

Fig. 6. Snubber design comparison considering cases of a 30 μH and 200 μH commutating inductance within the PG. From Top: Snubber settling time. Peak current draw. Peak dV/dt stress imposed across thyristors (dV/dt design limit shown in bold). Energy loss in snubber network per SM switching event.

TABLE II
DESIGN COMPARISON FOR A PG DESIGN WITH 8 SMS

Turn-off method	SSMV	DSMV
Required Number of bipolar SMs	1	2
Required Number of half-bridge SMs	7	6
Number of IGBTs within the conduction path	9	10
Required commutation inductor size	$\sim$200 uH	$\sim$30 uH
Loss per turn-off event (at 1500 A)	$\sim$20 J	$\sim$2 J
Snubber loss per SM switching event	$\sim$0.01 J	$\sim$0.1 J

III. CONVERTER COMPARISON WITH PG DESIGNS USING DSMV AND SSMV

This section compares the designs of a PG augmented MMC using both considered turn-off/turn-on strategies. A comparison of the consequences of the two turn-off methods on the overall PG design is shown in Table II. If the SSMV technique is used then only one bipolar SM is required within each PG. If the DSMV technique proposed in [17] is to be used then two bipolar SMs are required within each PG with resulting increase in conduction losses. On the other hand, SSMV imposes a larger commutating voltage and therefore a larger commutation inductance is required to limit both the di/dt during turn-on of the thyristors, and to limit the reverse recovery current and power-loss within the thyristors at turn-off [17]. The commutation inductor in the PG using SSMV is sized to limit the di/dt through the thyristor valve at turn-on to a value of 10 $A/\mu s$. For the DSMV-PG the commutation inductor is sized to allow for effective dV/dt snubbering of the thyristors [17].

The level of power-loss reduction that can be achieved by using the PG concept is strongly linked to the fraction of time for which the low-impedance bypass branch within each PG can be used. This has been found to be influenced not only by the wave-shape of the converter arm voltage but also by the thyristor turn-off method employed. Compared to SSMV, DSMV causes lower turn-off losses within the thyristor assembly as well as requiring a smaller commutation inductor. The notable disadvantage of DSMV is that the differential voltage between two SMs must be controlled by actively discharging one of the SMs within the PG by inserting it into the current path prior to the firing of the PG thyristor assembly. This introduces a delay in how fast the thyristor is fired once the logical firing signal for the thyristor is received from the controller. As the PG structure that utilizes SSMV does not require this step, the thyristor can be fired once the decision to utilize that PGs thyristor is made. This leads to slightly improved utilization of the thyristor branch.

Simulation results from an Augmented MMC (A-MMC) that has been augmented with both the SSMV and DSMV PGs are shown in Fig. 7. The converter control scheme used for the simulation results is similar to the ones presented in [22], [23], with an energy controller that regulates the sum energy within each converter arm by generating balancing current references. Current control is achieved by using an

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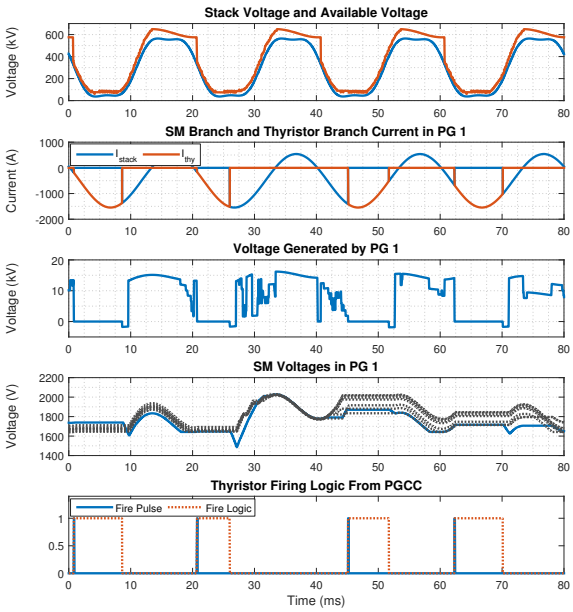
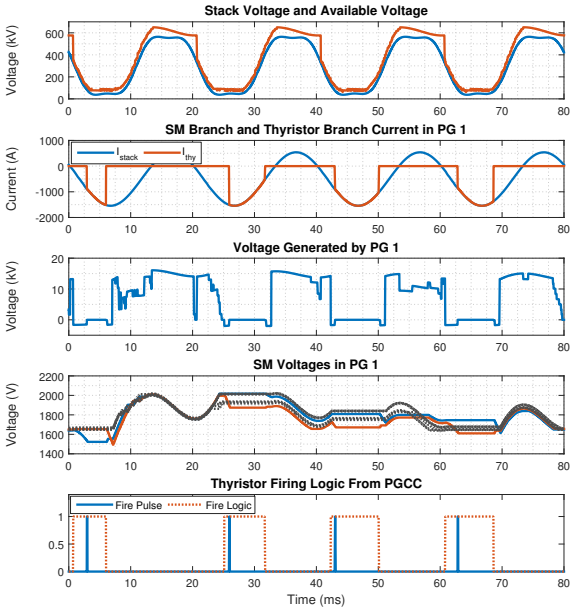
LQR derived state feedback controller. The addition of the PGs requires little modification to overall MMC control scheme, with changes exclusively required in the low-level control i.e where the voltage references from the current controller are converted into gating signals for IGBTs. Decisions on when to turn-on/turn-off are made using PS-PWM [24], with a forward looking estimate of each PGs carrier signal and the overall stack voltage demand used to account for the delay introduced by the PG turn-off procedure. SM voltage balancing and modulation is achieved using a sorting mechanism which takes into account which SMs are available to it (i.e not bypassed or being used as part of a PG turn-on or turn-off process).

In both cases the PG bypass thyristors can be seen to tend to be used when the stack voltage is low, corresponding to the point where most PGs within the overall valve are not required for voltage generation. For SSMV, the thyristor is sent a firing pulse once the Fire Logic from the controller is received. For DSMV, a delay is introduced because of the need to establish the correct differential voltage prior to firing the PG thyristor assembly. These delays reduce the utilisation of the bypass thyristors, in comparison to the SSMV case, where no such delay is present. The length of this delay is dependent on the voltages of the SMs within the PG when the firing logic signal is received. In most cases, the required delay is relatively short (average measured as $\sim$1 ms) but in some cases a longer delay is introduced, such as at t=61 ms in Fig. 7b. Such longer delays occur when the arm current is at a low magnitude, reducing the rate at which the chosen FB-SM can be actively discharged, and when the FB-SMs are close to each other in terms of capacitor voltage, increasing the amount by which the chosen FB-SM must be discharged before the correct differential voltage can be generated. These delays could potentially be reduced by applying a more advanced SM balancing mechanism, which attempts to keep the difference between the FB-SMs close to the target differential voltage, this is not considered in this paper however.

Estimated power-losses of Augmented MMCs (A-MMC) with both considered PG structures are given in Table IVb. The specifications of both variants are given in Table III. The semiconductor devices considered are given in Table I. The thyristor utilization index (ϕ_{thy}) gives an indication of the extent to which the bypass branch of the PGs are utilized [17]. It is calculated as the ratio of the average current flowing through all PG thyristors to the overall average arm current ($\phi_{thy} = \frac{\overline{I_{thy}}}{\overline{I_{arm}}}$). The value of ϕ_{thy} can be seen to be slightly higher for the PG structure that employs SSMV, due to the removal of the active discharge portion of the turn-on procedure. This, combined with the lower number of IGBTs within the conduction path, result in lower IGBT conduction losses for the SSMV PG compared to the DSMV PG. The turn-off losses incurred within the SSMV-PGs are an order of magnitude greater than those of DSMV-PGs due to the reduction in magnitude of the commutating voltage applied at turn-off. In both cases the reduction in IGBT conduction losses dominates the additional losses incurred in the thyristors and additional switching losses caused by the turn-on/turn-off procedure. For the MMC augmented with SSMV-PGs, the power-loss reduction, compared to a standard half-bridge MMC, varies from $\sim 18-25\%$, depending on the operating-point. For the MMC augmented with DSMV-PGs the reduction is in the region of $\sim 11-20\%$. This indicates if the size of the commutating inductor is not a limiting factor then SSMV is the best PG design option to choose. This is because the additional IGBT conduction (due to higher thyristor utilisation) and snubber loss reductions which it allows exceed the additional



(a) A-MMC with SSMV-PG



(b) A-MMC with DSMV-PG

Fig. 7. Power-group voltage and currents of an Augmented Modular Multi-level Converter operating at rated power as an inverter. The upper plot (in each sub-plot) shows the voltage generated by overall valve of series connected PGs in the upper arm of phase A, and the instantaneous available voltage within the valve (indicating how many PGs are utilizing their bypass branch). Lower plots show currents and voltages from one (of 42) PG within that valve. FB-SM capacitor voltages are shown in solid lines, HB-SM capacitor voltages are shown in dashed lines.

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(in comparison to DSMV) thyristor turn-off losses incurred.

IV. Rectifying Diode Power-Group

The PG structures examined in the previous section are capable of using the low-impedance thyristor bypass branch irrespective of the arm current polarity. This section will examine a PG structure, shown in Fig. 8, where the bi-directional thyristor valve is replaced by a series connection of diodes. As will be explained later in this section, a FB-SM has been found to still be required in the design to aid in the commutation of the arm current into the diode bypass branch within the PG, even though negative voltage capability is not required to force the current from the thyristor branch back into the SM branch. The replacement of the bi-directional thyristor assembly with uni-directional series-connected diodes means that the bypass branch cannot be used when the current is flowing in a downwards direction and therefore the PG structure can only reduce power-losses significantly in rectifying mode. This PG structure may be useful however in applications where the converter operates in rectifying mode for a high proportion of its service, for example in off-shore wind-farms or converter stations that are in close proximity to a generating station. In addition to the efficiency improvements that this diode bypass branch may bring, it may also have other advantages, in particular improved DC fault ride through tolerance due to the high surge current rating of the diodes within the bypass branch. This however is not the prime purpose of the proposed diode bypass branch, and is not the focus of this paper.

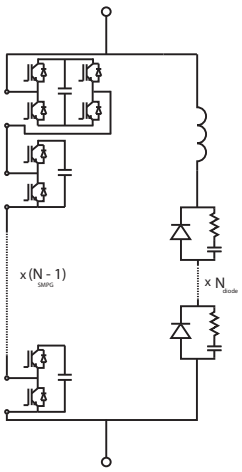

Fig. 8. Diode bypassed half-bridge power-group structure

The replacement of the thyristors with diodes leads to several simplifications to the design. Diodes have higher tolerance to dV/dt and di/dt stresses, and so the main factor that determines the commutation inductor becomes the limitation of turn-off losses in the diode assembly and the limitation of the peak reverse recovery current. In addition diodes do not exhibit the characteristic turn-off time of thyristors, meaning that their reverse blocking capability is regained once the stored charge within the junction is evacuated at turn-off. This results in a simplification of the turn-off procedure, with a removal of the need to hold the diode assembly reverse-biased once the current has been commutated back into the SM branch which in turn leads to higher utilization of the bypass branch.

A. Turn-on and turn-off control

The SSMV method discussed in Section II-A, for thyristor bypassed PGs, can be applied to the proposed DB-PG, but with a reduction in the time that the diode is held reverse biased after turn-off, as diodes do not have the characteristic hold-off requirement of thyristors.

Taking the removal of di/dt limitation requirements at turn-on into account, it has been found possible to apply a hybrid SM voltage (HSMV) turn-on/turn-off control to the DB-PG, which combines elements of both SSMV and DSMV, while also only requiring one FB-SM to be included within each PG. This proposed HSMV method uses a full SM voltage to force the current into the diode branch, and a differential voltage to commutate current back into the SM branch when required.

The proposed HSMV technique is illustrated in Fig. 9. In the first step the FB-SM is actively discharged to a voltage below one of the HB-SMs in the PG, so that it can later be used as part of a differential pair during the turn-off procedure. Once this is achieved the FB-SM is blocked, causing a voltage to be imposed across the commutating inductance which drives a circulating current around the PG, commutating the arm current into the diode bypass branch. To turn-off the diode the FB-SM is left in a blocked state. The half-bridge SM which the FB-SM was initially discharged below is then switched so that it generates a positive voltage. This results in the difference in voltage between the FB-SM and the HB-SM being imposed across the commutating inductance, driving a circulating current which commutates the arm current from the diode bypass branch back into the SM branch. Once this is achieved the PG can then immediately generate a positive voltage output again. This is in contrast to the thyristor bypassed PG structures, where a hold-off period must be applied.

B. Commutating Inductor Sizing

A SPICE simulation of the turn-off of the diode bypass branch, with varying commutation inductor sizes, is shown in Fig. 10. The diode used is a 6.8 kV 2.8 kA D3001N60T rectifier diode from Infineon Technologies [25], which was chosen for its low conduction losses. Each diode assembly within each PG is considered to be formed of four series diodes.

In the case of SSMV being applied, the lowest inductor size considered (150 μH) results in a peak reverse recovery current is ∼500 A, reducing to ∼250 A for the largest inductor (300 μH). The losses decrease in inverse relation to the inductor size from 27.2 J to 18.57 J. These losses are similar to those found in the SSMV-PG with thyristor bypass. Note that while there is significant overshoot in the voltage across the diode assembly (to ∼4000 V), this is not considered an issue as the assembly will be rated to block the combined voltage of 8 SMs (∼16 kV).

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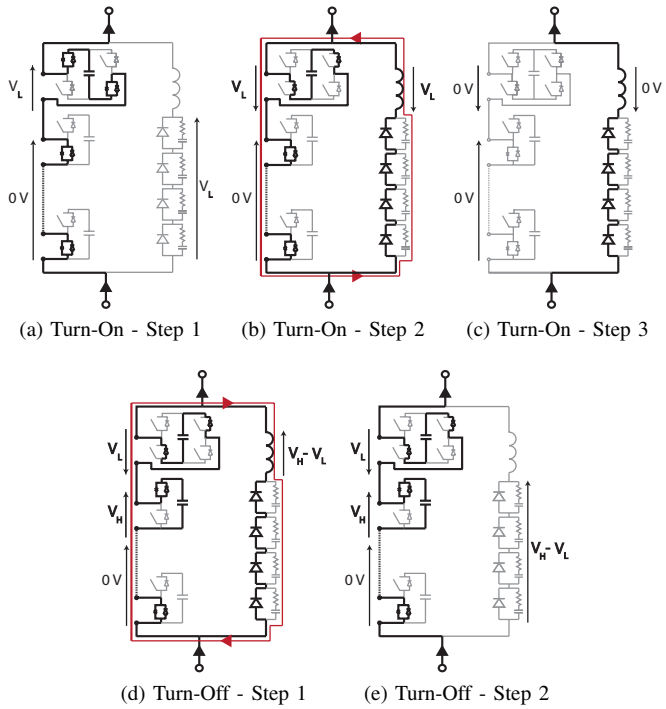
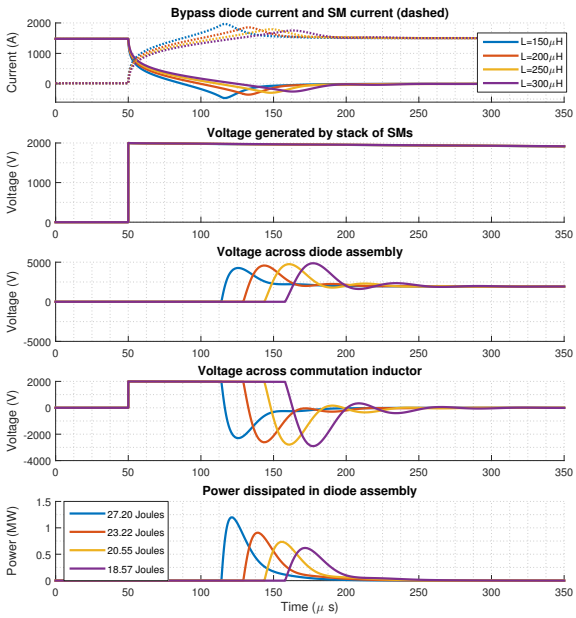


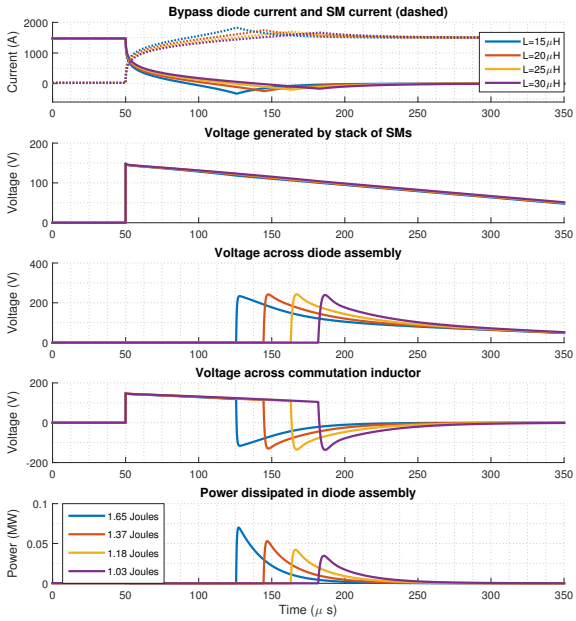
(a) Turn-On - Step 1 (b) Turn-On - Step 2 (c) Turn-On - Step 3

(d) Turn-Off - Step 1 (e) Turn-Off - Step 2

Fig. 9. Turn-on/turn-off control of diode bypass branch using a hybrid SM voltage (HSMV) commutation voltage generation - Black lines indicate that current is being conducted, grey indicates that there it is not. Red lines show circulating currents within the PG, forcing current into/out of the diode branch.



(a) Using a single 2 kV SSMV voltage



(b) Using 150 V generated with HSMV

Fig. 10. Turn-off of the diode bypass branch using with varying commutation inductance sizes.

In the case of HSMV being used, the commutating voltage is significantly lower, resulting in a reduction in the required size of the commutating inductor. Reverse recovery current magnitudes are also reduced. The magnitude of the turn-off losses incurred in the diodes is also reduced significantly below the SSMV case, varying from 1.56 J (15 μH) to 1.03 J (30 μH).

For the case of the DB-PG using SSMV, a design using only HB-SMs was initially considered. For turn-off of the diodes the HB-SMs are capable of generating the positive voltage required to force the current from the diode branch into the SM branch. However, for commutation of the current from the SM branch to the diode branch, the driving voltage across the commutation inductor is only the small difference in forward voltage drop between the diodes of the SM IGBT modules and the forward voltage drop of the diode assembly in the bypass branch. A simulation of this unforced commutation, with variation in the saturation current of the commutation inductor, is given in Fig. 11. The time for the arm current to commutate from the SM branch to the diode branch is large in all cases and this would significantly decrease the utilization ratio of the bypass diodes. For this reason it is considered necessary to include one bipolar SM in order to force commutation of current into the diodes. The added FB-SM will only be required to generate a negative voltage when it is blocked and so a sparse FB could potentially be used in which the upper right IGBT within the bridge is replaced by a diode [8].

The difference in conduction voltages of SM and diode paths means that when the SMs are commanded to produce zero voltage, and the current is flowing upwards, the current will begin to commutate to the bypass branch, even when not intended. The amount of recovered charge in high voltage diodes does not vary to a large degree with the forward current through the diode [26], and so such events would result in additional losses within the converter due to unnecessary diode turn-off events occurring. In DB-PGs which utilise HSMV for turn-off control this poses a particular risk of very large reverse-recovery currents occurring if the diode branch were to accidentally conduct, and then be commutated off by an SM voltage which is an order of magnitude higher than it's commutating inductance is sized for. To prevent this the diodes must be actively held off (unlike the thyristor which are simply

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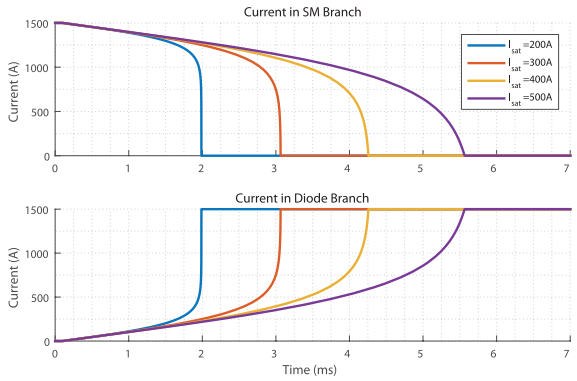
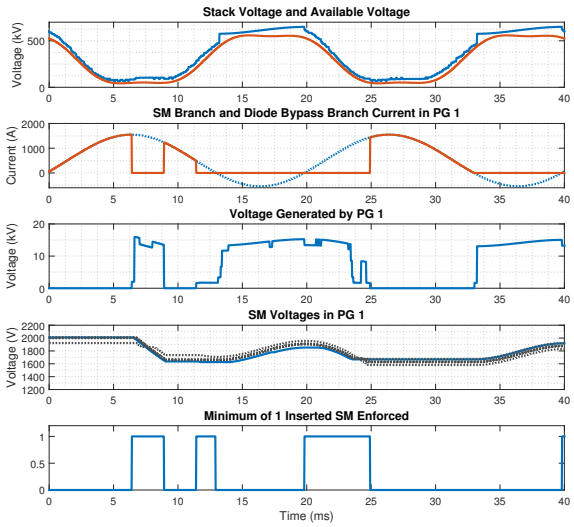


Fig. 11. Power-group voltage and currents of an Augmented Modular Multilevel Converter operating at rated rectifying power. Equivalent VI characteristic of diodes with SMs modelled with an intercept of 10 V and an on-state resistance of 0.01 Ω. Equivalent VI characteristic of diode bypass branch modelled with an intercept of 2.8 V and an on-state resistance of 0.0019 Ω.

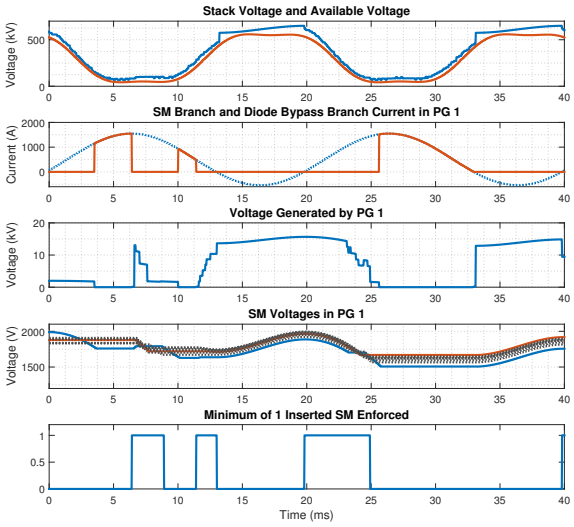
not triggered). This is achieved by modifying the modulation so that all PGs which are not commanded to be bypassed are assigned a voltage reference of at least 1 SM voltage, ensuring the current does no begin to commutate to the bypass branch.

Simulation results for an DB-PG augmented MMC using both SSMV and HSMV are given in Fig. 12. For the HSMV case the FB-SM must still be discharged prior to the commutation of the arm current into the diode branch. Similar to the thyristor bypassed DSMV case, this reduces the utilization of the bypass branch. In both cases the converter controller ensures that the diode bypass branch only conducts when it is commanded to by ensuring at least 1 SM in the PG keeps the diodes reverse-biased. This can be seen at $t = 11.25\ ms$ for the SSMV case, and $t = 7.5\ ms$ for the HSMV case.

Power-loss estimates for the Diode Bypassed A-MMCs (DB A-MMC) specified in Table. III, are given in Table IVc. For both cases, rectifying operation the converter has higher diode utilisation (ϕ_{diode}) than the thyristor utilisation in the equivalent thyristor bypassed A-MMC topologies resulting in a power-loss reduction approaching 26% (c.f. HB-MMC). This is due to the removal of the hold-off time required in the thyristor bypassed cases, allowing the bypass to be used for a longer period before it is required to be commutated off. For inverting operation the bypass branch is barely used which means the additional losses incurred in the snubber network and FB-SM within each PG are not compensated for. This results in an approximate 12% increase in losses at these set-points. Using SSMV results in higher utilisation of the bypass diodes, resulting in lower overall conduction losses. This is canceled out, however, by the reduced diode turn-off losses in the HSMV case, which results in the efficiencies of both variants being approximately equal.



(a) Using SSMV



(b) Using HSMV

Fig. 12. Diode bypassed PG voltage and currents in an A-MMC operating at rated rectifying power. Arm current shown in dashed line. FB-SM capacitor voltages are shown in solid lines, HB-SM capacitor voltages are shown in dashed lines.

TABLE III
CONVERTER SIMULATION MODEL SPECIFICATIONS

	DSMV A-MMC	SSMV A-MMC	SSMV DB A-MMC	HSMV DB A-MMC
Rated Power	900 MW	900 MW	900 MW	900 MW
DC Voltage	±300 kV	±300 kV	±300 kV	±300 kV
AC Voltage (Line to Line RMS)	367 kV	367 kV	367 kV	367 kV
SM Capacitor	9.6 mF	9.6 mF	9.6 mF	9.6 mF
N. of PGs	42	42	42	42
Total N. of SMs per PG	8	8	8	8
N. of FB-SMs per PG	2	1	1	1
N. of HB-SMs per PG	6	7	7	7
Total N. of SMs per PG	8	8	8	8
N. of SMs	336	336	336	336
Total N. of IGBTs	840	756	756	756
Total N. of Thyristors	252	252	0	0
Total N. of Bypass Diodes	0	0	168	168
PG Commutating Inductor Size	30 μH	200 μH	200 μH	30 μH

V. CONCLUSION

The potential of using Power-Groups (PG), which are structures of sub-modules containing a parallel bypass branch formed of series thyristors or diodes, to achieved efficiency gains in non-DC-fault-tolerant Modular Multilevel Converters (MMC) has been assessed. Results have shown that the PG concept can still be utilized to achieve significant power-loss reductions of ∼20-25%. The absolute losses achieved using the PG augmented topologies examined in this work are comparable to the most efficient PG augmented DC-fault tolerant topology (the Augmented Trapezoidal Alternate Arm Converter) presented in [17], though with significantly lower

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TABLE IV
POWER LOSS ESTIMATES FOR A HALF-BRIDGE MMC, AND A PG AUGMENTED MMC CONSIDERING FOUR TYPES OF PG STRUCTURES. POWER LOSS REDUCTION GIVEN IN COMPARISON TO THE HALF-BRIDGE MMC CASE.

(a) Half-Bridge MMC

P (pu)	-1	- 1	-1	1	1	1
Q (pu)	0.3	0	-0.5	0.3	0	-0.5
IGBT Conduction Loss	0.3802	0.3860	0.3636	0.4120	0.4153	0.3942
IGBT Switching Loss	0.0571	0.0484	0.0485	0.0555	0.0489	0.0473
Overall Loss (% Rated Power)	0.4374	0.4344	0.4121	0.4675	0.4642	0.4415

(b) PG Augmented MMC with Thyristor Bypassed Power-Groups

Turn-on/turn-off control applied:	SSMV						DSMV					
P (pu)	-1	- 1	-1	1	1	1	-1	-1	-1	1	1	1
Q (pu)	0.3	0	-0.5	0.3	0	-0.5	0.3	0	-0.5	0.3	0	-0.5
$\phi_{thy/diode}$	0.5502	0.5591	0.5726	0.5586	0.5191	0.5566	0.4745	0.4966	0.5035	0.4928	0.4348	0.4773
IGBT Conduction Loss	0.1676	0.1631	0.1496	0.1677	0.1887	0.1616	0.2206	0.2144	0.1978	0.2185	0.2483	0.2152
IGBT Switching Loss	0.0807	0.0709	0.0683	0.0723	0.0831	0.0734	0.0952	0.0860	0.0842	0.0890	0.1026	0.0907
Thyristor Conduction Loss	0.0514	0.0533	0.0516	0.0522	0.0490	0.0499	0.0451	0.0476	0.0459	0.0468	0.0423	0.0438
Thyristor Turn-On Loss	0.0092	0.0066	0.0077	0.0089	0.0124	0.0106	0.0101	0.0113	0.0105	0.0100	0.0097	0.0098
Thyristor Turn-Off Loss	0.0470	0.0490	0.0470	0.0469	0.0497	0.0488	0.0030	0.0032	0.0031	0.0031	0.0031	0.0031
Snubber Loss	0.0005	0.0005	0.0005	0.0006	0.0006	0.0006	0.0053	0.0049	0.0047	0.0058	0.0066	0.0063
Overall Loss (% Rated Power)	0.3565	0.3433	0.3245	0.3486	0.3835	0.3449	0.3793	0.3674	0.3463	0.3731	0.4125	0.3690
Power Loss Reduction Achieved (%)	18.497	20.970	21.241	25.428	17.375	21.891	13.281	15.436	15.973	20.184	11.130	16.429

(c) PG Augmented MMC with Diode Bypassed Power-Groups

Turn-on/turn-off control applied	SSMV						HSMV					
P (pu)	-1	- 1	-1	1	1	1	-1	-1	-1	1	1	1
Q (pu)	0.3	0	-0.5	0.3	0	-0.5	0.3	0	-0.5	0.3	0	-0.5
$\phi_{thy/diode}$	0.6033	0.6056	0.6214	0.0016	0.0080	0.0026	0.5304	0.5256	0.5440	0.0005	0.0011	0.0008
IGBT Conduction Loss	0.1443	0.1437	0.1294	0.4599	0.4621	0.4396	0.1737	0.1814	0.1608	0.4600	0.4637	0.4400
IGBT Switching Loss	0.0839	0.0765	0.0727	0.0571	0.0528	0.0459	0.1000	0.0889	0.0864	0.0572	0.0529	0.0460
Bypass Diode Conduction Loss	0.0674	0.0689	0.0669	0.0001	0.0006	0.0002	0.0601	0.0599	0.0591	0.0000	0.0001	0.0001
Bypass Diode Turn-Off Loss	0.0320	0.0330	0.0330	0.0060	0.0014	0.0080	0.0014	0.0010	0.0013	0.0000	0.0000	0.0000
Snubber Loss	0.0048	0.0048	0.0046	0.0036	0.0036	0.0035	0.0048	0.0047	0.0046	0.0036	0.0034	0.0034
Overall Loss (% Rated Power)	0.3324	0.3268	0.3067	0.5267	0.5205	0.4971	0.3400	0.3359	0.3123	0.5209	0.5201	0.4894
Power Loss Reduction Achieved (%)	23.993	24.770	25.577	-12.657	-12.124	-12.601	22.272	22.678	24.219	-11.423	-12.047	-10.842

number of required IGBTs ($\sim 55\%$) and SMs ($\sim 87.5\%$).

A method for controlling the turn-on/turn-off of the thyristor/diode bypass branch using a Single Sub-Module Voltage (SSMV), as opposed to the Dual Sub-Module Voltage (DSMV), has been presented and the design implications investigated. The SSMV technique results in the requirement to have a larger commutation inductance ($\sim$ 200 μH vs $\sim$ 30 μH for DSMV) within each PG, and also results in larger turn-off losses being induced within the thyristor assembly of each PG, but reduced losses within the dV/dt limiting snubber across each thyristor. When comparing MMC designs that use PGs designed for operation with SSMV and DSMV, greater power-loss reductions have been found to be possible when using SSMV. This is due to a reduction in IGBT conduction losses due to a need to include only one bipolar Full-Bridge (FB) SM within each PG, an increase in the utilisation of the bypass thyristors due to the removal of the active SM discharge procedure required by DSMV, and a reduction in losses within the dV/dt limiting snubber achievable due to the larger commutating inductor. These factors combine to exceed the thyristor turn-off power-loss reductions achieved with DSMV. A diode bypassed (DB) PG structure is also introduced, which shows promising power-loss reductions, although only when the converter is operating in rectifier mode. A Hybrid Sub-Module Voltage (HSMV) technique, which combines elements of both SSMV and DSMV, for controlling the diode turn-on and turn-off while also only requiring one FB-SM in each PG, has been described and compared against SSMV for the DB-PG case. The inclusion of the required FB-SM within each PG, and the additional power-losses associated with the snubber network, result in some power-loss increases ($\sim 12\%$) during inverting operation. Results indicate that the expected power-loss reductions in a PG augmented MMC, in comparison to the base-case of a standard half-bridge MMC, are in the region of 21% for the thyristor bypassed PG using SSMV, and in the region of 25% for the diode bypassed PG, using either SSMV or HSMV, during rectifying operation.

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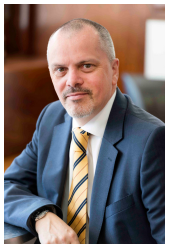

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