



Dymond, H., Liu, D., Wang, J., Dalton, J., & Stark, B. H. (2017). Multi-level active gate driver for SiC MOSFETs. In *2017 IEEE Energy Conversion Congress and Exposition (ECCE 2017): Proceedings of a meeting held 1-5 October 2017, Cincinnati, Ohio, USA* (pp. 5107-5112). Institute of Electrical and Electronics Engineers (IEEE).
<https://doi.org/10.1109/ECCE.2017.8096860>

Peer reviewed version

Link to published version (if available):
[10.1109/ECCE.2017.8096860](https://doi.org/10.1109/ECCE.2017.8096860)

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Multi-level active gate driver for SiC MOSFETs

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Abstract— Active gate driving has been shown to provide reduced circuit losses and improved switching waveform quality in power electronic circuits. An integrated active gate driver with 150 ps resolution has previously been shown to offer the expected benefits in GaN-based converters. However, the use of low-voltage, high-speed transistors limits its output voltage range to 5 V, too low for many emerging SiC and GaN devices. This paper introduces a series connection of two commercially available conventional drivers and an improved 5 V, 100 ps resolution active driver. The first conventional driver lifts the gate voltage from the negative hold-off voltage to just below the gate threshold voltage, the active driver performs active high-resolution control around the gate threshold, after which the second conventional driver raises the gate voltage to reach optimal $R_{ds(on)}$ values. This driver is demonstrated on a 900-V SiC MOSFET that requires a 15 V onstate gate voltage to achieve optimum $R_{ds(on)}$. The device is switched at 50 V/ns in a 100-kHz, non-synchronous, 1:10, 300-W boost converter, with the power device switching 600 V and 5 A. It is shown that the gate voltage can be affected on a 100 ps scale, and that meaningful changes to fast power waveforms can be achieved.

Keywords— SiC; active gate driver; oscillation; electromagnetic interference (EMI); gate signal profiling; arbitrary gate impedance; multi-level driver; series-connected drivers

I. INTRODUCTION

Active gate driving adjusts a power device's switching waveforms during the switching transient by shaping the gate voltage signal, as opposed to conventional gate drives that apply a voltage step-function to the gate via a fixed resistance. Active gate driving has been demonstrated with all types of MOS-gated silicon devices, usually with the intention of controlling di/dt and dv/dt [1], for example to allow dynamic voltage sharing of seriesed devices [2], and to reduce voltage overshoots [3] or combat EMI [1], [4]-[7]. It has been shown that by applying carefully shaped waveforms to the gate of silicon IGBTs, EMI is reduced without increasing switching loss [5]. In [6], the gate driver is an analogue amplifier with feedback, controlling high-power IGBTs, and in [7] a gate driver consisting of 8 digitally enabled parallel output stages reduces EMI in a power MOSFET circuit.

With the move to faster-switching wide-bandgap power devices, faster active gate drivers are required. An integrated high-speed active gate driver with a time-resolution of 150 ps has been shown to allow the shaping of switching transients that are just a few ns long. This can enhance switching waveforms in GaN-based converters without increasing circuit losses [8]-[10]. However, the high speed has come at the expense of a low 5 V maximum output voltage, due to the need to use fast low-voltage transistors in the design. Therefore new solutions are needed if

high-speed active gate driving is to meet the trend to higher gate voltages, and also for use with SiC MOSFETs that require a gate-source voltage of 15 V to be fully enhanced.

The principle aim of this paper is to show that a multi-level approach, illustrated in Fig. 1, enables both active high-speed driving and increased driver output voltage range. The approach presented uses a series topology of multiple discrete drivers, to provide an experimental platform for the investigation of high-speed active gate driving of SiC devices; in the future the topology could be integrated into a single driver for practical system implementation.

In Section II, the multi-level driver topology is introduced. It is shown how connecting two “assist” gate drivers in series with the active driver enables sub-ns resolution active gate driving whilst also allowing the gate of the driven device to be raised to 15 V, and held to a negative voltage in the off state, as illustrated in Fig. 1.

In Section III, detailed circuit operation is described and critical current loops identified. The hardware implementation is presented, showing the role of careful PCB layout and driver selection in keeping the inductance of the critical loops to a minimum. Functional operation of the proposed circuit, driving the gate of a 900-V SiC MOSFET, is demonstrated in Section IV showing that this is a viable platform for the investigation of high-resolution active gate driving of SiC MOSFETs. The capability of the proposed gate drive arrangement is compared to previously published work. Conclusions are drawn in Section V.

II. MULTI-LEVEL ACTIVE GATE DRIVE TOPOLOGY FOR SiC MOSFETs

Fig. 2 illustrates the third-generation programmable active gate driver used in this work. It is a refinement of the driver

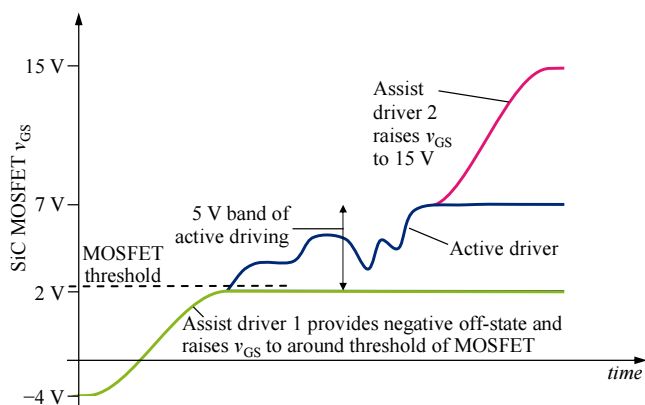


Fig. 1 Multi-level gate driving with high-resolution active driving around the gate threshold voltage.

detailed in [8]. Fabricated in AMS HVCMOS 180 nm technology, it integrates high-speed memory, a 400 MHz to 700 MHz voltage-controlled oscillator (VCO), hybrid synchronous and asynchronous control logic, and a dynamically-adjustable 120 mΩ to 64 Ω output stage, in a QFN32 package. The output stage consists of two parallel-connected drivers: a “main” driver that operates synchronously, with 2^8 resistance levels; and a “fine” driver that operates asynchronously, with 2^6 resistance levels. Once the memory is programmed, the gate driver operates autonomously. On each PWM edge, a gate-drive sequence of 8 internal clock cycles duration (11.4 ns to 20 ns) is read from memory by the control logic, and appropriate control signals are applied to the output stages. The setting in the 8th clock period is maintained until the next PWM transition, and there are independent resistance sequences for low-high and high-low transitions.

For the “main” driver, the sequence defines one pull-up (for PWM low-high transition) or pull-down (for PWM high-low transition) resistance value per clock cycle. During each clock cycle, further adjustments of the driver’s output resistance can be made using the “fine” driver, with a timing resolution of 100 ps. The fine driver can pull up or down regardless of the state of the PWM, so can pull in opposition to the main driver, if required.

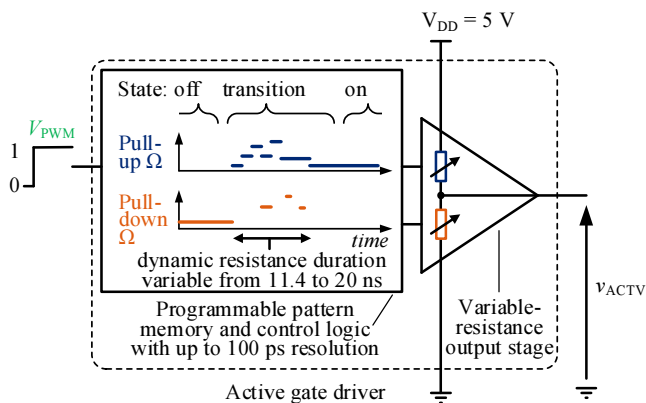


Fig. 2 Conceptual overview of the third-generation high-speed active gate driver used in this work.

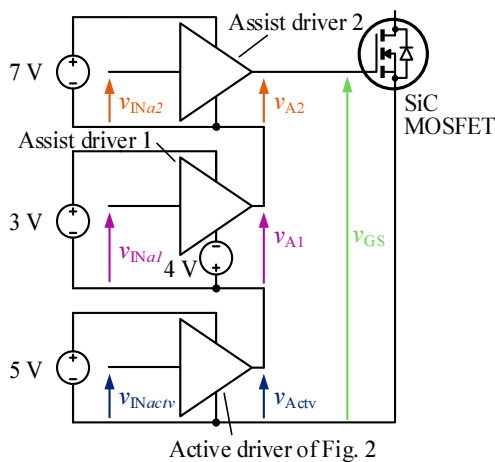


Fig. 3a Gate-drive topology combining active gate driver and conventional (“assist”) gate drivers in series

Normally, the active gate driver would be connected directly to the source and gate terminals of a power device. However, the driver operates from a maximum 5 V supply so cannot fully enhance a SiC MOSFET that requires 15 V gate-source for minimum $R_{ds(on)}$, such as the 900-V, 65-mΩ C3M0065090J¹ [11]. Nor can it provide a negative-off state bias. To circumvent these limitations, conventional gate drivers (referred to hereafter as “assist” drivers), powered from floating supplies, are inserted in series between the active driver’s output and the MOSFET gate. The output voltages of the assist drivers then add to that of the active gate driver. Fig. 3a shows a simplified schematic of the proposed driver, containing three series-connected sub-drivers, and Fig. 3b shows some idealised waveforms demonstrating the basic idea of operation.

Referring to Fig. 3, in time period t_0 to t_1 , the input demands (v_{INa1} , v_{INa2} , and v_{INactv}) are logic-low and their outputs (v_{A1} , v_{A2} , v_{Actv}) held low. The output of the active gate driver is therefore connected to the gate of the SiC MOSFET via the low resistance of the assist drivers’ pull-down transistors operating in the ohmic region, in series with the 4 V bias supply in the negative rail of assist driver 1. The MOSFET gate is therefore driven to 4 V below its source and it is off. From t_1 to t_2 , v_{INa1} transitions to logic high and the first assist driver raises the gate potential to around the threshold region of the SiC MOSFET. From t_2 to t_3 , v_{INactv} transitions to logic high, lifting the floating grounds of assist drivers 1 and 2 so the gate potential of the SiC MOSFET is increased by a further 5 V, with the active driver able to shape its output voltage during this switching transition. From t_3 to t_4 , v_{INa2} goes high and the second assist gate driver’s output transitions to pull up, resulting in an overall gate-source voltage of 15 V. The turn-off transient follows a similar pattern in reverse order, from t_5 to t_8 . The duration of t_1 to t_4 would typically be in the region of 30 to 60 ns. It is assumed here that the propagation delay from demand to output of the drivers is similar. If this is not the case, it may easily be accounted for by altering the time alignment between v_{INa1} , v_{INa2} , and v_{INactv} .

The relative activation timing of the three gate drivers provides additional variables in the gate voltage profiling process. Although the idealised waveforms of Fig. 3b show the

¹ Note that this is a third-generation device with $R_{ds(on)}$ specified at 15 V V_{GS} rather than 20 V V_{GS} of earlier-generation devices.

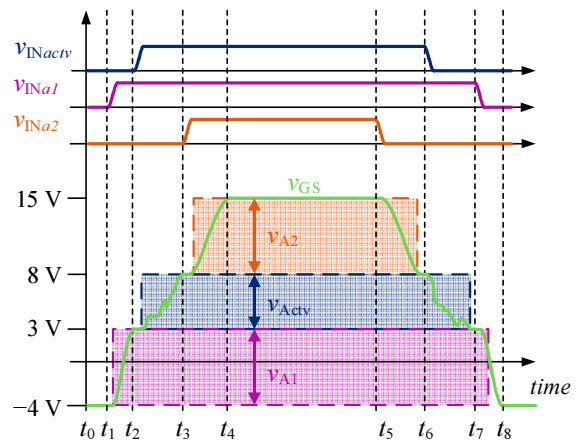


Fig. 3b Idealised waveforms demonstrating the multi-level series operation of active and assist drivers.

drivers activating and deactivating in sequence, it would be possible to activate and deactivate any combination of drivers simultaneously or closely together, to overlap their output transients. However, activating an assist driver simultaneously with the active driver can limit the ability of the active driver to shape the resulting gate transient, which will be discussed later.

When the drivers are activated in sequence, this gives a 5 V band during the gate switching transition within which shaping can occur (labelled v_{Actv} in Fig. 3b). To allow maximum flexibility, the value of the assist drivers' power supplies is made variable. If assist driver 1's positive power supply value is reduced, this lowers the gate voltage at which shaping can commence. Assist driver 2's power supply value must then also be changed in order to maintain a 15 V steady-state value when all drivers are on.

III. HARDWARE IMPLEMENTATION

A. Device selection and PCB layout for minimisation of parasitic inductance

In order not to diminish the shaping capability of the active driver, the total parasitic impedance of the gate drive loops in all switching scenarios should be minimised. As such, the assist gate drivers should have low-resistance FET (not bipolar) output stages to allow bi-directional current flow in both pull-up and pull-down states.

To inform the selection of appropriate assist drivers and physical layout of the circuit on PCB, the critical gate-drive current loops for each scenario are identified in Fig. 4 and Fig. 5. During switching transients, some SiC MOSFET gate current will flow via C_{GS} (gate-source capacitance), and some will flow via C_{GD} (gate-drain capacitance). The portion of the gate current that flows through C_{GD} will return to the gate-drive loop via the power circuit. Referring to Fig. 4 and Fig. 5, the current flow paths are illustrated in sequence: Fig. 4(a), then (b), then (c) for turn-on, and Fig. 5(a), then (b), then (c) for turn-off. If all drivers are activated or deactivated simultaneously, the current adopts the paths of subfigures (c). The assist driver packages should be small, preferably with power supply and output pins all arranged along one edge, as this should most easily facilitate minimisation of the current-loop area and hence its parasitic inductance. The driver selected is the MAX15024A [12]. This is available in a 3 mm × 3 mm QFN package, with specified typical pull up and pull down resistances of 0.875 Ω and 0.45 Ω respectively.

The supply bypass of all drivers should have high capacitance with low ESR to minimise overall transient impedance. Ceramic capacitors are ideal here. Supply bypass for the active driver and assist driver 2 both consist of a vertical stack of two parallel-connected X5R capacitors in 0603 (imperial) packages, each with nominal capacitance of 4.7 μF (2.6 μF @ 5 V and 1.6 μF @ 8 V) [13]. For assist driver 1, a vertical stack of six parallel-connected X5R capacitors in 0402 packages, each with nominal capacitance of 2.2 μF (540 nF @ 5 V) [14] is used. Note that current only flows in the negative bias supply of assist driver 1 when that driver pulls down, at the end of a MOSFET turn-off transition where shaping will not be required. The layout can therefore prioritise the reduction of the assist 1 positive supply parasitic inductance.

The PCB layout of the gate-drive circuit is shown in Fig. 6. The board has total thickness of 0.8 mm and four copper layers, with current paths carefully routed so that current flows in opposite directions on adjacent layers. The supply bypass capacitors are placed on the underside of the board, connected by vias to their respective driver supply pins. The floating supplies of the assist drivers are provided by standard diode-capacitor bootstrap arrangements, with assist driver 1's negative supply generated by an inverting charge-pump IC. The control signals for the assist drivers are transferred from ground-referenced to floating-ground-referenced with a digital isolator IC.

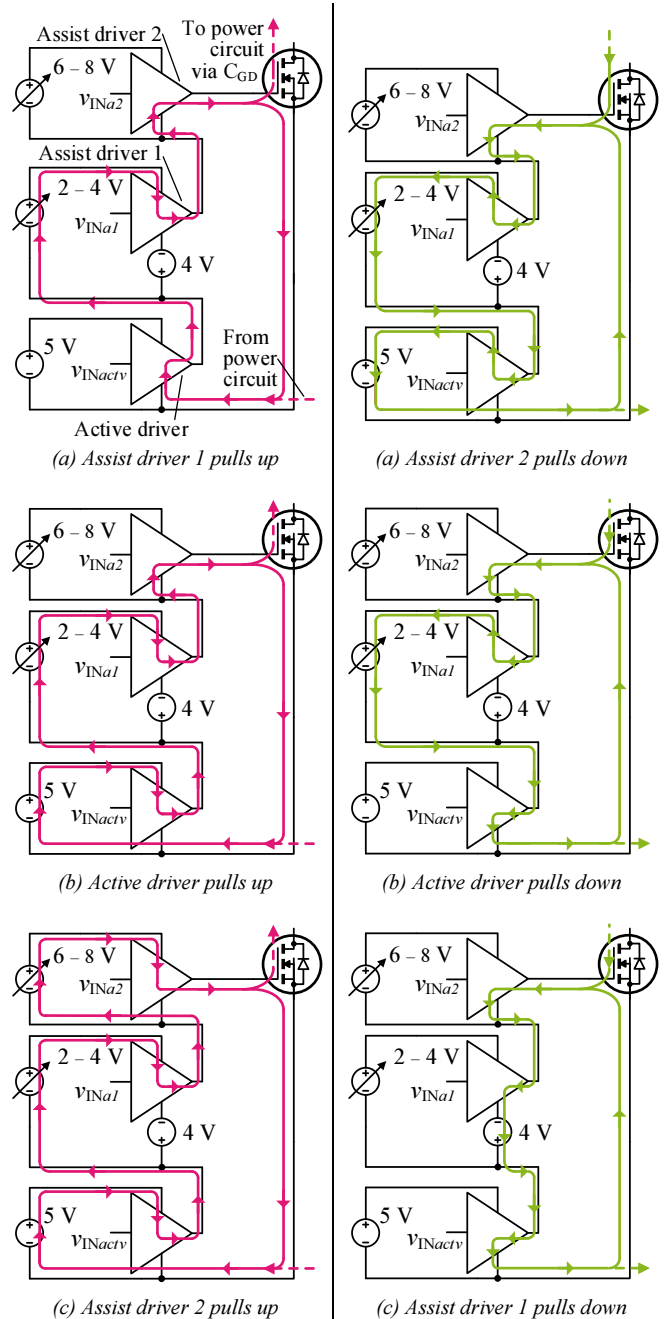


Fig. 4 Gate-drive current loops for SiC MOSFET turn-on

Fig. 5 Gate-drive current loops for SiC MOSFET turn-off

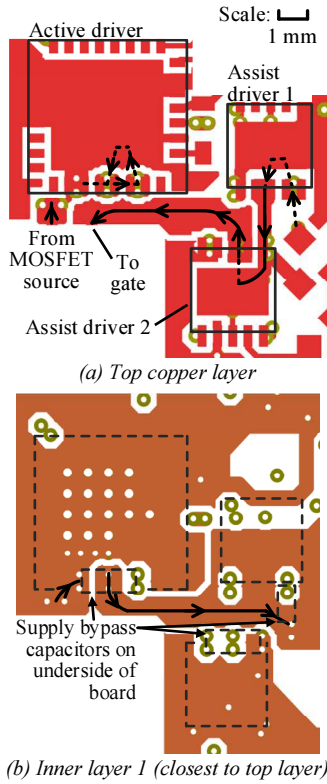


Fig. 6 PCB layout of gate driver. Both layers are top-views. The current pathway for active driver turn-on of Fig. 4(b) is indicated on each layer, with the dashed portions indicating current flow in components such as drivers and bypass capacitors.

B. Limitations during simultaneous slewing

Referring to Fig. 4 (c), this is the path that gate current will follow once the drivers have been activated in sequence, and the final driver is activated. It is also the path that the gate drive current may be expected to follow if all drivers are activated simultaneously. Under this scenario, it may be desirable to alter the active driver's output impedance to influence the gate voltage transient, for example by using a higher impedance to slow it down.

However, under this condition, the assist drivers' output slew rates are uncontrolled and current in the gate-drive loop can be forced through the active driver's internal capacitances (output stage bypass or parasitic capacitances), rather than via the external bypass network, as illustrated in Fig. 7. From LTSpice simulations, the path taken by the current depends on the active driver's output stage impedance setting. If the impedance is set

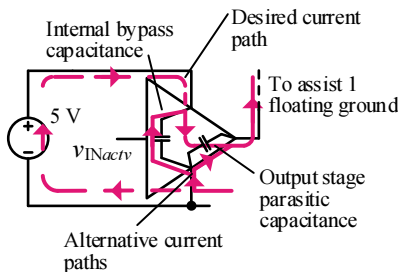


Fig. 7 Schematic showing alternative current pathways via the active driver's internal capacitances.

high, most current passes through the parasitic capacitance. If the impedance is set low, current passes through the external and internal bypass network. If the current in the internal bypass is large, the local supply voltage of the active driver dips significantly below 5 V. Therefore, there is a complicated relationship between the active driver impedance setting, assist driver slew rates, current pathway, and the resulting v_{GS} signal. Ultimately, the relationship between the driver pattern and the MOSFET's v_{GS} is not as might be expected.

Whilst shaping during simultaneous driver turn-on is therefore difficult, some shaping can be achieved with a small overlap between the end of assist 1's transient, which has a low slew rate, and the start of the active driver's transient.

C. The need for multiple levels

The need for the first assist driver is illustrated using a two-level version of the proposed topology, with an active gate driver operating from a 5 V supply and one assist driver operating from a 10 V supply. This is applied to a SiC MOSFET switching 300 V and 2.5 A. The activation timings of the two drivers are set far apart in order to observe the behaviour of the SiC MOSFET during the first 5 V of the gate transient. The resulting MOSFET v_{DS} transition is shown in Fig. 8. It can be seen that during the active driving phase, from $t = 10$ ns to 20 ns, the MOSFET's v_{DS} changes very little. v_{DS} then proceeds to fall slowly, until rapidly falling the remaining 70 V once the assist driver activates. The switching voltage and current are set to low values here in order to limit the switching loss in the MOSFET. This result suggests that effective active gate driving of this device requires v_{GS} shaping from around the V_{TH} point (specified as 1.8 V min; 2.1 V typ; 3.5 V max at room temperature, with a negative temperature coefficient) up to around 8 V.

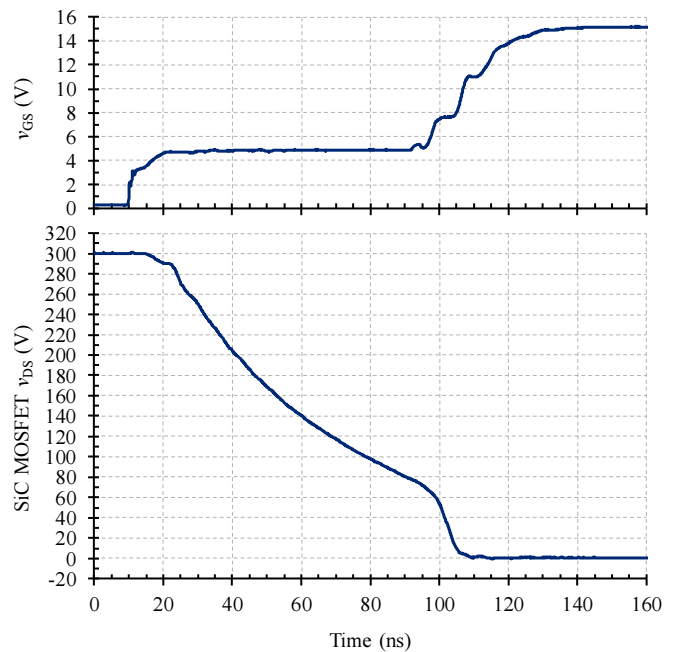


Fig. 8 Measured SiC MOSFET v_{GS} and v_{DS} waveforms with a two-level driver, where the assist driver is activated approximately 80 ns after the active driver. The MOSFET is switching approximately 2.5 A.

Combined with the limitations of the multi-level series topology when drivers are activated simultaneously, this necessitates the use of the three-level driver.

IV. TESTING PROCEDURE AND EXPERIMENTAL RESULTS

A. Test setup

The proposed gate drive topology has been used in an open-loop, non-synchronous boost converter operating with an output of 600 V and an input supply of 60 V and 5 A. A simplified schematic is shown in Fig. 9, with a photograph of the constructed converter in Fig. 10. The circuit is operated with a 100 kHz MOSFET switching frequency, with the on/off control signals for the gate drivers supplied by an external bench-top function generator and edge-delaying circuit. A variable resistance load determines the output power and consequently the input current. The switch-node and output voltages, v_{sw} and v_{out} , are measured with 400-MHz 100:1 passive probes. The v_{sw} probe is connected to the board with a PCB-mounted coaxial connector and the v_{out} probe with a low-inductance grounding clip. MOSFET v_{GS} is measured with a 2-GHz bandwidth Rhode & Schwarz RT-ZD30 active differential probe with RT-ZA15 attenuator.

B. High-resolution shaping of gate voltage

Firstly, to demonstrate the functionality of the multi-level gate drive, the circuit is operated with the power circuit inactive (V_{IN} open-circuit), and an arbitrary impedance sequence is programmed into the active driver for its turn-on transition. The driver sequence and resulting measured MOSFET v_{GS} are shown in Fig. 11.

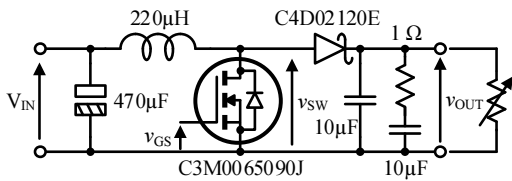


Fig. 9 Simplified schematic of boost converter, v_{GS} is provided by the multi-level gate driver.

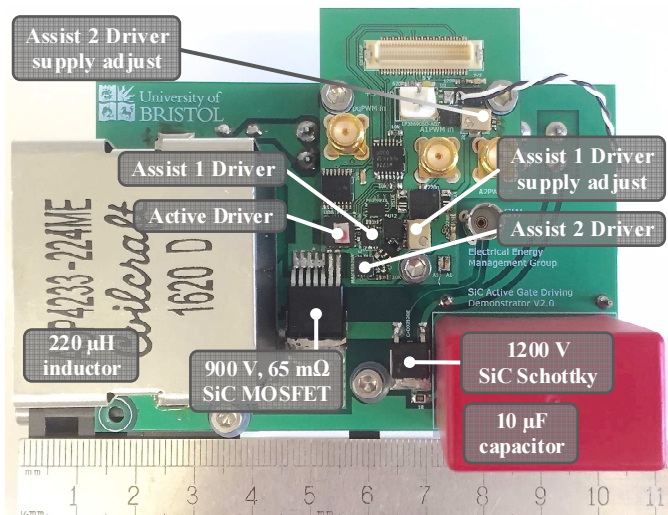


Fig. 10 600 V SiC boost converter, and multi-level driver.

C. Shaping of the power waveforms

Next, the converter is operated at full output power, with the SiC MOSFET switching 600 V and 5 A, under two different gate-drive scenarios: one where the active gate driver is set to a constant drive strength during its transition, and another where the active driver's output impedance varies during its transition. The results are shown in Fig. 12. Under the active driving scenario, disturbances seen at the output node during the switching transition are reduced by 30%, with a negligible change in measured circuit losses.

D. Comparison to existing active gate drivers

Compared to previously-published work, this SiC active driver arrangement has a higher time resolution and number of drive levels, at the expense of higher complexity and a limited voltage range over which shaping can occur. [15] and [16] present integrated active SiC gate drivers with wide output voltage ranges; however, they are significantly slower. The driver in [15] changes impedance from one switching event to the next, as opposed to during individual switching events. The driver in [16] has a similar architecture to the active driver used here, but operates at an order-of-magnitude lower internal clock frequency (25 MHz), and is more suited to slower higher-power circuits. It is demonstrated simultaneously improving switching waveforms and reducing losses in a 15-A converter switching 500 V in about 100 ns. The 5-A power circuit presented here switches 550 V in approximately 13 ns as shown in Fig. 12. In order to exert influence over such switching transitions, an

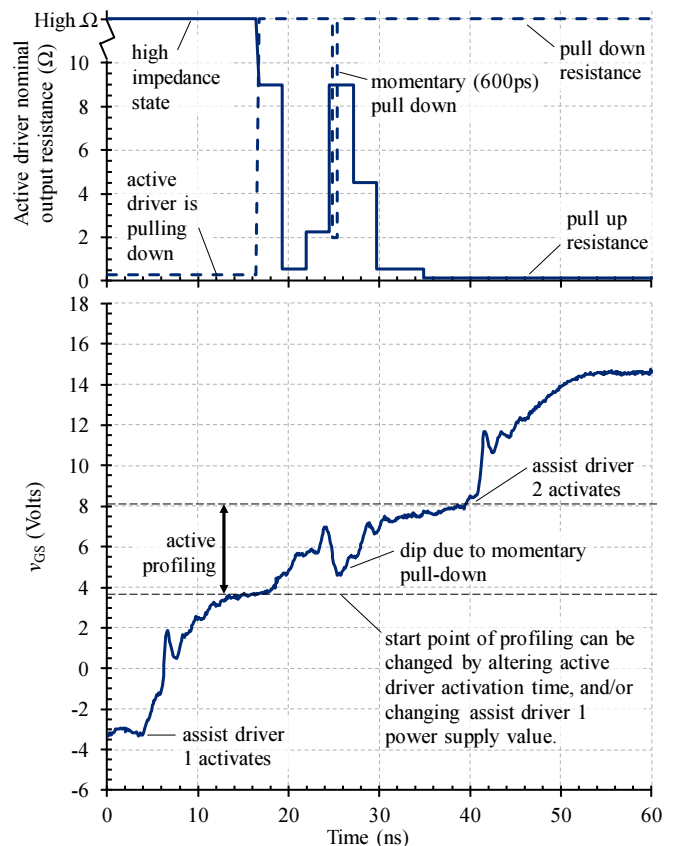


Fig. 11 Measured MOSFET v_{GS} , with V_{IN} open circuit. The top graph shows the arbitrary sequence of nominal resistance values used by the active driver during its transition.

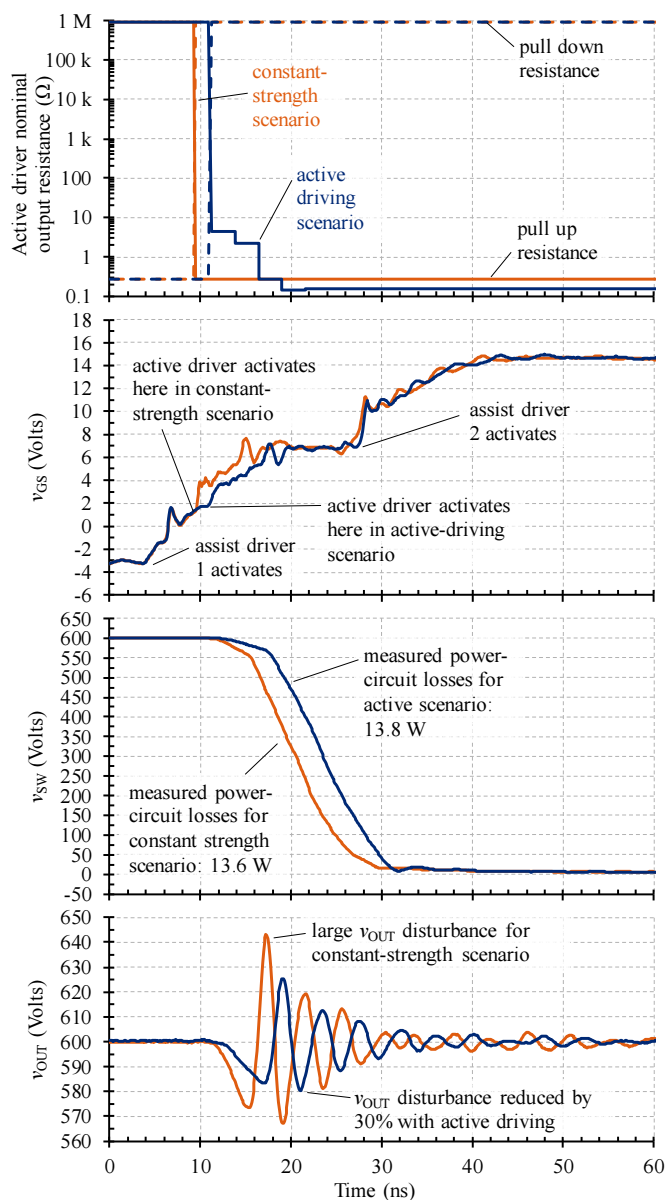


Fig. 12 Measured MOSFET v_{GS} , v_{SW} , and v_{OUT} for two different gate drive scenarios: one without shaping, and one with shaping. The top graph shows the sequence of nominal resistance values used by the active driver during its transition.

active gate driver must be able to shape its output with commensurate speed.

V. CONCLUSIONS AND FURTHER WORK

High-speed active gate driving of a SiC MOSFET has been achieved by breaking down the gate profile into three phases. An active 100 ps resolution shaping phase with 5 V active voltage range is placed around the gate voltage threshold. This is flanked by two voltage-level-shifting phases, where shaping is not necessary, in order to achieve a negative holdoff, and a high on-state gate voltage. Whilst in real applications it would not be desirable to use multiple discrete drivers, each with their own floating power rail, the intention has been to explore the feasibility of multi-level driving prior to integration into a single driver. In the present implementation, total gate-drive loop

inductance requires careful minimisation in order not to limit controllability during the active phase. Experimental results show that the active driver retains sufficient control to substantially shape the gate-source voltage of the SiC device. This opens up the possibility of 100 ps resolution active gate driving of SiC devices that require a -4 V to $+20$ V gate voltage range, eliminating the need to trade off time resolution to achieve these higher gate voltage ranges.

REFERENCES

- [1] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT Gate Driver," *IEEE Trans. Power Electronics*, vol. 30, no. 6, pp. 3402-3417, Jun. 2015.
- [2] P. R. Palmer and A. N. Githiari, "The series Connection of IGBTs with Active Voltage Sharing," *IEEE Trans. Power Electronics*, vol. 12, no. 4, pp. 637-644, Jul. 1997.
- [3] H. Riazmontazer and S. K. Mazumder, "Dynamic Optical Turn-Off Control of a High-Voltage SiC MOSFET," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 1274-1278.
- [4] N. F. Oswald, P. Anthony, and J. N. McNeill, B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," *IEEE Trans. Power Electronics*, vol. 29, no. 5, pp. 2393-2407, May 2014.
- [5] N. Oswald, B.H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of Shaped Pulse Transitions in Power Electronic Switching Waveforms for Reduced EMI Generation," *IEEE Trans. Industry Applications*, vol. 47, no. 5, pp. 2154-2165, Sept.-Oct. 2011.
- [6] X. Yang, Y. Yuan and P. R. Palmer, "Shaping High-Power IGBT Switching Transitions by Active Voltage Control for Reduced EMI Generation," *IEEE Trans. Industry Applications*, vol. 51, no. 2, pp. 1669-1677, Mar.-Apr. 2015.
- [7] W. T. Ng, et al., "Efficiency enhancement and EMI suppression via dynamically adjustable gate driving strength," in *Proc. IEEE 54th International Midwest Symp. on Circuits and Systems*, 2011, pp. 1-4.
- [8] H. C. P. Dymond et al., "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. Power Electronics*, vol. PP, no. 99, in press.
- [9] H.C.P. Dymond et al., "Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns," in *Proc. IEEE Energy Conversion Congress & Exposition (ECCE)*, Milwaukee, September 18-22, 2016.
- [10] J. J. O. Dalton et al., "Shaping switching waveforms in a 650 V GaN FET bridge-leg using a 6.7 GHz active gate driver," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, March 26-30, 2017.
- [11] Wolfspeed, "C3M0065090J data sheet," [Online] available: <http://www.wolfspeed.com/media/downloads/145/C3M0065090J.pdf>
- [12] Maxim Integrated, "MAX15024/MAX15025 Single/Dual, 16ns, High Sink/Source Current Gate Drivers Data Sheet," [Online] available: <https://datasheets.maximintegrated.com/en/ds/MAX15024-MAX15025.pdf>
- [13] TDK, "C1608X5R1E475K080AC specifications," [Online] available: https://product.tdk.com/en/search/capacitor/ceramic/mlcc/info?part_no=C1608X5R1E475K080AC
- [14] TDK, "C1005X5R1C225K050BC specifications," [Online] available: https://product.tdk.com/en/search/capacitor/ceramic/mlcc/info?part_no=C1005X5R1C225K050BC
- [15] R. Grezaud, N. Rouger and J-C. Crebier, "An Adaptive Output Impedance Gate Drive for Safer and More Efficient Control of Wide Bandgap Devices," *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, Columbus, OH, 2013, pp. 68-71.
- [16] K. Miyazaki et al., "General-purpose clocked gate driver (CGD) IC with programmable 63-level drivability to reduce Ic overshoot and switching loss of various power transistors," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1640-1644