Anisotropic magnetoconductance and Coulomb blockade in defect engineered Cr₂Ge₂Te₆ van der Waals heterostructures

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We demonstrate anisotropic tunnel magnetoconductance by controllably engineering charging islands in the layered semiconducting ferromagnet $Cr_2Ge_2Te_6$. This is achieved by assembling vertical van der Waals heterostructures comprised of graphene electrodes separated by crystals of $Cr_2Ge_2Te_6$. Carefully applying vertical electric fields in the region of ($E \sim 25-50 \text{ mV/nm}$) across the $Cr_2Ge_2Te_6$ causes its dielectric breakdown at cryogenic temperatures. This breakdown process has the effect of introducing subgap defect states within the otherwise semiconducting ferromagnetic material. Low-temperature electron transport through charging islands reveals Coulomb blockade behavior with a strongly gate-tuneable anisotropic magnetoconductance, which persists up to $T \sim 60 \text{ K}$. We report average tunnel magnetoresistance values of 100%. This work opens new avenues and material systems for the development of nanometer-scale electrically controlled spintronic devices.

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I. INTRODUCTION

Spintronic devices based on the electrical control of magnetism have attracted considerable attention because of the potential for new miniaturized devices suitable for novel nonvolatile memory and logic elements [1-4]. Recently, twodimensional (2D) ferromagnets such as CrI₃ [5,6], CrBr₃ [7], Fe_3GeTe_2 [8], and $Cr_2Ge_2Te_6$ [9] have been isolated, and they show significant promise for new applications. Curie temperatures have been shown to vary from T = 30 K to in excess of room temperature with magnetic ordering found to depend on both layer number as well as applied electric fields [10–14], which could offer new functionalities. To date, several van der Waals (vdW) spintronic heterostructure devices have been realized, including spin filters [8], magnetoresistance devices [6], and valley polarized light sources [15]. The multitude of different material combinations and simplicity in which various 2D materials can be assembled into heterostructures makes 2D van der Waals magnetic materials promising candidates for future technologies [16-18]. The field of nano spintronics is an equally exciting area, where the ability to manipulate single spins offers new opportunities for quantum computing applications [19-22].

In this work, we show that magnetic charging islands can be introduced into the ferromagnetic semiconductor $Cr_2Ge_2Te_6$ and that the low-temperature electron transport is best described by Coulomb blockade through a network of charging islands. We achieve this by assembling vertical heterostructures comprised of graphene electrodes separating crystals of $Cr_2Ge_2Te_6$ (CGT) and controllably introducing defects through a dielectric breakdown process. The temperature dependence of the conductivity after the breakdown process reveals a variable hopping mechanism. In certain temperature regimes, the transport is best described by hopping conduction in the presence of Coulomb interactions or Efrös-Shklovskii variable range hopping (ES-VRH [23]). However, large oscillations of the conductance with gate voltage are observed at low temperature (T = 4.2 K), which we attribute to Coulomb blockade. Furthermore, the magnetoconductance displays a large anisotropy with magnetic field, which is also highly sensitive to external gate voltages.

II. RESULTS AND DISCUSSION

We focus on heterostructures based on the semiconducting ferromagnet CGT [24]. This material is a *p*-type semiconductor [10,25] with an indirect band gap of $E_g \sim 0.7$ –0.8 eV [26] in bulk and a Curie temperature of $T \sim 65$ K [24]. Our heterostructure devices are produced by micromechanical exfoliation of individual bulk crystals and subsequent assembly into vdW heterostructures by standard dry-transfer methods in ambient conditions [27]. Figure 1(a) shows the electron transport behavior for a typical planar field-effect transistor based on a CGT crystal. We observe a reduction in the channel resistance with increasing negative gate voltage, consistent with *p*-type conduction, with a small level of hysteresis as a function of the gate voltage attributed to substrate impurities. The temperature dependence of the channel resistance for five planar devices is shown in Fig. 1(b). We find that the temperature dependence of the resistance in the high-temperature regime is well fit by the Arrhenius relation, $R(T) = R_0 \exp(\Delta E/T)$. From this, we are able to extract an energy gap of $\Delta E \sim$ 0.2 eV, which does not depend on the flake thicknesses, ranging from 10 to 100 nm. The structure of the material is confirmed by performing Raman spectroscopy as shown in Fig. 1(c) for a multilayer flake exfoliated and left in ambient conditions for several hours. The most prominent peaks are the E_g^2 mode located at 111 cm⁻¹ and the A_g^1 mode appearing

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FIG. 1. Initial material characterization. (a) Four-probe in-plane field effect of the resistance. Inset: schematic of the device structure and circuit. (b) Temperature dependence for five separate flakes with a typical Hall bar device shown in the inset. (c) Raman spectrum for a multilayer exfoliated flake. (d) Schematic of the device architecture studied in this work. (e) Temperature dependence of the *c*-axis conductivity. Inset: optical micrograph of one of our heterostructure devices (black outline, graphene electrodes; red outline, CGT crystal; and the green flake is the hBN substrate). (f) Left panel: Contour map of the differential conductance for different V_{dc} and back-gate voltage V_g . Right panel: differential conductance plotted for $V_g = +80$ and -80 V (measured at T = 4.2 K).

at 136.5 cm⁻¹, with narrow linewidths of \sim 1–2 cm⁻¹, which have previously been used as a measure of crystal quality [28]. We note that flakes that are one and two layers thick are highly unstable in ambient conditions and fully oxidize after several hours. However, thicker flakes >10 nm do not degrade rapidly and can be processed via standard microfabrication procedures. We attribute this to surface layer oxidation which protects and slows the subsequent oxidation of the bulk crystal; however, further structural studies are needed to confirm this. For comparison, we have also included in the supplementary materials the low-temperature back-gate and bias dependence vertical conductance for a device fabricated in inert conditions [29]. We find the transport properties to be similar to our devices fabricated in ambient conditions. This indicates that the oxidized surface layer of CGT does not effect the vertical transport properties significantly. The vertical heterostructure device that we focus on in this work is schematically illustrated in Fig. 1(d). This device consists of graphene electrodes separating a 40-nm-thick CGT crystal, confirmed by atomic-force microscopy (AFM); see the supplemental material [29]. Figure 1(e) shows the zero-bias and zero B-field cooled temperature dependence of the outof-plane differential conductance. The temperature dependence again follows well the Arrhenius relation with an energy gap of $\Delta E \sim 0.18$ eV, comparable to values observed in our planar devices and similar to values reported previously [24]. Figure 1(f) shows the low-temperature (T = 4.2 K) back-gate and source-drain bias dependence on the differential conductance between the top and bottom graphene electrodes for the device shown in the inset of Fig. 1(e). For small applied dc bias voltage, the recorded differential conductance indicates a vertical resistance $\sim 10^{10} \Omega$. As the gate voltage is increased to larger negative voltages, the conductance increases as expected for a *p*-type semiconductor as the valence band becomes populated.

Similarly, an increase of V_{dc} leads to an exponential increase of the conductance, which occurs at $V_{dc} \sim 0.75$ V. This sharp increase is attributed to the point where the quasi-Fermi levels of the graphene electrodes reach the band edges of the CGT. As V_{dc} is increased further, we find the conductance becomes unstable when measured at low temperature (T = 4.2 K). Figure 2(a) illustrates this showing a set of $|I_{sd}| - V_{sd}$ curves for increasing bias voltage and source-meter current compliance limits (bottom panel to top panel). The measurements are conducted from negative to positive bias voltage (blue curve) followed by a positive to negative sweep (red curve). As the bias voltage is increased above $V_{sd} = 2$ V and current compliance above 1 μ A (junction area ~25 μ m²), the $|I_{sd}| - V_{sd}$ curves become nonreversible [Fig. 2(a), third and fourth sweep]. This indicates a structural transformation



FIG. 2. Controllably creating defects. (a) $|I_{sd}| - V_{sd}$ sweeps with subsequently increasing bias voltage and compliance current; arrows indicate the sweep direction. Note: after the fourth sweep, the original $|I_{sd}| - V_{sd}$ curve is not recovered. (b) Zero-field applied temperature dependence of the vertical electron transport measured at $V_g = 0$ V. Inset: gate dependence of the differential conductance for before defect engineering (blue) and after (red). (c) Zero-field temperature and back-gate dependence of the Coulomb oscillations from T = 4.2 K (blue) to T = 25 K (red). (d) Contour plot of the differential conductance for bias and back-gate voltage measured at T = 4.2 K.

likely caused by the breaking of chemical bonds as a result of the applied electric field. The increase of the conductivity is therefore attributed to an increased density of subgap states. Figure 2(b) shows the zero bias and zero-field-cooled temperature dependence of the conductance after the breakdown process. We find that the dependence of the conductivity with temperature is transformed with an extracted energy gap of \sim 30 meV, a reduction of six times compared to the pristine material. In this instance, the extracted energy gap is known as the activation energy associated with hopping conduction, which is often observed in disordered semiconductor materials. To determine the type of conduction mechanism, we study the best fit for the exponent *n* in the following relation: $\sigma = \sigma_0 \exp(-T_0/T)^n$. We find a best fit for n = 1/4 for the temperature range T = 40-250 K, which is expected for Mott variable range hopping [23,30]. However, in the temperature range between T = 40 and 25 K a transition to (n =1/2) is observed that is the expected exponent for hopping conduction in the presence of Coulomb interactions, better known as Efrös-Shklovskii variable range hopping [23]. This conduction mechanism is characterized by the relation $\sigma =$ $\sigma_0 \exp(-T_0/T)^{1/2}$, where $T_0 = (2.8e^2)/(4\pi\epsilon_0\epsilon_r K_B\xi)$. Here, ϵ_r is the relative permittivity of the material, ξ is the localization radius, and e, ϵ_0 , and K_B are the electron charge, permittivity of free space, and the Boltzmann constant, respectively. Below T = 20 K, the temperature dependence deviates from the hopping conduction relation. This is because the system enters the Coulomb blockade regime, where $K_BT < E_C$; here E_C is the charging energy. In this regime, the temperature dependence of the conductance will strongly depend on the alignment on the Fermi level in the bottom graphene electrode relative to the energy levels in the charging islands [31].

Figure 2(b) shows the natural log of the conductivity plotted versus $T^{-1/2}$ (blue curve) consistent with ES-VRH. T_0 is then extracted from a linear fit, which we find to be $T_0 = 111$ K. It should be noted that a modified form of ES-VRH would be relevant here that takes into account the orientation of the magnetization of neighboring islands [32] if the sample were magnetized. However, as the sample is cooled from the paramagnetic state with zero applied magnetic field, the average orientation of the magnetic islands would equate to zero, allowing for the use of the general expression. To extract the localization radius, it is necessary to ascertain the low-temperature relative permittivity ϵ_r of the CGT. This is achieved by employing the CGT as a gating dielectric at T = 4.2 K in a dual gated graphene field-effect transistor where we are able to extract the back-gate dependence of the CGT capacitance. Combining this with the CGT thickness determined from AFM data allows us to make an estimate of ϵ_r for CGT; see supplementary Fig. S1 [29]. We find that the value of ϵ_r varies from 16 at $-80 > V_g > -30$ V to 4 at $-30 < V_g < -20$ V. We attribute the large variation of ϵ_r with gate voltage to the change of doping in the CGT crystal with applied gate voltage. Using these values for ϵ_r , we are then able to extract localization radii in the range of $\xi = 27 - 105$ nm, which indicates that only a few charging islands are responsible for the conduction mechanism through the defect engineered CGT crystal.

We find that the low-temperature (T = 4.2 K) gate dependence of the zero-bias conductance has been dramatically transformed after the breakdown process, with sharp oscillatory peaks appearing [inset Fig. 2(b)]. The peaks are associated with Coulomb blockade due to the strong Coulomb repulsion between neighboring charging islands,



FIG. 3. In-plane magnetoresistance behavior of the Coulomb oscillations. (a) Contour map of the conductance for different gate voltages and magnetic fields with the magnetic field swept from B = +2 to -2 T. (b) Contour map of the conductance for different gate voltages and magnetic fields with the magnetic field swept from B = -2 to +2 T. (c) Coulomb diamonds measured at different magnetic fields upon sweeping back from B = 2 to -2 T. (d) Temperature dependence of the anisotropic magnetoresistance recorded at $V_g = -50$ V; the arrows indicate magnetic-field sweep directions.

which is seen at temperatures less than the charging energy E_C .

One way to estimate the charging energy is through the temperature dependence of the oscillations. Figure 2(c) shows the temperature dependence of the Coulomb oscillations from T = 4.2 to 25 K. We observe that the oscillations disappear at ~ 25 K, which gives an associated charging energy of $E_C = K_B T = 2.2$ meV. Alternatively, the charging energy can be estimated through mapping the differential conductance for different back-gate and bias voltages. Figure 2(d) shows a contour map of the differential conductance versus back gate and dc bias voltage (V_{dc}) at T = 4.2 K. We observe typical Coulomb blockade features associated with transport through a multi-island system. This is characterized by a sequence of diamondlike features appearing in the contour maps shown in Fig. 2(d). The diamondlike features occur when the Fermi level of the bottom graphene electrode (adjusted with the back-gate voltage) passes the energy levels in the charging islands, leading to peaks in the differential

conductance. Similarly, the maximum value of V_{dc} at which the differential conductance increases exponentially [the first white color scale in Fig. 2(d)] gives the charging energy E_C of the smallest island. By analyzing the data in Fig. 2(d), we extract an average value of $E_C \sim 3$ meV over the entire gate voltage range. We note that this value is comparable to the value determined from the temperature dependence seen in Fig. 2(c).

Furthermore, if we assume that the charging island is spherical, then the charging energy $E_C \sim 3$ meV is related to the diameter of the island by the following equation: $E_C = e^2/4\pi\epsilon_0\epsilon_r d$, where ϵ_r is the relative permittivity of the surrounding environment, *d* is the charging island diameter, and *e* and ϵ_0 are the electron charge and permittivity of free space, respectively. Using a value of $\epsilon_r = 16$ gives a charging island diameter of d = 30 nm, consistent with the previous estimation.

Recently, it has been reported that CGT displays phase change properties with the amorphous phase becoming more conductive than the crystalline phase [33]. Moreover, a recent STM study has revealed that subgap states associated with chromium vacancies are present in exfoliated crystals [26]. Therefore, it would seem reasonable to assume that charging islands could be based on collections of chromium vacancies, however further investigations are required to confirm this. The tunneling between islands would then be through thin insulating CGT tunnel barriers, which have not been disordered significantly by the dielectric breakdown process. Applying an external magnetic field could lead to the charging islands becoming magnetized, which results in a tunnel magnetore-sistance effect. Indeed, a variety of systems displaying similar behavior have been shown [33–37].

Figures 3(a) and 3(b) shows the zero-bias magnetoconductance for opposite magnetic-field sweep directions in the range of $B = \pm 2$ T (the magnetic field is in the plane of the crystal, perpendicular to the vertical current). A clear anisotropy of the magnetoconductance is observed as the external field is reversed. Furthermore, we also observe a strong gate and bias tunability of the magnetoconductance for different magnetic field sweep directions [Figs. 3(a) and 3(b)]. Such behavior is similar to reports on single-electron transistor (SET) devices based on carbon nanotubes with magnetic contacts [1]. Figure 3(c) displays contour maps of the differential conductance versus V_g and V_{dc} for different values of magnetic field in the B = +2 to -2 T direction, as highlighted by dashed lines in Fig. 3(a). We observe a large change in the charging energy from $E_C = 5$ to 1 meV due to the field-dependent tunneling through the charging islands. Similar data for a perpendicular magnetic field is included in the supplementary materials [29].

Figure 3(d) shows the temperature dependence of the anisotropic magnetoconductance at $V_g = -50$ V. The tunneling magnetoresistance ratio (TMR) is defined as TMR = $100 \times (\Delta R/R_p) = (R - R_p)/R_p$ or $100 \times (G_p - G)/G$, where G_p is the value of the conductance at high field where the charging islands are fully magnetized in the direction of the external magnetic field and G is the external magnetic-field-dependent conductance. Specifically we observe a reduction of the TMR value of -95% at T = 4.2 K to just $\sim -1\%$ at T = 60 K. Interestingly, this is close to the Curie temperature of the pristine CGT [9] material. We note that this temperature corresponds to an energy larger than the average charging energy, indicating a different mechanism to that described above. Furthermore, given that the resistance at these higher temperatures becomes comparable to the resistance of the graphene electrodes (~ 20 K Ω), then the small anisotropic magnetoconductance could be explained through the proximity effect of graphene with the CGT. Indeed, similar observations have been reported previously in vertical heterostructures based on CrBr3 barriers [7]. Therefore, a dielectric breakdown of CGT crystals could be used to inject spin currents into graphene devices.

The gate-dependent TMR value is extracted from Figs. 3(a) and 3(b) and is plotted in Fig. 4(a). From this, we can observe that the magnitude of the TMR strongly depends on the gate voltage with certain regions fluctuating between positive and negative values. Ultimately we observe gate voltage averaged values of 100% as shown in Fig. 4(b) and peak values in excess of 800% [see the inset of Fig. 4(b)].



FIG. 4. Gate dependence of the tunnel magnetoresistance. (a) Contour map of the extracted TMR for different gate voltage and external magnetic fields for both magnetic-field sweep directions. (b) Gate averaged TMR value between $-80 < V_g < 80$ V. Measured at T = 4.2 K. (Arrows indicate magnetic-field sweep directions.)

III. CONCLUSION

In conclusion, we demonstrate a method to realize magnetic charging islands in vertical heterostructures comprised of graphene- $Cr_2Ge_2Te_6$ -graphene heterostructures through a simple dielectric breakdown process. The resultant devices display anisotropic magnetoconductance with peak TMR values in excess of 800% and back-gate averaged values as high as 100%. The magnitude and sign of the TMR signal can be modified by simple gate and bias voltages allowing new functionalities for future miniaturized devices. This technology could be improved upon to realize transport through single vacancies in vertical heterostructures, opening new avenues to achieve single-electron spintronics.

Methods

1. Device fabrication

Graphene, hBN, and CGT are prepared through mechanical exfoliation from bulk crystals. Graphene is first exfoliated from bulk graphite and transferred onto an hBN substrate that has previously been exfoliated onto a Si/SiO₂ substrate. This is followed by dry transfer of a thin crystal 10–50 nm of CGT and finally followed by the transfer of a top graphene electrode. Standard electron beam lithography was then carried out to define the contact locations followed by metallization with Cr/Au (5/50 nm). The Cr₂Ge₂Te₆ was purchased from HQ graphene while the hexagonal boron nitrite was acquired from Manchester Nanomaterials.

2. Materials characterization

Raman spectroscopy was carried out using 532 nm excitation at 0.4 mW laser power that is focused onto a 1 μ m spot. AFM was performed using a Bruker Innova system operating in the tapping mode to ensure minimal damage to the sample's surface. The tips used were Nanosensors PPP-NCHR, which have a radius of curvature smaller than 10 nm and operate in a nominal frequency of 330 kHz.

3. Electrical measurements

Electron transport measurements were performed in a variable temperature insert equipped with a 2 T solenoid. Lowfrequency ac measurements were carried out using standard lock-in amplifier differential conductance techniques with $V_{\rm ac}$ always set so that measurements are in the equilibrium regime $(k_B T/e \sim 300 \ \mu \text{V} \text{ at } T = 4.2 \text{ K}).$

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