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Embedded Dielectric Microstructures in Molecular Beam Epitaxy: High-quality Planar Coalescence toward Enhanced Optoelectronic Materials

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Embedded Dielectric Microstructures in Molecular Beam Epitaxy: High-quality Planar Coalescence toward Enhanced Optoelectronic Materials

by

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DISSERTATION

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Embedded Dielectric Microstructures in Molecular Beam Epitaxy: High-quality Planar Coalescence toward Enhanced Optoelectronic Materials

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Seamless integration of embedded dielectric microstructures in III-V crystal growth is a continued area of research due to its numerous high-impact applications. Historically, investigations into embedded dielectric microstructures within existing crystal growth techniques were focused on blocking dislocations at the III-V/dielectric interface in the production of low defect relaxed high mismatched heteroepitaxy. However, recent efforts have broadened the use of embedded dielectric microstructures for enhancement of optoelectronic device functionality and development of monolithic growth schemes toward integrated photonic circuits.

The central challenge of embedding dielectric microstructures in III-V materials is achieving single-crystal high-quality planar coalescence within existing conventional III-V crystal growth techniques without defect. While

prevalent in the field of III-V crystal growth, solid-source Molecular Beam Epitaxy (MBE) has a well-known "coalescence problem," historically lacking approaches that achieve planar coalescence over dielectric microstructures. Limited coalescence is in large part due to low diffusion of III-adatoms on dielectric surfaces, typically below 300nm, readily forming polycrystalline deposition on dielectric surfaces exceeding this diffusion length. Several solid-source MBE highly-selective growth and lateral epitaxial overgrowth (LEO) growth approaches have been reported; however, none demonstrating complete planar coalescence over dielectric microstructures.

In this dissertation, to overcome the "coalescence problem," we demonstrate for the first time a general methodology for an all-MBE growth of high-quality planar coalescence over a variety of embedded dielectric microstructures. Underpinning the approach, we developed a two-stage all-MBE growth approach for GaAs and InAs on (001) substrates, producing highly selective LEO and planarization, returning the growth front to the (001) surface. Characterization of the growth approach demonstrates for the first time an all-MBE approach to planar coalescence. In application of the two-stage all-MBE growth approach towards photonics, we demonstrate enhancement of quantum emitters using buried silica gratings arrays and develop several methodologies for embedded high-contrast photonic materials through self-formed air voids and molded air channel processes. Lastly, in application to high-quality relaxed high mismatch heteroepitaxy, we demonstrate for the first time an all-MBE approach to III-V metamorphic heteroepitaxy, demonstrating threading dislo-

cation reduction in InAs/GaAs metamorphics with high fill factor embedded silica gratings. Thus, from the material presented here, we provide several significant advances to the long-standing challenge of marrying high-quality semiconductor crystal growth with dielectric microstructures, unlocking several high-impact applications, including high-quality material pathways for enhanced quantum emitters and embedded metasurfaces as well as an all-MBE approach toward heterogeneous III-V integration on silicon.

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Chapter 1

Introduction

Seamless integration of embedded dielectric microstructures in III-V crystal growth is a continued area of research due to its numerous high-impact applications. Historically, investigations into embedded dielectric microstructures within existing crystal growth techniques for were solely focused on blocking dislocations at the III-V/dielectric interface in the production of low defect high mismatch III-V metamorphic heteroepitaxy [3, 4, 5]. However, recent efforts have broadened the use of embedded dielectric microstructures to enhance optoelectronic functionality, such as increasing light extraction via air voids in the III-Nitrides [6, 7], site-controlling the lateral position of quantum emitters [8, 9], and embedding air holes to create 2D-slab and 3D photonic crystals to enhance quantum emitters [10, 11]. Moreover, high lattice mismatch heteroepitaxy has been revisited using modern growth and fabrication approaches for dislocation blocking in a variety of material systems for low defect III-V growth on silicon [12, 13].

With the wide array of applications in mind, the primary challenge of embedding dielectric microstructures in III-V materials is achieving single-crystal high-quality planar coalescence within existing conventional III-V crys-

tal growth techniques. Specifically, planar coalescence over embedded dielectric materials requires the joining of two or more crystal fronts without forming defects while ideally returning the growth to achieve a planar episurface. As such, the quality and methodology to achieve coalescence is entirely specific to each conventional III-V crystal growth technique. Previous demonstrations of planar coalescence over dielectric microstructures has been achieved for homoepitaxial liquid phase epitaxy (LPE) [3, 14] and in both homoepitaxial and metamorphic metal-organic vapor phase epitaxy (MOVPE) [4, 15, 16, 17] in large part due to liquid and/or gas phase precursors forming limited III-V polycrystalline nuclei on dielectric surfaces. While prevalent in the field of III-V crystal growth, solid-source Molecular Beam Epitaxy (MBE) has a well-known "coalescence problem," historically lacking approaches that achieve planar coalescence over dielectric microstructures. Limited coalescence is in large part due to low diffusion of III-adatoms on dielectric surfaces, typically below 300nm [18], readily forming polycrystalline deposition on dielectric surfaces exceeding this diffusion length. Several solid-source MBE highly-selective growth and/or LEO growth approaches have been reported [19, 20, 21, 22]; however, none demonstrating complete planar coalescence of dielectric microstructures.

In this dissertation, to overcome the "coalescence problem," we demonstrate for the first time a general methodology for the all-MBE growth of high-quality planar coalescence over embedded dielectric microstructures. Underpinning the approach, we developed a two-stage all-MBE growth approach for GaAs and InAs on (001) substrates, producing highly selective lateral epitaxial

overgrowth (LEO) that resolves to a planar episurface. In application of the two-stage all-MBE growth approach, we explore enhanced photoluminescent test emitters, produce embedded high-contrast photonic materials, and improve III-V metamorphics using aa buried dielectric blocking layer approach. Thus, from the material presented here, we provide several significant advances to the long-standing challenge of marrying high-quality semiconductor crystal growth with dielectric microstructures, unlocking several high-impact applications, including enhanced quantum emitters and embedded metasurfaces as well as an all-MBE approach to heterogeneous III-V integration on silicon.

1.1 How to Read This Dissertation

This dissertation is organized into six chapters including this introduction. In Chapter 2, the general methodology, fabrication, and primary characterization techniques used in the production of III-V materials analyzed in this thesis are detailed. Also, an introduction to embedding dielectric microstructures through planar coalescence in III-V crystal growth is provided.

In Chapter 3, the background and motivation behind an all-MBE approach to planar coalescence over dielectric microstructures are provided. The initial work developing the two-stage all-MBE growth approach is investigated, where we demonstrate for the first time an all-MBE growth approach to high-quality planar coalescence over silica gratings at the micron-scale. In particular, we show the planar coalescence of GaAs on (001) GaAs substrates using a two-stage MBE growth approach over silica gratings aligned to the

[010] direction. Also, we rigorously evaluate the material quality of the overgrowth region using an optically-pumped InGaAs/GaAs/AlAs QW emitter grown directly above dielectric gratings and determine the dielectric integration is equivalent and in some cases exceeding grating-free controls due to extraction and Purcell enhancements.

In Chapter 4, we expand the use of the two-stage growth approach, exploring dielectric integration tailored for applications in embedded high-contrast photonics. Specifically, we apply a modified two-stage growth approach for the integration of tall, high aspect ratio dielectric gratings suitable for embedded metasurfaces. Then, using taller gratings as a mold, highly selective etch is shown to remove the silica gratings through mesas over 200μm in depth, producing high aspect ratio air channels, and thus achieving the highest contrast ratio embedded gratings in III-V materials. And lastly, in extending the two-stage approach to disc arrays, self-formed air voids are observed. In modifying the two-stage growth approach, not only are the air voids fully encapsulated and achieve planar coalescence, but also air void formation mechanisms in disc arrays are identified through growth investigation of planar coalescence and air void formation over off-[010] aligned gratings.

In Chapter 5, we explore and extend the use of the two-stage all-MBE growth approach to dislocation blocking in relaxed high mismatch heteroepitaxy known as epitaxial lateral overgrowth (ELO). Specifically, the two-stage approach is developed for InAs on previously relaxed InAs/GaAs. From the integration, planar coalescence InAs over varying fill factor [010]-aligned silica

gratings is shown to have significant material improvements, including an up to 50% increase in photoluminescence as well as up to 3x reduction to threading dislocation density. As a result, it marks not only the first demonstration on ELO using an entirely MBE approach, but also the second crystal growth technique to achieve ELO with planar coalescence.

Lastly, in Chapter 6, we summarize the work presented in this thesis, Also, we provide some general conclusions on the general implementation of the two-stage growth approach to a wide variety of embedded dielectric microstructures within conventional III-V MBE growth. Additionally, future outlook is provided.

Chapter 2

Methodology

While this dissertation centers on the growth of high-quality embedded dielectric microstructures using entirely MBE crystal growth techniques and its applications, a wide array of fabrication and characterization methods were also utilized in the production and assessment of the material. In this chapter, we provide a brief introduction to coalescence. Also, we detail the methodology necessary to sufficiently understand the fabrication, growth, and characterization of materials presented in this thesis at a general level. Additional background, including previous reports, and specific methodology pertaining to the material development will be presented in adjoining chapters.

2.1 What is Coalescence?

While applications utilizing embedded dielectric microstructures in III-V materials offer high promise, the central challenge in creating these materials remains in embedding dielectric structures while also maintaining high-quality, low defect III-V growth. Specially, embedding dielectric materials requires a growth process known as coalescence, the joining of two or more crystal fronts. When the growth progresses from lateral growth to coalescence, this process

in known as lateral coalescence. Additionally, when the coalescence proceeds to return the growth front to the original substrate orientation, typically the (001) surface, this is known as planar coalescence. More specifically, planar coalescence can be achieved solely from lateral coalescence; however, in many cases, lateral coalescence progresses in a non-planar fashion, requiring additional tailored growth to then achieve planar coalescence.

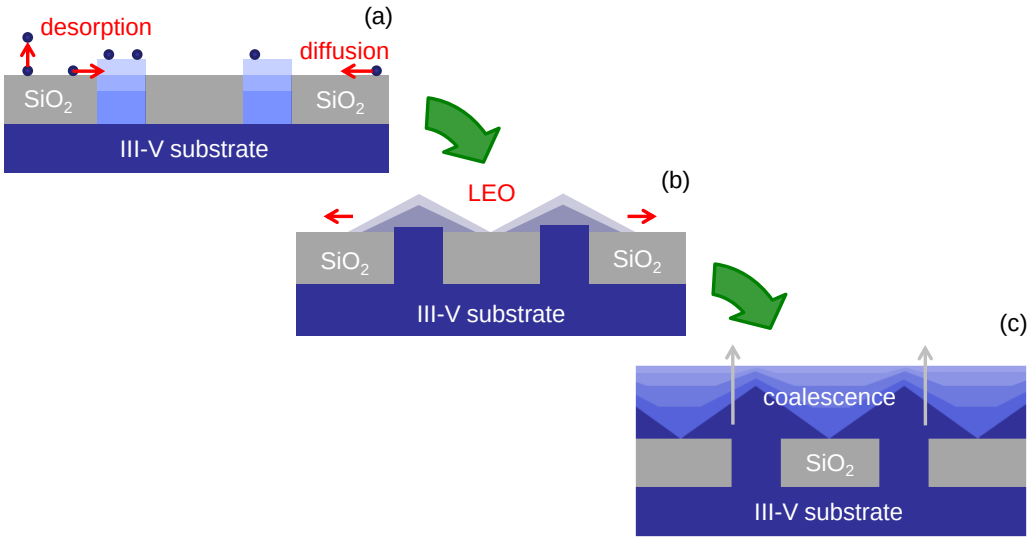

Figure 2.1: Key growth events in planar coalescence growth process starts by (a) maintaining selective growth, (b) producing LEO over dielectric surfaces using lateral growth techniques, and then (c) returning the growth toward a planar episurface.

While conventional crystal growth (MOCVD, MBE, LPE, etc.) each have unique methodologies for III-V epitaxy, the requirements needed to achieve coalescence over embedded dielectric microstructures can be broken down into three categorical steps as seen in Figure 2.1: highly selective growth, lateral

epitaxial overgrowth, and planar coalescence. The first step to coalescence is to achieve highly selective growth on dielectric surfaces as seen in Figure 2.1(a), which involves ensuring growth conditions at dielectric interface promote desorption and diffusion of growth species to avoid polycrystalline III-V nucleation on dielectric surfaces. In addition, the chosen dielectric materials must be chemically stable at growth conditions, ensuring the surfaces at the growth front do not react and/or decompose throughout the growth process. As such, dielectric materials are SiO_x and SiN_x are commonly used owning to their stability over a wide range of III-V growth conditions.

The second step to coalescence is lateral epitaxial overgrowth, where as the name suggests, a multistep growth process where crystal growth progresses across the dielectric patterns as seen in Figure 2.1(b). More specifically, LEO is seeded from openings in the dielectric pattern known as windows to the substrate. Then, seeded growth is tailored to promote lateral growth across the dielectric surface while also minimizing vertical growth. Since lateral growth occurs while maintaining selective growth conditions, the first and second step must be achieved simultaneously. Thus, sufficiently tailored LEO must also accommodate selective growth.

Lastly, the third step to coalescence is planar coalescence. Initially, lateral growth conditions are continued to achieve lateral coalescence, joining crystal fronts without defect as seen in Figure 2.1(c). Defective coalescence is not uncommon, occurring as threading dislocations in conventional III-V growth [14, 23] and grain boundaries in metamorphic GaN [24], but is

some cases be mitigated through changing the growth conditions and/or pattern alignments with primary crystal directions [15]. Then, once the growth achieves lateral coalescence, the growth is continued to resolve the lateral coalescence into planar coalescence. Ideally, a planar episurface would emerge immediately after lateral coalescence; however, this is not typical or should be the expectation of lateral coalescence. Instead, planar coalescence can be achieved secondarily after lateral coalescence through tailor growth conditions to drive planarization of the growth front [25]. Thus, in satisfying all three steps, successful planar coalescence is achieved.

2.2 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) was extensively used for the growth of single crystal III-V semiconductors in pursuit of an all-MBE approach to embedded dielectric structures through planar coalescence. As such, a brief overview of MBE is provided to give context to the extensive growth processes discussed in the adjoined chapters. This overview includes both general MBE reactor setup and conventional approaches to III-V MBE growth. As will been seen in later chapters, specialized MBE growth pertaining to planar coalescence over embedded dielectric growth will be provided therein.

2.2.1 What is MBE?

MBE is a crystal growth technique that allows for the growth of a wide range of thin epitaxial materials from oxides and metals to compound semi-

conductor alloys. Developed in the late 1960s by J.R Arthur and Al Cho [26], MBE differentiates itself from a variety of other crystal growth techniques as its ultra-high vacuum (UHV) growth environment allows for the full decoupling of key crystalline growth parameters. Specifically, under UHV growth conditions, mean free path of molecular species is on the order of kilometers, eliminating any reaction of molecular species prior to arriving at the growth surface. As a result, MBE permits growth under non-equilibrium, kinetically-limited conditions, and can be used to grow metastable materials that cannot be grown by near-equilibrium growth techniques. Furthermore, kinetic growth with MBE can achieve monolayer-scale smoothness at the growth front, yielding abrupt interfaces in layered stacks, ideal for quantum structures, such as quantum wells and quantum dots.

As an additional benefit to the UHV growth environment, reactor contaminants are limited from incorporation into the layered growth, allowing for low unintentional doped epitaxy when done in tandem with high purity source materials. Additionally, the UHV environment permits several in-situ analysis and characterization tools, the most common being reflection high-energy electron diffraction or RHEED. Thus, from the net growth benefits, MBE achieves the highest quality epitaxial growth among available crystal growth techniques.

2.2.2 MBE System Design

While a variety of commercial and research grade MBE system exist, all MBE system share core technological elements which permit MBE growth approach as depicted in Figure 2.2. To reach UHV conditions, MBE systems typically employee a host of pumps and cooling devices to maintain and regulate vacuum chamber pressure. Vacuum pumps (as well as a clean, well-baked vacuum environment) are key in achieving an UHV environment. An array of pumps, turbomolecular, cryogenic, and ion pumps are all commonly used in modern MBE systems depending on the residual gas dynamics of vacuum environment. In addition to pumps, the MBE reactor employs liquid nitrogen cooled walls known as a cryoshroud to freeze molecular contaminants such as C, O, and H_2O as well as the residual growth species from additional movement within the reactor. In tandem with UHV grade vacuum pumps, the cryoshroud help achieves the highest degree of UHV, typically between 10^{-10}-10^{-12} Torr. Lastly, monitoring residual molecular species is achieved using in-situ residual gas analyzers, essentially quadrupole mass spectrometers to measure the molecular mass of trace molecular species in the MBE reactor. Residual gas analysis is an especially useful tool in gauging system cleanliness and diagnosing MBE problems, such as vacuum leaks.

Delivery of molecular species is controlled through fluxes, the molecular arrival rate per unit area per unit time, through temperature-controlled effusion cells containing solid source material. Individual sources are further controlled using in-situ shutters that allow or block chemical fluxes at the growth

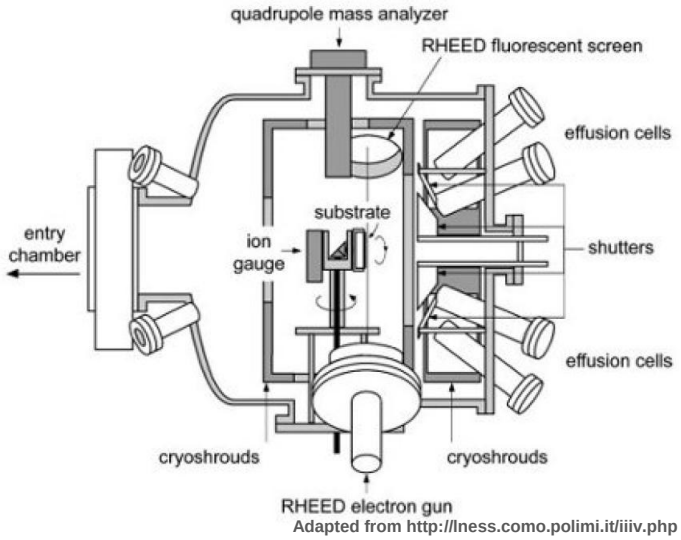

Figure 2.2: Schematic of a typical MBE system.

surface under actuation, effectively permitting digital control of composition down to the monolayer layer thicknesses. Calibration of molecular fluxes is achieved using an in situ beam flux monitor, essentially a vacuum filament gauge known as the beam flux gauge, which measures the beam equivalent pressure or BEP of the onset molecular flux. The beam flux gauge is mounted in the same position as the growth position; thus, flux calibration performed at the beam flux gauge should closely extend to the growth conditions. Lastly, the growth temperature is controlled by an azimuthally-rotated heating element with backside mounted thermocouple for precise control of the substrate temperature. When coupled with an ex situ viewport-mounted pyrometer, accurate calibration of temperature is added to the thermocouple readings.

Additional items added to the MBE reactor are typically in-situ char-

acterization tools which assess and monitor the epitaxial growth in real time. As mentioned previously, the most commonly added tool is RHEED. A powerful technique, RHEED utilizes electrons at a high energy where its effective wavelength is much smaller than the surface lattice conditions. Thus, focusing an electron beam at the sample surface causes diffraction with its constructive interference forming a distinct pattern based on surface conditions [27]. Generally, RHEED is key in monitoring basic growth events such as confirmation of a epitaxial surface after thermal deoxidation of a native oxide layer prior to growth. RHEED is also useful in estimation of growth rates using intensity modulations of primary secular spot known as RHEED oscillations [28]. To perform RHEED, an in-situ mounted high-energy electron gun is used to generate electron beams. To produce reasonably strong diffraction from the sample surface, low grazing angle of incidence of the electron beam is preferred in order to sample and collect over a wide area. Lastly, diffracted electrons are detected with an in-situ phosphor-coated viewport in which the visible phosphorescence is typically monitored using an ex situ camera.

To prevent outside contamination from loaded samples prior to growth, modern MBE systems commonly employ two additional chambers known as the load lock and buffer chamber, aligned in series to bake and clean samples several times before reaching the growth reactor. Load locks are used as an atmosphere-to-UHV pass-through, specifically to load and unload samples on a trolley/rail system. Incorporating entrance bakes to the load lock and sample-loaded trolley system, atmospheric contaminates are removed to reach

an acceptable UHV environment prior to entrance into the buffer chamber. Within the buffer chamber, sample-specific cleaning is performed, typically performing bakes of the sample and its sample holder known as a block prior to entering the reactor to further reduce contaminants. In many cases, sample-specific cleaning is performed, such as atomic hydrogen cleaning, to achieve a higher degree of surface contaminate removal prior to growth.

2.2.3 Conventional III-V MBE Growth Kinetics

While MBE growth applies to many material systems, this thesis solely focuses on the growth of conventional III-V alloys. Also, while highly tailored growth methods are detailed in the adjoined chapters, a basic overview of continuous III-V MBE growth is provide here as a baseline to the reader. Conventional III-V growth achieved through MBE is a direct result differing surface kinetics between the group-III and group-V adatoms on epitaxial surfaces [29]. Within a relatively wide range of growth temperatures (typically between 300-650°C depending on the III-V alloy), III-adatoms have unity sticking on both III-rich and V-rich epitaxial surfaces, meaning the entirety of group-III flux arriving the substrate surface will adhere at that surface. On the other hand, group-V adatoms under the same growth conditions will maintain unity sticking for III-rich surfaces but not for V-rich surfaces. Thus, under V-rich growth conditions, excess V-adatoms desorb from the growth front at an almost instantaneous rate.

Based on these differing kinetics, a recipe for robust III-V growth can be

formulated commonly referred to as continuous growth conditions. First, both III- and V-fluxes are deposited at the sample surface at the same time. Utilizing a group-V flux significantly greater than the group-III flux, the substrate surface maintains V-rich conditions. Since V-adatoms cannot oversaturate a growth surface, excess V-adatoms are desorbed, thus only incorporating stoichiometrically with unbonded III-sites. Common excess of V-adatoms compared to the III-adatoms between 1.5-3x known as a flux ratio can be used in the growth without concern of non-stoichiometric V-adatom excess incorporation, thus providing a very robust path to high-quality III-V growth.

These simple growth kinetics of III-V binary growth also extend to III-V tertiary and quaternary compounds since most III- and V-adatoms behave as described above. With that being said, this simple model breaks down under non-standard growth conditions. For example, very high or very low growth temperature change this III- and/or V- sticking models, and thus the growth quality without further tailoring continuous growth conditions. However, for most simple III-V heterostructures, continuous MBE growth conditions is sufficient.

2.3 Grating Fabrication and Growth Preparation

While the entirety of the fabrication process for growth-ready silica microstructures on (001) III-V substrates is detailed in Appendix 1, a brief summary is provided here. For MBE growth studies, silica gratings of varying crystal alignments and discs were fabricated on (001) III-V substrates.

Fabrication of silica microstructures started by stripping the native oxide and depositing silica via plasma-enhanced chemical vapor deposition (PECVD) at 250°C. Silica thickness varied between 20-300nm with individual thicknesses tailored for the specific growth investigation. After silica deposition, an additional α-Si layer was deposited and used as a sacrificial layer to protect the silica from fabrication contaminants, especially photoresist, to ensure the dielectric front was UHV/MBE compatible.

With deposition complete, conventional lithography and reactive ion etch (RIE) etch was used to generated silica features between 0.7-1.5μm in width. To generate features such as discs, bars, and/or windows as low as 0.7μm in size, high-resolution resist (Futurrex nr9-500p) along with vacuum contact conditions were used. Then, using the patterned resist as an etch mask, the PECVD silica was etched using RIE under a CHF_3/O_2 etch chemistry. Careful note was taken to adjust the etch duration according to α-Si/SiO_2 thickness to avoid forming crystal damage by overetching into the III-V substrate, undesirable for seeded regrowth.

After the dry etch, the resist mask was removed using AZ KwikStrip and a-Si sacrificial layer removed using 2.5% diluted TMAH at 60°C, both highly selective to III-V materials, such as GaAs and InAs, and silica. Next, the silica pattern was cleaned and the III-V substrate was recovered simultaneously using an O_2 plasma/HCl etch known as a digital etch. Essentially, the digital etch removes any trace amounts of contaminates such as photoresist while also oxidizing and stripping any III-V crystal damage isolated near the

episurface, Additional digital etches were repeated as needed if the episurface was not recovered on the first attempt.

After reclamation, fabricated patterned samples were loaded into the MBE load lock and buffer system, specifically to provide the final clean using atomic hydrogen [30], which ensures the episurface is clean of O and C from the fabrication steps, prior to transfer to the reactor. Once transferred to the growth position, any remaining surface oxides were removed using a 10 min thermal desorption under an V-overpressure. For the work detailed in this thesis, MBE growth was primarily performed on an EPI Mod Gen II MBE system including buffer chamber and load lock known as system Echo. While having several sources available on Echo, only three where primarily utilized: Ga and In elemental sources loaded in SUMO style effusion cells and a valved As source with cracking zone. Additional growths were performed on an Varian Mod Gen II MBE system including buffer chamber and load lock known as system Bravo. While having several sources available on Bravo, only four where primarily utilized: Ga, In, and Al elemental sources loaded in SUMO style effusion cells and a valved As source with cracking zone. Additionally, the Bravo-mounted atomic hydrogen station was frequently used for cleaning of patterned dielectric substrates prior to growth.

2.4 Characterization Methods

In this section, basic descriptions are provided for the primary material characterization methods utilized in this thesis. For brevity, references will

be provide for extended discussion elsewhere. Also, less used characterization techniques will be reported within adjoining chapters.

2.4.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is an imaging technique which uses the interaction of focused electron beams at a sample surface to produce an image. By using an electron beam instead of light, optical diffraction limits of a few hundred nanometers can be overcome. Through varying the beam conditions, such as beam intensity, resolution as low as 1nm can be achieved, making SEM an ideal surface imaging technique for high resolution micro- and nano-sized structures.

While SEM can provide a wide range of detection, sensing, and imaging, the most common imaging condition is the detection of secondary electrons emitted from the surface atoms excited by the electron beam. The magnitude of secondary electrons counts detected depends on a number of factors, such as sample topography and composition. Thus, by rastering and collecting the emitted secondary electrons using a detector, an image of the surface is generated.

Under these conditions, there are two methods of preparation of a semiconductor sample for surface imaging. Planview SEM was used to image the growth surface of the substrate and cross-sectional SEM was used to image the buried layer of an epitaxial stack. While planview SEM requires little sample preparation, cross-sectional SEM images requires some sample destruction by

cleaving the sample into pieces in order to expose the buried layers for imaging.

Both planview and cross-section SEM imaging were extensively used in this thesis. SEM imaging was performed using a Zeiss Neon40 FE-SEM. Planview SEM was employed to determining lateral growth rates and detection of polycrystalline formation on dielectric surfaces. Cross-sectional SEM was used to display embedded dielectric structures and determine facet plane angles. For more information regarding SEM techniques and its applications, a detailed overview can be found here [31].

2.4.2 Atomic Force Microscopy

Atomic force microscopy (AFM) is a high-resolution scanning probe technique which uses the optical detection of surface proximity cantilever deflections to measure surface properties, such as height, friction, and conduction. Using a piezoceramic cantilevered tip, a probe can be placed on or near the sample surface, and then in scanning the surface, small deflections of the probe tip can be optically measured by focusing a laser at the cantilever tip and detecting the optical signal using a position sensitive detector. AFM setup in this scanning configuration can achieve very high resolution with vertical displacements detection as low as 0.1nm. While AFM analysis can provide a wide range of surface analysis, the most common scanning condition used in this thesis was surface height topographical imaging, specifically to measure of the root mean square (RMS) of sample surface roughness. AFM was performed using Veeco Nanoscope V using a silicon probe tip in contact mode.

For more information regarding AFM technique and its applications, a detailed overview can be found here [32]

2.4.3 Fourier Transform Infrared Spectroscopy

Fourier transform infrared spectroscopy (FTIR) is a technique used to measure the emission and absorption features of samples in any phase of matter between the near- and far-IR spectrum of light. Specifically, by using a broadband light source, an interferometer is able to collect a wide spectrum signal known as the interferogram. In performing a Fourier transform of the interferogram, the spectral features are revealed. When performing spectral analysis under this approach, FTIR has a significant advantage in the rapidity of the measurement compared to a dispersive spectrometer, which measures light intensity over a narrow spectral range at a time.

While an FTIR spectrometer has a wide array of characterization applications, in this thesis FTIR was used to measure the change in reflectance of semiconductor samples as a result of embedded dielectric structures. Specifically, reflectance measurements used a Bruker Vector 80v FTIR spectrometer interfaced with a liquid nitrogen cooled microscope-focused HgCdTe detector and mid-IR light source able to achieve spectral measurements between 1.25-16μm. Also, in normalization of reflectance measurements, a gold mirror was used as the reference sample. For more information regarding FTIR and its applications, a detailed overview can be found here [33].

2.4.4 Photoluminescence Spectroscopy

Extensively used in this thesis, photoluminescence (PL) spectroscopy is a general characterization technique used to probe the electronic structure and its associated radiative properties of semiconductor materials. Fundamental to PL, a laser is used to optically pump materials to generate electron-hole pairs within the sample and its resulting radiative recombination measured. More specifically, a laser is focused at the surface of the sample where the majority of the photocarriers are generated at the position of the laser focus. For efficient absorption of the pump laser, the lasing emission energy must be above the band gap of the semiconductor material. Then, photogenerated carriers which radiative recombine are collected and measured using a dispersive spectrometer and detector configured for the specific PL emission. For more information regarding PL and its applications, a detailed overview can be found here [34].

For the majority of PL presented in this dissertation, a custom coaxial PL system was utilized as depicted schematically in Figure 2.3. A green 532nm frequency-doubled neodymium-doped yttrium aluminum garnet (Nd:YAG) solid-state diode-pumped laser was used to optically pump semiconductor samples up to 110mW (2.4 kW/cm^2). For samples in the near-to-mid IR, pump conditions were sufficient in achieving several absorption depths within a few hundred nanometers. Light emitted by the samples was collected by 1 inch diameter CaF_2 optics, dispersed by a 0.5m grating spectrometer, and detected by either a thermoelectrically-cooled InGaAs detector to detect near-IR PL emission up to the 1.65 μm cutoff or a liquid-nitrogen-cooled InSb detector

to detect both near- and mid-IR PL emission up to the 5μm cutoff. Heterodyne detection using a chopper wheel in front of the pump laser and a lock-in amplifier was utilized to maximize the signal-to-noise ratio. Lastly, a nitrogen purge of the spectrometer and pump collection box was used to minimize H_2O and CO_2 absorption features within the near- and mid-IR.

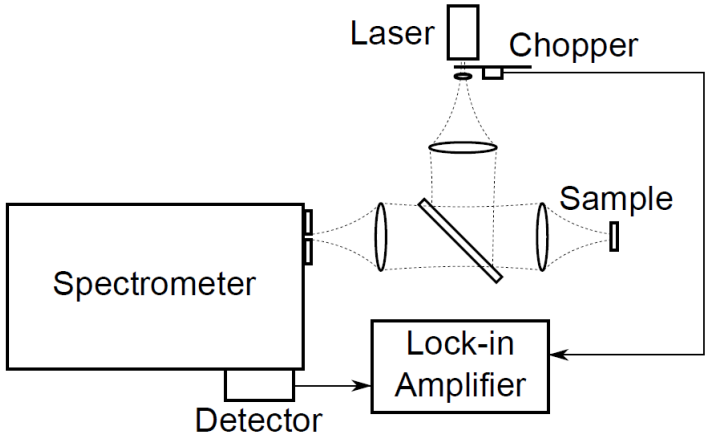

Figure 2.3: Schematic of the coaxial photoluminescence system used in this dissertation.

While the majority of the PL spectroscopy presented here was performed at room-temperature at high-excitation to generate a large signal, more specific PL analysis was performed as needed. For example, excitation-dependent PL is a form of PL analysis which varies the optical pump intensity, essentially varying the photocarrier density within the sample to determine any pump dependent phenomena. To perform EDPL, pump intensities were varied using neutral-density (ND) optical filters to attenuate the pump inten-

sity prior to exciting the sample. Another PL analysis technique frequently used was temperature-dependent PL (TDPL). By varying temperature of a semiconductor sample, TDPL can determine a host of phenomena, such as activation energies, increasing signal strength, red- and blue-shifting emission, etc. To perform TDPL, less than 1x1cm^2 samples were mounted to copper chuck within a liquid-nitrogen cooled cryostat. Additionally, using mounted heater wire with thermocouple at the copper chuck, sample temperatures were adjusted and controlled between 77-320K.

Chapter 3

High-quality All-MBE Planar Coalescence over Embedded Dielectric Microstructures

Historically, MBE has a well-known "coalescence problem," having limited methods for highly-quality lateral epitaxial overgrowthv (LEO) and planar coalescence over micron-scaled dielectric structures [35, 36]. To this end, in this chapter, we detail a new methodology for achieving high-quality planar coalescence over dielectric microstructures using entirely MBE growth. In overcoming the "coalescence problem," we demonstrate for the first time an all-MBE growth approach for planar coalescence over micron-scaled dielectric microstructures. Specifically, we developed a two-stage all-MBE approach to planar coalescence which first uses III-cyclic growth to produce a highly selective {011}-faceted lateral epitaxial overgrowth over [010]-aligned silica gratings patterned on (001) substrates, then secondly utilizes continuous growth to resolve the non-planar LEO template toward a planar episurface. As a sensitive probe to the crystal quality, an InGaAs/GaAs/AlAs photoluminescence (PL) test emitters grown directly above the embedded dielectric gratings after planar coalescence, resulting in equivalent emission characteristics compared to grating-free controls. In addition, we demonstrate that it is possible to further tailor these structures to enhance emission of the test emitter. In particular,

we show a 1.4x enhancement to photoluminescence from test emitter grown directly above encapsulated 1.4μm pitch silica gratings as a result combination of Purcell and extraction enhancements.

3.1 Previous Methods in Homoepitaxial III-V Embedded Dielectric Integration

Lateral epitaxial overgrowth leading to planar coalescence over embedded dielectric microstructures remains an active area of conventional III-V crystal growth from a fundamental material perspective owing the challenges associated with producing high-quality single-crystal integration. The primary challenge in LEO is producing sufficiently high lateral-to-vertical growth while also limiting the formation of poly-crystalline deposition on dielectric surfaces. When growth leading to planar coalescence is required, additional challenges are realized, primarily producing lateral coalescence of growth fronts without major defects while also regaining a planar episurface.

Since the challenges are growth-based, investigation into high-quality planar coalescence focuses entirely around the methodologies of a specific crystal growth technique, dielectric microstructure geometries (typically gratings) and substrate orientation. Historically and presently, MOVPE is the preferential lateral growth technique owing to its vapor phase growth precursors which form limited polycrystalline nucleation on amorphous dielectric patterns like silica, thus achieving highly selective growth. As such, the first reports of LEO with conventional III-V materials were investigated in the homoepitaxial

growth of GaAs and InP using chloride VPE and MOVPE on (110) substrates [37, 4, 38]. In this initial work, high lateral-to-vertical growth over silica and carbonized resist gratings were reported, as high as 25x, while material quality specific characterization of the LEO and coalescence were not reported.

Greater attention to LEO including planar coalescence was explored by Nishinaga et al. in LPE growth experiments in both homoepitaxial GaAs, InP, and GaP over silica microstructures on (111)B and (100) oriented substrates [39, 40, 41]. Like MOVPE, LPE is another preferred crystal growth technique for lateral growth due to the liquid phase which is highly selective to amorphous materials like silica. While demonstration some exceedingly high lateral-to-vertical growth using LPE as much as 50x was reported, some of the most impactful work was performed in homoepitaxial investigations of planar coalescence. Specifically, modeling of planar coalescence was heavily investigated determining to key coalescence modes [14]. When crystal fronts coalesce at a singular point known as a "one-zipper" mode, no defects form in the coalescence. However, when crystal fronts coalesce at more than one front, known as "two-zipper" modes, threading dislocations form at the last point of coalescence. With respect to high optical quality applications, "two-zipper" coalescence is considered undesirable as it would result in threading dislocation density on the order of 10^7 cm^{-2}, exceeding high for applications in both relaxed high mismatch heteroepitaxy and optoelectronic applications.

While use of LPE growth has diminished, recent progress using modern MOVPE growth has been demonstrated in high-quality homoepitaxial dielec-

tric integration. Since its initial work, planar coalescence through MOVPE has been demonstrated in a wide array of homoepitaxial systems over micron-scaled structures in InP and GaAs [15, 42]. Among recent reports, detailed investigation to planar coalescence in MOVPE growth was performed by Bowers et al. of homoepitaxial InP over silica gratings on (001) InP substrates [15]. Specifically, LEO was found to vary with V/III ratio and coalescence varied based on grating alignment to primary crystal directions. Importantly, planar coalescence was preferred in gratings aligned with the $\langle 010 \rangle$ directions. Also, "one-" and "two-zipper" like coalescence modes were identified in MOVPE growth mirroring similar investigations in LPE.

3.2 The "Coalescence Problem" in MBE

While prevalent in III-V crystal growth, solid-source MBE has a well-known "coalescence problem," historically lacking approaches which achieve planar coalescence over dielectric microstructures. As identified in Chapter 1, limited coalescence is in large part due to low diffusion of III-adatoms on dielectric surfaces, typically below 300nm [18], readily forming polycrystalline deposition on dielectric surfaces exceeding a diffusion length as illustrated in Figure 3.1.

3.2.1 Previous Work in MBE LEO and Coalescence

Several approaches have been demonstrated to extend LEO to MBE growth; however, many implementations lack desirable growth characteristics

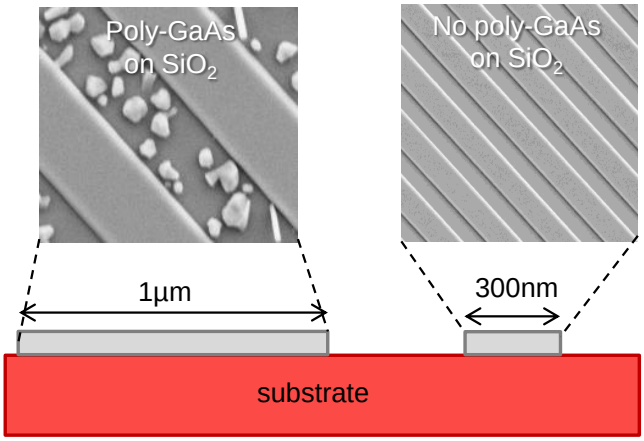

Figure 3.1: Illustration depicting polycrystalline formation on dielectric gratings due to low adatom diffusion lengths on amorphous surfaces using conventional MBE growth. Structures scaled above a diffusion length form polycrystalline nuclei (left) whereas structures scaled below it do not (right).

such as limited coalescence or requiring specialized growth equipment. For example, low-angle incidence microchannel epitaxy (LAIMCE) proposed by Nishinaga et al. is an selective MBE growth technique that enhances both lateral diffusion and selective growth by sending Ga and As fluxes at a low angle fixed at 10° with respect to the substrate leading to micron-scale LEO over dielectric masks [19, 23]. While successful at achieving LEO at relatively high growth rates of 1μm/hr, this technique is undesirable due to the need to produce a highly modified MBE reactor to achieve similar results. Also, using the LAIMBE technique for lateral coalescence results in the formation of screw dislocations at the joined crystal fronts, undesirable for high optical quality applications. Additionally, no pathway for planar coalescence was reported using the LAIMCE technique.

MBE-based LEO can also be accomplished through the fabrication of dielectric structures below sub-adatom diffusion length scales and growth at elevated temperatures [20]. At 630°C, Ga adatom sticking coefficient on silica surfaces is less than 1% of the total flux while maintaining near unity Ga sticking on GaAs surfaces. Thus, through the fabrication of nanostructures below Ga adatom diffusion length scales typically below 200nm, poly-crystalline free growth on silica surfaces is guaranteed. As such, under tailored growth conditions, LEO was reported on silica surfaces. While successful, many aspects of this approach are undesirable, chiefly use of nanoscale dielectric structures, requiring challenging lithography, limiting using in practical photonic structures as well as applications utilizing large silica bar width schemes such as dislocation blocking in metamorphics. Also, this work did not demonstrate a pathway to planar coalescence.

The most effective approach to date for MBE LEO over micron-scaled patterns was reported by Nishinaga et al. using Periodic Supply Epitaxy (PSE) [43], a solid-source MBE growth technique that cycles group-III deposition under a constant group-V overpressure. Periodic cycling the group-III source limits polycrystalline formation to small nuclei on dielectric surfaces after which the periodic growth pauses allow for the decomposition and desorption of the polycrystalline nuclei off the dielectric surface. Importantly, PSE growth is able to extend GaAs diffusion length on silica surfaces from 300nm under continuous conventional MBE growth to nearly 60μm using PSE growth approach [44], sufficiently high for dielectric integration at the

micron scale. Additional PSE work demonstrated highly-selective LEO over micron-scale gratings aligned to the [110] and [1$\bar{1}$0] directions, demonstrating to non-planar encapsulation and lateral coalescence over the silica gratings [22]. While promising, this report only confirms lateral coalescence via plan-view and cross-sectional AFM; no other imaging nor characterization of the material quality of the lateral coalescence was reported. Additionally, no pathway toward planar coalescence was provided.

3.2.2 A New Pathway toward MBE Planar Coalescence

Utilizing the most promising pathways reported for all-MBE LEO, we performed a systematic investigation of LEO and coalescence in using solid source MBE with the goal of producing high optical quality embedded dielectric integration. However, before investigating planar coalescence over dielectric microstructures utilizing solely MBE growth methods, key materials and growth variables were identified. A test material system was chosen as silica gratings encapsulated in GaAs epitaxial growth on (001) GaAs substrates seen in Figure 3.2. Silica was the preferred dielectric for embedding due to its chemical stability at conventional III-V MBE growth conditions, and GaAs was chosen as the preferred III-V material due to its wide growth space as well as its well-reported growth on masked silica substrates [21]. Since the integration of dielectric structures exceeding the Ga adatom diffusion lengths on silica was the goal, grating bar widths were varied at 0.7μm, 0.8μm, and 0.9μm, all exceeding the conventionally grown GaAs diffusion length by 2-3x. To keep the

methodology simple, the grating fill factor was fixed at 50%; thus, changing bar width correspondingly changed the pitch as 1.4μm, 1.6μm, 1.8μm, respectively. Lastly, since GaAs growth is highly anisotropic with lateral growth preferred along the [1$\bar{1}$0] direction [45], three grating alignments were varied, individually aligned to the [110], [010], and [1$\bar{1}$0] directions, respectively. Thus, in total, nine grating pitch and alignments were investigated.

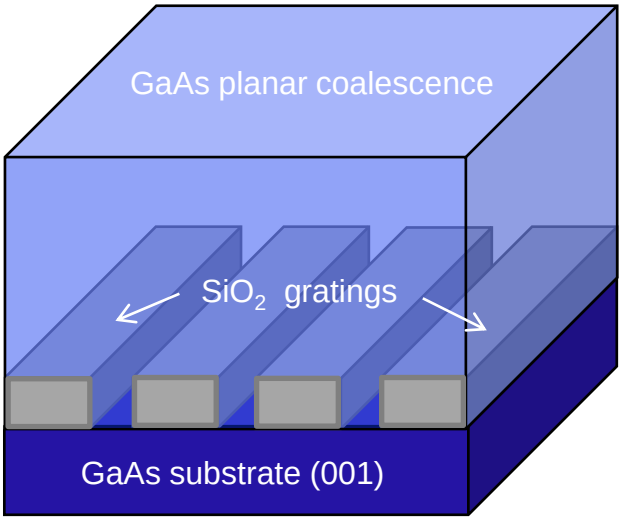

Figure 3.2: 3D drawing depicting the test material system: silica gratings encapsulated in GaAs.

3.2.3 Using PSE-MBE to Achieve Highly Selective GaAs LEO

With the material system and growth space identified, the first challenge to planar coalescence was producing simultaneously highly selective growth and LEO of GaAs over silica gratings as depicted in Figures 3.3(a) and 3.3(b).

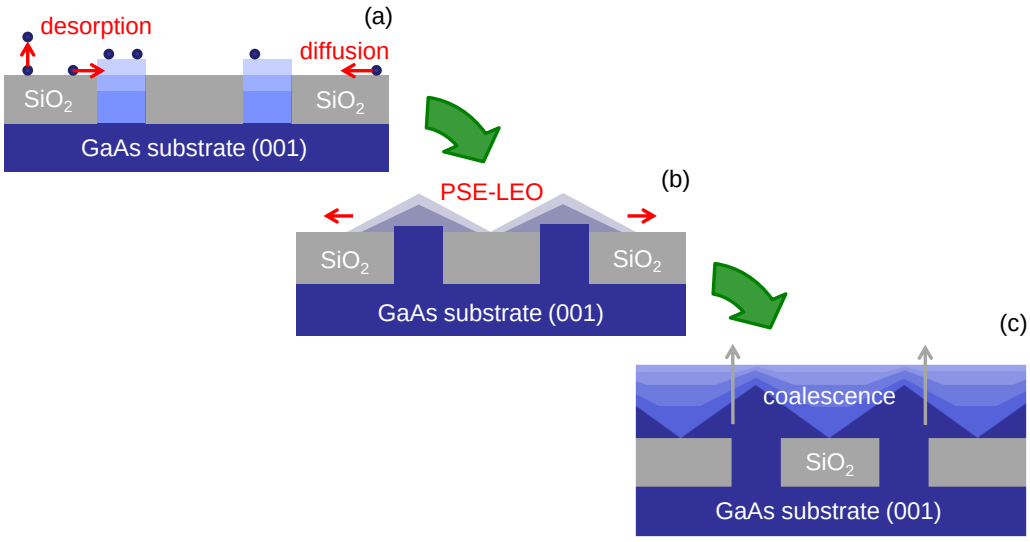

Figure 3.3: Planar coalescence in the all-MBE growth process starts by (a) maintaining selective growth and (b) producing faceted LEO over silica bars using PSE then (c) resolving the growth toward a planar episurface once templated with GaAs LEO using continuous growth.

As a starting point to the LEO investigation, we utilized PSE growth conditions from the only report of MBE lateral coalescence over silica microstructures [22]. In particular, using PSE-MBE growth for LEO, GaAs growth over silica gratings was initiated at growth temperatures between 625-630°C under a large As_4 overpressure, 76x As_4/Ga BEP ratio utilizing a 50% PSE duty cycle (30s growth then 30s growth pause) at a growth rate of 0.25μm/hr as these conditions were sufficient in producing highly selective growth while also maintaining a reasonably high growth rate. To examine the PSE-LEO over the silica gratings, the total number of PSE cycles was varied between 180 and 360 cycles and the resulting growth geometry was visually

inspected through planview SEM images as seen in Figure 3.4.

From the initial LEO investigation, distinct differences emerged entirely dependent on the alignment of the gratings with respect to crystal direction and independent of grating pitch and bar width. Gratings aligned parallel to the [110] direction had significant LEO as seen in Figures 3.4(a) and 3.4(b), emerging as {111}B faceted growth, consistent with MBE-GaAs growth on [110]-oriented mesas [46]. However, as the LEO evolved over the silica surface, nodules of dissimilar facets clearly emerged the edges of the {111}B lateral overgrowth after 180 cycles as seen in Figure 3.4(a) and when further pushed to 360 cycles, its formation appeared to result in uneven lateral coalescence as seen in Figure 3.4(b). While successful at generating LEO, the uneven lateral coalescence from [110]-aligned gratings was marked as unsuitable for resolving to planar coalescence.

For gratings aligned parallel to the $[1\bar{1}0]$ direction, limited LEO was observed, resulting in mostly vertical, wire-like growth as seen in Figures 3.4(c) and 3.4(d). Even after 360 cycles of PSE-GaAs growth, limited LEO was observed, forming {110} faceted sidewalls. This is consistent with preferred lateral growth for MBE-GaAs along the $[1\bar{1}0]$ direction, preferring growth along the windows, parallel to the gratings with limited LEO from forming across the silica surfaces. As such, the lack of lateral coalescence marks the $[1\bar{1}0]$-aligned gratings unsuitable for resolving the growth to planar coalescence.

Interestingly, successful LEO was found for gratings aligned parallel to the [010] direction producing the most uniform and well-faceted PSE-LEO as

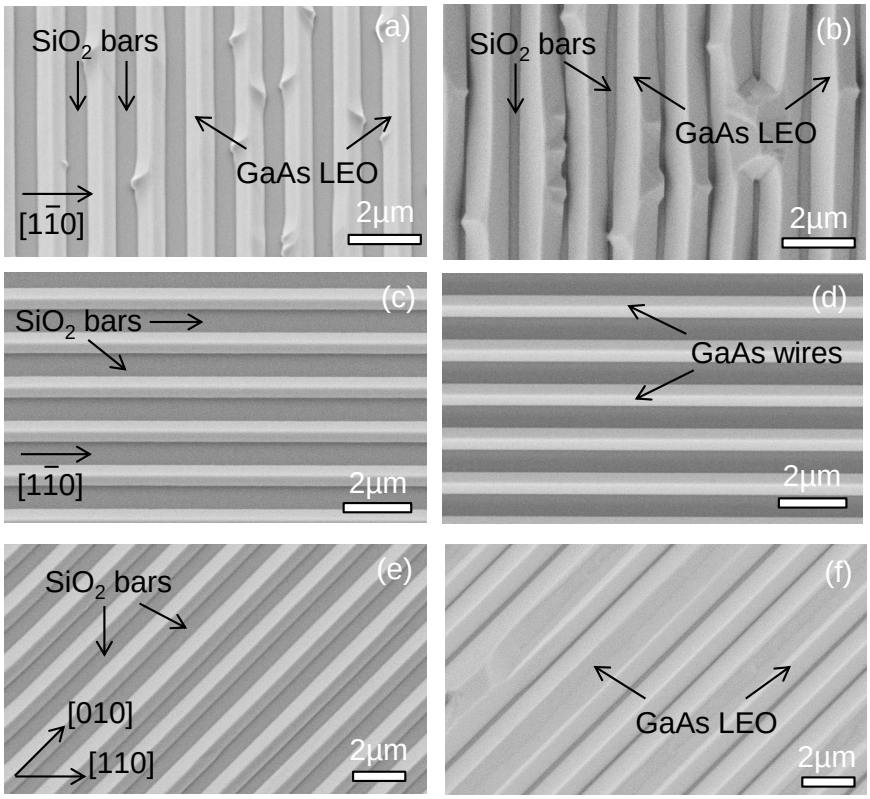

Figure 3.4: Planview SEM of PSE-LEO over silica bars (a)-(f). Gratings aligned to [110] direction show uneven LEO for (a) 180 and (b) 360 PSE cycles. Gratings aligned along the [1$\bar{1}$0] direction show vertical wire-like growth for (c) 180 and (d) 360 PSE cycles. Gratings aligned along the [010] direction show well-faceted, uniform LEO for (e) 180 (f) 360 PSE cycles.

seen in Figures 3.4(e) and 3.4(f). As the LEO evolved over the silica surface, smooth {011}-faceted growth clearly emerged after 180 cycles as seen in Figure 3.4(e) and consistent with MBE-GaAs growth on [010]-oriented mesas [17]. When further pushed to 360 cycles, its formation appeared to result in partial lateral coalescence as seen in Figure 3.4(f). Looking at cross-sectional

SEM in Figure 3.5, after 360 cycles, PSE-LEO clearly forms {011} facets, a preferred geometry due to its nearly 3:1 lateral to vertical growth along the [110] direction as well as the encapsulation of silica bars through lateral coalescence as seen in localized areas. Due to the smooth, well-faceted {011} LEO as well as partial lateral coalescence, [010]-aligned gratings were marked as the preferred growth space for resolving the PSE-based LEO into complete planar coalescence.

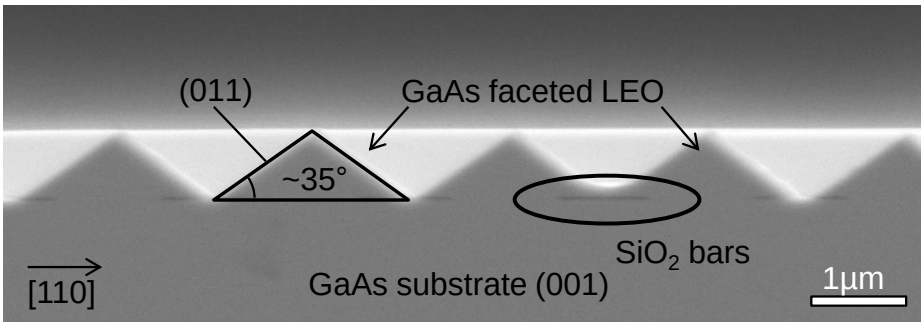

Figure 3.5: After 360 cycles, gratings aligned along the [010] direction show the formation of {011}-faceted LEO and lateral coalescence.

3.2.4 Demonstrating Planar Coalescence using Continuous Growth

In identifying a growth space where highly selective LEO occurs over micron-scale silica gratings, a two-stage growth approach could be identified. Since the lateral coalescence effectively produces a non-planar GaAs patterned template, a second stage of MBE growth leveraging planarization of valleyed microstructures can resolve lateral coalescence into planar coalescence as depicted in Figure 3.3(c). Thus, in identifying a second stage to complete the

planar coalescence over a laterally grown template, tailored continuous growth conditions offered the most promising growth characteristics for growth toward planarization as faceted valley structures with high surface diffusion, such as those in the {011} family [17] have the potential to planarize due "capillary" growth in the valleys due to slow growth rate along these facets [47].

Thus, to investigate planar coalescence using a two-stage approach, gratings were initially templated with 300 cycles of LEO over [010]-aligned 1.4-1.8μm pitch gratings using the previously described PSE-LEO method. In the first stage, LEO was tailored to specifically not to complete lateral coalescence but rather to reach below an Ga adatom diffusion length as this is sufficient to use continuous MBE growth without concern of polycrystalline formation on the silica bars. Then, in the second stage, 2μm of GaAs was grown using continuous MBE growth over the LEO template. Continuous GaAs growth conditions utilized a 45x As_4/Ga BEP ratio with growth temperatures and rates at 570°C and 0.5μm/hr, respectively. Upon completion of the second stage growth, it was clear the templated growth of the first stage had reached planarization in-situ as RHEED showed a clear streaky 2x pattern, indicating a smooth growth front as seen in Figure 3.6.

Taking a closer look at planar coalescence ex-situ, cross-sectional SEM and AFM were performed. Planar encapsulation of the silica gratings can be clearly seen in Figure 3.7 from the cross-sectional SEM images where the thin 1.4μm pitch silica gratings are seen embedded under 2.6μm of total GaAs growth resulting from both LEO and continuous growth stages. Surface rough-

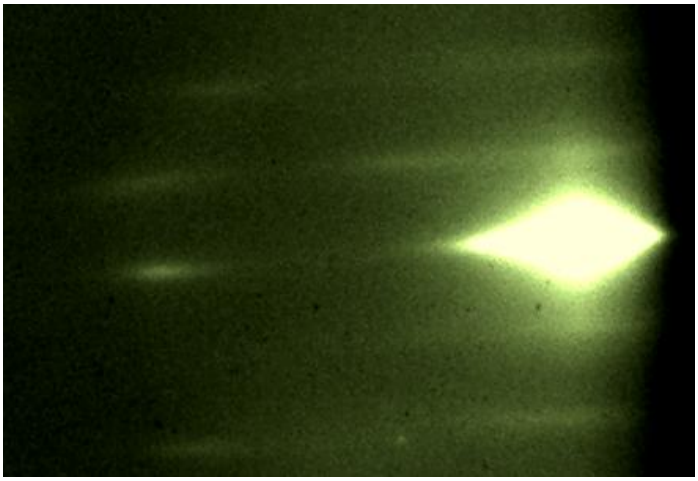

Figure 3.6: RHEED image showing a clear 2x pattern after planarization of the GaAs episurface.

ness after planar coalescence also remained low but varied between 1.4-1.8μm pitch samples, achieving a range between 3.2-7.2nm RMS roughness as plotted in Figure 3.8. A clear trend emerged as the surface roughness of the planar coalescence fit well to an exponential trendline with varying grating pitch. Extrapolating the trendline, a grating pitch of 1.0μm at a 50% fill factor was projected for coalescence below 2ML of RMS roughness. Further surface roughness reduction may also occur for additional continuous growth and/or use of growth surfactants such as Bi [48, 49].

As a sensitive probe to the material quality of the all-MBE two-stage approach to GaAs planar coalescence, PL spectroscopy was performed. As an indicator of coalescence quality, an optical-pumped emitter was grown after planar coalescence, composing of a single 10nm $In_{0.15}Ga_{0.85}As$/GaAs quantum

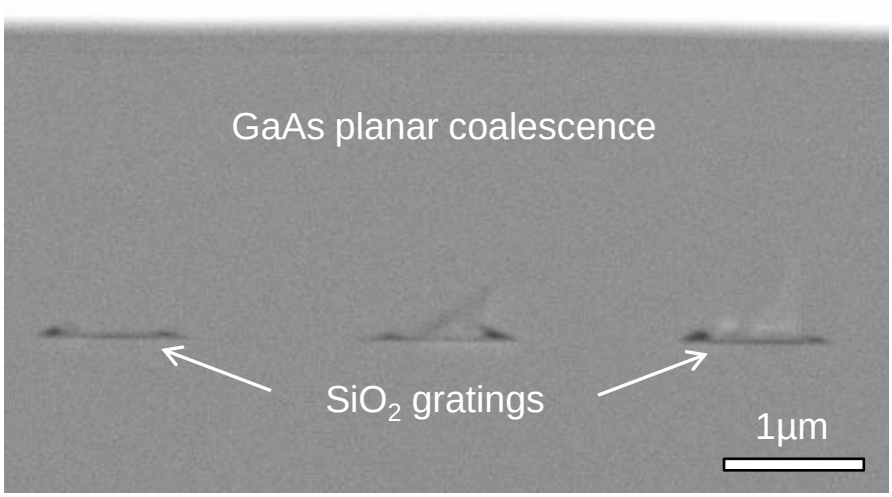

Figure 3.7: Cross-sectional SEM image showing embedded silica gratings, resulting from the two-stage growth approach.

well (QW), 200nm GaAs absorbing region sandwiched between two 10nm AlAs wide band gap carrier blocking layers, electrically isolating the photogenerated carriers to the quantum well instead of alternate non-radiative recombination sites such as surface state or the silica/substrate interface. Thus, the indicator emitter gauges any reduction in PL as a result of non-radiative material defects from coalescence such as threading dislocations, point defect, and/or grain boundaries. Also, as a control, an identical emitter was grown on unpatterned grating-free (001) GaAs substrates using equivalent layer thicknesses including a 2.6μm buffer layer.

From an initial investigation at room-temperature conditions, all embedded grating samples achieved peak PL response within 2x compared to the

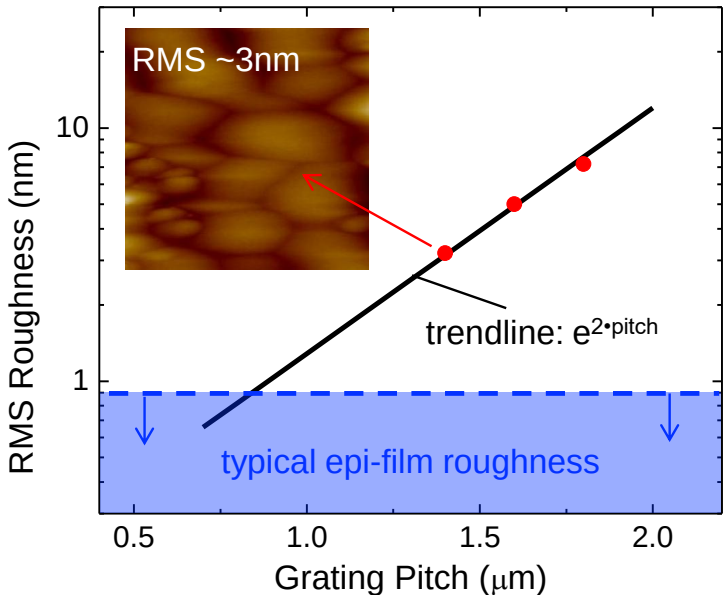

Figure 3.8: Plot of surface roughness varying grating pitch which fit well to trendline projecting sub-2ML roughness for 1.0μm pitch gratings. (Inset) AFM shows the surface morphology of a 10x10μm scan for the embedded 1.4μm pitch gratings with 3.2nm RMS surface roughness.

grating-free control as seen in Figure 3.9. The equivalent degree of luminescence of the material above embedded gratings compared to control strongly suggests the planar coalescence from the two-stage growth approach is without significant non-radiative defects, such as threading dislocations, and that coalescence likely occurs as a "one-zipper"-like mode as opposed to the dislocation creating "two-zipper" mode [14]. Also, two-stage MBE planar coalescence is in agreement with planar coalescence in MOVPE which observed equivalent dislocation-free coalescence for [010]-aligned dielectric structures [15] as characterized by TEM.

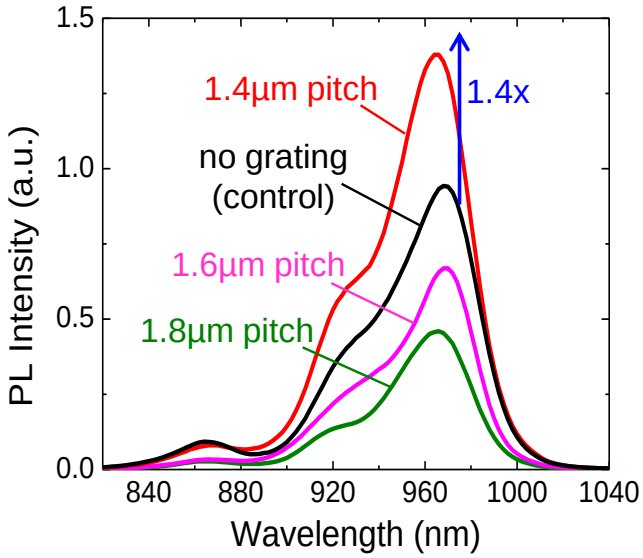

Figure 3.9: PL response of [010]-aligned embedded silica gratings compared to control. Peak PL of the gratings samples were within 2x of the grating-free control.

3.3 Investigating PL Enhancement in InGaAs/GaAs QW Emitters over Embedded Gratings

As a consequence of the PL material quality investigation, a significant increase in peak PL occurred for the emitter grown above the 1.4μm pitch embedded gratings demonstrating 1.4x increase compared to control. As such, further investigation was led to understand this increase. Excitation-dependent PL was performed on both the embedded 1.4μm pitch gratings and control emitters to determine if the enhancement was due to high pumping intensities employed in the initial investigation. As seen in Figure 3.10(a), the peak PL emission normalized to control remained largely unchanged over a

two orders of magnitude change in pump intensity. This suggests that the PL increase observed was not pump-dependent and must be associated with other mechanisms.

Next, temperature-dependent PL was performed specifically utilizing red- and blue-shift from temperature-tuning to move the peak InGaAs/GaAs QW emission between 920-970nm to probe any wavelength-related extraction-related mechanisms. As seen in Figure 3.10(b), peak PL emission normalized to control was not constant, rather forming two distinct peaks over the range of peak emission achieved by the emitter. Specifically, for room-temperature emission at 960nm, a 1.2x enhancement compared to the floor of the oscillation was observed. More interesting, for emission at 920 and 955nm, a 1.36x enhancement relative to the floor of the oscillation and a total enhancement of 1.6x compared to control, suggesting higher enhancement is possible requiring only minor tuning of growth geometry such as grating pitch and fill factor and/or InGaAs/GaAs QW composition to yield further enhancement at room-temperature. Since the control emitter extraction efficiency remains constant, any differences are suggestive of increased light extraction from the InGaAs/GaAs QW. More specifically, emitter emission that is typically lost to the substrate is instead partially reflected back toward the top surface, increasing net extraction.

While increased light extraction appears to be a primary cause of enhancement in the emitter above embedded 1.4μm pitch gratings, the floor of the oscillation still remained above the normalized control. Since the extrac-

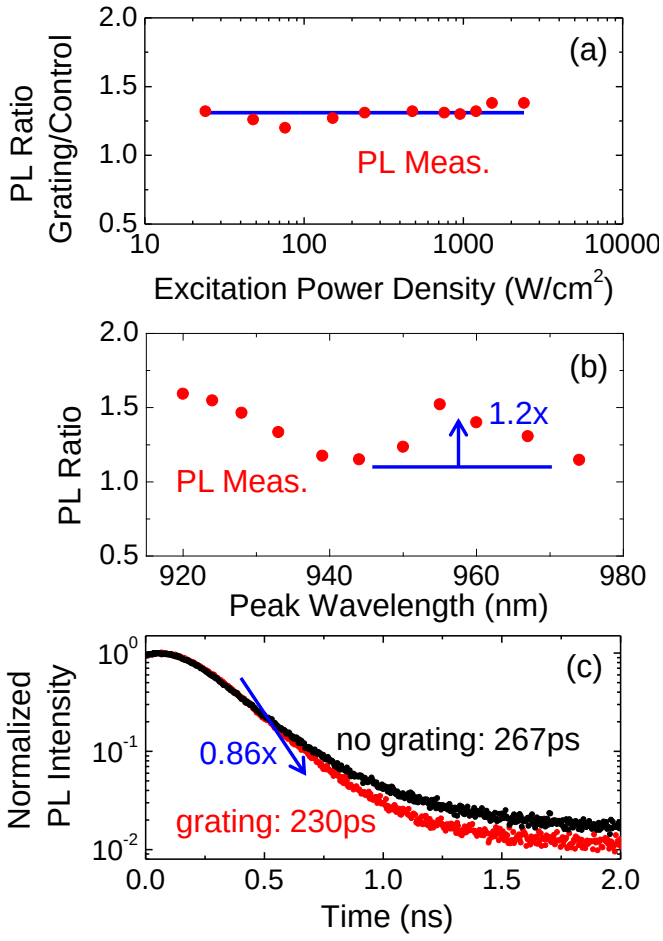

Figure 3.10: (a) Excitation-dependent PL performed on the 1.4μm pitch embedded gratings showed no change compared to control over two order of magnitude of pump-excitation. (b) Temperature-dependent PL (TDPL) performed on the 1.4μm pitch embedded gratings show distinct changes in peak PL compared to control, forming two distinct oscillations, resulting in 1.2x extraction enhancement. (c) TRPL demonstrating 1.16x decrease in carrier lifetime of the 1.4μm pitch embedded gratings compared to control, suggesting a 1.16x Purcell effect as the second component to emitter enhancement.

tion is in part a result of resonance between the top surface and embedded silica gratings, the secondary mechanism of enhancement was likely a weak, but significant Purcell effect. To confirm the presence of Purcell effect, time-resolved PL measurements were performed to estimate the carrier lifetime as seen in Figure 3.10(c). From this analysis, a 1.16x decrease in carrier lifetime was observed in the emitter above embedded 1.4μm pitch gratings compared to grating-free control at the peak emission wavelength at room-temperature. As carrier lifetime is inversely proportional to the localized density of states, this suggests an approximately 1.16x increase in spontaneous emission in the emitter above embedded 1.4μm pitch gratings compared to control. When accounting for the 1.2x extraction enhancement, the net enhancement totals 1.4x, nearly exactly the observed enhancement in peak PL emission of the emitter above the embedded 1.4μm pitch gratings compared to control. Thus, from this PL investigation, it demonstrates for the first time a net enhancement to photoluminescence in single quantum well InGaAs/GaAs/AlAs emitter seamlessly grown directly above embedded silica gratings and marks the most sensitive probe of planar coalescence in any homoepitaxial conventional III-V crystal growth technique. As such, not only does this result provide the pathway for high-quality planar coalescence utilizing all-MBE growth approach, but also unlocks applications requiring the highest level of crystal quality above embedded dielectric microstructures, such as enhanced quantum emitters or low defect III-V heteroepitaxy on silicon.

3.4 Summary

Thus, in summary, we demonstrated for the first time an all-MBE approach to high-quality GaAs planar coalescence over dielectric microstructures. A two-stage growth approach was used, first using III-cyclic PSE growth to form highly selective, (011)-faceted LEO over silica gratings aligned to the [010]-direction, then secondly utilizing continuous MBE growth to achieve planar coalescence. Planar coalescence achieved surface roughness as low as 3nm RMS and optical quality was determined to be equivalent to grating-free controls. Additionally, in demonstration of the high-quality GaAs coalescence, we also presented for the first time an intentionally enhanced single quantum well InGaAs/GaAs/AlAs emitter seamlessly grown directly above embedded silica gratings using the two-stage MBE approach, leading to a 1.4x enhancement in photoluminescence as a result of both Purcell and extraction enhancements. Forward-looking, the presented all-MBE growth approach to planar coalescence marks a significant advance in the long-standing challenge of seamlessly integrating high-quality semiconductor crystal growth with dielectric microstructures, and from this, opens the door to several high-impact applications, including enhanced quantum emitters and embedded metasurfaces as well as an all-MBE approach to heterogeneous III-V integration on silicon.

Chapter 4

Extending High-quality GaAs Planar Coalescence to Embedded High-Contrast Photonic Microstructures

A promising new field that intersects photonics and seamless crystal growth approaches utilizes embedded low-index dielectric structures in high-index direct band gap semiconductors to manipulate light toward the enhancement and improvement of optoelectronic devices. From the two-stage all-MBE growth approach to GaAs showcased in Chapter 3, while promising owing to its high optical quality integration of low-index silica microstructures in GaAs, the growth methodology presented remains largely unexplored within the practical growth space of dielectric microstructures for photonic applications. Thus, in this chapter, we explore and expand the methodology surrounding the two-stage approach to the growth space of embedded low-index microstructures specifically tailored for photonic applications.

4.1 Previous Work in Embedded High-contrast Photonics

An emerging trend in photonics is to utilize embedded low refractive index dielectric microstructures to manipulate light in the design of practi-

cal optical phenomena, such as phase engineering and resonance, toward the enhancement of photonic and optoelectronic devices. Embedded dielectric microstructures are a subset of the general field of high-contrast photonics, which at its core, uses the large difference in refractive index between two or more materials when suitably tailored in the control of optical mechanisms. Historically, high-contrast photonic structures have been relegated to the device periphery for ease of fabrication and device integration [50, 51]. However, as seamlessly integrated photonic circuits become the goal, methods to encapsulate or embed low-index microstructures married with active III-V active quantum structures has become a more recent focus.

Recent effort has demonstrated use of embedded low-index photonic material to enhance photonic and optoelectronic devices using seamless crystal growth approaches. One emerging application is to utilize embedded air voids to increase light extraction in LEDs which is fundamentally limited by total internal refraction [6, 7]. Using low-index voids as backscatters, emission typically lost to the substrate is redirected out the top, increasing the net extraction efficiency. While successfully demonstrated in the III-Nitrides, extending these methods to embedded void formation within conventional III-V materials presents a greater challenge due to fundamental differences between Wurtzite and zincblende crystal structures. Also, a general lack of reports in zincblende self-formed air void formation adds to further limitations.

Another proposed application is using embedded low-index microstructures arranged in 3D and 2D slab photonic crystals schemes to act as a backside

mirrors or resonant cavities to enhance spontaneous and stimulated emission for quantum emitters. The most notable reports are from Noda. et al. where backside embedded 2D photonic crystal slabs are used to create photonic crystal surface emitter lasers (PCSEL) demonstrated in both GaN- and GaAs-based active materials [10]. While promising, the technique is not self-formed in-situ, requiring ex-situ dry etching and regrowth, which is undesirable due to crystal damage and contamination in close proximity to active III-V regions. Also, the air hole formation process requires growth at sub-adatom diffusion length; thus, air holes would not scale accordingly to extend PCSELs to the mid-IR. Thus, a scalable, higher quality option through embedded dielectric structures would benefit the device performance for both near- and mid-IR operation.

Due to the challenging production of embedded dielectric media in III-V crystal growth, many device designs remain theoretical at present. Some interesting applications using embedded low-index microstructures in III-V media include guided mode resonance for embedded optical filters [52], embedded low-index structures for backside perfect all-dielectric broadband mirrors [53, 54], and active III-V emitters coupled to embedded waveguides using an integrated photonic circuit approach [55]. Thus, from the multitude of recent theoretical and experimental reports, it demonstrates the potential impact of embedded low-index microstructures to active III-V optoelectronic devices.

4.2 Two-stage MBE Approach to Tall Gratings

Based on the emerging embedded low-index photonic material previously investigated, it is clear that extending high-quality conventional III-V planar coalescence over embedded dielectric structures tailored for photonic systems can bridge many of the gaps in these recent reports. In starting, we looked to extend the two-stage growth approach to much taller features as illustrated in Figures 4.1(a) and 4.1(b). Specifically, as part of the methodology of the initial investigations all-MBE GaAs growth over silica microstructures, grating thickness were kept thin 25nm in thickness to solely investigate LEO and planar coalescence. While successful in embedded silica microstructures at a high optical quality, from a photonics point-of-view, dielectric gratings at a much greater aspect ratio are needed to fully unlock the design space. For example, to achieve a quarter-wavelength phase change in within an embedded silica microstructure at a commonly used telecom wavelengths, the dielectric structures would need to have a height greater than 250nm, over an order of magnitude taller than the initial investigation thickness. Thus, additional growth exploration is required to determine the growth conditions are needed to achieve planar coalescence over tall dielectric gratings within the two-stage growth approach as well as the optical quality of the coalescence.

4.2.1 Poly-GaAs on 300nm Tall Gratings

While additional growth challenges were anticipated for gratings of higher aspect ratio and height compared to thin gratings, the initial method-

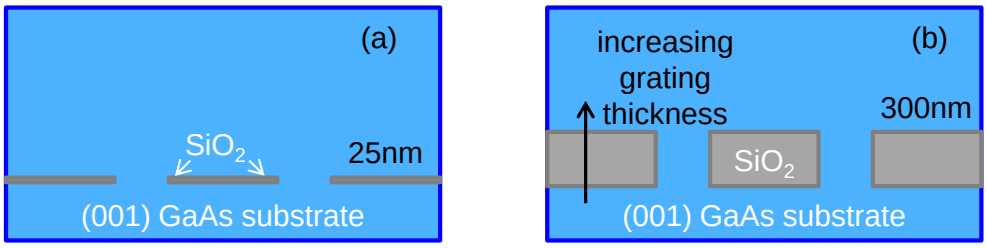

Figure 4.1: An illustration depicting the embedded silica grating thickness increase from (a) the thickness of 25nm used in the initial planar coalescence studies from Chapter 3 to (b) much taller, higher aspect ratio features in this study.

ology used the exact two-stage growth approach as formulated and detailed in Chapter 3. Since this approach already provided high-quality integration over thin gratings, any differences in quality would yield a point of comparison. Thus, to examine the tall grating integration, 300nm thick gratings were fabricated on (001) GaAs substrates. As before, grating pitch and bar width between 1.4-2.2μm, 0.7-1.1μm were varied, respectively, with all gratings maintaining a 50% fill factor. Also, as before, silica gratings were aligned to the $\langle 010 \rangle$-direction since this placement produce the well-faceted (011) LEO and achieving high-quality planar coalescence.

In performing the initial LEO studies over tall gratings, the first departure was observed from the two-stage approach developed for thin gratings. After 180 cycles of PSE-GaAs growth, significant formation of polycrystalline GaAs on silica bars was observed by visually inspection as seen in Figure 4.2(a). This was initially troubling as no GaAs polycrystalline formation was

ever observed to form on thin gratings using the equivalent first stage PSE growth approach.

In search for a reason why polycrystalline GaAs formed on tall gratings as opposed to thin grating, a clue was provided in polycrystalline difference between 0.7μm and 1.1μm bar widths as seen in Figures 4.2(a) and 4.2(b). Specifically, 0.7μm bars yielded a lower density of polycrystalline deposition compared to the wider 1.1μm bars. As such, this difference implies at tall grating heights, Ga surface kinetics are dominated by desorption rather than diffusion owing to the lack of exposed crystal front in the initial stages of LEO to promote site-seed Ga-adatoms on silica. Thus, the wider 1.1μm bars will have a great density of polycrystalline GaAs formation since it is further away from the next crystal front compared to the smaller 0.7μm bars.

4.2.2 High-quality LEO over 300nm Tall Gratings

Thus, to achieve highly selective growth of the LEO over taller gratings, the LEO growth conditions required modification. More precisely, the PSE-based LEO was tailored to promote desorption as a means of selectivity rather than diffusion since desorption is surface dominated phenomena agnostic to the crystal front. To increase desorption in the initial stages, a slower effective growth rate at a slightly higher growth temperature was employed. Specifically, the effective growth rate was lowered by reducing the PSE duty cycle from 50% to 20%, effectively lowering the deposition per cycle from 7ML per cycle to 2.5ML per cycle while also increasing the periodic annealing by

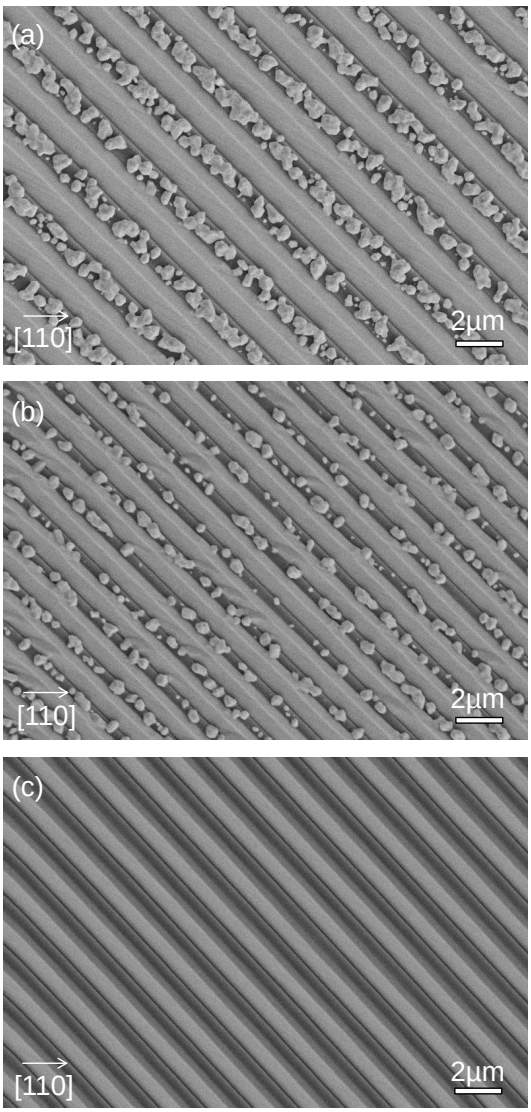

Figure 4.2: Planview SEM image showing polycrystalline GaAs at the top surface of 300nm tall gratings using 50% PSE duty cycle in (a) 2.2 μm pitch gratings and (b) 1.4 μm pitch gratings. (c) Using a slower 20% PSE duty cycle, no polycrystalline GaAs formation was observed as represented in 1.4 μm gratings.

60%.

To examine selectivity under these modified growth conditions, 450 cycles of PSE was deposited at the growth front, equivalent to the deposition from the initial LEO study. Under these tailored PSE growth conditions, high selectivity with silica was achieved using a slower effective growth rate and confirmed by visual inspection as seen in Figure 4.2(c). Also, the LEO formed the equivalent (011)-faceted LEO as observed with thin gratings, enabling use in forming non-planar GaAs template with which to planarize in the second stage.

Thus, the growth can proceed under the two-stage growth approach for thin gratings to achieve high-quality planar coalescence en route to embedded tall, high aspect ratio dielectric gratings. Using the previously detailed tailored first stage, 2μm of continuous growth was employed, resulting in planar coalescence where the complete integration can be seen in the cross-sectional SEM image in Figure 4.3. Here, much larger silica gratings can be seen embedded surrounded by the epitaxial GaAs. Additionally, material quality of planar coalescence was further investigated using AFM and PL, both demonstrating integration at similar levels of surface roughness and PL quality to thin gratings.

While the growth demonstration of embedded silica gratings remains below an aspect ratio of one, it represents over an order of magnitude increase from the thin grating approach, increasing the aspect ratio from 0.04 to 0.4. Also, based on the modification to the first stage, it provides a pathway to

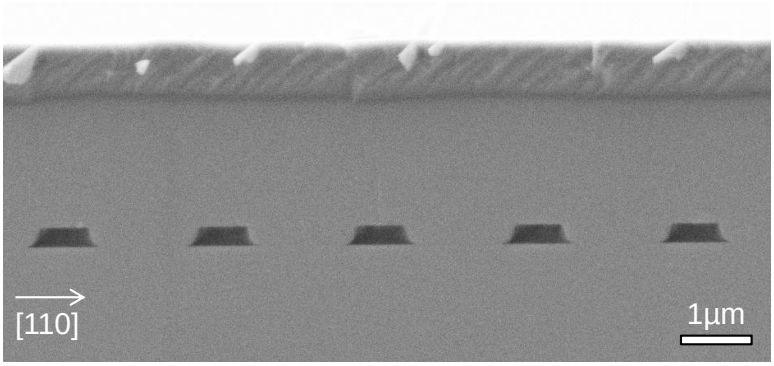

Figure 4.3: Cross-sectional SEM image showing high-quality embedded 300nm tall dielectric gratings in GaAs.

embedded growth of arbitrarily high aspect ratio dielectric microstructures by simply decreasing the effective growth rate. Once the crystal front begins to lateral encapsulate the gratings, a much higher growth rate can then be used for the LEO stage since the gratings act effectively as thin gratings and surface diffusion becomes a more dominant mechanism for selectivity.

4.3 Embedded Silica Gratings as an Etch Mold for Air Channels

With a pathway for the integration of arbitrarily tall embedded dielectric gratings in place, additional photonic design considerations are motivated to achieve the highest index contrast as possible. While silica in III-V semiconductors offer an index contrast between Δn=2-2.5, the highest possible contrast at Δn=2.5-3 is achieved through embedded air microstructures in conventional III-V semiconductors. While an index contrast of 2.5 is often

sufficient, some high-contrast optical phenomena such as broadband mirrors [50] and 2D photonic slabs [56] require the highest contrast possible to achieve the desire phenomena, such as complete photonic band gaps. Thus, increasing the contrast of embedded dielectric structures to the maximum allowable by natural law is a desirable outcome.

Motivated by an increase to embedded index contrast, the generation of air gratings or air channels in conventional III-V materials of an arbitrary morphology and scale becomes possible with the recent demonstration of large embedded dielectric gratings. As illustrated in Figure 4.4, essentially using the silica gratings as a mold, the silica acts as a placeholder for air, initial embedded through the high-quality two-stage growth approach. Then leveraging a highly selective wet etch, the removal of the silica grating leaves behind an air channel in its place, thus producing an embedded air/semiconductor grating at the highest contrast.

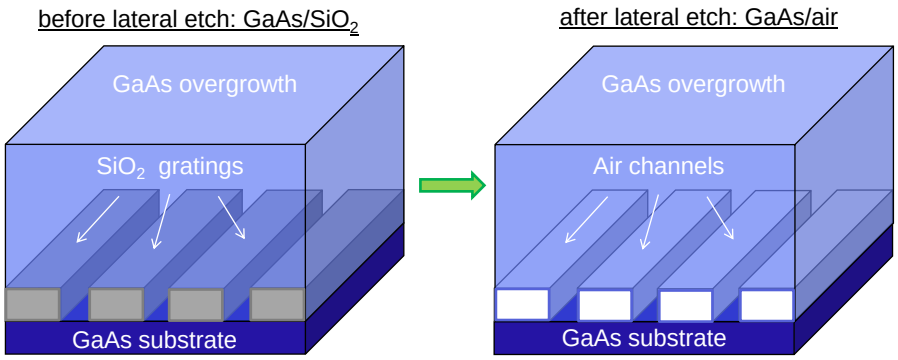

Figure 4.4: Using embedded silica gratings as a mold (left), a highly selective lateral etch can leave behind air channels for the purpose of increasing the index contrast for high-contrast photonic applications.

In pursuit of this goal, we recently demonstrated the high selective etch removal process of embedded silica gratings, creating embedded air channels [1]. By creating large 5-200μm defined mesas etched back into the overgrown GaAs, the embedded silica gratings can be re-exposed as a means to provide access to a wet etchant. Buffer oxide etch (BOE) was chosen wet etchant as BOE is highly selective to GaAs as well as provides a buffer agent to prevent the primary etchant hydrofluoric acid from becoming diffusion limited in the silica channels, important since the silica gratings have relatively small cross-section, 0.3x1.1μm at its largest. Using the BOE soak up to 8 hours in duration, the complete removal of silica within the defined mesas including the largest investigated at 200μm. As such, the lateral etch rate was estimated to be 200nm/min with the etch rate slightly reduced as the lateral etch progressed through the larger mesas.

From the mesa side walls, confirmation of the removal of silica gratings was determined using visual inspection from the cross-sectional SEM image as seen in the defined mesas of Figure 4.5, where embedded air channels can be seen. Also, as more sensitive probe, confirmation of silica removal in the center of the mesa was achieved using the phonon resonance absorption of silica as an indicator. Using FTIR analysis, the reflectance spectra of the embedded silica grating before and after their removal can be seen in Figure 4.6. Specifically, the absorption feature seen near 1000 cm^{-1} in wavenumber

[1] the complete methodology of silica etch removal in embedded III-V semiconductors will be reported in a future Master thesis by Alec M. Skipper. Only an executive summary of the methodology and results is provided here.

previously indicating the presence of embedded silica from the center of a mesa was seen to be removed after etch, implying complete removal throughout the entity of the mesa.

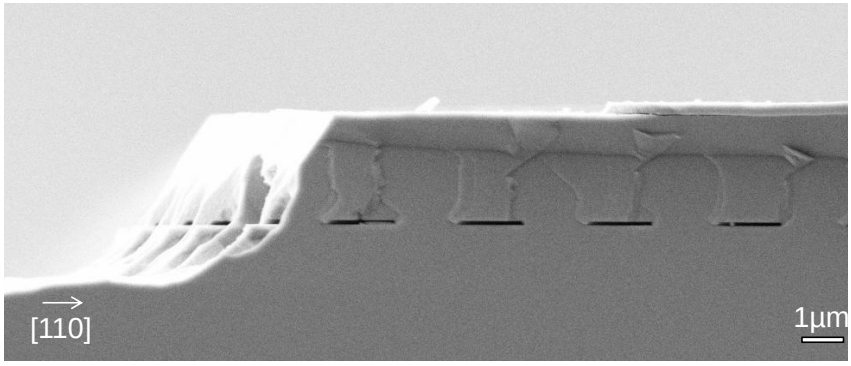

Figure 4.5: Cross-sectional SEM image of a GaAs mesa with air channels formed by the etch removal of the silica gratings originally encapsulated from the two-stage MBE approach to planar coalescence.

Additionally, other features of increased index contrast were observed in reflectance between the post-etch air channels and pre-etch silica gratings. As seen in Figure 4.6, a slight increase in the minimum and maximum reflectance as well as a slight phase shift in near-IR portion of the reflectance (between 7000-8000 cm^{-1} in wavenumber) can be seen, consistent with an index contrast increase. Thus, from this investigation, the etch removal of silica gratings was confirmed, effectively using silica as a etch mold in the creation of air channels. Thus, with the addition of the etch removal process, it unlocks an even wider photonic material design space with which both tailored geometry and index contrast in the design for embedded high-contrast grating for photonic and optoelectronic applications can be achieved.

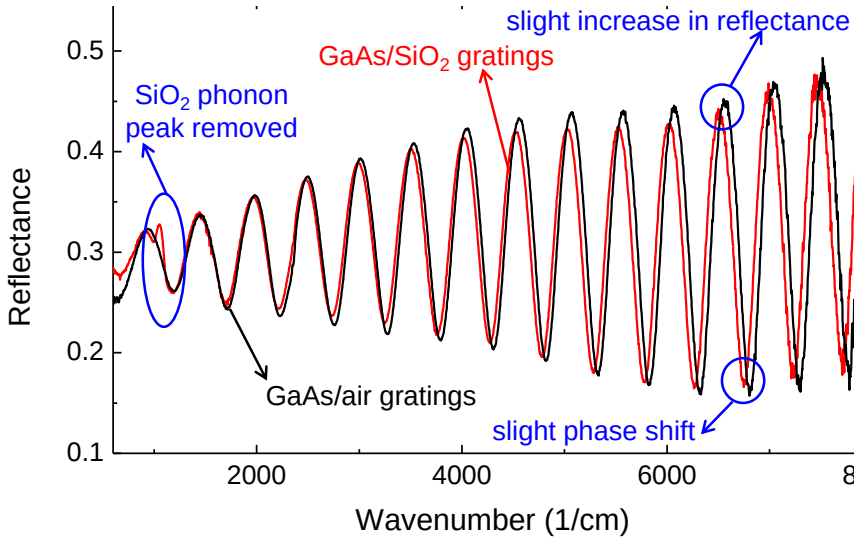

Figure 4.6: Reflectance spectra of before and after of silica etch removal. Slight changes in the reflectance are all indicative of complete silica removal in 200μm width mesas.

4.4 Embedded High-contrast Distributed Bragg Reflector (DBR)

As an example of how embedded dielectric gratings can improve optoelectronics device performance, a proposed application is improving backside DBRs performance in VCSELs. While a great deal of attention has been given to improving top side DBRs, notably using suspended high-contrast gratings to produce thin, tunable broadband all-dielectric mirrors [50], top side DBRs can be fabricated completely outside the growth environment. However, backside DBR improvement has historically remained a challenge since active III-V emitters must grown above the backside DBRs. Thus, any novel alterative to backside broadband mirror structures must also incorporate, seed, and/or

transfer active III-V grown layers at a high optical quality. Further motivation is provided from traditional all-III-V DBRs applied to mid-IR VCSELs, which require greater than 6 microns of growth to achieve 99.5% reflectance [57], producing not only a growth challenge but also causing a significantly reduction to thermal conductance, degrading VCSEL performance.

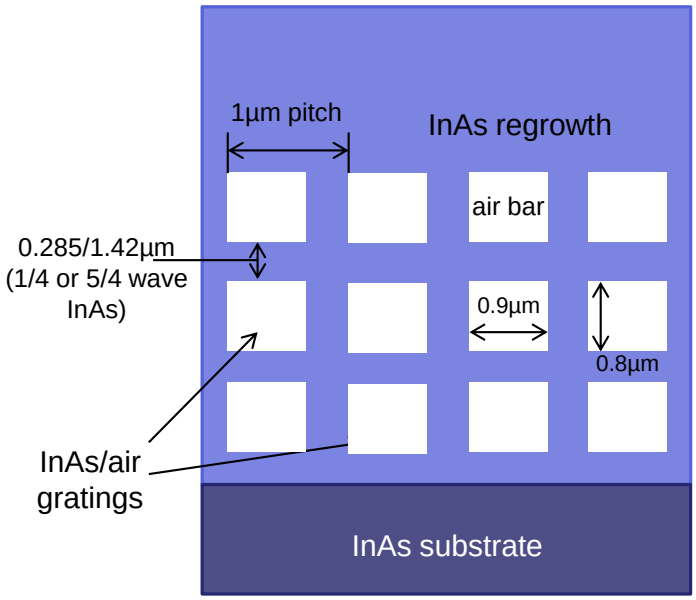

Figure 4.7: Illustration of an III-V/air high-contrast DBR tailored for use in the mid-IR.

Utilizing both the two-stage growth approach for high aspect ratio silica gratings and molded silica removal process to form embedded air gratings, a backside DBR replacement is proposed using stacked air/III-V embedded gratings as seen in Figure 4.7. Using a grating pitch scaled below the III-V medium effective wavelength, subwavelength air/III-V gratings effectively act as a low-index layer with the effective low-index scaling by the fill factor of

the air within the grating. Thus, when stacked in either quarter or five-fourth wavelength layers under a traditional DBR low-index high-index periods, the staggered media act effect scheme, only three layer stacks are needed to achieve 99.5% reflectance as seen in Figure 4.8.

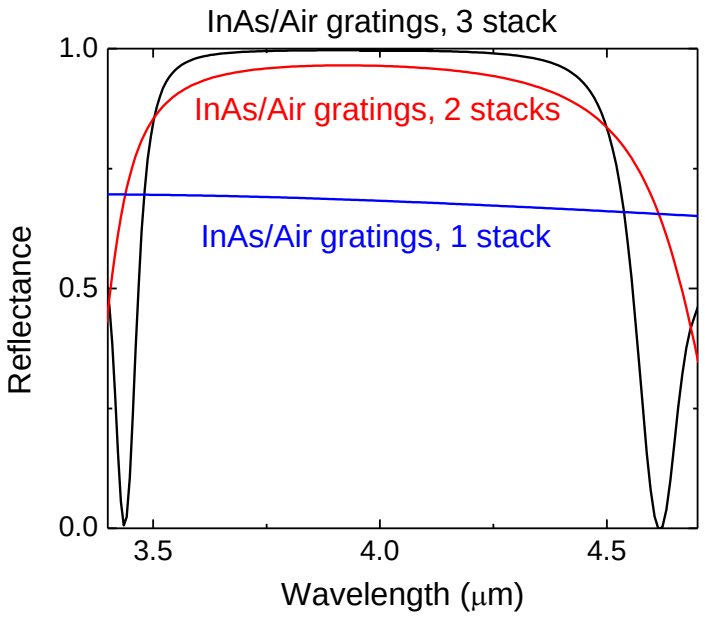

Figure 4.8: Increasing the number of InAs/InAs-air periods dramatically increased the peak reflectance. A total of 3 stacks is all that is needed to produce a broadband all-dielectric mirror with 99.5% reflectance.

When compared to a conventional entirely III-V based DBR, the increase in index contrast from 0.6 to 2.6 in the high-contrast DBR produces several performance benefits as seen in Figure 4.9. While the high-contrast DBR produces backside broadband reflection, the increase contrast achieves 2-3x increase to reflectance bandwidth compared to all-III-V mid-IR sourced DBRs at the same 99.5%. In addition, the high-contrast DBR reduces the

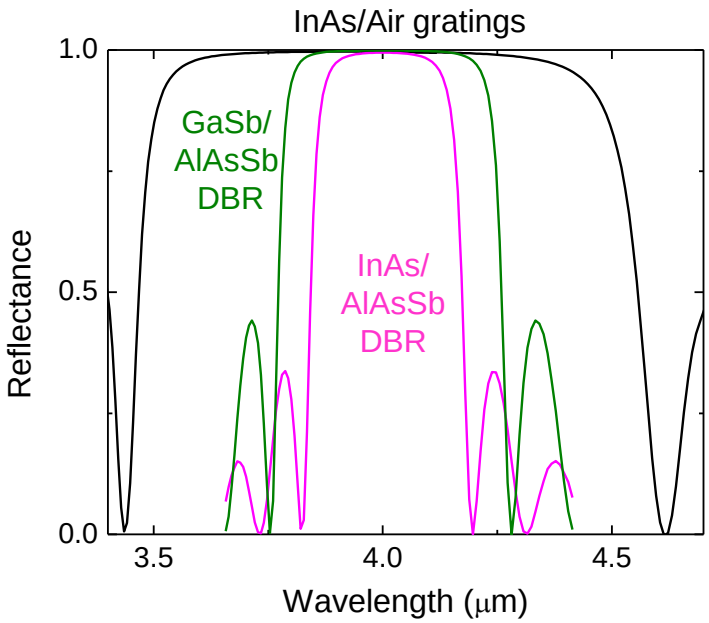

Figure 4.9: The high-contrast DBR exceeds the reflectance bandwidth by over 2-3x compared to conventional all-III-V DBRs while also achieving it at much thinner stack heights.

total growth thickness to a few microns compared to greater than 6 microns, improving thermal conductance. Also, while more computational optimization of the high-contrast DBR is required, importantly it demonstrates a potential optoelectronic application where embedded dielectric microstructures can improved device performance in an integrated epitaxial approach.

4.5 Air Void Formation above Disc Arrays and off-[010] Gratings

Based on the success of the two-stage all-MBE growth approach of embedded [010]-aligned silica gratings, a broader investigation into general

dielectric integration was explored. Since this initial investigation was tailored around gratings solely aligned to primary crystal planes, it left an open question of the quality of growth integration for alternatively shaped dielectric microstructures, such as off-aligned gratings or non-grating-like dielectric structures like discs. While motivated by embedded structures like photonic crystal slabs, a broader study would have more utility in understanding and modeling the growth mechanism within the two-stage growth approach at-large.

4.5.1 GaAs LEO over 1.4μm Disc Arrays

As a starting point, we looked to investigate the two-stage growth approach on disc arrays on GaAs. Motivated by recent work in PCSELs [10], the investigation started with the growth exploration of disc arrays. More specifically, 1.4μm diameter silica disc arrays were patterned on (001) GaAs arranged in a 1.9μm hexagonal lattice as seen in Figure 4.10. As before, the disc thickness were kept thin to solely focus on LEO and planar coalescence within the two-stage approach. In starting the investigation of LEO growth over the pattern disc arrays, identical growth conditions of the first stage LEO as detailed in Chapter 3 were used. To examine LEO, 270 cycles of PSE was performed under the same growth conditions previous reported and the resulting LEO visually inspected using planview and cross-sectional SEM as seen in Figure 4.11.

From visual inspection, a clear departure of growth morphology of sil-

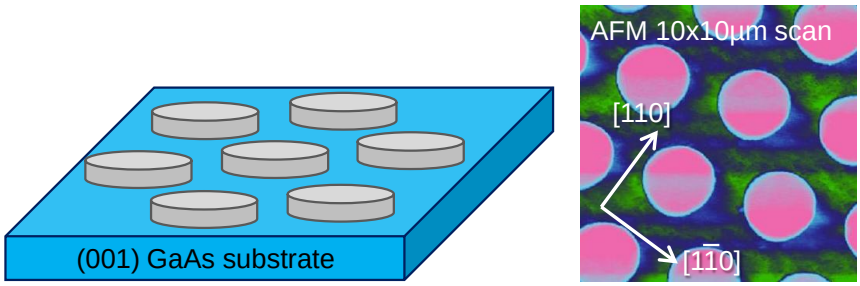

Figure 4.10: 1.4 μm silica disc arrays were patterned on (001) GaAs to initially explore non-grating-like embedded dielectric using the two-stage apporach.

ica patterned as observed, specifically in non-"wetted" lateral growth over the silica discs, greatly differing from gratings aligned to primary crystal directions forming only "wetted" lateral growth. Thus from this initial study, the lateral growth as it progress over the silica disc formed a partially faceted void with a non-coalesced portion forming a distinct "skylight." Thus, based on these initial lateral growth observations, the investigation into planar coalescence over disc arrays was bifurcated to examining the following two questions: (1) will continued lateral growth under a PSE approach produce lateral coalescence, effectively closing the "skylight," allowing for the air void above the silica disc to be encapsulated and (2) why are air voids present above disc arrays when only "wetted" growth to gratings was observed?

4.5.2 Lateral Coalescence over 1.4μm Disc Arrays

In examination of the first question, lateral coalescence and air void encapsulation over the silica disc array was the primary goal. In pursuit of lateral coalescence, 540 cycles of PSE was performed determine if lateral coa-

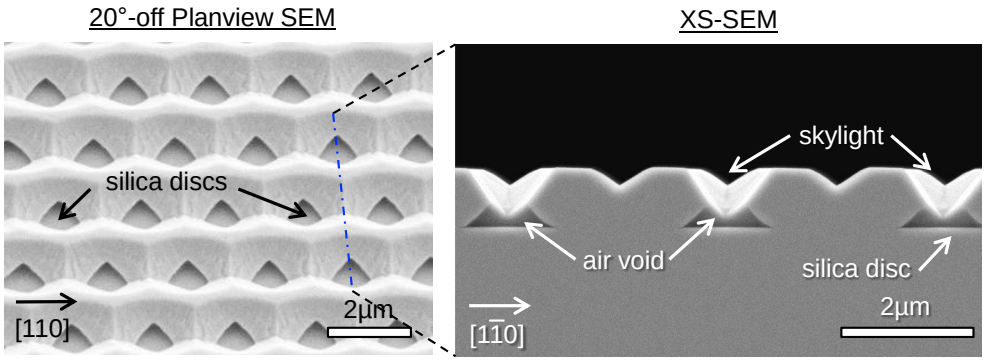

Figure 4.11: Non-"wetted" LEO over the silica discs was observed, producing partially formed air voids over the silica discs with an non-coalesced portion forming a distinct "skylight."

lescence would occur using an entirely PSE approach. From visual inspection of cross-sectional SEM as seen in Figure 4.12, complete lateral coalescence was identified, effectively encapsulating the air void above the disc and closing the "skylight." The encapsulated air void appeared to be well-faceted as seen in Figure 4.12(a). In addition to air void encapsulation, the disc array was also effective embedded in GaAs. From planview SEM as seen in Figure 4.12(b), lateral coalescence was anisotropic. Overlaying the original disc array template, lateral growth was highest toward the [1$\bar{1}$0] direction, and as stated previously, this was to be expected as lateral growth in MBE-grown GaAs in preferred along the [1$\bar{1}$0] direction.

4.5.3 Planar Coalescence over 1.4μm Disc Arrays

With well-faceted lateral coalescence occurring over the disc array, the second stage of the two-stage approach could be investigated, using continuous

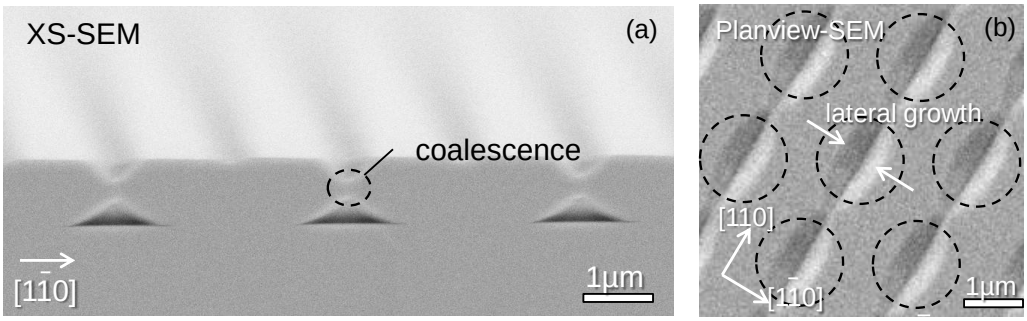

Figure 4.12: (a) Lateral coalescence occurred when increasing the number of PSE cycles to 540. (b) Lateral coalescence was observed to be anisotropic, preferring growth along the [1$\bar{1}$0] direction, consistent with MBE growth kinetics.

growth to produce planar coalescence. In pursuit of planar coalescence, equivalent growth conditions to the second stage were utilized as previously reported in Chapter 3, using 0.5μm/hr GaAs growth with As_4/Ga 45x BEP ratio at 570°C. Due to the shallow valleys after lateral coalescence, planarization occurred rapidly, only requiring less than 1μmm of continuous growth to achieve planar coalescence. The resulting planar coalescence over the embedded disc arrays including the encapsulated air voids is seen in the cross-sectional SEM images of Figure 4.13. Noting that both images at the same scales, the void density is different since the hexagonal array density differs with alignment along the primary cleaving directions [110] and [1$\bar{1}$0], respectively.

Further investigation into material quality of the planar coalescence was also performed with using AFM and PL as seen in Figure 4.14. Specifically, 3.5nm RMS surface roughness was achieved above the embedded disc arrays, similar to roughness occurring in the [010]-aligned grating which achieved

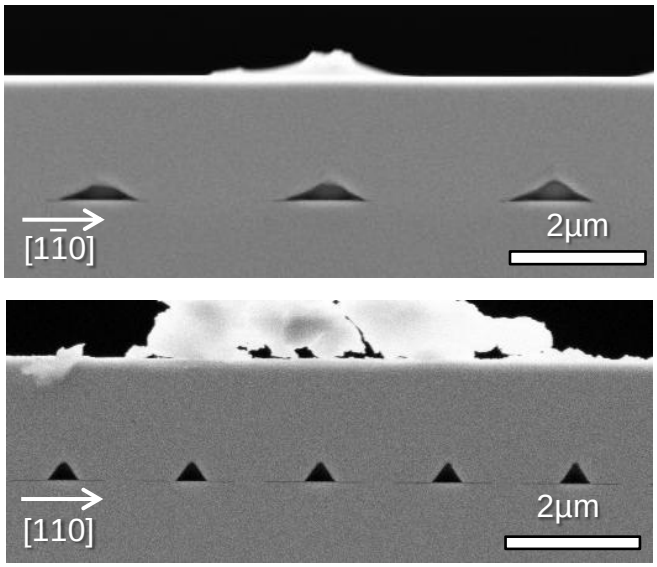

Figure 4.13: Cross-sectional SEM images showing the completed modified two-stage approach to embedded disc arrays. As a consequence of the process, self-formed air voids were produced above the silica disc arrays.

3.2nm RMS roughness for the smallest 1.4μm pitch gratings. Residual periodic peaks in the surface image scans correlate with the original disc array template. While the surface roughness is low, further roughness reduction can be achieved using additional continuous growth and/or use of a growth surfactant such as Bi [48, 49]. Additionally, PL of the bulk GaAs planar coalescence was measured at room-temperature and no significant difference in PL intensity of the planar coalescence compared to disc-free controls was observed. A slight red shift was observed in the embedded disc arrays; however, this likely to due to a slight increase in light extraction due to the micron-scale air voids acting as backscatters, which would occur on the red side of bulk emission since light

below the band gap would be less sensitive to re-absorption.

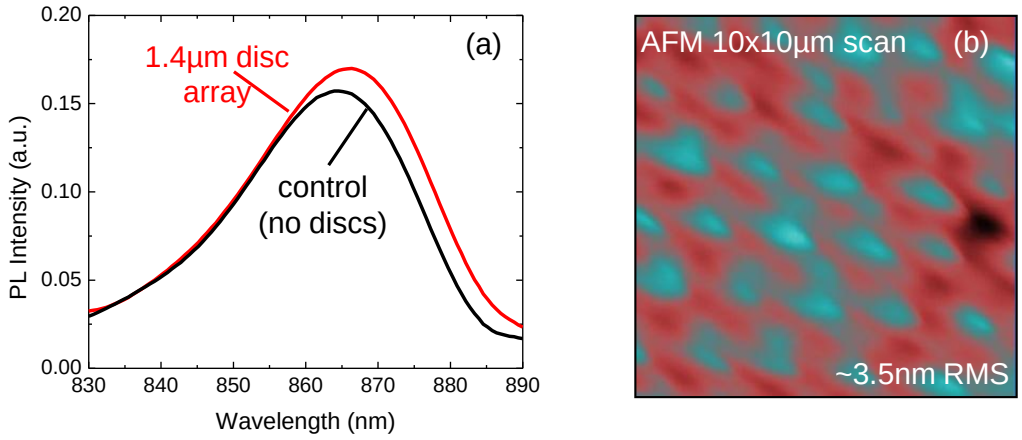

Figure 4.14: (a) Peak PL intensity of the GaAs planar coalescence bulk response over the embedded disc arrays with encapsulated air voids is comparable to disc-free GaAs control. (b) Planar coalescence achieve low surface roughness, approximately 3.5nm RMS roughness.

Interestingly, it is slightly remarkable that the bulk response is close to control given the presence of air voids without wide band gap carrier blocking layers preventing carrier drift to the air voids. One may suggest a reduction in bulk PL since the air voids above embedded disc could potentially add surface states. However, the generation of surface states does not appear largely due to limited oxidation of the air/GaAs interface since their complete encapsulation through coalescence occurring in the UHV-MBE environment. Thus, including the low surface roughness results, the planar coalescence of embedded disc array include air voids appears to be at similar optical quality as the two-stage growth approach when applied to [010]-aligned gratings.

4.5.4 Coalescence over Off-[010] Gratings

While the two-stage growth approach was successful in producing high-quality the planar coalescence over silica disc arrays, the formation of well-faceted air voids departs from the initial investigations in gratings which showed only "wetted" lateral growth. This is perplexing as the lateral growth over disc arrays sample from all crystal directions unlike gratings which sample from a few direction. It follows then if air voids form above disc arrays while also achieving planar coalescence, then there must also be some grating alignments which produces air voids over the gratings while also achieving planar coalescence.

In searching for air void formation above gratings, off alignments from the primary crystal directions were identified as the likely growth space. In particular, gratings off-aligned from the [010] direction toward the [110] were mostly likely to form both air voids an planar coalescence as lateral growth was observed in grating aligned to these primary direction directions. Thus, to hunt for air void formation, thin silica gratings were patterned on (001) GaAs, aligned in 5$\circ$ increments off the [010] direction toward the [110] direction and first stage PSE lateral growth was performed as previously reported in Chapter 3.

From this initial lateral growth study, another large departure in LEO morphology was observed as seen in Figure 4.15. Specifically, gratings aligned off the [010]-direction toward the [110] formed "non-wetted" inverted mesa type LEO significantly different than the "wetted" LEO across the silica grat-

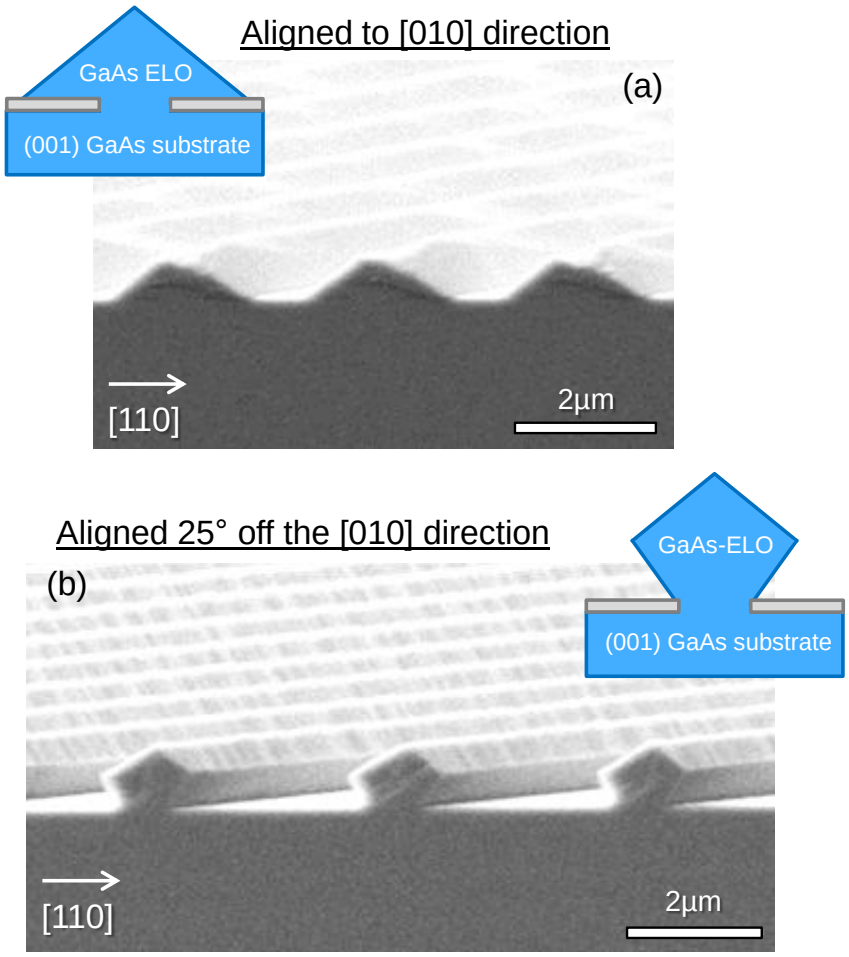

Figure 4.15: (a) (011)-type "wetted" LEO occurs across [010]-aligned gratings. (b) However, non-"wetted" growth forming an inverted mesa type LEO forms in off [010]-aligned gratings toward the [110]-direction.

ing when aligned to the [010]-direction. Since the inverted mesa type LEO observed was well-faceted and progressed over the gratings, the modified two-stage growth approach developed for disc arrays was applied to the off-[010] aligned gratings. Specifically, the first stage used 540 cycles to achieve lateral

coalescence, then transitioned to the second stage growth using continuous growth to produce planar coalescence.

The resulting integration using the modified two-stage approach produced planar coalescence in gratings aligned between 5-25° off the [010] direction toward the [110] direction as seen in Figure 4.16. Like the embedded disc arrays, embedded off-oriented gratings also formed well-faceted encapsulated air voids above the silica gratings. Interestingly, air void facet planes differed, increasing in angle as the alignment moved further away from the [010]-direction. Specifically, for gratings aligned 5° off the [010], (011) plane emerged in the encapsulated air void. However, as the gratings became closer in alignment with the [110] direction, void angle steepened. When the off-aligned gratings reached 25° from the [010] (20° from the [110]), the air void facet planes completely changed from (011) to (111)A planes. Thus, not only were air void formation confirmed above gratings as anticipated, but also offered some degree of tunability in void angle, using grating alignment between the [010] and [110] directions.

From an material quality perspective, the surface and optical quality of the planar coalescence of embedded off-aligned gratings was equivalent to both embedded disc arrays and [010]-aligned gratings as previously investigated. Specifically, surface roughness of the planar coalescence varied between 3-6nm RMS was achieved, equivalent to both embedded disc arrays and [010]-aligned gratings. Also, PL of the bulk GaAs planar coalescence, measured at room-temperature remained comparable to grating-free GaAs controls, only

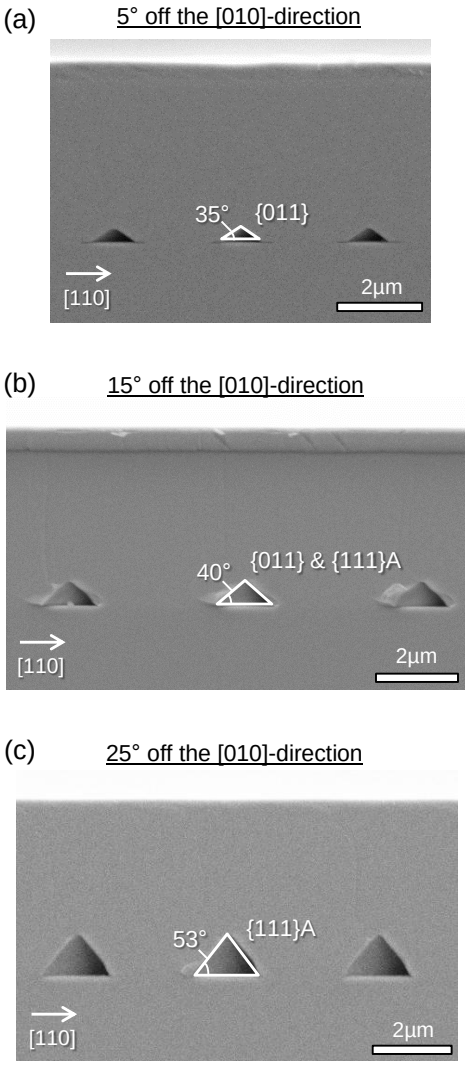

Figure 4.16: Using the two-stage growth approach, off [010]-aligned grating were embedded forming encapsulated air voids above the silica gratings. (a) Gratings aligned 5° off the [010], (011) faceted air voids emerged. (b) Gratings aligned 15° off the [010], a mixture of (011) and (111)A faceted air voids emerged. (c) Gratings aligned 25° from the [010] (20° from the [110]), entirely (111)A faceted air voids emerged.

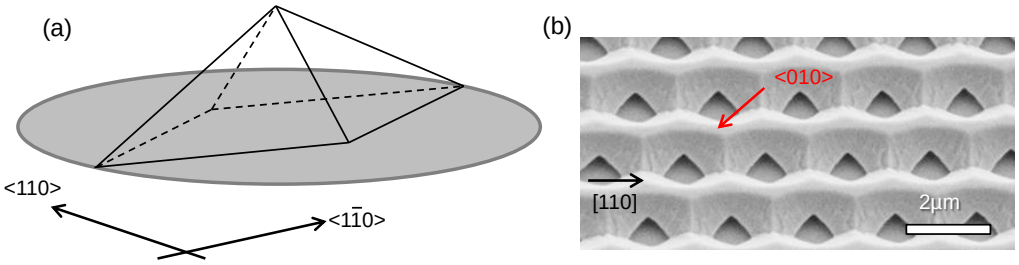

Figure 4.17: (a) Revisiting the air void above silica disc arrays, the void shape appears to form a rhombic pyramid as a first order approximation. (b) Also, lateral growth is dominate along ⟨010⟩ directions, all of which is unsurprising given the recent findings of air void formation and planar coalescence over off [010]-aligned gratings.

producing minor degradation for gratings aligned 25° from the [010]-direction. Thus, through the two-stage growth approach, encapsulated air voids above off [010]-aligned gratings produced high-quality planar coalescence.

In light of the self-formed air voids above off [010]-aligned gratings, the air voids formation over the embedded silica disc arrays is no longer a surprise, but rather an expectation. In reexamining the LEO over the disc arrays as seen in Figure 4.17, it is clear that the lateral growth is most dominate along the ⟨010⟩ directions, as would be predicted from the lateral growth investigation over off [010]-aligned gratings. Also, as the disc array sample lateral growth from all crystal directions, it is no surprise to observe the dominate LEO along ⟨010⟩ including the off-alignments, which all achieve lateral and planar coalescence. However, since the off-alignments in gratings maintain a degree of air void formation in its coalescence, planar coalescence over disc array necessitate that it also forms an air void. Thus, looking more closely at the

air void facets, (111)A and (11n)B facets are clearly identified along with significant "wetted" LEO along the $[1\bar{1}0]$ direction. Using the SEM imaging as a first order approximation, air void volume is estimated to be a rhomboidal pyramid, although more accurate description would include some curvature to account for (011) and (111) plane mixing.

4.6 Summary

From these collective results, the two-stage all-MBE approach to planar coalescence was modified and extended to achieve high-quality planar coalescence over a wide range of embedded dielectric microstructures specially suited toward high-contrast photonic applications. Specifically, tall, higher aspect ratio dielectric gratings were embedded using decreased LEO growth rate. Then, using the silica gratings as a mold, highly selective wet etch was shown to remove the silica, producing embedded air channels and achieving the highest index contrast ratio gratings embedded III-V media. Lastly, in extending the two-stage approach to embedded disc arrays, self-formed air voids were observed above silica discs. Modifying the two-stage growth approach enabled full encapsulation of the air voids and achieving planar coalescence at a high optical quality above the air voids. Also, in explanation of the self-formed air voids above disc arrays, air void formation was identified above off-[010] aligned gratings, providing a general growth model for embedded dielectric microstructures within the two-stage growth approach.

Chapter 5

An All-MBE Growth Approach to Epitaxial Lateral Overgrowth Metamorphics

Historically, the primary driver of investigation into high-quality lateral growth is the utilization of embedded dielectric microstructures as interfaces for dislocation blocking in relaxed metamorphic heteroepitaxy. As before, metamorphic integration of embedded dielectric microstructures was exclusive to MOVPE and LPE crystal growth techniques which only until recently had success in producing planar coalescence in high mismatch films. However, with the success of the all-MBE approach to planar coalescence over embedded dielectric microstructures, in this chapter, we extend the two-stage growth approach to relaxed metamorphic integration. Specifically, using InAs/GaAs as test system, we demonstrated for the first time material quality improvements including a nearly 3x reduction in dislocation density and 50% increase in PL through an entirely MBE growth approach.

5.1 Previous Work in Epitaxial Lateral Overgrowth Metamorphics

One the primary challenges of high lattice mismatch metamorphics is achieving low defect substrate invariant growth, particular motivated for the

growth of commonly used direct band gap III-V semiconductors such as GaAs, InP, and InAs and their alloys on silicon substrates. As frequently repeated goal, high-quality III-V heterogeneous integration on silicon is an ultimate target as large scale CMOS processing can lead to a whole array of low cost, high performing direct band gap III-V devices on silicon with pathways leading to monolithic fabrication of integrated photonic circuits. While highly motivated, direct band gap III-V engineering is limited to the reduced lattice constant of silicon, only permitting lattice-matched conditions to indirect band gap $Al_xGa_{1-x}P$, important, but limited in use. Thus, the wide range of high lattice mismatch of direct band gap $In_xGa_{1-x}As_yP_{1-y}$ alloys must be grown as a relaxed layer, which inevitably generates defects, notably threading dislocations which propagate in the vertical direction toward the episurface, typically referred as the device region as illustrated in Figure 5.1(a).

With high-quality heterogeneous layers as the goal, one of the primary objectives of relaxed high lattice mismatch metamorphics is to reduce threading dislocation densities in relaxed films within the device region. While a great deal of progress has been made to relaxed a wide array of binary high lattice mismatch III-V alloys on Si and GaAs substrates as reviewed in Figure 5.1(b), the common trend is the generation of exceedingly high densities of threading dislocations, greater than 10^8 cm^{-2} even with thick buffer layers are employed. This is particularly troubling as threading dislocation densities below 10^5 cm^{-2} are typically needed for reasonable performance of light emitting and detecting devices utilizing direct band gap III-V materials, several orders

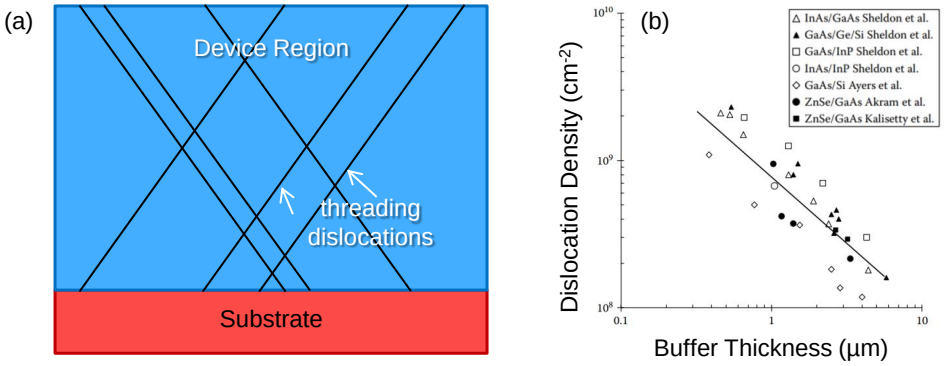

Figure 5.1: (a) Basic illustration of high lattice mismatch metamorphics which when relaxed generates threading dislocations that propagation into the device region. (b) Common among several high lattice mismatch III-V material systems is the generation of exceeding high threading dislocation densities Adapted from [1] .

of magnitude above simple thick buffer layer schemes. Thus, for the practical growth of direct gap III-V materials on silicon and GaAs, additional methods must be employed to further reduce dislocation densities in relaxed III-V high mismatch buffer layers.

Several growth methods to reduce threading dislocation propagation in relaxed metamorphic buffer layers have been proposed such as graded buffer layer schemes [58, 59], strained superlattice dislocation filters [60, 61, 62], and compliant substrates [63, 64]. One technique that has shown great promise with high lattice mismatch metamorphics is epitaxial lateral overgrowth heteroepitaxy or ELO as it is commonly abbreviated [1]. In the ELO technique as

[1]The heteroepitaxial growth technique abbreviated as ELO has many names and abbreviations which can make reading the literature quite confusing. For example, the vast

illustrated in Figure 5.2, patterned dielectric microstructures, typically using SiN_xO_{1-x}-based gratings or meshes, block threading dislocation propagation at a former growth front while also incorporating periodic openings commonly referred to as windows to seed LEO across dielectric microstructures. As such, performing high-quality LEO produces regions directly above the dielectric microstructures with limited threading dislocations, ideally only threading dislocations placed near the seed window openings continue propagation. Resolving the growth to coalescence (ideally planar coalescence) results in a net reduction in threading dislocation density in the device region.

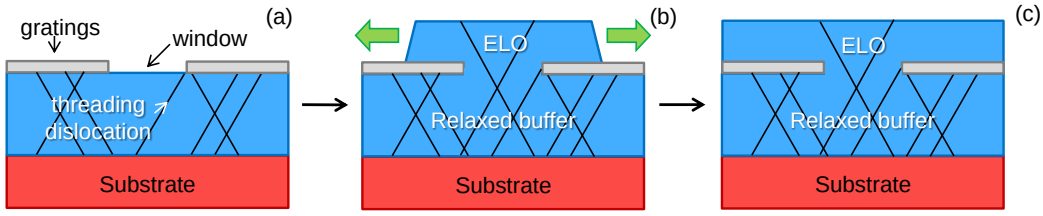

Figure 5.2: Flowchart of ELO metamorphics begins with (a) initially relaxing a high lattice mismatch buffer layer on a substrate and ex-situ patterning dielectric gratings or meshes at the top surface to block dislocations at this interface. Then, (b) seeded lateral growth across the dielectric microstructures embeds the dielectric pattern, and (c) the growth continues until coalescence, ideally resolving the lateral growth into planar coalescence.

ELO metamorphics as described here is not the only embedded dielectric technique used for a dislocation blocking. The notable difference is aspect

majority of the LPE-ELO work is coined microchannel epitaxy or MCE for short by Nishinaga et al.. In this thesis, to keep terminology unified, we will refer to the lateral growth process as LEO, but the entirety of relaxed mismatched heteroepitaxial growth process as ELO.

ratio trapping (ART) [12, 65], which utilizes patterned high aspect ratio fins to block dislocation propagation at the vertical dielectric interface as opposed to ELO which uses horizontal patterns at low aspect ratios to block dislocation propagation. The difference between ELO and ART is best visualized in Figure 5.3. While both techniques can be highly effective, ART benefits from integration in a single epitaxial growth step with the challenge of fabricating tall dielectric fins at a very high aspect ratio using unconventional nano-patterning whereas ELO has relatively straightforward conventional micron-scale dielectric grating fabrication but requires at least two separate growth steps. Going forward, in this chapter, we solely focus on the ELO technique.

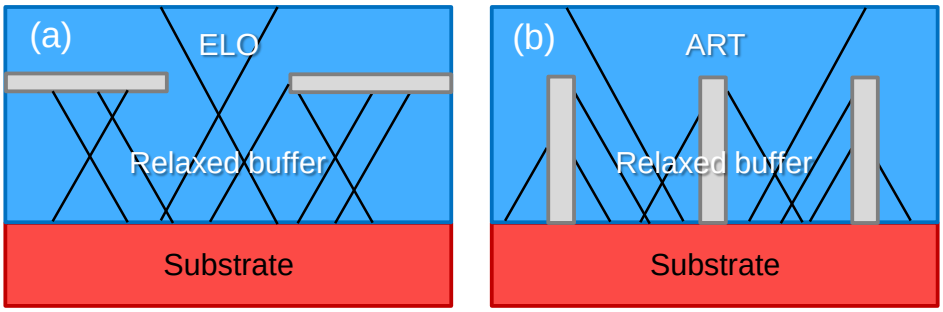

Figure 5.3: Within the embedded dielectric heteroepitaxial growth space, (a) ELO uses lateral dielectric interfaces to block dislocations whereas (b) ART differs by using vertical fins.

As addressed throughout the previous chapters, the challenges associated with achieving ELO (with LEO and coalescence in general) is specific to crystal growth techniques. As such, ELO metamorphic integration within crystal growth closely mirrors the success with homoepitaxial dielectric integration, previously demonstrated within MOVPE and LPE crystal growth

techniques. First metamorphic demonstration of ELO was performed by LPE with the growth on GaAs on (111) silicon substrates, and later on InP on (001) silicon substrates [66, 67]. While successful at producing significant LEO with low defect density above dielectric regions and demonstrating III-V/silicon integration, the entire growth process was not entirely achieved by LPE, instead using MBE growth to relax the initial III-V buffer layer on silicon, then using LPE for the lateral growth steps. Also, unlike the homoepitaxial LPE growth which demonstrated planar coalescence, no lateral or planar coalescence in LPE ELO was reported.

More recently, MOVPE has been widely applied to ELO metamorphic III-V systems [16, 68], including the first demonstrations ELO III-V planar coalescence on silicon substrates [69]. A more in depth approach was provided by Bowers et al. using homoepitaxial InP a comparative control. From this methodology, ELO planar coalescence was identified as high-quality without added defects, identifying the origination of stacking faults from the initially relaxed buffer layers.

Based on the high-quality dielectric integration demonstrated in Chapters 3 and 4 with the growth of homoepitaxial GaAs on (001)-oriented substrates over a wide array of dielectric microstructures, it stands to extend the two-stage all-MBE growth technique to a high lattice mismatch heteroepitaxial system differing from GaAs as such an investigation has potential multifactorial benefits. Foremost, examining the two-stage all-MBE growth approach to planar coalescence in a second III-V binary alloy would demonstrate the

general applicability of the two-stage growth approach rather than its specific use to GaAs. Additionally, an investigation into planar coalescence to high mismatch heteroepitaxy in any material system through the two-stage method potentially broadens its use to ELO and more notably would represent only the second III-V crystal growth technique to achieve planar coalescence within the ELO approach. Forward looking, successful high-quality high lattice mismatch heteroepitaxy would firmly unlock MBE growth as a viable ELO crystal growth technique and establish a new platform through which seamless all-MBE heterogeneous integration can be explored.

5.2 Two-stage Approach for MBE ELO Metamorphics

With an entirely seamless all-MBE approach to high mismatch ELO utilizing the two-stage approach motivated, a test material was identified as InAs/GaAs for several reasons as seen in Figure 5.4(a). As InAs must first be relaxed on (001) GaAs prior to any InAs-LEO, it is most simply achieved using a predominately MBE growth technique known as interfacial misfit dislocation arrays or IMF as it is commonly abbreviated as seen in Figure 5.4(b). In general, the IMF technique is able to nearly complete relax high lattice mismatch layers at an interface through the formation of periodically spaced edge dislocations under tailored growth conditions [2, 70]. Looking toward lateral growth stages, InAs also has high promise for planar coalescence as since In-adatom diffusion on silica is equivalent to Ga-adatoms and maintains the same group-V through As_4, creating a high chance of success of transferring

the two-stage approach from GaAs to InAs with only minor anticipated adjustments to the growth conditions, such as growth temperature and growth rate.

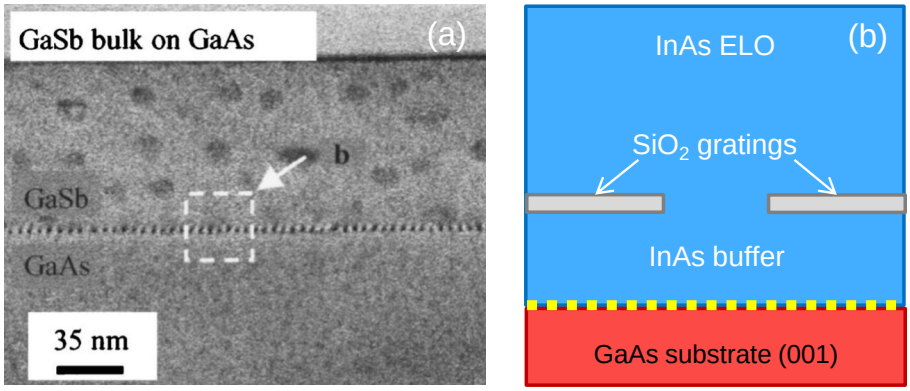

Figure 5.4: (a) InAs is initially relaxed on GaAs using the IMF technique (Adapted from [2].) (b) MBE ELO test system in InAs on GaAs.

From the InAs-ELO/GaAs test system identified, the growth process to InAs-ELO integration on (001) GaAs can be generally outlined in four steps as seen in Figure 5.5. First, InAs IMF is relaxed on (001) GaAs. Secondly, InAs/GaAs is patterned ex-situ with dielectric gratings accordingly to the two-stage approach, specifically using [010]-aligned gratings. Thirdly, InAs lateral growth is performed using PSE growth approach until lateral coalescence (or approaching lateral coalescence) occurs. Then lastly (and fourthly), continuous InAs growth is performed to achieve planar coalescence.

Since the first two steps of the proposed InAs-ELO integration are well-established, a brief summary if provided here. The InAs IMF was formed through the growth of 300nm GaAs buffer layer to smooth the growth front

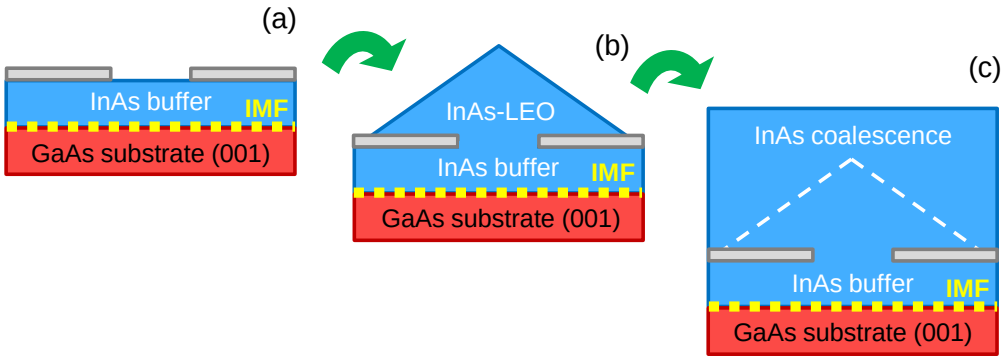

Figure 5.5: (a) InAs is initially relaxed on (001) GaAs. Also, dielectric gratings aligned to the [010]-direction are patterned ex-situ. (b) Then, InAs LEO is grown using a newly developed InAs PSE growth approach. Lastly, (c) InAs growth is resolved to regain a planar episurface.

prior to IMF formation. The growth temperature is then reduced to 410°C where the first 26ML of InAs was grown under In-rich conditions at a As_2/InAs flux ratio at 0.7x. Then, growth conditions were transitioned to As-rich conditions at 430°C with As_2/In flux ratio at 1.3. The total InAs growth needed to relax InAs on GaAs to nearly 100% was 500nm. Next, with the InAs buffer grown, the samples were transferred ex-situ for the fabrication of [010]-aligned silica gratings. Mirroring the methodology outlined for the homoepitaxial GaAs investigation detailed in Chapter 3, silica gratings were patterned varying pitch between 1.4-1.8μm all at a 50% fill factor. Lastly, gratings patterned on InAs/GaAs was prepped for in-situ growth and transitioned back to MBE reactor for the third and fourth growth steps, LEO and coalescence growth studies. More information on the grating fabrication and sample preparation can be referred to in Appendix 1.

5.2.1 Developing InAs LEO using a PSE approach

With silica gratings patterned on InAs/GaAs, an investigation into heteroepitaxial InAs LEO could be examined. In the pursuit of InAs planar coalescence in heteroepitaxial ELO, this step was the most pivotal as two key growth attributes needed to be identified. First, as reports of PSE growth were solely developed around the $Al_xGa_{1-x}As$ alloys, a new InAs PSE approach needed to be developed for the first time. Secondly, and more importantly, with a highly selective InAs PSE approach developed, "wetted" growth of (011) faceted LEO needed to be replicated for InAs as this is critically necessary to lateral encapsulated the silica grating providing a InAs non-planar template to achieve InAs planar coalescence.

To develop InAs PSE growth, growth conditions needed to be identified where highly selective growth occurred. Since the selective growth space is depended upon several growth variables, namely growth temperature and growth rate, the initial PSE InAs study fixed growth rate and PSE duty cycle 0.25μm/hr and 50%, respectively, equivalent to those used in the GaAs PSE forming LEO. As such, growth temperature was varied between 480-520°C as seen in the planview SEM images Figure 5.6. Using visual inspection, the point of high selectivity was identified with InAs growth at 520°C with minor polycrystalline InAs nuclei forming at 500 °C and heavy InAs polycrystalline deposition at 480°C.

With high selectivity of InAs on silica in place, InAs lateral growth over [010]-aligned gratings using PSE was investigated. As an initial investi-

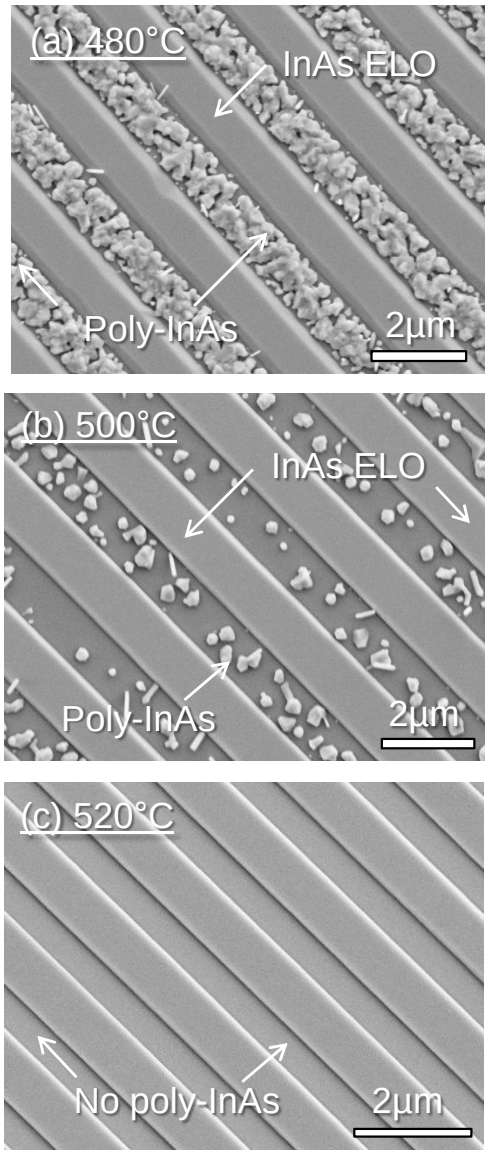

Figure 5.6: Planview SEM images showing polycrystalline InAs nucleation on silica bars with PSE growth at (a) 480°C and (b) 500°C). (c) Polycrystalline-free growth occurs for InAs PSE growth beginning at 520°C.

gation, InAs PSE was performed with the objective of identifying the facet formation rather than observing lateral coalescence. As such, 180 cycles of InAs PSE under the previously describe growth conditions was performed. As seen in Figure 5.7, using visual inspection InAs PSE was identified to form (011) facets with the initial progression of "wetted" lateral growth occurring across the [010]-aligned gratings, mirroring the growth attributes identified with the GaAs PSE approach. With the two-stage approach in mind, InAs lateral growth using the PSE approach was well suited for producing lateral encapsulation of silica gratings, forming a non-planar template with which to enable planar coalescence in the second stage .

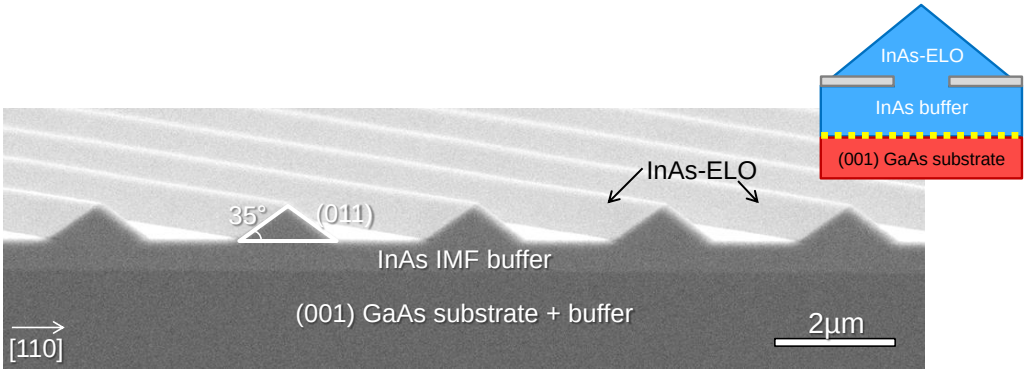

Figure 5.7: The initial progression of "wetted" InAs lateral growth occurred across the [010]-aligned gratings, demonstrating the equivalent growth attributes of InAs PSE identified with the GaAs PSE first stage approach.

5.2.2 Achieving InAs Planar Coalescence

With the first stage of the all-MBE InAs two-stage approach confirmed, planar coalescence over non-planar InAs lateral template was investigated.

Mirroring the two-stage growth approach to GaAs, continuous InAs growth was used to planarize the non-planar InAs template through "capillary" growth in the faceted valleys, driving the growth front toward planar conditions. Thus to investigate InAs planar coalescence, 170 cycles of InAs LEO over [010]-aligned 1.4-1.8μm pitch gratings was deposited using the previously described InAs-PSE method. In the first stage, LEO was tailored to specifically not to complete lateral coalescence but rather to reach within below an In adatom diffusion length as this is sufficient to use continuous MBE growth without concern of polycrystalline formation on the silica bars. Then, in the second stage, 2μm of InAs was grown using continuous MBE growth over the LEO template. Continuous InAs growth conditions utilized a 45x As_4/In BEP ratio with growth temperatures and rates at 480°C and 0.5μm/hr, respectively. Upon completion of the second stage growth, it was clear the templated growth of the first stage had reached planarization in-situ as RHEED showed a clear streaky 4x and 2x patterns, indicating a smooth growth front as seen in Figure 5.8.

Taking a closer look at InAs planar coalescence ex-situ, cross-section SEM and AFM were performed. By visual inspection, InAs planar coalescence over the silica gratings can be clearly seen in Figure 5.9 from the cross-sectional SEM images showing thin 1.8μm pitch silica gratings are seen embedded under 2.25μm of total InAs growth, the net layer thickness resulting from both LEO and continuous growth stages. Also, owing to differing material contrasts, a clear separation between the InAs and GaAs can be identified. Surface rough-

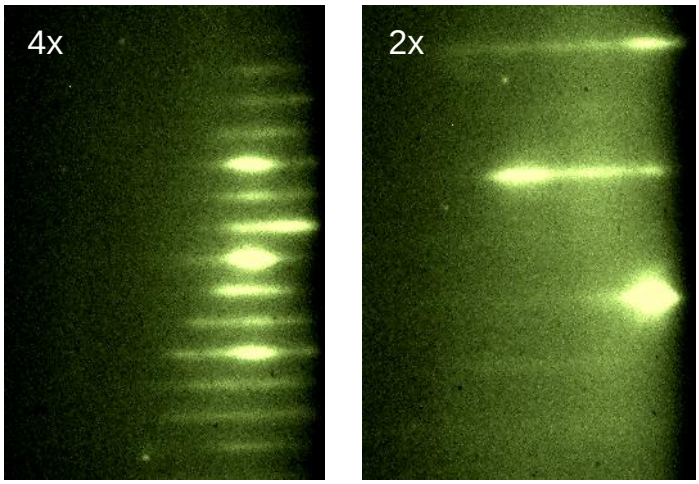

Figure 5.8: RHEED demonstrated a clear streaky 4x and 2x patterned after InAs planarization.

ness after planar coalescence was also reasonably low between 1.4-1.8μm pitch samples, all achieving between 5-7nm nm RMS roughness, an example of which can be seen in Figure 5.10. As a comparison, InAs ELO surface roughness was compared to grating-free InAs/GaAs control grown to an equivalent thickness [2], which achieved a 2.5nm RMS surface roughness approximately 2-3x lower than InAs/GaAs ELO. The increase roughness in the InAs ELO can partially be attributed to the elevated first stage growth at 520°C when using the two-stage approach, but remains at similar surface roughness levels as observed in homoepitaxial GaAs planar coalescence. Further surface roughness reduction studies may demonstrate control levels, for example using additional continuous growth and/or use of growth surfactants such as Bi [48, 49] to further

[2]In the InAs/GaAs control, the InAs was initially relaxed using the prescribed InAs IMF technique and then continuously grown at 480°C

smooth the (001) episurface.

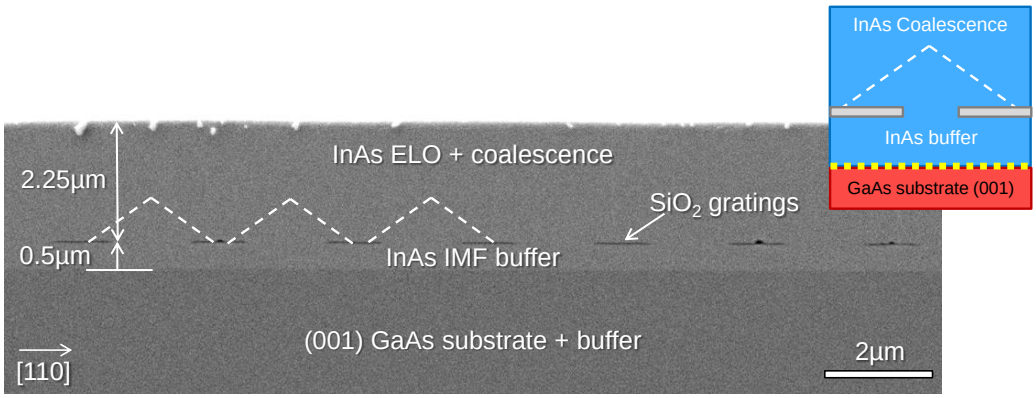

Figure 5.9: Cross-sectional SEM image showing the complete integration of thin 1.8μm pitch silica gratings embedded under 2.25μm of total InAs growth resulting from both LEO and continuous growth stages. Also, owing to differing material contrasts, clear separation between the InAs and GaAs can be identified.

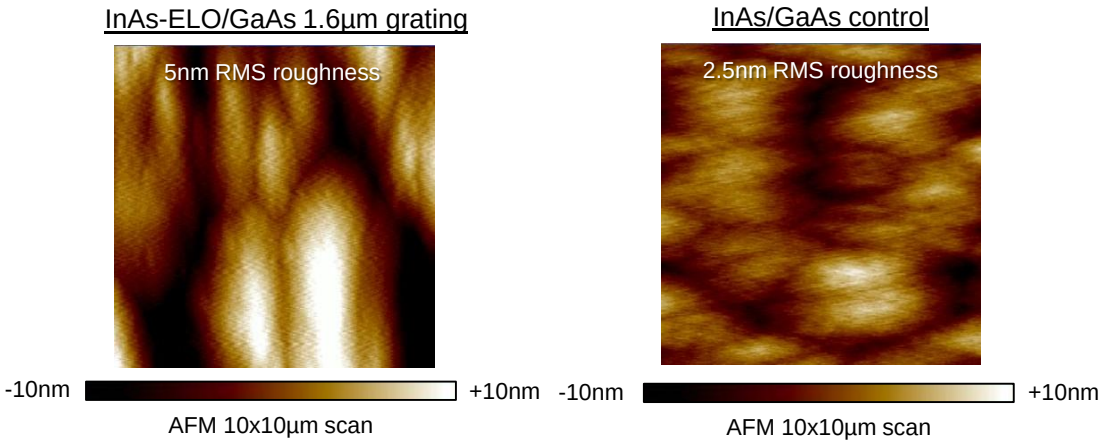

Figure 5.10: The lowest surface roughness of the planar coalescence occured for 1.6μm pitch gratings which achieved 5nm RMS roughness. A grating-free InAs/GaAs control achieved surface roughness at 2.5nm RMS, 2x lower than the ELO sample.

Importantly, based on the in-situ and ex-situ characterization, it is clear that the two-stage growth approach original developed for homoepitaxial GaAs could be applied without significant deviation for heteroepitaxial InAs. Sharing almost the same growth conditions except for growth temperature, a first stage highly-selective PSE growth approach for InAs produced (011)-faceted LEO across [010]-aligned gratings enabling a non-planar lateral encapsulation of silica grating which was then planarized in the second stage using continuous InAs growth, resolving the growth to planar coalescence. From these results, it marks the first demonstration of an all-MBE approach to InAs planar coalescence as well as high lattice mismatch InAs ELO heteroepitaxy.

5.3 Dislocation Reduction in MBE InAs-ELO/GaAs Metamorphics

With a growth approach to InAs ELO on (001) GaAs in place, the investigation central to high lattice mismatch heteroepitaxy could begin investigating the core question at hand: does the two-stage growth approach to InAs heteroepitaxy improve material quality compared to grating-free controls? To begin to answer this question, an initial investigation sought to observe a key ELO trend: increasing embedded grating fill factor should decrease threading dislocation density and increase bulk PL in the device region. To investigate this trend, grating fill factor was varied between 40-68%. In this initial investigation, grating fill factors were restricted to mid range values since conventional optical lithography techniques were limited to minimum window

sizes of approximately 0.7μm, while reasonable growth timescales limited the maximum bar width to 1.5μm, hence a maximum fill factor at 68%.

In identifying the grating fill factor growth space, InAs ELO samples were grown use the two-stage InAs growth approach as developed in the previous section. For comparison, grating-free InAs/GaAs controls were grown under equivalent conditions as detailed in the surface roughness investigation. With InAs ELO and controls identified, threading dislocation densities in the device region were estimated using Electron Channeling Contrast Imaging, an SEM-based technique which utilizes calibrated electron backscattering to resolve crystal defects such as threading dislocations and stacking faults at the surface of crystalline materials. Practically, defects appear as bright spots in the images, and the surface density estimated by selecting representative areas and counting dislocations via visual inspection. Based on the threading dislocations density investigated here, ECCI scans were performed representative InAs ELO and control 5x6μm and 10x11μm areas.

From ECCI analysis, a general observation was made, in particular, all InAs ELO samples had reduced threading dislocation densities compared to grating-free InAs/GaAs controls. Also, all InAs-ELO (and controls) has a remarkable lack of stacking fault formation, only one identified in all InAs ELO samples imaged. To make a representative comparison, ECCI scans of InAs ELO with an embedded 1.6μm pitch silica grating at 50% fill factor compared to control can be seen in Figure 5.11. Here, a clear reduction in dislocation density can be seen in the InAs ELO sample compared to the grating-free con-

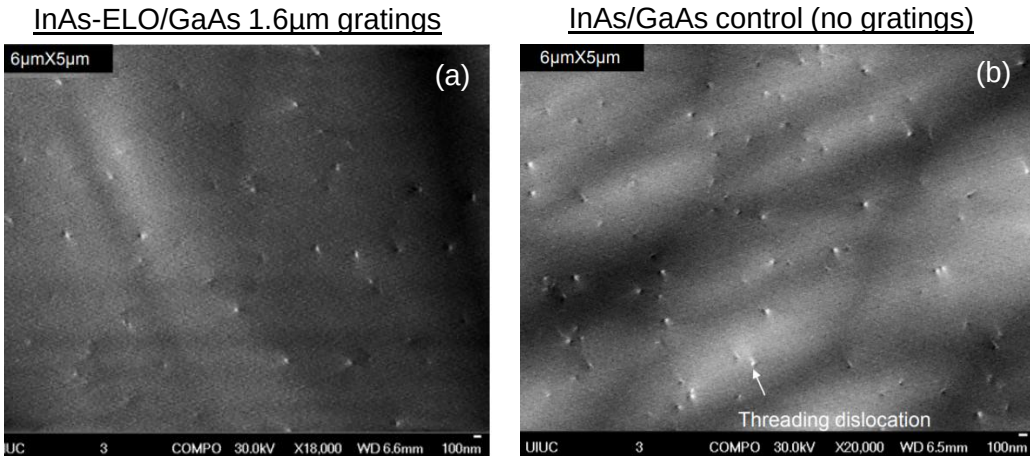

Figure 5.11: ECCI scans of (a) InAs ELO with an embedded 1.6μm pitch silica grating at 50% fill factor compared to (b) grating-free InAs/GaAs control. An approximately 50% reduction in threading dislocation was estimated the in the InAs ELO samples compared to control.

trol. Using visual inspection and counting, the threading dislocation density is estimated as 1.2×10^8 cm^{-2} for the InAs ELO and 2.2×10^8 cm^{-2} for control, an approximately 50% reduction.

In performing visual inspection and counting for all InAs ELO and control samples, an expected trend emerged: increasing grating fill factor from 40% to 68% decreased threading dislocation density as seen in Figure 5.12. The largest grating fill factor investigated at 68% also had the largest reduction in threading dislocation density achieving 7×10^7 cm^{-2}, a nearly 3x reduction compared to control. Also, the reduction in threading dislocation density mapped closely to the linear proportional reduction extrapolated from initial control threading dislocation density. Thus, based on the ECCI analysis, the material quality improvements from InAs ELO was remarkably promising as a

decrease in dislocation density and lack of stacking faults suggests of dislocation blocking from the embedded silica gratings and high-quality InAs planar coalescence.

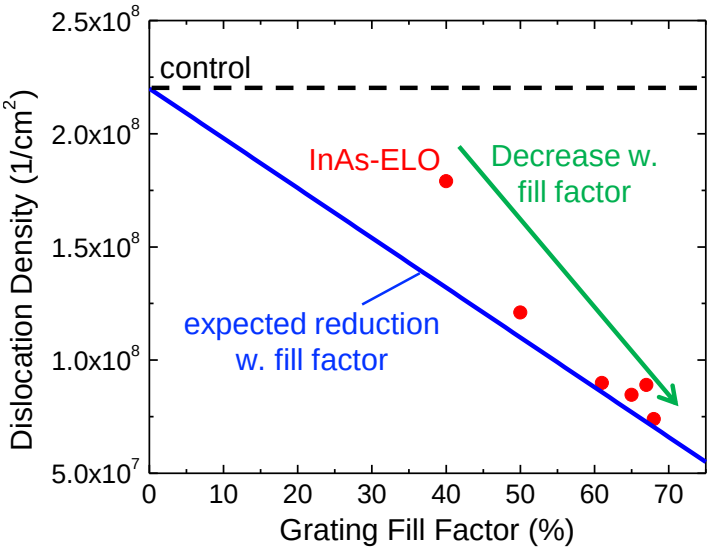

Figure 5.12: Increasing grating fill factor from 40% to 68% decreased threading dislocation density. The largest grating fill factor investigated at 68% also had the largest reduction in threading dislocation density achieving 7×10^7 cm^{-2}, a nearly 3x reduction compared to control. Also, the reduction in threading dislocation density mapped closely to the linear proportional reduction extrapolated from control.

To compliment the observed threading dislocation reduction trend observed in ECCI, PL was also performed on both InAs ELO and grating-free controls to confirm this increase to material quality. More specifically, PL is sensitive to non-radiative recombination sites such as threading dislocations and stack faults as well as other material defects such as grain boundaries and

point defects; thus an increase in PL should be observed for the InAs ELO when compared to control Additionally, since the pump spot size at 80μm can sample a wider area compared to ECCI, PL should also be more agnostic to selection bias.

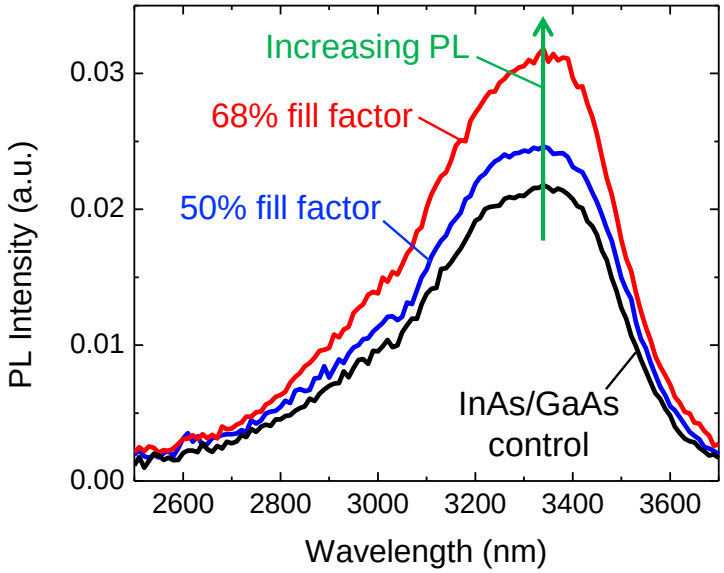

Figure 5.13: An increase in peak PL was observed compared to control. For 50% fill factor embedded gratings, a 1.2-1.3x increase in PL was observed in InAs ELO compared to control. Also, for 68% fill factor embedded gratings, a nearly 1.5x increase in PL was observed in InAs ELO compared to control.

PL was performed under at room temperature under high pump excitation. Under these condition, an increase in peak PL was observed compared to control. As seen in Figure 5.13, for 50% fill factor embedded gratings, a 1.2-1.3x increase in PL was observed in InAs ELO compared to control. Also, for 68% fill factor embedded gratings, a nearly 1.5x increase in PL was observed in InAs ELO compared to control. Additionally and importantly, the

peak PL response of all InAs ELO samples aligned well with the control peak, suggesting all samples measured were relaxed equivalently and that relaxation in all samples was nearly 100%. Based on the PL analysis, this confirmed with material quality improvements from InAs ELO heteroepitaxial integration.

5.4 Summary

In summary, the all-MBE growth approach originally developed for embedding dielectric microstructures in homoepitaxial III-V growth also extends high-quality dielectric integration to high lattice mismatch heteroepitaxy. Specifically, a two-stage growth approach to InAs was developed which exactly mirrored the approach to GaAs. Thus, using InAs/GaAs as test system, we demonstrated for the first time material quality improvements including a nearly 3x reduction in dislocation density and 50% increase in PL using an entirely MBE growth approach. Importantly, this test system marks the first demonstration of ELO metamorphics using an all-MBE approach and the second crystal growth technique to demonstrate planar coalescence in high lattice mismatch ELO metamorphics. Going forward, the two-stage all-MBE growth approach to ELO metamorphics forms a new pathway toward high-quality, low defect III-V heterogeneous integration on silicon.

Chapter 6

Conclusion

In the dissertation, we have presented for the first time a robust methodology for planar coalescence over embedded dielectric microstructures using an entirely all-MBE approach. Utilizing core principles of two-stage growth methodology, high-quality planar coalescence was achieved for the first time in both GaAs and InAs in homoepitaxial and heteroepitaxial systems embedding a variety of dielectric microstructures including gratings and hexagonal disc arrays. Based on these findings, neither quality nor application limitations have been observed in its implementation, making this technique a robust path forward for seamless integration of embedded nano- and microstructures, marrying dielectric/III-V materials for applications photonics and high lattice mismatch heteroepitaxy toward optoelectronic devices with enhanced functionality.

6.1 General Observations on MBE Coalescence

Before summarizing the results of this dissertation, we provided several general observations on the growth behavior of the two-stage all-MBE growth approach within the wider integration space of embedded dielectric

microstructures. In particular, it should be noted that the growth observed over dielectric microstructures is not a statement of MBE growth in general, but rather specific to the two-stage growth approach as detailed in this thesis. Other highly selective growth techniques within MBE, such as metal-modulated epitaxy (MEE) [71], might achieve significantly different lateral growth and coalescence. Additionally, the results presented here were grown entirely on (001)-oriented substrates; thus, significant morphology and growth behaviors are expected of growth on alternate substrate orientations.

6.1.1 On Lateral Growth Morphology

Morphology of the lateral growth over dielectric microstructures is entirely dependent on the pattern shape and alignment with primary crystal planes. No difference in morphology has been observed based on III-V binary alloys. Currently, no difference in lateral growth morphology between InAs and GaAs has been observed.

The vast majority of lateral growth across gratings occurs in an non-"wetted" form typically producing an inverted mesa-like shape with limited growth in close proximity across the dielectric surface. This is especially true for lateral growth in gratings aligned off the $\langle 010 \rangle$ directions toward the [110] direction. "Wetted" lateral growth across gratings is a special form, only occurring in gratings closely aligned to the $\langle 010 \rangle$ directions, forming well-faceted $\{011\}$ triangular lateral growth.

More complex patterns beyond gratings. such as discs, sample growth

from multiple crystal fronts and directions, resulting in the lateral growth maintaining a mixture of lateral growth morphologies. This is especially true for disc arrays which sample from all crystal directions. Empirically, crystal directions with the greatest lateral growth dominate the overall lateral growth dynamics, and when suitably tailored, can achieve lateral coalescence.

6.1.2 On Air Void Formation

Non-"wetted" lateral growth will form air voids immediately above the dielectric surface which can often be encapsulated through lateral coalescence. "Wetted" lateral growth will not form air voids. Since more complex patterns, such as disc arrays, sample the lateral growth from several crystal directions, air void formulation is expected somewhere above the dielectric surface. A special case may be rectangular mesa arrays aligned to the $\langle 010 \rangle$ directions; although not performed in this thesis, the "wetted" lateral growth at this alignment would likely lead to a voidless embedded dielectric surface.

From a photonic design perspective, air void shape above gratings can be tailored based on the degree of alignment off the $\langle 010 \rangle$ direction while still maintaining high-quality planar coalescence. This feature may be useful for designing air voids for light extraction/absorption. Also, since embedded dielectric microstructures like discs will contain air voids to some degree above the dielectric surface, their presence must be accounted within the design of the photonic material and can possibly be utilized to further enhance the photonic system.

6.1.3 On Lateral Coalescence

For "wetted" lateral growth, lateral coalescence is not required to be achieved, rather lateral encapsulation below an adatom diffusion length. Unless a particular valleyed structure is needed, such as in using a valley to site-select quantum wires or dots, partial lateral encapsulation is sufficient without nucleation of polycrystalline deposition on the dielectric surfaces. For non-"wetted" lateral growth, lateral coalescence is required. Since the lateral growth morphology progresses as an invested mesa, nearly the entire dielectric microstructure is exposed up until the point of lateral coalescence. Thus, continuous growth prior to lateral coalescence risks formation of polycrystalline deposition on the dielectric surface. Therefore, lateral coalescence for non-"wetted" lateral growth conditions is required.

6.1.4 On Planar Coalescence

High-quality planar coalescence occurs in both voidless "wetted" systems and encapsulated air void non-"wetted" growth. High-quality planar coalescence based on the current growth investigations is limited to gratings with alignments along the $\langle 010 \rangle$ directions, grating off the $\langle 010 \rangle$ directions toward the [110] direction, and disc arrays. Gratings aligned outside this direction have varying degree of lateral growth, but none of the type to planarize in regaining the (001) direction. Planar coalescence only occurs if the initial lateral coalescence is well-faceted. While lateral growth occurs on gratings aligned to the [110] direction, nodules of dissimilar facets occur at the leading

edge of the lateral growth, resulting in coalescence that is non-planar. This growth behavior occurs for both InAs and GaAs.

6.2 Summary

In summary, this dissertation demonstrated for the first time several dielectric integration techniques and associated materials using an entirely all-MBE approach. Underpinning the methodology was the development of a two-stage growth approach for high-quality planar coalescence for embedding dielectric microstructures. In applying it to the growth GaAs over silica microstructures patterned on (001) substrates, we achieved to the best of our knowledge highest quality planar coalescence of any conventionally grown III-V binary alloy, owing to the sensitive probe of the coalescence material quality. Specifically through an InGaAs/GaAs/AlAs PL emitter, overgrown GaAs was shown not only to be of equivalent optical quality compared to grating-free controls, but also demonstrated PL enhancement through extraction and Purcell enhancements, a first of its kind using a seamless growth approach.

In extending the techniques to photonic material systems, the two-stage growth approach was tailored for a wide range of embedded dielectric structures. Using a slower LEO growth rate, the two-stage growth approach was able to embed gratings at a much higher aspect ratio. Also, using tall silica gratings as an etch mold, highly selective wet etches in mesa-defined area produce air channels, achieving the highest possible index contrast embedded gratings in III-V semiconductors. Additionally, in applying the two-stage

growth approach to hexagonal disc arrays, self-formed air voids were observed. Rooted from this observation, further investigation revealed equivalent air void formation in off [010]-aligned gratings, developing for the first time a fully scalable crystal growth approach to faceted embedded air voids at the micron-scale using dielectric masks in conventional III-V materials.

In exploring material improvements to relaxed high lattice mismatch heteroepitaxial systems, we demonstrated for the first time an all-MBE approach to ELO metamorphics. Using InAs/GaAs as the test system, we developed a two-stage growth approach for InAs including reporting for the first time a highly selective PSE approach to InAs on silica gratings. Then, through increasing embedded grating fill factor to 68%, we demonstrated a 3x decrease in threading dislocation density and 50% PL improvement in InAs-ELO/GaAs versus grating-free InAs/GaAs controls. As a result, the InAs-ELO/GaAs marked for only the second crystal growth technique to achieve planar coalescence in an ELO metamorphic system.

Looking from a historical perspective, the demonstrated all-MBE growth approach to planar coalescence over embedded dielectric microstructures marks a significant advancement in the long-standing challenge of seamlessly integrating high-quality semiconductor crystal growth with dielectric microstructures. Not only do these findings unlock MBE as a crystal growth approach for planar coalescence over embedded dielectric microstructures, but also demonstrates to the best of our knowledge the highest quality planar coalescence based on the sensitive probing of PL studies to date. Forward looking, these results open the

door to several high-impact applications, including enhanced quantum emitters and embedded metasurfaces as well as an all-MBE approach to heterogeneous III-V integration on silicon. More specifically, based on the progress in these material investigations presented here, device level dielectric/III-V integration can be seen as the next step, immediately achievable for the enhancement or improvement in the wide array of optoelectronic and photonic devices.

Appendices

Appendix A

Grating Fabrication and Growth Preparation

In this appendix, procedures for the ultraclean grating fabrication, substrate preparation for epitaxial regrowth, and MBE regrowth loading and cleaning procedures are detailed.

A.1 Pre-Fabrication Notes

The silica grating fabrication guidelines presented here are tailored specifically for regrowth on III-V substrates. It assumes that the wafers are full 2" wafers. Also, this process is capable of achieving linewidths and pillars down to 650nm. However, the height/thickness of the features are limited to 300-400nm as the etch mask is thin. Lastly, an a very important point to remember: clean tools, such as tweezers, are always used when handling the samples. Use the LASE Group UHV treatment on the clean tools prior to fabrication. Once a critical step is complete, change the clean tools to another set and consider the previous used tools as dirty, needing the UHV treatment before re-use. Always wrap clean tools in clean foil origami, such as foil boats.

A.2 PECVD Procedure

PECVD is the first major step in the fabrication of silica gratings on III-V substrates. When done properly, a few wafers can be processed in about 4 hours.

1. Clean the PECVD hotplate. Visually inspect hotplate for scratches, odd debris, etc.. Lightly clean shower head and hotplate with water. After hand cleaning, pump down the PECVD reactor and use standard CF_4/O_2 clean at 250°C, the deposition temperature. If the hotplate is already relatively clean, a 30 minute is suitable. A long duration clean may be necessary if the hotplate conditions are worse.

2. After the hotplate is clean, deposit 0.5μm of silica on the hotplate. This acts as a clean barrier between the hotplate and the sample to keep the unprotected wafer backside and epi-side from contamination from the hotplate. Approximately 10 minutes of silica deposition using the Bank group recipe is needed to achieve 0.5μm thickness for the hotplate barrier.

3. Acid dip III-V wafers. You'll want to remove any surface oxides prior to deposition to ensure any PECVD materials bond directly to the III-V crystal. Using the III-V acid bench, make a dilution of 1:10 HCl:water. This is sufficient strength to remove III-V surface oxides. Using the house HCl 1:10 dilution is 40ml added to 120ml of DI water. These don't have to be super exact, just close.

4. Using the clean beakers and acid dippers, dip the III-V wafer into the dilution for 60s. Make sure to use a clean pair of clean tools solely for handling the sample at this stage. Make sure to visually inspect the wafer surface goes hydrophobic; as this implies the surface oxide has been remove and the native crystal is exposed, ready for deposition. N_2 dry. Do not use the metal tweezers directly in the acid solution. Also, after successful oxide removes, do not reuse the tweezers for future processing steps until a treatment is performed.

5. Make sure to have a PECVD clean tweezers set. This includes a wafer handler and rounded nose tweezers. Two clean tweezers are needed to handle the sample on the hotplate; in particular, picking up and flipping the samples. Also, make a clean foil boat for the sample. This boat will be used to cool the sample back to room temperature prior to its placement in its wafer container. A hot sample will melt the wafer container ruining the sample for regrowth purposes.

6. Load the sample onto the hotplate. Minimize the time between surface oxide removal and transit to the hotplate as surface oxides will start to reform. Deposit materials as per the desired layer structure. If uniformity is desired, make sure the sample is placed as close to the center of the hotplate as possible. The deposition here is the most uniform. Also, if a very specific thickness is needed, err on the side of too much deposition. Cleanly checking with the ellipsometer to see if the thickness is

correct and check across the sample to check for uniformity. If too thick, you can always wet etch back down to the desired thickness.

7. Deposit the α-Si sacrificial layer. Only about 4-5nm is needed to act as a top side sacrificial layer.

8. Vent PECVD chamber and carefully flip the sample epi-side down with α-Si layer for backside sacrificial layer deposition. Avoid flipping the wafer too aggressively as this will cause the wafer to shatter. Also, avoid the sample epi-side down from sliding on the hotplate as this will scratch the episurface.

9. Deposit backside sacrificial layer. Typically 2 minutes of α-Si deposition is sufficient to protect the backside from clean room contaminates.

10. Remove sample from PECVD hotplate and place on clean foil boat to allow to cool. Placing straight into sample holder will cause the plastic to melt and ruin your sample. Once cool, transfer your sample in its sample holder. After successful transfer, do not reuse the tweezers for future processing steps until a clean treatment is performed.

11. Lastly, clean the PECVD chamber for the next user; 15 minutes is typically sufficient.

A.3 Lithography Procedure

Lithography is the second major step in the fabrication of silica gratings for regrowth. Prior to this step, make sure to check the stack thickness using the ellipsometer. After spinning on the resist, it is often difficult to check stack thickness once the resist mask is applied. To check the stack, make sure to check several spots across the entire wafer as the PECVD deposition is often non-uniform especially if the wafer drifted or was place off the center of the shower head. When done properly, a few wafers can be process in 2 hours.

1. Setup hotplate and set temperature at 70°C. Make sure the hotplate has new clean foil to protect the backside from contamination. Also, confirm the hotplate temperature using the spring thermometer at the center of the hotplate. Adjust hotplate temperature accordingly.

2. Acquire new clean tweezers. Also, make a new clean foil boat. This will be for placing a baked sample of the hotplate to cool prior to transfer to its wafer carrier.

3. Spin on the resist. We currently use nr9-500p negative resist by Futurrex. It's a high resolution resist capable of making features down to 650nm under optimal conditions. Apply resist about 14-16 drops to yield a full coating of a 2" wafer. Set spinner for 4000 rpm and spin for 40s. Testing the revolutions and duration is best done prior on a dummy wafer prior to coating a regrowth sample.

4. Perform the pre-bake on the pre-set hotplate. Confirm temperature. Pre-bake at 70°C for 3 minutes. Once pre-bake is complete, set the hotplate to 100°C. This is the post-bake temperature. Again, use the spring thermometers to ensure the actually hotplate temperature is accurate. Adjust the hotplate setting to achieve this temperature accordingly. After pre-bake is complete, place wafer on clean foil boat to cool wafer before placing in its plastic wafer carrier.

5. Setup the MA6 for the following exposure conditions. Use full-vacuum contact with 6s pre-vac, 30s vac, and 6s post-vac conditions. Also set the a1 gap at 20μm. Lastly, set exposure time. This is variable based on the contact and desire linewidths for the sample grating structures. The minimum empirically determined exposure is 10-11s at full vacuum. However, if underexposure is an issue, expose sample up to 24s as this has resulted in successful results. Tailor the exposure accordingly. Also, make sure the lamp line is set to CH1.

6. Set up the 2" mask holder and 2" chuck. Make sure the chuck is centered in the mask before placing the mask on the mask holder. Carefully place the mask onto the mask holder. Confirm visually that the desire mask portion is centered in the opening on the mask holder.

7. Run wafer using the MA6 load command. Take note of the vacuum gauges and ensure the exposure intensity at 7.5mW is met.

8. Unload wafer. Perform the post-bake at 100°C for 3 minutes. Extending to 4 minutes is suitable but not always necessary. This may be advantageous if greater adhesion of the resist mask to the substrate is needed. Also, as the gratings are diffractive to visible light, after 1 minute in the post bake, visual confirmation of diffraction should be confirmed. After 3 minutes of the post-bake, the diffraction should be quite strong. Weak diffraction is often a sign of poor lithography and the resist will wash away at the development stage. Place on clean foil boat to cool the sample before placing it in its plastic wafer carrier.

9. Develop the wafer using MF-26A, the house developer. It is a 2.5% TMAH-based developer. Setup lithography bay solvent hood with clean kemwipes. Setup necessary development beakers and wafer handlers. Develop for 10s maximum. Rinse for 60s and N_2 dry. After successful lithography, do not reuse the tweezers for future processing steps until a treatment is performed.

A.4 Etch Procedure

Dry etching is the third major step. The etching process can often be combined with the sample prep and cleaning stages. Etch processing when done properly will take 2 hours for a few wafers.

1. Clean etch chamber. Vent system place quartz ring and clean silicon backing wafer prior to cleaning. Make sure there is not any chuck exposed

between the silicon wafer and the quartz ring as the etch of the chuck can contaminate the sample. Use a standard O_2 chamber clean recipe; 30 minutes is typically enough to clean the chamber well. More may be necessary if chamber look especially dirty.

2. If you haven't already, check on resist free areas with the ellipsometer to check layer thickness stacks. Ideally, do this before the lithography steps. If forgotten, do this now.

3. Calculate total etch time. On the Plasma Therm #2 using the house CHF_3/O_2 etch recipe, the etch rate is 32nm/min for silica and 12nm/min for α-Si. I typically calculate the etch for the stack plus added time equivalent to 20% extra silica. For example, if my stack was 5nm α-Si and 30nm silica, my etch rate duration would act as if my stack was 5nm α-Si and 36nm silica. Thus, my total etch time would be 24s + 68s = 92s total. Avoid over etching beyond the necessary over estimates as this will damage the episurface, taking many digital etches to regain an episurface and too much damage may be unrecoverable. Also, the 20% rule only applies to thin gratings. Thicker gratings may have shadowing from steep vertical walls, requiring a longer duration etch to account for the decreased etch rate.

4. Load the sample. Use clean tweezers when handling the sample. Make sure it is placed near the center of the silicon wafer. Also, ensure it does not drift during the etch as the quartz ring can shadow the edge of the

wafer causing an a non-uniform etch. Run the etch recipe.

5. Unload sample with clean tweezers. A second pair is needed as a back-stop as the silicon backing wafer is smooth and hard to grasp with only one pair. Remove clean backing wafer. Clean dry etch reactor. After successful etch, do not reuse the tweezers for future processing steps until a treatment is performed.

A.5 Resist and Sacrificial Layer Removal

This is the fourth major step in the grating fabrication process which includes the resist and sacrificial layer removal. Cleaning steps are difficult to predict in duration. The entirety of the cleaning and prep process can take as little as 2 hours for a single wafer to several depending on the sample condition after the PECVD, lithography and etch steps.

1. Heat KwikStrip to 90°C in the bat-cave solvent hood. Make sure to use the regrowth dishes and not the laser processing dishes. No need to confirm the KwikStrip is accurately at 90°C. Simply setting the hot plate to 90°C is sufficient. Also, remember to use a new clean set of clean tweezers. This set can be used for both the KwikStrip and TMAH steps.

2. Once heated to 90°C, add the sample. Visually confirm the resist is removed. This is often difficult for thick silica gratings, but for thin

gratings, you should see the resist film wash off almost instantly. Typically no more than 2 minutes is needed to reasonably remove the resist. Carefully cascade rinse or dip wash for 1 minutes and N_2 dry.

3. Carefully remove the hot KwikStrip from the hotplate and set the hotplate to 60°C. Add MF-26A developer to the regrowth TMAH dish. This is for the α-Si sacrificial layer removal. Allow the TMAH solution to heat to 60°C for 15 minutes before adding the sample.

4. Add sample to TMAH solution. The total duration can be a little tricky to determine. I usually position the sample epi-side up for the first 5-10 minutes, then flip the sample epi-side down to etch the backside sacrificial layer for 10-20 minutes until visually confirmation of the layer is removed. I avoid letting the wafer sit for no longer than 40 minutes as THMA solution as it is prone to slowly etch III-V especially InAs. Cascade rinse or dip wash for 1 minute and N_2 dry.

5. Carefully dispose of the TMAH solution in the appropriate waste container in the lithography bay. Visually inspect sample in the microscope. More than likely regions will have hardened resist that was not removed by both the KwikStrip and the sacrificial layer removal. Note these locations. This is OK since the O_2 plasma and digital etch will remove these areas in the next step. After successful resist removal, do not reuse these tweezers for future processing steps until a treatment is performed.

A.6 O_2 Plasma and Digital Etch

This is the fifth and last major step of the grating fabrication process. This is typically completed before loading. This can be the most stressful part of the process as this step will reveal if the III-V surface is epi-ready. The entirely of the O_2 plasma and digital etch can take as little as 1 hour per sample or several hours if etch correction and significant epi-recovery is needed.

1. Clean etch chamber. Vent system place quartz ring and clean silicon backing wafer prior to cleaning. Make sure there is not any chuck exposed between the silicon wafer and the quartz ring as the etch of the chuck can contaminate the sample. Use a standard O_2 chamber clean recipe. 30 minutes is typically enough to clean the chamber well. More may be necessary if chamber look especially dirty.

2. Load the sample. Use clean tweezers when handling the sample. Make sure it is placed near the center of the silicon wafer. Also, ensure it does not drift during the etch as the quartz ring can shadow the edge of the wafer causing an a non-uniform etch. Run the O_2 descum recipe. It doesn't take much time to re-oxidize the episurface and remove the harden resist. No more than 2 minutes on the first pass is necessary. Too many O_2 descum cleans can cause the top surface to form micro-cracks.

3. Unload sample with clean tweezers. A second pair is needed as a backstop as the silicon backing wafer is smooth and hard to grasp with only one

pair. Keep these tweezers clean using a foil boat, but do not use them for the acid dip steps.

4. Unload sample and visually inspect, especially the areas where there was harden resist. There should be a visual change in the resist and/or removal.

5. Acid dip the wafers exactly in the sample manner as in the PECVD step (HCl dilution, acid hood prep, etc.). This removes crystal damage oxidation as well as any oxidized resist. Make sure clean kemwipes are used to protect the sample from the bench in case it is dropped. Also, make sure a new set of clean tweezers are used.

6. Most IMPORTANT Step: Make sure to visually inspect the sample and that its surface goes hydrophobic; as implies the surface oxide has been remove and the native crystal is exposed and minimally damaged. Crystal damage and/or remaining silica will show the surface as hydrophilic. If hydrophilic regions of the surface remain, perform a second O_2 descum. This will reform another surface oxide layer to remove further crystal damage and is performed by repeating the previous steps until the surface goes hydrophobic.

7. (only if needed). If the sample doesn't go hydrophobic after the second O_2 descum, it is possible the silica etch did not make it through the silica and a few nanometers left. If this seems to be the case, check any hydrophilic unpatterned area with the ellipsometer. If it shows any

oxide just after an acid dip, this is more than likely silica and not native oxide. Perform a quick CHF_3/O_2 etch (cleanly!) or a very dilute and quick HF dip to etch down to the III-V surface and then perform a third O_2 descum. My record is four descum steps in total to recover the episurface. Do not attempt more than 4 as more than likely the sample has a fabrication related problem which will likely have unsuccessful growth and/or a hardy surface contamination either of which should not be loaded into the MBE system.

A.7 Sample Loading and Cleaning

At this point, the sample is prepared for growth. You may decide to clean a full 2" wafer, remove from the system, and cleave into smaller piece for growth. The choice is yours depending on the experiment. I would advise full 2" cleaning as you only have to do one H-clean for a full 2" wafer as oppose to a sample by sample basis. If this method is use, only a standard heater station bake is necessary once a sample reenters the system, essentially standard sample prep procedures.

1. Load sample into load lock as per LASE Group loading procedures. Discuss with senior LASE Group member if using the faceplate and backing wafers for regrowth is appropriate and/or if it will impact there growth quality. This may impact members requiring the highest optical quality growths.

2. Always hydrogen clean a newly processes sample prior to any growth or bake! This removes free C and O on the surface. Also, always follow current LASE Group AHS cleaning rules!

3. Prior to a new regrowth campaign, it is always good practice to baseline the MBE reactor via an RGA scan. Baselining is always done with an unprocessed fresh GaAs piece at thermal deoxidation temperatures. Once an AHS clean regrowth sample is prepared, check the RGA at the equivalent thermal deox temperature. The regrowth sample after all of the prep and clean steps should look within a factor of a unprocessed sample among the RGA partial pressures. Make sure to look for concerning peaks. If a concerning peak emerges, terminate growth and evaluate the cause.

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