Trapezoidal Current Modulation for Bidirectional High Step-ratio Modular DC-DC Converters

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***Abstract*—Modular dc-dc converter (MDCC) has been proposed for high step-ratio interconnection in dc grid applications. To further optimize the performance of MDCC, this paper presents a trapezoidal current modulation with bidirectional power flow ability. By giving all the sub-module (SM) capacitors an equal duty to withstand the stack dc voltage, their voltages are balanced without additional feedback control. Moreover, based on soft-switching performance and circulating current analysis, three-level and two-level operation modes featured with high efficiency conversion and large power transmission, respectively, are introduced. The control schemes of both modes are designed to minimize the conduction losses. Besides, the SM capacitor voltage ripples with different switching patterns are compared and the option for ripple minimization is presented. A full-scale case study is provided to introduce the design process and device selection of the MDCC. The experimental tests based on a down-scaled prototype are finally presented to validate the theoretical analysis.**

***Index Terms*—Dc-dc converter, inherent-balancing, medium voltage direct current (MVDC), modular dc-dc converter (MDCC)**

I. Introduction

THE fast development of high voltage direct current (HVDC) transmission and the promising prospect of low voltage direct current (LVDC) distribution provide an important impetus to consider dc schemes in medium voltage level [1]–[3]. Medium voltage direct current (MVDC) system may potentially become an advantageous option when it comes to the large-scale integration of offshore wind farms and large-scale power distribution in metropolitan city [4], [5]. Compared with medium voltage alternating current (MVAC) system, MVDC system could be more efficient owing to the elimination of extra ac-dc or dc-ac conversion stages [6]–[8]. Moreover, it can avoid the bulky transformer which exists in the ac system, and the compact design would considerably reduce the platform or land cost in offshore area and metropolitan city. Because of these benefits and advantages, MVDC systems are expected to become a very important complement of the traditional MVAC scheme in future medium voltage structures.

In MVDC systems, medium voltage dc-dc converters or dc transformers are the key equipments and various solutions have been proposed in recent decade. To meet the high step-ratio interface requirement between MVDC and LVDC systems, modular dual active bridge (DAB) converter and modular multilevel converter (MMC) are two major schemes. Modular DAB with input-series-output-parallel (ISOP) configuration could inherit all the operational advantages in single DAB, such as bidirectional power flow ability, soft switching-on and high power density [9]–[15]. Nevertheless, the insulation requirements of the transformers used in ISOP DAB are challenging in medium voltage applications, especially under high frequency operation. Besides, the failure of ISOP DAB could be caused by the breakdown of any single transformer. All these drawbacks undermine the reliability of the entire converter.

With front-to-front (F2F) symmetrical arrangement, the concept of MMC could solve the problems of ISOP DAB. By introducing lumped transformer, the insulation requirements are moderated and the system reliability is increased [16]–[21]. However, compared with ISOP DAB, the cost of F2F MMC is higher because of its bigger volume and lower device utilization [22]. To decrease the system volume and increase the device utilization, the topology of modular DC-DC converter (MDCC) has been developed in [23], [24], which not only combine the main advantages from both DAB and MMC but also avoid the major disadvantages from these two. The typical topologies of MDCC can be divided into monopolar [25] and bipolar [23] as well as one-phase [24] and double-phase [26]. Considering the step-ratio of the bipolar and monopolar schemes, the bipolar structure is more suitable for the high step-ratio dc interconnection. In the meantime, noting that one-phase configuration is enough to satisfy the power requirement in MVDC application, it would be a more cost-effective choice than the double-phase counterparts since it could save a plenty cost of devices as well as the isolation distance from phase to phase. Because of theses considerations, the bipolar one-phase topology (see in Fig. 1) has has been regarded as a proper choice to serve as the high step-ratio interface for MVDC network interconnection [23], [24], [27]–[29].

Sub-module (SM) stack modulation is always one of the most important aspects for MDCC operation and various modulation schemes have been developed recently to optimize the performance in different perspectives. The sinusoid modulation proposed in [30], [31] is a mature approach to realize the high efficiency and high reliability dc-dc conversion, but the it needs relatively large SM capacitance in the operation, which increases the system volume and overall cost. Square-wave or near-square-wave modulation could reduce the SM capacitance

This work was supported by the National Key R&D Program of China 2018YFB0904600.

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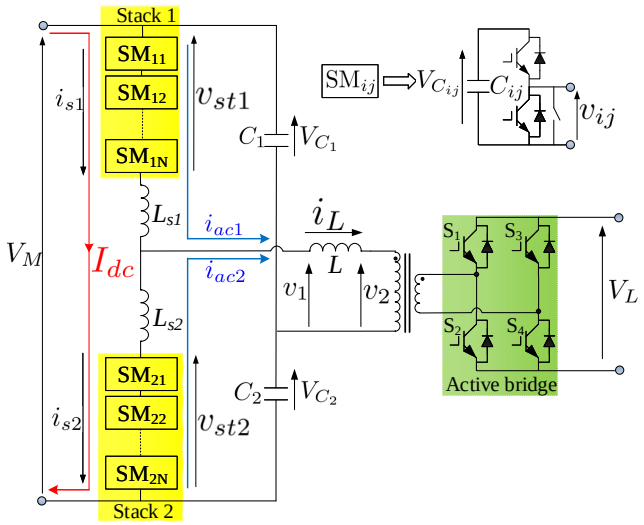

Fig. 1. The bipolar one-phase topologies of N-SM MDCC.

in the system, but a large dv/dt is produced on the transformer, which renders the transformer design difficult [23], [32]. To mitigate the dv/dt of transformers, triangle and trapezoidal modulation are the trade-off design between sinusoidal and square-wave modulation, which could address the dv/dt challenges and also avoid the large SM capacitance [33]–[38]. Nevertheless, complicated voltage balancing control algorithm is needed for both triangle and trapezoidal modulation. A predefined switching pattern and the DAB like modulation have been proposed in [39], in which bidirectional power flow and SM capacitor voltage balancing have been achieved. However, the scheme can only achieve voltage balancing in some specific cases.

This paper proposes a trapezoidal current modulation for MDCC. Compared with the modulation methods mentioned before, inherent-balancing and bidirectional power flow are achieved in this paper. The detailed reason of inherent-balancing is explained and a general switching pattern is proposed to guarantee voltage balance under all circumstances. Among different operation patterns, two modes are chosen to increase the efficiency. Soft-switching and zero circulating power are achieved in the first mode while the transmitted power can be larger in the second mode. The control schemes for both operation modes are presented to reduce the conduction losses. Moreover, the voltage ripples of SM capacitors are reduced by an optimized modulation of stacks. The design process is demonstrated via a case study and the experimental tests on a downscaled prototype are presented to validate the theoretical analysis.

II. Improved Switching Pattern for SM Capacitor Voltage Balancing

An inherently-balanced 7/5 modulation has been proposed in [39], in which a predefined switching pattern is used for SM stacks. In the prior 7/5 modulation, seven SMs are involved in a stack and square-wave stack voltages are produced. Taking Stack 1 as an example, the detailed switching pattern is illustrated in Table I. In this case, seven SM capacitors and five SM capacitors are inserted into the circuit alternately. The reason why the 7/5 modulation can achieve automatic balancing is explained as follows.

TABLE I
The Prior 7/5 Switching Pattern of Stack 1

Stage	Connected SM Capacitors						
1	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
2	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}		
3	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
4		C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	
5	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
6			C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
7	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
8	C_{11}			C_{14}	C_{15}	C_{16}	C_{17}
9	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
10	C_{11}	C_{12}			C_{15}	C_{16}	C_{17}
11	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
12	C_{11}	C_{12}	C_{13}			C_{16}	C_{17}
13	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}
14	C_{11}	C_{12}	C_{13}	C_{14}			C_{17}

Assuming that all the SM capacitors are large enough and their voltage ripples can be neglected, based on Kirchhoff's voltage law, a set of equations can be acquired as

$$\begin{bmatrix} \boldsymbol{A}_{7/5} & \mathbf{1}_{7\times7} \\ \mathbf{1}_{7\times7} & \boldsymbol{A}_{7/5} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_{C_1}} \\ \boldsymbol{V_{C_2}} \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{7\times1} \\ \mathbf{1}_{7\times1} \end{bmatrix} V_M \tag{1}$$

with $\boldsymbol{A}_{7/5}=\begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$, $\boldsymbol{V_{C_1}}=\begin{bmatrix} V_{C_{11}} \\ V_{C_{12}} \\ V_{C_{13}} \\ V_{C_{14}} \\ V_{C_{15}} \\ V_{C_{16}} \\ V_{C_{17}} \end{bmatrix}$, and $\boldsymbol{V_{C_2}}=\begin{bmatrix} V_{C_{21}} \\ V_{C_{22}} \\ V_{C_{23}} \\ V_{C_{24}} \\ V_{C_{25}} \\ V_{C_{26}} \\ V_{C_{27}} \end{bmatrix}$. It can be noticed that the voltages of L_{s1} and L_{s2} are not involved in equation (1) because they are negligible compared with SM capacitor voltages. The rank of $\boldsymbol{A}_{7/5}$ is seven, so the coefficient matrix of equation (1) is full rank and its solution is unique. This means the prior 7/5 modulation can realize balancing without extra control.

However, when applying the previous scheme in 4/2 modulation, inherent-balancing may not be guaranteed. In this mode, four SM capacitors and two SM capacitors are inserted into the circuit alternately, and the corresponding switching pattern is illustrated in Table II. Similarly, the equations can be deduced as

$$\begin{bmatrix} \boldsymbol{A}_{4/2} & \mathbf{1}_{4\times4} \\ \mathbf{1}_{4\times4} & \boldsymbol{A}_{4/2} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_{C_1}} \\ \boldsymbol{V_{C_2}} \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{4\times1} \\ \mathbf{1}_{4\times1} \end{bmatrix} V_M \tag{2}$$

with $\boldsymbol{A}_{4/2}=\begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 \end{bmatrix}$, $\boldsymbol{V_{C_1}}=\begin{bmatrix} V_{C_{11}} \\ V_{C_{12}} \\ V_{C_{13}} \\ V_{C_{14}} \end{bmatrix}$, and $\boldsymbol{V_{C_2}}=\begin{bmatrix} V_{C_{21}} \\ V_{C_{22}} \\ V_{C_{23}} \\ V_{C_{24}} \end{bmatrix}$. The rank of $\boldsymbol{A}_{4/2}$ is three, so the coefficient matrix in equation

TABLE II
THE PRIOR 4/2 SWITCHING PATTERN

Stage	Connected SM Capacitors							
1	C_{11}	C_{12}	C_{13}	C_{14}	C_{21}	C_{22}		
2	C_{11}	C_{12}			C_{21}	C_{22}	C_{23}	C_{24}
3	C_{11}	C_{12}	C_{13}	C_{14}		C_{22}	C_{23}	
4		C_{12}	C_{13}		C_{21}	C_{22}	C_{23}	C_{24}
5	C_{11}	C_{12}	C_{13}	C_{14}			C_{23}	C_{24}
6			C_{13}	C_{14}	C_{21}	C_{22}	C_{23}	C_{24}
7	C_{11}	C_{12}	C_{13}	C_{14}	C_{21}			C_{24}
8	C_{11}			C_{14}	C_{21}	C_{22}	C_{23}	C_{24}

(2) is not full rank and its solution is not unique either. This means the original 4/2 modulation can not achieve automatic balancing.

It is worth noting that a general automatically balanced modulation method should achieve balancing under all circumstances. To solve the problem of the prior 4/2 modulation, this paper proposes a switching pattern using all the combinations of SM capacitors equally. Taking 4/2 modulation as an example, the improved switching pattern is shown in Table III. Four additional stages are added in this pattern and the corresponding equations about SM capacitor voltages can be obtained as

$$\begin{bmatrix} \boldsymbol{B}_{4/2} & \mathbf{1}_{6\times4} \\ \mathbf{1}_{6\times4} & \boldsymbol{B}_{4/2} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_{C_1}} \\ \boldsymbol{V_{C_2}} \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{6\times1} \\ \mathbf{1}_{6\times1} \end{bmatrix} V_M \tag{3}$$

with $\boldsymbol{B}_{4/2}$=$\begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$, $\boldsymbol{V_{C_1}}$=$\begin{bmatrix} V_{C_{11}} \\ V_{C_{12}} \\ V_{C_{13}} \\ V_{C_{14}} \end{bmatrix}$, and $\boldsymbol{V_{C_2}}$=$\begin{bmatrix} V_{C_{21}} \\ V_{C_{22}} \\ V_{C_{23}} \\ V_{C_{24}} \end{bmatrix}$.

In this improved switching pattern, the rank of $\boldsymbol{B}_{4/2}$ is four, so it is column full rank and the solution of (3) is unique. This means inherent-balancing can be achieved with the proposed modulation method.

The detailed waveforms of gate signals are illustrated in Fig. 2(a). It can be found that one switching cycle T_s contains six operation cycles, termed as T. It is worth noting that all the analysis above is based on an assumption that the voltage ripples of SM capacitors can be neglected. Actually, the gate signals of SM_{11} to SM_{24}, termed as S_{11} to S_{24}, are different within one T_s. This means that the transient voltages of SM capacitors are not exactly equal and the inherent-balancing mentioned before only refers to the balancing of SM capacitor average voltages, which can be written as

$$V_C = \frac{1}{T_s}\int_0^{T_s} v_{C_{11}}(t)dt = \ldots = \frac{1}{T_s}\int_0^{T_s} v_{C_{24}}(t)dt \tag{4}$$

The extent of transient imbalance is depended on the voltage ripples of SM capacitors, which will be introduced in Section IV.

From the Table III, it can be discovered that all the combinations of two capacitors are involved in the proposed switching pattern to achieve $v_{st1} = 2V_C$ and $v_{st2} = 2V_C$. This scheme can be extended to a general method. When there are N SMs in a stack and the stack voltage is MV_C, all $\binom{N}{M}$ combinations of SM capacitor should be used equally to achieve inherent-balancing. In addition, in order to reduce the stress of dv/dt applied on the transformer primary windings, three-level modulation or multilevel modulation can be used. Taking three-level modulation as another example, the detailed gate signal waveforms are illustrated in Fig. 2(b). Twenty-four stages are involved in one switching cycle T_s, among which the equivalent circuits of twelve stages are the same as that in Fig. 2(a), meaning that the equations of these twelve stages are the same as that in (3). Therefore, inherent-balancing ability is also guaranteed for 3-level modulation.

TABLE III
THE IMPROVED 4/2 SWITCHING PATTERN

Stage	Connected SM Capacitors							
1	C_{11}	C_{12}	C_{13}	C_{14}	C_{21}	C_{22}		
2	C_{11}	C_{12}			C_{21}	C_{22}	C_{23}	C_{24}
3	C_{11}	C_{12}	C_{13}	C_{14}		C_{22}	C_{23}	
4		C_{12}	C_{13}		C_{21}	C_{22}	C_{23}	C_{24}
5	C_{11}	C_{12}	C_{13}	C_{14}			C_{23}	C_{24}
6			C_{13}	C_{14}	C_{21}	C_{22}	C_{23}	C_{24}
7	C_{11}	C_{12}	C_{13}	C_{14}	C_{21}			C_{24}
8	C_{11}			C_{14}	C_{21}	C_{22}	C_{23}	C_{24}
9	C_{11}	C_{12}	C_{13}	C_{14}	C_{21}		C_{23}	
10	C_{11}		C_{13}		C_{21}	C_{22}	C_{23}	C_{24}
11	C_{11}	C_{12}	C_{13}	C_{14}		C_{22}		C_{24}
12		C_{12}		C_{14}	C_{21}	C_{22}	C_{23}	C_{24}

III. TRAPEZOIDAL CURRENT OPERATION

Combining the benefits of proposed balancing method and DAB scheme, this paper proposes a trapezoidal current modulation, which can achieve inherent-balancing and bidirectional power flow in MMC-based high step-ratio dc-dc converters.

A. Basic Operation Principles

The total step-ratio is the product of three factors, i.e., $V_M/V_L = \gamma_s\gamma_L\gamma_T$ (the step ratio of stacks γ_s, the inductor ratio γ_L, and the transformer turns ratio γ_T) with

$$\gamma_s = \frac{V_M}{|v_1|_{max}}, \tag{5}$$

$$\gamma_L = \frac{|v_1|_{max}}{|v_2|_{max}}, \tag{6}$$

and

$$\gamma_T = \frac{|v_2|_{max}}{V_L}, \tag{7}$$

where $|v_1|_{max}$ and $|v_2|_{max}$ are the maximum amplitudes of v_1 and v_2 respectively. If the maximum and minimum number of connected SM capacitor in a stack are defined as X and Y respectively, according to previous analysis, the voltage of SM capacitor can be calculated as

$$V_C = \frac{V_M}{X+Y}. \tag{8}$$

Assuming the voltage ripples of C_1 and C_2 can be negligible, v_1 is complementary to the ac components of v_{st1} because of Kirchhoff's voltage law. Therefore, the peak-to-peak value of

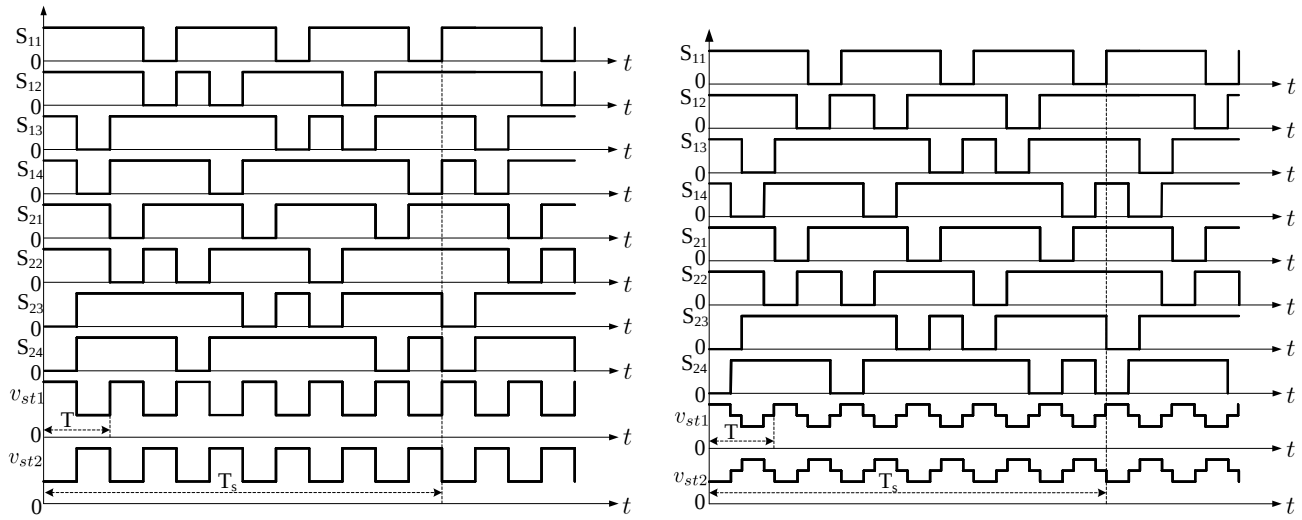

Fig. 2. The inherently-balanced modulation methods of stacks for $N = 4$ with (a) two-level voltage operation; (b) three-level voltage operation.

TABLE IV
ALL STEP-RATIOS FOR $N = 4$

X	Y	γ_s	V_C
4	3	14	$V_M/7$
4	2	6	$V_M/6$
4	1	10/3	$V_M/5$
4	0	2	$V_M/4$
3	2	10	$V_M/5$
3	1	4	$V_M/4$
3	0	2	$V_M/3$

v_1 is the same as that of v_{st1}. As the dc offset of v_1 is zero, its maximum amplitude can be obtained as

$$\begin{aligned} |v_1|_{max} &= \frac{1}{2}(v_{st1\,max} - v_{st1\,min}) \\ &= \frac{X-Y}{2(X+Y)}V_M. \end{aligned} \tag{9}$$

Therefore, the step-ratio of stacks is obtained as

$$\gamma_s = \frac{2(X+Y)}{X-Y} \geq 2. \tag{10}$$

Obviously, γ_s can not be smaller than two. For efficiency consideration, γ_L and γ_T can not be smaller than one, because it is less effective to step down the medium voltage with $\gamma_L < 1$ (a step-up stage).

From equation (10), it can be noticed that γ_s is depended on X and Y. For safe operation, usually one redundant SM can be used to replace the failed one. Therefore, it's better to set X to N or $N-1$ to fully utilize SMs. To make it clear, all the possible step-ratios based on $N = 4$ are presented in Table IV, in which six step-ratios can be generated. In practical applications, the number of SMs is much larger than four, so multiple step-ratios can be generated to meet different requirements.

The current of inductor L is controlled by v_1 and v_2, and six typical operation modes with a trapezoidal inductor current are shown in Fig. 3, in which D_1 and D_2 are the duty ratio of v_1 and v_2 respectively compared with one operation cycle T and d is the phase delay ratio from v_1 to v_2. When $d > 0$, the power is transmitted from the medium voltage side to the low voltage side, termed as forward power flow (see Fig. 3(a)-(e)). Conversely, when $d < 0$, the power is transmitted from the low voltage side to the medium voltage side, termed as reverse power flow (see Fig. 3(f)). Owing to the symmetry between them, only forward power flow is analyzed in detail in the following sections. Among Fig. 3(a)-(e), the competitively advantageous modes will be selected.

In order to achieve zero-current-switching (ZCS), it's desirable for a switch to be turned on or turned off with a zero current. In Fig. 3(a)-(c), the inductor current is zero at the switching instant of t_1, t_4, t_5 and t_8, while in Fig. 3(d) and (e) the currents at t_1-t_8 are not zero. Therefore, the modes of Fig. 3(a)-(c) achieve ZCS while the modes in Fig. 3(d) and (e) fail to do so.

Additionally, as can be seen in Fig. 3(d) and (e), the transient power in blue zones is negative, yielding circulating power and reducing the overall efficiency. In contrast, circulating powers are zero in Fig. 3(a)-(c).

In order to figure out the exact requirements of operating in ZCS and non-circulating-power mode, the inductor currents at t_1-t_4 are calculated in Table V. When

$$\begin{cases} \gamma_L D_1 = D_2 \\ \gamma_L D_1 + d \leq 0.5, \end{cases} \tag{11}$$

the currents at t_1 and t_4 are zero, and the currents of t_5 and t_8 are also zero because of symmetry. According to the two requirements in (11), two operation modes, named soft-switching non-circulating-power mode and hard-switching circulating-power mode, are separated and analyzed independently in the following two subsections.

B. Soft-switching and Non-circulating-power Mode

From the previous analysis, the operation modes of Fig. 3(a)-(c) belong to this case. To figure out a competitively

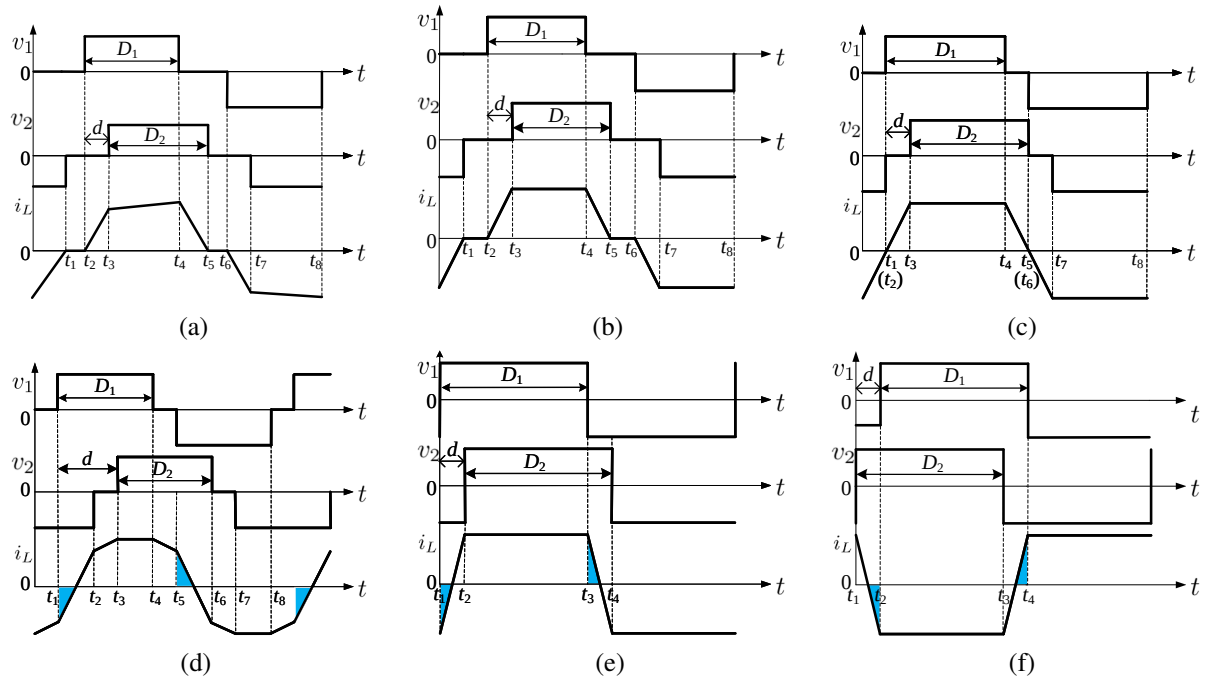

Fig. 3. Soft-switching and non-circulating-power mode with (a) $\gamma_L D_1 + d < 0.5$ and $\gamma_L > 1$, (b) $\gamma_L D_1 + d < 0.5$ and $\gamma_L = 1$, and (c) $\gamma_L D_1 + d = 0.5$ and $\gamma_L = 1$; hard-switching and circulating-power mode with (d) $\gamma_L D_1 + d > 0.5$ and $\gamma_L = 1$, (e) $D_1 = 0.5$ and $\gamma_L = 1$, and (f) reverse power flow.

TABLE V
INDUCTOR CURRENTS AT SWITCHING INSTANTS

i_L	$\gamma_L D_1 + d \leq 0.5$	$\gamma_L D_1 + d > 0.5$
$i_{L(t_1)}$	$-\frac{V_M}{2\gamma_s\gamma_L Lf}(\gamma_L D_1 - D_2)$	$\frac{V_M}{2\gamma_s\gamma_L Lf}(-\gamma_L D_1 - D_2 - 2d + 1)$
$i_{L(t_2)}$	$\frac{V_M}{2\gamma_s\gamma_L Lf}(D_2 - \gamma_L D_1 + 2\gamma_L d)$	$\frac{V_M}{2\gamma_s\gamma_L Lf}[-\gamma_L D_1 + (2\gamma_L + 1)D_2 + 2\gamma_L d - \gamma_L)]$
$i_{L(t_3)}$	$\frac{V_M}{2\gamma_s\gamma_L Lf}(D_2 + \gamma_L D_1 - 2D_1 + 2d)$	$\frac{V_M}{2\gamma_s\gamma_L Lf}(-\gamma_L D_1 + D_2 + 2\gamma_L d)$
$i_{L(t_4)}$	$\frac{V_M}{2\gamma_s\gamma_L Lf}(\gamma_L D_1 - D_2)$	$\frac{V_M}{2\gamma_s\gamma_L Lf}[(\gamma_L - 2)D_1 + D_2 + 2d]$

advantageous mode, the influence of γ_L and $\gamma_L D_1 + d$, which are the differences among these three modes, should be studied. As a general rule, the cost of an IGBT is partly depended on its current stress. The peak current of IGBTs on medium voltage side is the same as the peak value of i_{st1} and i_{st2}, which are calculated as

$$i_{st1} = I_{dc} + i_{ac1} = \frac{P}{V_M} + \frac{1}{2} i_L \tag{12}$$

and

$$i_{st2} = I_{dc} - i_{ac2} = \frac{P}{V_M} - \frac{1}{2} i_L \tag{13}$$

respectively, and the peak current of switches can be deduced as

$$\begin{aligned} i_{sw\,max} &= i_{st1\,max} = I_{dc} + |i_{ac1}|_{max} \\ &= \frac{P}{V_M} + \frac{V_M}{2\gamma_s Lf}[d + \frac{\gamma_L - 1}{\gamma_L}(D_1 - d)], \end{aligned} \tag{14}$$

in which $f = 1/T$. As $\gamma_L \geq 1$, the peak current is minimized when $\gamma_L = 1$.

Among various sorts of power losses in high-step ratio dc-dc converters, conduction losses normally reign supreme in that the operation frequency is competitively low. For an IGBT, its collector-emitter voltage is approximately constant when turned on. Provided the voltage drops of IGBTs and its anti-paralleled diodes are identical, the conduction losses are proportional to the absolute average value of inductor current, which can be calculated as

$$\begin{aligned} \langle |i_L| \rangle_T &= \frac{1}{T} \int_0^T |i_L(t)| dt \\ &= \frac{V_M}{\gamma_s Lf} D_1 [2d + (\gamma_L - 1) D_1]. \end{aligned} \tag{15}$$

When $\gamma_L = 1$, $\langle |i_L| \rangle_T$ can be minimize , thereby diminishing conduction losses. Considering current stress and conduction losses, the operation modes in Fig. 3(b) and (c) are more desirable than the one in Fig. 3(a). In order to simplify the analysis, γ_L is selected as one in the following analysis.

The aim of control is to minimize conduction losses under the same transmitted power, which is calculated as

$$P = \frac{1}{T} \int_0^T v_1(t) i_L(t) dt = \frac{V_M^2}{\gamma_s^2 Lf} [d(2D_1 - d)]. \tag{16}$$

Assuming the base power and base current are defined as

$$P_{base} = \frac{V_M^2}{8\gamma_s^2 Lf} \tag{17}$$

and

$$\langle|i_L|\rangle_{T\,base} = \frac{V_M}{8\gamma_s L f} \tag{18}$$

respectively, the per-unit value of P and $\langle|i_L|\rangle_T$ are obtained as

$$P^* = 8d(2D_1 - d) \tag{19}$$

and

$$\langle|i_L|\rangle_T^* = 16D_1 d \tag{20}$$

respectively. From (19) and (20), the relationship between P^* and $\langle|i_L|\rangle_T^*$ is deduced as

$$\langle|i_L|\rangle_T^* = P^* + 8d^2. \tag{21}$$

It can be discovered that minimizing d can minimize $\langle|i_L|\rangle_T^*$, thereby minimizing the conduction losses. Moreover, from (14) we can also find with the smallest d, the current stress can also be minimized. From (19), the relationship between D_1 and d is acquired as

$$d = D_1 - \sqrt{D_1^2 - \frac{P^*}{8}}. \tag{22}$$

The derivative of d with respect to D_1 is negative, i.e.,

$$d'(D_1) = 1 - \frac{D_1}{\sqrt{D_1^2 - \frac{P^*}{8}}} < 0. \tag{23}$$

Thus, when D_1 becomes larger, d is smaller. In this operation mode, due to the limitation of $D_1 + d \leq 0.5$, when $D_1 = 0.5 - d$, d can be minimized. This means the operation mode of Fig. 3(c) is more suitable than that of Fig. 3(b). Therefore, it is beneficial to use the mode of Fig. 3(c) to achieve soft-switching and non-circulating-power operation. Substituting $D_1 = 0.5 - d$ into (19), d can be calculated as

$$d = \frac{1 - \sqrt{1 - 1.5P^*}}{6}. \tag{24}$$

Under this control scheme, only d is the parameter we should control.

C. Hard-switching and Circulating-power Mode

In this case, two typical operation modes are shown in Fig. 3(d) and (f). In this mode, it is inevitable to introduce some circulating power, thereby leading to a relatively low efficiency. However, the transmitted power in this mode can be larger than the previous one. In the first mode, according to the equation (19), the maximum per-unit power is $2/3$ when $D_1 = 1/3$ and $d = 1/6$.

In the second mode, the power can be calculated as

$$P = \frac{V_M^2}{\gamma_s^2 L f}(D_1 - D_1^2 + d - 2d^2 - 0.25) \tag{25}$$

Normalizing P with the base value in (17), the per-unit power can be obtained as

$$P^* = 8(D_1 - D_1^2 + d - 2d^2 - 0.25). \tag{26}$$

From (26), the maximum per-unit power is 1 when $D_1 = 1/2$ and $d = 1/4$. In order to make it clear, a 3-D plot of transmitted power with respect of D_1 and d is illustrated in Fig. 4. Despite low efficiency, the second mode is still valuable because it can provide some power margin in case of a heavy load.

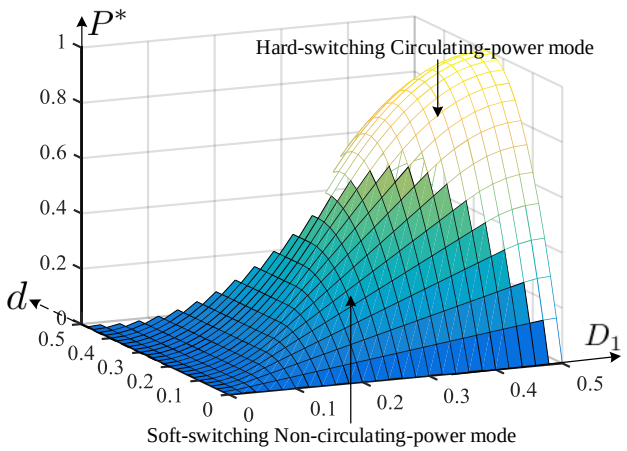

Fig. 4. Per-unit power with respect of D_1 and d.

In this operation mode, the introducing of circulating power will increase conduction losses, switching losses and transformer losses. To simplify the analysis, only conduction losses are considered here. Similar to the previous operation mode, the absolute average inductor current and its per-unit value based on the base value in (18) can be calculated as

$$\langle|i_L|\rangle_T = \frac{V_M}{\gamma_s L f}(D_1 - D_1^2 + d - d^2 - 0.25) \tag{27}$$

and

$$\langle|i_L|\rangle_T^* = 8(D_1 - D_1^2 + d - d^2 - 0.25) \tag{28}$$

respectively. The relationship between P^* and $\langle|i_L|\rangle_T^*$ is acquired as

$$\langle|i_L|\rangle_T^* = P^* + 8d^2, \tag{29}$$

the same as that in (22). Similarly, d also needs to be minimized in the second mode. From (25), the relationship between d and D_1 is deduced as

$$d = \frac{1 - \sqrt{8(D_1 - D_1^2) - P^* - 1}}{4}, \tag{30}$$

in which the derivative of d with respect to D_1 is negative, i.e.,

$$d'(D_1) = \frac{2D_1 - 1}{\sqrt{8(D_1 - D_1^2) - P^* - 1}} < 0. \tag{31}$$

In order to minimize d, D_1 should be as large as possible, meaning that the two-level voltage operation mode is more suitable for the second mode. Thus, the operation mode in Fig. 3(e) is advantageous compared with the mode in Fig. 3(d). Substituting $D_1 = 0.5$ into equation (30), d is obtained as

$$d = \frac{1 - \sqrt{1 - P^*}}{4}. \tag{32}$$

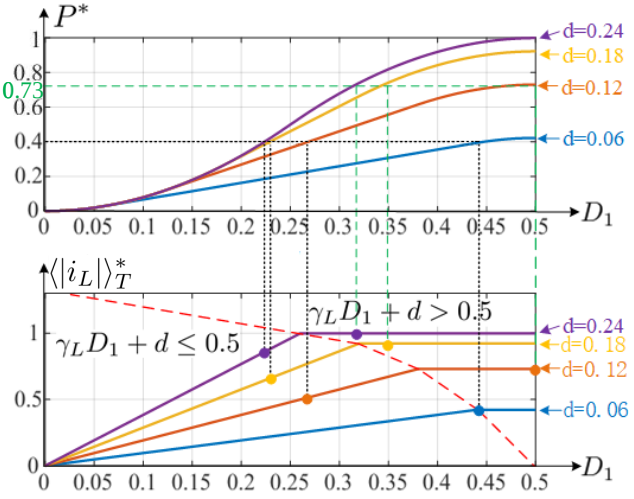

Fig. 5. The average current with respect of D_1 and d under the same power

D. Control Scheme

According to the previous analysis, it is better to use the operation modes in Fig. 3(c) and (e). Both operation modes have their own advantages. For the mode of Fig. 3(c), soft-switching is achieved and the circulating power is zero, meaning that the efficiency is higher in this operation mode. In the mode of Fig. 3(e), the transferred power can be larger but the efficiency is a little bit lower. Based on the equations deduced before, the relationship among P^*, $\langle|i_L|\rangle_T^*$, D_1 and d is shown in Fig. 5. Taking $P^* = 0.4$ and $P^* = 0.73$ as two examples, the configuration of $P^* = 0.4$ is $D_1 = 0.44$ and $d = 0.06$ while if $P^* = 0.73$, the corresponding configuration is $D_1 = 0.5$ and $d = 0.12$.

The control scheme is a combination of feedback and feedforward control (see Fig. 6), including four input signals and four output signals. When a severe fluctuation happens on DC grid, γ_s should be adjusted first to set γ_L close to one. When entering into normal operation, the operation mode is chosen according to the power reference. In the first operation mode, the range of per-unit power P^* is from 0 to 2/3, while the range in the second mode is from 0 to 1. Therefore, $P^* = 2/3$ is used as a threshold to choose the operation mode. The d_0 is the theoretical value of d, which is calculated by equations (24) and (32). The actual power is calculated from the voltage and current feedbacks. The fine-tuning of d, termed as Δd, is calculated via a PI controller by the difference between actual power and power reference. The final d is calculated as $d = d_0 + \Delta d$. According to the previous analysis, D_1 and D_2 are calculated as

$$\begin{cases} D_1 = 0.5 - d & (P^* \leq 2/3) \\ D_1 = 0.5 & (P^* > 2/3) \end{cases} \tag{33}$$

and

$$\begin{cases} D_2 = \gamma_L D_1 & (P^* \leq 2/3); \\ D_2 = 0.5 & (P^* > 2/3) \end{cases} \tag{34}$$

respectively.

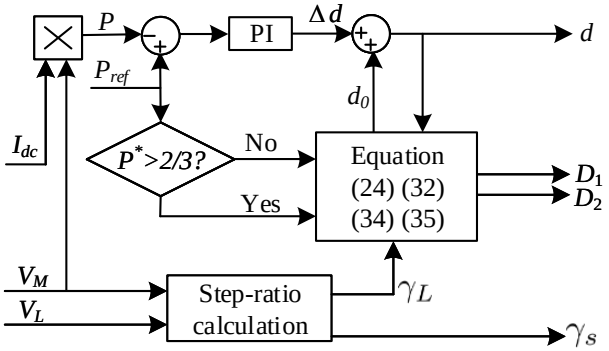

Fig. 6. Conduction-losses-minimized control model of MDCC

IV. Capacitor Voltage Ripple Reduction

In Section II, complete automatic balancing of SM capacitor average voltage has been realized. Actually, the transient voltages of SM capacitors are not exactly the same, and the degree of transient imbalance is depended on the maximum ripple, which will be introduced in this section.

Taking the improved 4/2 modulation as an example, six operation cycles are involved in one switching cycle. The sequence of those six operation cycles does not affect inherent-balancing ability but it will affect the maximum voltage ripple of SM capacitor. If a SM capacitor is charged and discharged alternately, its voltage ripple is small. In contrast, large voltage ripples are yielded by consecutive charging or discharging periods. In order to make it clear, two different switching patterns, producing the same v_1, are compared in Fig. 7(a) and (b).

In the first half cycle, $v_{st1} = 4V_C$, yielding a negative v_1. For forward power flow, the average value of i_L is negative when $v_1 < 0$ (see Fig. 3(d)). If equal division of i_L is achieved, the average value of i_{s1} in this period is deduced as

$$\begin{aligned} \langle i_{s1}\rangle_{T_1} &= \frac{2}{T}\int_0^{\frac{T}{2}} (\frac{i_L}{2} + I_{dc})dt = -\frac{V_M}{|v_1|_{max}} I_{dc} + I_{dc} \\ &= (1 - \frac{\gamma_s}{2}) I_{dc} \leq 0. \end{aligned} \tag{35}$$

From the analysis before, $\gamma_s \geq 2$. Therefore, $\langle i_{s1}\rangle_{T_1}$ is negative and all the SM capacitors in Stack 1 are discharged in the first half cycle.

In contrast, in the second half cycle, $v_{st1} = 2V_C$, producing a positive v_1. From Fig. 3(d), the average value of i_L is positive when $v_1 > 0$. The average value of i_{s1} in this period is deduced as

$$\begin{aligned} \langle i_{s1}\rangle_{T_2} &= \frac{2}{T}\int_{\frac{T}{2}}^{T} (\frac{i_L}{2} + I_{dc})dt = \frac{V_M}{|v_1|_{max}} I_{dc} + I_{dc} \\ &= (1 + \frac{\gamma_s}{2}) I_{dc} > 0. \end{aligned} \tag{36}$$

Thus, in the second half cycle, those two connected SM capacitors are charged but the voltages of the other two bypassed SM capacitors remain unchanged. When the next operation cycle begins, those two bypassed SM capacitors are discharged again. As a result, their voltage ripples become large.

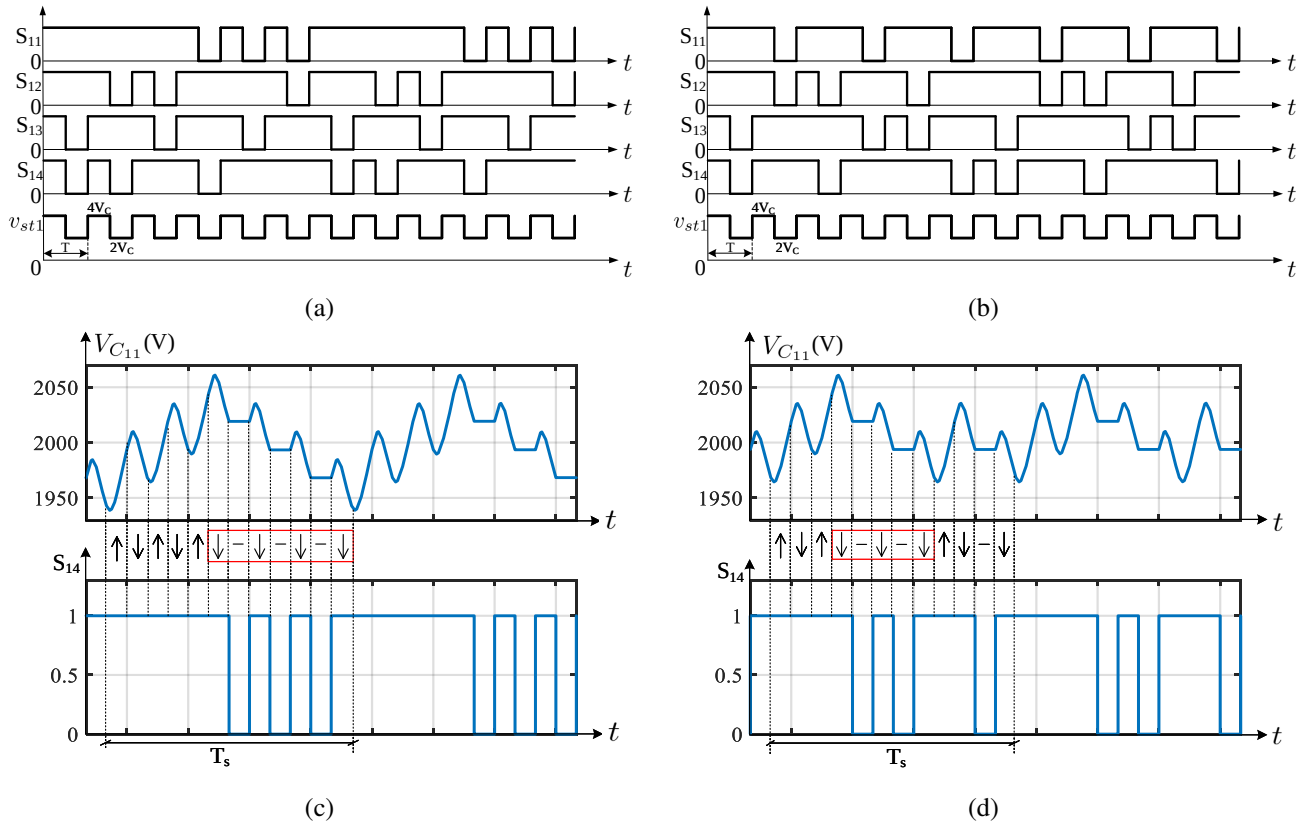

Fig. 7. Comparison of 2 different modulation methods based on maximum SM capacitor ripples. (a) The first modulation method. (b) The second modulation method. (c) The voltage ripple of the first modulation method. (d) The voltage ripple of the second modulation method.

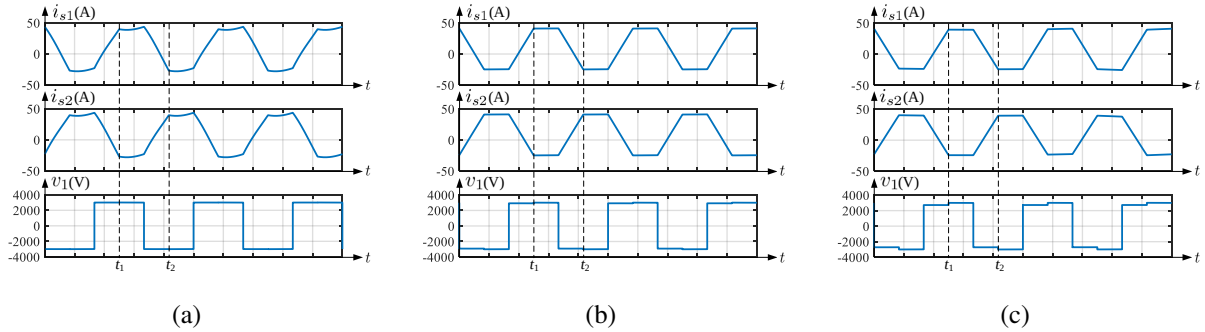

Fig. 8. The current sharing performance between 2 stacks with (a) $L_{s1,2}/L = 0.3\%$, (b) $L_{s1,2}/L = 3\%$ and (c) $L_{s1,2}/L = 10\%$.

Based on the same specification ($V_M = 12$kV, $V_L = 1$kV and $P_{max} = 45$kW), the simulation waveforms of $V_{C_{11}}$ and gate signal S_{11} with those two modulations in Fig. 7(a) and (b) are illustrated in Fig. 7(c) and (d) respectively. The charging and discharging periods of C_{11} are represented by the direction of a set of arrows. Additionally, the periods when C_{11} is bypassed are represented by horizontal lines. For the first modulation method, C_{11} undergoes 4 consecutive discharging periods. In contrast, for the second modulation method, only 3 consecutive discharging periods exist. The simulation result of the maximum voltage ripple yielded by the second modulation is 79% of that produced by the first modulation. It can be found that when a negative pulse appears in a gate signal, two consecutive discharging periods are yielded. Therefore, in order to minimize the voltage ripple of SM capacitors, it is preferable to minimize the number of consecutive negative pulses in gate signals. In optimized modulation, this minimum number is $X - Y$.

V. Design Example

In this section, with the ratings shown in Table VI, a case study is provided to explain the design process. The first step is dividing the total step-ratio into two parts (γ_s and γ_T). It's better to set γ_L near to one. Various allocations exist and an example of $\gamma_s = 6$ and $\gamma_T = 2.5$ is used here. The allocation in practical applications is a trade-off between the efficiencies of stacks and transformer. The number of SM is depended on the voltage stress of IGBTs. If ABB 5SNG 0150P450300

TABLE VI
RATING OF CASE STUDY

Symbol	Description	Value
P	Power	100 kW
V_M	Medium Voltage	18 KV
V_L	Low Voltage	1.2 kV

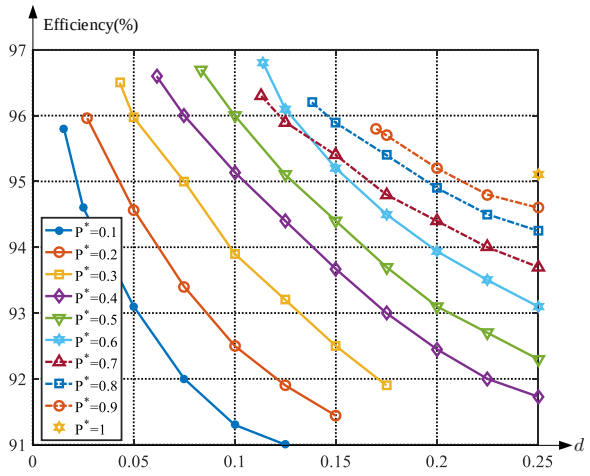

Fig. 9. The simulation results of efficiency with different powers and phase shifts.

($V_{CE} = 4500$V, $I_c = 150$A) is used in SMs, $N = 4$. In this case study, the modulation method is the same as that shown in Fig. 2(a) and (b).

The selection of inductor L is related to the maximum transmitted power. Substituting $D_1 = 0.5$ and $d = 0.25$ into (25), L is calculated as 3.75mH. The selection of SM capacitor is depended on the maximum tolerance of voltage ripple. The values of series inductors are related to the current sharing performance between two stacks. Assuming $L_{s1} = L_{s2}$, the simulation waveforms of i_{s1}, i_{s2} and v_1 are illustrated in Fig. 8 with different values of L_{s1}. When series inductors are too small, equal division of i_L can not be guaranteed (see Fig. 8(a)). In contrast, large series inductors will produce too much voltage drops. If $L_{s1}/L \geq 10\%$, obvious voltage steps are produced on the waveform of v_1 at t_1 and t_2 due to the change of di_L/dt (see Fig. 8(c)). Under this condition, the peak current of transformer is larger than before. A good trade-off is achieved when L_{s1} and L_{s2} are 1%-5% of L. In this case study, $L_{s1} = L_{s2} = 112.5\mu H$.

Based on different transmitted powers, the relationship between simulation efficiency and phase shift is shown in Fig. 9. It can be noticed that under the same transmitted power, the efficiency is higher with smaller d. Moreover, the highest efficiency of $0.3 \leq P^* \leq 2/3$ is higher than that of $P^* > 2/3$ due to less switching losses and circulating power. When $P^* < 0.3$, owing to poor device utilization, the efficiency is lower than that of $0.3 \leq P^* \leq 2/3$.

VI. EXPERIMENTAL RESULTS

The theoretical analysis is validated by the experimental results based on a down-scaled prototype, in which four SMs are deployed in one stack. Therefore, 20 IGBTs in total are involved in this prototype, which are controlled by a digital signal processor (DSP) and a FPGA. The detailed parameters of this prototype are listed in Table VII.

TABLE VII
EXPERIMENTAL PARAMETERS

Symbol	Description	Value
V_M	Medium voltage	1500 V
V_L	Low voltage	100 V
P_{max}	Maximum transmitted power	789 W
f	Operation frequency	3 kHz
L	Inductor	$3.3mH$
L_s	Series inductor	110 μH
L_a	Primary side leakage inductor	50 μH
L_b	Secondary side leakage inductor	8 μH
L_m	Magnetizing inductor	460 mH
γ_T	Transformer step-ratio	2.5
C_1, C_2	Shunt capacitor	550 μF

For forward power flow, the experimental waveforms of $P^* = 2/3$ are illustrated in Fig. 10. According to the equations deduced before, in this case, $D_1 = D_2 = 1/3$ and $d = 1/6$. The voltage and current waveforms of inductor L are shown in Fig. 10(a). In the dead zones of SMs and active bridge, resonance happens between the inductor L and the parasitic capacitors of IGBTs. Thus, the peak voltage exists at the switching instants. The current sharing performance between two stacks is shown in Fig. 10(b). The inductor current i_L is divided between two stacks approximately equally. A phase shift of π is produced between i_{s1} and i_{s2} because of the complementary operation of two stacks (see Fig. 10(c)). In forward power flow mode, I_{dc} is positive. Thus, the average values of i_{s1} and i_{s2} are positive. To demonstrate the soft-switching ability, the voltages and currents of both switches in SMs are shown in Fig. 10(d). In addition, the voltage and current of S_1 is illustrated in Fig. 10(e). It can be found that for switches in SMs, they realize soft-switching for most of the time and for switches in active bridge, they achieve soft-switching all the time. The modulation method of Stack 1 is shown in Fig. 10(f) by the output voltages of SMs, the same as that shown in Fig. 2(b).

The experimental waveforms of $P^* = 1$ are shown in Fig. 11. In this case, the voltage and current of inductor are illustrated in Fig. 11(a). The maximum value of i_L is larger than that of Fig. 10(a) because the transmitted power is larger in this operation mode. However, the circulating power is produced in this case. The current sharing performance is shown in Fig. 11(b), in which the average values of i_{s1} and i_{s2} are higher than that of Fig. 10(b) due to the larger I_{dc} in this operation mode. The voltages and currents of two stacks are shown in Fig. 11(c). In this operation mode, according to the analysis before, $D_1 = D_2 = 0.5$, so two complementary square wave voltages are produced on the two stacks. The soft-switching performance is illustrated in Fig. 11(d) and (e), in which some soft-switching instants in Fig. 10(d) and (e) are now hard-switching, yielding larger switching losses. The output voltages of SMs are shown in Fig. 11(f) to introduce the modulation method, the same as that shown in Fig. 2(a).

When it comes to reverse power flow, the experimental

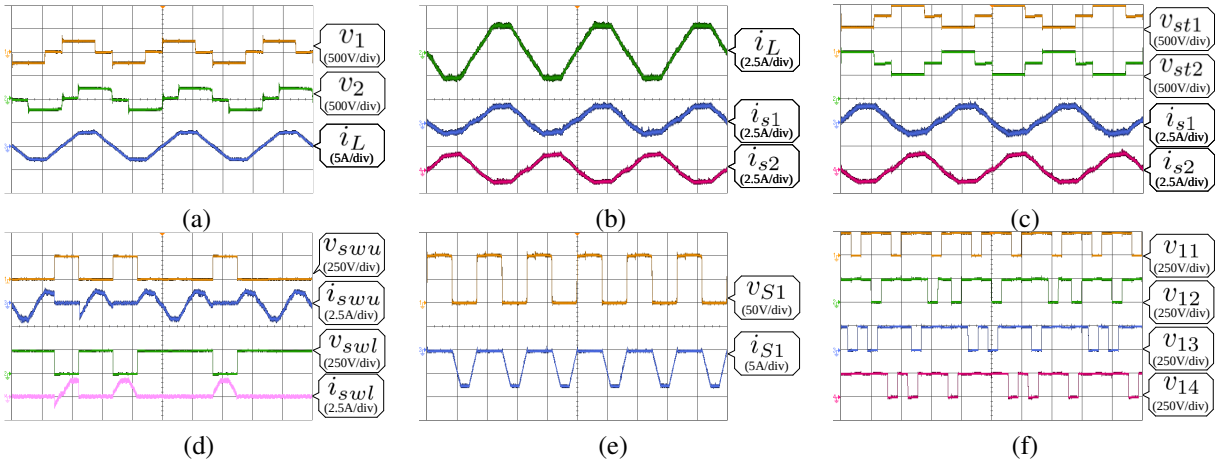

Fig. 10. Experimental waveforms of forward power flow with $P^* = 2/3$. (X–axis: Time, 100 μs/div): (a) voltage and current of inductor; (b) current sharing performance between two stacks; (c) voltages and currents of stacks. (X–axis: Time, 200 μs/div): (d) voltages and currents of upper switch (v_{swu} and i_{swu}) and lower switch (v_{swl} and i_{swl}) in SMs; (e) voltage and current of the switch S_1 in active bridge. (X–axis: Time, 500 μs/div): (f) SM output voltages.

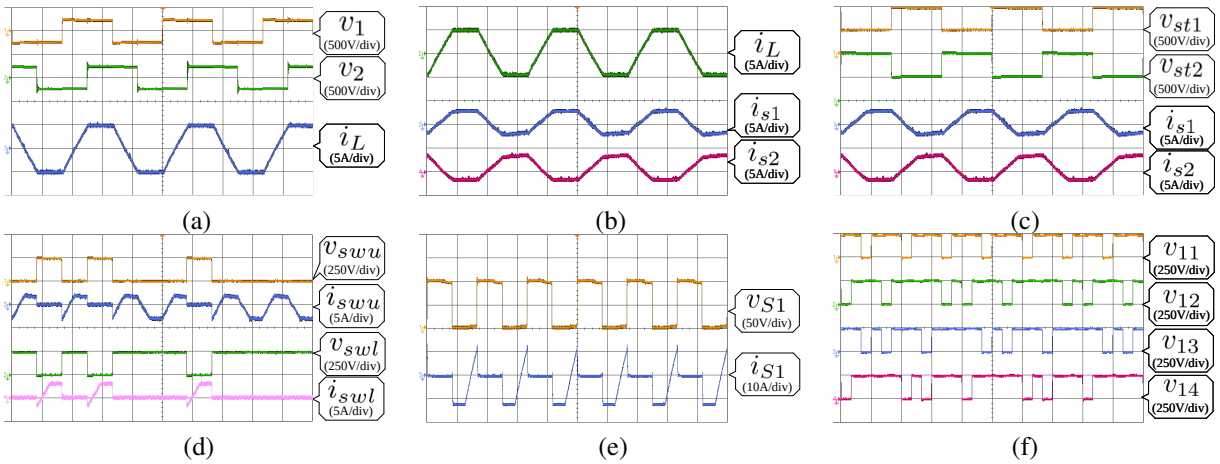

Fig. 11. Experimental waveforms of forward power flow with $P^* = 1$. (X–axis: Time, 100 μs/div): (a) voltage and current of inductor; (b) current sharing performance between two stacks; (c) voltages and currents of stacks. (X–axis: Time, 200 μs/div): (d) voltages and currents of upper switch (v_{swu} and i_{swu}) and lower switch (v_{swl} and i_{swl}) in SMs; (e) voltage and current of the switch S_1 in active bridge. (X–axis: Time, 500 μs/div): (f) SM output voltages.

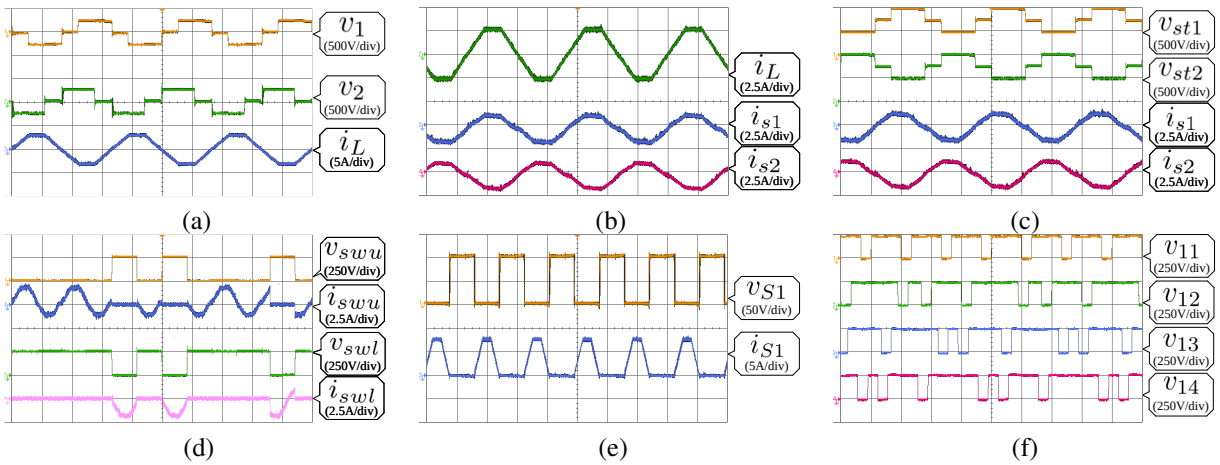

Fig. 12. Experimental waveforms of reverse power flow with $P^* = -2/3$. (X–axis: Time, 100 μs/div): (a) voltage and current of inductor; (b) current sharing performance between two stacks; (c) voltages and currents of stacks. (X–axis: Time, 200 μs/div): (d) voltages and currents of upper switch (v_{swu} and i_{swu}) and lower switch (v_{swl} and i_{swl}) in SMs; (e) voltage and current of the switch S_1 in active bridge. (X–axis: Time, 500 μs/div): (f) SM output voltages.

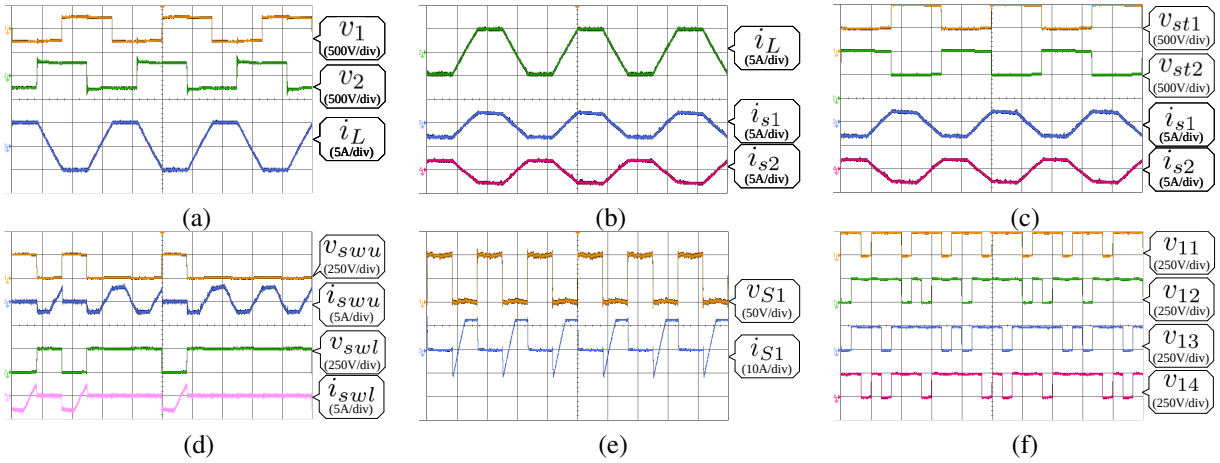

Fig. 13. Experimental waveforms of reverse power flow with $P^* = -1$. (X–axis: Time, 100 μs/div): (a) voltage and current of inductor; (b) current sharing performance between two stacks; (c) voltages and currents of stacks. (X–axis: Time, 200 μs/div): (d) voltages and currents of upper switch (v_{swu} and i_{swu}) and lower switch (v_{swl} and i_{swl}) in SMs; (e) voltage and current of the switch S_1 in active bridge. (X–axis: Time, 500 μs/div): (f) SM output voltages.

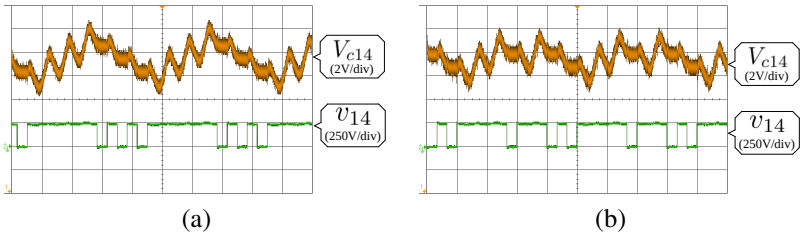

Fig. 14. Experimental waveforms of SM capacitor voltage and SM output voltage(X–axis: Time, 500 μs/div). (a) Large voltage ripple modulation. (b) Small voltage ripple modulation.

TABLE VIII
THE VOLTAGES OF SM CAPACITORS

	Stack 1				Stack 2					
P^*	$V_{C_{11}}$(V)	$V_{C_{12}}$(V)	$V_{C_{13}}$(V)	$V_{C_{14}}$(V)	$V_{C_{21}}$(V)	$V_{C_{22}}$(V)	$V_{C_{23}}$(V)	$V_{C_{24}}$(V)	V_{C_1}(V)	V_{C_2}(V)
2/3	250	249	250	250	249	249	250	250	750	749
1	250	250	249	250	250	249	250	250	750	749
-2/3	249	250	249	250	249	250	249	250	749	750
-1	249	249	250	250	250	249	249	250	749	750
traditional 4/2 modulation	241.5	255	240	257	254	246	255.5	245.5	749	749

TABLE IX
THE EXPERIMENTAL EFFICIENCY

P^*	1	2/3	1/3	-1/3	-2/3	-1
Efficiency	92.4%	93.2%	92.6%	92.8%	93.5%	92.7%

waveforms of $P^* = -2/3$ are shown in Fig. 12. Compared with forward power flow, d is negative in this operation mode, meaning that v_1 has a phase lag compared with v_2 (see Fig. 12(a)). The current sharing performance is illustrated in Fig. 12(b). For reverse power flow, I_{dc} is negative, so the average values of i_{s1} and i_{s2} are negative, contrary to that of Fig. 10(b). The soft-switching performance and modulation method of $P^* = -2/3$ are similar with that of $P^* = 2/3$ (see Fig. 12(d), (e), and (f)).

When maximum reverse power ($P^* = -1$) is transferred in the proposed converter, the experimental waveforms are illustrated in Fig. 13. For this operation mode, $D_1 = D_2 = 0.5$ and $d = -0.25$ (see Fig. 13(a)). The current sharing performance is shown in Fig. 13(b). The average values of i_{s1} and i_{s2} are also negative. The soft-switching performance and modulation method of $P^* = -1$ is similar to that of $P^* = 1$ (see Fig. 13(d),(e), and(f)).

As mentioned in Section IV, the voltage ripple of SM capacitor is related to the modulation method of stacks. For the modulation methods shown in Fig. 7(a) and (b), the experimental waveforms of SM capacitor voltage and its corresponding SM output voltage are shown in Fig. 14(a) and (b) respectively. It can be noticed that the voltage ripple of Fig. 14(b) is 83% of that of Fig. 14(a), close to the simulation results shown in Fig. 7(c) and (d).

Inherent-balancing ability is a key feature of proposed modulation method. The experimental SM capacitor voltages are illustrated in Table VIII. It can be found that the proposed

converter realizes inherent-balancing under different powers without extra balancing control. Due to voltage ripples of SM capacitors, slight differences exist among these voltages. In contrast, when using the prior 4/2 modulation method, the corresponding SM capacitor voltages are also listed in Table VIII. In the traditional method, the odd-numbered SM capacitors of Stack 1 have higher voltage than their even-numbered counterparts while the adverse pattern can be found in Stack 2. Thus, in this case the balancing among SM capacitor voltages can not be achieved by the prior scheme, and some extra limitations are required during designing.

The experimental efficiency is shown in Table IX. For forward power flow, the efficiency of $P^* = 2/3$ is the highest. When $P^* = 1$, hard-switching and circulating power will undermine the overall efficiency, and the low device utilization contributes to the relatively low efficiency when $P^* = 1/3$. Compared with forward mode, the efficiency of reverse mode is a little bit higher. In both modes the ac currents are the same, but I_{dc} is negative in reverse mode and it will flow through the anti-paralleled diode of IGBT. The power losses of a diode is normally lower than that of an IGBT under the same power rating, so the efficiency of reverse mode is higher than forward mode. Compared with simulation efficiency in Fig. 9, the efficiency in experiment is slightly lower. Owing to the safety regulations of the laboratory, the medium voltage V_M can not be high enough to achieve high device utilization, which holds the key to a desirable efficiency.

VII. Conclusion

A trapezoidal current modulation of MDCC has been proposed for the bidirectional high step-ratio interconnection between MVDC and LVDC systems. With this modulation method, the SM capacitor voltages are inherently-balanced without extra feedback control. Two operation modes are involved in this scheme. The three-level operation mode is preferable for small power transmission because of soft-switching and zero circulating power. In contrast, the two-level operation mode is capable of transmitting large power. In both modes, the conduction losses can be minimized with the least phase shift modulation scheme. Besides, the SM capacitor voltage ripple can be reduced by an optimized switching pattern. The analytical study indicates that the modulation method is a trade-off between the balancing performance and the volume of SM capacitor. A good trade-off is achieved in full-scale simulation and down-scaled experiment by selecting appropriate parameters. The result shows that the modulation strategy is suitable for high step-ratio MDCC.

References

[1] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power dc/dc converters for offshore wind energy systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013.

[2] H. Li, W. Li, M. Luo, A. Monti, and F. Ponci, "Design of smart mvdc power grid protection," *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 9, pp. 3035–3046, Sep. 2011.

[3] A. Gómez-Expósito, J. M. Mauricio, and J. M. Maza-Ortega, "Vsc-based mvdc railway electrification system," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 422–431, Feb. 2014.

[4] C. Zhan, C. Smith, A. Crane, A. Bullock, and D. Grieve, "Dc transmission and distribution system for a large offshore wind farm," *in 9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, pp. 1–5, 2010.

[5] M. Stieneker and R. W. D. Doncker, "Medium-voltage dc distribution grids in urban areas," *in 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–7, 2016.

[6] H. A. B. Siddique, S. M. Ali, and R. W. D. Doncker, "Dc collector grid configurations for large photovoltaic parks," *in 2013 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1–10, 2013.

[7] L. Zhang, K. Sun, Y. Xing, L. Feng, and H. Ge, "A modular grid-connected photovoltaic generation system based on dc bus," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 523–531, Feb. 2011.

[8] S. Lumbreras and A. Ramos, "Optimal design of the electrical layout of an offshore wind farm applying decomposition strategies," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 1434–1441, May 2013.

[9] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[10] X. Li and Y.-F. Li, "An optimized phase-shift modulation for fast transient response in a dual-active-bridge converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2661–2665, June 2014.

[11] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3931–3940, Aug. 2013.

[12] M. Sato, K. Domoto, Y. Ishizuka, S. Manabe, H. Okubo, M. Yamaguchi, and A. Itagaki, "High efficiency design for isop converter system with dual active bridge dc-dc converter," *in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2465–2472, 2016.

[13] T. Todorčević, R. van Kessel, P. Bauer, and J. A. Ferreira, "A modulation strategy for wide voltage output in dab-based dc–dc modular multilevel converter for deap wave energy conversion," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1171–1181, Dec. 2015.

[14] X. Wang, J. Liu, S. Ouyang, T. Xu, F. Meng, and S. Song, "Control and experiment of an h-bridge-based three-phase three-stage modular power electronic transformer," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2002–2011, Mar. 2016.

[15] P. Zumel, L. Ortega, A. Lázaro, C. Fernández, A. Barrado, A. Rodríguez, and M. M. Hernando, "Modular dual-active bridge converter architecture," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2444–2455, May/June 2016.

[16] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[17] H. Yang, J. Qin, S. Debnath, and M. Saeedifard, "Phasor domain steady-state modeling and design of the dc–dc modular multilevel converter," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2054–2063, Oct. 2016.

[18] J. Ferreira, "The multilevel modular dc converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[19] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A novel medium-voltage modular multilevel dc–dc converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7939–7949, Dec. 2016.

[20] W. Lin and D. Jovcic, "Average modelling of medium frequency dc–dc converters in dynamic studies," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 281–289, Feb. 2015.

[21] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for hvdc interconnects," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 148–162, Jan 2015.

[22] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. D. Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan 2015.

[23] X. Xiang, X. Zhang, T. Luth, M. M. C. Merlin, and T. C. Green, "A compact modular multilevel dc–dc converter for high step-ratio mv and hv use," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 7060–7071, Sep. 2018.

[24] T. Lüth, M. Merlin, and T. Green, "Modular multilevel dc/dc converter architectures for hvdc taps," *in 2014 16th European Conference on Power Electronics and Applications*, pp. 1–10, 2014.
[25] M. A. Elgenedy, A. Darwish, S. Ahmed, and B. W. Williams, "A transition arm modular multilevel universal pulse-waveform generator for electroporation applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8979–8991, Dec. 2017.
[26] S. Shao, M. Jiang, J. Zhang, and X. Wu, "A capacitor voltage balancing method for a modular multilevel dc transformer for dc distribution system," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3002–3011, April 2018.
[27] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4873–4879, Nov. 2013.
[28] E. Solas, G. Abad, J. A. Barrena, A. Carear, and S. Aurtenetxea, "Modulation of modular multilevel converter for hvdc application," *in Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010*, pp. T2–84–T2–89, 2010.
[29] X. She, A. Huang, X. Ni, and R. Burgos, "Ac circulating currents suppression in modular multilevel converter," *in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pp. 191–196, 2012.
[30] T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107–4115, Aug 2014.
[31] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, Feb. 2014.
[32] X. Zhang, X. Xiang, T. C. Green, and X. Yang, "Operation and performance of resonant modular multilevel converter with flexible step ratio," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6276–6286, Aug. 2017.
[33] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "High-frequency-link modulation methodology of dc-dc transformer based on modular multilevel converter for hvdc application: Comprehensive analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3413–3424, May 2017.
[34] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Modular multilevel structure of a high power dual active bridge dc transformer with stepped two-level output," *in 2014 16th European Conference on Power Electronics and Applications*, pp. 1–10, 2014.
[35] P. Li, G. P. Adam, D. Holliday, and B. Williams, "Controlled transition full-bridge hybrid multilevel converter with chain-links of full-bridge cells," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 23–28, Jan. 2017.
[36] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 108–123, Jan 2015.
[37] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams, "Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage dc-dc transformers," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5439–5457, Oct. 2015.
[38] P. Li, G. P. Adam, S. J. Finney, and D. Holliday, "Operation analysis of thyristor-based front-to-front active-forced-commutated bridge dc transformer in lcc and vsc hybrid hvdc networks," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1657–1669, Dec. 2017.
[39] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 89–98, Jan. 2015.

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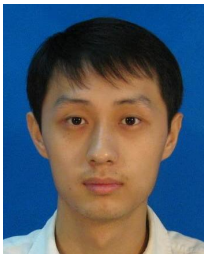

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