A Hybrid Modulation Technique for the DC-Bus Voltage Balancing in a Three-Phase NPC Converter

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***Abstract* — In this paper a new pulse width modulation technique for three-phase neutral point clamped (NPC) converter is presented, with the aim to actively control the dc-bus capacitors' voltages. To meet this requirement, usually NPC modulation techniques are either based on the sole common mode voltage injection (*CMI*) or on the sole multi-step (*MS*) switching mode of operation. Contrarily, the presented approach combines these two strategies, taking advantages of all their main benefits while keeping the switching transitions to the minimum required number. The approach has been numerically tested and compared with some of the other strategies, showing an overall better behaviour, especially for high modulation indices.**

Keywords — Diode Clamped, Neutral Point Clamped, Multilevel Converter, Pulse Width Modulation, Voltage Balancing.

I. Introduction

The neutral point clamped (NPC) converter is, at present, among the most widely used multilevel topologies both for industry and for grid-connected applications [1]. One of its main drawbacks is the need for control of the dc-bus capacitors' voltages which, in standard applications, should be equally balanced around their rated values, in order not to stress neither the capacitors nor the switching devices [2-3]. Standard pulse width modulation (PWM) approaches for multilevel converters do not actively address this requirement and, as a result, voltage fluctuations or even instability may arise [3].

Many solutions have been proposed to solve this problem. Some of them are based on additional hardware balancing circuits [4], while others exploit a proper modification of the modulation technique via software.

Most of these software strategies, either based on space vector (SV) [5-7] or on carrier-based (CB) modulation methods [8-11], exploit a common mode voltage injection (*CMI*) into the output reference voltages to perform the desired equalization. This means that the switching signals of each phase can be produced through standard single-reference/multiple-carriers comparison approaches, like level-shifted (LS) approaches. In this case the output leg voltages only switch between two consecutive levels in each modulation interval, thus working in a single-step (*SS*) switching mode. This leads to minimization of both the switching losses and of the output voltage harmonic distortion. Nevertheless, in some operating conditions, like for high modulation indices, the feasible interval for the common mode voltage injection is narrow and cannot guarantee the desired behaviour. Then, for the voltage fluctuation suppression it is usually demanded to utilize bigger size dc-link capacitors.

Other strategies, instead, take advantage of the possibility to switch between all three levels in a single modulation interval [12-16], thus exhibiting a multi-step (*MS*) switching mode. Through these approaches it is possible to actively control the average time for which the output node of each phase is connected to the neutral point (NP) of the converter, independently of the converter's operating condition. In the extreme case the phase output voltage can be constrained to switch only between the positive and the negative dc-link rail, behaving like a two-level converter (*TL* switching mode). The main drawbacks of these strategies are the higher switching losses and a poorer output voltage harmonic content. Additionally, multiple-references/single-carrier comparison techniques are needed to allow the decoupled control of the switching devices of each leg. To partially mitigate the increase of the number of switching transitions, some papers focus on finding the minimum number of phases needed to switch in the *MS* mode in order to guarantee the capacitors' voltage equalization [14].

The present paper aims to combine these two approaches in order to exploit all their benefits and, at the same time, to neutralize their drawbacks. When the sole *CMI* is able to guarantee the equalization needed, the usage of *MS* mode is avoided to keep the switching losses low; vice versa, when the *MS* mode is needed, a proper *CMI* is simultaneously exploited to keep the number of switching transitions at a minimum feasible value. Indeed, it is shown that, in each operating condition, it is sufficient to apply the *MS* mode to just one of the phases if, contemporarily, one of the other two is clamped to the positive/negative dc-link rail.

The paper is organized as follows. In Section II the mathematical model of the system is obtained. In Section III the model is first modified to highlight all the available degrees of freedom and then it is used to explain the proposed modulation strategy. Section IV presents the numerical validation of the presented method and comparisons with the other techniques. Section V synthetize the conclusions.

II. Mathematical Model

The examined topology is shown in Fig. 1. Each NPC leg has four controllable switching devices, which can be divided in two complementary pairs (respectively denoted with the subscripts *B* and *T*) and their switching states are represented by the signals $s_{(B/T),k} \in \{0,1\}$ (where $k = \{a,b,c\}$ denotes the inverter's leg). As a result, each leg has four possible switching combinations, summarized in Table I.

The leg configuration {1,0} is not used for control purposes since the corresponding output voltage depends on the output current through the function $f_v(i) = v_{DC}(\text{sign}(i) - 1)/2$. The switching functions are then constrained by the relation $s_{T,k} \leq s_{B,k}$. In other words, the top switch is not closed if the bottom one is open.

TABLE I NPC k-TH PHASE SWITCHING STATES

State	$s_{T,k}$	$s_{B,k}$	v_k	$i_{NP,k}$
{0,0}	0	0	0	0
{0,1}	0	1	$v_{DC,B}$	i_k
{1,0}	1	0	$f_v(i_k)$	0
{1,1}	1	1	v_{DC}	0

The converter's output leg voltages and the NP current can be expressed as a linear combination of the corresponding switching signals:

$$\begin{cases} v_k = s_{B,k} v_{DC,B} + s_{T,k} v_{DC,T} \\ i_{NP,k} = (s_{B,k} - s_{T,k}) \cdot i_k = \Delta s_k \, i_k \end{cases} \quad , \quad \text{with } k = \{a,b,c\} \tag{1}$$

The dc-bus voltage unbalance dynamic can be easily linked to the total current flowing in the NP rail as:

$$C \frac{\mathrm{d}}{\mathrm{d}t}\left[v_{DC,T} - v_{DC,B} \right] = i_{NP} = \sum_{k=a,b,c} \Delta s_k \, i_k \tag{2}$$

Since the converter is of three-wire configuration (i.e. with isolated load's neutral point), it can be assumed that the load currents depend only on the phase-to-phase output voltages. Therefore, it results $\partial i_k / \partial v_0 = 0$, where:

$$v_0 = (v_a + v_b + v_c)/3 \tag{3}$$

is the converter's common mode output voltage.

Through a standard averaging approach, applied to a moving window spanned over a T time interval, each variable $x(t)$ in (1)-(2) can be decomposed in a slow-varying component:

$$\bar{x}(t) = \frac{1}{T} \int_{t-T}^{t} x(\tau) \mathrm{d}\tau \tag{4}$$

and a fast-varying component $\delta x(t) = x(t) - \bar{x}(t)$.

Consider a multi-references/single-carrier PWM technique, where each switching signal $s_{(B/T),k}$ is obtained through the comparison between the corresponding duty-cycle $d_{(B/T),k} \in [0,1]$ and a common triangular carrier $\sigma_c(t)$. By choosing T in (4) to be equal to the carrier period T_c and by neglecting the fast-varying contributions, the system of equations (1) and (2) can be rewritten as:

$$\begin{cases} \bar{v}_k = d_{B,k} \bar{v}_{DC,B} + d_{T,k} \bar{v}_{DC,T} \\ C \frac{\mathrm{d}}{\mathrm{d}t}\left[\bar{v}_{DC,T} - \bar{v}_{DC,B} \right] = \bar{i}_{NP} = \sum_{k=a,b,c} \left(d_{B,k} - d_{T,k} \right) \bar{i}_k = \sum_{k=a,b,c} \Delta d_k \, \bar{i}_k \end{cases} \quad , \quad \text{with } k = \{a,b,c\} \tag{5}$$

with the duty-cycles constraint:

$$0 \le d_{T,k} \le d_{B,k} \le 1 \quad , \quad \text{with } k = \{a,b,c\} \tag{6}$$

III. MODULATION STRATEGY

The proposed modulation strategy is aimed to supply the desired set of phase-to-phase output voltages while actively controlling the dc-bus voltage unbalance. Additionally, the strategy should minimize the number of switching transitions, which cause additional losses and worsen the output voltage harmonic content.

A. Degrees of Freedom Available for the Voltage Balancing

The formulation of the proposed strategy requires all the available degrees of freedom to be exposed first.

In general, the output currents are driven only by the leg-to-leg voltages. By introducing the differential voltages $\tilde{v}_k$ with the condition:

$$\tilde{v}_a + \tilde{v}_b + \tilde{v}_c = 0 \tag{7}$$

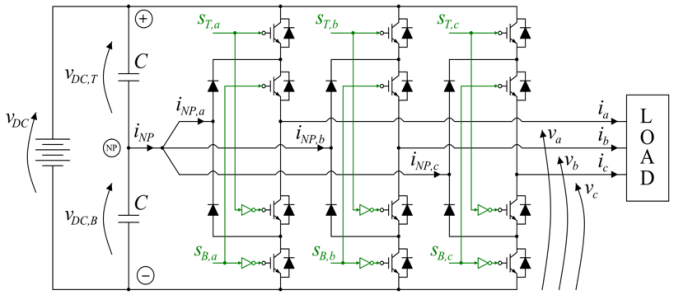

Fig. 1. Power circuit of a three-phase NPC converter.

the converter leg voltages can be expressed as:

$$v_k = \tilde{v}_k + v_0 \quad , \quad \text{with } k = \{a,b,c\} \tag{8}$$

thus highlighting the role of the common mode voltage v_0, which is a first available degree of freedom. Note that, for a linear and symmetrical configuration, each differential voltage $\tilde{v}_k$ represents the load phase voltage.

The controller needs to supply a desired set of differential voltages $\tilde{v}_k^*$ in each modulation interval. Then, the extremes of the available range for the reference common mode voltage v_0^* are easily found to be:

$$\begin{cases} v_{0,\min}^* = -\tilde{v}_{k,\min}^* = -\min\limits_{k=a,b,c} \left\{ \tilde{v}_k^* \right\} \\ v_{0,\max}^* = \bar{v}_{DC} - \tilde{v}_{k,\max}^* = \bar{v}_{DC} - \max\limits_{k=a,b,c} \left\{ \tilde{v}_k^* \right\} \end{cases} \tag{9}$$

As per (5), the differential duty-cycle Δd_k, does not affect the leg voltage $\bar{v}_k = v_k^*$ and, therefore, is an additional degree of freedom of the system. Note that Δd_k actually represents the normalized average time for which the output node of the k-th leg is connected to the NP rail during each modulation interval. The same average reference leg voltage can be obtained in different ways by just changing Δd_k in the feasibility interval $[0 \; ; \Delta d_{k,\max}]$, thus leading to the *SS* mode when it is at maximum, to the *TL* mode when it is zero and to the *MS* mode in all the other cases. This property is exemplified in Fig. 2.

The maximum feasible value $\Delta d_{k,\max}$ is given either by the condition $d_{B,k} = 1$ or by $d_{T,k} = 0$ and, from (5), it can be expressed as a function Δd_{max} of the leg reference voltage v_k^*:

$$\Delta d_{k,\max} = \Delta d_{\max}\left(v_k^* \right) = \min \left\{ \frac{v_k^*}{\bar{v}_{DC,B}} \; , \; \frac{\bar{v}_{DC} - v_k^*}{\bar{v}_{DC} - \bar{v}_{DC,B}} \right\} \tag{10}$$

Consequently, the function $\Delta d_{\max}$ is piece-wise linear and such that $\Delta d_{\max}(0) = \Delta d_{\max}(\bar{v}_{DC}) = 0$ (i.e. when the phase output is clamped either to the negative or the positive dc rail) and $\Delta d_{\max}(\bar{v}_{DC,B}) = 1$ (i.e. when the phase output is clamped to the NP rail). This function has the same shape for all the phases and its qualitative behaviour is shown in Fig. 3.

Value of Δd_k can be conveniently referred to $\Delta d_{k,\max}$ through the introduction of the normalized coefficient:

$$\alpha_k = \Delta d_k \big/ \Delta d_{k,\max} \in [0;1] \quad , \quad \text{with } k = \{a,b,c\} \tag{11}$$

When $\alpha_k = 1$, the leg output is connected to the NP rail for the maximum feasible time and works in the standard SS mode. When $\alpha_k = 0$, the leg output is never connected to the NP rail and works in *TL* mode (i.e. as a two-level converter). Finally, when $0 < \alpha_k < 1$, the leg output voltage switches between three levels in a single modulation interval and, therefore, works in *MS* mode (see Fig. 2).

By combining (10) and (11) into the 2nd equation of (5), the voltage unbalance dynamic equation can be rewritten as:

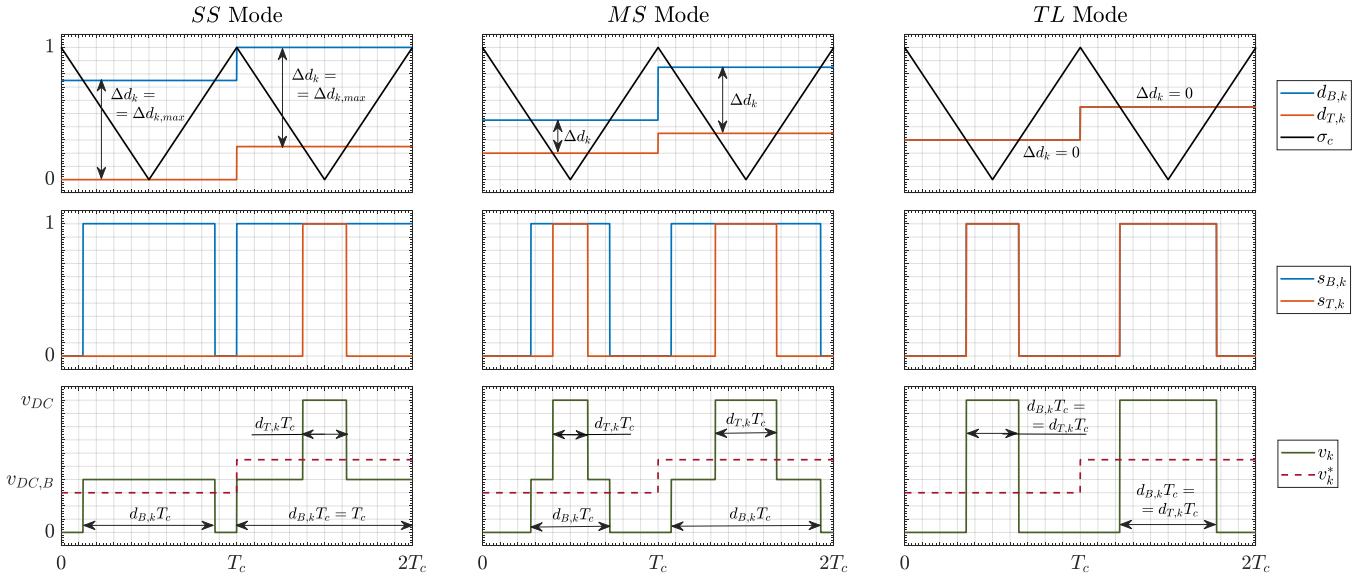

Fig. 2. Qualitative time behavior of the different switching modes for the same output voltage references.

$$C\frac{\mathrm{d}}{\mathrm{d}t}\left[\bar{v}_{DC,T}-\bar{v}_{DC,B}\right]=\bar{i}_{NP}=\sum_{k=a,b,c}\alpha_k\cdot\Delta d_{k,\max}\left(\tilde{v}_k^*+v_{\emptyset}^*\right)\cdot\bar{i}_k \qquad (12)$$

This relation formalizes the dependence of the voltage unbalance from all the available degrees of freedom offered by the structure ($v_{\emptyset}^*$ and all the α_k).

B. *Proposed Modulation Technique*

Most of the NPC-oriented PWM techniques with voltage balancing capabilities available in the literature ultimately aim to properly control the NP current. Commonly, those methods are constraining the set of control variables which drive the voltage unbalance of (12). Indeed, the *CMI* based techniques only exploit $v_{\emptyset}^*$ while keeping all the $\alpha_k = 1$ (*SS* mode), while the *MS* based approaches only act on the α_k while choosing $v_{\emptyset}^*$ with different strategies. The proposed technique aims to exploit both the degrees of freedom to actively control the voltage unbalance while minimizing the switching transitions.

As per (12), when the converter operates in *SS* mode, $\bar{i}_{NP}$ is reduced to a piece-wise linear function of $v_{\emptyset}^*$, resulting from the superposition of the three piece-wise linear functions obtained by scaling and shifting $\Delta d_{\max}(v^*)$ by $\bar{i}_k$ and $\tilde{v}_k^*$, respectively, [10]. Naturally, the internal breaking points $v_{\emptyset,h}^*$ of $\bar{i}_{NP}(v_{\emptyset}^*)$ either satisfy the relation $\Delta d_{\max}(v_{\emptyset,h}^*)=1$ or $\Delta d_{\max}(v_{\emptyset,h}^*)=0$ and are effectively feasible common mode voltages only if they belong to the range $[v_{\emptyset,\min}^*; v_{\emptyset,\max}^*]$. Consequently, a NPC converter working in *SS* mode has at most 5 breaking points (3 internal plus the feasibility interval extremes). The four possible conditions are qualitatively shown in Fig. 4 and correspond to the ones described in [10].

The proposed modulation aims to set $\bar{i}_{NP}$ to a certain current reference i_{NP}^*, which could be, for example, the output of a feedback controller acting on the voltage unbalance.

Referring to the case $i_{NP}^* > 0$ [$i_{NP}^* < 0$] and taking into account (12), the following regions can be identified:

- the region $0 < \bar{i}_{NP} < i_{NP}^*$ [$i_{NP}^* < \bar{i}_{NP} < 0$] makes the voltage unbalance moving towards the reference with a reduced slope and thus represents a *Natural Balancing* region;
- the region $\bar{i}_{NP} > i_{NP}^*$ [$\bar{i}_{NP} < i_{NP}^*$] makes the voltage unbalance move towards the reference faster than needed and thus represents an *Excessive Slope* region;
- the region $\bar{i}_{NP} < 0$ [$\bar{i}_{NP} > 0$] makes the voltage unbalance move away from the reference and represents a *Wrong Direction* region.

The modulation process is executed according to the shape of the piece-wise linear function $\bar{i}_{NP}(v_{\emptyset}^*)$ in relation with i_{NP}^*.

Firstly, the procedure searches for a common mode voltage reference which satisfies the relation $\bar{i}_{NP}(v_{\emptyset}^*)=i_{NP}^*$. This condition is verified only if there are two consecutive breaking points $v_{\emptyset,h}^*$ and $v_{\emptyset,h+1}^*$ satisfying the crossing condition $\left(\bar{i}_{NP}(v_{\emptyset,h}^*)-i_{NP}^*\right)\cdot\left(\bar{i}_{NP}(v_{\emptyset,h+1}^*)-i_{NP}^*\right)<0$. The optimal voltage is then obtained through a simple linear interpolation:

$$v_{\emptyset,\mathrm{opt}}^*=v_{\emptyset,h}^*+\left(v_{\emptyset,h+1}^*-v_{\emptyset,h}^*\right)\cdot\left[\frac{i_{NP}^*-\bar{i}_{NP}(v_{\emptyset,h}^*)}{\bar{i}_{NP}(v_{\emptyset,h+1}^*)-\bar{i}_{NP}(v_{\emptyset,h}^*)}\right] \qquad (13)$$

The situation is qualitatively depicted in Fig. 5a. Since $\bar{i}_{NP}(v_{\emptyset}^*)$ might be non-monotonic, more than one optimal voltage may exist. In this case, the effective common mode voltage to be applied can be chosen arbitrarily since the different solutions are equivalent for balancing purposes.

When the crossing condition is not verified, there might be an interval of $v_{\emptyset}^*$ where the $\bar{i}_{NP}(v_{\emptyset}^*)$ function is located inside the

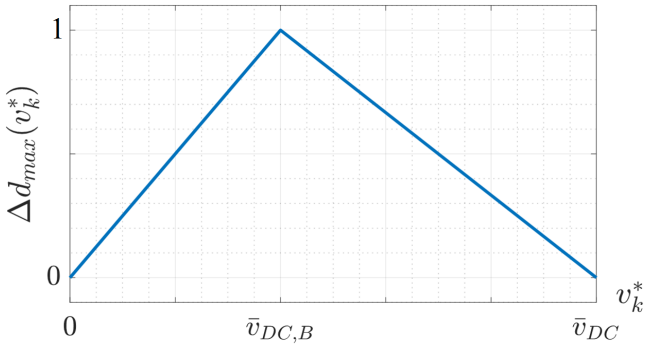

Fig. 3. Maximum differential duty-cycle function.

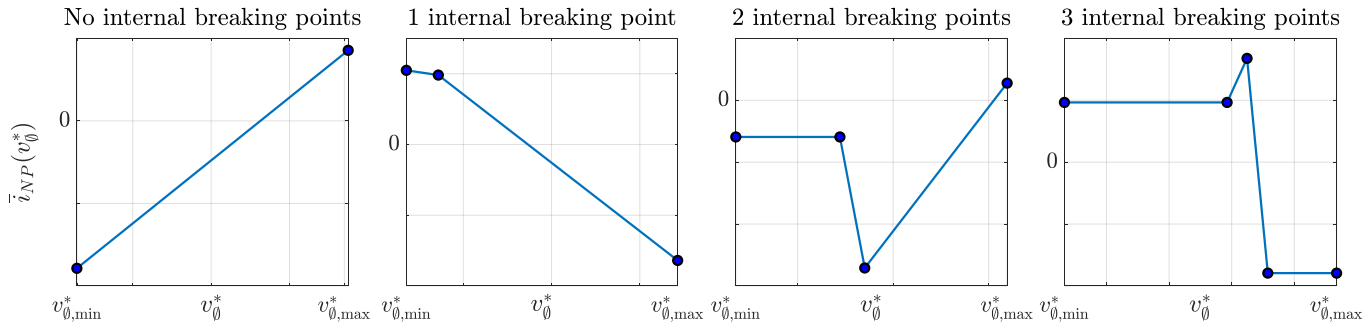

Fig. 4. Shape of the NP current function in *SS* mode.

Natural Balancing area, as in Fig. 5b. The choice of any $v^*_{\mathbf{0}}$ in that region would make the voltage unbalance evolve correctly, guaranteeing the equalization without any need for a *MS* mode. Then, the optimal injection $v^*_{\mathbf{0},\text{opt}}$ corresponds to the closest point to i^*_{NP} and, given the piece-wise linear nature of $\bar{i}_{NP}(v^*_{\mathbf{0}})$, it is always one of the breaking points. As a result, this strategy clamps one of the phases to one of the three dc-bus rails, thus lowering the switching losses as a positive side effect.

Last, if the $\bar{i}_{NP}(v^*_{\mathbf{0}})$ function resides entirely in the *Excessive Slope* or in the *Wrong Direction* region (see Fig. 5c), the NP current control can be achieved only by activating the *MS* mode. However, a proper *CMI* always allows to clamp one of the converter legs to the negative or positive rail and, by selecting it in a way that the other legs have opposite current signs, the *MS* mode makes it possible to choose any desired sign of the neutral rail current and thus move the operating condition in the *Natural Balancing* region.

Indeed, by sorting the phase voltages and denoting as {I,II,III} the index set for which $\tilde{v}^*_I \geq \tilde{v}^*_{II} \geq \tilde{v}^*_{III}$, given the three wires constraint $i_a + i_b + i_c = 0$, six combinations of sign(i_k) can be examined (the zero current case is neglected). For each allowed combination (see Table II) it is possible to properly clamp either the phase leg voltage v_{I} or v_{III} while preserving the aforementioned current sign opposition in the non-clamped phase currents. This corresponds to the selection of an optimal *CMI* either as $v^*_{\mathbf{0},\text{opt}} = v^*_{\mathbf{0},\max}$ or $v^*_{\mathbf{0},\text{opt}} = v^*_{\mathbf{0},\min}$. It should be noted that in two instances ({2} and {5}) the clamping choice can be made with both selections. In this case, the phase to be clamped can be chosen as the one with the highest current in order to minimize the switching losses.

Once $v^*_{\mathbf{0},\text{opt}}$ has been determined, the *MS* switching phase *m* has to be controlled by reducing the corresponding α_m in order to move the current $\bar{i}_{NP,SS}$ (obtained when the converter operates in *SS* mode with $v^*_{\mathbf{0}} = v^*_{\mathbf{0},\text{opt}}$) towards the reference.

Regardless of the region (i.e. either in the *Excessive Slope* or in the *Wrong Direction*) the *MS* phase is selected as the one whose current i_m has the same sign of $\bar{i}_{NP,SS}$ and the differential duty-cycle reduction is achieved by choosing:

$$\alpha_m = 1 - \left(\bar{i}_{NP,SS} - i^*_{NP}\right) \Big/ \left(\bar{i}_m \, \Delta d_{\max} \left(\tilde{v}^*_m + v^*_{\emptyset,\text{opt}}\right)\right) \tag{14}$$

If this value is outside the feasibility region, α_m is saturated to zero, forcing the *m* phase to operate in *TL* mode and allowing the converter to work in the *Natural Balancing* area.

The clamped phase does not have any switching transition in the corresponding modulation interval and therefore compensates for the additional losses due to the *MS* mode.

TABLE II VOLTAGE CLAMPING CASES IN *MS* MODE

State	i_{I}	i_{II}	i_{III}	Voltage Clamping
{1}	+	+	-	$v_{\text{I}} = v_{\text{DC}}$
{2}	+	-	+	$v_{\text{I}} = v_{\text{DC}}$ or $v_{\text{III}} = 0$
{3}	+	-	-	$v_{\text{III}} = 0$
{4}	-	+	+	$v_{\text{III}} = 0$
{5}	-	+	-	$v_{\text{I}} = v_{\text{DC}}$ or $v_{\text{III}} = 0$
{6}	-	-	+	$v_{\text{I}} = v_{\text{DC}}$

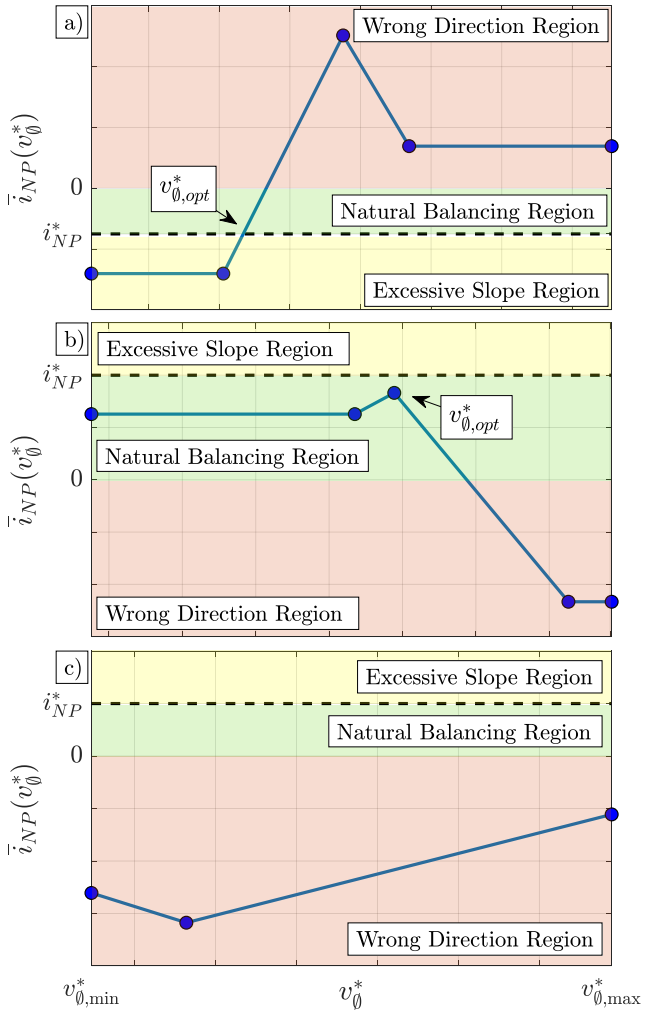

Fig. 5. NP current function assuming different conditions.

Once both the $v^*_{0,\mathrm{opt}}$ and the α_k have been chosen, the top and bottom duty-cycles can be easily found as:

$$\begin{cases} d_{T,k}=\dfrac{\tilde{v}_k+v^*_{0,\mathrm{opt}}}{\overline{v}_{DC}}-\dfrac{\overline{v}_{DC,B}}{\overline{v}_{DC}}\alpha_k\Delta d_{\max}(\tilde{v}_k+v^*_{0,\mathrm{opt}}) \\ d_{B,k}=\dfrac{\tilde{v}_k+v^*_{0,\mathrm{opt}}}{\overline{v}_{DC}}+\dfrac{\overline{v}_{DC,T}}{\overline{v}_{DC}}\alpha_k\Delta d_{\max}(\tilde{v}_k+v^*_{0,\mathrm{opt}}) \end{cases}, \text{ with } k=\{a,b,c\} \quad (15)$$

The flowchart of the proposed modulation technique is depicted in Fig. 6. The procedure is straightforward and does not need any iterative loop. The equalization is always guaranteed, despite the operating conditions of the converter, and the switching losses are kept at their minimum value compatible with the NP current control requirement.

IV. Numerical Validation

The proposed modulation technique has been intensively tested through numerical simulations in the Matlab/Simulink environment. In order to highlight its effectiveness, it has been compared with the modulation algorithms proposed in [10] and in [12], which can be considered as the state-of-the-art techniques based on the sole *CMI* or on the sole *MS* mode, respectively. Additionally, as a baseline, the proposed approach is also compared with a standard carrier-based PWM (CBPWM) technique without any NP voltage control. The converter supplies a simple balanced *R-L* load in open-loop. As shown in [2-3], a balanced passive load guarantees a stable behaviour even with standard CBPWM techniques. The simulation parameters are reported in Table III.

The testing scenarios involve both a transient operation and a steady state behaviour. All techniques [10], [12] and the presented one, are capable of setting the value of the dc-link capacitors voltages (i.e. of setting their unbalance), to the desired one. In both testing scenarios the reference voltage unbalance has been set to zero, in order to keep the dc-bus voltages perfectly balanced. However, a non-zero reference for unbalance of the capacitors would not impact the effectiveness of the proposed strategy.

The NP current reference is given by a feedback predictive controller acting on the measured value of the voltage unbalance. Through a simple integration of (2), over a modulation interval, the reference current is found as:

$$i^*_{NP}=\left(C/T_c\right)\cdot\left[(\overline{v}_{DC,T}-\overline{v}_{DC,B})^*-(\overline{v}_{DC,T}-\overline{v}_{DC,B})\right] \quad (16)$$

A. Transient Test for Voltage Equalization

This scenario is aimed to compare the transient behaviour of the proposed technique with the other existing ones.

The dc-bus capacitors, starting from a complete unbalanced state ($v_{DC,B}=250$ V ; $v_{DC,T}=0$ V), are driven to the desired

TABLE III Simulation Parameters

Variable	Symbol	Value
Rated Power	S_R	10 kVA
Rated DC Voltage	$v_{DC,R}$	250 V
Rated Output Current	$i_{out,R}$	32.7 A (rms)
DC Capacitance	C	300 µF
Sampling Frequency	f_s	2 kHz
Carrier Frequency	f_c	2 kHz
Load Resistance	R	4 Ω
Load Inductance	L	5 mH

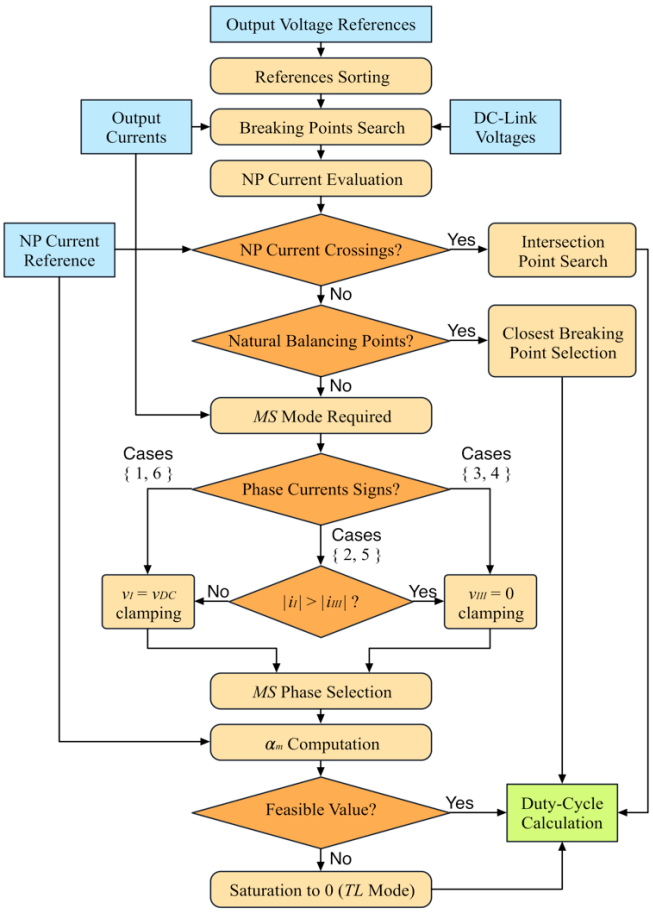

Fig. 6. Proposed modulation technique logical flow chart.

equalization state by operating the converter with a set of three symmetrical sinusoidal voltages at 50 Hz and modulation index of 0.8. The results are depicted in Fig.7. The leg voltages are normalized by the rated DC voltage (250 V), while the output currents are normalized by the peak rated current (46.2 A). Some global simulation parameters are given in Table IV. The equalization time has been measured from the control activation up to the first intersection between $v_{DC,B}$ and $v_{DC,T}$. The number of switching transitions has been evaluated considering all the converter devices for the whole 40 ms time window of interest.

As can be easily seen, apart from the initial time interval, the results obtained with the proposed method are almost equivalent to the ones obtained with the sole *CMI*. This is expected since for the used modulation index of 0.8 there is a good range for the common mode voltage injection (good feasibility interval of v^*_0), which is, as explained, a degee of freedom used to balance the dc-link voltages. The injection can be clearly identified in the reference leg voltages v^*_a, v^*_b, v^*_c in Fig.7. Moreover, as can be seen from Table IV, both the techniques show the same number of switching transitions. When the proposed method works in *MS* mode, the simultaneous voltage clamping is able to neutralize the additional transitions through a proper common mode injection.

The approach based on the sole *MS* mode, in this case, is both slower and has higher number of switching transitions (and, hence, higher losses) with respect to the other methods.

The standard CBPWM shows the worst NP voltage behaviour since not only it has the slowest convergence rate, but

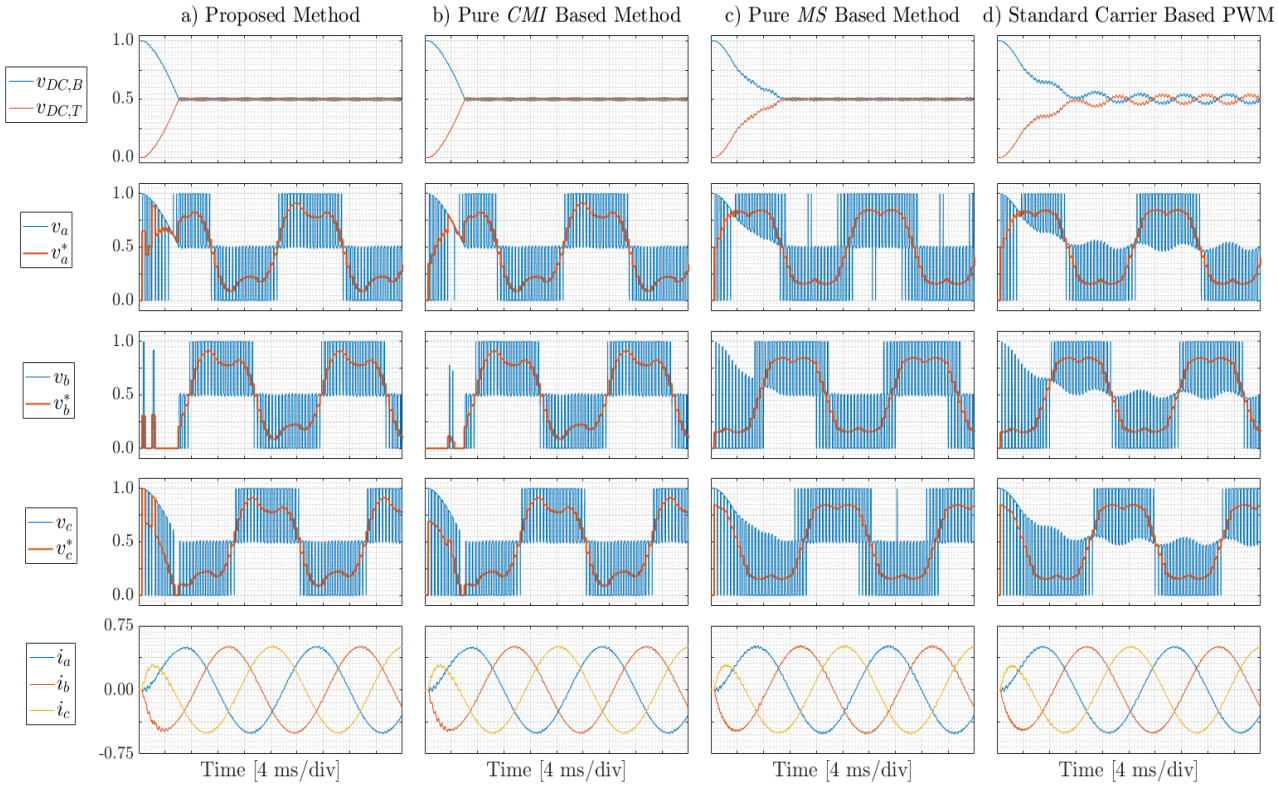

Fig. 7. Simulation results in the equalization sequence scenario (modulation index $M = 0.8$).

TABLE IV GLOBAL SIMULATION RESULTS IN THE EQUALIZATION TEST (MODULATION INDEX 0.8)

Modulation Technique	a) Proposed Method	b) Pure *CMI* Based Method	c) Pure *MS* Based Method	d) Standard Carrier Based PWM
Equalization Time	6.07 ms	6.07 ms	10.61 ms	11.63 ms
N° of Switching Transitions	900	900	1176	960

is even unable to suppress the steady state voltage fluctuation, whose effects are evident in the output voltages.

B. Steady State Test with High Modulation Index

In this test the behaviour of the proposed method during the steady state is examined. The converter references are set to three symmetrical sinusoidal voltages at 50 Hz with a modulation index of 1.1 (slightly below the overmodulation limit). As it is known, this is a critical working condition both for the *CMI* and for the *MS* based methods. The results are graphically depicted in Fig. 8 and summarized in Table V.

As can be seen from Fig. 8b, the pure *CMI* based approach is unable to suppress the NP voltage fluctuations (due to the reduced feasibility interval of v_0^*) and behaves similarly to the standard CBPWM (Fig. 8d). In both cases peak-to-peak steady state NP voltage oscillation is over 10 % of the rated voltage.

The *MS* based approach is unaffected by this issue and keeps the capacitors voltages at the reference value with a 2.10% peak-to-peak oscillation, mainly caused by the secondary switching effects (i.e. the fast-varying dynamics which have been neglected in the average model (5)). However, the presence of multiple transitions among the three available levels is almost always present in one of the converter legs (Fig. 8c middle three plots), resulting in a 30% higher switching transition rate with respect to the standard CBPWM.

Contrarily, the proposed technique, while showing an *MS* like behaviour, with respect to the voltage fluctuations shows significantly lower number of switching transitions (Fig. 8a) which, indeed, is equal to the CBPWM approach. This is thanks to the voltage clamping performed by the *CMI*. As a consequence, the proposed technique is able to guarantee lower losses and a lower harmonic content, which, therefore, leads to output currents with a slightly reduced ripple. Again, the 2.22% voltage ripple is due to the secondary effects. It can also be noted that the injected common mode voltage is similar to the one provided by the strategy proposed in [10].

V. CONCLUSIONS

A novel PWM technique for three-phase NPC converters, able to guarantee the dc-bus capacitors voltage balancing, is presented in the paper. Contrarily to standard approaches, which are either based on the sole injection of a common mode voltage, *CMI*, or on the sole exploitation of the multi-step, *MS*, capabilities of the NPC, the proposed technique is taking advantages of both approaches, while keeping the switching transitions to the minimum required number, in order to guarantee a good efficiency and a reduced output voltage harmonic content.

The approach has been numerically tested and compared with some of the other pre-existing techniques available in the technical literature. The proposed method is showing overall better performance, especially at high modulation index values, in terms of both the NP voltage fluctuation suppression and of the number of switching transitions.

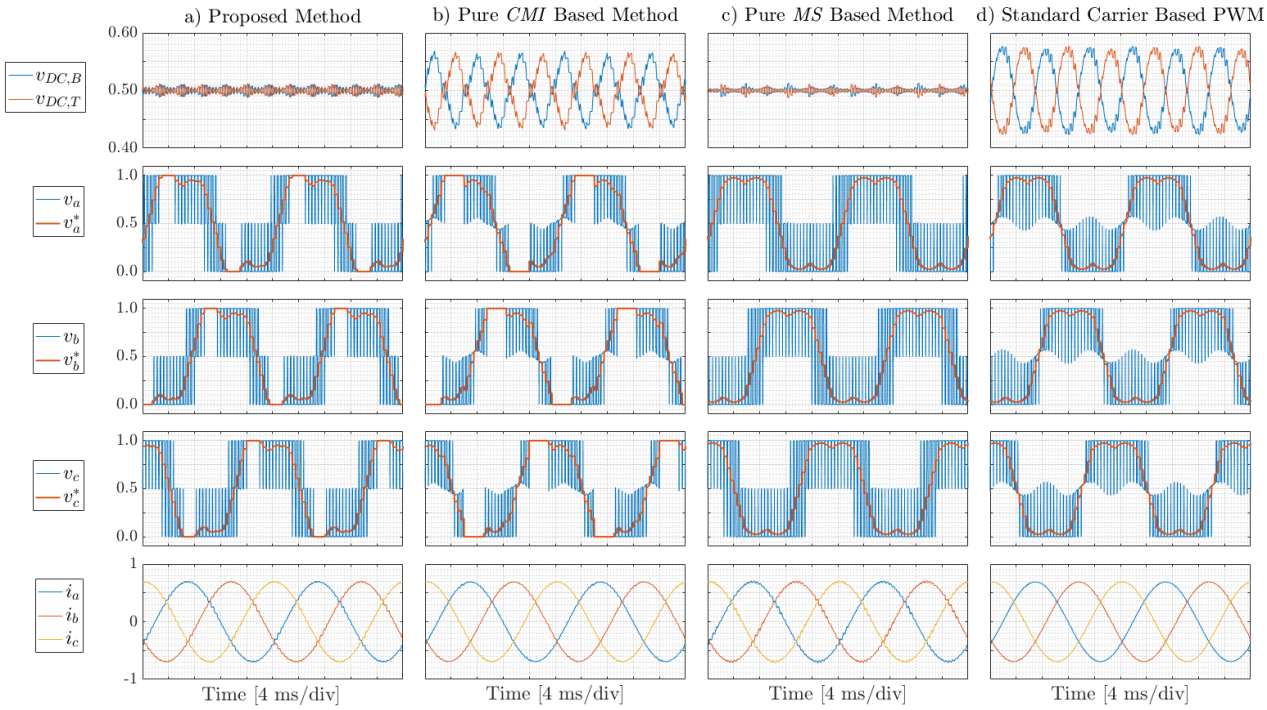

Fig. 8. Simulation results in the steady state with high modulation index scenario (modulation index M = 1.1).

TABLE V GLOBAL SIMULATION RESULTS IN THE STEADY STATE TEST (MODULATION INDEX 1.1)

Modulation Technique	a) Proposed Method	b) Pure *CMI* Based Method	c) Pure *MS* Based Method	d) Standard Carrier Based PWM
N° of Switching Transitions	960	704	1248	960
NP Voltage Ripple	2.22 %	13.15 %	2.10 %	14.86 %
Output Current THD	2.18 %	1.40 %	2.55 %	1.07 %

REFERENCES

[1] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, Aug. 2002.

[2] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Pow. Electron.*, vol. 15, no. 2, Mar. 2000.

[3] J. Pou, D. Boroyevich and R. Pindado, "Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter," *IEEE Trans. Pow. Electron.*, vol. 20, no. 1, Jan. 2005.

[4] Z. Shu, X. He, Z. Wang, D. Qiu and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuits," *IEEE Trans. Pow. Electron.*, vol. 28, no. 5, May 2013.

[5] P. Kant and B. Singh, "Multi-pulse AC–DC converter fed SVM controlled NPC inverter based VCIMD," *IET Pow. Electron.*, vol. 11, no. 14, Nov. 2018.

[6] H. Zhang, S. Jon Finney, A. Massoud and B. Wayne Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, Nov. 2008.

[7] Y. Jiao, F. C. Lee and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Pow. Electron.*, vol. 29, no. 10, Oct. 2014.

[8] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Pow. Electron.*, vol. 27, no. 2, Feb. 2012.

[9] I. López, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, E. Ibarra and G. Konstantinou, "Generalized PWM-based method for multiphase neutral-point-clamped converters with capacitor voltage balance capability," *IEEE Trans. Power Electron.*, vol. 32, no. 6, Jun. 2017

[10] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, Jul. 2010.

[11] M. Mehrasa, M. Ahmadigorji and N. Amjady, "A new dual Lagrangian model and input/output feedback linearization control of 3-phase/level NPC voltage-source rectifier," *Automatika*, vol. 55, 2014.

[12] I. López, S Ceballos, J. Pou, J. Zaragoza, J. Andreu, I. Kortabarria and V. G. Agelidis, "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Trans. Pow. Electron.*, vol. 31, no. 2, Feb. 2016

[13] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, Feb. 2009.

[14] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, Feb. 2009.

[15] C. Wang, Z. Li, X. Si and H. Xin, "Control of neutral-point voltage in three-phase four-wire three-level NPC inverter based on the disassembly of zero level," *CPSS Trans. Pow. Electron. and Appl.*, vol. 3, no. 3, Sept. 2018.

[16] F. Luo, K. Loo and Y. Lai, "Simple carrier-based pulse-width modulation scheme for three-phase four-wire neutral-point-clamped inverters with neutral-point balancing," *IET Pow. Electron.*, vol. 9, no. 2, Feb. 2016.