Short-range Quality-factor Modulation (SQuirM) for Low Power High Speed Inductive Data Transfer

Matthew Schormans, *Member, IEEE,* Dai Jiang, *Member, IEEE,* Virgilio Valente, *Member, IEEE,* and Andreas Demosthenous, *Fellow, IEEE*

***Abstract*—Wireless data telemetry for Implantable Medical Devices (IMDs) has, in general, been limited to a few Mbps, and used for applications such as transmitting recordings from an implanted monitoring device, or uploading commands to an implanted stimulator. However, modern neural interfaces need to record high resolution potentials from hundreds of neurons; this requires much higher data rates. While fast wireless communication is possible using existing standards such as WiFi, power consumption demands are far too high for IMDs. Short range inductive link based telemetry, in particular impulse-based systems such as pulse-harmonic modulation (PHM), have demonstrated transfer speeds of up to 20 Mbps with a small power budget. However, these systems require complex and precise circuits, making them potentially susceptible to inter-symbol-interference. This work presents a new method named Short-range Quality-factor Modulation (SQuirM), which retains the low power consumption and high data rate of PHM, while improving the resilience of the system and simplifying the circuit design. Transmitter and receiver circuits were fabricated using 0.35 µm CMOS. The circuits were capable of reliably transceiving data at speeds of up to 50.4 Mbps, with a BER of $< 4.5 \times 10^{-10}$, and a transmitter energy consumption of 8.11 pJ/b.**

***Index Terms*—biomedical telemetry, inductive link, low-power CMOS, near-field communication.**

I. Introduction

IMPLANTABLE medical devices (IMDs) have been the subject of much research and development, covering a wide range of potential applications, including neurostimulators [1], [2], pressure sensors [3], [4], and neural recording devices [5]–[7]. With this wide range of applications comes a wide range of potential telemetry requirements; each device will generally require some combination of wireless power and wireless data connection, with the specifics varying widely by application. In the case of neural recording interfaces, large amounts of data must be transferred quickly, especially as the number of recording channels increases. This is a challenging task for many existing data transfer approaches for IMDs, where data transfer rates are often limited to a few Mbps [8]–[10]. This is far too low for neural interfaces with many channels, for example the system in [5] requires 25 Mbps to transmit recordings from 13 ADCs across 52 analog channels. As systems scale to have even more channels, this number will only increase further. It is therefore imperative that existing data telemetry systems are improved to meet this demand.

TABLE I
Pros and cons for the schemes shown in Fig. 1

Method	Power Draw	Data Rate	Range	Needs Carrier?
Non-Inductive	V. High	High	High	Yes
Shared Power Link	Low	Low	Low	No
Dedicated Link: Carrier	High	High	Low	Yes
Dedicated Link: Impulse Based	**Low**	**High**	**Low**	**No**

Existing methods for high-speed data transfer can generally be classified as either non-inductive or inductive. Differences between approaches, and their respective advantages and disadvantages, are listed in Table I.

Non-inductive data-transfer methods use far-field omnidirectional transmission; e.g. Bluetooth, ZigBee, or WiFi (see Fig. 1(a)). These have the benefit of being widely used technologies, with commercial chips and designs available for easy implementation. They also have large working ranges, and capacity for high data rates, but at the cost of high power consumption. To transmit large quantities of high-rate data using a WiFi transmitter requires power in the range of 100s of milliwatts to a watt [11]. This is far too much continuous power consumption for an IMD. In addition, the high frequencies (usually 915 MHz or 2.4 GHz) used by far-field transmitters suffer significant loss due to absorption by body tissues [12].

Inductive data-transfer methods can be split into two categories; those that modulate an existing inductive power link (Fig. 1(b)), and those that make use of a dedicated inductive link for data transfer (Fig. 1(c)).

Shared power links are an attractive option for low-data rate applications, as they are fairly simple to implement, and make further use of the power link that is already in place. The example in Fig. 1(b) shows a typical arrangement using on-off keying (OOK) modulation for downlink data, and load-shift keying modulation (LSK) for uplink data. These systems can also operate with little power; they do not need to generate their own carrier. However, since they must modulate

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M. Schormans, D. Jiang, and A. Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. (e-mail: matthew.schormans.10@ucl.ac.uk,d.jiang@ucl.ac.uk,a.demosthenous@ucl.ac.uk)

V. Valente was with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK. He is now with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands. (e-mail: v.valente@tudelft.nl)

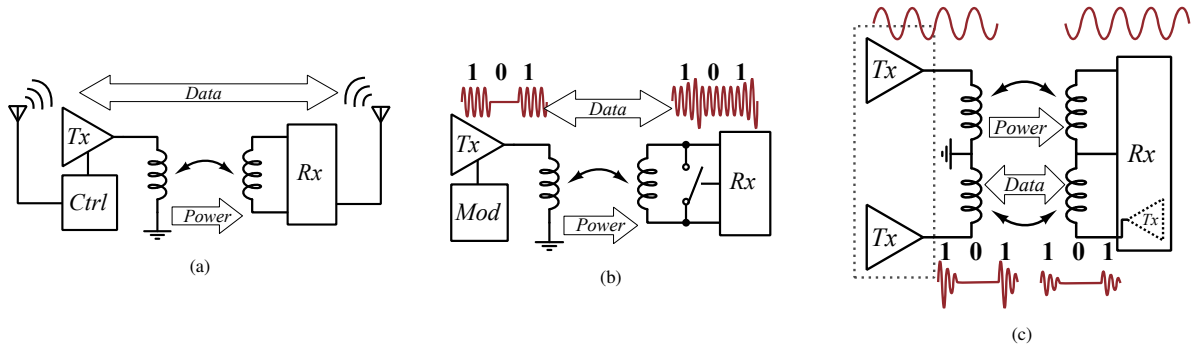


Fig. 1. Inductive WPT with (a): WiFi-style data link, (b): shared power link, and (c): dedicated data link.

the power carrier to transmit data, they are limited by the frequency of the power carrier with respect to data rate. For a typical power carrier frequency of 13.56 MHz, sending data at rates beyond 1-2 Mbps becomes difficult; each symbol needs several carrier cycles to be correctly demodulated [8], [13]. In addition, as the transmitted data rate increases, the power transfer efficiency of the link decreases. For example, an OOK modulated transmitter sending data at full capacity, such that it has a 50% duty cycle, will reduce the average transmitted power to 50%. These limitations render shared power links unattractive for continuous transmission of high speed data.

On the other hand, dedicated link systems are not limited in this way. Data can be transmitted over a separate link, without impacting power delivery. There are a number of ways to implement dedicated link solutions, but here they can be broadly classified as continuous-wave (CW), or impulse-radio (IR) styles. CW systems require generation of a continuous carrier in the transmitter side, which can then be modulated using AM, FM, PM, etc to transmit data, in the same way as any traditional radio system. Simard et al. [14] use 3 links in parallel: one for power, one for data uplink, and one for data downlink. While this system is shown to work with a data rate of 4.15 Mbps, it requires continuous carrier generation, and does not efficiently saturate the carrier with data. The system could theoretically boost its data rate by increasing the carrier frequency from 13.56 MHz, but this would inevitably require faster and more power hungry local oscillators.

IR based systems avoid the problem of power hungry carrier (re-)generation by dispensing with the carrier completely. They rely on the fact that by striking a high-Q resonant circuit with a current impulse, it will ring at its natural frequency for a period of time, and then fade away. These oscillatory bursts can be considered both a carrier frequency and as symbols. If the resonant circuit is a transmitting coil of an inductive link, this ringing can be easily detected in a closely coupled receiver coil (with the same resonant frequency). Fig. 1(c) illustrates an IR style system. Inanlou et al. [15] give an example of a short-range IR based system, using pulse-harmonic modulation (PHM) [16]. PHM has been shown to achieve data transmission rates of up to 20 Mbps [17], using small closely coupled coils, without requiring power hungry local oscillators for carrier (re-)generation. Since PHM has the benefits of low power consumption and high speed, it is well suited to IMD data subsystems. However, it suffers from some limitations,

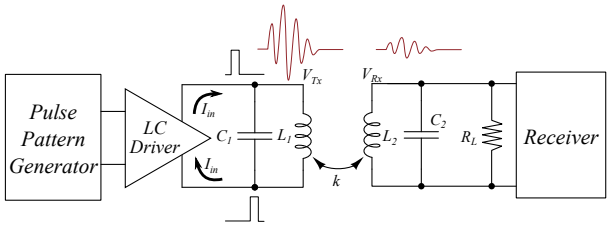


Fig. 2. PHM system block diagram.

particularly regarding inter-symbol interference (ISI). PHM requires the timing of the excitation and suppression pulses to be very precise; should the timing vary from the optimum by a small margin, significant ISI and bit corruption can result [18].

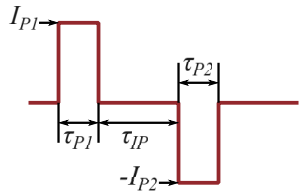
This paper presents a novel method named Short-range Quality-factor Modulation (SQuirM), developed by building on the principles of PHM. SQuirM eliminates the ISI issues that PHM suffers from, and greatly simplifies the circuit implementation. The work presented here is a development of the original simulations presented in [18], providing improved theoretical explanations, and measured results from the fabricated 0.35 µm chip. The rest of the paper is structured as follows: Section II describes the underlying theory of both PHM and SQuirM, highlighting differences in the methodologies. Section III describes the transmitter and receiver circuit designs in detail. Section IV reports measurements of the fabricated system, including power consumption, range, and BER measurements. Finally, Section V concludes the paper, and presents some potential improvements and future direction for SQuirM.

II. Theory

A. Fundamentals

This section considers the fundamental principles of both PHM and SQuirM, to show the differences in their theories of operation, and how SQuirM resolves some of the difficulties encountered by PHM.

1) PHM: A simplified block diagram of a PHM system is shown in Fig. 2, from Inanlou et al. [15]. The key elements are the pulse-pattern-generator and bidirectional LC-driver, that are used to inject precise current pulses into the transmission coil (L_1). The transmission coil is coupled to a receiver coil in a parallel-parallel (PP) inductive link arrangement, and both sides are tuned to the same resonant frequency.



Param	Value
τ_{P1}	5 ns
τ_{P2}	5 ns
I_{P1}	1 mA
I_{P2}	0.9 mA
τ_{IP}	21 ns

Param	Value
$L_{1,2}$	129 nH
$C_{1,2}$	15 pF
$R_{1,2}$	0.6 Ω
k	0.1
R_L	50 Ω

Fig. 3. Pulse-driving mechanism for PHM, with tables of values for an example system.

Fig. 3 shows the nature of the pulses transmitted by the LC driver, the first pulse is the *activation pulse*, and the second is the *suppression pulse*. The activation pulse starts an oscillation in the transmission coil, then by sending a perfectly timed suppression pulse in the opposite direction, a counter oscillation perfectly cancels the first oscillation. This generates a short oscillatory burst, which can be detected as a symbol by the receiver coil (see Fig. 4(a)).

For this to work however, the activation and suppression pulses must be perfectly formed and synchronized. Inanlou provides an exact expression for the impulse response of a PP inductive link, and an associated expression for finding the ideal value of τ_{IP}, which 'should be an integer multiple of $[1/f_0]$ plus a half cycle' [16]. Fig. 4(b) shows the effect of a 1 ns (4.8%) error in the inter-pulse delay (τ_{IP}) for the example system specified in Fig. 3. The short symbol becomes extended into a long ringing signal, which would result in extreme ISI if sending a data sequence with a period any shorter than 300 ns in this case (any faster than ≈3 Mbps). While this kind of pulse-desynchronization can occur as a result of process or temperature variation in the pulse generator, the optimum value of τ_{IP} is also strongly dependent on the exact link state i.e. the values of L, C, R, k and R_L. This means that the quality of the data link can suffer significantly due to changes in coupling (k) and load (R_L). This fundamentally reduces the resilience of PHM as a method for data transfer, particularly for the case of IMDs, as there is no guarantee that the link coupling will remain stable.

A final point to note, is that proper PHM operation requires some load resistance R_L, in this example 50 Ω. Without the effect of this load resistance, the secondary coil would contain a freewheeling current that would return to the coupled primary, undoing the effect of the suppression pulse. This load resistor has the unwanted side-effect of reducing the link gain, since it reduces the secondary side quality factor by an order of magnitude or more.

2) SQuirM: In contrast to PHM's twin-pulse cancellation strategy, the operating principle for SQuirM is based on the idea of successively *striking* and *damping* a PP inductive link.

Fig. 5(a) shows a simplified block diagram of a SQuirM system, the theory of operation is as follows. An incoming datastream is fed to both the impulse generator and the transmit-side damping switch, M_{Txd}. 'Data In' high represents a '1', and the pulse width of these incoming '1's determines how long the transmit side remains undamped. Sending longer data-in pulses gives more time for the Tx oscillation amplitude (and therefore the received oscillation amplitude) to build up, at the cost of reducing the data rate. '0's are represented by a lack of any oscillation; the bit rate must therefore be agreed *a priori* between the transmitter and receiver. Once the oscillation has been detected in the receiver, and V_{Rx} reaches sufficient amplitude, the receiver can detect its envelope and produce an output pulse. This pulse can then be *re-used* in order to damp the secondary coil once a bit has been received. Since the link is damped at both sides, the secondary coil can be terminated in a high impedance; the freewheeling current that would flow back to the primary instead terminates into the damping switch when it turns on. The benefit of this high impedance termination is a great increase in link gain compared with the PHM setup, where the secondary side Q must be reduced to achieve short symbols. By way of comparison, for the same link parameters and setup, the simulated peak to peak voltage at the receiver is 10× higher for SQuirM than for

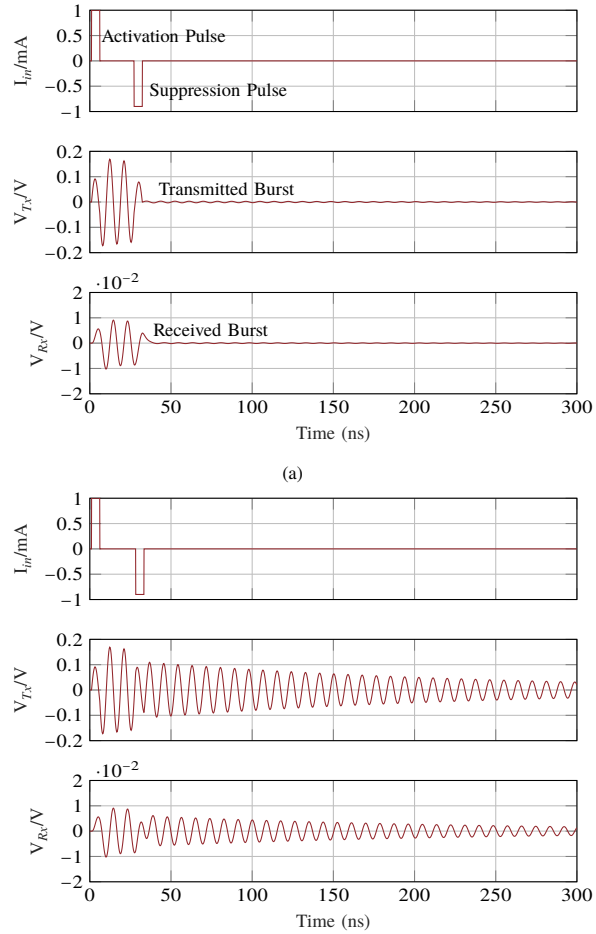


Fig. 4. (a): Ideal PHM waveforms; τ_{IP} =21 ns (b): Erroneous PHM waveforms; τ_{IP} =22 ns.

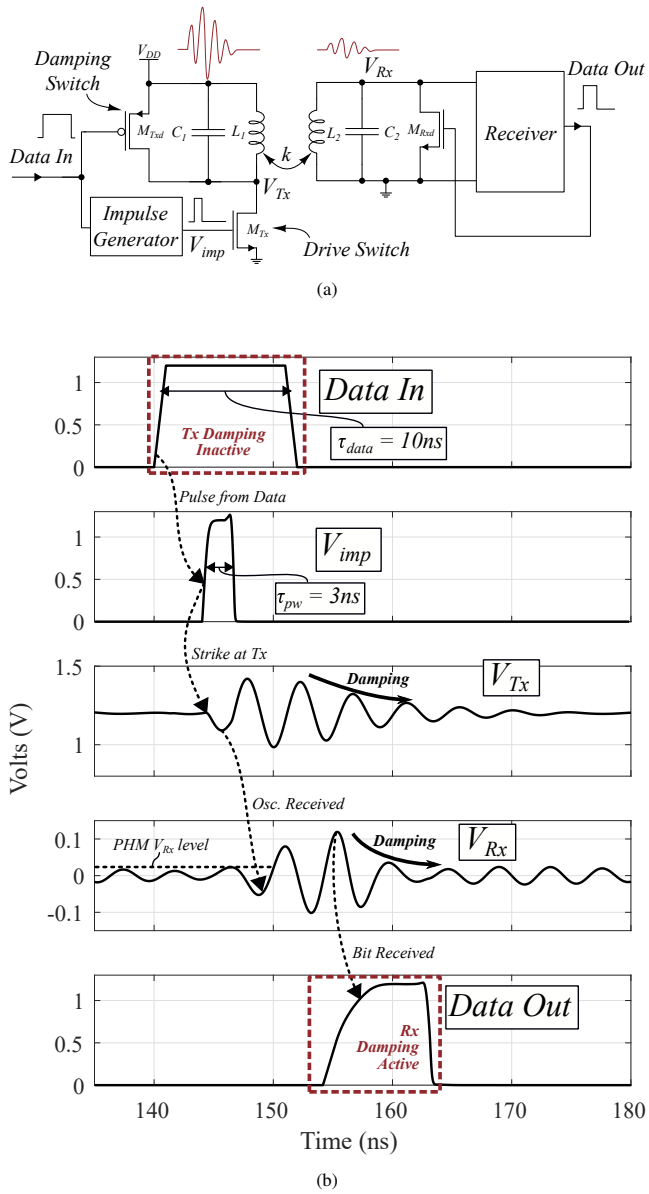


Fig. 5. (a): Block and (b): timing diagrams for SQuirM.

PHM. It should be noted that the received voltage for PHM can be increased by increasing the load resistance R_L, however, this will also have the effect of increasing the time taken for bits to decay at the receiver, reducing the maximum achievable data rate. How to approach this tradeoff would depend on the specific application, and whether data rate or link gain is more valuable.

The purpose of the damping switches is to modulate the Q-factor of both sides of the link; when a bit is to be transferred, they are open so the Q is high. When a bit has been transmitted and received, the switches close, reducing the Q of both sides and clearing the remaining energy from the transmission channel.

The benefits of SQuirM can be summarized as follows:

- **Reduced power consumption:** The transmitter only needs to generate one sharp pulse instead of two; the amplitude at the receiver is higher, therefore the receiver requires less gain.
- **Reduced complexity:** Timing requirements are far less strict, with only monopolar pulsing. There is no need for precise timing circuitry or bidirectional drivers.
- **Improved resilience:** Small errors in impulse generation, or deviations in link parameters have far less impact on data transmission than in PHM. Striking and damping pulses in SQuirM do not need to be as precise as PHM demands, they only need to be 'good enough'.

III. Transmitter and Receiver Circuits

A. Transmitter Details

Fig. 6 shows the transmitter circuit. It consists of three key parts, the impulse generator, the trimmable output switch (M_{Tx}), and the damping switch (M_{Txd}). The sizing of the output stage and damping devices is a tradeoff between r_{on} and parasitic capacitances. The damping switch M_{Txd} should be large enough that its r_{on} is small (to sufficiently damp the transmission coil), but also be small enough so as not to cause charge-injection problems, or overload the data input with gate-capacitance. A target value of $r_{on(M_{Txd})}$, (referred to as R_D from this point onward) can be found by using the principle of loaded Q [19]. Take for example a 120 nH transmission coil with a Q-factor of 100 at 300 MHz, ($\therefore R_S = 2.26\Omega$), the loaded Q can be considered in terms of R_D as:

$$Q_L = \frac{R_D\,(Q + 1/Q)}{\omega L\,(Q + 1/Q) + R_D}\,. \tag{1}$$

By rewriting Q_L as Q/α, (1) can be rearranged into an expression for R_D, that will make the Q smaller by a factor of α:

$$R_D = \frac{\omega L}{\frac{\alpha}{Q} - \frac{1}{Q+\frac{1}{Q}}}\,. \tag{2}$$

In order to reduce the Q of this example coil 10× (from 100 to 10), (2) returns the minimum value of R_D to be 2.51 kΩ. The on-resistance of M_{Txd} was simulated to be 1.6 kΩ; more than sufficient to damp this typical example coil.

The output switch M_{Tx} shown in Fig. 6(b) is programmable with 3 power control taps, and also has similar tradeoffs. The switch should be large enough to draw a large current burst through the transmission coil, but must have a low enough gate capacitance for the impulse generator to be able to drive it. If M_{Tx} is too large, the capacitance at its drain (C_{DD}) will add to C_1, detuning the coil. To save power, M_{Tx} was fairly small in this implementation. With all three power taps switched on, the peak drain current into M_{Tx} is approximately 2 mA.

The impulse generator is shown inset into Fig. 6(a). The pulse-width is mainly dependent on the length of the delay set by the delay capacitor, but also has some dependence on the rise-time of the incoming data, as well as process variation in the logic gates. To reduce errors in pulse timing, the data rise time should be as consistent as possible. Differences in rise time between bits would create inconsistent impulse widths, and therefore inconsistent ringing symbols. Fig. 7 shows post-layout simulated pulse widths for the impulse generator against changing capacitor codes, with a Monte Carlo spread included

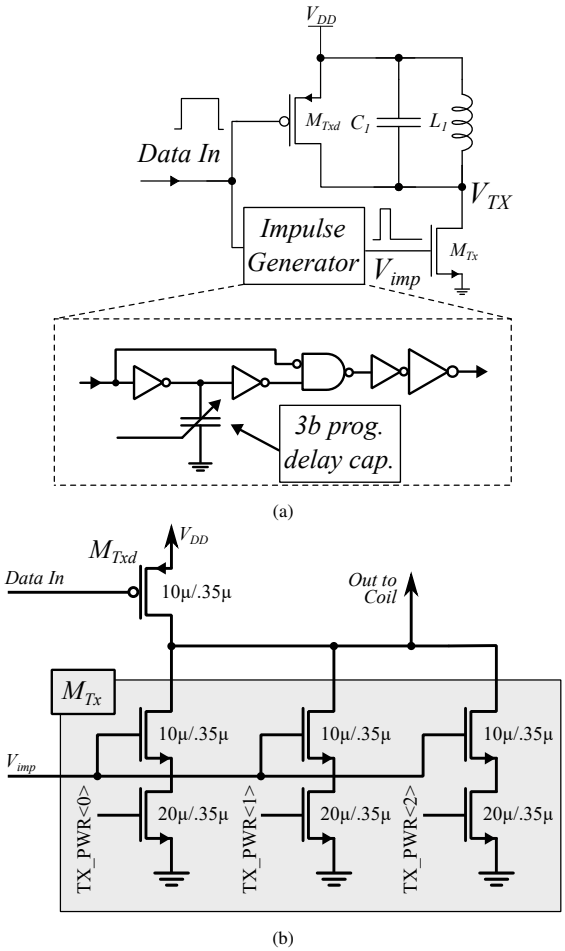


Fig. 6. (a): Detailed transmitter circuit block diagram. (b): Expanded view of the output stage. M_{Tx} has 3 taps to alter the output power. The 3-bit trimcap is binary weighted, with 40, 80, and 160 fF MIM capacitors.

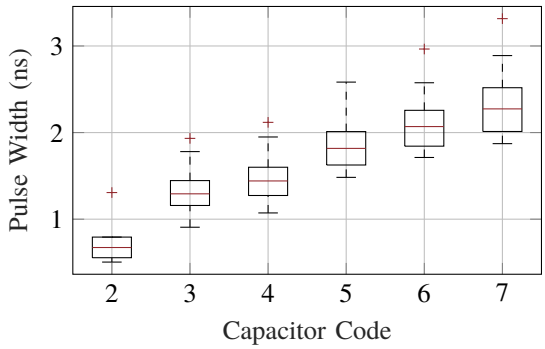


Fig. 7. Postlayout Monte Carlo spread of pulse widths from the impulse generator in Fig. 6(a)

(20 runs per code). The wide spread of the boxplots shows the limitations of the logic-gate based method; small variations in the trip-threshold of the gates can lead to comparatively large variations in delay. However, it is a small low-power design, which is more valuable than extremely refined pulse-width control in this context.

To generate maximum output amplitude, the drive pulse width should ideally be exactly one-half cycle of the Tx coil natural frequency [15]:

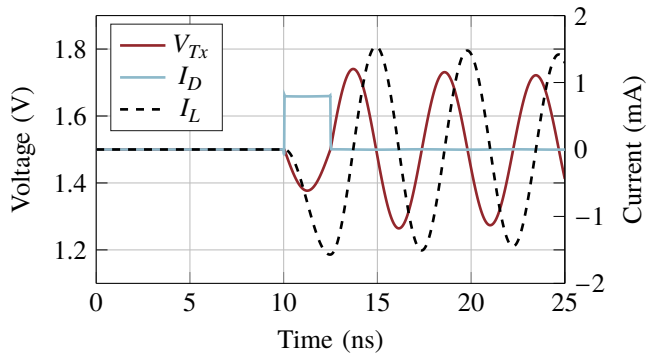


Fig. 8. A well-timed current pulse into a resonant circuit, f_0 = 205.5 MHz.

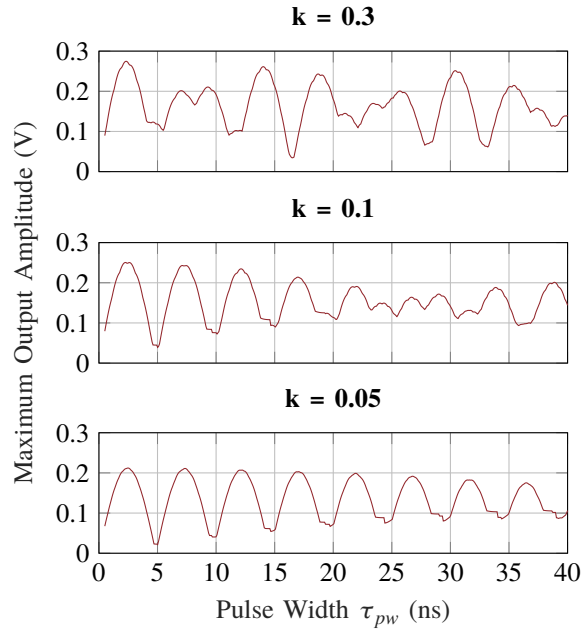


Fig. 9. Simulated data of maximum amplitude seen at the receiver, for varying pulse widths and coupling factors, for two coupled tanks with f_0 = 205.5 MHz, $\tau_{pw(opt)} \approx 2.433$ ns.

$$\tau_{pw(opt)} = \pi\sqrt{L_1 C_1} = \frac{1}{2f_0}\,. \tag{3}$$

A drive impulse from M_{Tx} with a pulse width of $\tau_{pw(opt)}$ will draw current through the inductor until the maximum current is reached. This is illustrated in Fig. 8; the falling edge of I_D aligns perfectly with the peak negative current in I_L. A shorter pulse will give a lower amplitude, but also save power, since less overall charge is being injected. A pulse longer than $\tau_{pw(opt)}$ will have a reduced amplitude, since some of the freewheeling current in the tank will be drawn away by M_{Tx}. If the pulse generator cannot generate a short enough pulse, a compromise solution is to make the pulse width close to any other odd multiple of half-cycles. The falling edge of I_D will still align with a maximum negative coil current, and achieve a higher amplitude. This relationship does not hold perfectly when taking into account the coupled receiver however, particularly at higher coupling factors. The

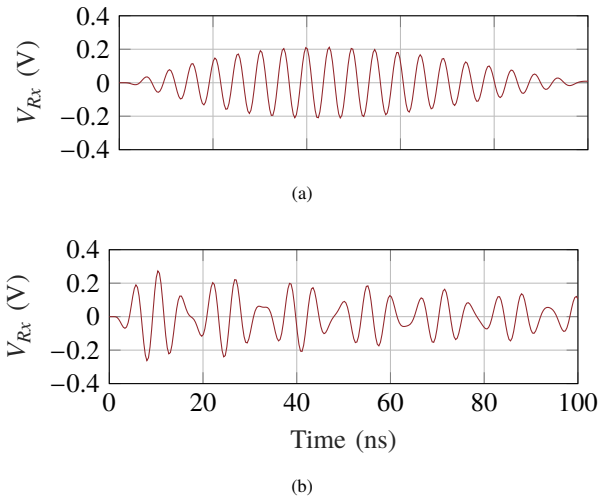


Fig. 10. Output voltage responses of the example link at (a): low (k = 0.05) and (b): high (k = 0.3) coupling factors. The response shows a mix of the two peak frequencies at high coupling.

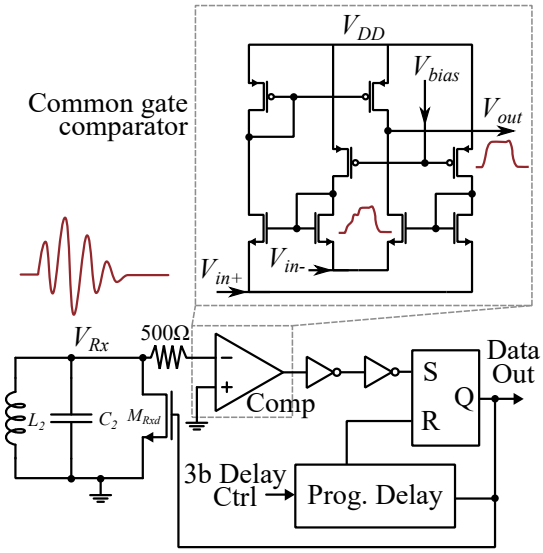


Fig. 11. Details of the receiver circuitry.

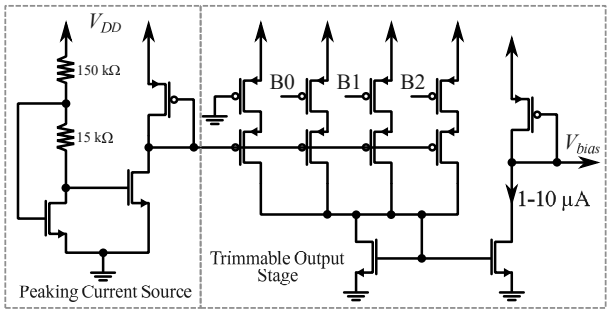


Fig. 12. Trimmable peaking current source, with 3 equally weighted output taps.

effect of higher coupling factors is illustrated in Fig. 9; at lower coupling factors, the odd-multiple half-cycle rule holds, but breaks down as the coupling factor increases. This effect must be accounted for when tuning the drive pulse-width with tightly coupled coils.

The reason this behaviour occurs at high coupling factors is because of the double-peaked impedance curve that the link has due to frequency splitting [20], [21]. After a link with a split response is struck with an impulse, instead of both sides ringing at f_0, they will ring at a combination of the two peak frequencies that result from splitting. Double peak ringing is illustrated in Fig. 10.

B. Receiver Details

Fig. 11 shows the receiver circuit; the key components are the input comparator, and the programmable delay-reset block. The comparator design is a ground-referenced common-gate based comparator [22]. While any AM-demodulator would be able to recover the received datastream, this comparator-only approach was chosen because it is low power and effective. The comparator operates by balancing two common-gate amplifiers that push-pull the output stage. The comparator trips when one branch current becomes larger than the other, activating the push or the pull device. The trip-threshold of the comparator can be adjusted by modifying the sizes of the PMOS devices driven by V_{bias}. The offset can also be fine-tuned by adding a resistor in series with one of the inputs; here a 500 Ω resistor was used to give a small offset, as well as some isolation between the receiving tank and the comparator input. V_{bias} was generated with a peaking current source with a trimmable output stage as shown in Fig. 12. The output taps provide some control over the bias current, to compensate for process variation in the comparator devices.

Fig. 13 shows simulated waveforms for the receiver chain blocks. The 'push' PMOS in the push-pull output stage of the comparator generates more current than the 'pull' NMOS; as a result, the comparator output voltage gets pushed further up with each cycle at the input, rather than returning fully to ground each cycle. In this way the comparators perform both amplification and envelope detection in a single circuit. The inverters at the output of the comparator square up the glitchy output, to be fed to the output data latch.

The output data latch is set whenever the comparator buffer swings high, offering further protection from glitches in the comparator output. The programmable delay block determines how long output data bits are held on the latch before they are cleared. Since the received pulses are directly used to damp the receiver coil, setting this width also controls the length of time that the coil is damped. Longer delays will damp the receiver more, but will also reduce the maximum achievable data rate.

IV. Chip Measurements

The transmitter and receiver were designed in 0.35 µm CMOS, capable of operating with supplies between 1.2 V and 3.6 V. Fig. 14 shows the layout and dimensions of the final circuits.

A. Experimental Setup

Fig. 15 shows the arrangement for performing measurements. One chip was used as a dedicated transmitter, and one

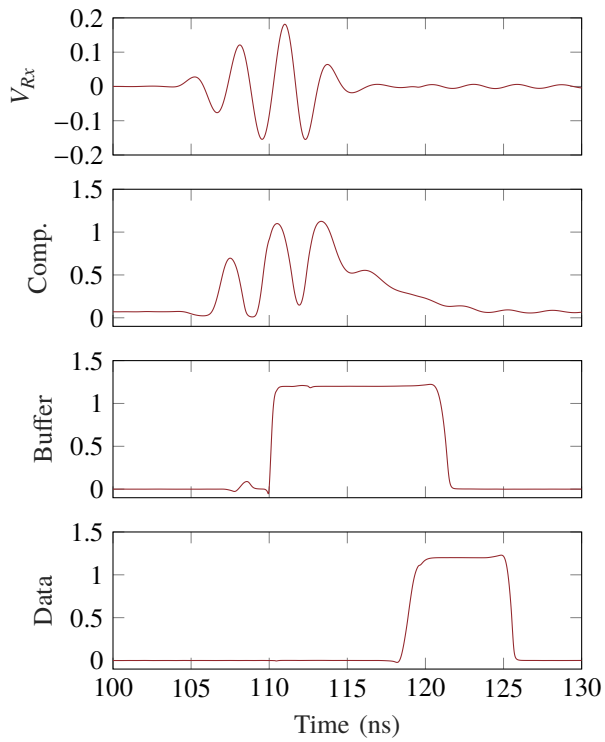
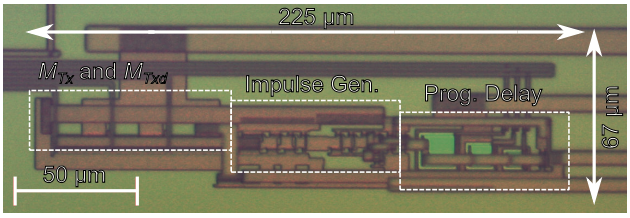


Fig. 13. Simulated voltages for the receiver chain, with a short delay set in the delay block. All vertical axis units are Volts.



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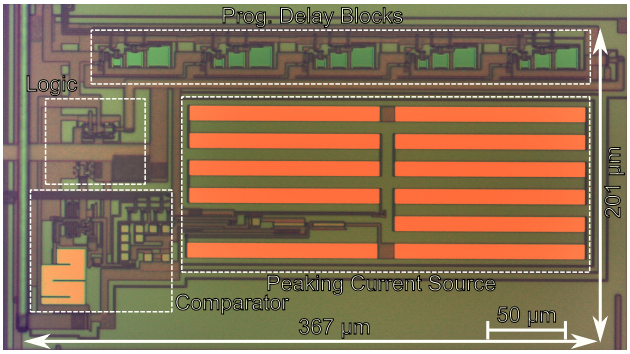
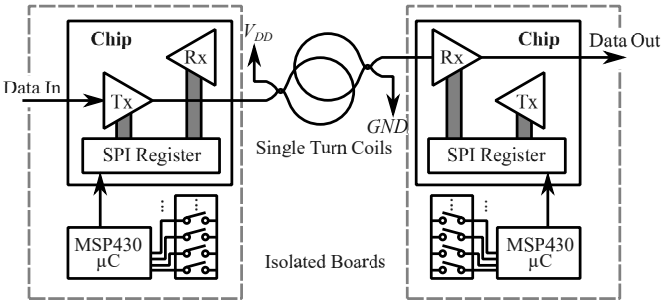


(b)

Fig. 14. Chip photos showing the layout and dimensions of (a) the transmitter circuit, and (b) the receiver circuit.



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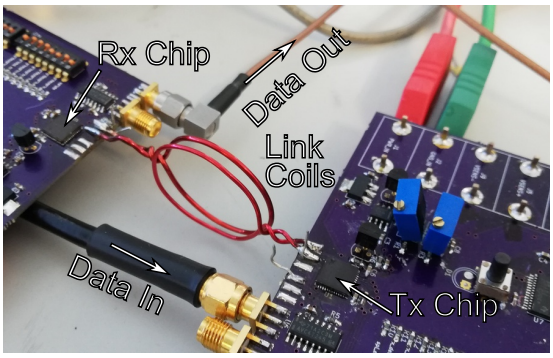


(b)

Fig. 15. Experimental setup: (a) diagram and (b) photo.

as a dedicated receiver, each with it's own isolated board. The trimmable circuit elements were controlled using SPI to reduce pin count. This SPI register was controlled by a microcontroller (TI MSP430), which periodically reads the state of a bank of toggle switches. Each board was also equipped with adjustable power supplies, with current monitoring. The single turn coils were 28 mm in diameter, wound using standard 1 mm diameter magnet wire. They were directly soldered to pads as close as possible to the chip, to minimize parasitics. The length of the PCB traces for the Tx and Rx coils were closely matched, so that any parasitic losses should be similar.

The coils were both measured to have inductances of 70 nH $\pm$1 nH, with negligible losses at frequencies below 30 MHz, measured using an impedance analyzer (Wayne Kerr 6500B). Due to the 30 MHz limit of the instrument, it was difficult to measure the quality factor and self-resonant frequency (SRF) f_0 of these coils directly. The SRF could be inferred by inspecting the resonant bursts from running the system however. Using this method, the resonant frequency of these coils (in parallel with all other system parasitics) was found to be 181.8 MHz. This suggests a total in-system parallel capacitance of 10.95 pF; it is not feasible to measure this precisely however. Substituting this value for f_0 back into (3) yields a value of $\tau_{pw(opt)}$ = 2.75 ns. This is well within the capabilities of the impulse generator (see Fig. 7).

Fig. 16 shows the arrangement that was used for generating input data streams, and recovering them in the case of bit-error rate (BER) tests. A function generator (Agilent 33250A) was used to generate strings of repeated 1's to determine the maximum data rate the link could handle. To test the BER of the system, an FPGA (Xilinx Spartan 7) was used to generate

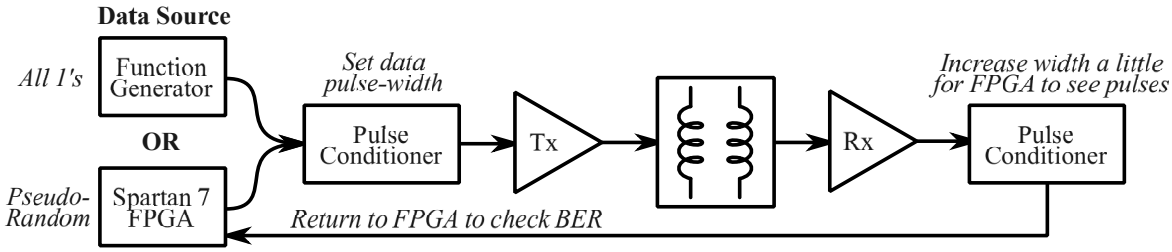
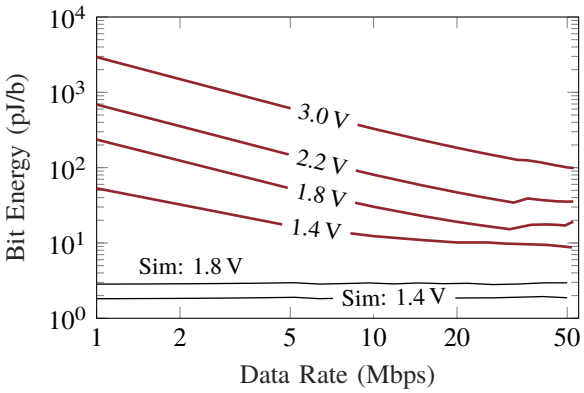
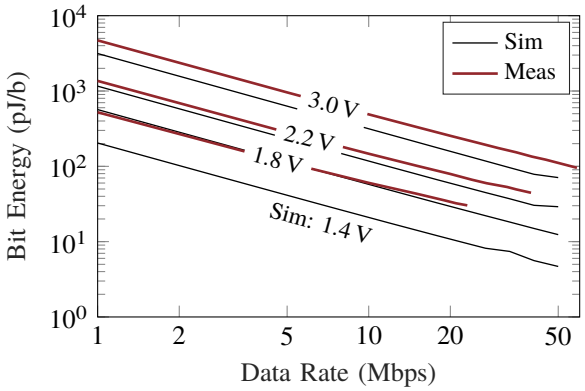


Fig. 16. Equipment setup for producing and recovering datastreams.



(a)



(b)

Fig. 17. Measured and simulated power consumption per bit for (a): transmitter and (b): receiver circuits.

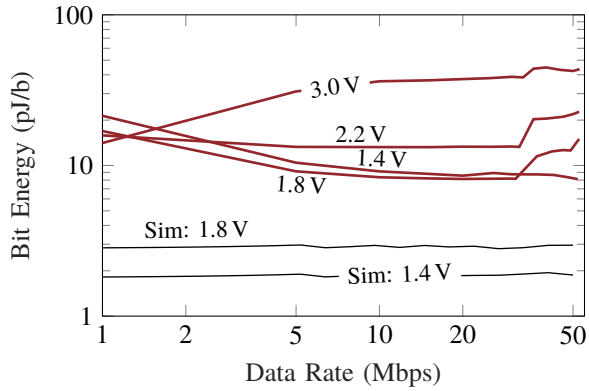


Fig. 18. Inferred measured Tx power without quiescent draw from the receiver.

(8.6 Gb) pseudorandom sequences, which are fed back to the FPGA for comparison after transmission through the system. Any non-matching bits are counted, and a BER calculated.

B. Power Consumption

Fig. 17 shows the measured energy-per-bit values for the Tx and Rx circuits. When testing power, the data rate was a stream of continuous 1's to simulate a theoretical worst case.

Fig. 17(a) shows that at low supply voltages and high data rates, the transmitter mostly consumes dynamic power; this is because the transmitter is essentially all digital, unless it is sending a bit, it requires no current. The best recorded Tx power consumption being 8.72 pJ/b, with a data rate of 52 Mbps at 1.4 V supply voltage.

Fig. 17(b) shows power consumption curves for the Rx circuit; for all supply voltages the consumption is almost completely quiescent. The consumption is mostly quiescent as a result of the peaking current source used to generate a bias for the receiver. By improving this block to use less power, the consumption would become more dynamic. Reducing the supply voltage here gives significant power savings, but at the cost of maximum data rate. At a supply voltage of 3.0 V, the receiver operates at a maximum data rate of 58.6 Mbps, but only reaches 23.1 Mbps with a 1.8 V supply.

The profile of Fig. 17(b) shows a very similar gradient to the quiescent Tx power in Fig. 17(a). Measurements revealed that the quiescent Tx component was drawn by the Rx circuit, even when its bias generator was disabled. Since both circuits were connected to the same supply pad, this baseline current draw from the Rx had to be removed from the measurements afterwards.

Fig. 18 shows the recorded Tx power consumption after subtracting the quiescent baseline drawn by the disabled receiver; it shows that the true Tx power consumption is almost purely dynamic. However, the measured power consumption is still significantly higher than the simulated case (1.47 pJ/b [18]), with the best recorded value being 8.11 pJ/b at 52 Mbps at 1.4 V. This extra power draw and anomalous changes in gradient of the measured results at high and low data rates are difficult to explain, they are potentially the result of unaccounted leakages or parasitics in the system.

It should be noted that while both circuits were designed to ideally operate from 1.2 V supplies, this voltage was found experimentally to be too low for them to operate. While the transmitter generates successful V_{Tx} pulses at 1.2 V, the range is limited. The speed of the circuit degrades significantly for supplies lower than 1.8 V.

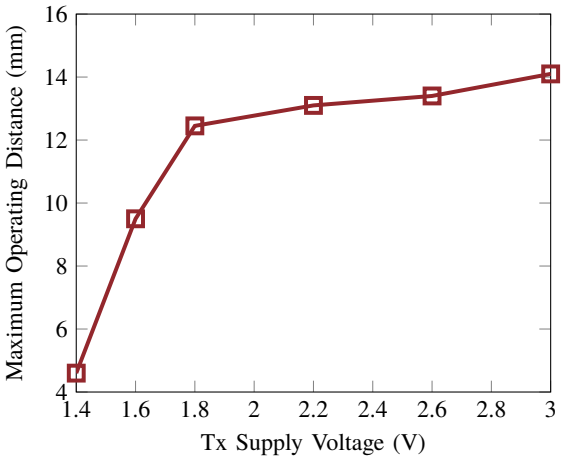


Fig. 19. Maximum coil distance vs Tx supply voltage.

C. Bit Error Rate and Resilience

Fig. 19 shows the measured maximum operating distance of the system for a range of Tx supply voltages. For each distance step, the supply voltage was reduced and the datastream was visually inspected using an oscilloscope, if significant jitter or dropped bits were apparent, then the supply was backed off by a few mV and noted. The plot shows a sudden drop in range for Tx supplies lower than 1.8 V, this is expected, since the 0.35 µm process is designed for 3 V operation. By implementing the design in a smaller process node, e.g. 65 nm, better performance would be expected at lower supply voltages.

The Rx supply was swept in these tests, but since it has no real effect on gain, rather on the maximum data rate that can be recovered, it has no real impact on the maximum operating distance. The Rx supply voltage was therefore fixed at 3.0 V for these tests, and a 40 Mbps pseudorandom stream was used. A clean example sequence is shown in Fig. 20, where several hundred captures are overlaid to demonstrate the observed jitter. The input stream has approximately 0.5 ns of jitter, and 1 ns at the output; the jitter here is low enough that no significant problems in data transfer were observed at the speeds that were tested.

The BER performance of the system was tested by using the arrangement in Fig. 16. The FPGA (a Xilinx Artix-7) was configured to generate an ≈ 8.59 Gb long pseudorandom sequence, generated by a 33 bit linear feedback shift register. This sequence was passed through the system at a range of distances and data rates, and the number of errors was counted. Both power supplies were fixed at 3 V for these BER tests.

Bit error rates were determined to a 95% confidence level by using Wilson's score interval [26].

Fig. 21 shows the results of the BER tests. The upper and lower black lines are the upper and lower confidence levels, respectively. The regions between these lines are shaded. For data rates of up to 49.5 Mbps, the calculated BER is less than 4.472×10^{-10}. The exception is when the coil distance increases to 14.5 mm, where it increases slightly at some lower data rates, e.g. 14.5 mm, 37.5 Mbps, the calculated BER is between 7.151×10^{-10} and 2.293×10^{-9}. Overall the BER results here show a very slight dependence on coil distance:

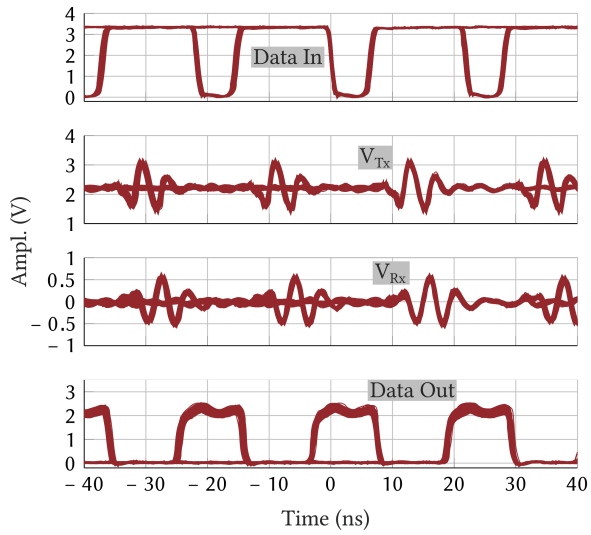


Fig. 20. Measured waveforms for a 40 Mbps pseudorandom data sequence, demonstrating a low level of jitter over time. The 'Data In' stream is an inverted copy, the true stream is active high.

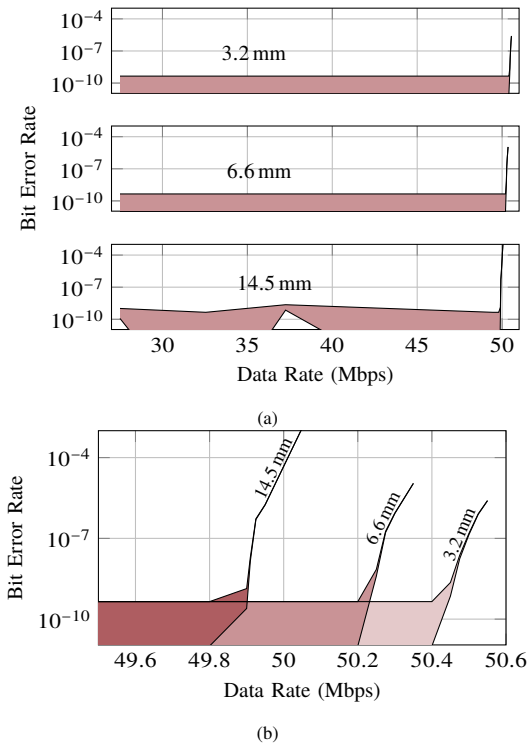


Fig. 21. (a): BER results across a range of coil spacings and data rates. (b): Zoomed in view of the point at which many errors occur. The regions between the upper and lower confidence levels are shaded. If the lower bound is zero, the shaded area extends downward forever.

TABLE II
TABLE OF COMPARISON FOR INDUCTIVE DATA TELEMETRY SCHEMES.

Ref.	Scheme	Range	Data Rate (Mbps)	Tx Power (pJ/b)	CMOS Node	BER	FoM ($\frac{\text{bps}\times\text{dist}}{\text{BER}\times\text{pwr}}$)
[15]	PHM	10 mm	10.2	345	0.5 µm	6.3×10^{-8}	0.00469
[17]	PHM	10 mm	20	180	0.35 µm	8.7×10^{-8}	0.0127
[14]	OQPSK	5 mm	4.16	N/A	0.18 µm	2×10^{-6}	N/A
[23]	TTC†	70 mm	50	0.475	0.18 µm	$< 1 \times 10^{-3}$	0.00737
[24]	LSK	20 mm	2.8	35.7	0.5 µm	$< 10^{-6}$	0.00157
[25]	PDM	10 mm	13.56	960	0.35 µm	4.3×10^{-7}	0.000328
This Work	SQuirM	14.5 mm	49.8	43.56	0.35 µm	$< 4.5 \times 10^{-10}$	36.838

†Transmission Time Control.

the maximum data rate (before rapid increase in BER) for 3.2 mm is ≈50.4 Mbps, whereas for 14.5 mm it is ≈49.7 Mbps, a difference of only 1.4%.

1) Coil Misalignment: The system operating range is currently expressed in terms of millimeters of coaxial displacement. This can be considered in a more general sense as a range of coupling coefficient values. By simulating the coupled coils in software [27], the range of coaxial displacements were converted to coupling coefficients; the maximum distance of 14.5 mm translates to $k = 0.082$. Since misalignment in any dimension translates to a change in k, this translation can be used to translate between misalignments across different dimensions.

Lateral misalignments were simulated across a range of coaxial distances, to determine an operating region that combines both coaxial and lateral misalignments. This is shown as a contour plot in Fig. 22. Distances are all measured from center to center. The contours show how the overall lateral displacement tolerance is of a similar magnitude to the coaxial displacement tolerance, and define an elliptic envelope within which the link should operate well.

Angular misalignments can be treated in exactly the same way as lateral misalignments, by considering them in terms of k, and mapping contours as in Fig. 22; this is omitted here for the sake of brevity. Previous analyses suggest that angular misalignment has a similar effect on the coupling to lateral misalignment, but overall is dependent on coil geometry and total misalignments across all dimensions [28], [29].

2) Power Carriers: Since most IMDs employing SQuirM would require an inductive power link in parallel, it is important to consider the possibility that the power link acts as a strong out of band blocker, severely degrading the SQuirM link. There are many approaches that can be used to mitigate this problem. For example, the original PHM implementation uses figure-8 coils for data, and round coils for power [15], to minimize cross-coupling between power and data channels. Assuming there is sufficient physical space, power and data coils can also be physically separated laterally to minimize cross-coupling [14]. Depending on implementation, if the power carrier frequency f_{pwr} is sufficiently far away from the data coil SRF f_0, the natural filtering effect of the resonant data

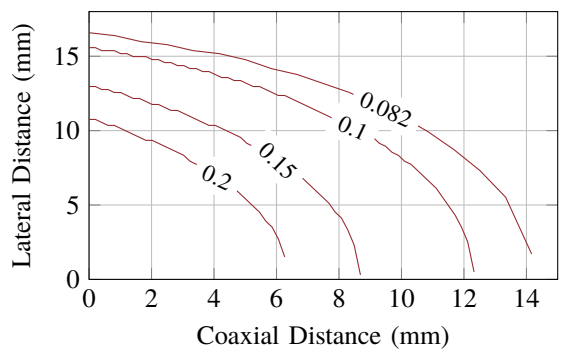


Fig. 22. Lines of constant k for varying displacements.

coils may be enough to suppress the power carrier. In addition, a notch filter at f_{pwr} can be added in parallel with the data coils to further suppress a fixed frequency power carrier.

To assess the impact of a nearby power carrier on the SQuirM link, a class-E power amplifier was used to drive a resonant transmitter coil at 13.56 MHz, which was then placed 2-3 mm from the data coils, coaxially aligned with them, to simulate a worst case scenario. Fig. 23 shows the effect of this power carrier on data transmission. Fig. 23(a) shows that even with strong interference (the power signal is 6.38 dB larger than the data), if the data coils are sufficiently coupled, demodulation is still successful. Fig. 23(b) shows that at larger data coil separations, the strong, uncompensated power carrier degrades data transmission.

3) Surrounding Tissue: In the case of an IMD, the effects of surrounding tissue can be a problem for some wireless telemetry systems, due to RF absorption and coil detuning. This could pose a problem for a SQuirM system if it were scaled to use much smaller coils, with self resonant frequencies in the GHz range, as tissue absorption increases with frequency. Since the system presented here uses coils with SRFs of approximately 180 MHz, the presence of tissue should not significantly impact the link performance. Testing the system with an approximately 1 cm thick cut of pork belly (with muscle, fat, and skin layers) wrapped in plastic between the coils yielded no measurable difference compared to the in air measurements.

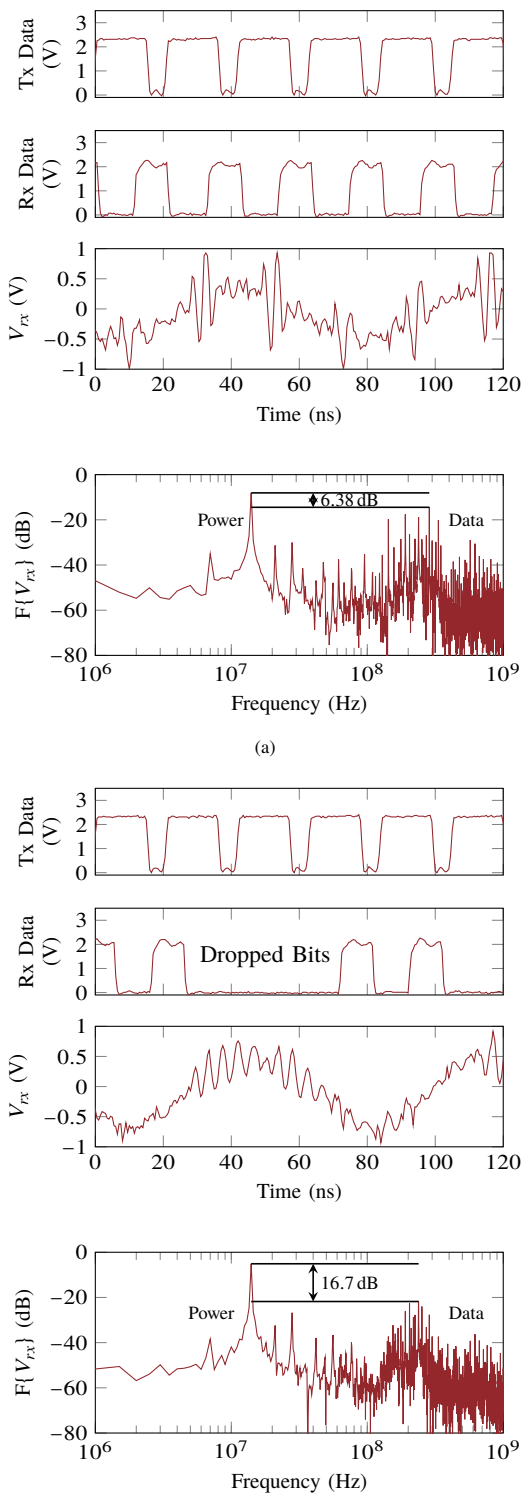


Fig. 23. Measured results with an interfering power carrier, closely coupled to the data coils (within 3 mm of Rx coil). Data coil separation is (a): 3 mm, and (b): 14 mm.

V. Discussion and Conclusions

Table II shows how SQuirM compares to other inductive link based data transmission schemes. SQuirM achieves far better performance than other methods mainly used in the biomedical circuits field (LSK, OQPSK, PHM) in terms of data rate, power consumption, and BER, while working at a similar range. While the TTC scheme presented by Lee et al. [23] is superior in terms of power consumption and range, its BER performance is not. The FoM in Table II is based on the range in millimeters, the data rate in megabits per second, the BER in parts per billion, and the transmitter bit energy in picojoules per bit, defined as:

$$\text{FoM} = \frac{\text{Data Rate (Mbps)} \times \text{Range (mm)}}{\text{BER (ppb)} \times \text{Tx Bit Energy (pJ/b)}}. \tag{4}$$

SQuirM achieved a FoM that is three orders of magnitude better than the state-of-the-art. The energy efficiency, data rate, and BER results represent a significant improvement over the results of previous impulse-based systems. In addition, given the simplicity of the scheme, SQuirM lends itself to easy adoption without the need for complex tuning and trimming. Given its capacity for high data rate transmission, which can be further increased by using smaller coils with a higher SRF, SQuirM also lends itself to consumer applications where large amounts of data need to be transferred over a short distance.

Future work could include re-implementation in smaller CMOS nodes, to improve performance, and improving the robustness of the receiver design with respect to process variations. This could also include redesign of the impulse generator to be less process dependent, making it easier to drive different coils with different SRF values, targeting higher data rates.

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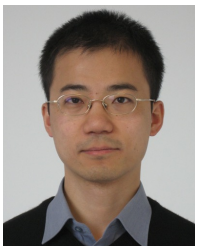
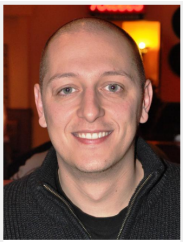
Matthew Schormans (S'14-M'19) received the M.Eng. degree in electronic and electrical engineering from University College London, London, U.K., in 2014, where he is also currently working towards the Ph.D. degree in electronic and electrical engineering, with a focus on short-range wireless power and data telemetry for implantable medical devices.

He has authored several conference and journal publications on biomedical systems employing inductive links and techniques for employing inductive links for both power and data transfer in a biomedical context.

His research is concerned primarily with biomedical wireless power telemetry systems, but his interests also include inductive link modelling, oscillators, and more general power converter and mixed signal design.



Dai Jiang Dai Jiang (S'07–M'09) received the B.Sc. and M.Sc. degrees from the Beijing University of Aeronautics and Astronautics, Beijing, China, in 1998 and 2001, respectively, and the Ph.D. degree from University College London (UCL), London, U.K., in 2009, working on frequency synthesis. From 2001 to 2002, he was with Datang Telecom Group, China, developing FPGA functions for WCDMA signal processing. He joined the Analog and Biomedical Electronics Group at UCL in 2006, where he is a currently a Senior Research Fellow. His research interests include CMOS analog and mixed-signal integrated circuit design for biomedical applications. Dr Jiang is a Member of the Biomedical and Life Science Circuits and Systems Technical Committee of the IEEE Circuits and Systems Society.



Virgilio Valente (S'09-M'11) was born in Milan, Italy, in 1979. He received the B.Sc. degree (first class honors) in electronic engineering in 2004 from the University of York, York, U.K., the M.Sc. degree in biomedical engineering in 2006 from Aalborg University, Aalborg, Denmark, and the Ph.D. degree in electronic and electrical engineering from University College London (UCL), London, U.K., in 2011. From 2011 to 2017 he was a Research Associate in the Analog and Biomedical Electronics Group at UCL, during which, in 2015, he also joined Tetrivis Ltd, U.K., as an IC design engineer. In 2017 he was a Visiting Scholar in the Nano Lab at Tufts University, USA. Currently, he is an Assistant Professor (Research) in Bioelectronics, within the Department of Microelectronics at Delft University of Technology, Netherlands.

His research interests focus on the development of analog and mixed-mode CMOS integrated circuits for a range of applications, including BioCMOS, lab-on-CMOS and organ-on-chip platforms, implantable and injectable CMOS biosensors, CMOS-microfluidic devices and smart wireless telemetry systems.

Dr. Valente is a member of the Biomedical Circuits and Systems (BioCAS) Technical Committee of the IEEE Circuits and Systems Society (CASS), the recipient of the 2017 EPSRC IRC i-sense Mobility Fellowship, and the Technical Chair of the Biomedical Circuits and Systems Track of the IEEE 2019 Asian Pacific Conference on Circuits and Systems (APCCAS).

Andreas Demosthenous (S'94-M'99-SM'05-F'18) received the B.Eng. degree in electrical and electronic engineering from the University of Leicester, Leicester, U.K., the M.Sc. degree in telecommunications technology from Aston University, Birmingham, U.K., and the Ph.D. degree in electronic and electrical engineering from University College London (UCL), London, U.K., in 1992, 1994, and 1998, respectively. He is a Professor in the UCL Department of Electronic and Electrical Engineering and leads the Analog and Biomedical Electronics Group. His research interests include analog and mixed-signal integrated circuits for biomedical, sensor, and signal processing applications. He has made outstanding contributions to improving safety and performance in integrated circuit design for active medical devices, such as spinal cord and brain stimulators. He has authored over 300 articles in journals and international conference proceedings, several book chapters, and holds several patents.

He is currently the Editor-in-Chief of the IEEE Transactions on Circuits and Systems I: Regular Papers, an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems, and serves on the International Advisory Board of Physiological Measurement. He is a member of the Technical Programme Committee of several IEEE conferences, including the European Solid-State Circuits Conference and the International Symposium on Circuits and Systems.

Dr. Demosthenous is a fellow of the Institution of Engineering and Technology and a Chartered Engineer.