Noise Analysis of Multiplicative Distributed Amplifiers

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***Abstract*—This paper analyses the noise performance of cascaded and matrix single stage distributed amplifiers (C-SSDA and M-SSDA), together termed multiplicative distributed amplifiers. The analytical expressions derived are verified and applied in predicting the noise figure of a two- and three-tiered M-SSDA based on a full foundry model of an InP double heterojunction bipolar transistor (DHBT). Based on observations from the analytical study, we provide design considerations that optimise noise, gain and bandwidth performance for this class of distributed amplifiers, for improved utility in ultra-wideband applications.**

***Index Terms*—Distributed amplifier, Noise figure, Ultra-wideband, Noise modelling, Circuit modelling, Single stage distributed amplifier (SSDA), cascaded-SSDA, matrix-SSDA,**

I. Introduction

The distributed amplifier (DA) was conceived as a multi-stage amplifier with better wideband performance arising from the absorption of bandwidth-limiting intrinsic capacitances into artificial transmission lines; and additive gain properties [1–3]. However, recent studies have established the potential of the single stage distributed amplifier (SSDA) and its cascaded and matrix derivatives for remarkable gain-bandwidth performance [4–13]. The cascaded SSDA (C-SSDA) and matrix SSDA (M-SSDA) both share a unique property in that they employ purely multiplicative gain [14], hence we have termed them multiplicative DAs. While the SSDA topology presents notable advantages in design simplicity, wideband performance and higher average gain, it offers a poorer signal-to-noise behaviour compared to multi-stage DAs. This is due to a rather interesting property of the multi-stage DA, where each additional stage reduces the overall noise figure, a merit which the SSDA and its multiplicative derivatives do not share [14–16]. Hence, it is necessary to assess the noise performance of multiplicative DAs, in order to appraise the utility of the topology in system applications.

This paper presents an analytical and simulation-based study of the noise figure of multiplicative DAs. Studies of the noise figure performance of field-effect-based DAs have been reported, the most definitive of which are the works of Niclas and others in [14, 15] and Aitchison in [16]. Noise figure analysis for cascaded and matrix multi-stage DA configurations [17], with different gain cells (common emitter [14–16, 18], cascode [19] and common collector-cascode [20]) and under different loading and termination conditions [21–23] have also been reported. This work builds on these studies to offer insight into the noise performance of multiplicative DAs, the aim of which is to highlight the peculiarities of the SSDA topology and its multiplicative derivatives. Based on observations from the analytical study, we present approaches to design optimisation that minimise overall noise, to match given design requirements and system specifications.

The outline of this paper is as follows; section II presents a new analytical model for the intrinsic noise figure of multiplicative DAs, describing how it is derived. The model is also verified in this section and applied in predicting the noise figure of a two-and three-tiered M-SSDA based on a common-emitter gain cell which features the full foundry process model of Teledyne TSC250 InP double heterojunction bipolar transistor (DHBT) as active device. Section III discusses approaches to optimising the noise performance, gain and bandwidth of multiplicative DAs. Section IV concludes the paper.

II. Modelling of Noise in Multiplicative DAs

A. Evaluating Single Stage Noise Figure

The noise sources of DAs have been identified as: noise associated with the active device(s) in each of the n gain stages; thermal noise contribution from the source impedance at the standard temperature T_o; thermal noise contribution from input and output transmission line terminations at T_o; and noise contributions from lossy transmission line elements [15, 16]. The noise associated with the load impedance is considered part of the network that follows the DA and is therefore not included as a contributor to the DA noise figure. It is usual also, to neglect the losses associated with the transmission line elements (which may include lossy inductors or capacitors) as these are comparatively small [14–16, 21].

First, we consider the case in which a field effect transistor (FET) such as the MESFET or HEMT is used as the active device. Fig. 1 shows a simplified equivalent circuit for a MESFET/HEMT featuring its associated Van der Ziel gate and drain noise sources [24].

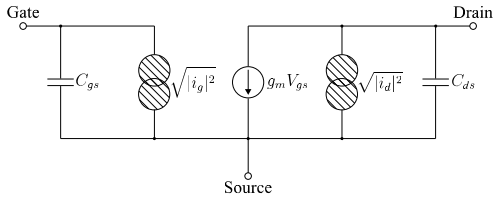


Fig. 1: Simplified equivalent circuit of a MESFET/HEMT with its associated gate and drain noise sources.

The noise factor (F) of the amplifier is defined as [23]

$$F_n = 1 + \frac{\Delta N}{kT_o B G_f} \tag{1}$$

where G_f is the distributed amplifier forward gain, k is Boltzmann's constant ($1.38 \times 10^{-23} J/K$), T_o is 290K, B is the bandwidth at which noise is measured [23] and ΔN is the added noise from the amplifier to its output,

$$\Delta N = N(Z_{\pi d}) + N(Z_{\pi g}) + N_{FET}, \tag{2}$$

where $N(Z_{\pi g}) = kT_oB$ and $N(Z_{\pi d}) = kT_oBG_r$ are the noise power contribution of the drain and gate line terminations (in a π transmission line configuration), respectively; G_r is the reverse gain and N_{FET} is the overall noise associated with the FETs in the amplifier. $Z_{\pi g}$ and $Z_{\pi d}$ are π-image impedance of the gate(input) and drain (output) line transmission lines, respectively of the DA, defined by $Z_\pi = \sqrt{(L/C)/(1-(\omega/\omega_c)^2}$ [3, 16]. Combining (2) and (1) yields

$$F_n = 1 + \frac{1}{G_f} + \frac{G_r}{G_f} + \frac{N_{FET}}{kT_oBG_f}. \tag{3}$$

For the SSDA,

$$G_f = G_r = \frac{g_m^2 Z_{\pi g} Z_{\pi d}}{4}, \tag{4}$$

such that

$$F_1 = 2 + \frac{4}{g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{N_{FET}}{kT_oBG_f}. \tag{5}$$

To evaluate the noise contribution due to the active device (i.e. the last term of (5)), the two main noise contributors in the FET device have been identified by Van der Ziel (1962) as the gate and drain noise power contributors defined as $\overline{i_g^2} = 4kT_oBC_{gs}^2\omega^2 R/g_m$ and $\overline{i_d^2} = 4kT_oBg_mP$, respectively; where R and P are dimensionless coefficients from Van der Ziel's FET noise behaviour model that depend on bias conditions, device geometry and other technological parameters [24, 25].

$$F_1 = 2 + \frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}}. \tag{6}$$

For the multistage DA, the noise figure F is derived as [16]

$$\begin{aligned} F_n = 1 + \left(\frac{sin(n\beta)}{nsin\beta}\right)^2 + \frac{4}{n^2 g_m^2 Z_{\pi d} Z_{\pi g}} \\ + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R \sum_{r=1}^{n} f(r,\beta)}{n^2 g_m} + \frac{4P}{n g_m Z_{\pi g}}, \end{aligned} \tag{7}$$

where

$$\begin{aligned} f(r,\beta) = (n-r+1)^2 + \left(\frac{sin((r-1)\beta)}{sin\beta}\right)^2 \\ + \frac{2(n-r+1)sin(r-1)\beta)cosr\beta}{sin\beta}, \end{aligned} \tag{8}$$

accounts for the phase difference between the two noise sources; $\beta = 2sin^{-1}(\omega/\omega_c)$; n, is the number of amplifier stages; and r represents individual stages [16].

B. Modelling of Noise Factor in Multiplicative DAs

Fig. 2 shows the schematic of a multiplicative DA with *m* gain tiers. For a FET-based DA with *m* multiplicative tiers, the overall added noise is given by,

$$\Delta N = N(Z_{\pi d}) + N(Z_{\pi g}) + \sum N(Z_{\pi - int}) + \sum N_{FET}, \tag{9}$$

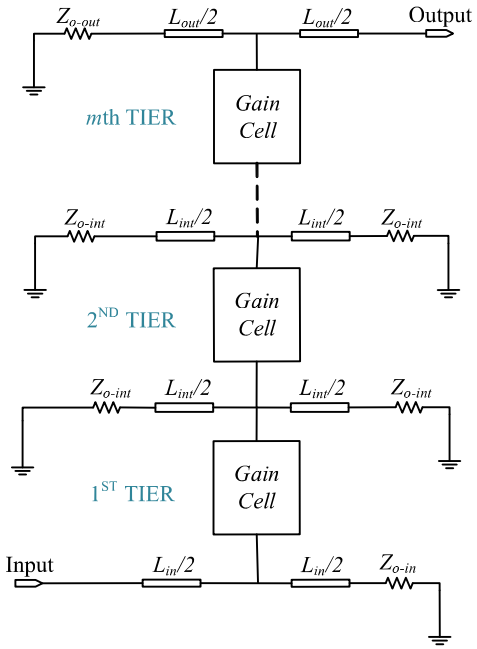


Fig. 2: Schematic of *m*-tier multiplicative DA.

such that we derive the noise factor F_m^m - where the superscript *m* indicates the multiplicative DA and the subscript denotes the number of gain tiers - as

$$F_m^m = 1 + \frac{1}{G_f} + \frac{G_r}{G_f} + \sum_{i=1}^{m-1} \frac{G_r}{G_{int}(i)} + \sum_{l=1}^{m} \frac{N_{FET}(l)}{kT_oBG_f}. \tag{10}$$

$G_{int}(i)$ represents the cumulative gain up to the ith tier of the *m*-tier multiplicative DA and the third term of the equation is multiplied by 2 to account for the presence of two equal terminating resistors on the intermediate line. Forward gain, $G_f = (N^{2m} g_m^{2m} Z_{\pi int}^{2(m-1)} Z_{\pi g} Z_{\pi d})/4^m$, however, as under usual bias conditions, $C_{gs} \gg C_{ds}$, $Z_{\pi int} \approx Z_{\pi g}$, such that $G_f \approx (N^2 g_m^2 Z_{\pi g} Z_{\pi d}/4)^m$. Hence, (10) becomes

$$\begin{aligned} F_m^m = 1 + \left(\frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}}\right)^m \\ + 2\left(\frac{sin(N\beta)}{Nsin\beta}\right)^2 \cdot \sum_{l=0}^{m-1} \left(\frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}}\right)^l \\ + \left(\frac{Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}}\right) \cdot \sum_{l=0}^{m-1} \left(\frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}}\right)^l. \end{aligned} \tag{11}$$

For example, for a two-tiered multiplicative MESFET DA,

$$\begin{aligned} F_2^m = 2 + \frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}} \\ + \left[\frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{4 Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m^3 Z_{\pi d} Z_{\pi g}} + \frac{16P}{g_m^3 Z_{\pi d} Z_{\pi g}^2}\right]. \end{aligned} \tag{12}$$

From (11), we may observe that the highest proportion of total noise is contributed by the first stage, and the noise

contribution from successive stages is only a small fraction of the one preceding it. This is expected in multiplicative amplifiers and agrees with the findings in [14], which followed a chain matrix approach in deriving the overall noise figure in matrix amplifiers. It also suggests that in the case where the gain and noise figure of individual stages are known, the Friis formula for evaluating overall noise figure in cascaded systems may be applicable [26].

An equivalent expression for the intrinsic noise figure of the HBT-based multiplicative DAs may be readily derived following the approach adopted in arriving at (10).

$$\Delta N = N(Z_{\pi b}) + N(Z_{\pi c}) + \sum N(Z_{\pi - int}) + \sum N_{HBT}, \tag{13}$$

such that

$$F_m^m = 2 + \frac{1}{G_f} + 2\sum_{i=1}^{m-1} \frac{G_r}{G_{int}(i)} + \sum_{l=1}^{m} \frac{N_{HBT}(l)}{kT_oBG_f}. \tag{14}$$

with $N(Z_{\pi b})$, $N(Z_{\pi c})$ and $N(Z_{\pi - int})$ are noise contributions from the input (base), output (collector) and intermediate transmission line terminating impedances, respectively; $G_f = G_r = (g_m^2 Z_{\pi b} Z_{\pi c}/4)^m$; and N_{HBT} comprises

$$\overline{i_b^2} = 4kT_oBRe(Y_{ebp} - Y_{ce}) + 2kT_oBg_{be}, \tag{15}$$

and

$$\overline{i_c^2} = 2kT_oBg_m \tag{16}$$

where $Y_{ebp} = gm\sqrt{2j\omega\tau_D}/\tanh\sqrt{2j\omega\tau_D}$; $Y_{ce} = gm\sqrt{2j\omega\tau_D}/\sinh\sqrt{2j\omega\tau_D}$; τ_D is the diffusion time through the base region; and g_{be} is the total input conductance [27, 28].

C. Verification of derived models

We recall the Friis formula for cascaded systems as [26]

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + ... + \frac{F_m - 1}{G_1G_2...G_{m-1}}; \tag{17}$$

where F_{total} is the total noise factor, F_i and G_i are the noise factor and available power gain, respectively of the i-th stage, and m is the number of cascade stages. However, for our application, it is important to note that for Friis' formula to hold, the multiplicative DA must be divided into individual stages, such that F_m and G_m account for the noise and gain contributions, respectively, from the m-th stage alone, rather than cummulative noise or gain contributions. This is achieved by considering the interstage transmission line network(s) as belonging to the output of the preceeding stage [29]. This means that noise figure for successive stages need to be computed excluding noise contribution from the terminating resistances of the intermediate transmission lines they share with their respective preceding stages.

Hence, if F and G of individual stages are known,

$$F_m^m = F_1 + \frac{F_2 - 1 - \Pi_1}{G_1} + \frac{F_3 - 1 - \Pi_2}{G_1G_2} + ... + \frac{F_m - 1 - \Pi_{m-1}}{G_1G_2...G_{m-1}}; \tag{18}$$

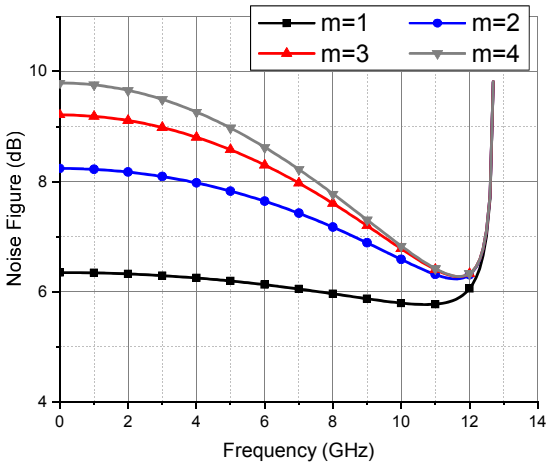


Fig. 3: Verification of (11) for estimating noise figure in multiplicative DAs. Solid lines represent result from (11); symbols represent results from (18).

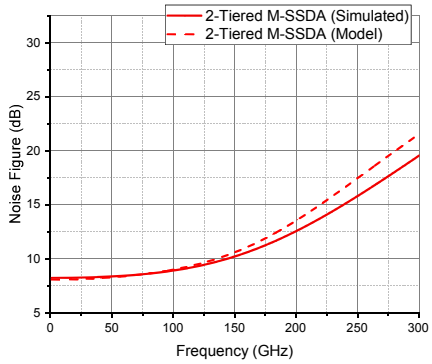
Table I: MESFET Transistor Parameters [16]

Parameter	Value
$Z_{\pi g}$ (Ω)	50
C_{gs} (pF)	0.5
C_{ds} (pF)	0.2
g_m (mS)	30
R	0.2
P	0.6

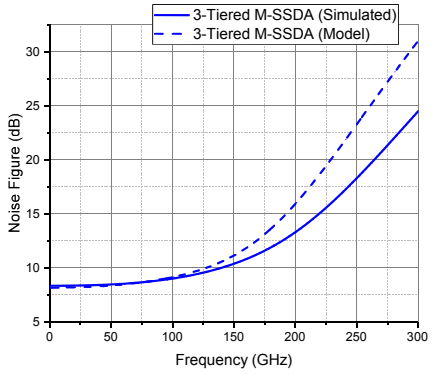
where $\Pi_m = \left(\frac{1}{G_m} + \frac{\sin n\beta}{n\sin\beta}\right)$ represents the noise contribution from the terminating resistors - in both the forward and reverse direction - of the intermediate transmission line that form the input of the tier for which the noise contribution is being computed. The validity of (11) can thus be verified for the case where the multiplicative DA is comprised of identical stages such that $F = F_1 = F_2 = ... = F_m$, and $G = G_1 = G_2 = ... = G_{m-1}$, using the Friis formula with F defined by (6), and G by (4) [26].

Fig. 3 compares the results obtained from adopting (11) and (18) to estimate the noise figure of an assumed MESFET based multiplicative DA using values adopted in [16] and [30]. The equivalent circuit values are presented in Table I As can be seen in Fig. 3, there is perfect agreement between the results obtained using (11) and (18), validating the application of (11) in estimating noise figure in multiplicative DAs. It is important to point out that while (18) can also be used to the same end, its application is limited, as it would require that both the noise figure and gain of individual stages be already known.

Figs. 4(a) and (b) shows the result of the application of the derived models in estimating the noise figure of a two- and a three-tiered M-SSDA, respectively, based on a common-emitter gain cell with a full foundry process model of Teledyne TSC250 DHBT InP device [31, 32]. The close agreement between both solid and dashed lines - representing simulated and modelled results, respectively - within the 3-dB bandwidth of the amplifier (~100 GHz) further validates the derived equation. The deviation - which increases with frequency - is attributed to contributions from the inductive reactance from



(a) 2-Tiered M-SSDA



(b) 3-Tiered M-SSDA

Fig. 4: Verification of (11): Comparison based on a common-emitter gain cell, with transmission lines optimised for bandwidth and gain flatness.

the transmission lines which has not being subtracted from the noise contributions from the individual stages.

III. Discussion: Noise Performance Optimisation for Multiplicative DAs

The following inferences can be drawn from observing (7), in comparison to (6), all pointing to the clear noise-advantage of the multi-stage DAs over the SSDA.

1) The second term is small for large n except for $n\beta \approx 0$ or π, when the expression has a maximum value of unity; for other phase angles, the term can be minimised by increasing n.
2) The third term is the reciprocal of the forward available gain, and can also be minimised by increasing n.
3) The fourth and fifth terms, accounting for noise contributions from the FET gate and drain noise generators, respectively, also reflect inverse proportionality to n, and can be made negligible by increasing n.

However, while it is clear that the SSDA has a disadvantage in noise performance, it is possible to improve gain-to-noise ratio of the multiplicative DA by considering available design trade-offs. A major insight that both (11) and the adapted Friis fomula offer is the need to make the noise factor of the first stage of the multiplicative DA as low as possible while keeping the gain high. Firstly, by inspecting (6), we can see that increasing the impedance of the input line $Z_{\pi g}$ - $Z_{\pi b}$ in the HBT-based case - the second and last terms can be made smaller, reducing F in both the first tier and the overall amplifier. This would also result in increased gain (from (4) however, the cut-off frequency of the input line, and as a result, the amplifier bandwidth would be reduced commensurately.

An alternative solution that does not sacrifice bandwidth but slightly increases design complexity is to use a transistor with a higher bandwidth potential in the first stage. We might recall that the main bandwidth limiting intrinsic elements of the FET and HBT active devices, C_{gs} and C_{π}, respectively, are both dependent on bias current and emitter/source area. This presents a trade-off: a smaller active area reduces the input capacitance thus increasing the bandwidth, but yielding lower gain and lower output power due to lower transconductance values [12, 33]. Adopting such a device in the first stage creates an allowance to design the transmission line of the first stage at a higher characteristic impedance with reduced overall bandwidth penalty. The shortfall in gain can then be compensated by using transistors with higher transconductance in subsequent gain-cell tiers. A useful figure-of-merit for determining the optimum gain-noise relation for the initial cell of cascaded systems is the noise measure (M) from [34].

Overall, considering the noise performance merit of the conventional multi-stage DA, vis-à-vis its gain and bandwidth performance limitation, the case for multiplicative DAs becomes even more compelling. While the noise figure of the multiplicative DA increases quadratically with additional stages, this trend is offset by the gain which increases at an exponential rate, progressively increasing the margin between amplification and added noise. Furthermore, considering that the limitations of the multi-stage DA become more pronounced in ultra-high frequency designs as process parasitics become more predominant in their effect, we find higher justification in adopting the multiplicative DA topologies for ultra-wideband amplification.

IV. Conclusion

In this paper, we have derived and verified new models that describe the noise performance of multiplicative DAs. These models have also been applied in predicting the noise performance of a two- and three-tiered M-SSDA which feature common-emitter gain cells with a full foundry model of an InP DHBT as active device. Based on observations from the analyses, we have presented design considerations that draw on the peculiarities of the multiplicative DA topology which may yield optimal results in noise, gain and bandwidth performance to match design requirements and specifications.

Acknowledgement

The support of the Petroleum Technology Development Fund (PTDF) of Nigeria through the sponsorship of T. Odedeyi's PhD program is acknowledged.

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