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ABSTRACT

Cosmic Infrared Background ExpeRiment-2 (CIBER-2) is an international project to make a rocket-borne measurement of the Cosmic Infrared Background (CIB) using three HAWAII-2RG image sensors. Since the rocket telemetry is unable to downlink all the image data in real time, we adopt an onboard data storage board for each sensor electronics. In this presentation, the development of the data storage board and the Ground Station Electronics (GSE) system for CIBER2 are described. We have fabricated, integrated, and tested all systems and confirmed that all work as expected, and are ready for flight.

Keywords: CIBER-2, Cosmic infrared background, Sounding rocket experiment, Ground station electronics

1. INTRODUCTION

The infrared background radiation is believed to originate from astrophysical sources at various distances: from nearby sources such as galaxies in the local universe to energetic sources in the early universe. We observe that the extragalactic infrared background is larger than expected from local galaxies ($z = 1 \sim 3$), suggesting that a new class of high mass stars or mini-quasars may dominate star formation in early universe.[1] The Cosmic Infrared Background ExpeRiment (CIBER) was a rocket-borne instrument designed to study the cosmic near-infrared extragalactic background to understand the primordial galaxy formation. It consisted of two wide-field near-infrared imagers to observe the spatial fluctuations in the background where the first light galaxy signature is expected to peak, a low-resolution spectrometer and a high resolution narrow band imaging spectrometer.

Cosmic Infrared Background ExpeRiment-2 (CIBER-2)[2] is the next international project to make a rocket-borne measurement of the Cosmic Infrared Background (CIB) as a collaboration of the institutes in the U.S.A., Korea, Japan, and Taiwan. To better understand the origin of the extragalactic background light, CIBER-2 will observe the spatial fluctuations with the bigger telescope, and higher sensitivity detectors working over a wider

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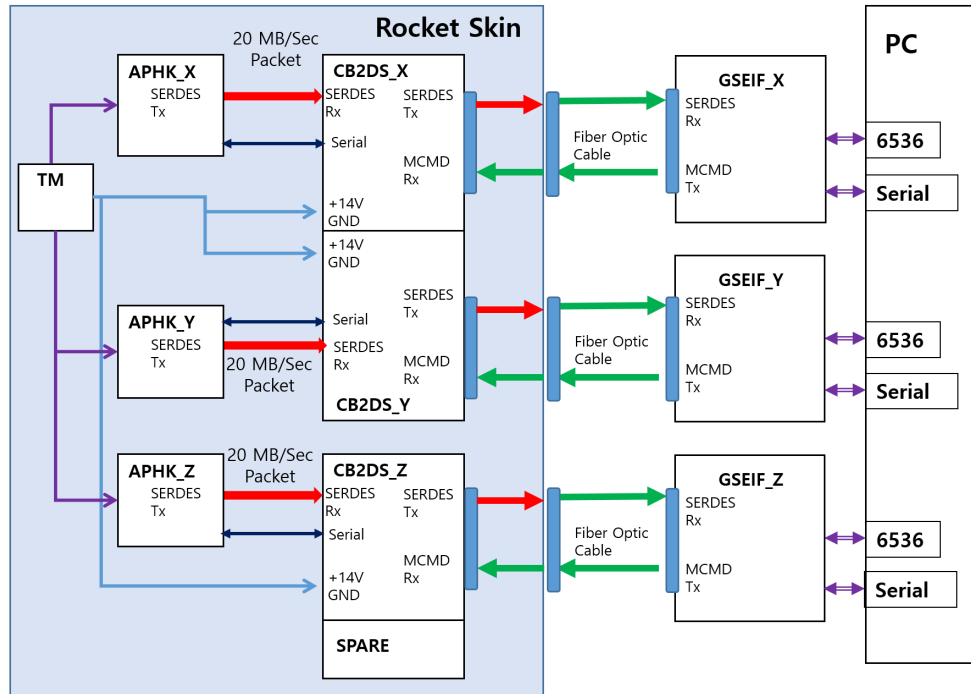Won-Kee Park: E-mail: wkpark@kasi.re.kr, Telephone: +82 42 865 3397

Figure 1. Block diagram describing the CIBER-2 electronics configuration. Three chains of APHK board, CB2DS board, and GSEIF boards exist for each CIBER-2 H2RG sensors. APHK board drives a H2RG sensor and sends out raw data to CB2DS board, the CIBER-2 data storage board. CB2DS board stores the data during the flight. APHK board and the data storage boards are going to be onboard the sounding rocket. In the laboratory, GSE interface board is connected to data storage board to read the data out.

wavelength range. CIBER-2 uses three $2k \times 2k$ HAWAII-2RG HgCdTe sensors from Teledyne,[3] to obtain the wide-field (2.3 square degrees) imaging data for six broadband wavelength bands. Since the rocket telemetry is unable to downlink all image data in real time, we adopt an onboard data storage system for each sensor in the CIBER-2 readout system. Dual SLC NAND flash memory is used as the storage medium in the onboard data storage system. The Ground Station Electronics (GSE) was designed to control the data storage system, and to acquire the large amount imaging data with high speed. A graphical user interface software was written to accompany the hardware.

In this paper, we describe the CIBER-2 data storage and the GSE systems. Section 2 describes the CIBER-2 data storage board, and the GSE hardware and the software in detail. The test performance of the both systems and the result of Total Ionizing Dose test of the data storage board are presented in Section 3. We summarize our results in Section 4.

2. DESCRIPTION OF THE SYSTEM

2.1 CIBER-2 GSE System Hardware

The electronics for CIBER-2 consists of three identical channels for data acquisition from the three HAWAII-2RG imaging sensors. The block diagram showing the configuration of CIBER-2 electronics is given in Figure 1. The APHK board drives the H2RG sensors to obtain observational data during the flight, and sends the raw data packets through a SERDES interface to CIBER-2 data storage board which is shown as CB2DS in the figure. This part of the system will be onboard the sounding rocket. On the ground, three GSE interface cards are connected to each data storage board via optical fiber cable, either to send commands to onboard electronics, or to read out the observational data from the CIBER-2 data storage board.

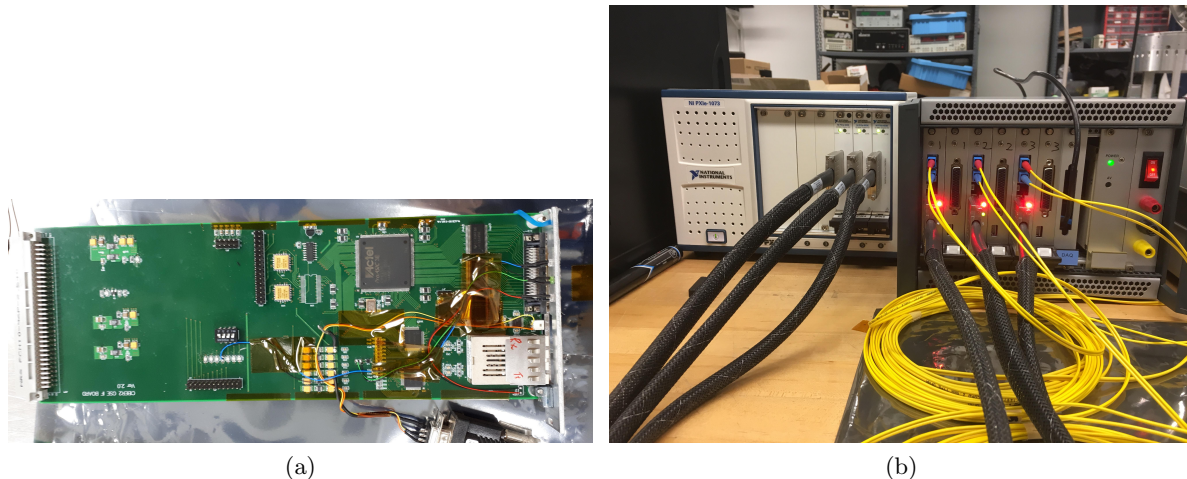(a)   (b)

Figure 2. The CIBER-2 GSE system: (a) CIBER-2 GSE interface board. Note the photo shows additional wires to connect the LED indicators in front panel for chassis, which does not affect the operation in any way. (b) PXIe-1078 chassis (White box) containing three PXIe-6536 cards, and VME chassis with three GSE interface cards.

The CIBER-2 data storage board is equipped with two Microsemi A3PE3000L FPGA chips, four 256 giga bit Single-Level Cell (SLC) NAND flash memory chips, and two optical fiber interfaces to send data to the control PC. The SLC NAND flash memory chip used in the data storage board, consists of 8384 blocks, and each block has 256 pages in it. Each page in a block can store 17,600 byte data. CIBER-2 operation requires that flash memory page write time is less than $350\mu s$, which can be met only by a SLC type flash memory. Two identical circuits are designed on a single PCB board to support two CIBER-2 H2RG sensors. The FPGA on the data storage board controls the data packet flow according to commands from the user such that either raw data from APHK board are stored on the onboard flash memory, or sent directly through optical fiber interface to the control PC in real time. Direct readout mode is used in the laboratory for the various system tests. During the flight, observational data are stored in the flash memory chips since rocket telemetry cannot downlink all the data in real time. The CIBER-2 flight operations are programed before launch. The data storage board is set to data ready mode just before launch by the user, and will store all data coming from APHK board during the flight. Two flash memory chips are installed for a single H2RG image sensor. The two flash memory chips are identical both in size and I/O speed. The same data are stored to both flash memory chips for redundancy. CIBER-2 data storage board can store up to 32 giga byte data per image sensor. The stored data can be retrieved in the laboratory through the GSE interface card.

The GSE interface board, shown in Figure 2a, is hardware that interfaces between the CIBER-2 data storage and the control PC. The GSE interface board is connected to data storage board via optical fiber cable, enabling a long distance separation between rocket-borne electronics and laboratory electronics system. Three GSE interface boards are required for three CIBER-2 H2RG channels. The board shape is of VME form factor, so that three cards can be installed together in a J1 backplane-equipped VME chassis. The GSE interface board consists of a FPGA, a Microsemi A3PE1500, an optical fiber interface to send command or to receive data from CIBER-2 data storage board, a parallel interface to send data to host PC, and a serial interface to transfer the commands and status information with the control PC. The FPGA assembles the received serial CIBER-2 data packet into 32 bit wide parallel format, and sends it to the control PC. A PXIe-6536 digital DAQ system from National Instruments is used for the data acquisition from GSE interface card. Figure 2b shows the PXIe-1078 chassis with PXIe-6536 cards, along with VME chassis containing three GSE interface cards. The burst handshaking mode of the PXIe-6536 enabled us to send data with 26.4 mega bytes per second speed per CIBER-2 channel.

Table 1 shows the format of the CIBER-2 data packet generated by the CIBER-2 APHK board. A data packet starts with three byte header, and ends with three byte footer. Between the header and footer, 99 bytes

Table 1. CIBER-2 data packet format

Word number	SERDES data source	Description
1	SYNC1	Packet start header
$2 \sim 4$	DAS_B1_U1	Four 18 bit pixel data
$5 \sim 7$	DAS_B1_U2	Four 18 bit pixel data
$8 \sim 10$	DAS_B1_U3	Four 18 bit pixel data
$11 \sim 13$	DAS_B1_U4	Four 18 bit pixel data
$14 \sim 16$	DAS_B1_U5	Four 18 bit pixel data
$17 \sim 19$	DAS_B2_U1	Four 18 bit pixel data
$20 \sim 22$	DAS_B2_U2	Four 18 bit pixel data
$23 \sim 25$	DAS_B2_U3	Four 18 bit pixel data
$26 \sim 28$	DAS_B2_U4	Four 18 bit pixel data
$29 \sim 31$	DAS_B2_U5	Four 18 bit pixel data
32	HKP	Housekeeping data
$33 \sim 34$	SCAN1, SCAN0	Frame scan data, flag information
35	SYNC2	Packet end footer

[1] One word is three bytes. A CIBER-2 packet is 105 bytes long.

are allocated for H2RG pixel data, housekeeping data, scan data and flag information, making a CIBER-2 data packet 105 bytes long. CIBER-2 sensor electronics produces 18 bit long pixel values. 90 bytes after the packet start header are used for data of 40 pixels including 32 image pixels and 8 reference pixels. Housekeeping data occupies next three bytes. The remaining six bytes before the packet end footer are for scan data such as the column and row numbers in the H2RG sensor, and flag information. 131,072 data packets are needed to complete a $2k \times 2k$ H2RG frame. Error Correction Code (ECC) algorithms are utilized to correct the bit error in a packet caused by the NAND flash memory. Hamming code based ECC[4] are calculated to correct single bit error. The FPGA on the data storage board calculates the 22 bit long ECC for every 105 byte long CIBER-2 data packet and adds it at the end of the packet when the FPGA writes the data to the flash memory.

2.2 GSE User Software

A Graphic User Interface software was designed to control the CIBER-2 GSE system hardware. The program is developed in LabWindows/CVI IDE from National Instruments. LabWindows/CVI IDE offers a good integration with NI PXIe-6536, the DAQ device in CIBER-2 GSE, since both products are made by same company. The C language environment enables it to integrate existing astronomical libraries and other heritage libraries into the program with minimal modifications.

The GUI of the GSE control program consists of three panels: GSE Display, GSE controls, and Log panels. The GSE Display panel has three canvases to show the raw image data obtained from three CIBER-2 H2RG image sensors. It also displays the image pixel statistics such as the mean and standard deviations of a single image. Each canvas displays the images as soon as they are extracted from the raw data independently from other two canvases. The GSE controls panel is equipped with all device control and monitoring. The user first selects which channel to operate, then establishes the serial connection to the selected GSE interface boards, and selects the command from the menu and sends them to the data storage board. The commands for CIBER-2 data storage board are listed in Table 2. Finally, the Log panel displays all log messages generated by the system, so that the user can easily track a problem when it occurs.

To read out the data from three channels simultaneously, GSE program adopts a multi-threaded scheme. Main thread runs the GUI, while three other threads run the data acquisition processes to acquire data from
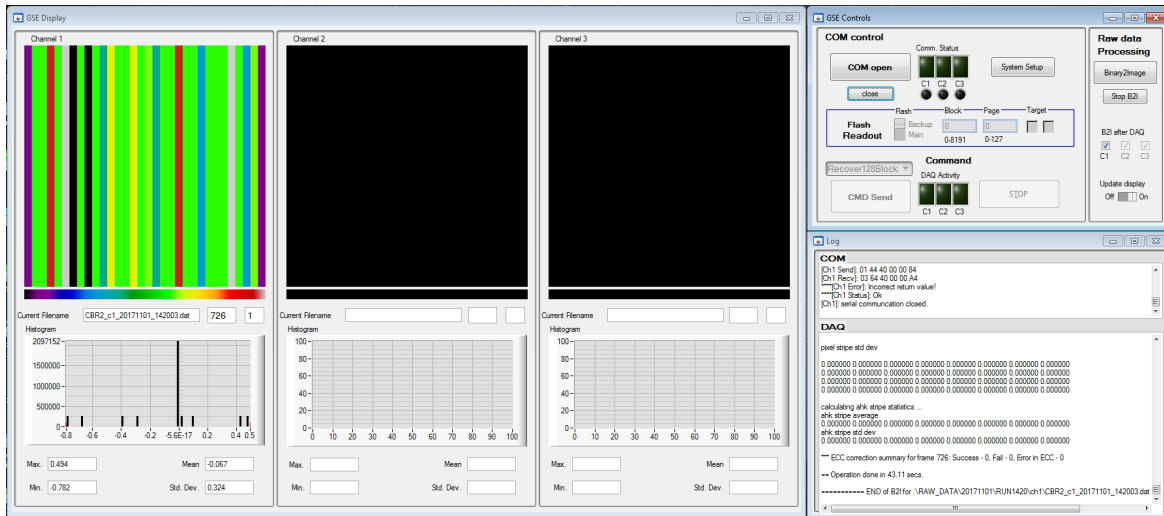
Figure 3. The GUI panels of CIBER-2 GSE control software. The left panel displays the raw image data from three CIBER-2 H2RG sensors. The GSE control panel is shown in the upper right, where various menus and buttons are located to control the CIBER-2 GSE system. The lower right panel displays all log messages generated by the system.

three CIBER-2 data storage boards. Upon completing the data acquisition, image data and status information extraction procedure starts under different thread. Thus, data acquisition in a given channel can continue while image data extraction runs in a different thread. The extracted image data are stored in FITS format and each FITS file is displayed in the GUI panel for quick data checks.

GSE software can correct the bit errors in the CIBER-2 data packet with ECC when it extracts the image data from the raw data file. The error correction procedure is implemented as in Ref 4. The GSE software first determines if there is an ECC in a data packet, and if an ECC is found at the end of the raw data packet, GSE software calculates the ECC again with the retrieved raw data packet. It then performs XOR operation to compare the calculated ECC with the one sent from the data storage board in the raw data. When the operation result indicates there is single bit error, the GSE software corrects the error in the packet before adding it to the output FITS file.

Table 2. CIBER-2 GSE system command list.

Command	Description
Flight	Start writing H2RG data to flash memory
RecoverAll	Read all data from flash storage
Recover128Block	Read 128 block data from flash storage
LabTest1	Read data directly from H2RG sensor, without writing to flash memory
LabTest1+write	Read data directly from H2RG sensor, with writing to flash memory
EraseAll	Erase all data from main/backup flash
Stop	Immediate stop of read/write actions
readStatus	Current status of actions

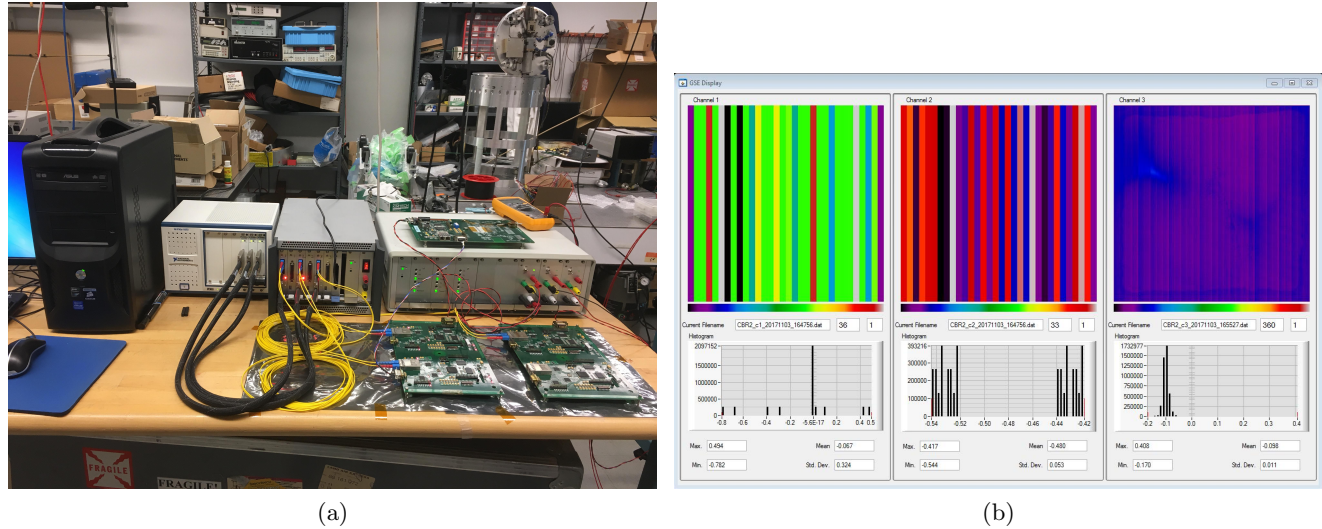|	
(a)	(b)

Figure 4. (a) The CIBER-2 data storage board and the GSE system assembled in the laboratory. From the left, control PC, NI PXIe-1073 chassis with three NI PXIe-6536 DAQ cards, VME chassis containing three GSE interface cards, and power supply unit for data storage board. Two CIBER-2 data storage boards are laid on the desk in front of the power supply unit. The data storage board and GSE interface board are connected with yellow optical fiber cables. (b) Screenshot of the GSE control software showing a result after a raw data acquisition. The left and middle panels show the test pattern generated by the simulator, and the right panel shows the NIR LED image taken by a H2RG sensor in a cryogenic chamber.

3. TEST OF THE SYSTEM

3.1 Lab Operation Test

The CIBER-2 data storage flight boards and GSE interface boards were made by Korea Astronomy and Space Science Institute (KASI) in 2017. The fabricated boards were all assembled and tested at the lab at the California Institute of Technology, U.S.A., on November 2017. Figure 4a shows two CIBER-2 data storage boards and their power system, and the CIBER-2 GSE system consisting of the GSE interface boards in the VME chassis, NI PXIe-6536 DAQ system, and the PC. We installed an adapter that has four USB-to-RS232c converters inside the VME chassis so that the control PC and three GSE interface cards are connected with a single USB cable.

With one H2RG sensor installed, a data writing test was carried out for the flash memory on the data storage board. SLC NAND flash memory chips successfully saved all CIBER-2 imaging data without any loss. It took about 45 minutes before the storage volume filled completely, which is long enough for CIBER-2 flight operations. Several 128 block data were randomly selected and retrieved from the flash memory, and these were consistent with completely successful data storage. The number of resultant image files differs by only one because the start point of a image frame is different in each raw data file. That the number of image files are same in most cases indicates that bit errors in the flash memory have little effect on the final data products.

The command communication and data acquisition test between the host PC and the data storage board was also carried out successfully. The result is shown in Figure 4b. However, whenever the user issued a command during the data transfer to the host PC, the data packet when the command was issued was corrupted as the command was transmitted in opposite direction to the data through the same optical fiber cable. For example, the last data packet in the raw data stream would be corrupted if a user stopped the data transfer by issuing a stop command. Therefore, it is not recommended to issue a command during the data transfer, unless it is acceptable to have a partial transfer.

The data correction test with ECC information was tested on several raw data files. The test indicated that the GSE software successfully corrected every single bit error in the data packet. However, it was found that there are often more than two bit errors in a 105 byte long CIBER-2 packet. These multiple bit errors caused
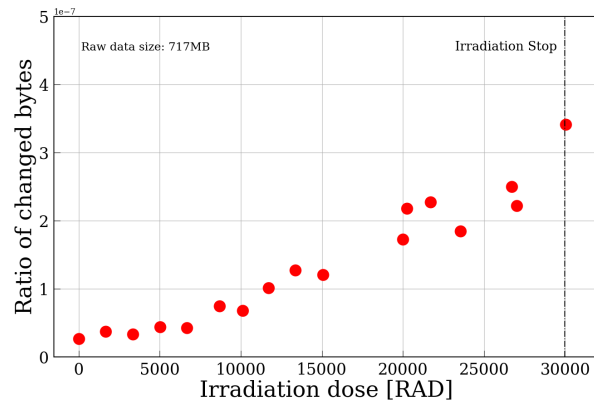
Figure 5. The fraction of incorrect bytes in a 717MB raw data file against gamma irradiation dose.

the software to incorrectly repair the packet so that fewer image data were successfully extracted from the raw data than when ECC correction was not applied. Because of this result, data correction with ECC has been disabled in the software until an improved algorithm is devised to correct multiple bit errors.

3.2 Total Ionizing Dose Test

The CIBER-2 data storage board uses a SLC NAND flash memory chip as its storage, which is not certified for operation in space environment, in addition to the commercial grade FPGA chip on the board. To validate our system, we carried out a Total Ionizing Dose (TID) test on the CIBER-2 data storage board. The TID test was carried out on August 2017 at Advanced Radiation Technology Institute, Jeongeup, Korea. A CIBER-2 data storage board loaded with a lab test image data was placed inside a radiation chamber, and it was irradiated with gamma radiation from a Cobalt-60 source at 10k rad/hour. The same 128 block of data in the SLC NAND flash memory was repeatedly retrieved every hour, that is, after each 10k of rad radiation was accumulated. The data storage board stopped working after the accumulated dose reached 30k rad. We examined if the raw data were affected by the radiation. Every byte of each readout data was compared with those in the raw data which had read out before the irradiation. The ratios of changed bytes over whole bytes of a file are plotted against the dose in Figure 5. Though the number of changed bytes is very small, it increases more than ten fold during the irradiation. For example, 19 bytes out of 717MB size were incorrect just after the irradiation began, increasing to 257 after the accumulated dose reached 30k rad. It should be noted these are very small numbers compared to the whole raw data size: the error ratio is lower than 4×10^{-7} for our irradiation test dose at 30k rad is seen in the number of changed bytes against irradiation dose, which is more or less linear from about 5k rad up to 30k rad. A weaker increasing relation is seen in the dose range less than 5k rad, which does not look to be due to a gamma radiation effect but rather due to property of the SLC NAND memory. Ref 5 reported that first single error appeared at 20k – 30k rad level in their TID test for 8G bit NAND flash chip. Our test indicats that single errors appear at a much lower level of around 5k rad, which is likely to be due to the higher flash memory cell density. Based on this test result, we conclude that the CIBER-2 data storage board works up to 30k rad dose. The bit errors in the flash memory increase according to the dose, but the overall error rate is not significant. We conclude that the data storage board can be used for our CIBER-2 rocket experiment.

4. CONCLUSION

CIBER-2 is a rocket-borne instrument designed to observe the near infrared background light. It uses three HAWAII-2RG imaging sensors for its wide-field cameras. We have fabricated the data storage and the Ground Station Electronics system for the CIBER-2. The CIBER-2 data storage board is a part of the rocket-borne electronics that stores the observational data during the flight. SLC NAND flash memory is used as its storage medium. The data storage board can save up to 32GB data per image sensor for about 45 minutes after the

system starts recording. The TID test on the storage board confirmed that the data storage board works up to accumulated dose level of 30k rad. The number of changed bytes increased approximately linearly above a dose of 5k rad. ECC algorithm can be used to correct single bit errors in the raw data, but multiple bit errors in the raw data result in erroneous error correction.

Ground Station Electronics (GSE) hardware and software are designed to control the rocket-borne instruments in the laboratory. The GSE system operates three high speed data acquisition boards to read data from three data storage systems, and serial communication ports to exchange command/status information with the individual data storage systems. The GSE software runs under multi-thread environment to acquire and process the data from three channels simultaneously. The CIBER-2 data storage board and GSE systems are ready for the launch of the CIBER-2 system.

REFERENCES

[1] Bock, J., Battle, J., Cooray, A., Kawada, M., Keating, B., Lange, A., Lee, D.-H., Matsumoto, T., Matsuura, S., Pak, S., Renbarger, T., Sullivan, I., Tsumura, K., Wada, T., and Watabe, T., "The cosmic infrared background experiment," *New Astronomy Review* **50**, 215–220 (Mar. 2006).

[2] Shirahata, M., Arai, T., Battle, J., Bock, J., Cooray, A., Enokuchi, A., Hristov, V., Kanai, Y., Kim, M. G., Korngut, P., Lanz, A., Lee, D.-H., Mason, P., Matsumoto, T., Matsuura, S., Morford, T., Ohnishi, Y., Park, W.-K., Sano, K., Takeyama, N., Tsumura, K., Wada, T., Wang, S.-Y., and Zemcov, M., "The cosmic infrared background experiment-2 (CIBER-2) for studying the near-infrared extragalactic background light," in [*Space Telescopes and Instrumentation 2016: Optical, Infrared, and Millimeter Wave*], *Proc. SPIE* **9904**, 99044J (July 2016).

[3] Beletic, J. W., Blank, R., Gulbransen, D., Lee, D., Loose, M., Piquette, E. C., Sprafke, T., Tennant, W. E., Zandian, M., and Zino, J., "Teledyne Imaging Sensors: infrared imaging technologies for astronomy and civil space," in [*High Energy, Optical, and Infrared Detectors for Astronomy III*], *Proc. SPIE* **7021**, 70210H (July 2008).

[4] Micron Technology, I., "TN-29-36: Error Correction Code (ECC) in Micron Single-Level Cell (SLC) NAND." Micron Technology Technical Note TN-29-63 https://www.micron.com/~/media/documents/products/technical-note/nand-flash/tn2963_ecc_in_slc_nand.pdf (2011). (Micron Technical Note TN-29-63).

[5] Schmidt, H., Gruermann, K., Nickson, B., Gliem, F., and Harboe-Sørensen, R., "TID Test of an 8-Gbit NAND Flash memory," in [*IEEE Transactions on Nuclear Science*], **56**, 1937–1940, IEEE (Aug. 2009).