Experimental Validation of a Thirteen Level H-Bridge Photovoltaic Inverter Configuration

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***Abstract*— Highly efficient and compact multilevel inverters are desirable in many applications such as wind farms, solar energy harvesting and electric vehicles. The authors present a single-phase thirteen level inverter control method employing semiconductor power devices for photovoltaic applications. The unique configuration of source inverters with multilevel voltage capabilities enables large voltages together with minimal harmonic distortion without the employment of associated harmonized switching devices or transformers. A multilevel inverter is commonly used to create a desired voltage from several dc voltage levels. Therefore multilevel inverters can satisfy the large electric power requirements for high power devices. The proposed inverter system based on a simple H-bridge inverter structure provides accurate voltage control and excellent efficiency. The proposed inverter is demonstrated using MATLAB/SIMULINK simulation software and experimental validation is executed using high-efficiency ARM controller.**

Keywords; PV system, multi-level inverter. H-Bridge inverter, total harmonic distortion.

I. INTRODUCTION

Multilevel voltage inverters possess useful intrinsic features such as reduced voltage stress upon switches, low electromagnetic interference, fewer output filters and improved harmonic profile outputs. These features mean that they could be a practical alternative to conventional inverters for high power applications [1]. The main advantage of multilevel (MLI) design is in the reduction of harmonic distortion without the need of increasing the switching frequency. The MLI output voltage waveform is a representation of the number of voltage levels, typically obtained from series of capacitor voltage sources that are obtained from one main source such as a photovoltaic (PV) system. The output total harmonic distortion (THD) approaches zero when the number of output levels reaches infinity. The number of the realizable output voltage levels however, is limited by voltage stability problems, circuit design (switches driving), and voltage clamping obligations.
In general, four general MLI topologies have been studied and presented. Those being the neutral-point-clamped structure [2], cascaded inverters [3], neutral-point-clamped inverter structures [4] and flying capacitor inverters [5].
In this paper, we present a practically realised multilevel inverter structure which can reduce the general operating cost of a system by employing a reduced number of power switches, drivers and voltage sources. The proposed structure comprises one PV voltage source, six series connected capacitors utilized as particular voltage source energy-sharing elements and nine power switches to create thirteen output voltage level.

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II. PHOTOVOLTAIC SYSTEMS

PV schemes are used to directly alter sunlight into electricity. Such systems comprise different elements such as the cells (connected in parallels or series), cell electrical connections, and the converters to convert/invert the electrical DC output. Energy then produced from such schemes can (a) be stored for local use, or (b), supply energy to the national grid.

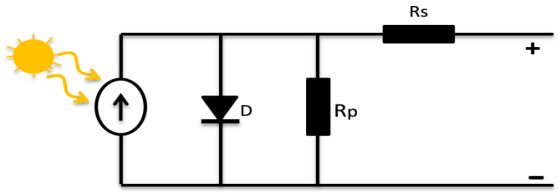

Figure 1. Equivalent Circuit of a PV cell.

An equivalent PV cell circuit is shown Figure 1 above. The series (Rs) and parallel resistance (Rp) represent the active portion resistance and the equivalent parallel resistance of the PV cell respectively. Series/parallel (Rs/Rp) resistance values can be calculated using the PV cell output current (1).

$$I = I_{ph} - I_o\left(\frac{q(V+IR_S)}{nkT} - 1\right) - \frac{V+IR_S}{R_p} \qquad (1)$$

Where:

- I = PV Cell current
- I_o = Diode saturation current
- q = Electron charge ($1.6\text{x}10^{-19}$ C)
- k = Boltzmann constant ($1.38\text{x}10^{-23}$J/K)
- n = Ideality factor
- T = Temperature (ºK)

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- I_{ph} = Photon Current (A)

A more realistic and accurate PV cell current-voltage (IV) characteristic is shown in figure 2. This graph shows the maximum power point (MPP) region, short circuit current (Isc) and open circuit voltage (Voc) points. MPP is the point where the cell can produce maximum power from the light hitting it. The pivotal elements provided via the PV model are:

- Voc, Vmpp = Maximum and optimum voltages respectively.
- Isc, Impp = Maximum and optimum currents respectively.

Fig. 2. I-V Characteristic of a typical photovoltaic cell

III. PROPOSED METHOD

The major drawbacks associated with the MLI configurations are their circuit difficulty and complexity, demanding a large number of power switches [6]. Utilizing a basic H-Bridge multilevel inverter means that the number of power devices required decreases and with that so does circuit difficulty [7]. Implementing a reduction in device numbers etc. means circuit loss disadvantages such as that observed in switching power also diminish. The structure presented here comprises a simple H-Bridge inverter with additional bidirectional switches (auxiliary switches). The proposed multilevel H-bridge inverter diminishes the required switch numbers and employs a simple switch driving system. The proposed single-phase, simplified thirteen-level power inverter circuit with auxiliary switches is shown in Figure 3.

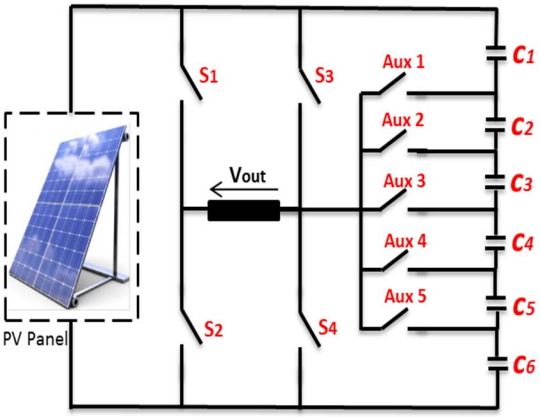

Fig. 3. Proposed simplified 13-level inverter schematic

B. Proposed Structure Advantages

1) Useful for large voltage and current applications.
2) Smaller output filter size due to improved THD.
3) Low number of switches employed.
4) Comprises an orthodox H-bridge inverter, two-way secondary switches and a passive capacitor voltage divider created via standard components.
5) Because switching occurs at low frequencies (650 Hz), the circuit has a very high efficiency.
6) Reduced electromagnetic interference (EMI) and total harmonic distortion (THD).
7) Minimized circuit complexity even as levels increase.

IV. OPERATING MODES OF PROPOSED INVERTER

The experimentally validated inverter produces thirteen separate voltage levels *at (Vpv, Vpv/6, 2Vpv/6, 3Vpv/6, 4Vpv/6, 5Vpv/6, 0Vpv and –Vpv, -Vpv/6 -2Vpv/6, -3Vpv/6, -4Vpv/6 and -5Vpv/6)* from the PV source which has been divided into six voltage sources by means of the series of capacitors C1 to C6. The simulated 13 level output voltages of the proposed inverter shown in figure 4 below.

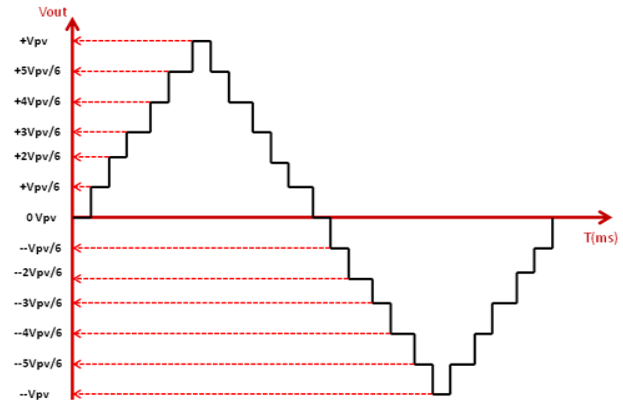

Fig. 4. Modelled 13-level inverter output voltage waveform

The operation of the proposed 13-level inverter structure can be divided into thirteen positive and negative modes of operation. The following nomenclature is used to describe the operation: For reference, switches are named S_n, Capacitors C_n, bidirectional switches are AUX_n, where n = 1,2, etc.

A. MODE 1(0 Vpv)

In this case S4 is closed, creating a connection between the positive load terminal and Vpv. S2 is closed, linking the negative load terminal to ground. C1-C6 are charging. S1, S3, AUX1, AUX2, AUX3, AUX4, and AUX5 are all open giving a 0Vpv output voltage.

B. MODE 2(+Vpv/6)

AUX5 is now closed; linking the positive load terminal to Vpv. S2 is also closed, joining the negative load terminal to ground. C1-C5 are now charging. S1, S3, AUX1, AUX2, AUX3, AUX4, and S4 are now open giving an output voltage of Vpv/6.

C. MODE 3(+2Vpv/6)

AUX4 is closed, making the positive load terminal Vpv. S2 is closed, making the negative load terminal ground. C1 - C4 are now being charged. S1, S3, AUX1, AUX2, AUX3, AUX5, and S4 are opened; the output voltage is 2Vpv/6.

D. MODE 4(+3Vpv/6)

In this case AUX3 is closed; making the positive load Vpv. S2 is closed, joining the negative terminal to ground. Now C1 - C3 are being charged. S1, S3, AUX1, AUX2, AUX4, AUX5, and S4 are all open giving a 3Vpv/6 output voltage.

E. MODE 5(4Vpv/6)

AUX2 is closed, making the positive terminal Vpv, and S2 is closed, grounding the negative terminal. C1 and C2 are charging. S1, S3, AUX1, AUX3, AUX4, AUX5, and S4 are now open; the output voltage is 4Vpv/6.

G.MODE 6(5Vpv/6)

AUX1 is closed, making the positive terminal Vpv, S2 is closed, grounding the negative terminal. C1 is charging. S1, S3, AUX2 - AUX5 and S4 are all open; the output voltage is 5Vpv/6.

H.MODE 7(+Vpv)

S3 is closed, making the positive terminal Vpv, S2 is closed, making the negative terminal ground. S1, AUX1-AUX5 and S4 are now open; the output voltage is Vpv.

I.MODE 8(-Vpv/6)

S1 is closed, giving Vpv at the positive terminal, and AUX1 is closed, grounding the negative load terminal. C2 - C6 are now being charged. S3, AUX2 - AUX5, S4 and S2 are open; the output voltage is -Vpv/6.

J.MODE 9(-2Vpv/6)

S1 is closed, making the positive load terminal Vpv, AUX2 is closed, grounding the negative load terminal. C3 - C6 are charging. S3, AUX1, AUX3, AUX4, AUX5, S4 and S2 are all opened; the output voltage is -2Vpv/6.

K.MODE 10(-3Vpv/6)

S1 is closed, providing Vpv at the positive load terminal, AUX3 is closed, grounding the negative load terminal. C4 - C6 are charging. S3, AUX1, AUX2, AUX4, AUX5, S4 and S2 are opened; the output voltage is -3Vpv/6.

L.MODE 11(-4Vpv/6)

S1 is closed, making the positive load terminal Vpv, AUX4 is closed, grounding the negative load terminal. C5 and C6 are now charging. S3, AUX1, AUX2, AUX3, AUX5, S4 and S2 are open providing -4Vpv/6 output voltage.

N. MODE 12(-5VDC/6)

S1 is closed, making the positive load terminal Vpv, AUX5 is closed, grounding the negative load terminal. Now C6 is being charged. S3, AUX1 - AUX4, S4 and S2 are all open; the output voltage is -5Vpv/6.

O.MODE 13(-Vpv)

S1 is closed, connecting the load positive terminal to Vpv, S4 is also closed, grounding the negative load terminal. S3, AUX1 - AUX5 and S2 are all open; the output voltage is -Vpv.

All output voltage modes are summarised in table 1 below.

TABLE 1: 13-LEVEL OUTPUT SWITCHING MODES

Levels	Vout	Mosfet switch designation								
		S1	S3	AUX1	AUX2	AUX3	AUX4	AUX5	S4	S2
Level 01	Vpv	1	0	0	0	0	0	0	1	0
Level 02	5Vpv/6	1	0	0	0	0	0	1	0	0
Level 03	4Vpv/6	1	0	0	0	0	1	0	0	0
Level 04	3Vpv/6	1	0	0	0	1	0	0	0	0
Level 05	2Vpv/6	1	0	0	1	0	0	0	0	0
Level 06	Vpv/6	1	0	1	0	0	0	0	0	0
Level 07	0 Vpv	0	0	0	0	0	0	0	0	0
Level 08	-Vpv/6	0	0	0	0	0	0	1	0	1
Level 09	-2Vpv/6	0	0	0	0	0	1	0	0	1
Level 10	-3Vpv/6	0	0	0	0	1	0	0	0	1
Level 11	-4Vpv/6	0	0	0	1	0	0	0	0	1
Level 12	-5Vpv/6	0	0	1	0	0	0	0	0	1
Level 13	-Vpv	0	1	0	0	0	0	0	0	1

V. MATLAB SIMULATION RESULTS

In order to evaluate the overall performance of the proposed technique, a simulation employing MATLAB/SIMULINK software was performed. During the simulation all of the semiconductor mosfet devices are assumed ideal. A resistive load (R) of 100 Ω is used and connected to the inverter output. Also, the magnitude of PV voltage source is adjusted to 300 V. The following criteria were agreed for the simulation;

a) PV Panel:

Voc is set at 400 V,

Vmpp is considered 300 V,

Isc is 14.25A,

Impp is 11.4 A.

b) Inverter capacitors:

DC capacitors Cl - C6 are all set to 10mF

The proposed assembly, established employing Matlab/Simulink Sim-Power-System library, comprises standard components such as mosfets and drivers and discrete elements, resistors and capacitors.

The thirteen level output voltage waveform is illustrated in Fig. 5. The maximum value of load current is approximately 2.2A. The MPPT settling time can be observed between 0 and 0.1s. The 13 levels can be clearly observed in Figure 6.

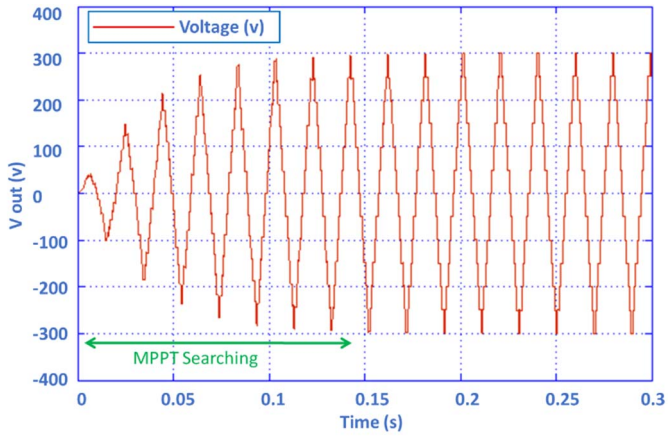

Fig. 5. Thirteen level output voltage waveform of proposed inverter structure

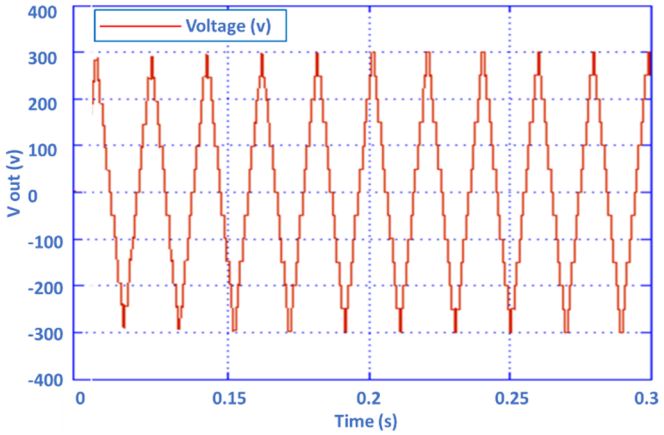

Fig. 6. Zoom for Thirteen level output voltage waveform of proposed inverter structure

VI. EXPERIMENTAL VALIDATION

Once simulation design and ensuing results proved satisfactory, a laboratory based experimental endorsement of the thirteen-level inverter was subsequently performed. The proposed inverter was constructed and contained nine power switches, four of them comprising the H-bridge inverter and the other five switches representing the auxiliary switches. This was configured such that one auxiliary switch required two MOSFETs with one photocoupler integrated circuit (TLP250) and two shielding capacitors.

The inverter consisted of three main sections; in the first section a high efficiency 180 MHz clock frequency microcontroller ARM-STM32F407 was employed. This controller included the embedded control program written in the C language based on Matlab software.

The second section encapsulates and provides the mains voltage isolation, using opto-isolation devices to separate the high and low voltage sections. This isolation section uses TLP250 drivers capable of performing two functions (Mosfet driving / isolation) on the same chip.

The third section comprises the power part. This consisted of nine power switches (Mosfets IRF840).

The experimental set-up along with associated components etc. is displayed in Figure 7 below. Two tests were carried out; the first without the use of an output filter and the second test with the inclusion of a low pass filter. Results for both are presented below.

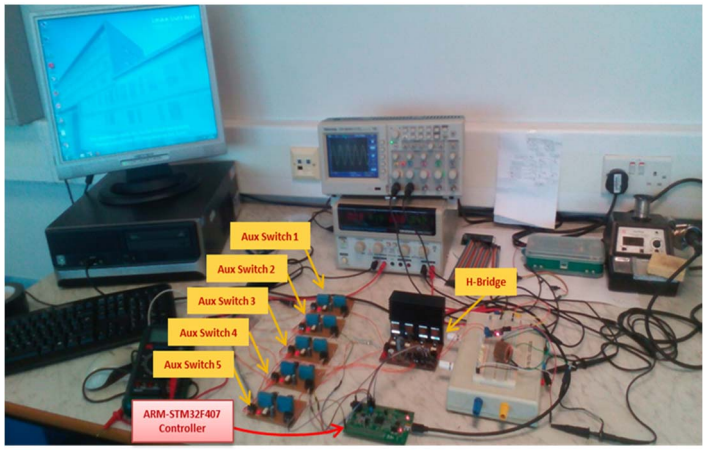

Fig. 7. Laboratory prototype for proposed inverter experimental validation.

The experimentally investigated inverter provided exceptional results with the thirteen output voltage and current levels clearly observable in figures 8a and 8b. The results here present the first experimental testing of such a device without any output filtering. The fast Fourier transform (FFT) of the experimental output voltage for the first test (without filter) is shown in figure 8-c and displays a 28dB variance between the fundamental and third harmonics at 150 Hz and 19dB ratio between the fundamental and fifth harmonics at 250 Hz.

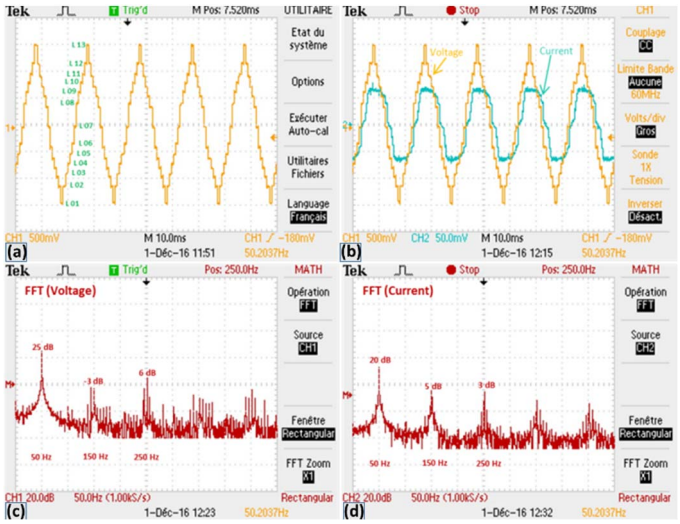

Fig. 8. Experimental results for 13-level inverter without output filter

The FFT analysis of the experimental output current in the same test is shown in figure 8-c and displays a 15dB difference between the fundamental and third harmonics at 150 Hz and 17dB difference between the fundamental and fifth harmonics at 250 Hz.

Subsequently further experimental testing took place with the inclusion of an output LCL low-pass filter. The output voltage and current level stages for this part of the experiment are presented in Figures 9a-b below respectively. Here the experimental FFT output voltage for the first test (using LCL filter) is shown in figure 9-c and displays a 21dB difference between the fundamental and third harmonics at 150 Hz and an 18dB difference between the fundamental and fifth harmonics at 250 Hz. The output current FFT analysis for the same test is displayed in figure 9-d. This shows a 12dB difference between the fundamental and third harmonics at 150 Hz and 19dB difference between the fundamental and fifth harmonics at 250 Hz.

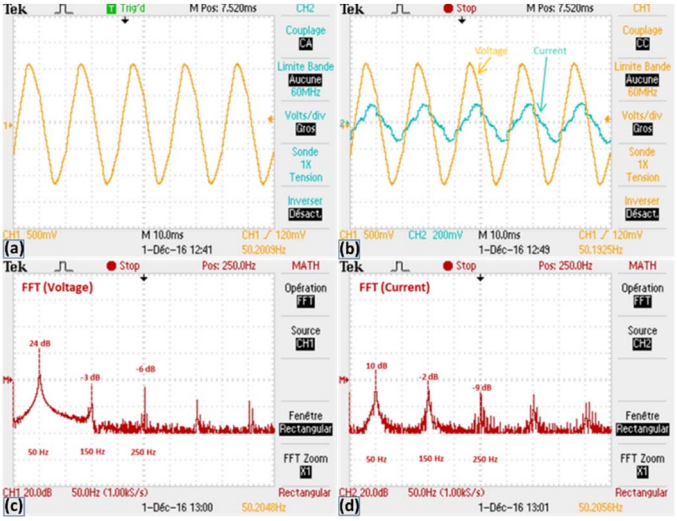

Fig. 9. Experimental results for 13-level inverter with inclusion of LCL low-pass filter

Negligible steady-state oscillations in the level transition stages were produced. Thus, the thirteen level inverter presented here is extremely feasible and displays the expected harmonic distortion reduction required for MLI applications in photovoltaic generation schemes.

VII. CONCLUSIONS

This work demonstrates the experimental validation of a innovative thirteen-level inverter for PV applications. These results show that by implementing a high efficiency control strategy this inverter design can effectively deliver a combination of low total harmonic distortion and high power efficacy without function stress. Further work is being performed on realistic implementation scenarios and field trials.

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