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THE APPLICATION OF MICROPROCESSORS

TO PULSE-WIDTH-MODULATED

INVERTERS

By

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In collaboration with Black Clawson International Limited.

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MEMORANDUM

MICROPROCESSOR CONTROL OF POWER INVERTERS

This thesis incorporates the results of a three year investigation into variable speed drives for induction motors with particular reference to the use of a microprocessor. The work was carried out in the laboratories of the Polytechnic of Wales from April 1979 to April 1982, under the supervision of Dr. M.G.Jayne and with the industrial collaboration of Black Clawson International of Newport, Gwent.

All work and ideas are original unless otherwise acknowledged in the text or by reference. This work has not been submitted for another degree of the C.N.A.A., nor for the award of a degree or diploma at any other institution. The main contribution that the author claims to have made to the subject of variable speed AC drives include :

1. The application of communication principles as the background philosophy to the modulation strategy for the generation of pulse width modulation (PWM) waveforms utilized in the realisation of variable speed a.c. drives.

2. The design and development of a mark II analogue rig suitable for generating several types of PWM waveforms which were then evaluated in terms of their practical performance in the speed control of a three phase induction motor.

3. The development of computer programs, written in Basic on the PET microcomputer for the purpose of :

   (i) Analyzing the frequency spectrum of the natural Sampled form of PWM generation using Bessel Functions;

   (ii) Analysing the frequency spectrum of the Regular Sampled Asymmetric form of PWM generation using a Fast Fourier Transform technique.

4. The design and development of a novel microprocessor system for the variable speed control of AC drives. Prior art techniques had not investigated this approach which offers several advantages :

   (i) A reduction in the amount of hardware required over other techniques;

   (ii) the use of an interrupt system and a specialised programmable peripheral chip so that :

        (a) Only a single microprocessor is required;

        (b) A control program routine can be added to the system without the need for a second processor;

        (c) No external computation of pulse widths, on a mainframe

(i)

computer, is required;

(d) Only 2 kilobytes of memory are required for the software;

(e) A far greater degree of flexibility is achieved in the control of the pulse number of the PWM waveform whereby its value can be freely selected and is not fixed by the setting of carrier and modulation frequencies as in the prior art analogue rig;

(f) New data, for controlling pulse number, speed and torque, can be entered into the system whilst the motor is being run, at speed, by the microprocessor so that smooth, incremental changes in motor speed can be achieved.

5. As a consequence of (4) a novel programmable interface unit has been designed which incorporates a software control technique for the starting and stopping of the programmable timer whilst the hardware configuration allows the reversal of motor rotation to be simply achieved.

6. Also, as a consequence of (4) a novel technique – the implementation of the formula describing the Regular Sampled Asymmetric form of PWM using numerical software – was utilised for generating three phase PWM waveforms. This necessitated the design of several software programs to provide 16 bit by 16 bit multiplication, 24 bit by 8 bit division, code conversion, scaling, a 16 bit sine routine using the co-ordic algorithm was particularly useful in that a complete range of sine values could be obtained allowing enough accuracy to distinguish 1° differences in the input data. This approach allowed a significant saving in memory size- 180 bytes of data, with the added memory requirement of a program to access the table of data would have been necessary in a table look-up approach.

7. The graphs comparing the measured frequency spectra of the analogue and digital techniques of PWM generation with the theoretical spectra as predicted by the FFT analysis show conclusively that :

(i) The microprocessor is, in fact, emulating the regular sampled asymmetric form of PWM modulation;

(ii) the microprocessor implementation is far more accurate than the analogue rig and was able to control a 5h.p. induction motor over a 100:1 speed range, the frequency varying from 1Hz to 100Hz whilst the frequency ratio varied from 21 to 3. The modulation index was selected to maintain a constant V/F ratio, although, at its extremities, a change in D.C. link voltage was necessary in order to generate the appropriate torque so that the proper operating speed could be achieved.

(ii)

The investigation has supported the publication of several articles :

Jayne,M.G.; Williams,A.B.; 'An Investigation Into the Operation of a Thyristor with Law Harmonic Control' pp464-467 Int.Conf. on Electronics and Microelectronics (EUROCON 80) Stuttgart, Germany, march 1980.

Jayne,M.G.; Williams,A.B.; "An Investigation Into the Application of Microprocessors. to Pulse-Width-Modulated Inverters" pp.11-51 to 11-63 Int.Conf. on Numerical Control of Electrical machines (CONUMEL 80) Ecole Control de Lyon, Lyon, France, April 1980.

Williams,A.B.; Jayne,M.G.; "A Software Approach to the generation of P.W.M. Waveforms for Variable Speed Induction Motor Drives" 17th Universities Power Engineering Conference U.M.I.S.T., April 1982.

LIST OF symbols

V	= amplitude of pulse
T	= (1) periodic time
	(2) pulse width value
N,K,n,m,r	= integers
A	= (1) amplitude of wave
	(2) variable
B	= (1) variable
	(2) arbitrary constant
C	= (1) capacitance
	(2) variable
E	= (1) direct supply voltage
	(2) variable
F	= (1) frequency
	(2) variable
G,G	= variables
K	= modulation index
L	= inductance
M	= magnitude of vector
Mi	= modulation index
R	= (1) frequency ratio
	(2) resistance
W	= exponential constant ($W = \exp(-2\pi j/n)$)
I	= current
X	= (1) X co-ordinate
	(2) variable
Y	= Y co-ordinate

J_n	= Bessel function of order n
e	= (1) exponential
	(2) instantaneous values of time function
f	= frequency
t	= time
k	= integer ratio
h	= height
b	= bit
v	= instantaneous voltage
t_O	= pulse width
w	= angular frequency
ϕ	= (1) phase designation
	(2) phase angle
	(3) vector angle
θ	= phase angle
α	= (1) gradient
	(2) vector angles
$\Delta_O(t)$	= function of time incorporating an infinite series of unity amplitude impulses, period T
$\Delta_\perp(t)$	= function of time incorporating infinite series of unity amplitude impulses, period To
$V(t),U(t),f(t),x(t),h(t)$	= functions of time
$\hat{h}(t)$	= sampled function of continuous function h(t)
$\hat{\hat{h}}(t)$	= time domain product of two sampled data functions
$\delta(t)$	= impulse function
$X(n),A(n),Xk,Yk,Zk,h(k)$	= sampled data time series
$\tilde{H}(n)$	= fourier transform
$f(x)$	= arbitary function of x

*	= convolution
⬡	= transformation between time and frequency domain, or vice versa
DFT	= discrete fourier transform
FFT	= fast fourier transform
PWM	= pulse width modulation
NS PWM	= natural sampled pulse width modulation
RSA PWM	= regular sampled asymmetric pulse width modulation
ROM	= read only memory
RAM	= random access memory
EPROM	= electrically programmable read only memory
TTL	= transistor transistor logic
CMOS	= complementary metal oxide silicon semiconductor
PTM	= programmable timer module
IRQ	= interrupt request control line of microprocessor
R/W	= read/write control line of microprocessor
DMA	= direct memory access line of microprocessor
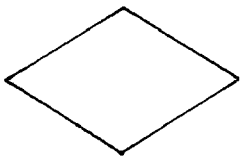
Decision
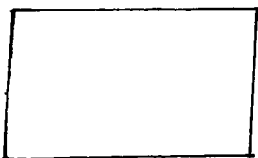
Process

◯   Connector

⬭   Terminal

Suffices

c   – pertaining to carrier wave

m   – pertaining to modulating wave

s   – pertaining to sampling

r   – pertaining to repetition wave

a   – pertaining to phase of 3-phase system

b   – pertaining to phase of 3-phase system

c   – pertaining to phase of 3-phase system

SUMMARY

The introduction gives consideration to the aspects of communication principles, power converters, PWM modulation techniques and the application of LSI intergrated circuits as regards their effect on the design of variable speed AC drives.

Chapter 1 includes background material where several types of variable speed A.C. drives are compared. The theoretical possibilities of various PWM schemes show that certain techniques offer improved harmonic spectrum properties, more suited to the wide range speed control of induction motors. Chapter 2 introduces alternative approaches to the analysis of sinuisoidal or natural PWM and the regular sampled PWM waveforms. The latter waveform is analysed by expressing the function in terms of the time domain; conversion from the time to the frequency domain is then obtained using a Fast Fourier Transform (FFT) technique implemented on the 32K PET microcomputer. Chapter 3 describes a successful analogue rig designed to generate several, alternative PWM waveforms which were used to drive an induction motor via the McMurray bridge inverter. Practical performances of the differing PWM waveforms were evaluated, using this equipment and the regular sampled, asymmetric PWM waveform was shown to have some operational advantages - it was this technique which was then given further consideration for microprocessor implementation.

Chapter 4 outlines the top-down, structured design philosophy necessary for the efficient successful realisation of the hardware and software of a microprocessor system. The detail of the complete unit

is given in Chapter 5 which describes the hardware and software of a microprocessor design used to provide the switching drive to the induction motor via the inverter. Several sotware algorithms are described which, when run by the control program in the appropriate sequence, produce the three phase PWM output waveform. An analysis of results is provided in Chapter 6 which shows that both the analogue and microprocessor rigs can operate an induction motor over wide speed ranges. The micropocessor realisation was far more accurate in its emulation of the Regular Sampled Asymmetric PWM waveform and controlled the motor over a 100:1 speed range.

The concluding chapter summarises the problems, state-of-art and further applications of the microprocessor implementation whose unique properties are hardly obtainable with other, more conventional forms of practical realisation.

INTRODUCTION

Communication Principles

One of the main requirements of a variable speed cage rotor induction motor drive system is that the magnitude and frequency of the voltage applied to the motor be independantly variable over a wide range. However, such a requirement is not easily met in practice. Generally mains power supplies are constant frequency constant voltage sources so that power transmission can be cost effective. Therefore, some method of achieving an efficient variable frequency, variable voltage supply from the static mains supply is required.

There are many techniques of power conversion where the aim is to provide a three-phase variable frequency, variable voltage source [1],[2]. For high power converters, where efficiency is at a premium the use of pulse modulated systems has found favour because the system can operate with efficiencies in excess of 90%. Further the technology of thyristors has advanced such that fast turn-off, high power devices are available at a low enough cost to ensure the economic viability of power inverters.

The availability of high power thyristors has accentuated the development of pulse modulated power transfer, a technique which has been used extensively in the communications field for the transmission of information signals.

The process of static frequency change is known as modulation. For example, amplitude modulation is a process which changes both the amplitude and frequency of a fixed frequency source. Information transmission and coding techniques cover frequency modulation (FM), amplitude modulation (AM), phase modulation (PM), double sideband modulation (DSM), pulse position modulation (PPM), pulse code modulation (PCM) and pulse amplitude modulation (PAM). All of these approaches can be applied to the problem of variable frequency power transmission from the A.C. supply to the induction motor; not all will be efficient and those techniques most suited to information transmissions will not, of necessity, be most efficient in application to power transfer.

The application of communication principles to variable-frequency, solid-state power converters has resulted in significant improvements in efficiency of power inversion through the implementation of pulse width modulation (PWM) as a means of frequency and voltage control [3]. PWM is a well-known principle of information communication [4] and the concept of a.c. power converters as modulators (since frequency changing can only be obtained by modulation) has influenced research activities in employing the premise that communication principles can be applied to modern power converters with some benefit [5].

Other practical examples of the application of communication principles to power converters are the use of amplitude modulation to achieve a 2:1 speed change [6], the stepped sine wave modulation principle [7], which achieves the elimination of sub harmonic problems (at non-integer frequency ratios) and the implementation of

mathematical analyses which allow a fundamental appreciation of the modulation principle involved [8]. Alternative analyses can also provide a clear insight into the frequency spectra of the modulation process when integer frequency ratios are adopted [9].

Waveform analysis is an important aspect of any investigation into PWM motor drives. The harmonics present in a PWM waveform can produce major problems - large eddycurrent losses, torque pulsations and sub-harmonic rotational torques [10]. A knowledge of the amplitude, phase and frequency of the harmonics is essential for effecting assessments of motor operation and system performance.

Power Conversion
———— ————————

The recent Bart experience [19] has cast great doubt on the suitability of the DC motor for industrial and transport use. Experience has shown that the DC machine is the weakest link of the drive system and that the brushes and commutators are responsible for maximum failure rates, which result in expensive equipment outages.

For many years the inherent simplicity, ruggedness, low cost and high torque/inertia ratio of the induction motor has been a crucial factor in determining its use for constant speed drives - about 80% of motor production is taken up by induction motors. For a similar period these same qualities have spurred research into variable speed induction motor drives. However, in many cases, the significant advantage of the isolated rotor, with no electrical connection, has been sacrificed in order to achieve the range of speed control.

Of the remaining techniques, such as the cycloconverter, speed limitations still exist [11] in the design of the unit (even though there have been some improvements) and a high cost penalty is incurred in operation in that 36 thyristors are required in order that low frequency 'cogging' effects can be avoided - different approaches [12],[13] incur other limitations in response time, complexity and economic viability whilst variable D.C. link, 6 step inverters [14] introduce cogging at low frequencies (below 5Hz) and require two power modulation stages. With PWM inverters, both voltage and frequency conversion are achieved in a single set of power modulators. Using McMurray bridge inverters only twelve thyristors are required, whilst six of these are needed for commutation only and do not operate at the high power levels of the load circuitry - in addition, the design of the McMurray bridge inverter is well documented.

Even with these limitations, there are still many areas which require investigation. Several different types of PWM could be generated and it is shown in the earlier chapters that regular sampled asymmetric PWM has definite practical advantages over the natural sampled form of PWM.

PWM Modulation Techniques

Using a mixer/multiplier in communications circuits has some similarity to the use of a comparator in power circuits. By changing the character of the two input signals to the mixer, differing processes of modulation can be obtained (that is AM and DSM). In the same way, very different forms of PWM can be obtained simply by changing the two modulating signals to the comparator.

- 4 -

A large number of PWM generation techniques have been proposed in the literature [15], [16] in an effort to produce an improved A.C. variable speed induction motor drive with lower losses, fewer pulsating torques and greater frequency stability. The PWM waveforms can appear to be similar, when studied in the time domain, but a frequency domain analysis immediately indicates major differences in their spectra.

Under normal operating conditions the induction motor has a sine-wave drive. If it is assumed that this is an optimum drive condition then the harmonic content of the PWM waveform can be seen to be an important parameter in determing operational performance. Further, the amplitude, frequency (or frequency ratio) and phase of the harmonics will set the resultant pulsating torques, their level, direction and stability.

In an effort to reduce the harmonic content multi-voltage-level PWM waveforms [17] have been proposed for use in motor drives. However, practical constraints generally limit engineered systems to the use of two-level waveforms, although, three-level waveforms are occasionally utilized. When using two level PWM drives it is important to have a three-wire connection to the three-phase motor since a four-wire system, which would include a neutral return, would radically alter the characteristics of the drive. Carrier harmonics, present in the PWM signal, would be provided with a return path, hence current flow is obtained at all frequencies. In the three-wire system, in the absence of a neutral connection, harmonic current flow only occurs when there is an amplitude and/or phase difference between the harmonics in the three phase PWM waveforms. It is to be noted

that triple harmonics can actually be cancelled in this technique [18], when using triple integer frequency ratios. It is the two-level PWM waveform which is considered for further research.

Application of LSI Integrated circuits

Because of the recent availability of large scale integrated circuits, considerable effort has been devoted to the development of a digital PWM control system for power inverters, in order to eliminate the problems of drift and setting up procedure associated with analogue control techniques. However, it was also thought that these advantages should not be realised at the cost of deterioration in the harmonic spectra of the output PWM voltage waveform, or loss of adaptability and flexibility of the power inverter. Therefore, it was decided to implement the preferred regular sampled asymmetric PWM process by means of a microprocessor, where the switching points of the three-phase width-modulated pulses were determined by the stored program in conjunction with the input data.

After some initial re-design and testing of the analogue rig experimental results confirmed the suitability of the regular sampled form of PWM. Subsequently, a software based, microprocessor design was completed using the trignometric equation describing the individual pulse widths of the regular sampled, three phase, PWM waveform. The interface hardware containing the programmable timer module was re-designed several times since it was found that on some occasions the timer did not appear to operate to specification. Eventually the fault was found to be hardware based and caused by the inherent delays of the CMOS chips used for address decoding. Once

these delays were equalised the interface unit operated as required. The main hardware components retained from the analogue design, were the McMurray inverter and the pulse amplifier/sequence circuits.

The microprocessor rig was tested and used to control a 5h.p. induction motor over a range from 1Hz to 100Hz, although it was found necessary to modify the D.C. link voltage at both extremities. In addition, a spectrum analysis of the ouput waveform, from the microprocessor, proved that the system was accurately emulating the preferred regular sampled asymmetric technique of PWM generation far more accurately than the analogue rig.

1.1   Backround to the Application of the Thyristor in Variable Speed Drives

In early attempts, the generation of a variable frequency output, for induction motor power supplies, was both costly, complicated and only justified in special circumstances.   One practical application was as the propellor drive on battleships [20,21] where the generator speed was adjusted over a wide range by diesel or steam turbines.   In 1947 [22] Heumann reviewed the larger power (M.W.) techniques of producing variable frequency scources for induction motors. Alternators and frequency converters, driven by adjustable speed electric motors, were the two fundamental types of conversion apparatus in use.   Control of frequency was accomplished by the control of the speed of the driving motor of the conversion set, and the systems were used to spin large propellors, on test, for adjustable speed testing of compressor and gas turbines, and for the high power drive of large wind tunnels [23] (1958). Another scheme [24] generated the variable frequency by using a gas turbine alternator which powered six gas circulators which were driven by six 7,000H.P. squirrel cage induction motors. This was used for the CO_2 blower drives for the Hinkley Point and Bradwell Atomic Power Stations.

In 1956 Russian authors [25] considered the use of switching relays, in series with the 3 phase A.C. supply. Large inrush currents and slow switching speed limited the applications. This approach was further considered by Erlicki, [26] using thyratrons and

Bird [27] and Munoz [28] using thyristors. It appears that the approach could only produce a few discrete frequencies (such as 40Hz) at which proper operation of the induction motor was achieved. In 1958 Straughen [29] used a D.C. magnetic circuit as a frequency doubler which allowed the motor to operate at two discrete speeds, one being twice that of the other - even as late as 1961 [30] mercury arc rectifiers were still being considered for frequency changing.

The invention of the thyristor, in 1957, was to substantially improve the economics of power frequency - changing supplies for induction motors. By the early 1960's the thyristor had become well established as a power switching device. [31,32]

1.2 Classification of Present Day Variable Speed Drives

In the late 50's/early 60's, industrial manufacturers readily accepted the thyristor which compared so favourably with the fragile thyratron and bulky magnetic amplifiers as well as the motor generator sets, required for the generation of variable frequency sources, for motor speed control. The advent of the opto-coupler has also helped overcome the severe noise problems dictated by the heavy industry environment. This device has enabled the isolation of units, in order to avoid the problems of ground loops and parasitic capacitive coupling. Further, the continued increase in complexity and reduction in size of integrated circuits, has allowed the design of separate, modular units, which can be connected in various ways. These systems realise the functions of a wide range of variable speed A.C. drives such that costs are reduced and reliability improved.

Variable frequency inverters, for A.C. motors, have widely differing design approaches. Each design has its merits, although some techniques have distinct advantages which others do not possess. A brief description of the available types, is given together with an outline of their individual characteristics.

1.2.1 Variable Transformer Types

1.2.1.1 Type (a) Variable Input Transformer

The variable input transformer (VIT) inverter technique, Figure 1.1(a), transforms the input A.C. power line voltage, by a controllable turns ratio, which is determined by the ouput frequency of the inverter. The transformer output voltage is subsequently rectified and then modulated, by the inverter, to provide a three phase, quasi square-wave drive (i.e. the resulting phase voltage will have six steps) with adjustable voltage and frequency. Note that two controlled power conversion stages are required (the transformer and the inverter), that the transformer is expensive and would require mechanical maintenance. Further, the response time of the unit would be further limited by that of the variable ratio transformer whilst the inverter would have to be designed to operate over a wide voltage range.

FIXED 3 ∅
AC SUPPLY

VARIABLE
RATIO
TRANSFORMER

FIXED
RECTIFIER

THYRISTOR
VARIABLE
FREQUENCY
INVERTER

FREQUENCY
MONITOR

MOTOR

FIG 1·1(a)

FIXED 3 ∅
AC SUPPLY

FIXED
RECTIFIER

THYRISTOR
VARIABLE
FREQUENCY
INVERTER

VARIABLE
RATIO
TRANSFORMER

FREQUENCY
MONITOR

MOTOR

FIG 1.1(b)

FIXED 3 ∅
AC SUPPLY

PHASE CONTROLLED
THYRISTOR DRIVE
AC/DC CONVERTER

THYRISTOR
VARIABLE FREQUENCY
INVERTOR

MOTOR

FIG 1·1(c)

FIXED 3 ∅
AC SUPPLY

FIXED
RECTIFIER

THYRISTOR
CHOPPER

THYRISTOR
VARIABLE FREQUENCY
INVERTER

MOTOR

FIG 1·1(d)

1.2.1.2 Type (b) the Variable Output Transformer

The fixed A.C. supply is rectified and smoothed to provide a constant D.C. link voltage to the inverter Figure 1.1(b), whilst the inverter output is connected through a variable transformer whose turns ratio controls the voltage of the three phase supply to the motor Figure 1.1(b). The output transformer adjusts the amplitude of the motor supply, with output frequency, in order to maintain the proper voltage to frequency ratio.

The principle disadvantages are the slower response time, two power conversion stages are required whilst the output transformer must be a wide-band device, whose specifications must include its operation at the minimum output frequency and maximum rated load.

1.2.2 The Unrestricted Frequency Converter

This unit is very similar to the cycloconverter principle described later. The main difference is that the upper frequency limitations are removed through the introduction of forced commutation. Improvements in power factor are achieved, however, the extra costs and complexity of the device appears to have ensured that it still remains a project of research interest only, Miyairi and Takahashi [33] first proposed the system in 1968 and Westinghouse investigated a similar system although it is not, as yet, produced commercially.

1.2.3 The High Frequency Link Inverter

This technique uses a tuned circuit in the output which is excited from a pulse source – the output being transformer coupled to the motor. This approach is best adopted for constant speed drives as the tuned circuit components would require to be variable, necessitating some mechanical drive system. This system has proved useful in space applications for fixed frequency supplies and D.C. power conversion.

1.2.4 The Solid State Phase Shift Inverter

The input A.C. supply is rectified to a constant D.C. voltage which supplies two or more separate inverters, all in parallel. The output of the inverters are phase-shifted with respect to each other and added, algebraically by the use of output transformers. The phase shift can be modified in such a way as to control the output voltage amplitude.

This technique requires extra inverters and a wide-band output transformer increases complexity and cost although the method has again found use in space application for fixed frequency power supplies.

1.3 Practical Static Inverter Drives for A.C. Motors

1.3.1 The Six Step Voltage Fed Inverter

The most common waveform employed for static inverter drives is the six step or quasi-square wave drive Figure 1.1(c). Twelve, eighteen and twenty four step versions are possible, but their cost is seldom justified by the reduced harmonic content present in the output waveform. The six step waveform is specifically designed so that the third harmonic, and all its multiples, are identically zero. All the systems are capable of regeneration to a certain extent – resistors can be included to dissipate the regenerated energy. However, for true regeneration the diode bridge or thyristor bridge needs to be replaced by a bi-lateral thyristor bridge which would allow power flow in both directions. No further modifications are normally required to the inverter sections.

Commercially available stepped waveform inverters use many schemes to attain frequency and voltage control and all units are restricted to operation above 5Hz due to the crawling and cogging torques produced in the motor at lower frequency operation. The speed range is limited to about 10:1 and the predominant conversion methods are as follows.

1.3.1.2 Variable Voltage-Phase Controlled

Two power conversion stages are utilised Figure 1.1(c). The first stage converts the constant A.C. input voltage to a variable D.C. voltage by employing a phase controlled thyristor bridge, circuit. The second power conversion generates the quasi-square waveforms which determine the operating frequency of the supply to the motor. In this way a variable voltage, variable frequency, six-step, three-phase waveform is generated. In addition, by varying the D.C. voltage and the inverter frequency, simultaneously, a constant voltage/frequency ratio can be maintained, for a wide range of speeds.

It is usually necessary to provide a separate, constant voltage D.C. supply for the commutating circuit to ensure correct operation over the full speed range. This system tends to be the least expensive and although it cannot be operated from a standby battery, nor is it satisfactory for low frequency operation, it is the most common industrial power conversion technique. The system has a good response time, the limitations being determined by motor characteristics rather than those of the solid-state units.

1.3.1.3 Variable Voltage-Chopper-Controlled

The system requires three power conversion sections all in series Figure 1.1(d) a diode bridge for converting the A.C. input to a constant D.C. potential, a chopper and filter, for producing a variable D.C. supply and an inverter to set the frequency of the final A.C. drive to the motor.

The system has several advantages. It can be operated from a standby battery system, it has a fast response time, can operate a number of inverters at different frequency/voltage settings for multi-motor drives and the use of the high frequency chopper enables the design of sophisticated protection circuitry. Inverter fuse failures, due to load faults, are reduced by this safety system.

1.3.1.4 Six Step Current Fed Inverters

The basic systems are as previously outlined, the main differences being confined to the inverters. Large inductors are placed in series with the supply to the inverters. This has the effect of forcing the current to be constant, rather than the voltage. That is, it is the polarity of the voltage which reverses as the power flows to and from the load, during the cycle. In this case, it is necessary to provide voltage limiting circuits, instead of the current limiting circuits of the previous units.

The main advantage provided by this approach is the rugged reliability achieved in application. Momentary shorts, caused by load faults or interference, can be easily tolerated, without fusing, since the current remains constant (as determined by the D.C. link inductance). The inverter can be designed with low speed rectifier grade thyristors whilst the regeneration process is simple and no additional components are required - further only six thyristors are required. The current inverters do have several limitations however - they cannot operate on no load and are unstable on light load, high speed applications. Further the frequency range is somewhat lower and the large series inductor and commutating capacitor components

increase both size and costs of the inverter, whilst, at present, a single current inverter cannot be utilised with multi-motor drives.

1.3.2 The Cycloconverter

In theory, the cycloconverter Figure 1.2(a) requires only a single power conversion unit to convert the incoming constant voltage, constant frequency supply, to a variable voltage variable frequency supply. It is a direct A.C. to A.C. converter, since no intermediate D.C. link is required.

In practice, a three phase to six phase transformer is required, in order that the ripple amplitude on the output waveforms is reduced to a reasonable level. This entails the use of thirty- six thyristors (as compared to twelve in other bridge units) in the power conversion circuit, although commutation is effected naturally, by the polarity reversal of the input A.C. waveform.

The three phase sinusoidal output waveform is approximated by the phased addition of selected segments of the A.C. input waveforms as shown in Figure 1.2(b), so that its average value approaches a sine wave.

The cycloconverter is limited to producing low frequency drives - from below 1Hz to approximately one third of the supply frequency. If the modulator is operated beyond this limit, low frequency components are produced which interfere with the normal operation of the motor. Due to its high initial cost and low frequency limitations, its main application is found in controlling large motors (in excess of 500kW) or in controlling multi-motor stations as required in steel works

FIXED 3 ∅
AC SUPPLY

THYRISTOR
VARIABLE FREQUENCY
CYCLOINVERTER

MOTOR

SUPPLY VOLTAGE

OUTPUT VOLTAGE

FREQUENCY RATIO = 6

FIG 1.2(a)

FIXED 3 ∅
AC SUPPLY

FIXED
RECTIFIER

THYRISTOR BRIDGE
VARIABLE FREQUENCY
INVERTER

MOTOR

OUTPUT VOLTAGE

FREQUNCY RATIO = 5
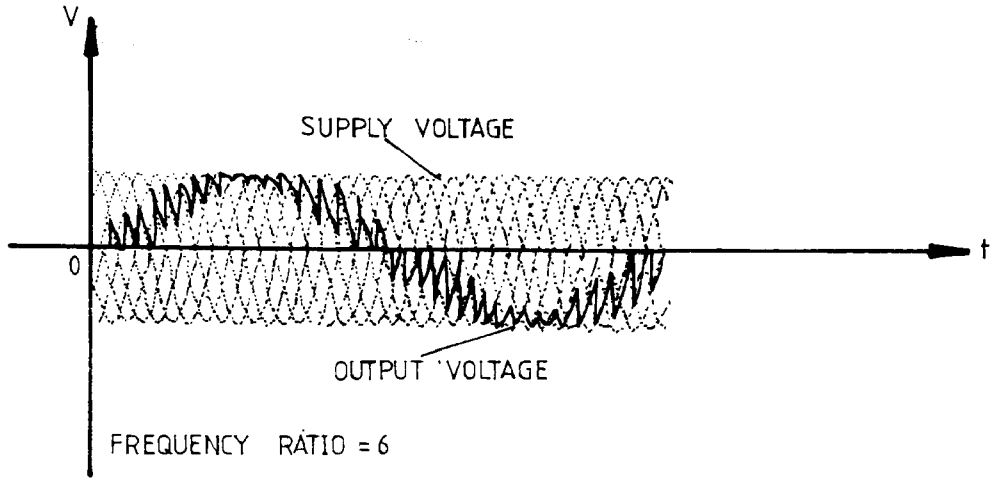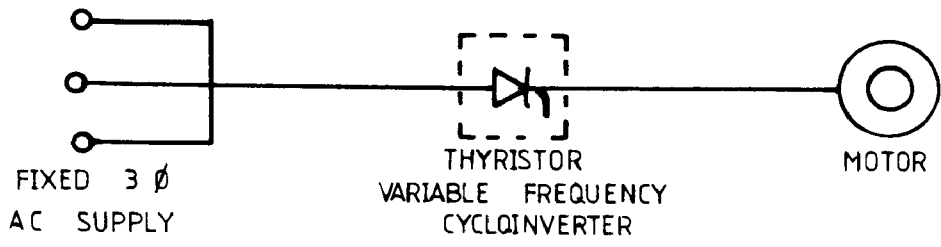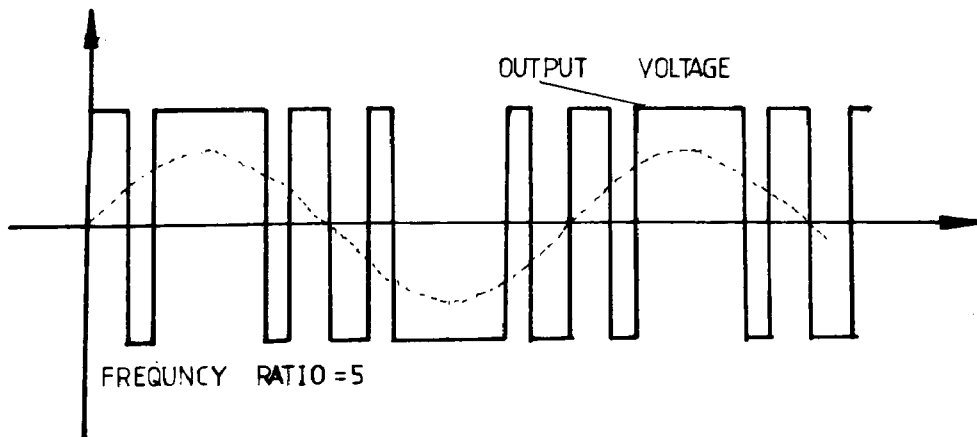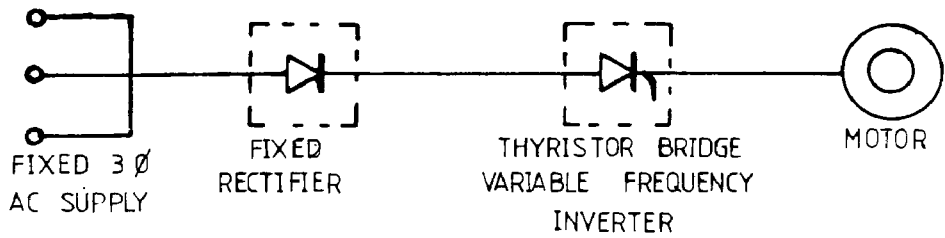
FIG 1.2(b)

roller tables. The drive can also suffer from poor power factor performance although it is fully regenerative in operation.

1.3.3 Pulse Width Modulation (PWM)

The input A.C. supply is rectified to provide a constant D.C. link voltage to a set of twelve thyristors connected in a bridge configuration Figure 1.2(b). The D.C. voltage is then converted into a set of pulses (the number may vary from one to over twenty- four) whose widths are varied, with respect to each other, and in such a way that their average value approximates to a sine wave as shown in Figure 1.2(b).

Two power conversion sections are required although both voltage and frequency control, of the output waveform, is achieved in a single set of thyristor bridge inverters. Voltage control is realised by varying the relative pulse widths whilst frequency control is achieved by varying the distances between the pulses (using some form of central reference point). As with the cycloconverter the number of pulses per cycle has a significant effect on the harmonic content of the waveform and the inductive reactance of the motor serves so as to smooth the input current waveform.

Good power factors (approximately 0.96 at all frequencies) and unrestricted frequency ranges are obtained. Low frequency operation below 5Hz, is also easily achieved through the use of larger pulse numbers (hence fewer low frequency harmonics). However, regeneration is not possible with a rectified three phase supply and the power handling capability is limited to approximately 100kW by the fact that

the fast-turn off inverter grade thyristors have a limited power specification.

All the schemes, presented in the brief review, are open loop control systems. That is there is no feedback control included in their circuitry. Although the dynamic performance of every unit could be improved using frequency, voltage, current or flux feedback information the basic limitations of each approach still remain.

1.4 Pulse Modulation - Theoretical Possiblities

Variable speed/torque induction motor drives require variable frequency/voltage sources. Generally, mains power supplies are constant frequency, constant voltage sources so that power transmission can be cost effective. Thus, some method of achieving a variable frequency, variable voltage supply from a static frequency, static voltage supply needs to be implemented.

There are many techniques of power conversion where the aim is to provide a three-phase variable frequency, variable voltage source [1,2]. For high power converters, where efficiency is at a premium the use of pulse modulated systems has found favour because the system can operate with efficiencies in excess of 90%. Further the technology of thyristors has advanced such that fast turn-off, high power devices are available at a low enough cost to ensure the economic viability of power inverters.

The availability of high power thyristors has accentuated the development of pulse-modulated power transfer [34] and pulse modulation techniques have also been used extensively in the

communications field for the transmission of information signals [8]. The process of static frequency change is known as modulation. For example, amplitude modulation is a process which changes both the amplitude and frequency of a fixed frequency source. Information transmission and coding techniques cover frequency modulation (FM), amplitude modulation (AM), phase modulation (PM), double sideband modulation (DSM) and pulse - position modulation (PPM), pulse code modulation (PCM) and pulse amplitude modulation (PAM). All of these approaches can be applied to the problem of variable frequency power transmission from the A.C. supply to the induction motor; not all will be efficient and those techniques most suited to information transmissions will not, of necessity, be most efficient in application to power transfer.

However, the application of communication principles to variable-frequency, solid-state power converters has resulted in significant improvements, in efficiency, of power inversion through the implementation of pulse width modulation (PWM) as a means of frequency and voltage control.[35]

PWM is a well known principle of information communication [4] and the concept of A.C. power converters as modulators (since frequency changing can only be obtained by modulation) has influenced research activities in employing the premise that communication principles can be applied to modern power converters with some benefit.[36]

Other practical examples of the applications of communication principles to power converters are the use of amplitude modulation to achieve a 2:1 speed change [28], the stepped sine wave modulation

principle   [7], which achieves the elimination of subharmonic problems (at non-integer frequency ratios) and the implementation of mathematical analyses which allow a fundamental appreciation of the modulation principle involved.[38] Alternative analyses can also provide a clear insight into the frequency spectra of the modulation process when integer frequency ratios are adopted. [9]

1.4.1 Types of Pulse Modulation

The unmodulated carrier-wave of a pulse-modulated system, is generally considered to consist of a series of regularly recurring pulses. Such a waveform can be completely defined by three parameters. The three parameters are :

1. The amplitude of the pulses, Vp.

2. The duration between pulses, T.

3. The duration of the pulses, to.

Normally the three parameters are constant. Modulation is the process of varying one or more of the three parameters, while the remaining parameters are held constant. Variation of the amplitude of the pulses while the duration between pulses and the duration of the pulses are held constant is termed - 'amplitude-modulation'. When the amplitude and duration of the pulses are held constant, and the duration between the pulses is made to vary, 'pulse-position-modulation' is achieved. The variation of the duration or width of the pulses, while the amplitude of the pulses and

V ↑   MODULATING WAVE

0   t

V ↑   PULSE CARRIER WAVE

0   t

V ↑   PULSE AMPLITUDE MODULATED WAVE

0   t

V ↑   PULSE WIDTH MODULATED WAVE

0

V ↑   PULSE POSITION MODULATED WAVE

0   t
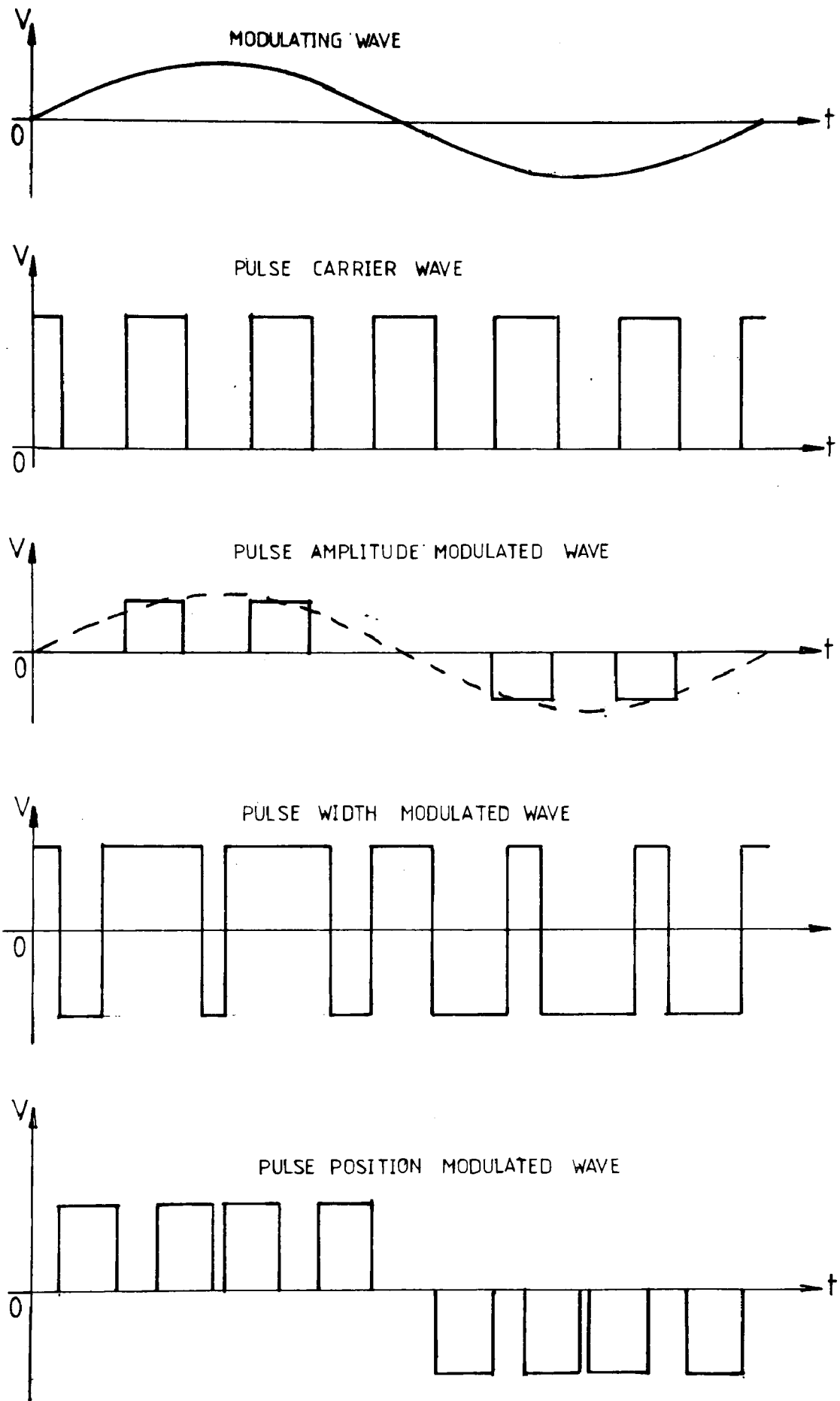
TIME DOMAIN REPRESENTATION OF PULSE MODULATION

FIG 1.3

duration between the pulses are held constant, is known as 'pulse-width-modulation'. The above modulation processes are illustrated in the time domain in Figure (1.3). Although pulse-modulation normally infers the variation of one parameter while the remaining two parameters are held constant, the possibility of simultaneously varying two of the three parameters or all three parameters cannot be ruled out.

1.4.2 The Unmodulated Pulse Carrier Wave

The zero on the time-axis of the unmodulated pulse-carrier wave may be positioned as shown in Figure 1.4(a). The carrier-wave can then be expressed by the following time function :

$$U(t) = k + k \sum_{m=1}^{m=\infty} \frac{\text{Sin } m \, k \, \pi}{m \, k \, \pi} \cdot \text{Cos } m \, \omega_c t \qquad \text{---- (1.1)}$$

where $k = \dfrac{t_o}{T}$.

1.4.3 Pulse Amplitude Modulation (P.A.M.)

This method of modulation basically entails the variation of the amplitude of the pulses according to the modulating signal, so that instead of the pulses having unit height, they have a height varying as V(t), where V(t) is the modulating function. Therefore, if the modulating function is defined by :

$$V(t) = A_m \, \text{Cos}(\omega_m t + \phi_m) \qquad \text{---- (1.2)}$$

then the process of amplitude modulation is given by :

$$V(t) \cdot U(t) = [A_m \text{Cos}(\omega_m t + \phi_m)] \quad [k + k \sum_{m=1}^{m=\infty} \frac{\text{Sin } m \, k \, \pi}{m \, k \, \pi} \cdot \text{Cos } m \omega_c t]$$

$$= k \, A_m \text{Cos}(\omega_m t + \phi_m) +$$

$$k A_m \sum_{m=1}^{m=\infty} \frac{\text{Sin } m \, k \, \pi}{2 \, m \, k \, \pi} \cdot \text{Cos } [(m\omega_c \pm \omega_m)t \pm \phi_m] \quad \text{---- (1.3)}$$

This process is illustrated in both the time and frequency domains in Figure 1.4. It will be seen from equation (1.3) that the products of modulation are upper and lower side bands of frequencies : $(m\omega_c + \omega_m)$ and $(m\omega_c - \omega_m)$ around the carrier of frequency, ω_c, and its harmonics, plus a remanent of the modulating wave of frequency, ω_m. The amount of modulating wave remaining, will depend on the magnitude of A_m and the value of k.

1.4.4 Pulse Position Modulation (P.P.M.)

P.P.M. causes the pulses illustrated in Figure 1.5 to be displaced in time according to instantaneous values of the modulating wave, the height and duration of the pulses being maintained constant. The unmodulated pulses which have a repetition period, T, and mid-time values at 0,T,2T,3T————, are described by the time function :

$$U(t) = k + k \sum_{m=1}^{m=\infty} \frac{\text{Sin } m\,k\,\pi}{m\,k\,\pi} \cdot \text{Cos } m\omega_c t \qquad\qquad \text{————(1.1)}$$

If the pulse centre lines are varied in time according to the function :

$$T.A_m \text{ Cos } (\omega_m t + \phi_m)$$

and to $\ll T$, then the pulse position modulated pulses are described by the time-function [37] :

$$f(t) = k + 2k \sum_{m=1}^{m=\infty} \frac{\text{Sin } m\,k\,\pi}{m\,k\,\pi} \text{ Cos } m\,\omega_c \Big[t -$$

$$T\,A_m \text{ Cos}(\omega_m t + \phi_m)\Big] \qquad\qquad \text{————(1.4)}$$

FREQUENCY DOMAIN

For k ≠ 1/2

(a)

(b)

(c)

TIME DOMAIN

CARRIER WAVE

$k = t_0/T$

MODULATING WAVE

OUTPUT WAVE

PULSE AMPLITUDE MODULATION

FIG 1-4

TIME DOMAIN

CARRIER WAVE

MODULATING WAVE

OUTPUT WAVE

PULSE POSITION MODULATION

FREQUENCY DOMAIN

For k ≠ 1/2

w_c $2w_c$

w_m

$(w_c - nw_m)$ $(2w_c - nw_m)$ $(2w + nw_m)$

$(w_c + nw_m)$

w_c $2w_c$

w_m
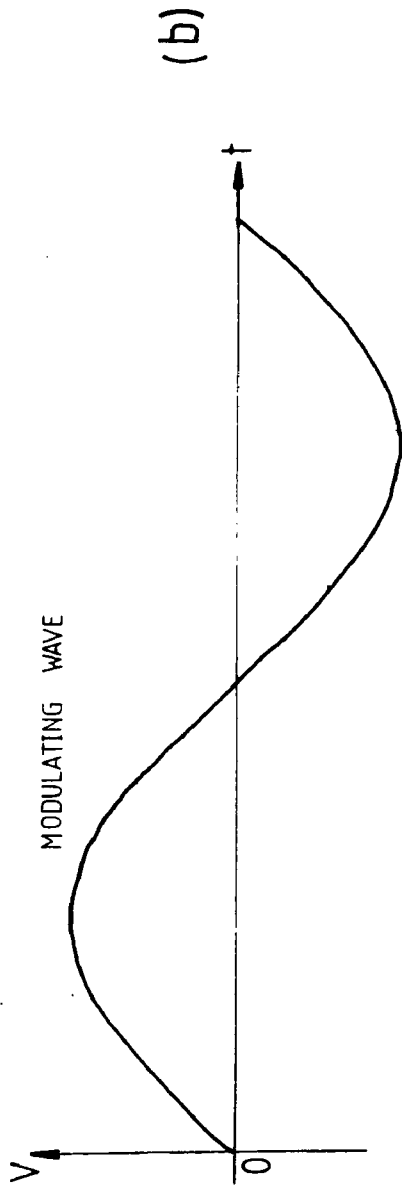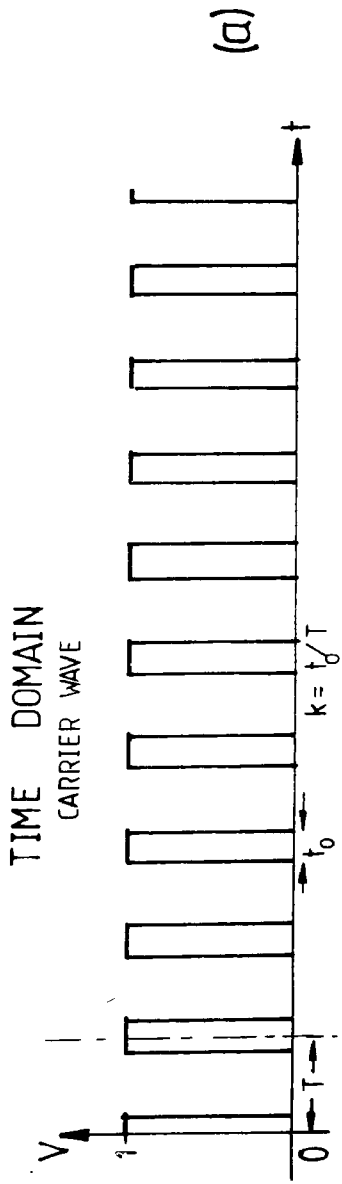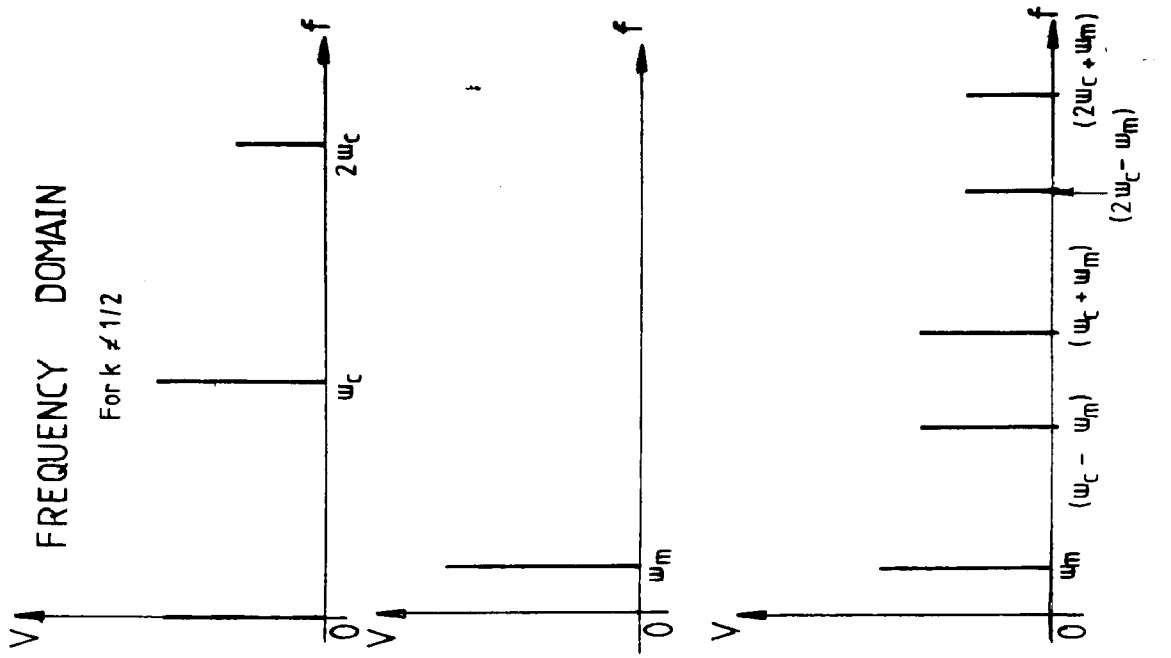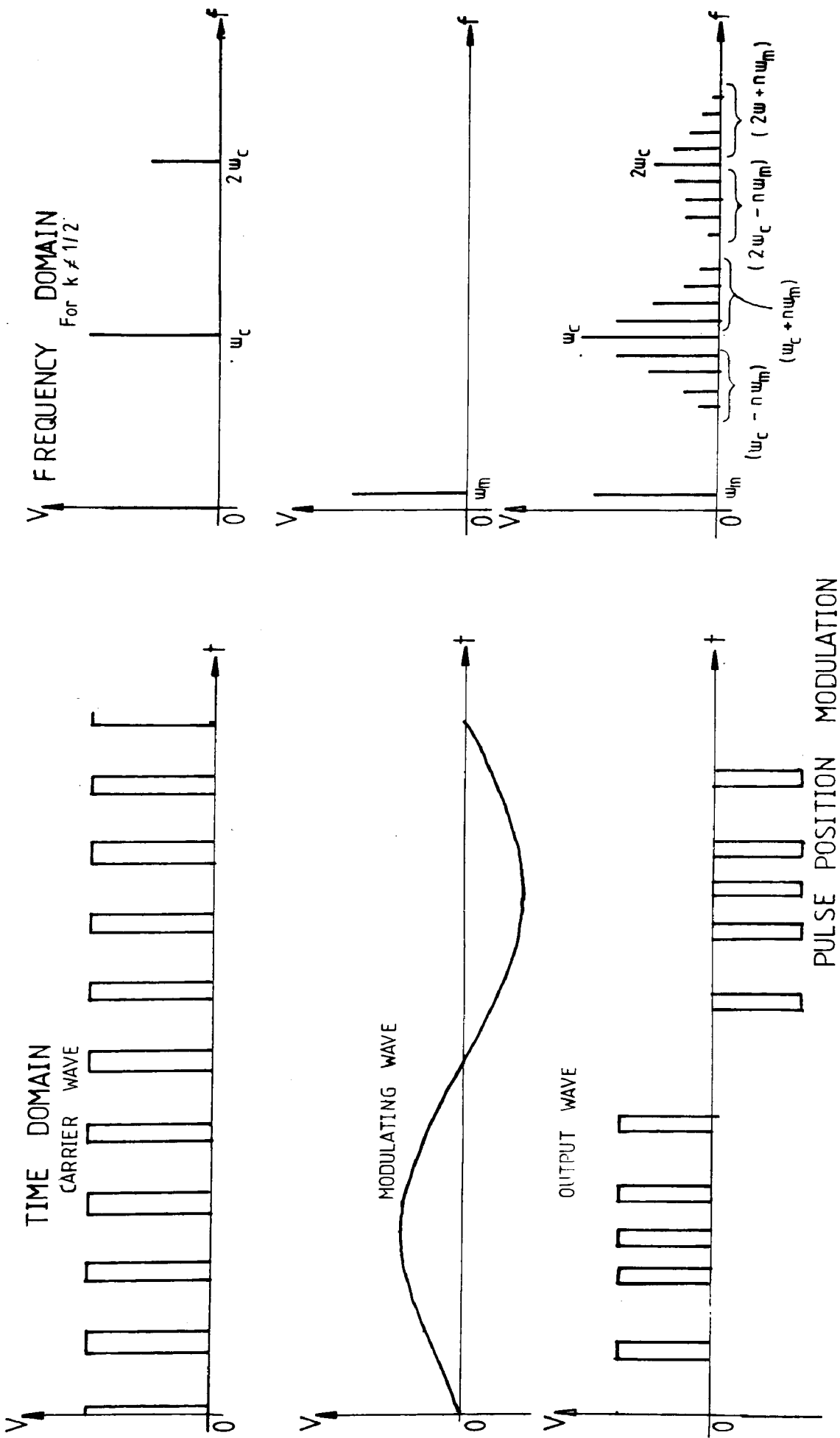
FIG 1-5

Equation (1.4) can be further expanded in terms of Bessel functions as follows :
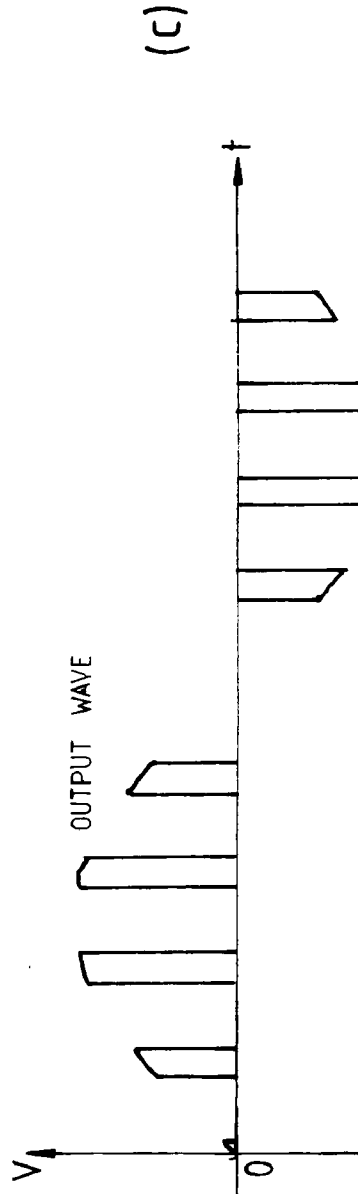
$$
\begin{aligned}
f(t) \;=\; & k + 2k \sum_{m=1}^{m=\infty} \frac{\text{Sin } m\,k\,\pi}{m\,k\,\pi} \,\{J_0(x)\text{Cos } m\omega_c t \\
& + J_1(x)\, [\text{Sin}\,[(m\omega_c - \omega_m)t - \phi_m] - \text{Sin}\,[(m\omega_c + \omega_m)t + \phi_m]] \\
& - J_2(x)\, [\text{Cos}\,[(m\omega_c - 2\omega_m)t - 2\phi_m] + \text{Cos}\,[(m\omega_c + 2\omega_m)t - 2\phi_m]] \\
& - J_3(x)\, [\text{Sin}\,[(m\omega_c - 3\omega_m)t - 3\phi_m] - \text{Sin}\,[(m\omega_c + 3\omega_m)t + 3\phi_m]] \\
& + - - - - - - - - - - - - - - - - \} \qquad\text{———(1.5)}
\end{aligned}
$$

where $x = 2\pi A_m m$.

Figure (1.5) illustrates the P.P.M. process in both the time and frequency domains. Equation (1.5) illustrates that the products of modulation are the carrier signal and its harmonics which have amplitudes of $2\,\dfrac{\text{Sin } m\,k\,\pi}{m\,\pi}\,J_0(x)$, and side-bands around the carrier and its harmonics of frequencies : $m(\omega_c - \omega_m)$ and $m(\omega_c + \omega_m)$ and amplitudes of $\dfrac{2\,\text{Sin } m\,k\pi}{m\,\pi}\,J_n(x)$.

It is important to note that equation (1.5) does not contain a harmonic component of modulating frequency whose amplitude is proportional to the amplitude of the modulating wave. This suggests that no linear means of voltage control of the wanted harmonic component is provided.

1.4.5 Pulse-Width-Modulation (PWM)

This method of modulation causes the widths of the pulses illustrated in Figure 1.4(a) to vary. The degree of variation in the width of each pulse, is dependent upon instantaneous values of the modulating wave. The three possible ways by which the duration of the

pulses can be varied are :

1. leading-edge fixed, trailing-edge varied,

2. trailing-edge fixed, leading-edge varied,

3. centre line of pulses fixed, both edges varied.

These three methods of varying the widths of the pulses are used to define the type of pulse-width-modulation, and are illustrated in Figure (1.6).

1.4.6 Trailing-Edge Pulse-Width-Modulation

This particular form of P.W.M. causes the leading-edges of the pulses to be fixed, whilst the trailing-edges are modulated, the degree of modulation being dependent upon instantaneous values of the modulating wave. This process is illustrated in Figure (1.7). The unmodulated pulses of duration, to, and repetition period, T, are described by the time function [38] :

$$f(t) = k + k \sum_{m=1}^{m=\infty} \frac{\text{Sin } 2m \text{ k } \pi}{m \text{ k } \pi} \text{ Cos } m\omega_c t$$

$$+ k \sum_{m=1}^{m=\infty} \frac{(1-\text{Cos } 2 \text{ m k } \pi)}{m \text{ k } \pi} \text{Sin } m\omega_c t \qquad \text{----(1.6)}$$

For this case one of the leading edges of the pulses, is chosen to coincide with zero time as illustrated in Figure (1.7). If the duration of the pulses are varied according to the function :

$$T_o(1 + A_m \text{Cos}(\omega_m t + \phi_m)) \qquad \text{----(1.7)}$$
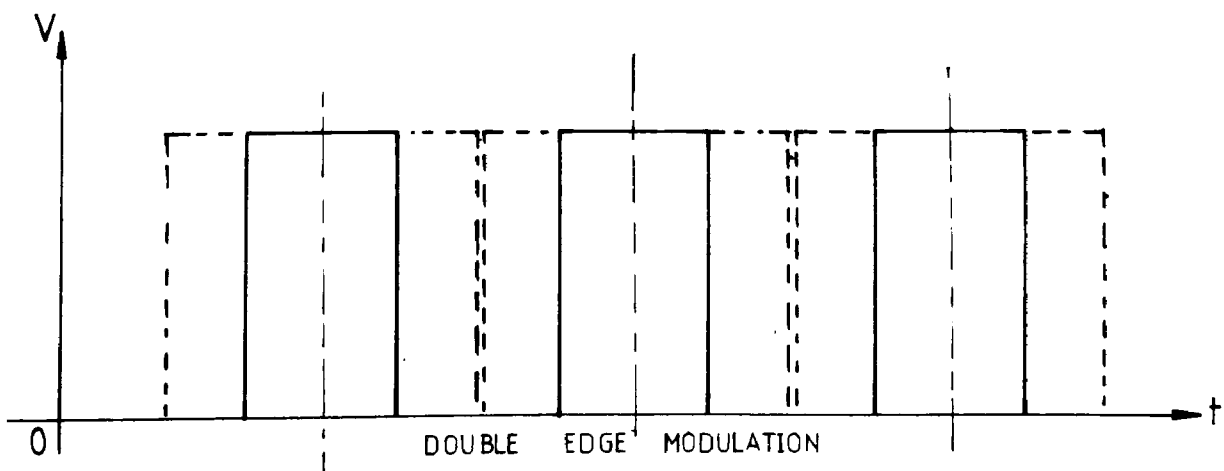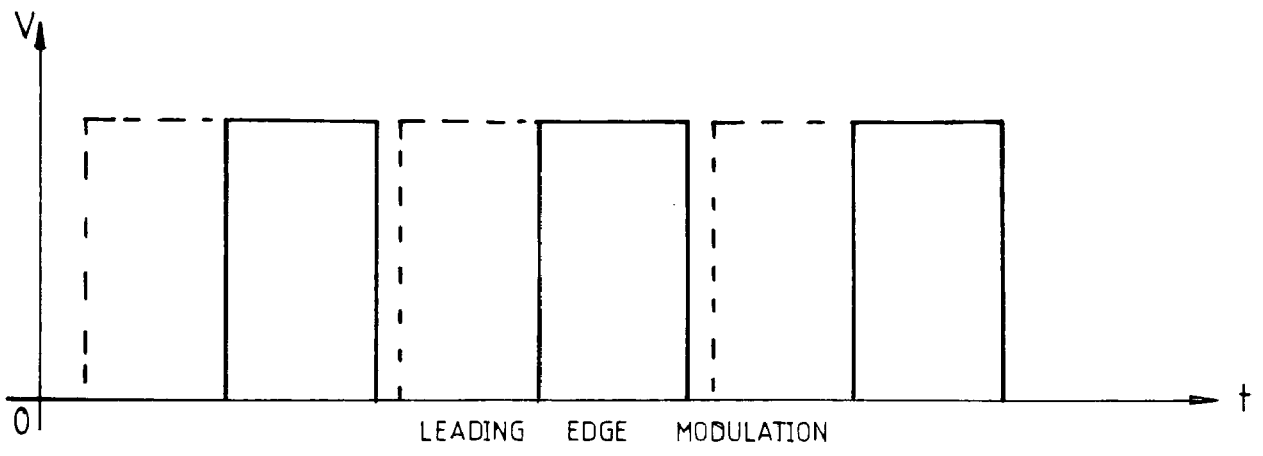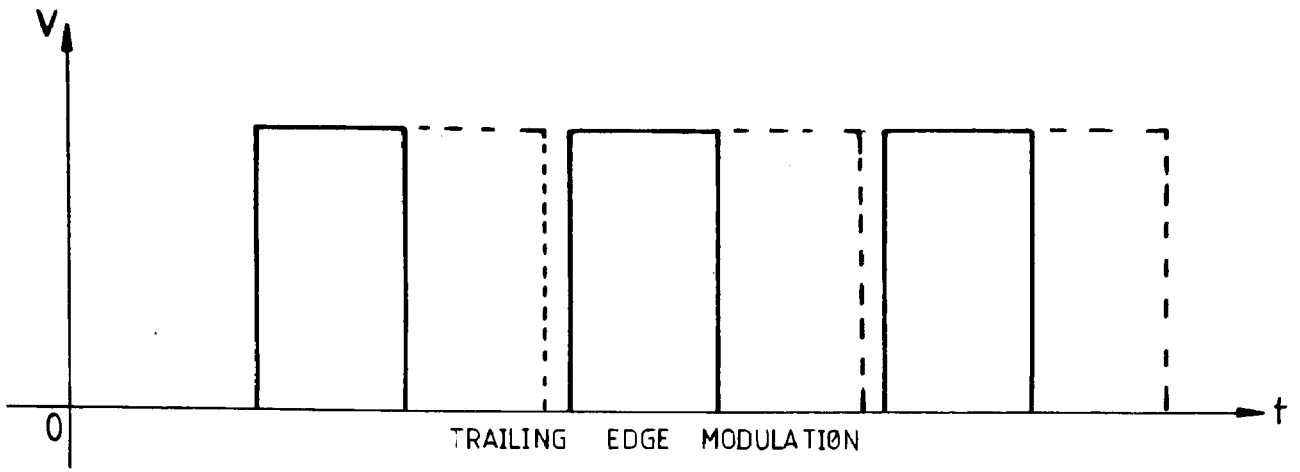
TYPES OF PULSE WIDTH MODULATION

FIG 1-6

FREQUENCY DOMAIN
For k =1/2

ω_c

ω_m

ω_c

$2\omega_c$

$(\omega_c - n\omega_m)$ $(\omega_c + n\omega_m)$ $(2\omega_c - n\omega_m)$ $(2\omega_c + n\omega_m)$

ω

TIME DOMAIN
CARRIER WAVE

t_0

T

MODULATING WAVE

OUTPUT WAVE
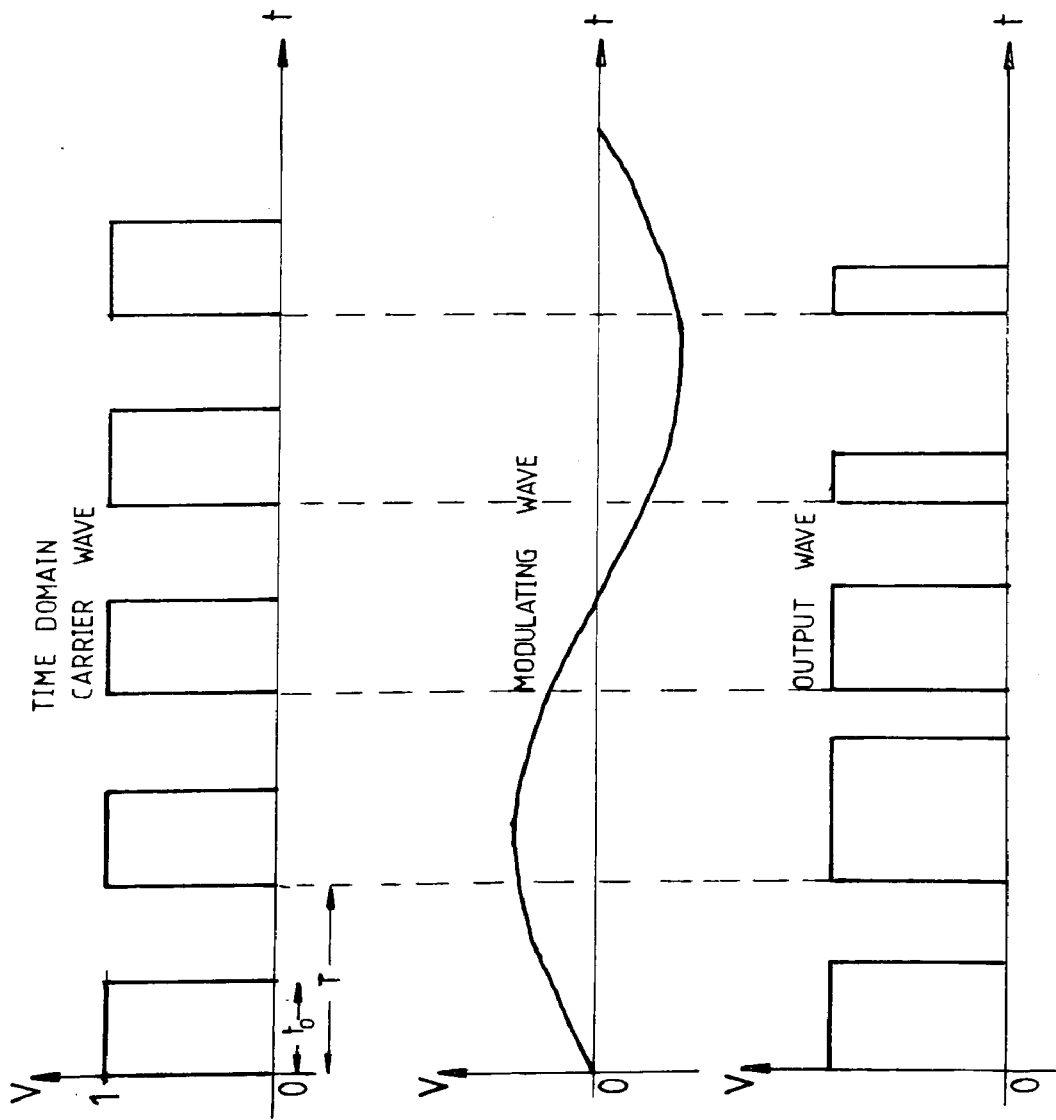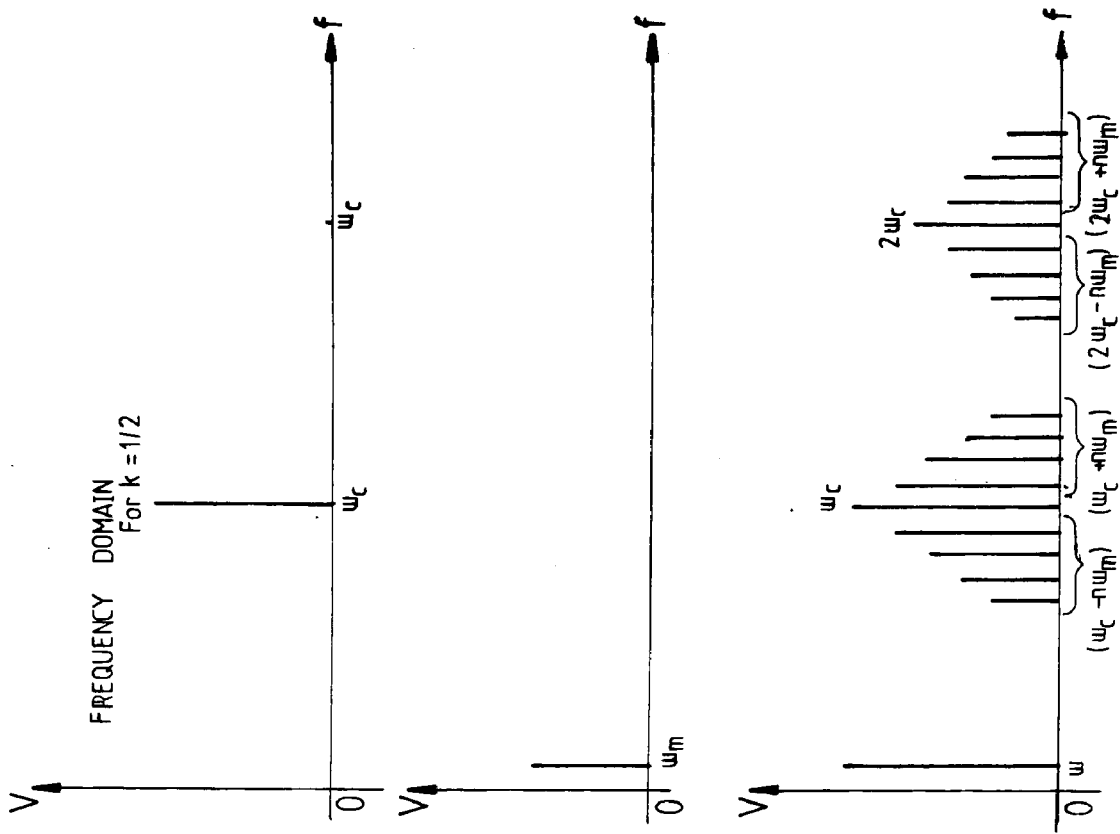
TRAILING EDGE MODULATION

FIG 1-7

then the width modulated pulses are described by the function :

$$f(t) = k(1 + A_m Cos(\omega_m t + \phi_m))$$

$$+ \frac{1}{\pi} \sum_{m=1}^{m=\infty} \frac{1}{m} [Sin \, 2 \, m \, \pi k(1 + A_m Cos(\omega_m t + \phi_m))] Cos \, m\omega_c t$$

$$+ \frac{1}{\pi} \sum_{m=1}^{n=\infty} \frac{1}{m} [1 - Cos \, 2 \, \pi m \, k(1 + A_m Cos(\omega_m t + \phi_m))] Sin \, m\omega_c t$$

$$\text{———(1.8)}$$

This function can also be described in terms of Bessel functions as follows :

$$f(t) = k(1 + A_m Cos(\omega_m t + \phi_m)) + \frac{1}{\pi} \sum_{m=1}^{m=\infty} \frac{1}{m} (Sin \, m\omega_c t)$$

$$+ \frac{1}{\pi} \sum_{m=1}^{m=\infty} \sum_{n=1}^{n=\infty} \frac{1}{m} [J_n(2 \, m \, \pi k \, A_m) Sin(2 \, m\pi \, k + \frac{n\pi}{2})] Cos((m\omega_c \pm n\omega_m)t \pm n\phi_m$$

$$- \frac{1}{\pi} \sum_{m=1}^{m=\infty} \sum_{n=1}^{n=\infty} \frac{1}{m} [J_n(2 \, m \, \pi k \, A_m) Cos(2 \, m \, \pi \, k + \frac{n\pi}{2})] Sin((m\omega_c$$

$$\pm n\omega_m)t \pm n \, \phi_m) \qquad \text{———(1.9)}$$

From equation (1.9), several interesting facts are apparent : the amplitude of the harmonic component of modulating frequency, is directly proportional to the amplitude of the modulating wave. No harmonics of the modulating wave are present. The amplitude of a harmonic of the carrier wave is inversely proportional to its order. It is of particular interest to note that if the mark/space ratio of the unmodulated pulse carrier-wave is made equal to 1:1, that is to say k = 1/2; then only one of the two side-band terms exists for integer values of m and n. Therefore, for odd values of m and n the

side-band components $\mathrm{Sin}((m\omega_c \pm n\omega_m)t \pm \phi_m)$ will exist with amplitudes of $\frac{1}{m\pi}J_n(2\ m\pi k\ A_m)$, whereas, for even values of m and n the side- band terms of $\mathrm{Cos}((m\omega_c \pm n\omega_m)t \pm \phi_m)$ will exist, their amplitudes being given by : $\frac{1}{m\pi}J_n(2\ m\ \pi\ k\ A_m)$.

This means that for all integer values of m and n, side-band frequency components of frequencies : $(m\omega_c + n\omega_m)$ and $(m\omega_c - n\omega_m)$ will always occur for this particular form of P.W.M.

1.4.7   Leading-Edge Pulse-Width-Modulation

For this P.W.M. process the trailing-edges of the pulses are fixed while the leading-edges are modulated. Figure (1.8) illustrates this process in both the time and frequency domains. The time function which describes the modulation of the pulses can be determined from equation (1.9) by reversing the time scale; that is to say : substituting -t for t. This results in the following function :-

$$f(t) = k(1 + A_m\ \mathrm{Cos}(\omega_m t + \phi_m)) - \frac{1}{\pi}\sum_{m=1}^{m=\infty}\frac{1}{m}\mathrm{Sin}\ m\omega_c t$$

$$+ \frac{1}{\pi}\sum_{m=1}^{m=\infty}\sum_{m=1}^{m=\infty}\frac{1}{m}[J_n(2\ m\pi k A_m)\mathrm{Sin}(2\ m\pi k + \frac{n\ \pi}{2})]\ \mathrm{Cos}((m\omega_c$$

$$+ n\omega_m)t + n\phi_m)$$

$$+ \frac{1}{\pi}\sum_{m=1}^{m=\infty}\sum_{m=1}^{m=\infty}\frac{1}{m}[J_n(2\ m\pi k A_m)\mathrm{Cos}(2\ m\pi k + \frac{n\ \pi}{2}))]\mathrm{Sin}((m\omega_c$$

$$+ n\omega_m)t - n\phi_m) \qquad \text{--(1.10)}$$

FREQUENCY DOMAIN
For k = 1/2

$2w_c$

w_c

w_m

$(w_c - nw_m)$ $(w_c + nw_m)$ $(2w_c - nw_m)$ $(2w_c + nw_m)$

$2w_c$

w_c

w_m

TIME DOMAIN CARRIER WAVE

MODULATING WAVE

OUTPUT WAVE

t_o

T
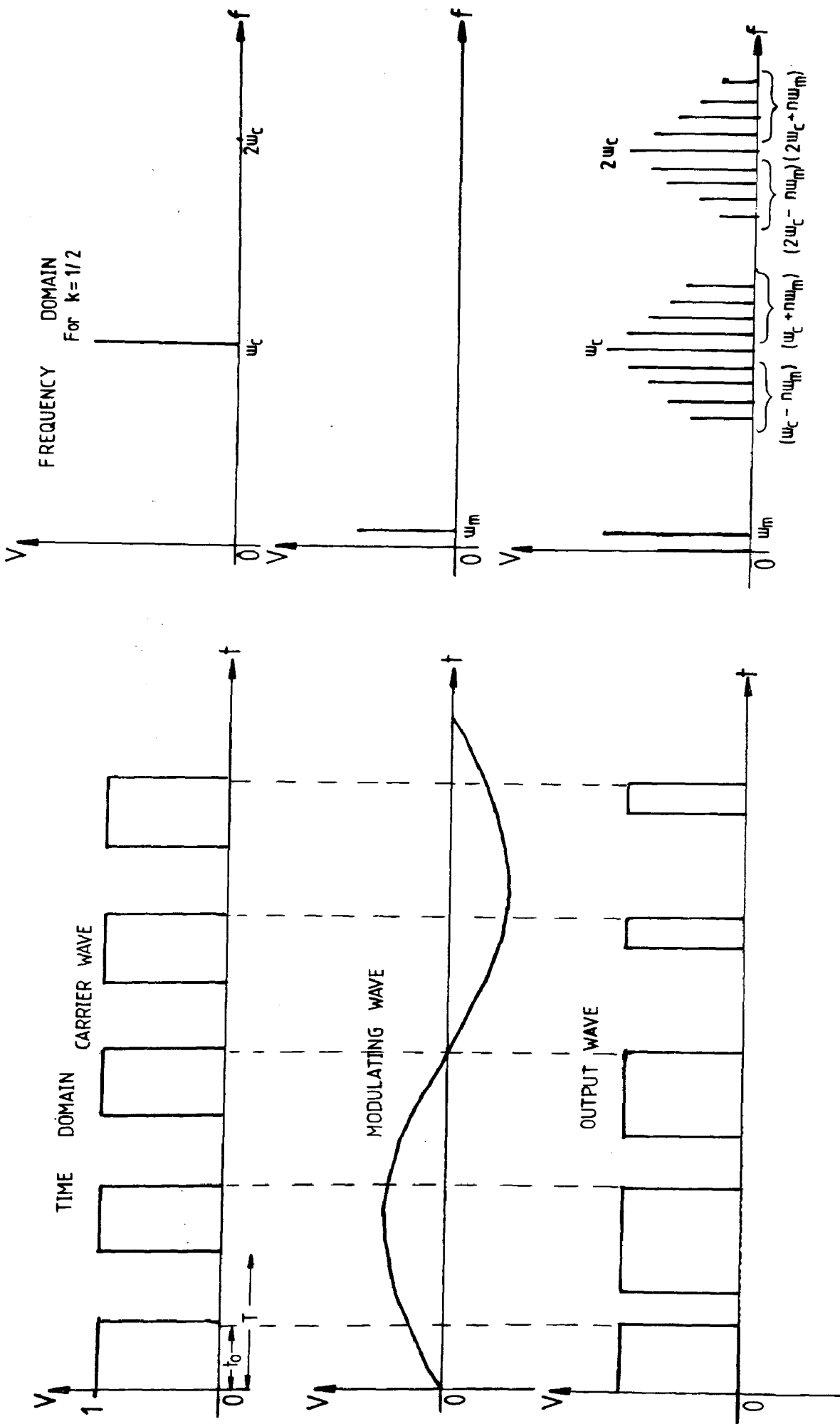
LEADING EDGE MODULATION

FIG 1-8

- 34 -

The amplitudes of the various components are the same as for trailing-edge modulation but the phase relationships are different.

1.4.8 Double-Edge Pulse-Width-Modulation

This form of modulation causes both edges of the pulses to be modulated. The instants in time at which the leading and trailing edges of each pulse occur, are dependent upon the respective instantaneous values of the modulating wave. This process is illustrated in Figure (1.9). The unmodulated pulses of duration, t , with one pulse centred at t= o, can be described by the time function :-

$$f(t) = k + \frac{2}{\pi} \sum_{m=1}^{m=\infty} [\frac{1}{m} \text{Sin } m \pi k] \text{ Cos } m\omega_c t \qquad \text{------}(1.11)$$

If the duration of the pulses are varied according to the function :

$$t_o(1 + A_m \text{ Cos}(\omega_m t + \phi_m)) \qquad \text{------}(1.12)$$

then the width - modulated pulses are described by the function :

$$f(t) = k(1 + A_m \text{Cos}(\omega_m t + \phi_m))$$

$$+ \frac{2}{\pi} \sum_{m=1}^{m=\infty} \frac{1}{m} \{ \text{Sin } m \pi k \text{ Cos } [m \pi k A_m \text{Cos}(\omega_m t + \phi_m)]$$

$$+ \text{ Cos } m \pi k \text{ Sin } [m \pi k A_m \text{Cos}(\omega_m t + \phi_m)] \} \text{ Cos } m\omega_c t$$

$$\text{----}(1.13)$$

FREQUENCY DOMAIN

For k=1/2

TIME DOMAIN

CARRIER WAVE

MODULATING WAVE

OUTPUT WAVE
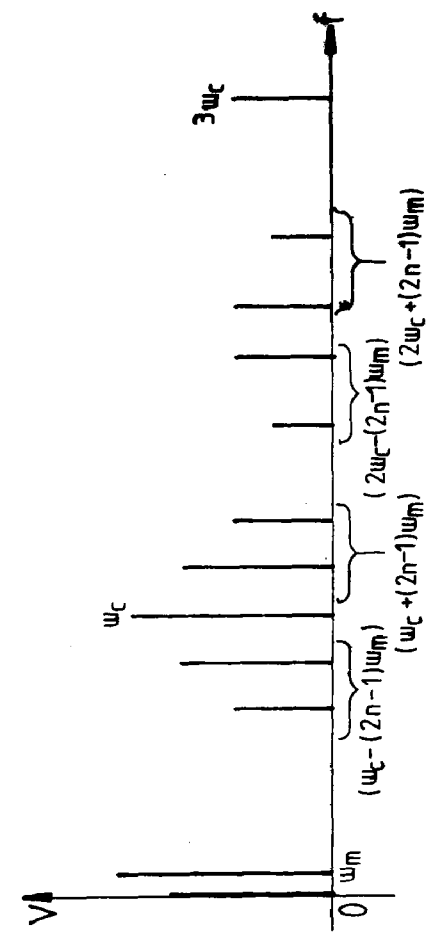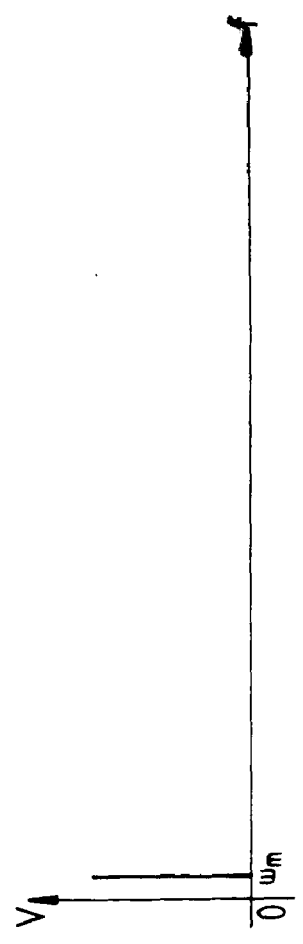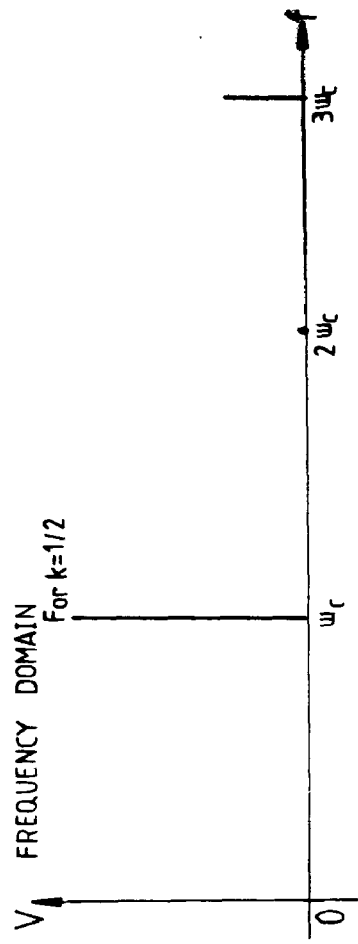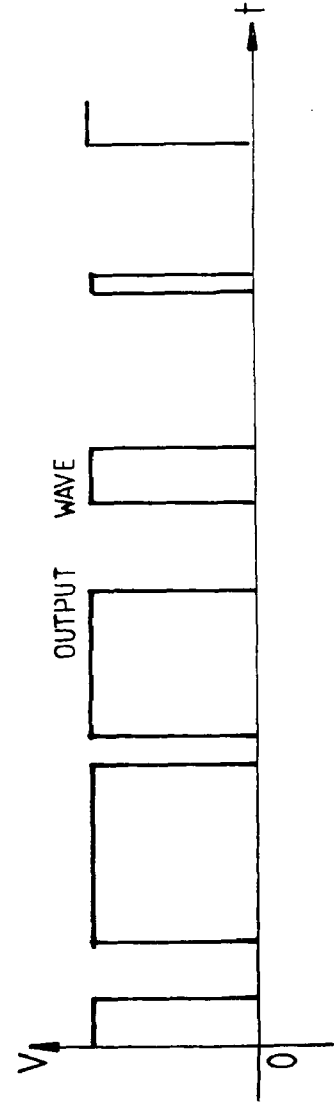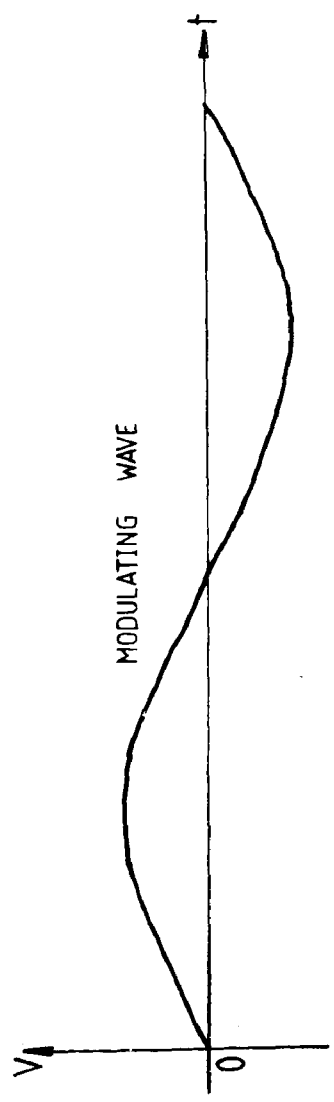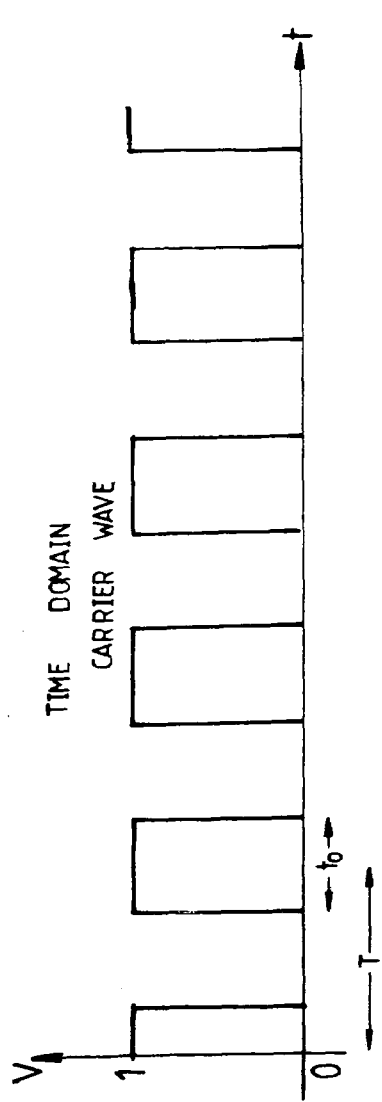
DOUBLE EDGE PULSE WIDTH MODULATION
FIG 1-9

- 36 -

This function can also be described in its Bessel function form as follows :

$$f(t) = k(1 + A_m \cos(\omega_m t + \phi_m))$$

$$+ \frac{2}{\pi} \sum_{m=1}^{m=\infty} \frac{1}{m} \{ [J_o(m \pi k A_m) \sin m \pi k] \cos m \omega_c t$$

$$+ \sum_{n=1}^{n=\infty} J_n(m \pi k A_m) \sin(m \pi k + \frac{n \pi}{2}) \ [\cos((m\omega_c$$

$$+ n\omega_m)t + n\phi_m)$$

$$+ \cos((m\omega_c - n\omega_m)t - n\phi_m)] \} \qquad \text{----(1.14)}$$

This function shows that, for this case also, the amplitude of the harmonic component of modulating frequency is proportional to the amplitude of the modulating wave.

The second term gives the carrier component and its harmonics of frequency $m\omega_c$. The amplitude of the harmonics of the carrier wave are dependent upon the value of k. If k = 1/2, (that is to say : the mark/space ratio of the unmodulated pulses is 1:1) then only odd harmonics of the carrier will be present.

The third term gives the side-band about the carrier whose frequencies are given by $(m\omega_c + n\omega_m)$ and $(m\omega_c - n\omega_m)$. The amplitude of the side-bands are once again dependent upon the value of k. If k = 1/2 as before then for odd harmonics of the carrier only even order side-bands exist, and for even harmonics of the carrier only odd order side-bands exist.

1.5 Techniques of P.W.M. Generation

It should be noted that when P.W.M. is used as a means of information communication that part of the signal power which carries no information to the receiver is wasted. The amount of power wasted depends upon the maximum extent to which a pulse can be modulated. When the redundant part is subtracted from the P.W.M. wave, we have P.P.M. and the power saved represents the fundamental advantages of P.P.M. over P.W.M.[39] for information transmission.

In the field of variable speed A.C. drives it is the transmission of power, not information, which is of fundamental importance. This fact produces a difference in the philosophical approach to the design of Power Systems. Optimum techniques of information transmission are not necessarily optimum techniques of power transmission. The redundant power frequency term in P.W.M. actually cancels in the three phase drive, which improves its qualities as a means of power transmisson. Further, P.P.M. will always have a greater pulse number than P.W.M. for any given power transfer and minimum pulse width requirement. These facts alone significantly reduce the efficiency of P.P.M. inverters due to the associated increase in power losses. Thus, for power systems, P.W.M. is superior to P.P.M. as a method of power conversion and transmission. Thus, when applying communications principles to power systems the philosophical differences should be given careful consideration.

The use of a pulse amplitude modulation scheme immediately introduces the practical requirement of a fast response time, variable voltage supply. This technique can provide a reduced harmonic content, in the output power signal, with respect to that of the P.W.M. signal. However, the extra cost and complexity involved would not appear to be justified by the gain in reduction of harmonic content. Further, the double-sided form of P.W.M. modulation has significant advantages over the single-sided forms of P.W.M. modulation. In addition, this does not involve any extra cost or complexity-simply a change in the modulation waveforms used to obtain the P.W.M. waveform. It is also of practical significance that both frequency and voltage control can be achieved in the P.W.M. signal with a single set of power modulators. Whilst problems of cogging, torque pulsations and poor low frequency operation [40,41,42] have been reported in the literature, as already demonstrated, the harmonic content of the P.W.M. waveform can be considerably changed by the choice of modulating waveforms, used to achieve the P.W.M. signal. This fact is of importance as it affects the harmonic content of the waveform at frequencies near the fundamental − this has a direct practical effect on the appearance of cogging and locking torques.

1.5.1 Specialist P.W.M.Schemes

Using a mixer/multiplier in communication circuits has some similarity to the use of a comparator in power circuits. By changing the character of the two input signals to the mixer, differing processes of modulation can be obtained (that is A.M., D.S.M.). In the same way, very different forms of P.W.M. can be obtained simply

by changing the two modulating signals to the comparator Figure 1.10(a).

A large number of P.W.M. generation techniques have been proposed in the literature [16,43] in an effort to produce an improved A.C. variable speed induction motor drive with lower losses, fewer pulsating torques and greater frequency stability. The P.W.M. waveforms can appear to be similar, when studied in the time domain, but a frequency domain analysis immediately indicates major differences in their spectra.

Under normal operating conditions the induction motor has a sine-wave drive. If it is assumed that this is an optimum drive condition then the harmonic content of the P.W.M. waveform can be seen to be an important parameter in determining operational performance. Further, the amplitude, frequency (or frequency ratio) and phase of the harmonics will set the resultant pulsating torques, their level, direction and stability.

In an effort to reduce the harmonic content multi-voltage-level P.W.M. waveforms [44] have been proposed for use in motor drives. However, practical constraints generally limit engineered systems to the use of two-level waveforms, although, three-level waveforms are occasionally utilized. When using two-level P.W.M. drives it is important to have a three-wire connection to the three-phase motor since a four-wire system, which would include a neutral return would radically alter the characteristics of the drive. All harmonics present in the P.W.M. signal would be provided with a return path, hence current flow is obtained at all frequencies. In the three-wire system, in the absence of a neutral connection, harmonic current flow,

MIXER

MODULATION SIGNAL — CARRIER

OUTPUT

COMMUNICATIONS MODULATOR

COMPARATOR

MODULATION SIGNAL — CARRIER

TWO-LEVEL

PWM OUTPUT

POWER MODULATOR

(a)

THREE PHASE MODULATION SIGNAL ϕ_2 ϕ_1 ϕ_3

SINGLE PHASE CARRIER

THREE PHASE OUTPUT

ϕ_1 ϕ_2 ϕ_3

SINGLE PHASE MODULATION SIGNAL

THREE PHASE CARRIER

ϕ_1 ϕ_2 ϕ_3

THREE PHASE OUTPUT

ϕ_1 ϕ_2 ϕ_3
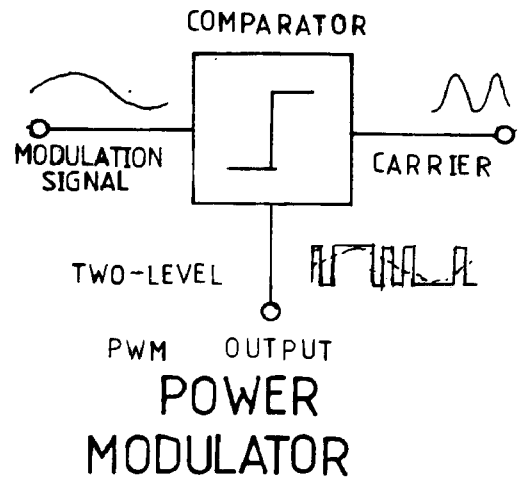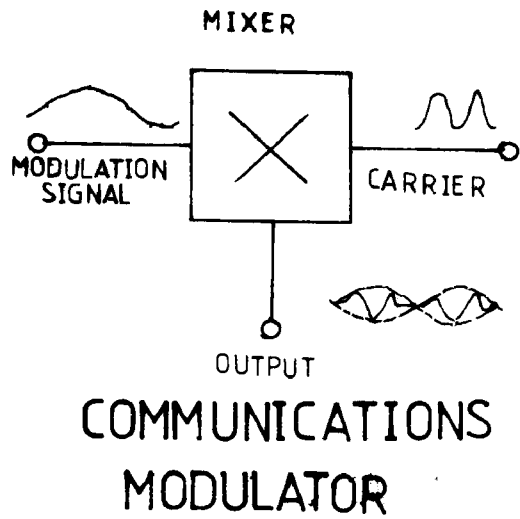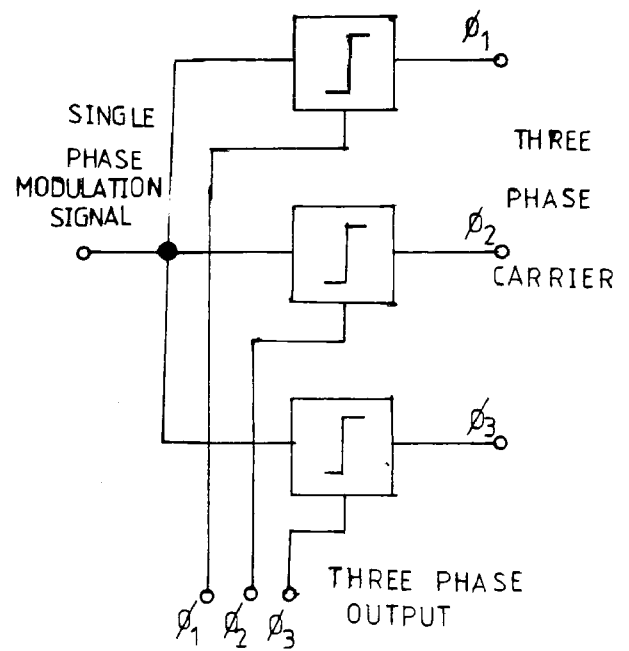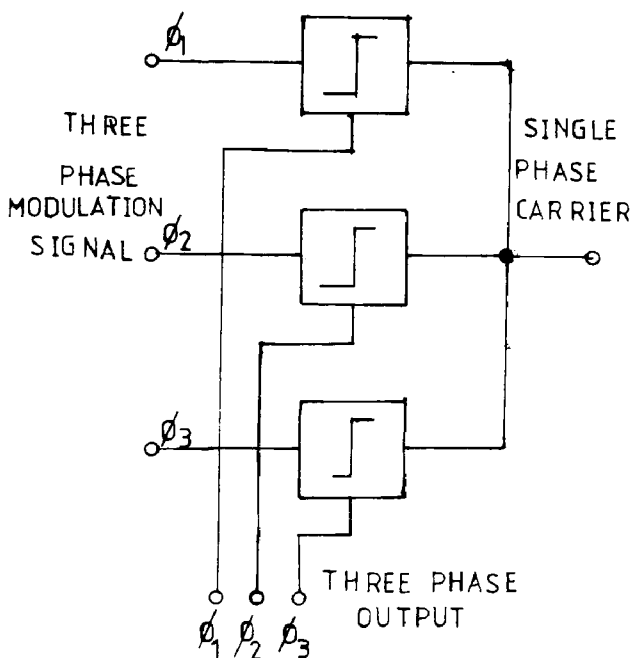
(b)THREE PHASE PWM GENERATION—TWO METHODS

TRIANGLE

SINE

TRAPEZOID

STEP-SINE

RECTIFIED-SINE

OUTPUT

TRIANGLE

SAWTOOTH

TRAPEZOID

SINE

SQUARE-WAVE MODULATED TRIANGLE
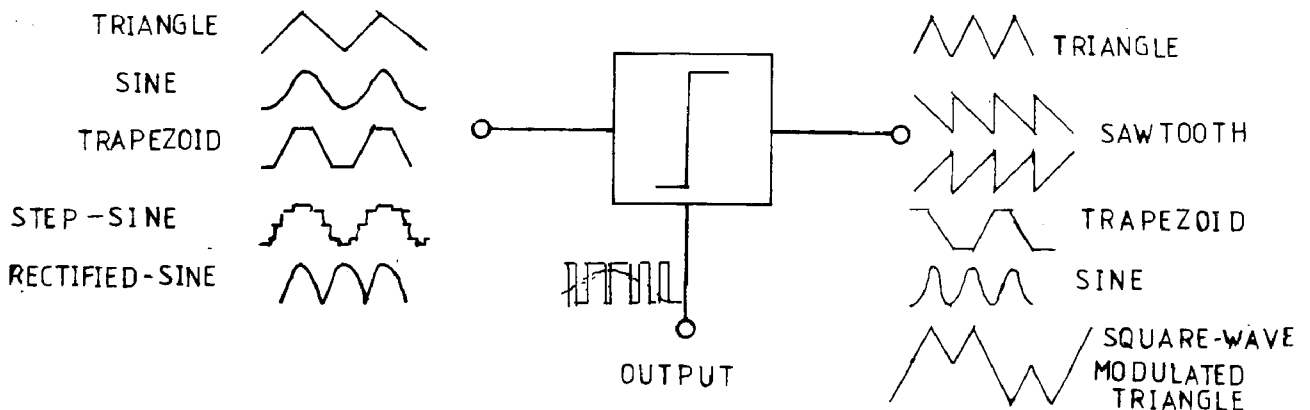
(c)EXAMPLES OF MODULATING SIGNALS

FIG 1-10

- 41 -

only occurs when there is an amplitude and/or phase difference between the harmonics in the three-phase P.W.M. waveforms. It is to be noted that triple harmonics can actually be cancelled in this technique [45], when triple integer frequency ratios are utilized. It is the two-level P.W.M. waveform which is considered for further research.

1.5.2 PWM Generation Systems

The analogue system of P.W.M. generation employs a carrier signal and modulating signal applied as the two inputs to a comparator, the resultant P.W.M. output being used as the power drive reference signal. Figure 1.10(b).

For three-phase systems, many techniques utilise a three-phase modulating signal as the reference and this is the approach adopted in the practical implementation to be described. Even with these limitations there are still a great many alternative techniques of P.W.M. generation, made possible by the variations of the waveshape of the carrier and modulating signals. Each system will produce unique frequency spectra complicated by the fact that the spectrum will change when the amplitude of the modulating wave (i.e. the modulation index) is changed.

As indicated in Figure 1.10(c), various signals can be used as the modulation signal, these include the use of a symmetrical triangular waveform, a full-wave rectified A.C. waveform, a trapezoidal waveform or a stepped sine waveform. The carrier signal can be a sawtooth waveform with a vertical trailing or leading edge, a sinusoidal waveform, a symmetrical triangular waveform or a

square-wave modulated triangular waveform synchronised to the modulation signal. Many other types of waveform can also be included.

When comparing modulation techniques using a triangular carrier with sinusoid modulation, a sawtooth carrier with sinusoid modulation, a triangular carrier with triangular modulation and a sinusoid carrier with sinusoid modulation, Takahashi [16] concluded that the harmonic content of the P.W.M. waveform is minimised when the carrier wave is triangular and the signal wave is purely sinusoidal.

Further, when a sinusoidal carrier and signal wave is employed, a non-linear relationship is induced between the amplitude of the signal wave (or modulation index) and the amplitude of the fundamental frequency in the P.W.M. output [46]. Also the symmetric triangular carrier wave is the most effective in suppressing low order harmonic amplitudes, whereas, the sawtooth reference introduces particular harmonic components which never appear in other schemes. Stepped sinewaves have also been employed as modulating signals, although the distortion introduced has been shown to be greater than the sine/triangle scheme [47]. However, this particular type of sampling has been widely used in communication systems. The reasons for its wide acceptance in communications are not clearly defined, the literature available suggest that its acceptance might have been influenced by two factors :-

1. it satisfies the basic sampling theorem and

2. it is argued that it provides an improved signal to noise ratio when compared with natural sampling.

The previously mentioned techniques of regular sampling did not include the synchronisation of the samples of the modulating wave to the apices of the triangular carrier wave. It may be possible that this was the fundamental cause of the distortion rather than the introduction of regular sampling itself. Therefore, it was thought that the application of regular sampling techniques to P.W.M. power convertors might provide a means of improving the harmonic spectra. The application of the regular sampling process to the generation of P.W.M. waveforms, basically entails the sampling of the modulating wave prior to comparison with the carrier wave (Figure 1.11). Samples of the modulating wave are taken at regular intervals by means of the sampling switch, and are then held constant over the sampling period by storing the samples on a capacitor. This converts the modulating wave to its regular sampled version which is then compared with the carrier wave to produce the switching instants of the width modulated pulses. It can be shown that the generation of the regular sampled modulating wave is achieved at a cost of only four extra components. This point is of considerable significance since the capital cost of the P.W.M. convertor must be kept to a minimum if it is to compete with prior-art systems.

1.5.3 Regular Sampled Asymmetrical-Double-Edge Modulation

Although there are numerous forms of asymmetrical double-edge modulation the form referred to throughout this thesis as 'asymmetrical' is dependent upon regular sampling at twice the carrier frequency and the comparison of the regular sampled modulating wave with an isosceles triangular carrier wave. This type of
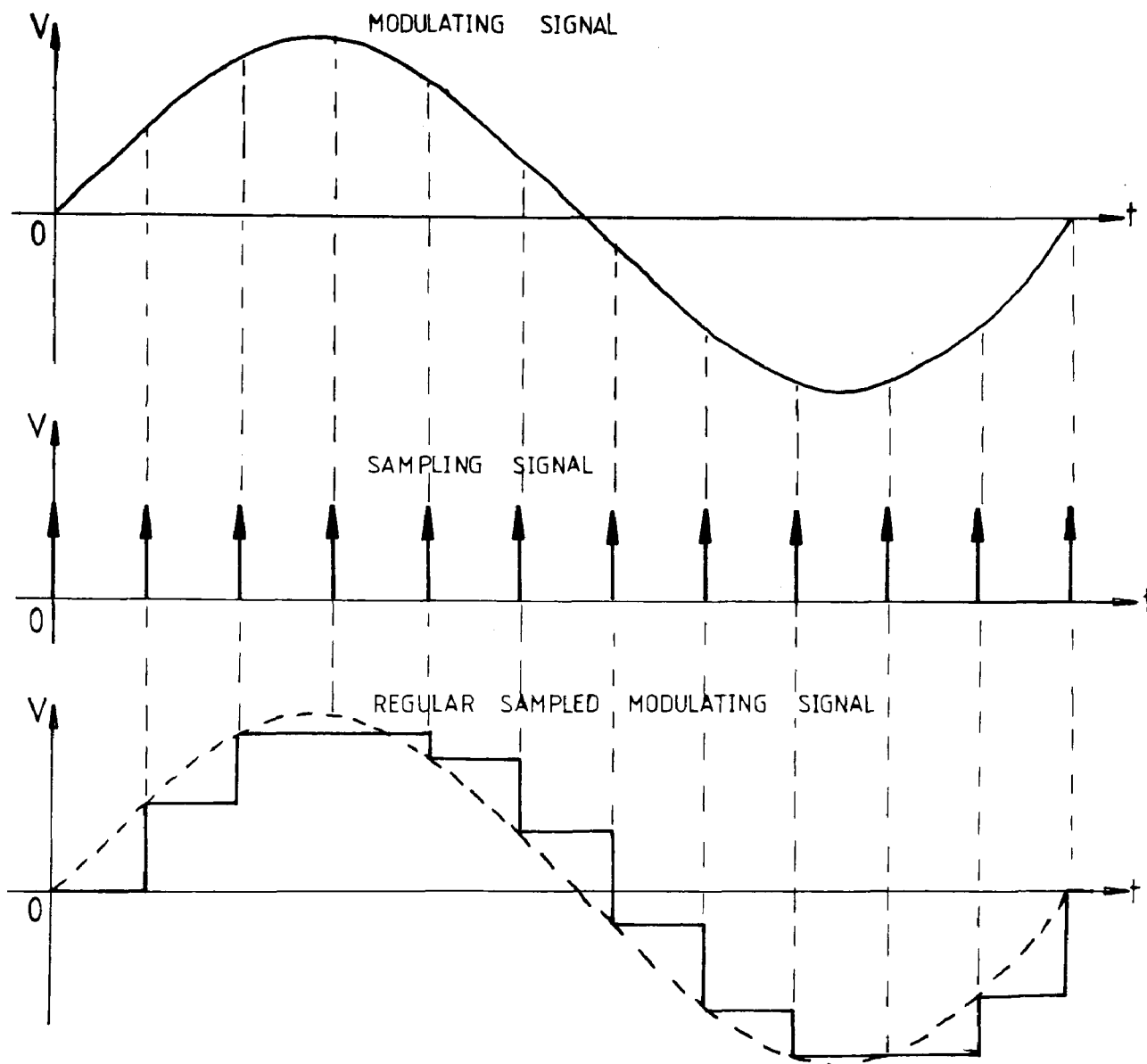
GENERATION OF REGULAR SAMPLED MODULATING SIGNAL

FIG 1-11

pulse-width-modulation is illustrated in Figure (1.12), and it is immediately apparent that both edges of the width-modulated-pulses are modulated by different amounts. The amount of modulation of both edges of each pulse is dependent upon the magnitude of the respective adjacent samples taken at regular intervals corresponding to the positive and negative apices of the isosceles-triangular carrier wave. It can also be seen that a time-phase displacement again exists between the sampling instants and switching instants. It will be shown in this thesis that this regular sampled asymmetrical-double-edge P.W.M. process which is entirely novel, is superior to existing P.W.M. processes in power convertors.

1.5.4 Limitations of the Regular Sampling Process in P.W.M. Systems

It is essential to the analogue method of generating pulse-width-modulated waveforms, that only one pulse per cycle of the carrier wave occurs. For this condition to be satisfied two requirements must be met :

1. each slope of the carrier wave must not be intersected by more than one held sample of the modulating wave and

2. the modulating wave must be sampled at a rate greater than twice the frequency of the modulating wave when the wave is a sinusoid.

Therefore, when the modulating wave is sampled at the carrier frequency or at a multiple of the carrier frequency the above requirements impose limitations on the minimum value of the ratio of carrier frequency to modulating frequency. It can be seen that for

CARRIER WAVE   REGULAR SAMPLED MODULATING WAVE

MODULATING WAVE

SAMPLING INSTANTS FOR MODULATING WAVE

SWITCHING INSTANTS OF COMPARATOR

PULSE WIDTH MODULATED OUTPUT FROM COMPARATOR
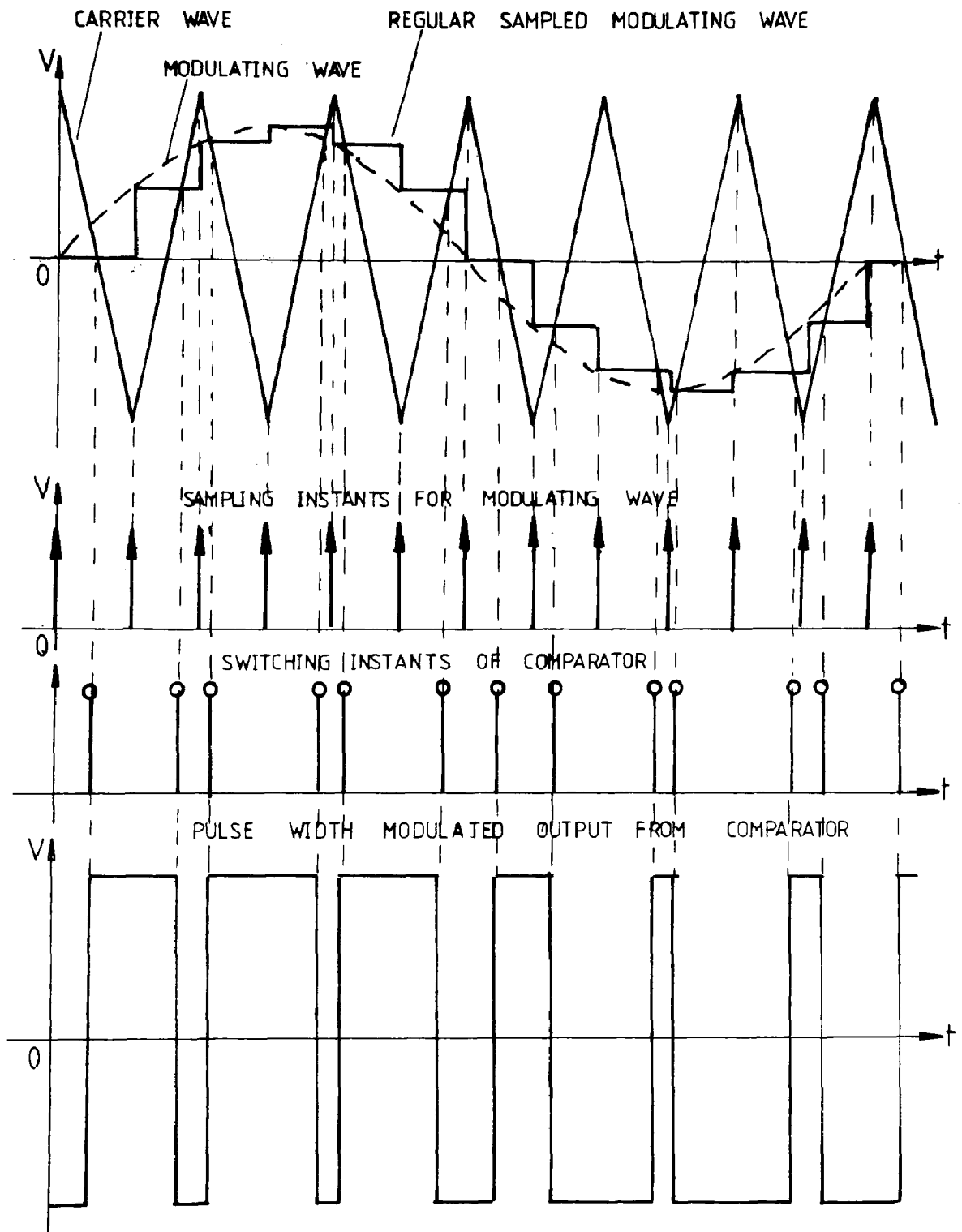
THE MODULATION PROCESS

FIG1-12

asymmetrical-double-edge modulation, the minimum value of frequency ratio must be greater than 'one' ($fc/f_m > 1$). Therefore, on account of the requirements of the regular sampled P.W.M. process alone, it is apparent that the asymmetrical-double-edge system is superior to other forms [48] when the main objective is to operate with a frequency ratio as low as possible.

1.6. Interim Conclusions

A brief historical background to the development of variable speed drives for induction motors has been presented. In particular the technique of frequency changing, in order to achieve induction motor speed control, has been reviewed. Further, a survey of modern, thyristor controlled, frequency changing variable speed units has been conducted.

The fundamental rules of frequency changing have been established, and it has been shown that all power inverters are basically pulse modulators. The various pulse modulation processes have been analysed, and it is shown that the P.W.M. process is most suited to power modulators.

An investigation into the theoretical possibilities of pulse modulation, with respect to obtaining variable frequency, variable voltage sources, has been concluded. Of the techniques considered, the P.W.M. technique appears to hold most promise for the future design of wide range variable frequency/voltage units. P.W.M. can be achieved utilizing many different techniques, each of which will produce a unique set of spectra. In turn, these waveforms will have

different properties when utilized in powering induction motors. Possible optimum techniques of P.W.M. generation have been considered and identified. A novel techique using stepped sinewaves, each individual step being synchronised to an apex of a triangular waveform has been presented. The resulting double-edge-modulated P.W.M. waveform has fewer harmonics than the single-edge-modulated waveform.

CHAPTER 2   WAVEFORM ANALYSIS OF PWM SIGNALS

2.1   Waveform Analysis

Waveform analysis is an important aspect of any investigation into PWM motor drives. The harmonics present in a PWM waveform can produce major motor drive problems - large eddycurrent losses, torque pulsations and sub-harmonic rotational torques[49]. A knowledge of the amplitude, phase and frequency of the harmonics is essential for effecting assessments of motor operation and system performance. As already noted the PWM waveforms can appear to be similar, when studied in the time domain, but a frequency domain analysis immediately indicates major differences in their spectra.

Under normal operating conditions the induction motor has a sine-wave drive. If it is assumed that this is an optimum drive condition then the harmonic content of the PWM waveform can be seen to be an important parameter in determining operational performance. Further, the amplitude frequency (or frequency ratio) and phase of the harmonics will set the resultant pulsating torques, their level, direction and stability. Bennet[8] used a double Fourier Series technique in two variables, to analyse PWM waveforms. This analysis was extended and simplified by Black [4] and remained in a generalised form covering the area where no rational relationship exists between the modulating frequency and the carrier frequency.

Where a rational relationship exists, a simplified single Fourier Series approach can be used for the expression of the modulation products [9]. The technique involves the development of a general

expression for the harmonic content of the waveform, recognising standard forms, and introducing the Bessel substitution to provide a simplified formula.

In both cases the generic harmonic is evaluated by over-lapping partial spectra and it has been found time consuming to compare different modulation processes. Alternative analyses [16,50] develop the equation by first determining the switching instants of the output PWM waveform, and then introducing an equivalent Bessel Function Series, before further development of the overall expression for the frequency spectrum of the signal. This approach, coupled with the fact that only integer frequency ratios are considered, allows faster computation of the spectra so that differing methods of PWM generation can be more easily compared. Although the results are not directly applicable to non-integer frequency ratios a limit procedure can be implemented to overcome this point.

Balestrino[51] expresses the equation for the switching instants directly, in terms of a Kapteyn series of Bessel functions, avoiding the need to repetitively determine switching instants, using Newton's recursive formula.

The Kapteyn series is then substituted into the Fourier equation representing the periodic output waveform. The resulting expression can be implemented using a computer program in order that the modulation products may be determined. It is claimed to be much faster in calculating the amplitudes of the harmonic spectra (10 seconds in computation).

Other simplified approaches [52] also assume integer frequency ratios although the Kapteyn series is not used. The formula for the switching instants is substituted into the Fourier series and it is only after this has been completed that the whole expression is then expanded in terms of the Jacobi Bessel series. This approach also allows fast computation of the spectra. An example of this approach is given in this chapter - all of these analyses relate to the sinusoid/triangle technique of PWM generation.

2.2   Frequency Domain Analysis of a Two Level P.W.M.   Waveform

This analysis illustrates an approximate, simple technique for the evaluation of a PWM wave, which has been found to provide computed spectra values accurate to 0.01% even when the frequency ratio of the carrier signal and modulating signal is non-integer and less than three. [50]

Consider a triangular wave Vc(t) and a modulating wave Vm(t), applied as the two inputs to the comparator, producing an output PWM waveform Vp(t). If it is assumed that the time origin is as shown in the diagram, Figure 2-1, and that the carrier to modulating signal frequency ratio R, is infinite, that is Vm(t) is a D.C. signal of amplitude Vm, then the output pulse waveform will be periodic and will be as indicated.

If the D.C. modulation signal is set above the positive apices of the triangular waveform then the ouput from the comparator will be a constant D.C. level of +Va volts. If the D.C. modulation is set such that $-Vm < -Vc$ then the output will be a constant negative
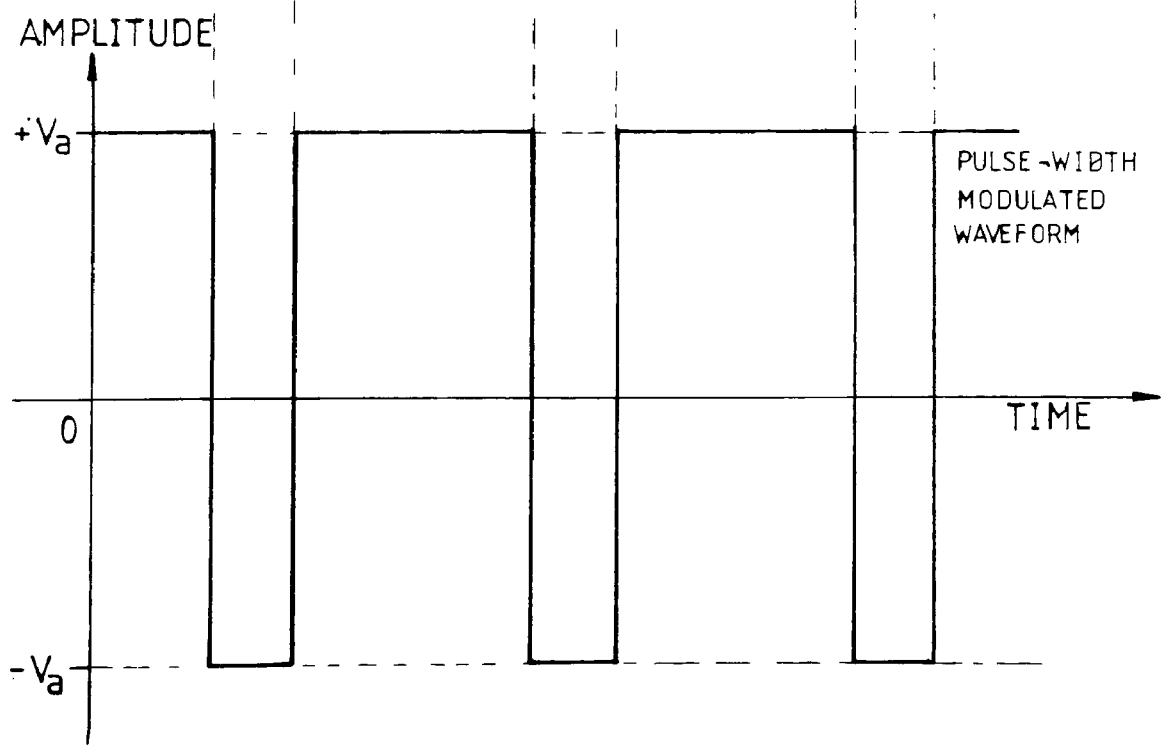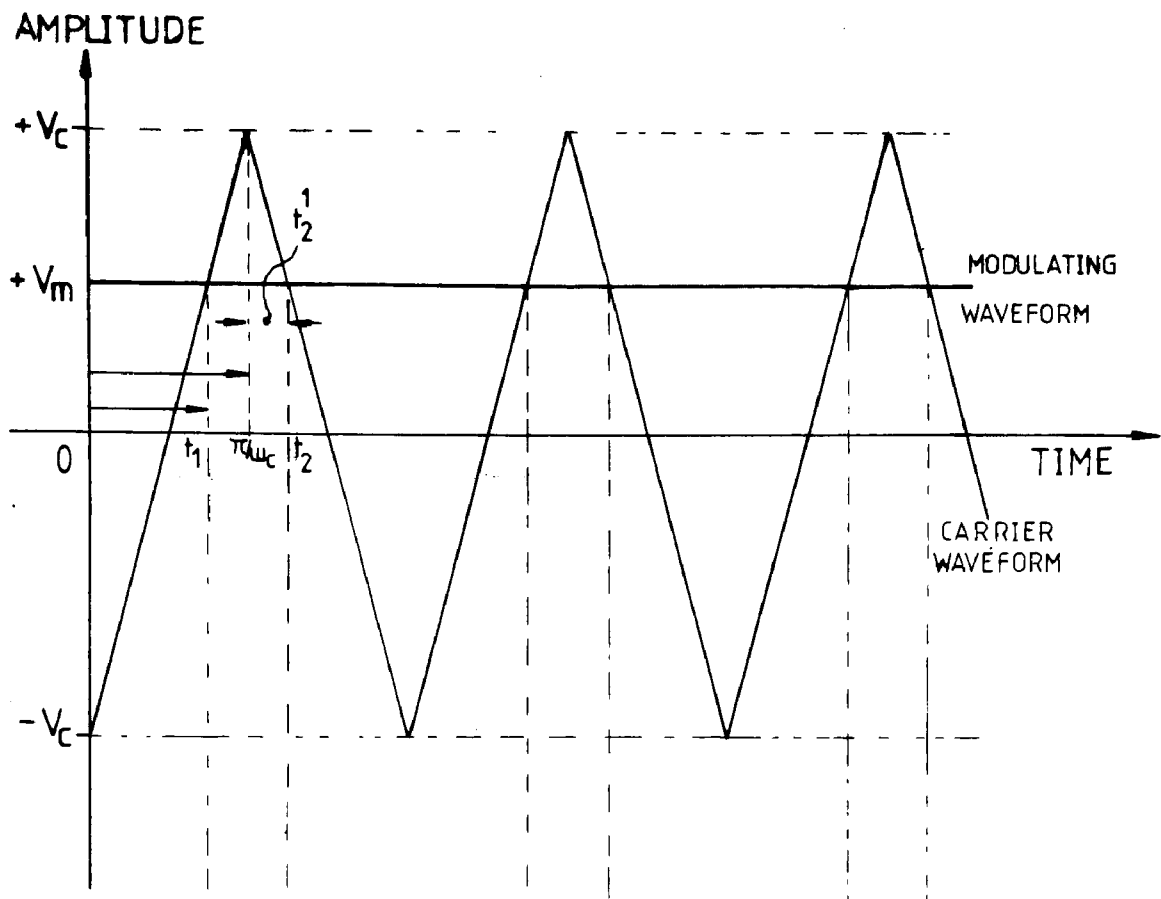
FIG 2-1

voltage -Va. The following analysis applies for modulation levels between these two extremes.

In reference to Figure 2-1

Solving for t_1

$$V_m = V_c \left(\frac{2\omega_c}{\pi} t_1 - 1 \right) \qquad 0 \leqslant t \leqslant \frac{\pi}{\omega_c}$$

$$\frac{V_m}{V_c} = \frac{2\omega_c}{\pi} \cdot t_1 - 1$$

$$t_1 = \frac{\pi}{2\omega_c} \cdot (M_i + 1) \qquad \text{(where the Modulation Index} = M_i = \frac{V_m}{V_c})$$

$$\tag{1}$$

Further for t_2^1, with $\frac{\pi}{\omega_c}$ as the time origin :-

$$V_m = V_c \cdot \left(1 - \frac{2\omega_c\, t_2^1}{\pi} \right)$$

$$\frac{V_m}{V_c} = 1 - \frac{2\omega_c\, t_2^1}{\pi}$$

$$\therefore \ t_2^1 = (1 - M_i) \cdot \frac{\pi}{2\omega_c}$$

Now $t_2 = \frac{\pi}{\omega_c} + t_2^1$

hence $t_2 = \frac{\pi}{\omega_c} + (1 - M_i) \cdot \frac{\pi}{\omega_c} = (3 - M_i) \frac{\pi}{\omega_c}$

$$\tag{2}$$

With the time origin as shown the sinusoidal components of the Fourier expansion of the waveform will be zero. Hence the co-sinusoidal components will be given by :-

$$a_n = \frac{\omega_c}{\pi} \int_0^{\frac{2\pi}{\omega_c}} f(t) \, \text{Cos} \, n\omega_c t \, dt$$

$$= \frac{\omega_c}{\pi} \left[\int_0^{(M_i+1)\frac{\pi}{2\omega_c}} V_A \, \text{Cos} \, n\omega_c t \, dt - \int_{(M_i+1)\frac{\pi}{2\omega_c}}^{(3-M_i)\frac{\pi}{2\omega_c}} V_A \, \text{Cos} \, n\omega_c t \, dt + \int_{(3-M_i)\frac{\pi}{2\omega_c}}^{\frac{2\pi}{\omega_c}} V_A \, \text{Cos} \, n\omega_c t \, dt \right]$$

$$= \frac{\omega_c V_A}{n\omega_c \pi} \left[\text{Sin}[n\omega_c \frac{\pi}{2\omega_c} (M_i + 1)] - 0 - \text{Sin}[n\omega_c \frac{\pi}{2\omega_c} (3 - M_i)] + \right.$$

$$\text{Sin}[n\omega_c \frac{\pi}{2\omega_c} (M_i + 1)] + \text{Sin}[n\omega_c \frac{2\pi}{\omega_c}] -$$

$$\left. \text{Sin}[n\omega_c \frac{\pi}{2\omega_c} (3 - M_i)] \right]$$

$$= \frac{2V_a}{n\pi} \left[\text{Sin}[\frac{n\pi}{2} (M_i + 1)] - \text{Sin}[\frac{n\pi}{2} (3 - M_i)] \right]$$

$$= \frac{2V_a}{n\pi} \left[2 \, \text{Cos} \, n\pi \, \text{Sin}[(M_i - 1) \frac{n\pi}{2}] \right]$$

Expanding :-

$$= \frac{4V_a}{n\pi} \, \text{Cos} \, n\pi \left[\text{Sin}(\frac{n\pi}{2} . M_i) \right] \text{Cos} \frac{n\pi}{2} - \text{Cos}(\frac{n\pi}{2} M_i) \, \text{Sin} \frac{n\pi}{2} \right]$$

$$= \frac{4V_a}{n\pi} \left[\text{Sin}(\frac{n\pi M_i}{2}) (\text{Cos} \frac{3n\pi}{2} + \text{Cos} \frac{n\pi}{2}) \cdot \frac{1}{2} - \text{Cos}(\frac{n\pi M_i}{2}) \right.$$

$$\left. \cdot \frac{1}{2} (\text{Sin} \frac{3\pi n}{2} - \text{Sin} \frac{n\pi}{2}) \right]$$

For n odd -

$$a_n = -\frac{4V_a}{n\pi} \cdot \text{Cos} \left(\frac{n\pi M_i}{2}\right) \cdot \left(\text{Sin} \frac{3\pi n}{2} - \text{Sin} \frac{n\pi}{2}\right) \cdot \frac{1}{2}$$

$$a_{2n-1} = (-1)^{(n+1)} \frac{4V_a}{(2n-1)\pi} \cdot \text{Cos} \left[(2n-1)\frac{\pi M_i}{2}\right], \quad n = 1 \to \infty$$

$$\tag{3}$$

and for n even :-

$$a_n = \frac{4V_a}{n\pi} \cdot \text{Sin} \left(\frac{n\pi M_i}{2}\right) \left(\text{Cos} \frac{3\pi n}{2} + \text{Cos} \frac{n\pi}{2}\right) \frac{1}{2}$$

$$a_{2n} = (-1)^n \frac{2 V_a}{n\pi} \cdot \text{Sin} \, n\pi M_i \qquad n = 1 \to \infty \tag{4}$$

$$a_0 = \frac{1}{T} \int_o^T f(t) \, dt = \frac{1}{T_c} \left[\int_0^{(M_i+1)\frac{\pi}{2\omega_c}} V_a \, dt - \int_{(M_i+1)\frac{\pi}{\omega_c}}^{(3-M_i)\frac{\pi}{2\omega_c}} V_a \, dt + \int_{(3-M_i)\frac{\pi}{2\omega_c}}^{\frac{2\pi}{\omega_c}} V_a \, dt \right]$$

$$= \frac{2\pi V_a}{\omega_c T_c} \left[\frac{(M_i+1)}{2} - 0 - \frac{(3-M_i)}{2} + \frac{(M_i+1)}{2} + 2 - \frac{(3-M_i)}{2} \right]$$

$$= V_a \quad [2 M_i]$$

i.e. $\quad \frac{1}{2} a_0 = M_i V_a$

giving :- $\quad V_p(t) = M_i V_a + \sum_{n=1}^{\infty} a_n \text{Cos} \, n\omega_c t \tag{5}$

where :-

a_n is given by (3) and (4).

If it is now considered that the modulation index varies consinusoidally, such that $M_i(t) = M_i \cos(\theta+\Phi)$ and the frequency ratio, R, becomes finite such that $\omega_c = R\omega_m$ then $\theta = \omega_m t$, M_i = Peak value of modulation index and Φ = the phase shift of the modulating waveforms relative to the origin, substituting in equations (3) and (4).

For n odd,

$$a_{2n-1} = (-1)^{(n+1)} \frac{4 V_a \cdot \cos}{(2n-1)\pi} [(2n-1) \cdot \frac{\pi}{2} \cdot M_i \cos(\theta+\phi)] \quad (6)$$
$$n = 1 \to \infty$$

For even values :

$$a_{2n} = (-1)^n \frac{2 V_a}{n\pi} \sin(n\pi M_i \cdot \cos(\theta+\phi)) \quad (7)$$
$$n = 1 \to \infty$$

Expressions such as $\cos(\chi \cos\beta)$ and $\sin(\chi\sin\beta)$ can be expanded in terms of Bessel functions of the first kind giving :-

$$\cos(\chi_{2n-1} \cdot \cos(\theta+\phi)) = J_0(\chi_{2n-1}) - 2J_2(\chi_{2n-1})\cos 2(\theta+\phi) +$$

$$2 J_4(\chi_{2n-1})\cos 4(\theta+\phi) - \dots$$

$$= J_0(\chi_{2n-1}) + \sum_{\kappa=1}^{\infty} (-1)^\kappa 2J_{2\kappa}(\chi_{2n-1})\cos(2\kappa(\theta+\phi))$$

$$- (8)$$

where $\chi_{2n-1} = \dfrac{(2n-1)\pi M_i}{2}$

Further :-

$$\text{Sin } (\chi_{2n}.\text{Cos } (\theta+\phi)) = 2 J_1 (\chi_{2n}) \text{ Cos } (\theta+\phi) - 2 J_3 (\chi_{2n}) \text{ Cos } 3 (\theta+\phi)$$

$$+ 2 J_5 (\chi_{2n}) \text{ Cos } 5 (\theta+\phi) - \ldots$$

$$= \sum_{\kappa = 1}^{\infty} (-1)^{\kappa+1} 2.J_{2\kappa-1} (\chi_{2n}) \text{ Cos}((2\kappa-1).(\theta+\phi)) \tag{9}$$

where $\chi_{2n} = n\pi M_i$.

Substituting (8) and (9) in (6) and (7), then in (5)

$$V_p(t) = M_i V_a \text{ Cos } (\theta+\phi) + \sum_{n=1}^{\infty} (-1)^{n+1} \frac{4V_a}{(2n-1)\pi} \left[J_0 (\chi_{2n-1}) + \sum_{\kappa=1}^{\infty} (-1)^{\kappa} 2 J_{2\kappa}.\right.$$

$$\left. (\chi_{2n-1}).\text{Cos } (2\kappa(\theta+\phi)) \right] \text{ Cos } (2n-1)\omega_c t$$

$$+ \sum_{n=1}^{\infty} (-1)^{n} \frac{2V_a}{n\pi} \left[\sum_{\kappa=1}^{\infty} (-1)^{\kappa+1} 2.J_{2\kappa-1} (\chi_{2n})\text{Cos } ((2\kappa-1) (\theta+\phi)) \right] \text{Cos} 2n\omega_c t \tag{10}$$

General expressions for the computation of the amplitude and phase of the spectral harmonic frequencies can be given as follows : Let F_{κ_n} be the κth sideband associated with the nth harmonic of the output P.W.M. frequency spectrum, then :-

For **odd** frequency components :-

The $(2n-1)^{th}$ harmonic itself (that is the carrier harmonics) are given by :-

$$F_{o(2n-1)} = (-1)^{(n+1)} \frac{4V_a}{(2n-1)\pi} \; J_o \left((2n-1)\frac{\pi M_i}{2}\right) \tag{11}$$

$$n = 1 \to \infty$$

The modulation sidebands of the carrier harmonics will be given by :-

$$F_{K(2n-1)} = (-1)^K (-1)^{n+1} \frac{8V_a}{(2n-1)\pi} \cdot J_{2K} (2n-1) \frac{\pi M_i}{2} \underline{/\pm 2K\phi} \tag{12}$$

THE Kth SIDEBAND — HARMONIC NUMBER   ORDER

$$n = 1 \to \infty$$
$$K = 1 \to \infty$$

For 'even' frequency components :-

$$F_{K(2n)} = (-1)^{K+1} (-1)^n \frac{4V_a}{n\pi} \; J_{2K-1} (n\pi M_i) \underline{\pm/(2K-1)\phi} \tag{13}$$

ORDER   ARGUMENT

$$n = 1 \to \infty$$
$$K = 1 \to \infty$$

Thus :-

1. The fundamental control frequency is given by

$$F_F = M_i \, V_a \, Cos \, (\theta + \Phi)$$

2. For the odd carrier frequency components :-

The $(2n-1)^{th}$ harmonic itself is given by :-

$$F_O \ (2n-1) = (-1)^{(n+1)} \ \frac{4V_a}{(2n-1)\pi} \ J_O \ ((2n-1)\frac{\pi M_i}{2})$$

$$n = 1 \rightarrow \infty$$

and the modulation sidebands will be given by

$$F_K(2n-1) = (-1)^K (-1)^{(n+1)} \ \frac{8Va}{(2n-1)\pi} \ J_{2K} \ ((2n-1)\frac{\pi M_i}{2}) \ \angle \pm 2K\phi$$

$$n = 1 \rightarrow \infty, \quad K = 1 \rightarrow \infty$$

3. For the even carrier frequency components, the harmonic itself and its modulation sidebands will be given by :-

$$F_{K(2n)} = (-1)^{K+1} (-1)^n \ \frac{4Va}{n\pi} \ J_{2K-1} \ (n\pi M_i) \ \angle \pm (2K-1)\phi$$

$$n = 1 \rightarrow \infty$$

$$K = 1 \rightarrow \infty$$

A computer program, written in basic for the P.E.T. microcomputer and which calculates the harmonics from the above formulae, is given in the appendix. It is to be noted that although the formulae imply that the frequency spectra of the waveform is independent of the frequency ratio, in further computation of the spectra, due account must be taken of the fact that the sidebands overlap each other. It is at this point that the frequency ratio is important since the overlapping partial spectra need to be added, algebraicly, to obtain the final value of the particular harmonic being considered.

2.3 Analysis of the Asymmetrical Regular Sampled PWM Waveform

The previous analysis refers only to the PWM waveform generated by the use of the sine/triangle technique. The following analysis is more general in approach in that, provided the PWM waveform can be expressed in time domain terms, the transformation from the time domain to the frequency domain is achieved by using the Discrete Fourier Transform (DFT). The FFT algorithm is used for computing the DFT. In this case it is the Regular Sampled Asymmetric form of PWM which is considered for analysis.

Assumptions

1. The modulating wave is synchronised to the carrier wave such that the triangular modulating wave is at a maximum at the zero start of the sine wave.

2. Amplitude of modulation never exceeds the amplitude of the carrier.

The height of any step, of the sinewave in Figure 2-2, can be desicribed by the equation $h = A \sin \omega t$ where A is the maximum amplitude of sinewave.

$$h = A \sin \left(\frac{(n-1)Tc.2\pi f_m}{2} \right)$$

where n = PWM pulse number

f_m = modulation frequency

and n = 1 to 2R (for a full cycle)

$$h = A \sin \left((n-1) \pi f_m / f_c \right)$$

$$= A \sin \left((n-1)\pi/R \right) \text{ where } R = f_c / f_m$$

- 61 -

FREQUENCY RATIO = $R = T_m / T_c$

MODULATION INDEX = $K = V_m / V_c$

MODULATION WAVEFORMS

PWM OUTPUT
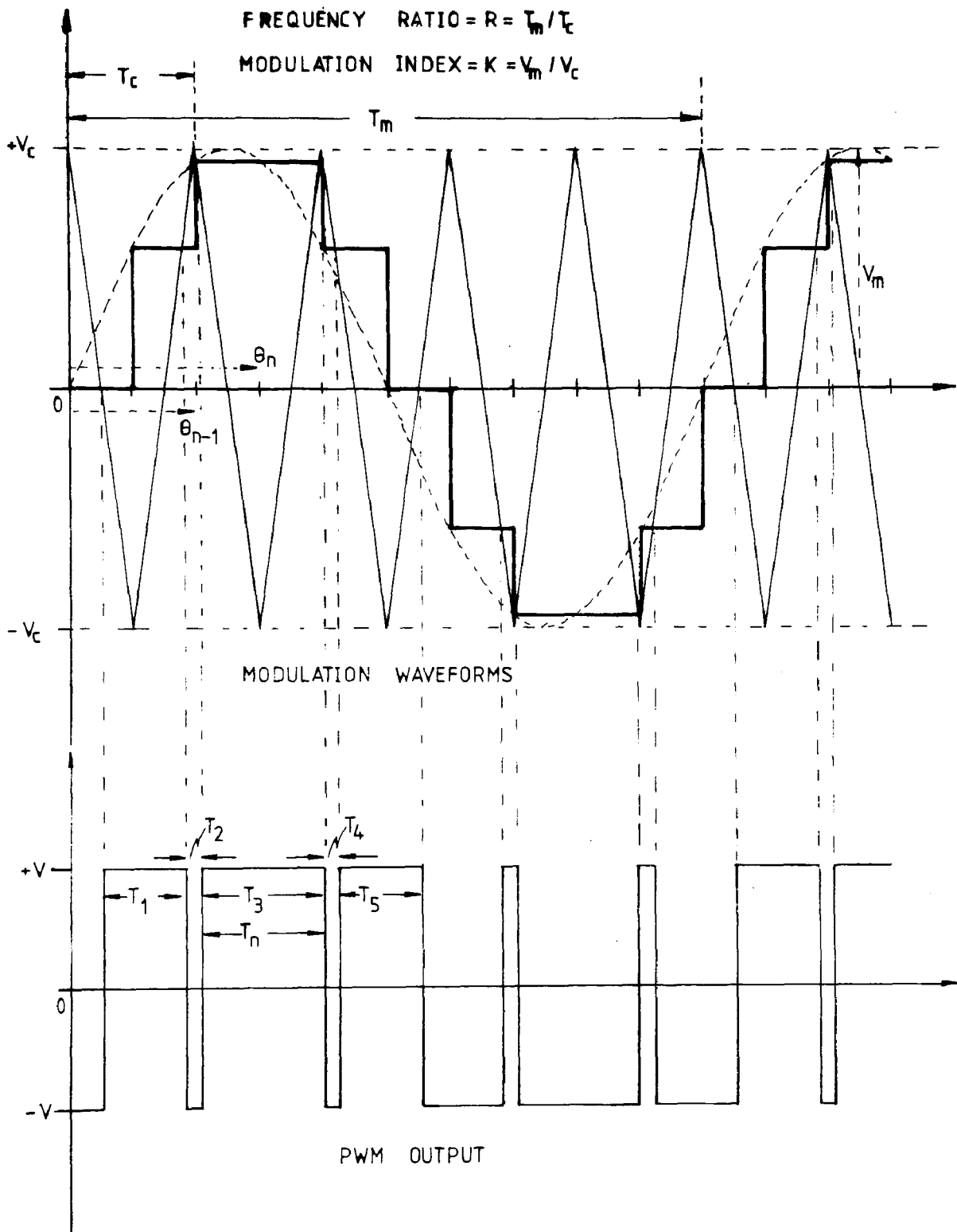
FIG·2-2

For the start time of the positive pulses then the triangular carrier is always sloping downwards so that the height of the triangle is :-

$$h' = (B-\alpha t)$$ $\qquad \alpha = \text{slope}$

$$= B-4B.t/T_c$$ $\qquad B = \text{Maximum Amplitude of triangular wave}$

$$= B(1-4t/T_c)$$

Thus the actual time to the intercept will be given by

$$t_s = (n-1).T_c/2+t_x \quad \text{(ts being the start time of the pulse).}$$

where t_x is given by the condition :-

$$h = h'$$

$$\therefore \ A \sin ((n-1)\pi/R) = B(1-4.t_x/T_c)$$

$$1-4.t_x/T_c = A/B.Sin(\pi(n-1)/R)$$

$$4.t_x/T_c = 1-\kappa \sin (\pi(n-1)/R)$$

$$\text{where } \kappa = \text{modulation index}$$

$$t_x = \frac{T_c}{4} .(1-\kappa\cdot\sin(\pi(n-1)/R))$$

The finish time of the pulse will be given by

$$T_f = \frac{nT_c}{2} + t'_x$$

where t'_x is the time from the start of the upward triangular slope to the intercept of the sine wave and triangular waveform.

$$\text{Amplitude} = B (\alpha t-1)$$

$$= B (4t/T_c-1)$$

Thus t'_x can be determined from :-

$$B(4t'_x/T_c-1) = A\sin(nT_c/2 \cdot 2\pi f_m)$$

$$4t'_x/T_c = 1+A/B.\sin(n\pi/R)$$

$$\therefore t'_x = (1+\kappa\sin(n\pi/R)).T_c/4$$

The pulse width of the nth pulse is thus given by :-

$$t_n = t_f - t_s = \frac{T_c}{4}.(1+\kappa\sin(\pi n/R))+\frac{nT_c}{2}-((n-1)T_c/2+(1-\kappa\sin(\pi(n-1)/R)).T_c/4)$$

$$= \frac{T_c}{2} + (\sin(\pi n/R)+\sin(\pi(n-1)/R)).T_c.\kappa/4$$

$$= \frac{T_c}{2}.(1+\frac{\kappa}{2}(\sin(\pi n/R)+\sin(\pi(n-1)/R))$$

An expression has now been derived for the time domain calculation of the PWM waveform. Thus, if this is now followed with a DFT transformation the required frequency spectra can be determined. The following analysis gives the background to the development of the DFT and FFT from the consideration of the Continuous Fourier Transform through to the development of the Basic Program. Several books and articles have been utilized in order to obtain the analysis sequence.

2.4   The Discrete Fourier Transform

Fourier Series analysis is a well known technique, for representing given periodic time domain functions in terms of the frequency domain. That is the detailed knowledge of a periodic waveform, in terms of its amplitude variation with time, can be utilised such that the same waveform can be described by a set of frequency components whose phase and amplitude are known. This can be determined from the relationship :-

$$f(x) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(nx)+b_n \sin(nx)]$$

where :- $a_0 = \dfrac{1}{2\pi} \cdot \displaystyle\int_{-\pi}^{\pi} f(x)dx$

$a_n = \dfrac{1}{\pi} \displaystyle\int_{-\pi}^{\pi} f(x)\text{Cos}(nx)dx$

and $b_n = \dfrac{1}{\pi} \displaystyle\int_{-\pi}^{\pi} f(x)\text{Sin}(nx)dx$

Practical analogue techniques for the real-time analysis of periodic signals have been based on the above relationship. For example, a Fenlow Analyser, SP4, uses sine and cosine reference signals of the same frequency; the incoming waveform is divided into two channels - one channel multiplies the signal by $\sin\omega$ t whilst the second channel multiplies the signal by $\cos\omega$ t. If both channels are integrated so that only the DC components remain then the combination of the two DC values can be used to determine both the phase and amplitude of the signal, its frequency being the same as that of the two reference waveforms, $\sin\omega$ t and $\cos\omega$ t. This process of multiplication (by $\sin\omega$t and $\cos\omega$t) and integration (utilizing a low pass filter) is the same as that being implemented in the previous formulae.

Now if a digital computer is to be used to implement the same formulae, in the same way, the task would be impossible. This is because the continuous analogue sine and cosine reference signals are made up of an infinite number of samples. That is, if one attempts to simulate the sine and cosine waves, exactly, in a digital form, then one needs to obtain an infinite number of samples of the signals such that the space between samples is negligable. Obviously, it is not possible to store or generate an infinite number of samples on the digital computer. Therefore, in practice, the space between the

samples must be increased so that the number of samples of sin ωt and cos ωt is limited. The process of integration is then achieved by averaging the samples obtained, the amplitude, phase and frequency of the input signal being determined in the same way, as previously outlined for the analogue case.

It can be deduced that because a finite number of samples are used then some error is introduced into the final calculation. Further, the degree of this error will depend on the number of samples being used — the greater the number the smaller the error.

Now, the process of the fourier analysis of periodic waveforms, is in point of fact, a special case of a more general technique of frequency domain analysis — the Continuous Fourier Transform. This technique can also be utilized to analyse waveforms whose nature is not fundamentally periodic.

The Continuous Fourier Transform identifies or distinguishes the different frequency sinusoids (and their respective amplitudes) which combine to shape an arbitrary waveform. It has long been used for characterising linear systems — consider the time function h(t) as shown in Figure 2-3(a).

Now, this function can also be defined by its magnitude/frequency content H(f) as shown in Figure 2-3(b).

The transformation process, from the time domain to the frequency domain, is characterised by the mathematical relationship :-

$$H(f) = \int_{-\infty}^{\infty} h(t) \exp(-j2\pi ft) dt$$

which provides a plot of the relative weight of different frequencies that comprise the given signal. In general, the Fourier Transform is
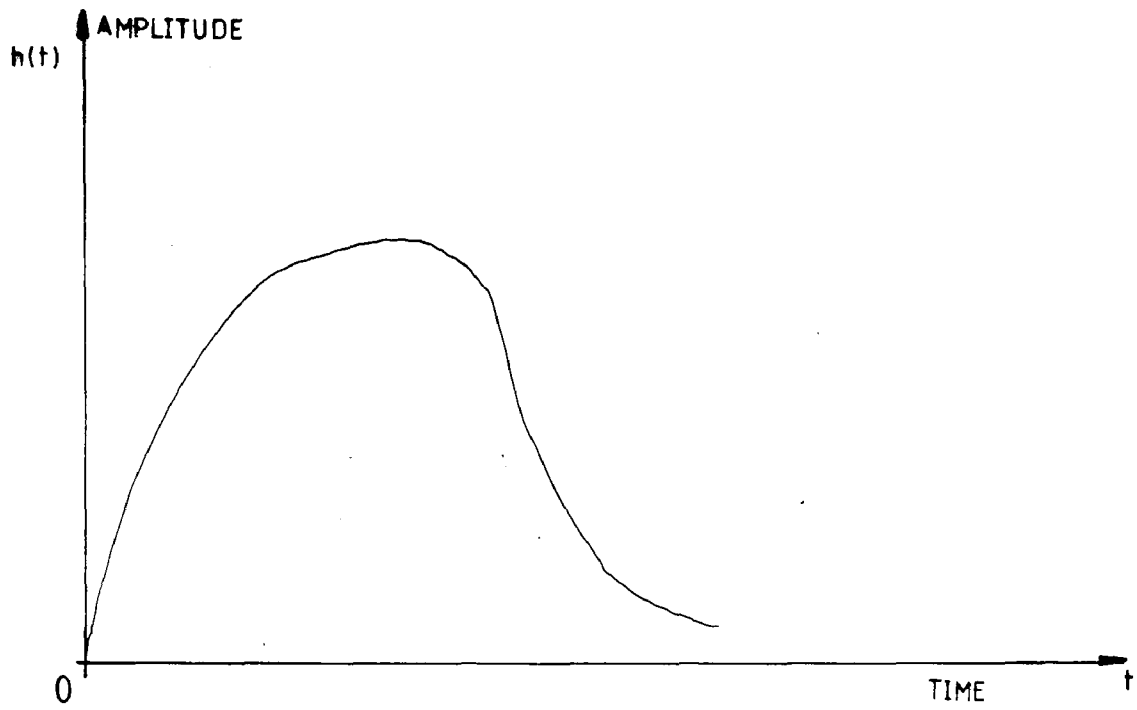
FIG 2-3(a)
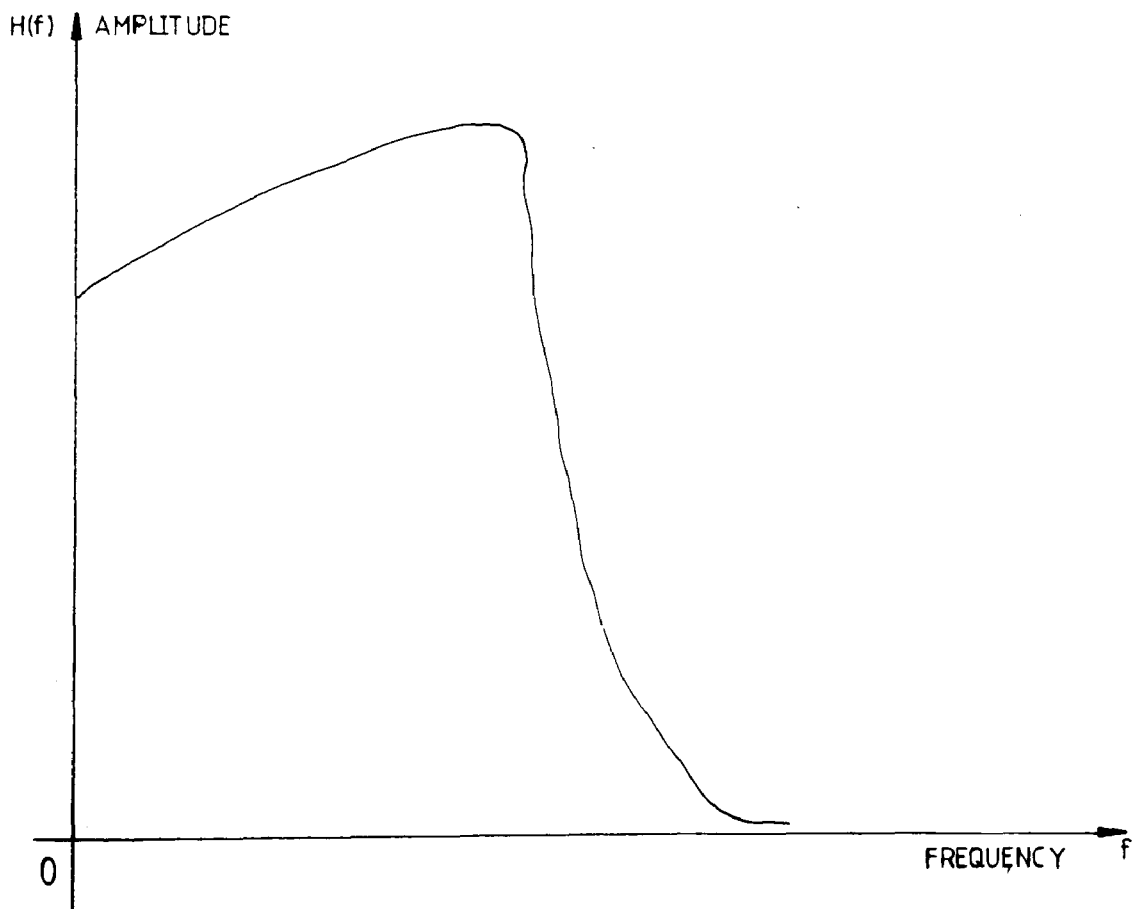
FIG 2-3(b)

a complex quantity

$$H(f) = R(f) + jI(f) = |H(f)| \exp(j\theta(f))$$

where $R(f)$ is the real part of the Fourier Transform, $I(f)$ is the imaginary part of the Fourier Transform, $|H(f)|$ is the amplitude or Fourier Spectrum of $h(t)$ and is given by $\sqrt{(R^2(f) + I^2(f))}$

$\theta(f)$ is the phase angle of the Fourier Transform and is given by $\tan^{-1}[I(f)/R(f)]$.

In order that a practical technique for spectrum analysis (based on this formula) be implemented on the digital computer the Continuous Fourier Transform must be converted to a Discrete Fourier Transform (DFT). This is necessary so that an infinite number of points need not be considered i.e. a limited number of points are considered to give an approximation to the real function. In this way, a practical technique of waveform analysis can be realised on a computer which implies that only a finite number of discrete samples of the time function and frequency spectrum can be considered.

In transferring the transform analysis to a digital computer, numerical integration signifies the relationship

$$H(f_\kappa) = \sum_{i=0}^{N-1} h(t_i) \exp(-j2\pi f\kappa t_i) \cdot (t_{i+1} - t_i)$$
$$\kappa = 0, 1 \ldots \ldots N-1$$

where there are N data points of the time domain function $h(t_i)$.

2.5 The Discrete Fourier Transform (Approximations)

The discussion is confined to periodic signals since this is the area of concern here. Although most of the properties of the continuous Fourier Transform (CFT) are retained, several constraints result from the conditions that the DFT must operate on sampled waveforms over finite intervals. In order to comprehend and anticipate errors in the computation it is necessary to consider the derivation of the DFT.

If the function $h(t)$ is continuous, then a sample of $h(t)$, $\hat{h}(t)$, at time equal to T, can be expressed as

$$\hat{h}(t) = h(t)\delta(t-T) = h(T)\delta(t-T)$$

where $\delta(t-T)$ is an impulse occurring at time $t=T$. The result is an impulse at time T whose amplitude is equal to that of the function $h(t)$ at time $t=T$. If now the function $h(t)$ is considered to be continuous and the sampling function to have an infinite number of impulses, equally spaced in time, $t=T$, the time domain product of the two waveforms can be expressed as

$$\hat{\hat{h}}(t) = \sum_{n=-\infty}^{\infty} h(nT)\delta(t-nT) \quad \text{for } n=0,\pm1, \pm2, \pm3.....$$

This equation describes the series of impulsive samples of the waveform $h(t)$, the resultant amplitudes being equal to the amplitude of $h(t)$ at the points in time, nT, for $n=0,\pm1,\pm2$————Figure 2-4 illustrates, graphically, the sampling concept. The Fourier Transform
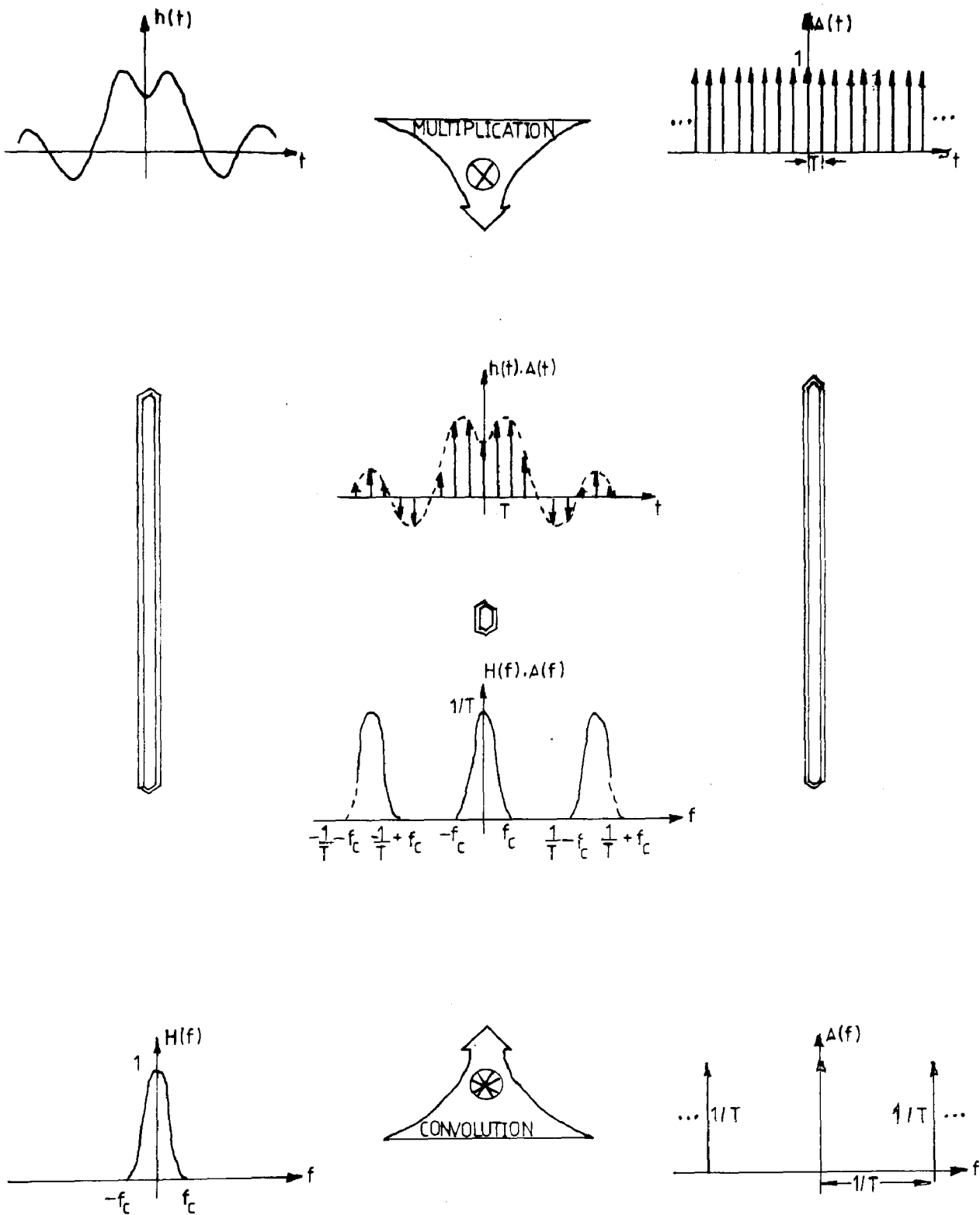
FIG 2-4

(or frequency spectrum) of the waveform can be obtained by using the frequency convolution theorem. That is, multiplication in time domain is equivalent to convolution in the frequency domain, which, in itself, is the Fourier Transform of the product $h(t).x(t)$.

$$h(t).x(t) \Longleftrightarrow H(f)*X(f)$$

Again, the process is illustrated graphically in Figure 2-4. It can be seen that the actual Fourier Transform of the product $\sum_{n=-\infty}^{\infty} h(nT)\delta(t-nT)$ is a periodic function. The required frequency spectrum actually exists within the limits $-1/T+f_c$ and $1/T-f_c$.

where T is the period of the sampling waveform and $\pm f_c$ is the frequency bandwidth of the original signal. It can be seen from Figure 2-5 that if $f_c = 1/T$ then the frequency bands overlap and the above limits reduce to zero. That is the frequency spectrum is now in no way representative of the original function. It is also clear that if $f_c = 2/T$ (that is the sampling period is twice that of the highest frequency of the original spectrum) then the bands do not overlap, Figure 2-6. This is simply an alternative statement of Nyquists criteria that a signal should be sampled at a frequency which is at least twice that of the highest frequency component of the original signal, if it is to be reconstituted with no error.

Thus it can be seen that the first requirement in using the FFT is that the original signal be sampled such that $1/T \geqslant 2f_c$, f_c being the highest frequency component of the waveform. In some cases where the spectrum is large, f_c may have to be limited (by a bandpass filter

- 71 -
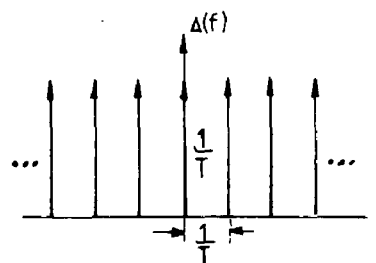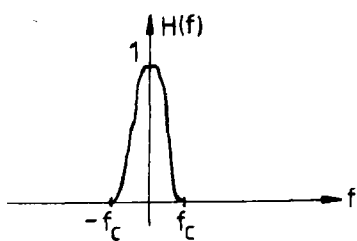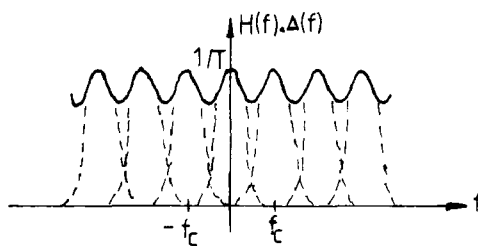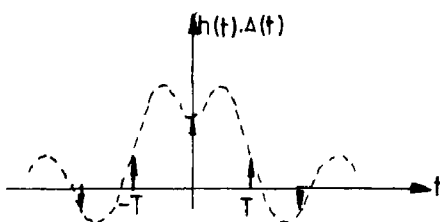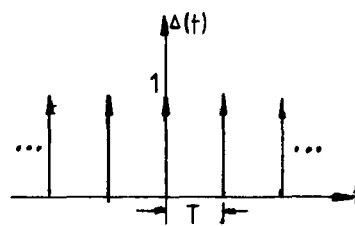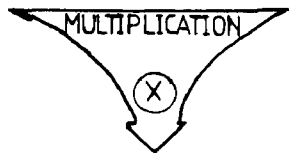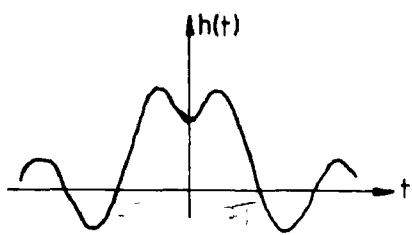
FIG 2-5
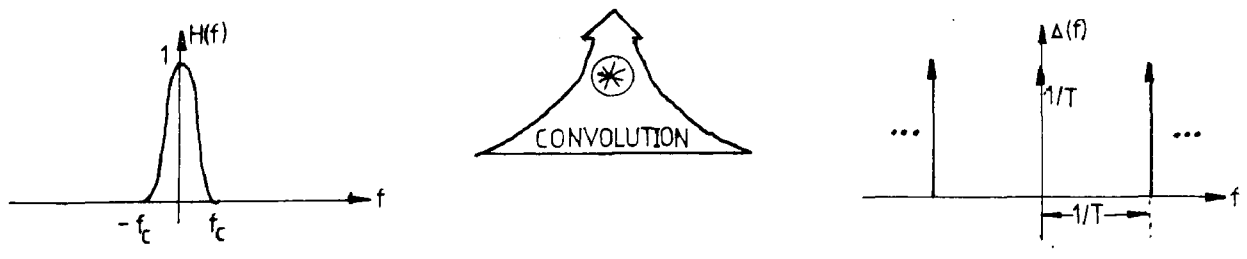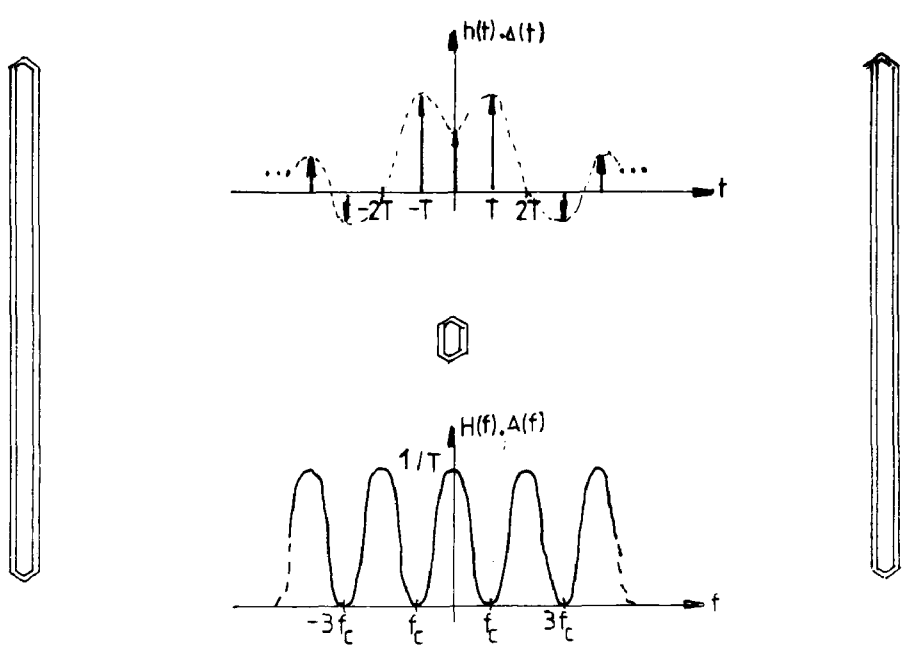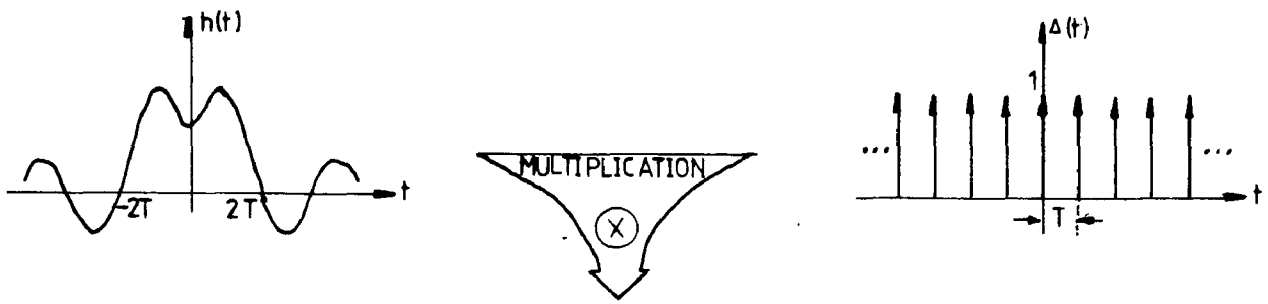
FIG 2-6

for example) however there is an alternative. The function can also be sampled at such a rate that the overlap, which occurs in the frequency spectrum, is small enough such that the spurious amplitude frequency components can be ignored.

Consider such a signal $h(t)$, $\left| H(f) \right|$ in Figure 2-7(a) undergoing the first step towards the discrete transform by being sampled at the appropriate frequency $1/T$, Figure 2-7(b), with the final result $h(t)$ $\Delta_0(t)$ Figure 2-7(c). The signals are represented in the time domain and frequency domain respectively and the relationship between the two domains is defined by the Fourier Transform. Note that the modified Transform pair differs from the original pair only by the aliasing effect which results from sampling. The sampled waveform can be described by :-

$$h(t) \; \Delta_0(t) = h(t) \sum_{\kappa=-\infty}^{\infty} \delta(t-\kappa T)$$

$$= \sum_{\kappa=-\infty}^{\infty} h(\kappa T) . \delta(t-\kappa T)$$

The Fourier transform pair in Figure 2-7(c) is unsuitable for machine computation because an infinite number of samples $h(t)$ exist in the time domain; it is necessary to truncate the sampled function so that only a finite number of points, say N, exists. For periodic signals it is convenient to set the window width equal to the period of the signal since this minimises harmonic interaction. The sampled function is truncated by multiplication with the rectangular function $x(t)$ illustrated.

$$x(t) = 1 \quad . \quad -T/2 < t < To-T/2$$

$$= 0 \quad \text{otherwise}$$

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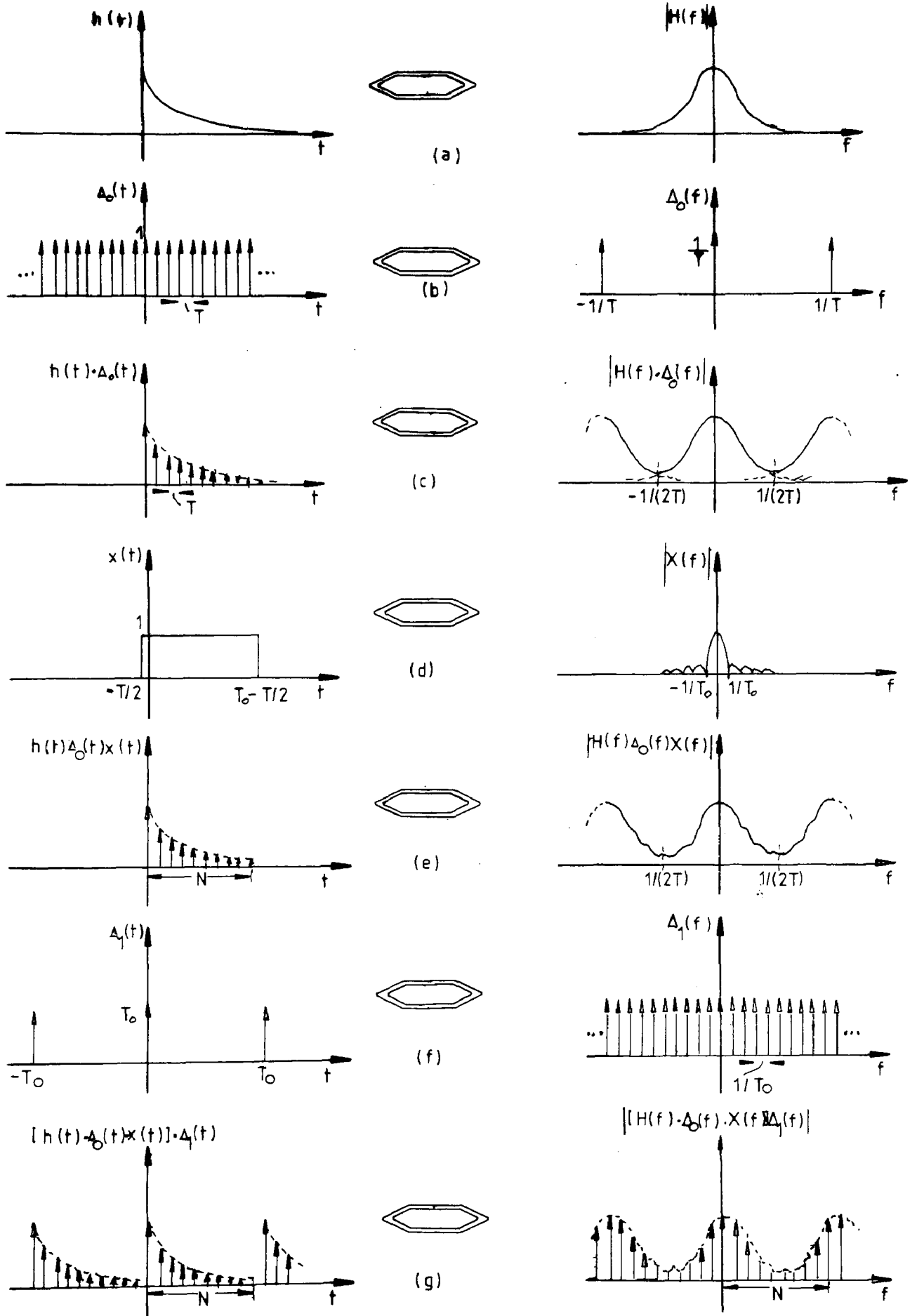
FIG 2-7

where To is the duration of the truncation function.

Truncation introduces a second modification of the original Fourier Transform pair. This effect is to convolve the aliased frequency transform of Figure 2-7(c) with the Fourier Transform of the Truncation function Figure 2-7(d). As shown in Figure 2-7(e) the frequency function now has a superimposed ripple — this effect has been accentuated, for clarity — in practice it is much smaller. Truncation yields :-

$$h(t) \cdot \Delta_0(t) \cdot x(t) = \left[\sum_{\kappa=-\infty}^{\infty} h(\kappa T) \delta(t-\kappa T) \right] \cdot x(t)$$

$$= \sum_{\kappa=0}^{N-1} h(\kappa T) \delta(t-\kappa T)$$

where it has been assumed that there are N equi-distant impulse functions within the truncation interval, that is $N = To/T$. The ripple can be reduced by extending the rectangular window function although, for periodic waveforms, this would only be effective if the extension was to integral multiples of the period of the original waveform. The $sin(f)/f$ function would approach that of an impulse and the error reduces.

The modified transform Figure 2-7(e) is still unacceptable because the frequency spectrum is not finite and represents a truncated time domain function. The next step is to sample the frequency spectrum at intervals of 1/To. This is equivalent to multiplying the frequency spectrum by an infinite series of

harmonically related impulses whose frequencies are integrally related to the fundamental. In turn, this would be equivalent to convolving the signal with impulses of amplitude To at $0, \pm$ To, ± 2 To.... $\infty, \Delta_1(t)$.

The desired relationship is :

$$[h(t)\Delta_0(t)x(t)]*[\Delta_1(t)]=[\sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-\kappa T)]*[T_0 \sum_{r=-\infty}^{\infty} \delta(t-rT_0)]$$

or
$$\overline{h}(t) = T_0 \sum_{r=-\infty}^{\infty} [\sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-\kappa T-rT_0)]$$

$$= \ldots\ldots\ldots +T_0 \sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t+T_0-\kappa T)$$

$$+T_0 \sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-\kappa T)+T_0 \sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-T_0-\kappa T)+\text{---------}$$

where $\overline{h}(t)$ represents the approximation to the function $h(t)$. Note that the convolution result of the final equation is a periodic function with period T_0 which consists of N samples. The rectangular window truncation function was chosen to offset from zero in order to obtain this result. If this had not been performed and the rectangular function had been chosen to be symmetrical about zero the convolution of the rectangular function, with impulses spaced at intervals of T_0 would result in time domain aliasing. That is, the Nth point of one period would coincide with, and add to the first point of the next period.

Now, the Fourier Transform of a periodic function $h(t)$ is a sequence of equi-distant impulses

$$\tilde{H}(n/T_0) = \sum_{n=-\infty}^{\infty} \alpha_n \delta(f-nf_0) \text{ where } f_0 = 1/T_0$$

and $\alpha_n = 1/T_0 \cdot \int_{-\frac{T}{2}}^{T_0-T/2} \bar{h}(t)\exp(-j2\pi nt/T_0)dt \quad n=0,\pm1,\pm2\text{----}$

Substituting the final equation in the above function

$$\alpha_n = 1/T_0 \cdot \int_{-T/2}^{T_0-T/2} T_0 \sum_{r=-\infty}^{\infty} \sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-\kappa T-rT_0)\exp(-j2\pi nt(T_0)dt$$

Integration is only over the period $-T/2$ to $T_0-T/2$ i.e. one period so that :-

$$\alpha_n = \int_{-T/2}^{T_0-T/2} \sum_{\kappa=0}^{N-1} h(\kappa T)\delta(t-\kappa T)\exp(-j2\pi nt/T_0)dt$$

$$= \sum_{\kappa=0}^{N-1} h(\kappa T) \int_{-\frac{T}{2}}^{T_0-T/2} \exp(-j2\pi nt/T_0)\delta(t-\kappa T)dt$$

$$= \sum_{\kappa=0}^{N-1} h(\kappa T)\exp(-j2\pi\kappa nT/T_0) \quad n=0,\pm1,\pm2\text{---since } T_0=NT$$

Thus

$$\tilde{H}(n/(NT)) = \sum_{n=-\infty}^{\infty} \sum_{\kappa=0}^{N-1} h(\kappa T)\exp(-j2\pi\kappa n/N)$$

It can be illustrated that this function is periodic by showing that there are only N distinct values. Considering the equation for $n = r$

$$\tilde{H}(r/(NT)) = \sum_{\kappa=0}^{N-1} h(\kappa T)\exp(-j2\pi\kappa r/N)$$

Consider the sequences for $n = r + N$

$$\tilde{H}((r+N)/(NT)) = \sum_{\kappa=0}^{N-1} h(\kappa T)\exp(-j2\pi\kappa(r+N)/N)$$

Now $\exp(-j2\pi\kappa(r+N)/N) = \exp(-j2\pi\kappa r/N)$

k is an integer and $\exp(-j2\pi\kappa) = \cos(2\pi\kappa) - j\sin(2\pi\kappa) = 1$

$\therefore \tilde{H}(r/(NT)) = \tilde{H}((r+N)/NT)$

and the N distinct values of the function will be given by :-

$$\tilde{H}(n/NT)) = \sum_{\kappa=0}^{N-1} h(\kappa T)\exp(-j2\pi n\kappa/N)$$

The final function, represented by the discrete Fourier Transform, is acceptable for the purposes of digital machine computation since both the time and frequency domain are represented by discrete values.

As shown, the original time function h(t) is approximated by N samples and the original Fourier Transform H(f) is approximated by N samples.

2.6   Program Implementation of the DFT

If n/(NT) is replaced by n, and kT by k, then the DFT reduces to

$$\tilde{H}(n) = \sum_{\kappa=0}^{N-1} h(\kappa)\exp(-j2\pi n\kappa)$$

where n now represents the harmonic frequencies and k the samples at intervals of T. A direct implementation of this formula could be as shown in Figure 2-8.
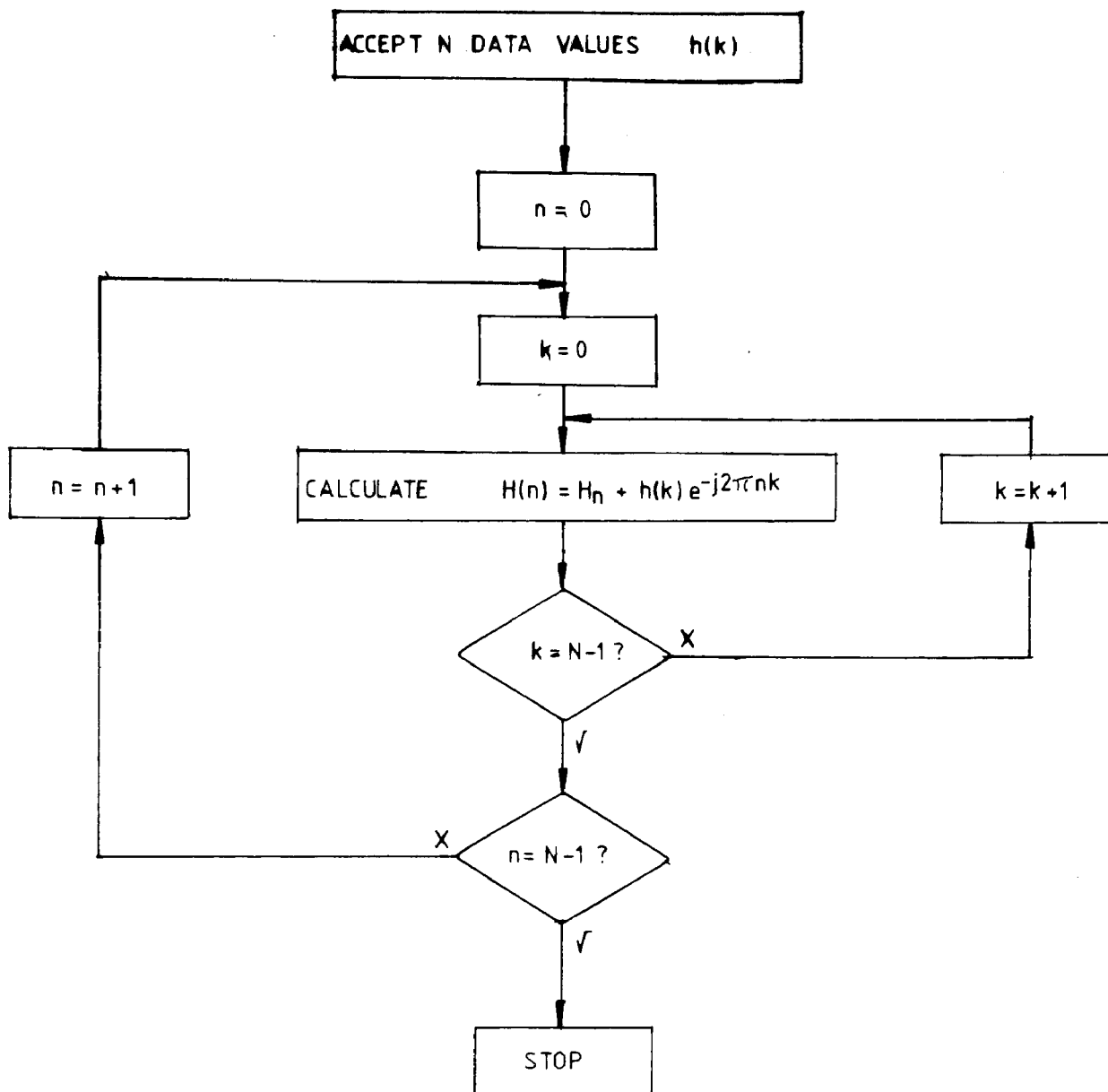
FIG 2-8
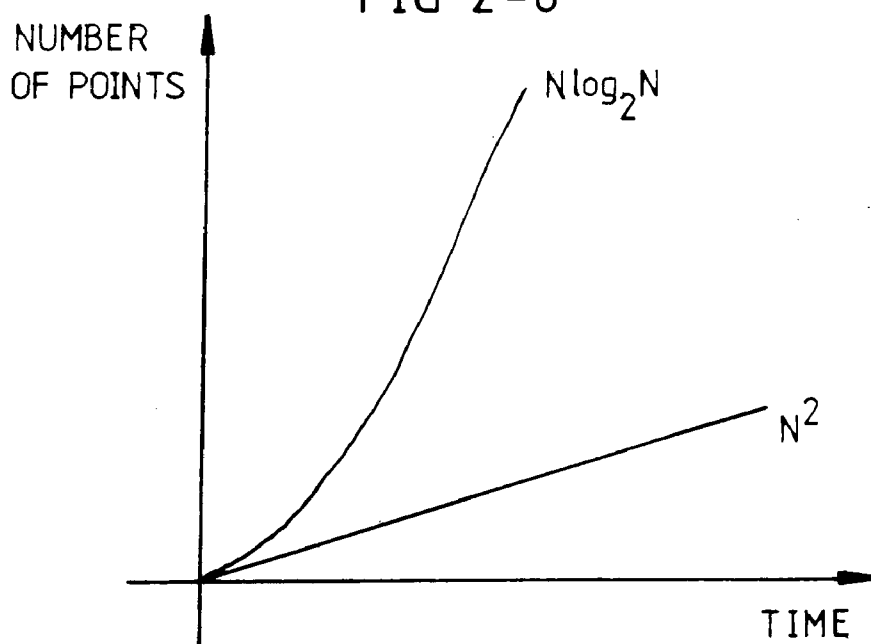
FIG 2-9

2.7   Programming the DFT - The Fast Fourier Transform

The fast Fourier Transform (FFT) is a computational method of calculating the DFT much more quickly than the direct technique shown. The FFT was originally revived and extended by Cooley and Tukey and represented a major step in the realization of modern high-speed digital Fourier Analysis Techniques. In computing equations the time taken to perform a multiply operation is far greater than that required for a simple addition. In the 'direct' technique, previously illustrated, a number of multiplications proportional to N^2 (N being the number of sample points) is required. Some techniques of programming the DFT have taken advantage of symmetries in the waveforms or special hardware facilities on the computers in order to reduce computational times, and cost, by orders of 50%.

However, Cooley and Tukey evolved a method whereby, provided the sample points were an integral power of 2 and hence not prime, the original number of time domain samples, N, could be repeatedly divided into two groups of equal numbers of N/2,N/4,N/8 and so on. This was achieved in such a manner that the DFT of the whole could be obtained by the successive addition and subtraction of the weighted Fourier Transforms of the individual groups. In this way the number of required multiplicative steps was reduced from N^2 to N log N so that the computational time could be improved by several orders (For example, a 1024 point transform would require only $1/100^{th}$ of the computational time). This method has become so successful that it is known as the Fast Fourier Transform method. Figure 2-9.

It should be noted that this procedure requires that N be an integral power of two. It can be modified to work on other values of N, however, the computation can be shown to become rather less efficient particularly if the number into which N can be factorized is not small. If N is a prime number, no fast algorithms exist and direct implementation of the DFT must be employed.

Modified FFT algorithms have evolved although all perform most efficiently when N is chosen as a power of 2. In particular a 'decimation in frequency' as opposed to the original 'decimation in time 'algorithm exists, which is equally as useful. Both methods require N/2 log N complex additions, subtractions and multiplications. Both computations can be executed 'in place' although the decimation-in-frequency method uses time samples in 'unshuffled' order and yields frequency samples in shuffled (bit reversed) order. Whilst the decimation in time algorithm yields the opposite result, the use of either algorithm depends on the application. It is the 'decimation in time' algorithm which will be considered here.

2.8 Mechanics of the FFT

For those more familiar with Matrix manipulation, the algorithm can be considered as the decomposition of a large matrix into smaller matrices and the explanation in Brigham[52] is recommended. Here, an alternative approach is presented.

2.8.1   The Decimation in Time Algorithm

Consider the sampled time domain function to be transformed. Suppose a time series having N samples (such as Xk) and shown in Figure 2-10 is to be divided into functions, Yk, Zk, each of which has only half as many points (N/2). The function Yk is composed of the even numbered points $(X_0, X_2, X_4, ..)$ and Zk is composed of the odd numbered points $(X_1, X_3, X_5, ...)$

These functions are shown in Figure 2-10 and may be written formally as :-

$$Y_k = Y_{2\kappa} \qquad \kappa = 0, 1, 2 \text{---}, N/2-1$$

$$Z_k = X_{2\kappa+1}$$

Since Y_k and Z_k are sequences of N/2 points each, they have discrete Fourier Transforms defined by

$$B_r = \sum_{\kappa=0}^{N/2-1} Y_k \exp(-4\pi jr\kappa/N)$$

$$C_r = \sum_{\kappa=0}^{N/2-1} Z_k \exp(-4\pi r\kappa j/N)$$
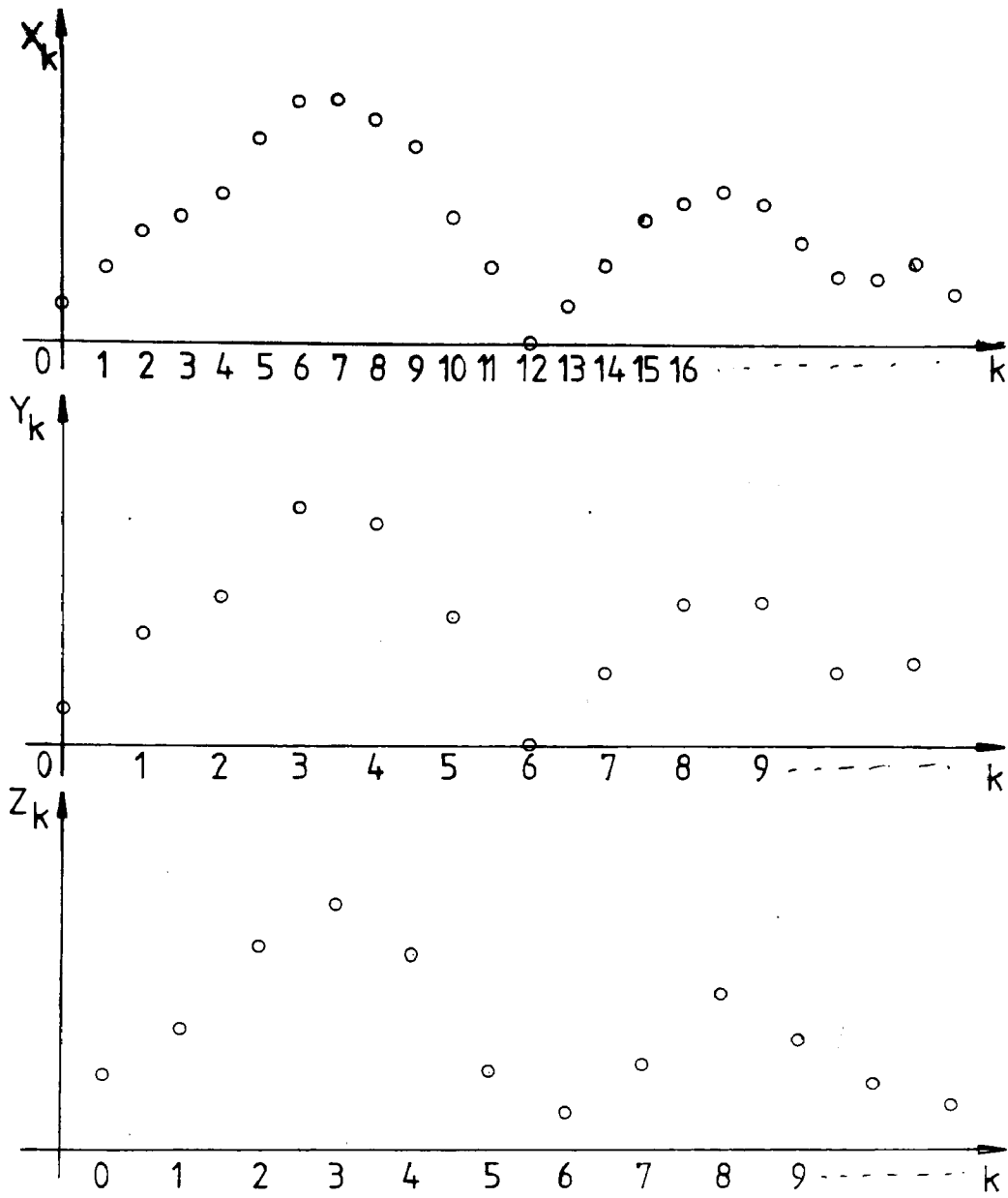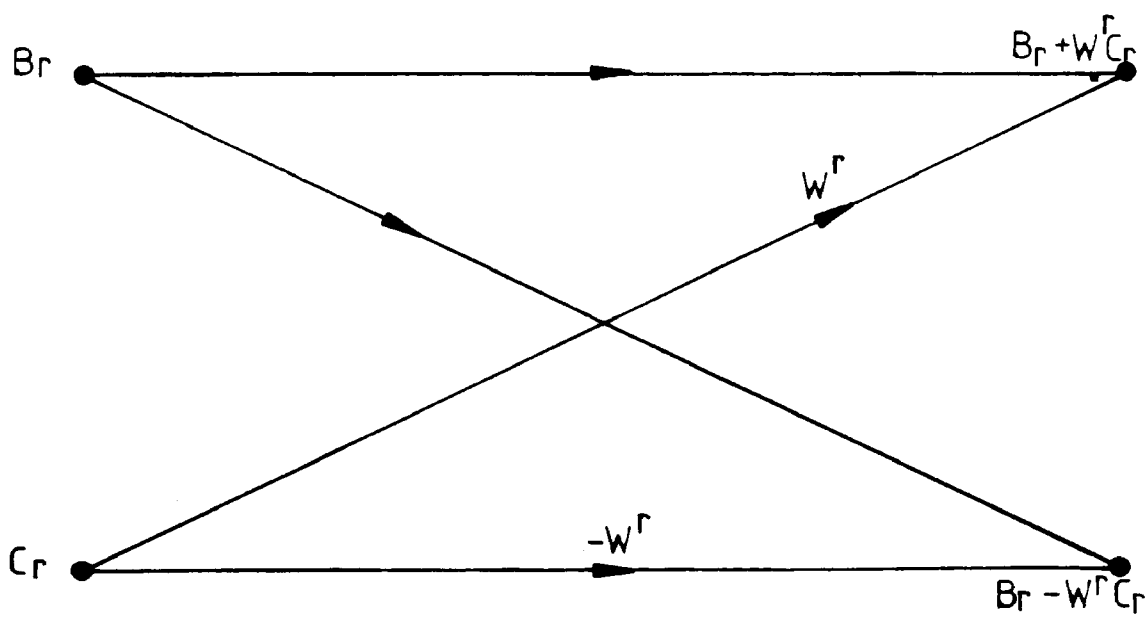
FIG 2-10

FIG 2-11

The discrete Fourier Transform that is required is Ar which can be written in terms of the odd and even numbered points.

$$A_r = \sum_{\kappa=0}^{N/2-1} Y_\kappa \exp(-4\pi jr\kappa/N) + Z_\kappa \exp(-2\pi jr(2\kappa+1)/N)$$

$$r = 0,1,2,3\text{----}N-1$$

$$= \sum_{\kappa=0}^{N/2-1} Y_\kappa \exp(-4\pi jr\kappa/N) + \exp(-2\pi jrN) \sum_{\kappa=0}^{N/2-1} Z_\kappa \exp(-4\pi jr\kappa/N)$$

which, using equations for B_r and C_r becomes

$$A_r = B_r + \exp(-2\pi jr/N)Cr \quad 0 \leqslant r < N/2$$

For values of r greater than $N/2$ the Discrete Fourier Transform Br and C_r, repeat periodically, their values where $r < N/2$. Thus, substituting $r + N/2$ for r in the above equations :-

$$A_{r+N/2} = B_r + \exp(-2\pi j(r+N/2)/N)C_r$$

$$= B_r + \exp(-\pi j)\exp(-2\pi jr/N)C_r$$

$$\underline{= B_r - \exp(-2\pi jr/N)C_r}$$

$$A_r = B_r + \exp(-2\pi jr/N)C_r \qquad (B)$$

$$A_{r+N/2} = B_r - \exp(-2\pi jr/N)C_r \qquad (C)$$

Therefore the first N/2 points of the DFT of Ar can be obtained with (B) whilst the last N/2 points of the DFT can be obtained with (C). Thus, it can be seen that the Fourier Transform of X_K (a sequence having N samples) can be simply obtained from the DFT of two series of N/2 samples Y_K, Z_K each being derived from the original sample in the manner previously described. These expressions can be applied recursively for each new group sub-division until only a single point remains in each group.

If the expression $\exp(-2\pi jr/N)$ is replaced by W^r, r denoting the order of the exponential then the previous equations become

$$A_r = B_r + W^r C_r$$

$$W^r = \exp(-2\pi jr/N)$$

$$A_{r+N/2} = B_r - W^r C_r$$

This process can be described graphically as shown in Figure 2-11. The graphical structure illustrating the process of the FFT is often referred to as the butterfly technique. This reference is due to the similarity of the basic graphical structure of the FFT and the butterfly outline.

The arrow denotes multiplication, the notation at the side of the arrow shows the magnitude of the multiplication constant. Where no constant is shown it is assumed that its magnitude is 1. Each node, following the start node, is a summing node where the input quantities are determined by defining those quantities on lines entering the node. It should also be noted that in some articles the weighting factor W^r is called the 'Twiddle' factor, 'phase' factor or 'rotation' factor. For an eight point waveform the previous process can be extended and expressed, graphically, as in Figure 2-12.

Initially, as described, the series is divided into an even and odd set of points whose Fourier Transforms are B_r and C_r respectively, that is :-

$$B_r = \sum_{k=0}^{N/2} Y_k \exp\,(-4\pi jrk/N), \quad C_r = \sum_{k=0}^{N/2-1} Z_k \exp\,(-4\pi jrk/N)$$

Hence :-

$$B_0 = Y_0 \qquad\qquad\qquad C_0 = Z_0$$

$$B_1 = Y_1 \sum_{k=0}^{3} \exp(-\pi jk) \qquad\qquad C_1 = Z_1 \sum_{k=0}^{3} \exp(-\pi jk)$$

$$B_2 = Y_2 \sum_{k=0}^{3} \exp(-2\pi jk) \qquad\qquad C_2 = Z_2 \sum_{k=0}^{3} \exp(-3\pi jk)$$

$$B_3 = Y_3 \sum_{k=0}^{3} \exp(-3\pi jk) \qquad\qquad C_3 = Z_3 \sum_{k=0}^{3} \exp(-3\pi jk)$$

The process is now continued by dividing the four point transform using the same recursive equation as shown in Figure 2-13.
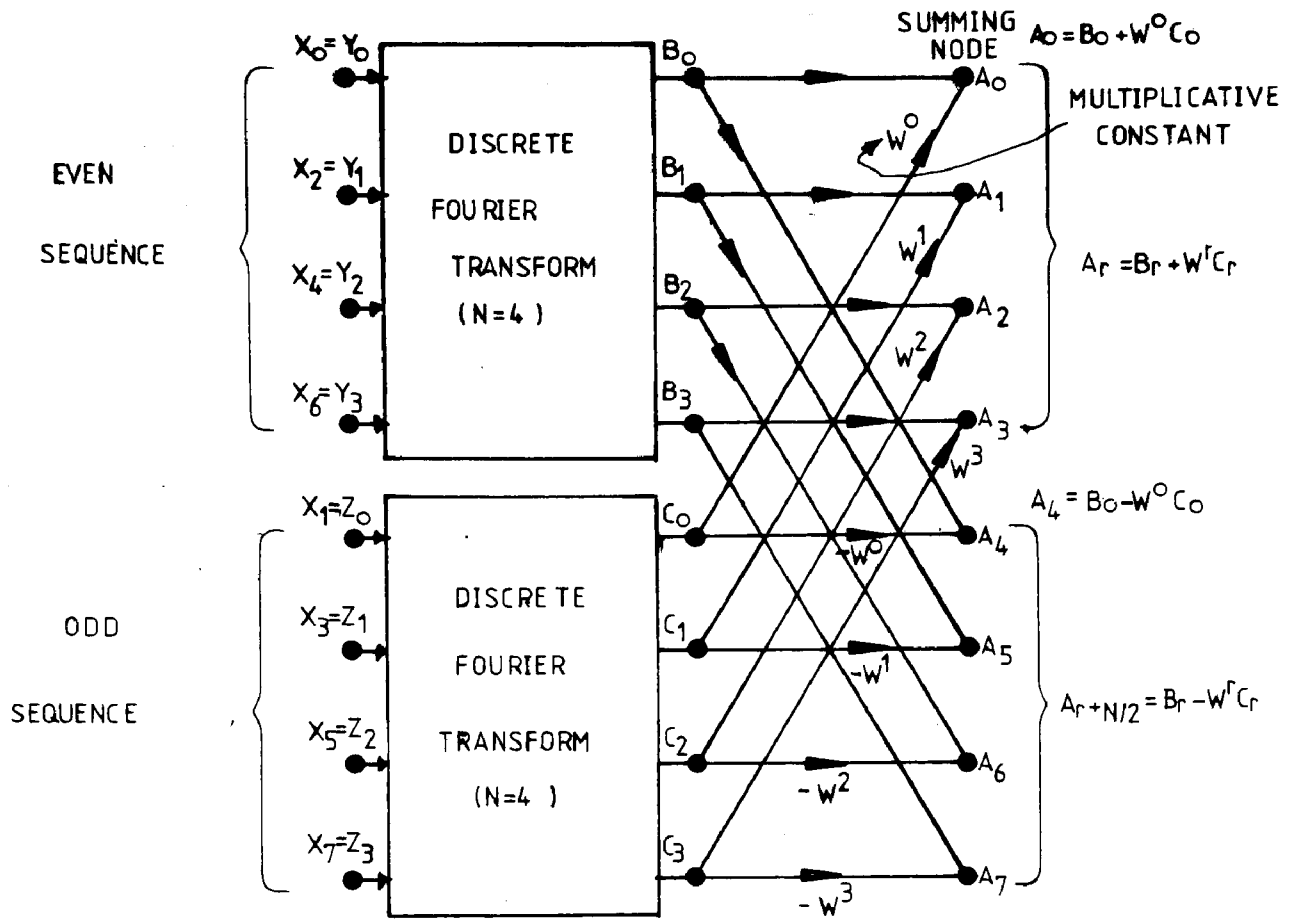
FIG 2-12
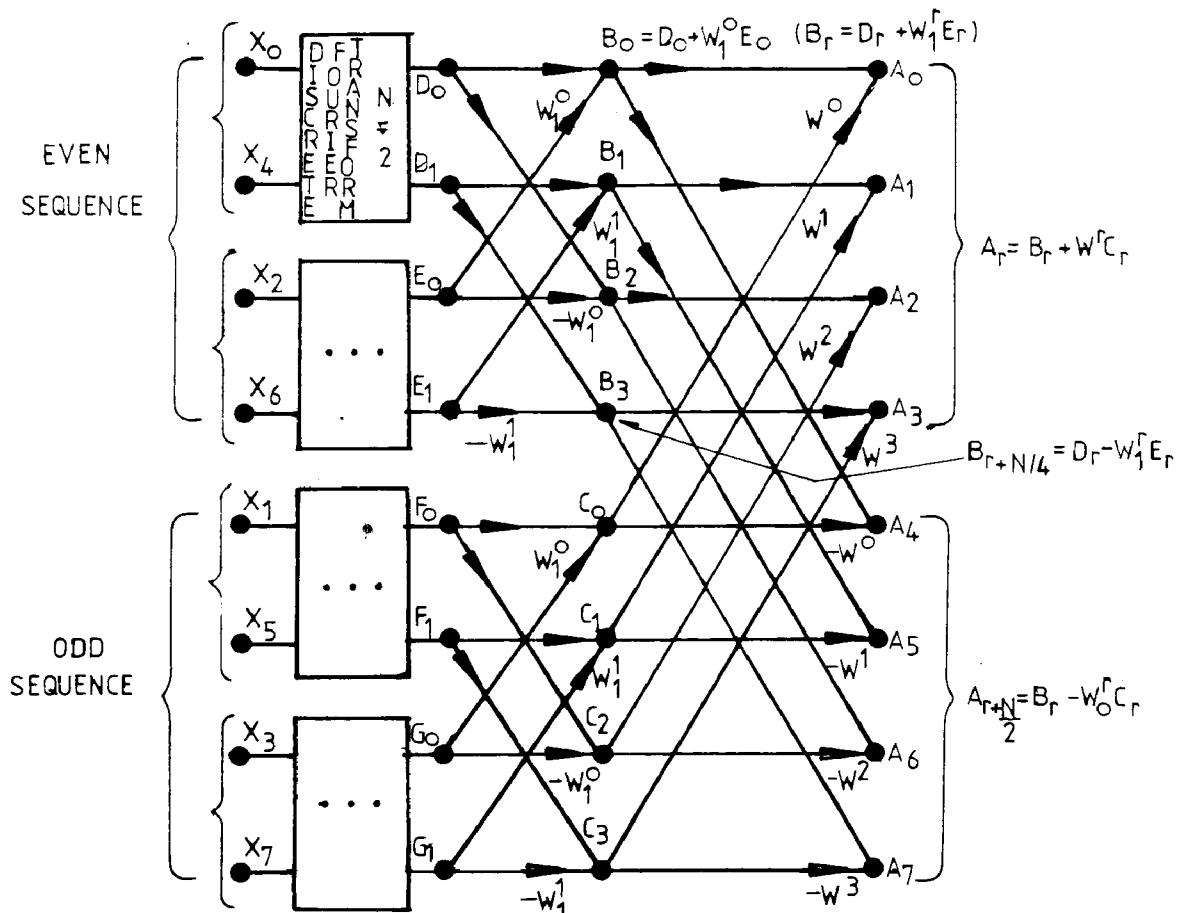
FIG 2-13

Note : W^o and W_1^o will be the same since the power of the exponential is '0' in both cases. However, W^1; and W_1^1 will be different since the exponential is finite and although r is the same, the number of points differ (N in the first case W^1, N/2 for the second case W_1^1;)

And finally Figure 2-14 shows the complete graphical form of the decimation in time algorithm for an eight point function.

It should be noted that the process of repeatedly dividing the sequences into equal groups of even and odd components has resulted in a re-distribution of the input time domain sequence. The inputs are now 'bit-reversed'. That is, if the input sequence is expressed, not in decimal, but in its binary equivalent i.,e. a sequence of eight samples will be expressed as X_{000}, X_{001}, X_{010}, X_{011},.....X_{111} then if the sequence is now re-expressed with the bits in reverse order X_{000}, X_{100}, X_{010}, X_{110},.... X_{111} then this is the new order in which they appear. Thus, for example, the second sample X_{001} will appear in the position 100 (or the X_4 position).

Since there are 2^N points, then due to the successive halving of points there must be $Log_2(2^N)$, or N stages. In summary then the process of decomposition is as illustrated in Figure 2-15.

$$A_r = B_r + W_0^r C_r$$

$$A_{r+N/2} = B_r - W_0^r C_r$$

FIG 2-14

EVEN SEQUENCE

ODD SEQUENCE
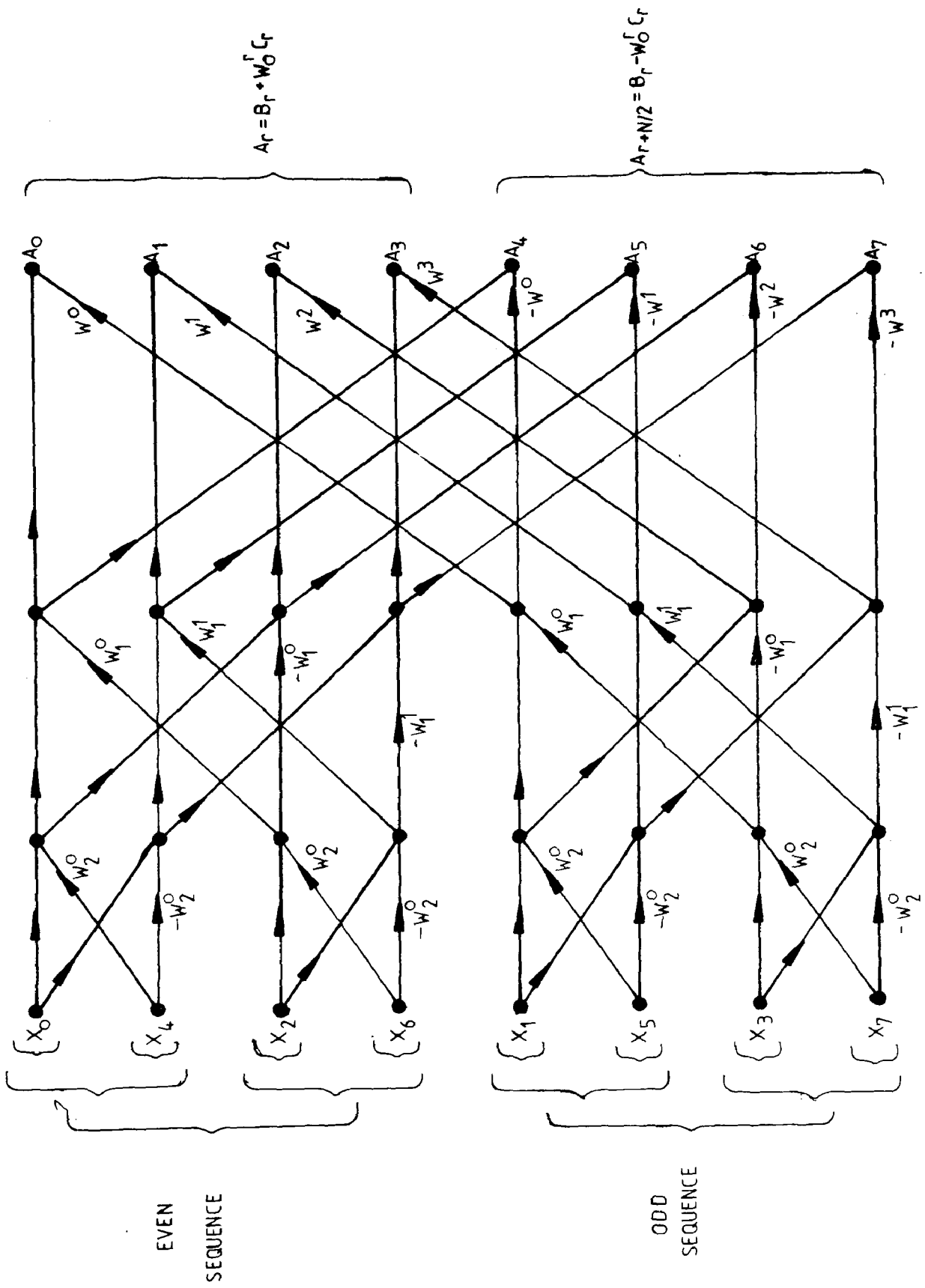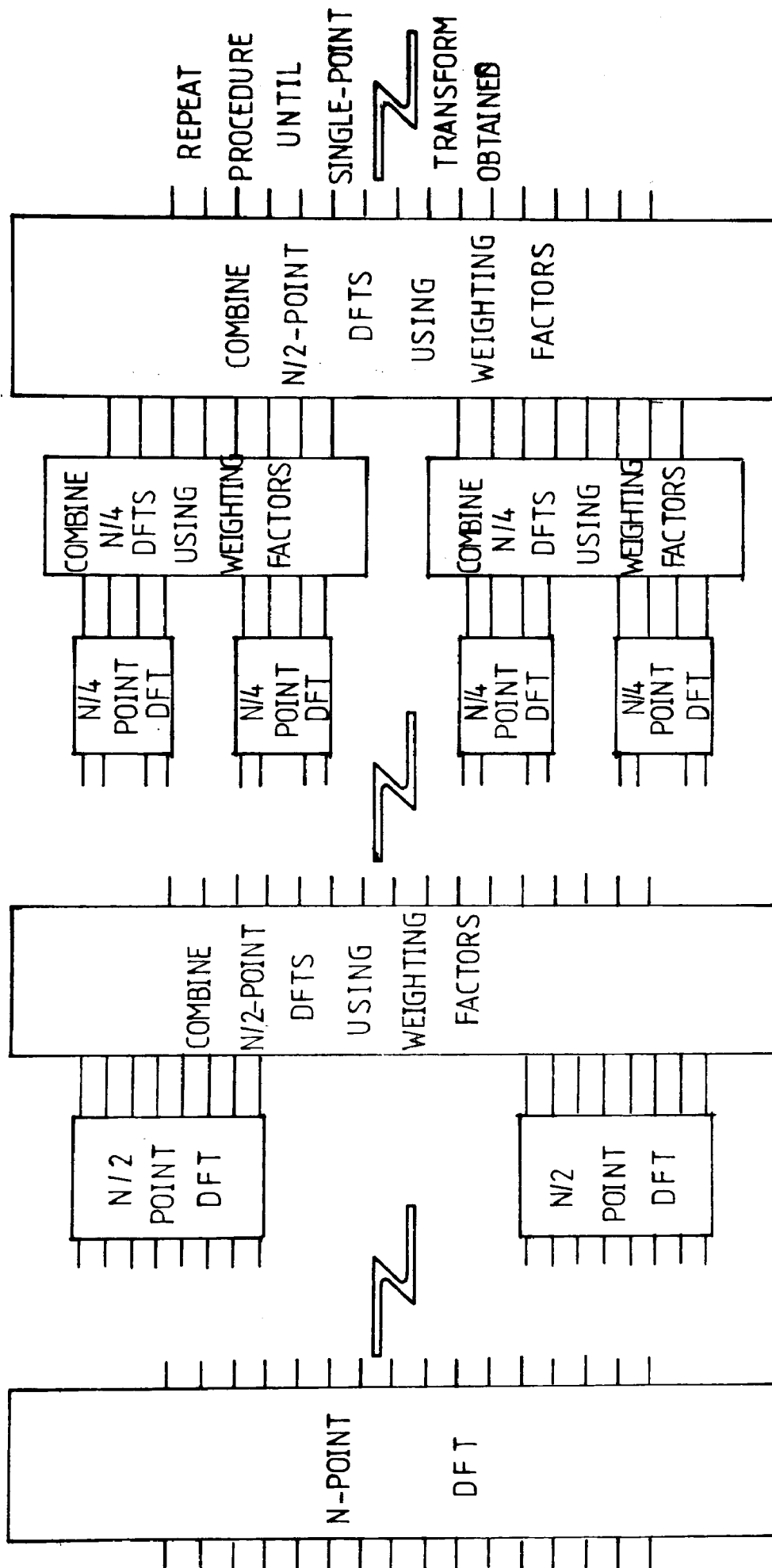
FIG 2-15

2.9 Programming the Algorithm

It can be seen from the previous figures that the original data is used to complete only the next row of data and is not required for further processing. Thus one can compute intermdediate stages of the FFT and store the results in the same locations in which the original data, being transformed, was stored. Thus the array, used to store the input sequence, is also the same array into which the output sequence is stored. An algorithm that uses the same locations to store both the input and output sequence is called an in-place algorithm.

2.9.1 The Binary Reversal Routine

In order that the output sequence of the FFT is in its proper order the input sequence of samples must be placed in a bit reversed arrangement. Figure 2-16 shows a flow chart (after Rader) for achieving the bit reversing process using a recursive routine. Using the initial bit reversed number (that is X = 0) the succeeding bit reversed number, say Y, can be obtained from X = 0 being entered into the routine. The next bit-reversed number, of the sequence, say Z, is then computed by entering X = Y into the routine, and so on, until the entire sequence has been calculated.
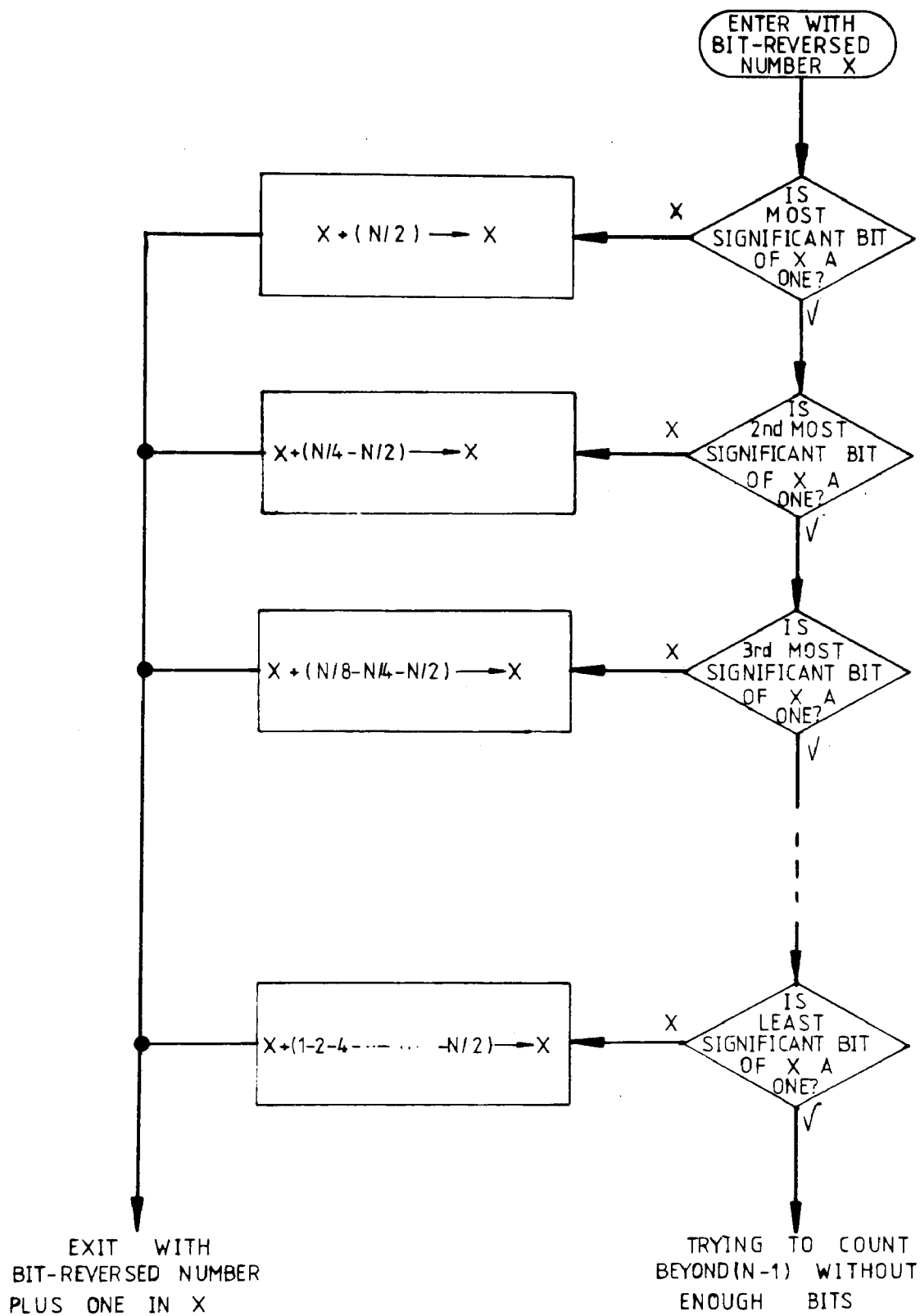
FIG 2-16

2.9.2   Programming the Recurring FFT Equation

The graphical representation of the 8 point FFT, as shown in Figure 2-14 can be alternatively expressed, as shown in Figure 2-17. In this diagram a subscript notation is used to identify the computed samples according to their position in the array matrix.

If the computational requirements are now considered then, initially the input sequence, X(k), are shuffled and replaced in bit reverse order. The equations

$$A_r = B_r + W^r C_r \qquad (W^r = \exp(-2\pi j r/N))$$

and $A_r + {}_{N/2} = B_r - W^r C_r$

are then applied recursively. Now, in order to program the algorithm the mathematical equations need to be converted to difference equations, suitable for substitution in a computer program.

From the nature of the graphical process previously outlined, it can be seen that each new array or sequence of results at the nodes, can be simply obtained from the previous array. The terms of the complete array can be denoted by $A_n(X)$, (replacing the B and C notation) where the suffix n specifies the column position in the graphical structure. X denotes the row of the array. Thus, for example, in Figure 2-17 of the 8 point sequence

$$A_4(1) = A_3(1) + W^3 A_3(5)$$

and $A_4(5) = A_3(1) - W^3 A_3(5)$
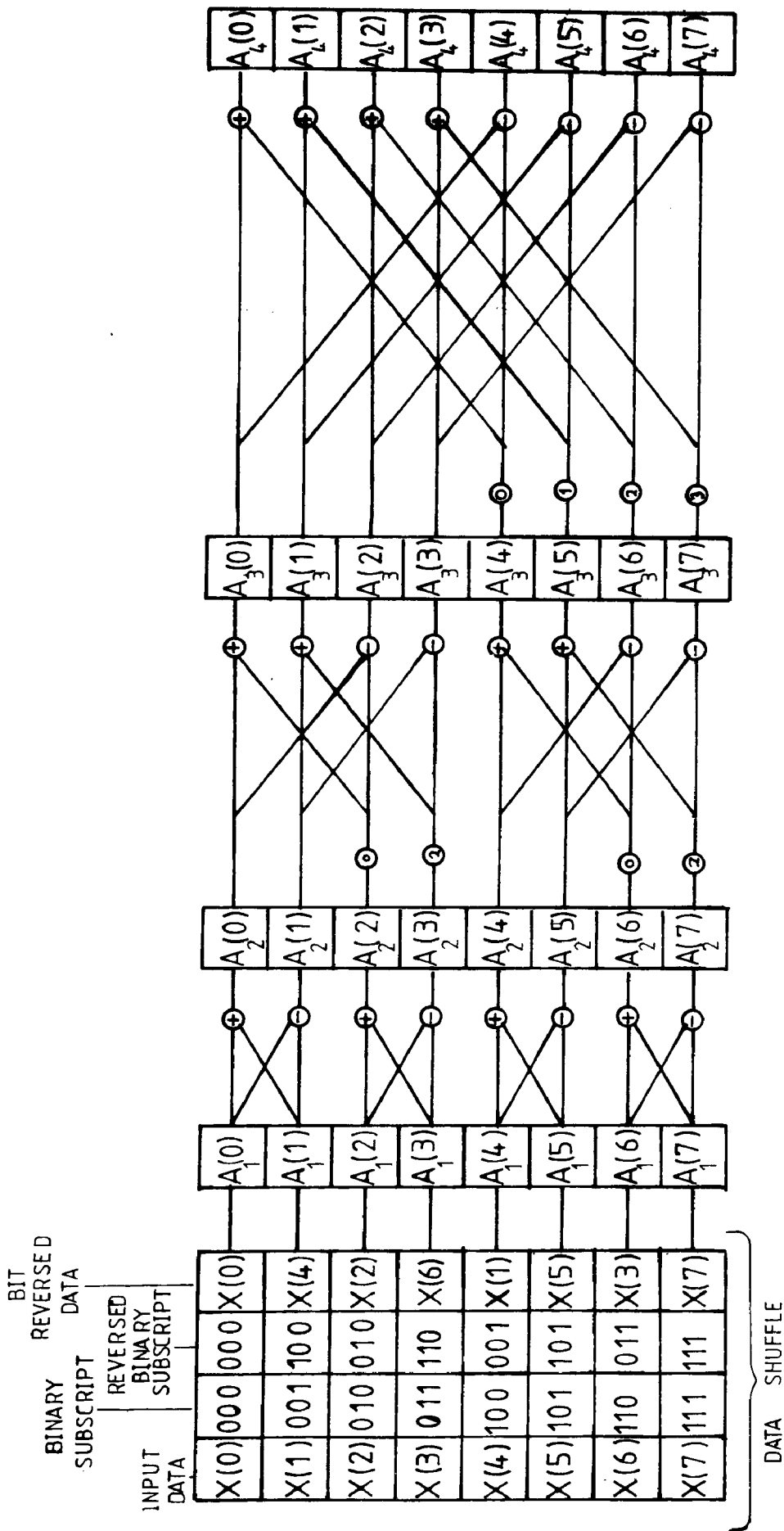
FIG 2-17

If the number of points in the sequence is represented as $N = 2^r$ then the sequence in the last column can be represented as

$$A_{r+1} (n) = A_r (n) + W^n(n+N/2)$$

$$A_{r+1} (n+N/2) = A_r (n) - W^n(n+N/2)$$

The difference equations can now be obtained by considering the general, intermediate array, $A_{i+1}(n)$ and its relationship to the previous array $A_i(n)$. In moving from left to right in the array i.e. $A_i(n)$ to $A_{i+1}(n)$.

1. The distance between the elements of the recursive equation doubles and its absolute value is dependent on the column position i. Thus the two elements of the recursive equation can be represented by $A(n)$ and $A(n+2^{i-1})$ as deduced from Figure 2-18.

2. Considering the original identities of $A(n)$ and $A(n+2^{i-1})$ as

$$B_r = \sum_{\kappa = 0}^{N/2-1} Y_k \exp (-4\pi jr\kappa/N) \text{ and}$$

$$C_r = \sum_{\kappa = 0}^{N/2-1} Z_k \exp (-4\pi jr\kappa/N) \quad \text{and Figure 2-18}$$

then the range of each summation must double, whereas the number of operational statements defining the total Fourier Transform must halve. This can be satisfied by writing

$$n = (m-1) + (\ell-1).2^i$$
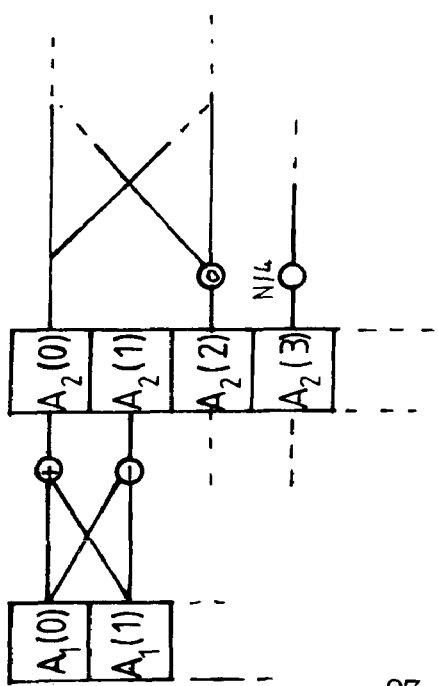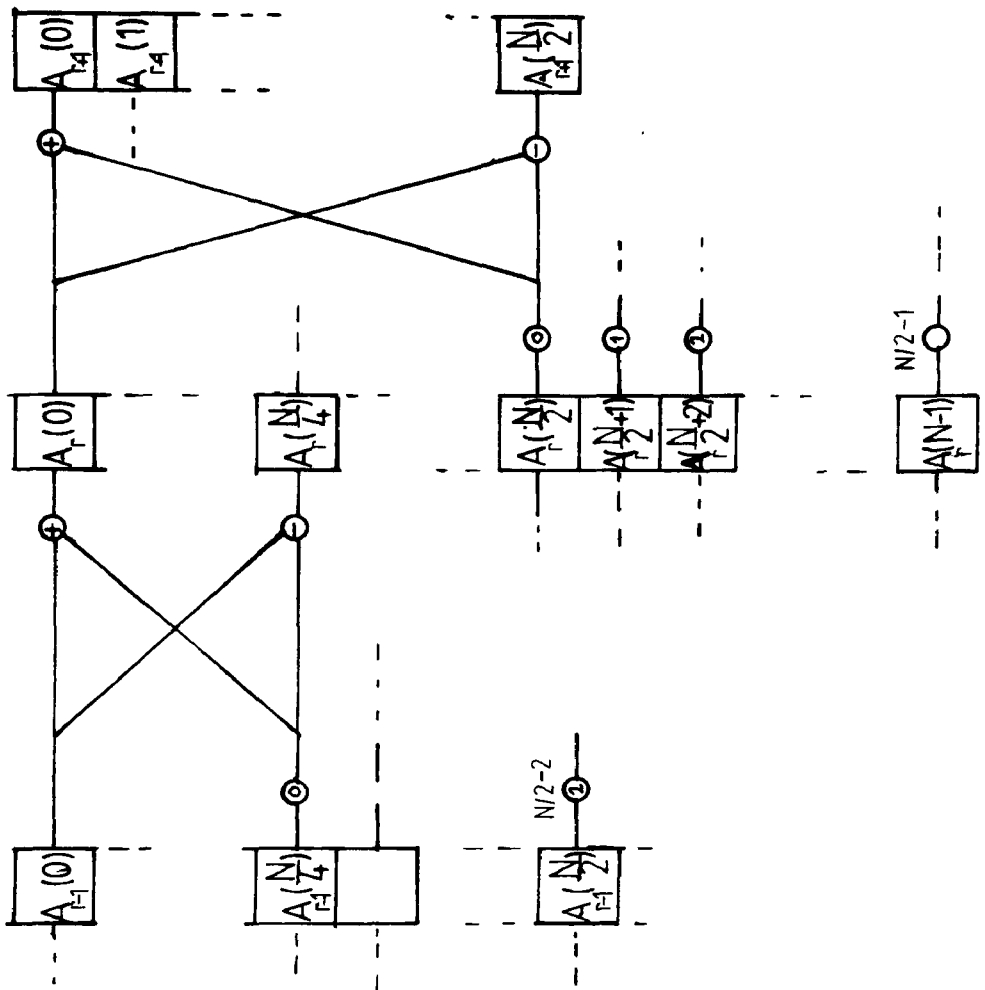
FIG 2-18

where there are ℓ pairs of operational statements, with $\ell = 1,2,\ldots\ldots 2^{r-i}$ and an independent variable m of range $m = 1, 2,\ldots 2^{i-1}$.

It should be noted that the variable n will always range over all its N values, irrespective of the value of i, as ℓ and m cycle over their own limits. However, the order of the selection of the values does depend on i.

3. The argument of the weighting function must halve which can be accounted for by expressing the weighting function as $W^{n\cdot 2^{r-i}}$. Substituting for n,

$$W^{n\cdot 2^{r-i}} = W^{(m-1)2^{r-i}} \cdot W^{(\ell-1)2^i \cdot 2^{r-i}}$$
$$= W^{(m-1)2^{r-i}} \cdot W^{(\ell-1)2^r}$$

Now $2^r = N$, thus

$$W^{n\cdot 2^{r-i}} = W^{(m-1)2^{r-i}} \cdot W^{(\ell-1)N}$$

and recalling that

$$W = \exp(-2\pi jr/N)$$

then

$$W^{(\ell-1)N} = \exp(-2\pi jr(\ell-1))$$

is always integer so that

$$W^{(\ell-1)N} = 1$$

Hence

$$W^{n.2^{r-i}} = W^{(m-1)2^{r-1}}$$

The final recursive expression for the computation of the FFT then becomes :-

$$A_{i+1}[(m-1)+(\ell-1).2^i] = A_i[(m-1)+(\ell-1).2^i] + W^{(m-1)2^{r-i}}.A[(m-1)+(\ell-1)2^i+2^{i-1}]$$

$$A_{i+1}[(m-1)+(\ell-1).2^i+2^{i-1}] = A_i[(m-1)+(\ell-1).2^i] - W^{(m-1)2^{r-1}}A_i[(m-1)+(\ell-1)2^i+2^{i-1}]$$

$$\text{for } i = 1,2 \text{ ---- } r$$
$$m = 1,2 \text{ ---- } 2^{i-1}$$
$$\ell = 1,2, \text{ --- } 2^{r-i}$$

Now that the recursive equations describing the FFT have been obtained the actual programming becomes fairly straightforward. The computation requires three 'loops' covering the ranges of i, ℓ and m, respectively. The least rapidly changing of these must be i, since both m and ℓ depend on its value to determine the limit of their ranges. A flowchart [53] describing the implementation of the recursive equations is shown in Figure 2-19. From this, it is an easy task to derive a BASIC program. The program, written by the author, is given in the appendix.

ACCEPT DATA
ARRAY X(k)

BINARY SHUFFLE
AND ENTER IN ARRAY
A( )

INITIALISE
$m = l = i = 1$

LET: $B = A[(m-1) + (l-1) \cdot 2^i)]$

$C = A[(m-1) + (l-1)2^i + 2^{i-r}]$

AND EVALUATE:

$A[(m-1) + (l-1)2^i] = B + C W^{(m-1)2^{r-i}}$

$A[(m-1) + ((l-1)2^i + 2^{i-1}] = B - C W^{(m-1)2^{r-i}}$

$m = 2^{i-1}?$ → $m = m + 1$

$l = 2^{r-i}?$ → $l = l + 1$

$i = r?$ → $i = i + 1$

STOP
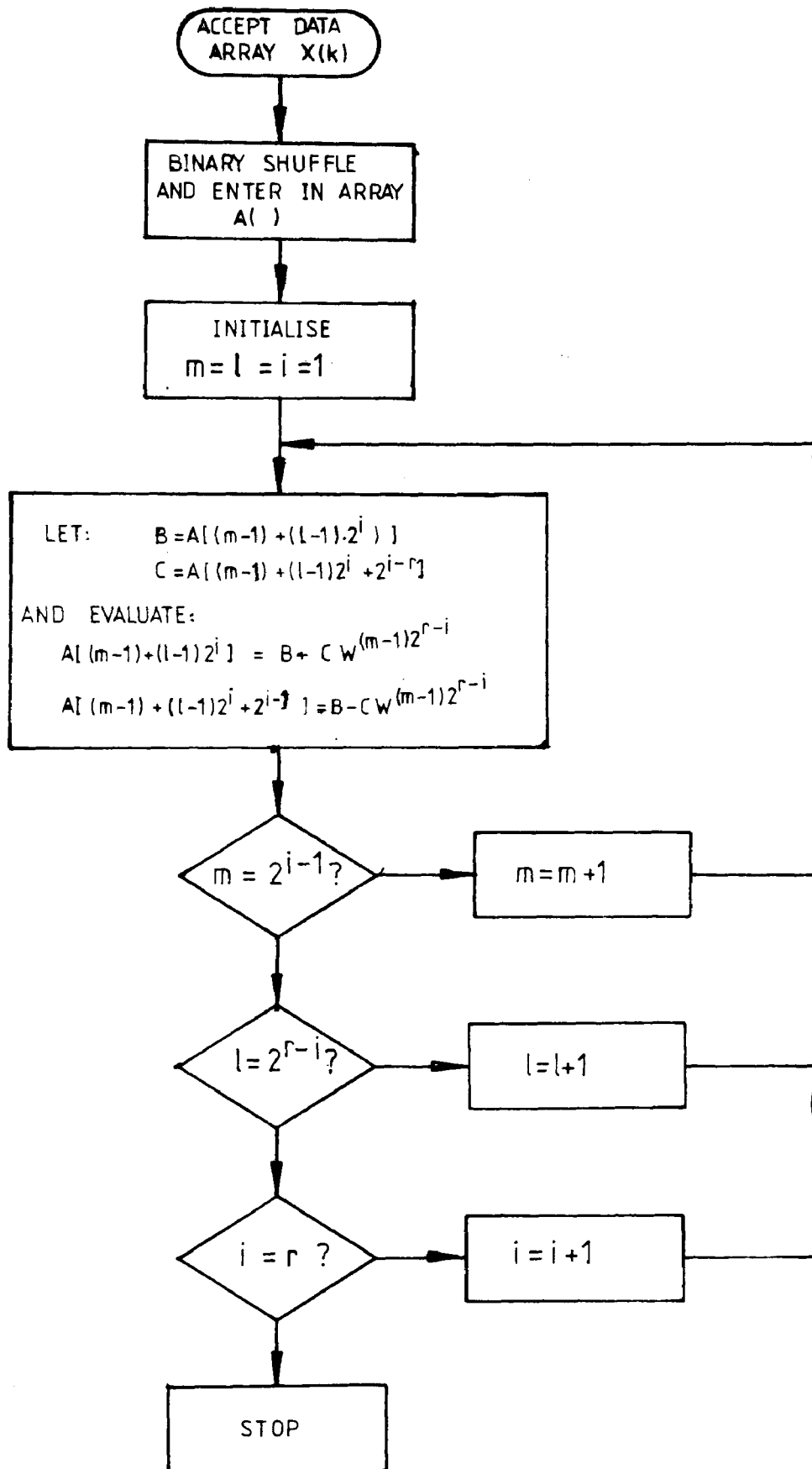
FIG 2-19

CHAPTER 3   The PWM Control System - The Analogue Approach

3.1 System Realisation of PWM Techniques

In order to compare differing techniques of PWM generation a Mark 1 Analogue Unit had been designed [48] to provide sawtooth and triangular carrier waveforms coupled with sinusoid and stepped sinusoid modulating waveforms as shown in Figure 3-1. The purpose of the unit was to generate differing basic waveforms for the realisation of several types of PWM signals. Spectral analyses and practical performance tests could then be conducted to evaluate the potential of each individual PWM waveform.

The modulating signal generator produces a three-phase sinusoidal output which can be switched to the sample and hold units to provide a three-phase stepped wave output. The selected modulating signals and carrier waveforms are applied to comparators in order to generate the PWM output. The three-phase PWM signal is then modified in the inverter pulse sequence and drive unit which outputs all the appropriate waveforms required for the operation of a three-phase McMurray Impulse Commutated Inverter [67]. The McMurray Inverter is then connected to the inputs of the induction motor.

New specifications were raised for the MkII analogue rig and some re-design of the MkI equipment sub-units was necessary in order to reflect the changes in its requirements.
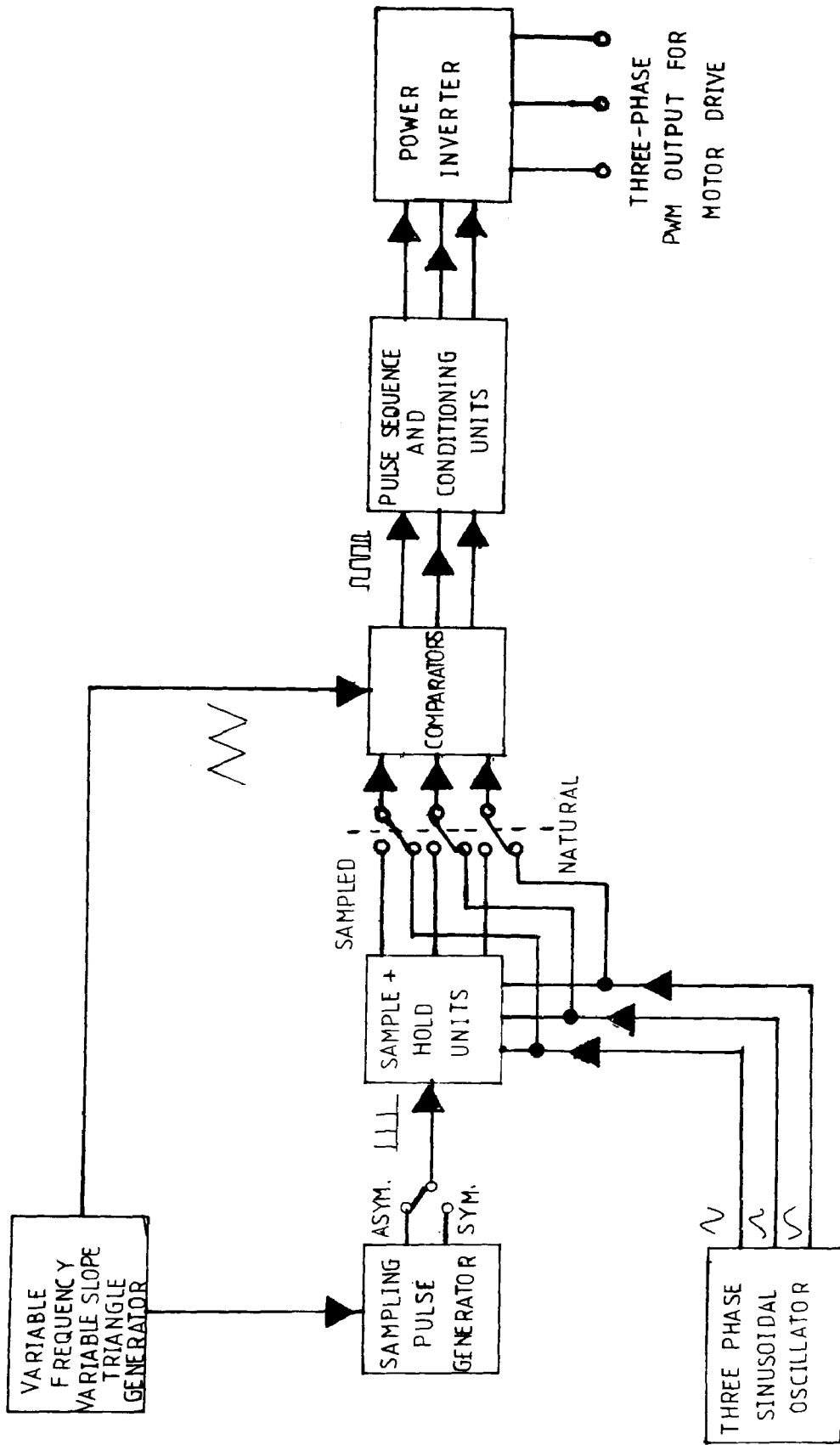
FIG:3-1 ANALOGUE HARDWARE SYSTEM DIAGRAM

3.1.1 The Carrier Waveform Generation Board

In Figure 3-2, and 3-3 the variable triangular waveform generator provides a carrier reference signal for the system. This sub-unit also generates, at appropriate points in the cycle, short pulses which synchronise the gating function of the sample and hold units.

The oscillator [68] utilizes a single section R-C network; the frequency being determined by the rate at which the integrator capacitor is charged. If it is assumed that the input to the integrator is a positive voltage, then the ouput voltage will fall, in a linear manner. A voltage is eventually reached, at which the positively biased comparator will switch. At this point the flip flop is triggered and the input to the integrator is inverted, from its positive level to the negative level. Simultaneously, the integrator output begins to rise and the positively-biased comparator switches its output back to its positive level, the flip-flop remains unaffected. A short pulse is therefore produced at the comparator output and the pulse width will be variable and determined by the combined switching delays of the comparator and flip flop. The integrator output is now rising and it is the negatively biased comparator which will now switch, producing a similar switching sequence to that already described, see Figure 3-4. The frequency of operation can be calculated from the relationship $V = -1/RC \int_{o}^{t} e \, dt$.

Since the pulse outputs from the comparators are undefined, they are used to trigger a monostable/timer designed to provide a fixed pulse width of $50 \mu S$ at a frequency determined by that of the input pulses. In this way, the output pulses are synchronised to the apices
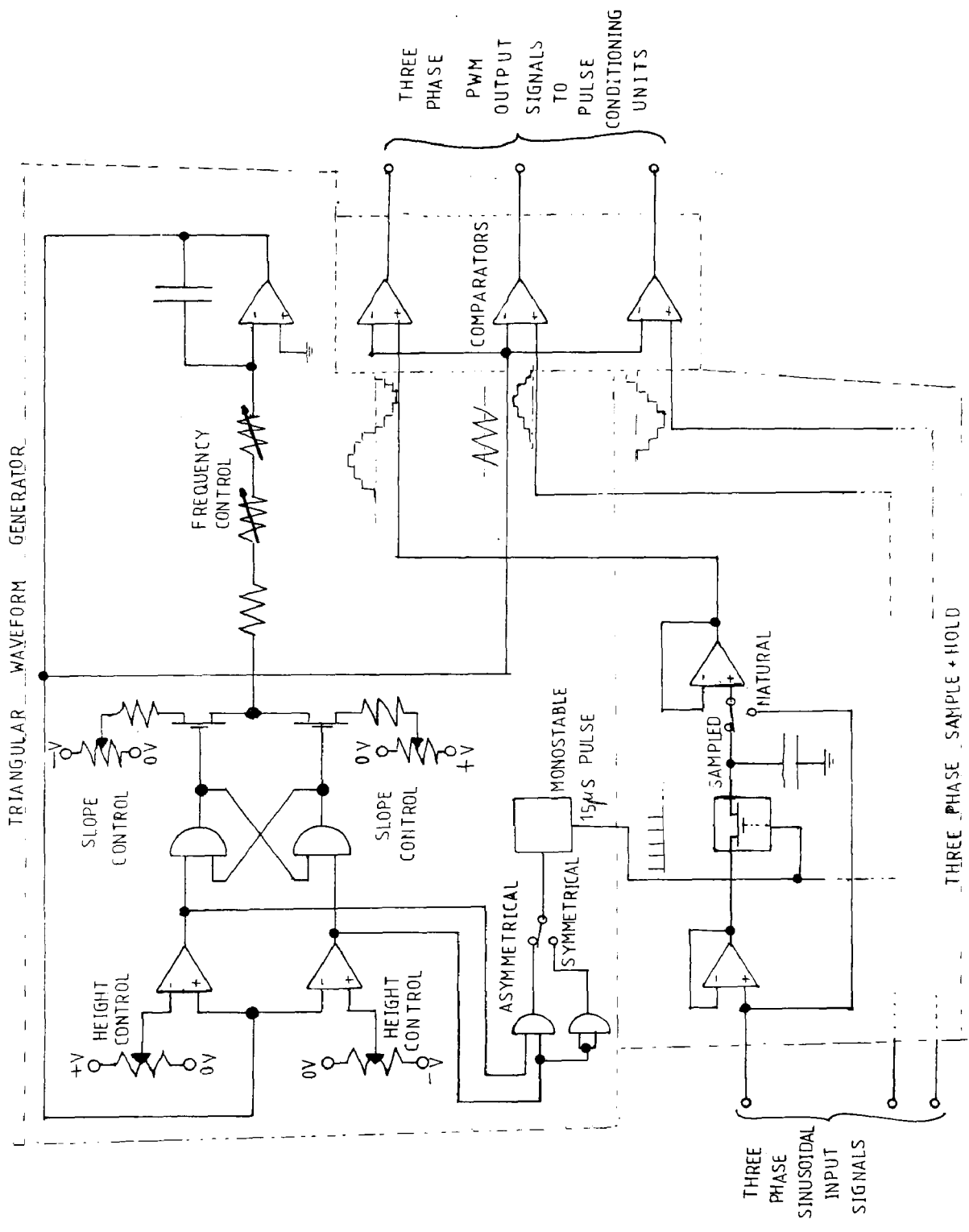
FIG:32 THREE PHASE PWM UNIT
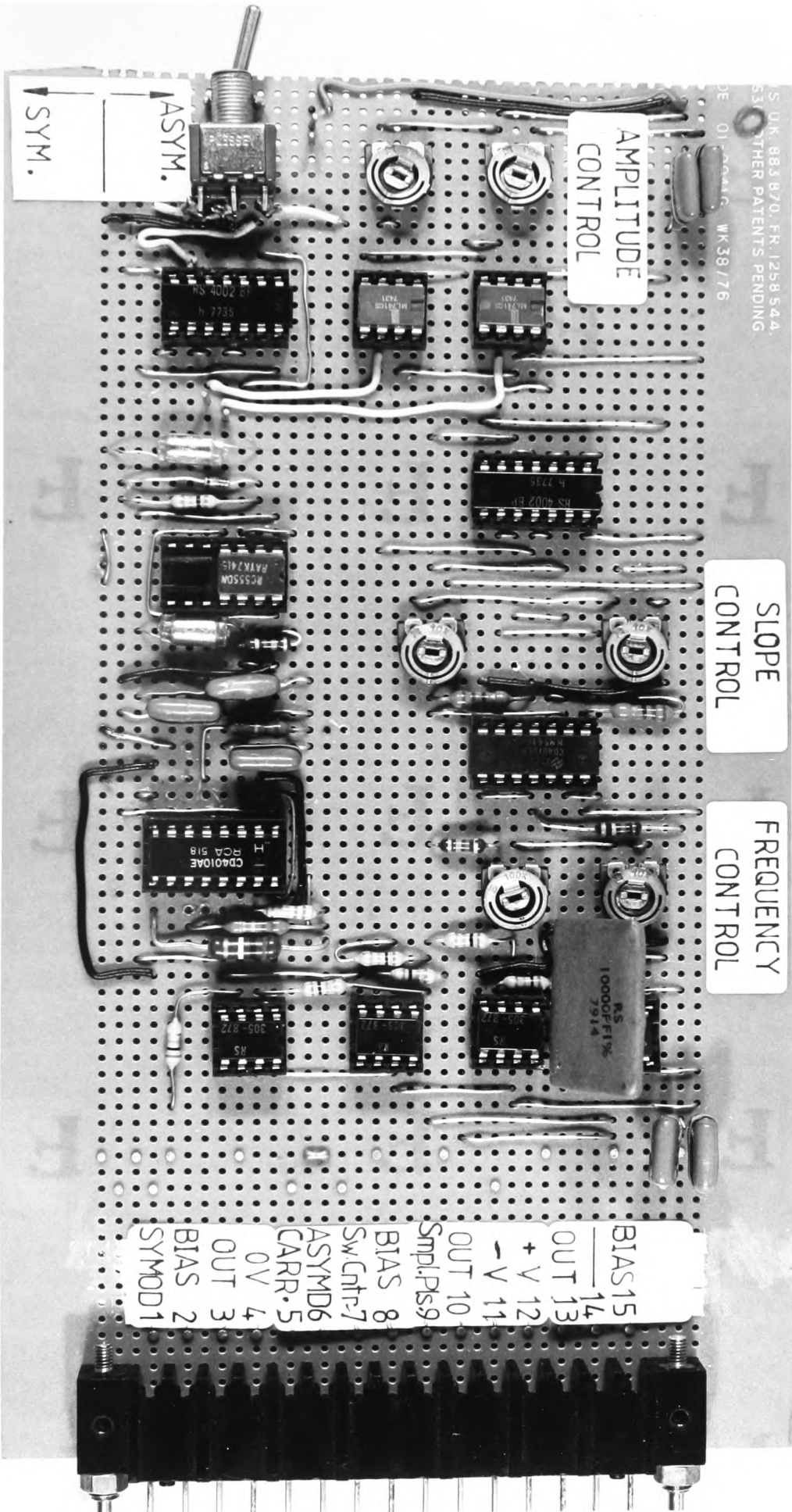
FIG 3-3

- 105 -
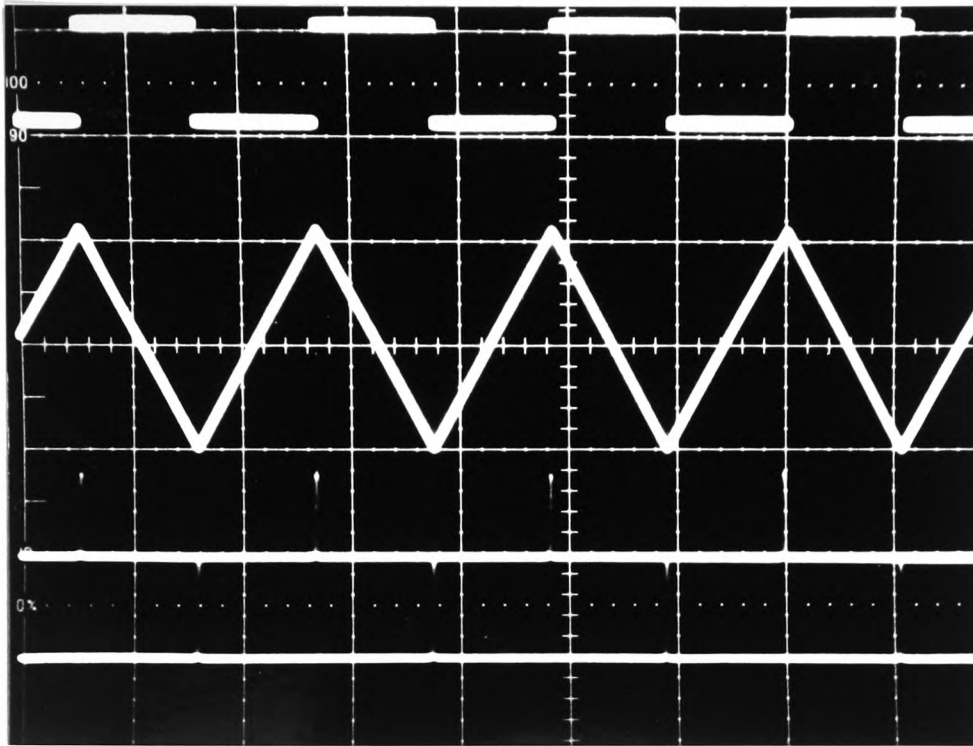
FIG 3-4
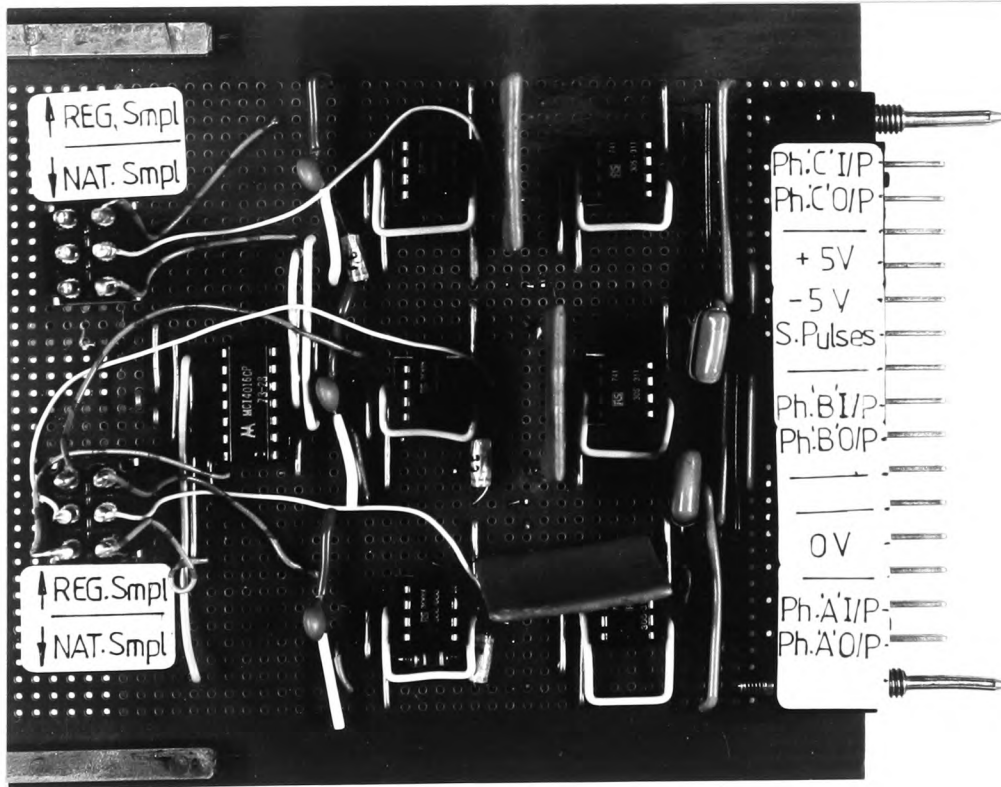
FIG 3-5

of the triangular waveform produced by the oscillator and act as the gating signal to the sample and hold network.

The triangular waveform is linked to three comparators whose parallel outputs produce the signal level, three phase, PWM waveforms. The secondary input to each of the comparators is obtained from the three-phase sample and hold unit.

3.1.2 The Three Phase Sample and Hold Unit

Each of the three phases is divided into three sections; a voltage follower which provides a low impedance input to the second section - the sampling MOS switch [69] and the storage capacitor. The output voltage from the capacitor is buffered with another voltage follower which provides a low output impedance so as to ensure that a minimal amount of interference is induced in the interboard wiring Figure 3-5.

The main design criteria were to provide a low impedance Mosfet switch such that the capacitor could be charged to the highest voltage within the specified gating period of $50\mu S$. Further the gating signal leakage from the Mosfet was to be kept to a minimum whilst, in order to minimise 'droop' levels, the storage capacitor should be connected to a high-impedance, low-leakage amplifier. A switch is incorporated to select either of the two signals, that is, the regular sampled or natural sinewave. The switch was placed on the circuit board in order to avoid pick up interference on long wires to control boards. The three phase output from this unit is connected directly to the inputs of the three comparators on the waveform generator board.

3.1.3 The Three Phase Modulating Waveform Generator

This unit provided the three phase sinusoidal source necessary
for the generation of the three phase PWM signals. The design and
construction of this unit was not changed. The three phase oscillator
uses a three section R-C phase shift network. Amplitude control is
effected by the incorporation of a half-wave rectifier and R-C
smoothing network whose D.C. output controls the resistance of a J
Fet which then sets the loop gain of the oscillator. The oscillator
has a frequency range of 5Hz-300Hz in 3 switchable sub range steps;
distortion was of the order of 2%. Figure 3.6.

3.1.4 Pulse Sequence and Conditioning Unit

The purpose of this unit was to provide a set of four output
pulse waveforms, for each of the three phases (one unit per phase),
suitable for driving a McMurray type bridge inverter. Figure 3-7
shows, in outline, the system operation of the unit.

Two of the output waveforms control the main arms of the bridge,
that is the positive voltage side and the negative voltage side. It
is absolutely essential that these two pulse waveforms do not overlap,
if they do, then the positive and negative supplies are instantly
shorted together, and , in this case, the fuses will blow. In order
to avoid this problem a 100μS delay is introduced, into the
complementary drive waveforms as shown in Figure 3-8, 3-9. Whilst
each of the positive voltage pulses is reduced by 100μS, each of the
negative pulses is increased by 100μS. This allows a 100μS recovery
period at each polarity changeover.
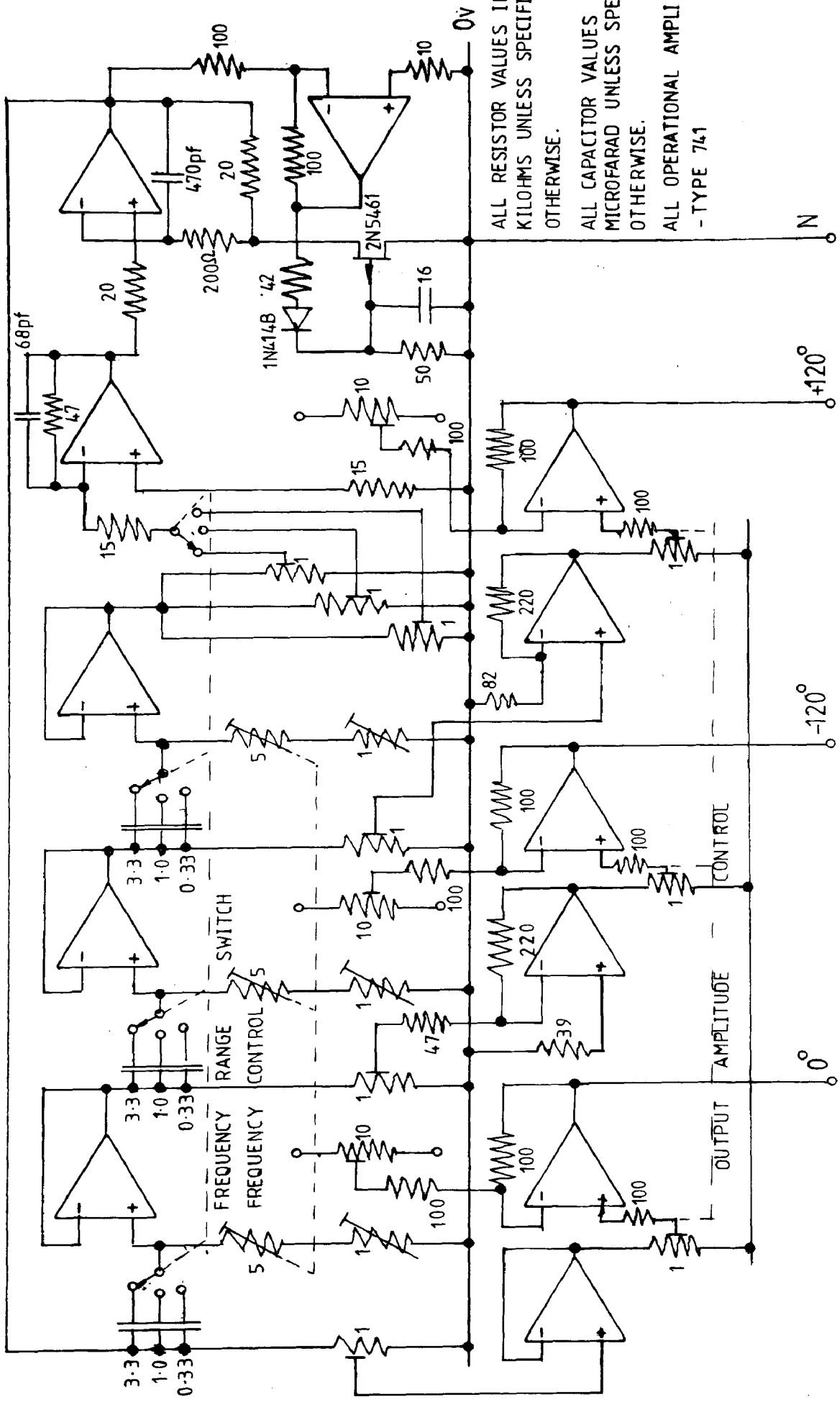
FIG 3-6

ALL RESISTOR VALUES IN KILOHMS UNLESS SPECIFIED OTHERWISE.

ALL CAPACITOR VALUES IN MICROFARAD UNLESS SPECIFIED OTHERWISE.

ALL OPERATIONAL AMPLIFIERS – TYPE 741

— 109 —

FIG 3-7

- 110 -
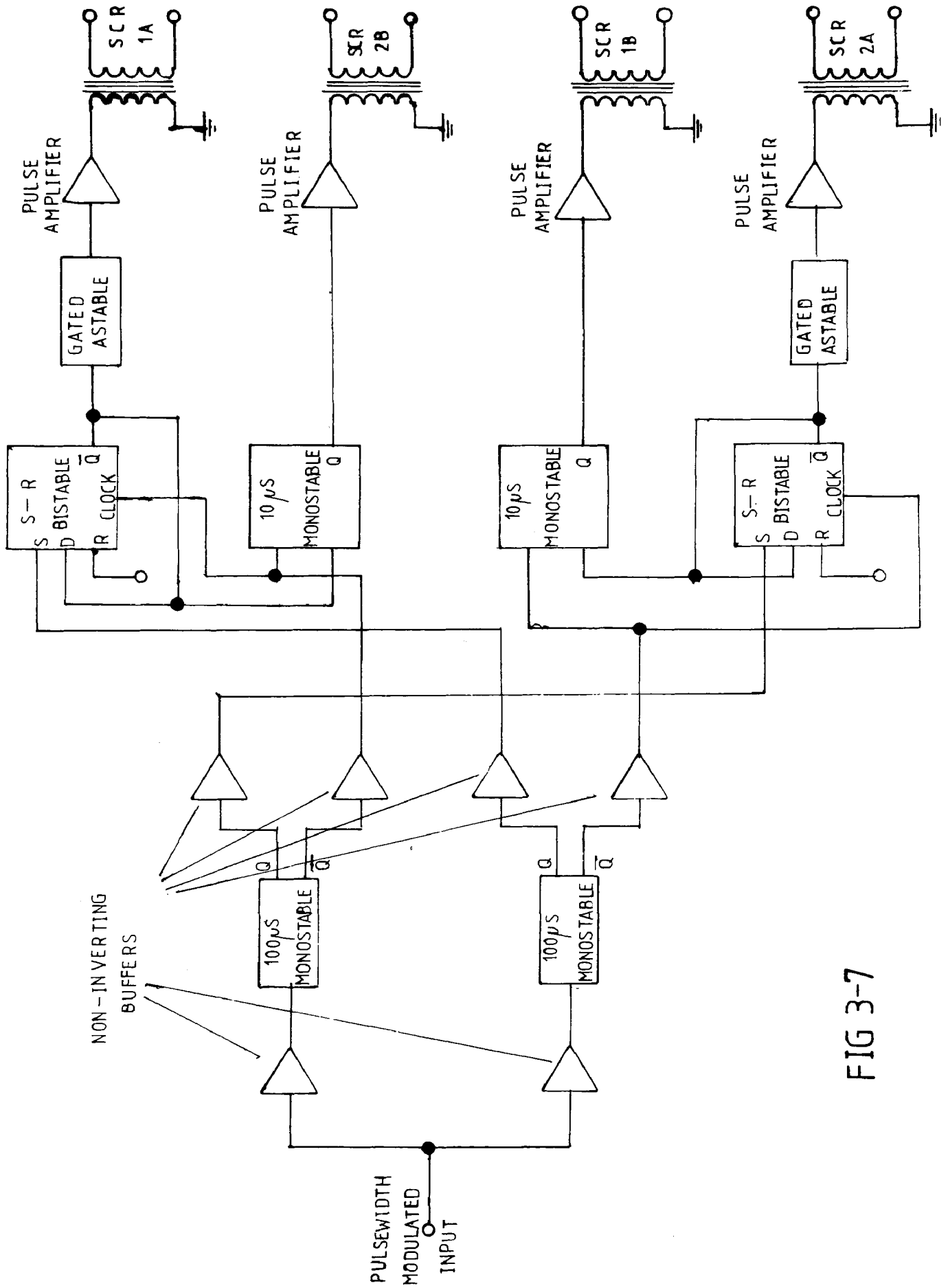
FIG 3-8
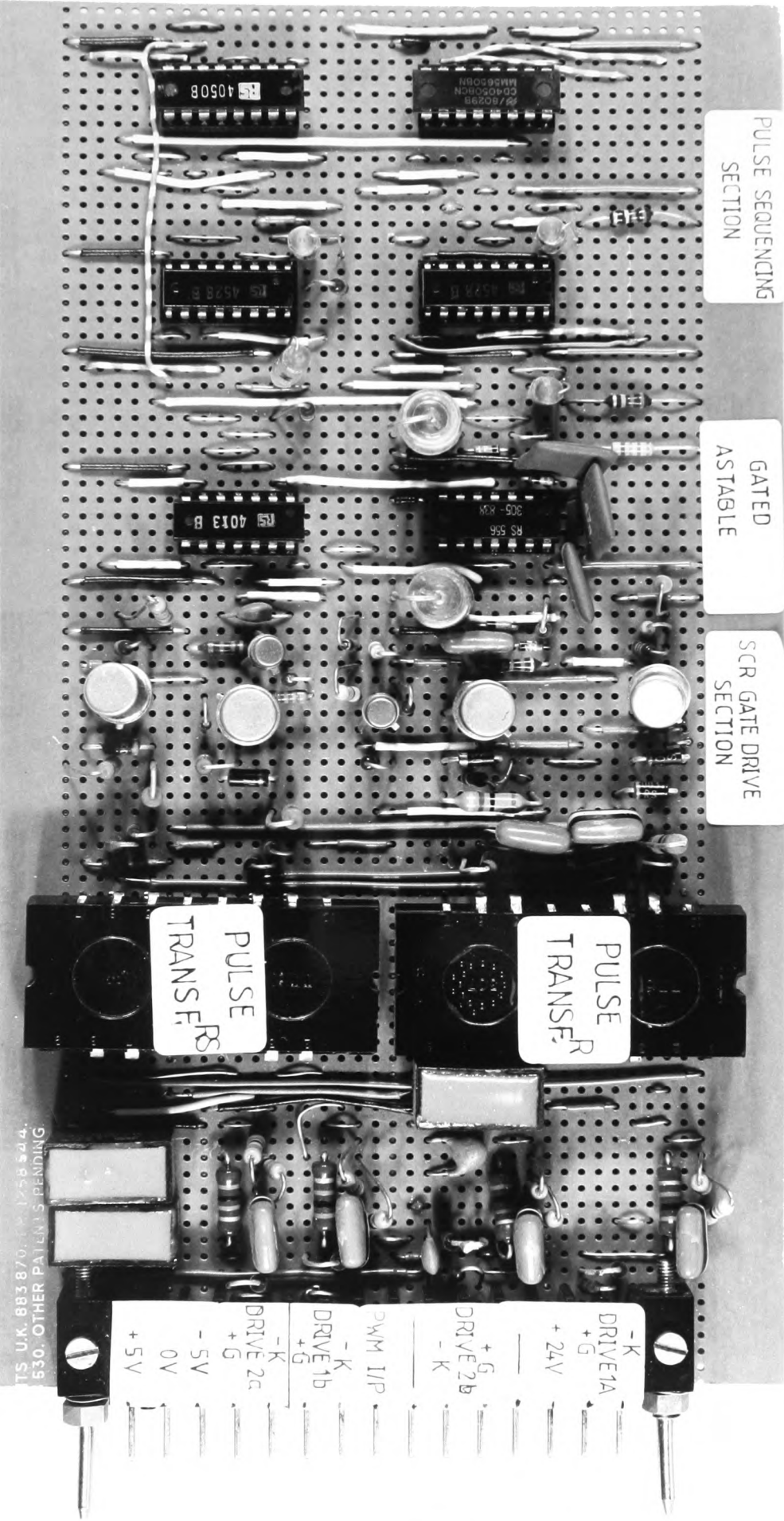
PULSE SEQUENCING SECTION

GATED ASTABLE

SCR GATE DRIVE SECTION

PULSE TRANSF. RS

PULSE TRANSF. R
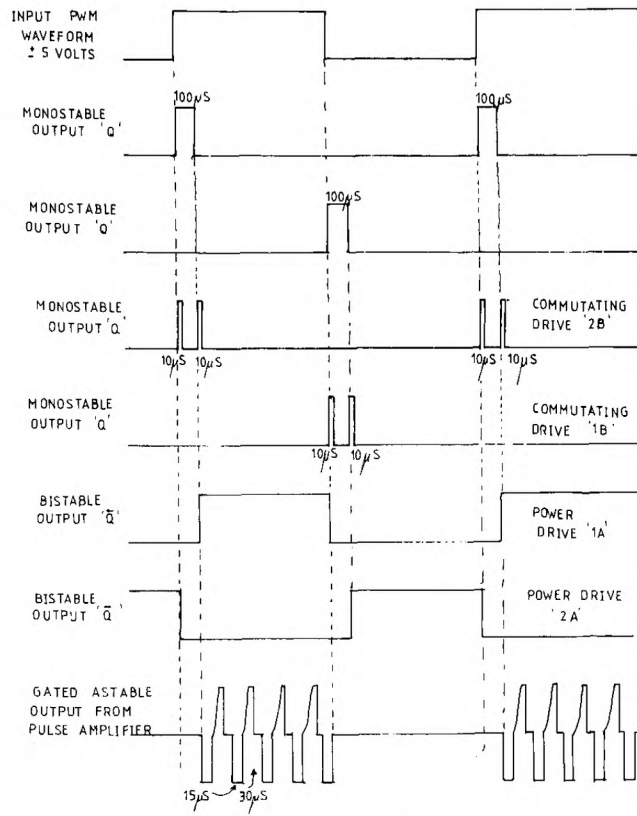
FIG 3-9
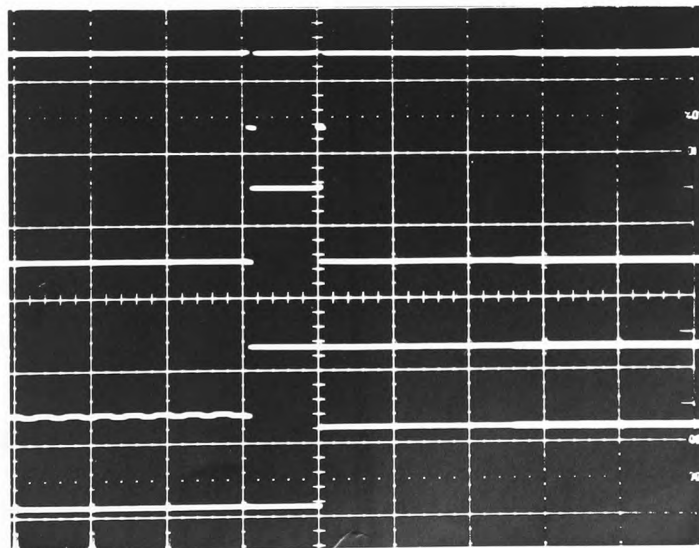
FIG 3-10

The incoming PWM waveform is used to trigger two 100µs monostables; one triggers on the positive edge whilst the second triggers on the negative edge of the PWM signal. The complementary output of monostables [72] are then interconnected to two S-R bistables. Using the truth table of the flip-flop and a pulse timing diagram it can be determined that the resultant output of the S-R flip-flop is as shown in Figure 3-10.

The Q output of each 100µs monostable is used to produce a dual 10µs pulse output, one 10µs pulse at each polarity transition of the input waveform. This pulse waveform is used to trigger the secondary commutation thyristors which then operate to turn off the appropriate thyristor. In this way, thyristor turn off is synchronised to the PWM drive waveforms.

Owing to the higher power transfer levels possible with a magnetically coupled circuit, a decision was made, to use a pulse transformer as the isolating network between the high voltage bridge and the low voltage electronic circuitry. This necessitated the provision of an A.C. drive whose pulse widths would be short enough to satisfy the voltage/time product of the pulse transformers. A gated astable circuit [73] with a 30µs period and 10µs pulse width was determined as being adequate to provide the necessary A.C. drive to the transformer connected thyristors. A pulse amplifier was also found to be necessary in order that the voltage and current levels of the thyristor gate could be achieved.

Proper decoupling, layout configuration and the provision of screened, twisted pair wiring was found to be an important aspect in determining the successful, operational performance of the units.

3.1.5 The McMurray Bridge Power Inverter

After describing the Pulse Sequence Generator Unit it is appropriate to understand the operation and requirements of the Bridge Inverter [67].

The object of the inverter is to modulate the DC input so that a dual voltage pulsed AC output is obtained. The choice of semiconductor power switch is important as this determines the design requirements of the bridge. In this case, the thyristor [74,75] was chosen and of the inverters considered the McMurray type inverter appeared to have proved itself as a rugged reliable unit suitable for the application to PWM invertors. Fast recovery thyristors are necessary in order to maximise efficiency whilst allowing the realisation of the smaller pulse widths generated by the PWM process (as compared to the quasi-square wave invertor).

3.1.5.1 Thyristor Protection

Thyristors have limited di/dt and dv/dt performances and in some cases, if the voltage change is rapid enough, an induced turn-on condition can occur. In order to avoid this condition a series R-C (or snubber) [76] network can be connected across the thyristor. This limits the rate of voltage rise since the capacitor has first to be charged before the full working voltage can appear across the thyristor. The di/dt limit is necessary in order to avoid overheating in parts of the junction within the thyristor. A simple series inductance is included to achieve this result and the relevant calculations [77] are provided in the appendix. Power diodes are

placed across each thyristor so that when it switches off, any reverse voltage transient is conducted by the diode, providing a signal path back to the supply. In this way, reverse voltage transients, across the thyristor, are reduced to 0.6 volts. Fuses are also included in series with the thyristor to provide over-current protection. The fuses are constructed from polythene containers, filled with water, into which two electrodes are placed, the ends of the electrodes being connected by a wire, thin enough to fuse at the rated current. This provided a low cost fusing system.

Having now provided adequate protection [78] for the thyristor the rest of the bridge can be constructed. The bridge needs to conduct both positive and negative currents thus necessitating the construction of two arms, one to the positive supply and one to the negative supply. Each of the thyristor arms needs to be provided with a commutating network which will be used to turn the thyristor off. A single L-C current control network can be used in conjunction with the commutating thyristors, serving to limit the reverse current rise to a level which would provide a minimum offtime of about 100μS. This acts to provide a long enough switching time such that the thyristor will remain off once the reverse current is removed. The circuit diagram of the bridge is shown in Figure 3-11 and the relevant calculations are confined to the appendix.
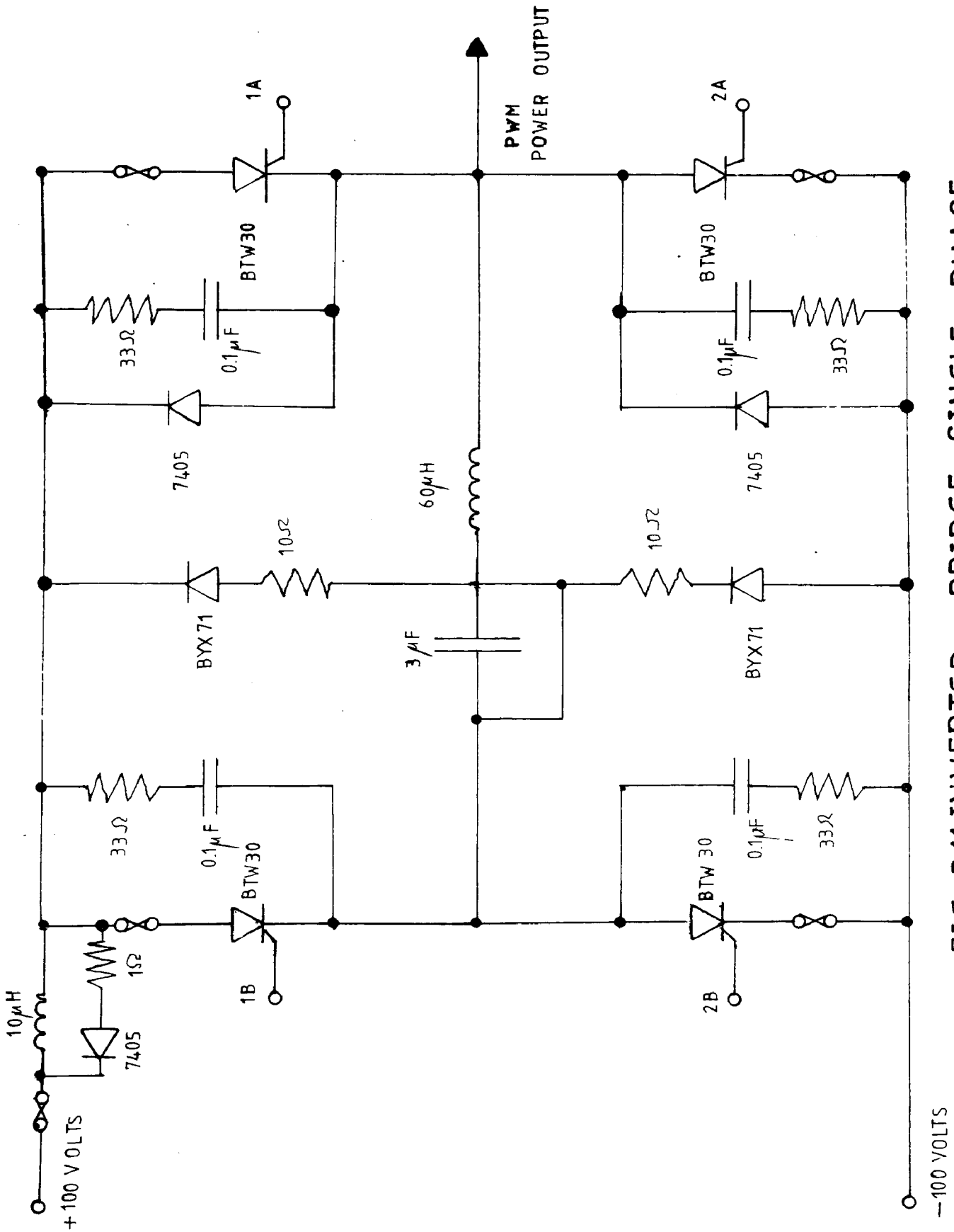
FIG:3-11 INVERTER BRIDGE -SINGLE PHASE

PWM POWER OUTPUT

1A
2A
1B
2B

BTW30
BTW30
BTW30
BTW 30

7405
7405
7405

BYX71
BYX71

0.1μF
0.1μF
0.1μF
0.1μF

33Ω
33Ω
33Ω
33Ω

10Ω
10Ω

60μH

3μF

10μH
1Ω

+100 VOLTS
−100 VOLTS

3.2 Advanced Semiconductor Technology - Discrete Switching Devices

Until quite recently the thyristor has been the most frequent choice of semiconductor switch for the control of power output exceeding about 5kW,. However. a number of developments have occurred in the semiconductor industry such that several devices, with differing fabrication processes, can now be included in the search for the optimum switch at, and above, these power levels. The power ratings of these devices have improved, dramatically in some cases, such that their application, in the field of inverters for variable speed drives, warrant serious consideration - these devices are the Gate Turn off device, the bipolar transistor, the Hexfet and Vmos device.

3.2.1 The Gate Turn-off Switch

The gate turn off switch (GTO) [79,80] is a four layer device, constructed in much the same manner as the ordinary thyristor and yet has a single significantly different operating characteristic - it can be turned off, even whilst carrying current, simply by applying a negative voltage across the gate cathode of the device. The G.T.O. is not a new device and has been known for 15 years and both RCA and International Rectifier have made batch quantities for about 2 years, although RCA have now ceased their production. The equivalent circuit of the G.T.O., like the thyristor, can be considered to be that of two interconnected transistors.

Further, in a similar manner to the thyristor if the main current, I, is sufficient for the sum of the transistor gains to exceed unity (that is $\alpha npn + \alpha pnp > 1$), then the device will latch in the 'on' state. Unlike the thyristor, the gain of the npn transistor, αnpn, is maximised whilst that of the pnp transistor, αpnp, is minimised such that $\alpha npn \gg \alpha pnp$. It is this property which allows a negative gate drive to interrupt regeneration and turn off the device.

In the early stages of development progress was hampered by the need for large negative turn off voltages, whilst the degree of process control could not be precise enough to render viable yields. However, with the increasing demand for LSI chips diffusion equipment and other associated operations such as photolithography have been improved to the point where production of G.T.O. devices has become a commercial proposition.

Due to its four layer construction the G.T.O device will withstand higher voltages, dv/dt levels, and overloads whilst requiring only a fuse for circuit protection. Mullard presently produce the BTW50 and BTW58 which has a dv/dt rating of 100V/μS whilst being able to turn off 10 amps, with a −10 volt gate bias, in less than 1μS. The BTW58 requires a gate current pulse of 100mA to switch on a 5 amp load whilst other devices are planned to have a blocking voltage of 1500V.

International Rectifier are considering two devices, 500A with a blocking voltage of 1200 Volts and 100A (average) with a capacity to interrupt 1000A in 5μS at a blocking voltage of up to 1200 volts. Toshiba have already produced, designed and incorporated a G.T.O. device handling loads in excess of 60kW in a three phase static

power supply for air conditioned coaches. Several devices have been developed by The Toshiba Research and Development centre, 600V, 200A; 600V, 600A; 1300V, 600A; and now 2500V, 600A, with a negative gate bias requirement of 5 to 10 volts, whilst the turn off pulse requirement was -40 volts at -200 Amps with a di/dt requirement of -20A and a pulse width of 20 to 30 μS. The main disadvantage in use is the low turn off gain of the device which demands a higher power gate drive signal.

3.2.2 The Bipolar Transistor

The improvements in semiconductor processing which has enabled the development of the G.T.O. has also allowed the production of transistors with accurately controlled base widths and collector regions [81,82,83]. This has enabled the commercial production of transistors with large well defined sustaining voltage characteristics. Westcode Semiconductors has already produced transistors which have an 800V, 250A characteristic and expect to be producing a 1000V 500A transistor within the next three years. The advantage of the transistor over the thyristor is that it can be turned off, whilst carrying load current, by the application of the appropriate base emitter bias voltage. No auxiliary commutating components are required which can lead to a 30% improvement in the size and weight of PWM inverters for motor control. However, the transistor cannot be protected with a simple fuse (excessive dissipation can only be tolerated for about 20μS) although passive protection can be provided by over design, concise layout, the use of zener/avalanche diodes, de-coupling capacitors and RC/LC filters and

snubber networks. Active protection using current/voltage transducers are inevitably more expensive and bulky although they may be required in special circumstances. Further, it should be noted that the transistor requires base drive throughout the cycle and the gain of the high power transistors is quite low - of the order of 3. Thus for a 24 Amp handling capability a base drive is required which provides 8 amps throughout the 'on' time of the power transistor. The cost of transistors may be somewhat higher than thyristors for certain power handling requirements, but absence of commutation circuits and the elimination of corresponding commutation losses may make the transistor more economical and efficient. It is significant that a number of authors have reported the use of transistors in bridge inverters. [84,95,96]

3.2.3 The Hexfet

The Hexfet [84,85], although a great improvement over other power Fet devices, is still limited to power handling capabilities below 5kW. International Rectifier are particularly active in this field and produce the IR150 which can pass 25 amps continuously with a sustaining voltage of 100 volts. The IRF350 can commutate 300 volts at 11 amps (25 amps pulsed) with a corresponding 'on' resistance of 0.3 ohms. It is perhaps unfortunate that these devices seem to be limited to this level of power as their switching characteristics are so near the ideal. Very little power drive is required to the gate since the device is voltage controlled rather than being current controlled. This fact ensures a minimum use of ancillary drive components for the device, requiring only a fixed DC voltage between

the gate and scource to maintain the 'on' condition. Other advantages of power Mosfets are related to the negative temperature coefficient of their drain current, which prevents the formation of thermal instabilities and simplifies the paralleling of devices to increase net current handling. By contrast, the bipolar transistor needs ballasting, as well as careful device matching, to prevent thermal runaway.

3.2.4 VFets

VFets [21], so called because of the geometry of the fabrication process, have exactly the same drive advantages as the Hexfet. Siliconix seem to be the active company in this field, although a device with a sustaining voltage of 100 volts, and an 'on' current of 25 amps, has been produced it appears that the device structure is such that its sustaining voltage cannot be improved upon. The application of this semiconductor switch will thus be limited to relatively low voltage motors, well below mains voltages.

Field-controlled thyristors

The field-controlled thyristor is another recent device innovation of interest for power-switching applications. Its structure is similar to that of the JFET, except for the presence of an injecting contact at the bottom of the wafer. This alteration makes profound changes in operation, because now minority carrier injection from the anode modulates the conductivity of the drift region during forward conduction. Consequently, field-controlled

thyristors can operate at current densities 10 times greater than those of MOSFETs and three times larger than those of bipolar transistors.

This improvement in the forward conduction characteristics, however, is made at the price of much larger gate-drive currents and slower switching speeds, because of the need to remove the injected minority carriers during switching. The GE Research and Development Centre has developed laboratory surface-gate structures that have breakdown voltages of up to 1000 V and current-handling capabilities of up to 10 amperes at switching speeds of less than 1 microsecond. These devices have also shown good high-temperature operating characteristics. Similar devices of buried-grid structure have been developed at Hitachi in Japan under the name of "static induction thyristors," their break-down voltages have been measured at up to 2500 V, and current-handling capabilities of 500 A have been reported-albeit at a reduced switching speed of $6\mu S$.

Field-controlled thyristors are promising for applications at frequencies between 1 and 10 kilohertz, because their switching speeds are superior to those of conventional thyristors and their operating-current densities are higher than those of bipolar transistors and MOSFETs.

Power-device designers have also been able to integrate MOS gates into the conventional thyristor structure (MOSCR). In this device, the MOS gate is used to trigger the thyristor structure from its blocking state to its forward-conducting state. The first devices of this type were fabricated at the GE Research and Development Centre with a V-groove structure. More recently, Siemens has applied its

SIPMOS (polycrystalline silicon gate MOS) process to fabricate DMOS structures that can handle about 40 kW. In addition to the advantage of requiring very low input gate-drive currents, this gate structure allows the decoupling of the gate sensitivity and the dV/dt capability of thyristors for the first time.

A table comparing the different devices is given in Figure 3-12. For low power, high frequency applications the MOS inverter has the attraction of reduced losses and low gate drive requirements.

3.3 Integrated Circuits (SSI-LSI)

Steady advances continue in the field of small scale integration. The number of devices circuit complexity, in a single silicon chip has been increasing yearly by a factor of two for a period which has now exceeded 20 years. It also appears likely, from the literature, that this scale of reduction will continue for at least another 10 years through to 1990. The scale of this miniaturisation has been more obvious in the field of digital electronics, however, in the analogue field, it is now possible to obtain several DC amplifiers or monostables in a single 16 pin package. In particular it is now possible to obtain a waveform generator chip from Mullard, the 8038CC, which contains all the elements for producing a sine, triangle and square wave which can be used in the generation of PWM signals.

Device characteristic	Bipolar transistor	Gate turn-off thyristor	MOSFET	JFET and static induction transistor	Field-controlled thyristor (FCT)	GaAs FET
Comparison of operating characteristics for gate turn-off devices						
Normally on/off	Off	Off	Off	On	On	On/off
Reverse blocking capability, volts	< 50	500 to 2500	0	0	500 to 2500	0
Breakdown voltage range	50 to 500	500 to 2500	50 to 500	50 to 500	500 to 2500	50 to 500
Forward conduction-* current density, A/cm²	40	100	10	10	100	100
Surge-current-handling capability	Poor	Good	Poor	Poor	Good	Poor
Maximum switching speed (approximate)	200 KHz	20 KHz	2 MHz	2 MHz	20 KHz	2 MHz
Gate-drive power	High (large base-drive current required during on-state and for turn-off)	Medium (large turn-off gate currents required)	Low (only small capacitive charging currents required)	Low	Medium	Low
Operating temperature, degrees centigrade	150	<125	200	200	200	200

*The forward current densities are compared here for 500-V devices operating at a forward voltage drop of 1.5 V.

FIG 3-12
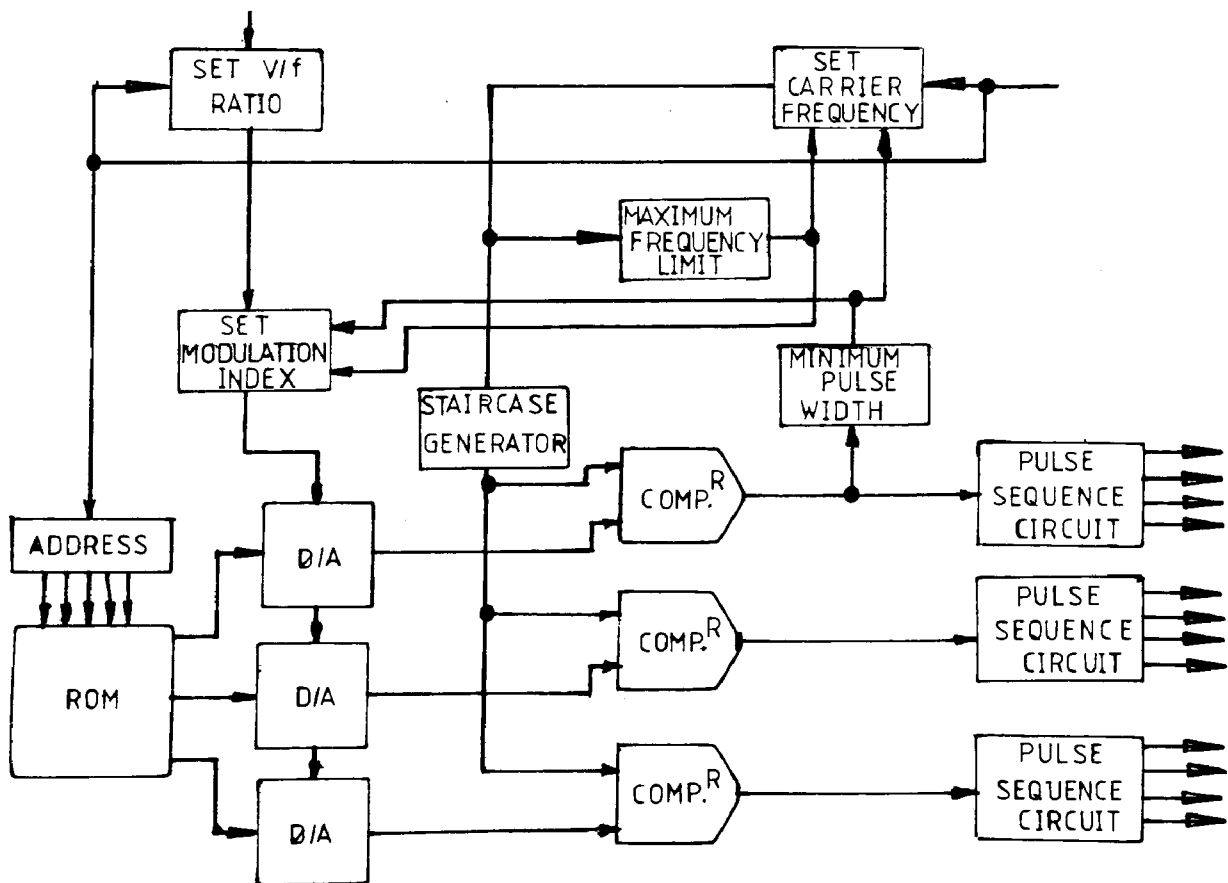
FIG 3-13

3.3.1 ROM Pulse Width Modulation

Techniques of producing Pulse Width Modulation using Read Only Memories have already been reported in the literature [47,87,88]. This approach offers more flexibility than a direct design approach [87] since the ROM has become available as an EPROM in which programs can be more easily altered for updating system operation.

One approach uses the ROM to store a matrix of information which is addressed in two orthoganal directions. One address (the source address) relates to the frequency of the supply waveform. The other address is related to the speed of the motor. The technique is used in application to a cycloconverter and a similar approach can be used in systems concerning PWM inverters. This particular system is less flexible and more complex than would be expected and a new ROM is required for each different power level output.

Another technique [88] uses three pulse generators to overcome the problem of voltage control. A pulse generator sets the output of a bistable which is used to generate a symmetrical square wave which is then used as the basic carrier waveform. The ROM stores a sine weighted pulse train and the number of sinewave steps is fixed at this point. Each number (n) stored as a sine weighted pulse, is then modified by a second pulse generator and the resulting value is utilised to modulate the pulse width of the bistable. This system controls the voltage amplitude of the fundamental modulating signal. The frequency of this signal is set by a third pulse generator which controls the rate at which 'n', modulates the pulse width of the bistable. Figure 3-14. The bistable waveform is modulated

asymetrically and in neither paper is any mention made of the frequency content of the output PWM waveform. In the system described by Edwards, the ouput must contain a significant number of undesirable harmonics.

Another ROM approach by Szabados [89] appears even more complex and uses three ROMS, a binary rate multiplier, up-down counters, address counter and digital comparator to produce a single phase PWM signal whose amplitude can only be controlled over a 12% to 97% range. Perhaps the most practical of all the ROM PWM design approaches is that due to Wilson. Here, the author attempted a direct digital simulation of the analogue PWM circuitry – only a single ROM is required. In Figure 3-13 a circuit outline of the configuration is provided. A ROM containing the basic sinusoidal reference is read at a rate corresponding to the desired fundamental frequency. variable gain digital – to – analogue converters produce the analogue sine wave reference from the ROM digital output. The triangular waveform is produced by using an up down counter and D/A converter. A simple comparator is then used to produce the PWM output. A sequencing network is included so that thyristor switching overlap is avoided.

The appearance of the Mullard PWM IC HEF4752V probably concludes the field of research into the application of ROMS to the production of PWM waveforms. The system is based on the one, already described [88] and the unit has been included in a commercially produced, three-phase, power controller for induction motor speed control [90]. Further research on the application of this IC is being conducted by Grant at Bristol University in an effort to formulate a practical approach to the problem of producing a workable PWM waveform strategy

wherein pulse numbers can be simply changed without undue variation in the amplitude and frequency of the fundamental waveform.

ROMS can reduce the package count when applied to PWM speed control systems, no claims have been made for improved technical performance of variable speed drives implementing this technique and 'cogging' torgues have been obtained. Some freedom from the DC drift problem of analogue circuitry is achieved at the expense of reduced amplitude control (torque) flexibility. However, it is to be noted that the Mullard IC reduced package count to almost a single item - further the technique of PWM modulation ensures that the harmonic content of the output is at or near the minimum possible for this type of approach. In this particular case improved performance is almost assured as parallel supportive research is being conducted into its application to AC drives by the University of Bristol.

3.3.2 The Microprocessor

All of these progressions help to reduce costs, component counts, circuit complexity and to improve the reliability and the economics of power control circuitry. Nevertheless, a radical change has occurred in the field of LSI semiconductor systems with the advent of the microprocessor [91,92,93] and its associated semiconductor products, notably the EPROM. The microcomputer system is a stored program controller for the efficient manipulation of information in logical sequence. As such, it has an equivalent circuit as shown in Figure 3-15. Data, entered into the microcomputer is manipulated by the microprocessor under the control of a sequence of instructions (the program) stored in the memory. In particular, the system can be used
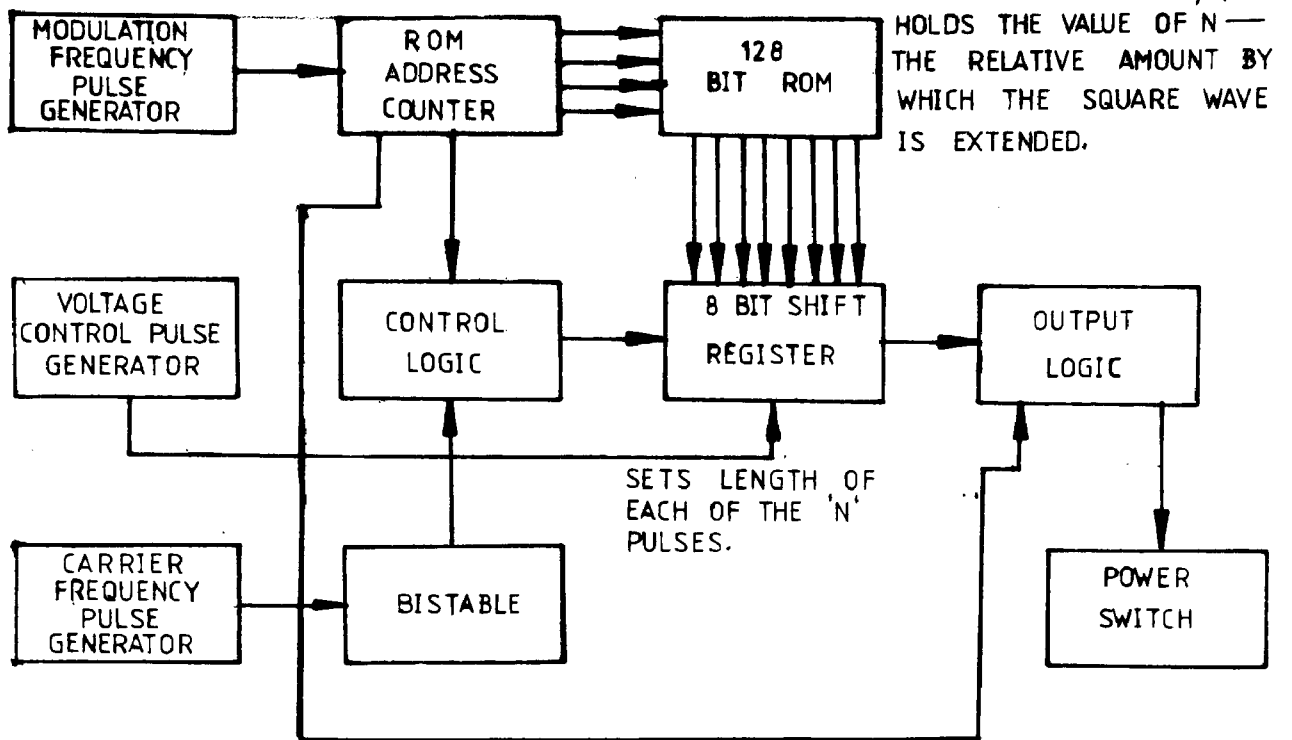
FIG 3-14
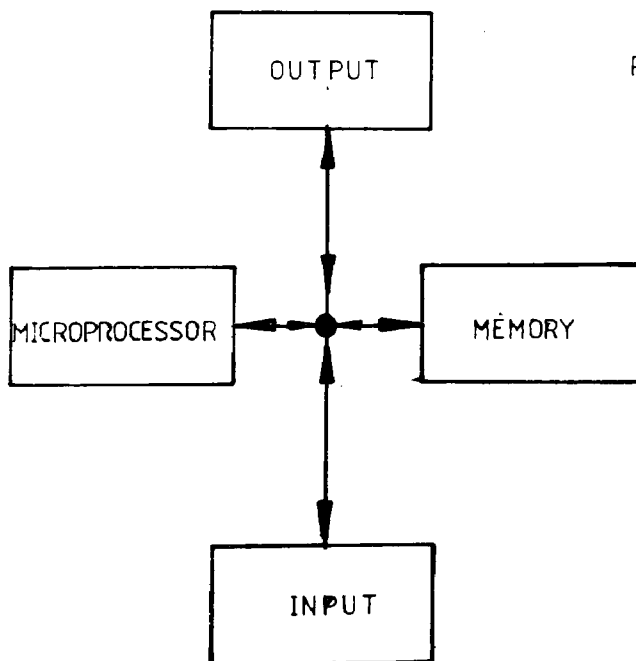
FIG 3-15
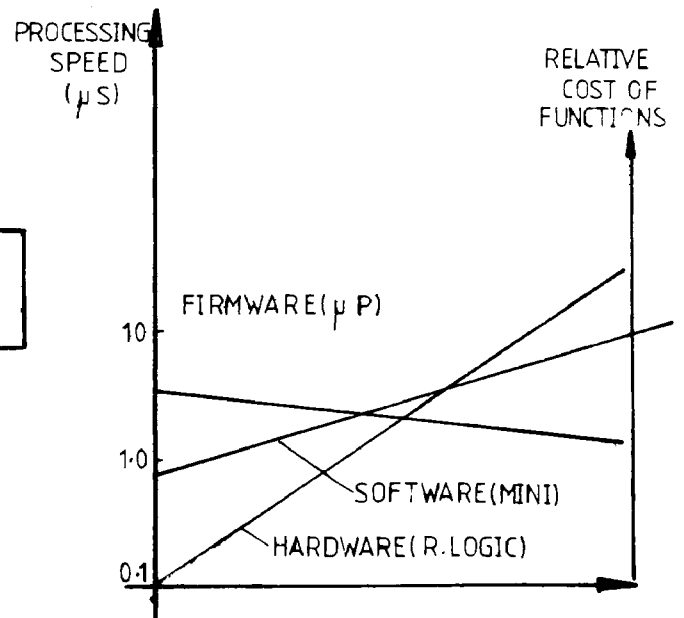
FIG 3-16

for the direct replacement of hard-wired, logic systems, and, in many cases, analogue signal processing equipment.

Thus, through the microprocessor, the medium of large scale integration of components becomes available for tasks of control as well as those of the referenced signal processing. However, stored program processing offers significant advantage over hard wired systems in that the microprocessor offers adaptability to control functions of a wide variety, providing flexibility in both hardware and software design.

As the trend towards stored program control has developed so has the design philosophy of microprocessor systems. The use of a bus structure, address, data and control lines, modular hardware and software closely coupled to the concepts of structured design and structured software are important to the successful completion of any project in this field.

Basically, these miniature computers substitute programming for logic design (logic instructions and conditional jumps for logic gates and programmed loops for time delays) and the following advantages are accrued.

1. The primary advantage of microprocessors is the short design turnaround time they make possible.

2. As a corollary advantage, easy field alterations are possible and customizing of the Unit is less expensive.

3. Maintenance and updating of the unit will be implemented in about 25% of the time it would take to modify a hard-wired system.

4. Economics - the present cost of a 6800 device is £5 for small systems, memory of the order of 2K is required, an interface section is also necessary so that in, one-off systems, it becomes economical to replace hard wired logic when the number of gates exceeds 30 - 50. In batch production, or high volume systems the figure would be less.

5. Flexibility - when a designer uses a microprocessor instead of hard wired logic, he determines the system functions by a program - a sequence of instructions - stored in memory. If he uses a read only memory, the program is immune to inadvertant alteration. Replacing the program can completely alter the function of the machine that contains the microprocessor.

6. As a corollary the same hardware can be used to perform completely different functions so that where a number of products exist, they could be rationalised to use identical hardware - only the software need be changed.

7. Automation - (greater functional capability for the same cost) control systems can be added to the software to improve the basic performance of the unit, only incurring the penalty of increased memory size. Further, the unit could be connected to a main computer for the purpose of monitoring and updating the unit. Another example is that instrument manufacturers are finding it practical to add such features as remote control, programmability, improved readout, and peripheral interfaces with little impact on

product price.

8. Reliability - fewer external connections and a reduced component count add significantly to the reliability of the system.

9. Efficiency - a single piece of hardware can be used to perform many different functions both in improving products and on the production line assembly unit.

·10. Should failure still occur, the computational capability of a microprocessor can be used to perform self diagnosing of the product to provide substantial improvement in availability of the unit.

With these advantages, a few disadvantages should also be noted. The 8 bit microprocessor is far slower than a minicomputer (and speed was noted as a problem in this design) and a greater number and degree of skills are required both for design and maintenance of the system.

It has been shown that a ROM can replace a large number of standard logic gates. For example, a single 16384 - bit ROM is equivalent, in logic power, to 100 or more TTL integrated circuits. Thus, once the basic microprocessor module is built, enormous logic power can be added with only a few additional integrated circuits. As shown in Figure 3-16, the cost of microprocessor system grows at about 15 percent. of the rate of growth for TTL systems. The main cost of the microprocessor system is the cost of software development and this can be overcome with the economies of large scale production.

CHAPTER 4   PHILOSOPHY OF MICROPROCESSOR SYSTEM DESIGN

4.1   The Criteria for the Adoption of the Microprocessor in place   of

Random Logic [97,98,99,100,101,102]

The microprocessor is a miniaturized stored program processor for the efficient manipulation of information in logical sequence. The fundamental difference between the discrete logic and microprocessor implementation of a given system is the inherent parallel nature of random logic arrays and the basically serial nature of the microprocessor logic. Further the number of packages required in the microprocessor implementation would be significantly lower, the wiring is not random and has a bus structure, whilst the system can be updated or redesigned simply by changing the ROM or the program stored in the ROM.

The compromises necessitated in the design of the microprocessor have also determined that it is slower in logic execution than its TTL counterpart (logic operations being achieved in microseconds, for the lower cost 6800, 8080 and 6502 systems, rather than nanoseconds). However, in many real-time applications such as industrial control, automatic vehicle control and instrumentation monitoring, required response times are often of the order of 10-100ms which can thus be simply accommodated. Further, where required,. response times are lower than this, the use of Interrupts and Direct Memory Access techniques can often provide the solution. In addition, the use of interrupts allows the microprocessor to divert, from its normal task, to some more important function and then return again to the original

activity. This facility can afford the appearance of parallel processing and is often found useful when, for example, new data has to be entered into a system.

Other considerations concern the total quantity of the system - is it for high volume production? Will the system require regular updating? What is the expected life cycle? All these aspects will affect the decision to use microprocessors. It is possible to be a little more specific. In 1975 it was found that if the system required more than 300 logic gates then a microprocessor replacement unit would be feasible and the amount of ROM required was based on the equivalence of 16 bits to every date function. In 1976 [102] Nichols estimated the breakpoint, for the implementation of a microprocessor system, as being 30 to 50 TTL packages and this value was being reduced. Certainly if the investment in support equipment (Assemblers, dissamblers, de-bug systems and loaders) has already been committed then the microprocessor solution can reduce costs to between 60% and 20% of the cost of the equivalent TTL circuits.

4.2 Real-Time Systems [103,104,105]

A real-time computer system may be defined as one which controls an environment by receiving data, processing it, and returning the results sufficiently quickly to affect the environment at that time. It is clear that this project is in fact a real-time system and it was found that by following the design pholosophy for real-time systems, the design objectives and coefficients could be clearly defined.

For example, during the design process it was found that there were three main types of data – transient data such as that contained in loop counters and temporary registers, intermediate data which was generated by individual program modules and important staticised data-the input/output data. By selecting separate data register areas in the memory space for each type of data it was established that this technique acted as a significant aid to design. For example, when a new module of code was being produced it was known that a certain area of memory was immediately available for loop counters and temporary data registers, further if processing errors occurred, one only needed to observe a fixed area of memory to determine where and when the data was corrupted and finally, the permanent data areas could be observed to determine that the input data was properly accepted and that the final data agreed with theoretical calculations. These principles are also related to structured programming (or structured design).

Basically the system was classified in Real Time standards, as described in Freedman and Lees [103] For example, data can be described on the following basis.

Accuracy – what are the limits or extent of errors which may cause malfunction?

Information Content – what is the information? What does it represent?

Response Time – The most important item which significantly affects cost. It is the delay between the demand and receipt of a particular signal.

This was found to be significant in respect of the delay introduced by the interrupt routine and the time taken to process input data before the output responded to this data.

Demand Level - Information rate or what is the peak level of the data flow-requirements?

Survival Time - some data exists for short periods only and needs to be staticised.

The software of the system can be divided into different layers of abstraction. For example, the control software can be divided into two areas management (software organisation such as maintenance and supervisory) and Service (useful input/output routines such as code conversion). In this case it was found sufficient to adopt the concepts of a control program and subordinate application programs - since the provision of ancilliary routines, such as memory resource allocation and device monitoring was not a critical part of the project design.

The software was divided into separate areas - the operating system, the control program and the application programs. The operating system had already been designed and was present in the MSI 6800 system. The control program was designed to transfer data and call the appropriate sequence of application programs which were functionally divided into I/O routines, code conversion, multiply, sine and so on. The control program also handled the transfer of intermediate data from one functional module to the next, each module being self-contained. The size of each module was also limited to lengths not exceeding approximately 256 bytes (or just over 200

instructions) whilst the typical length was 100 bytes. In one case, in the three phase sort routine, the module was divided into two in order that the transparency of the program could be maintained.

A decision was made to use a software polling technique in order to assess the state of the Programmable Timer. That is, at the end of a timing cycle, when the count is reduced to zero, the interrupt is transmitted to the microprocessor and the microprocessor responds by interrogating the control registers associated with the operational counters. When it is determined which counter initiated the interrupt, then new data is entered into that counter.

4.3 Structured Programming in Assembly Language [106,107,108]

Efficient software techniques through the use of Structured Programming, will lead to greater standardisation of components and the application of small families of components to meet all logic needs. The early design philosophy, related to the construction of stored program control units, was aimed at obtaining real-time efficiencies and memory space savings through the utilization of assembly language coding and programmers who had an intimate knowledge of the processor's instruction set. However, whilst efficient code was produced, it proved extremely difficult, both to understand and modify, so that new software errors (or 'bugs') and long time scales were often the result of updating equipment.

As the overall cost of producing software became a major factor in the design (as H/W costs fell) then the true meaning of efficient software became apparent. Software was then designed, not so much

with the short term view of restricted memory usage and improved response times, but more with the objects of ease of modifications or use and improving the transparency or clarity of the software algorithm.

Structured design [108] is a set of proposed, general program design considerations and techniques for making coding, debugging, and modifications easier, faster and less expensive, by reducing complexity. Simplicity is the primary measurement recommended for evaluating alternative designs relative to reduced debugging and modification time. Simplicity is introduced by dividing the system into separate modules in such a way that the modules can be considered implemented, fixed and changed with minimal consideration or effect on the other system modules. This can be achieved on the basis of functional division of the modules such that the logic of each module can be easily distinguished by sets of differing test procedures. Programming constructs which facilitate assimulation of the logic of modules can be defined as follows :-

4.3.1   A Module

A module is a collection of logically related code that is part of a program. Generally, the length of a typical module is defined as 100 lines of code whilst a second requirement is that it should have a single entry and exit point.

4.3.2 The Sequence Statement

This structure Figure 4-1 is the most fundamental of the structures and it provides for two functions to be executed in the order they appear.

4.3.3 The IF THEN ELSE Statement

The use of a straightforward if-then-else construct is as shown in Figure 4-2.

In assembly level coding the above construct would lead to an unstructered program in the sense that an unconditional branch or jump statement would be required since the construct implies parallel programming. This can be avoided by cascading two if- then-else constructs as shown in Figure 4-3.

4.3.4 The Do-While Statement

This structure provides for the repetitive execution or loop operation required by most computer programs Figure 4-4.

The logical flow passes through the merge point to the decision symbol. Here a logical expression is evaluated, if it is true, the process represented is executed and the expression is evaluated again. This interactive operation continues as long as the expression tested is true. When it becomes, false, there is an exit from the structure. Because the expression controlling the loop is tested first (before the process is ever executed) it is possible that a false conditon may

FIG 4 -1

FIG 4 -2

SINGLE
ENTRY

TEST ?

✓

X

PROCESS 'A'

TEST ?

✓

X

PROCESS 'B'

SINGLE
EXIT

FIG 4-3

SINGLE
ENTRY

PROCESS 'C'

TEST ?

✓

X

SINGLE
EXIT
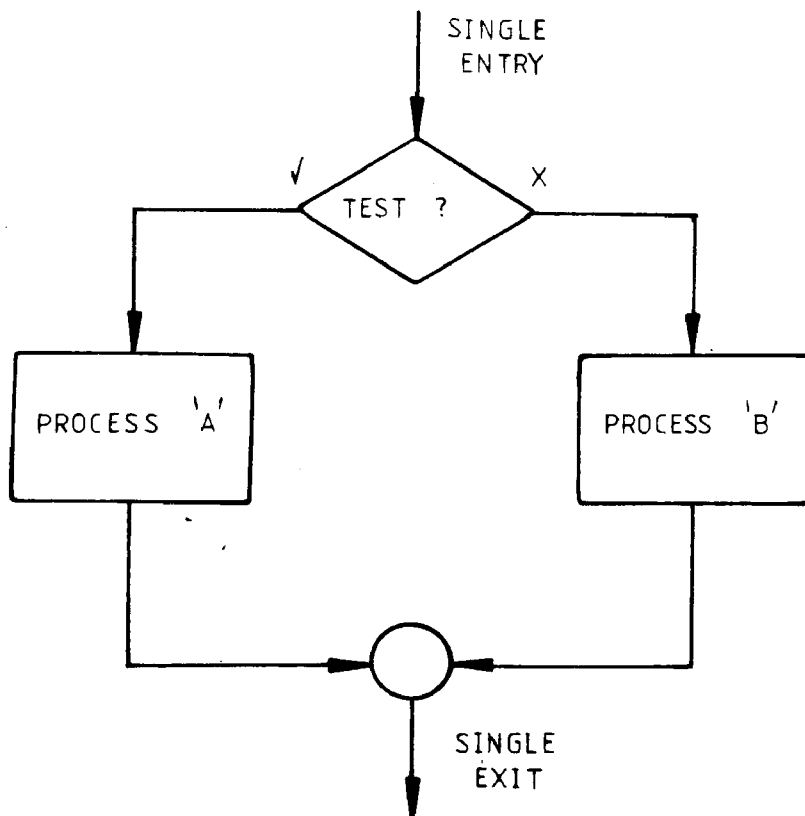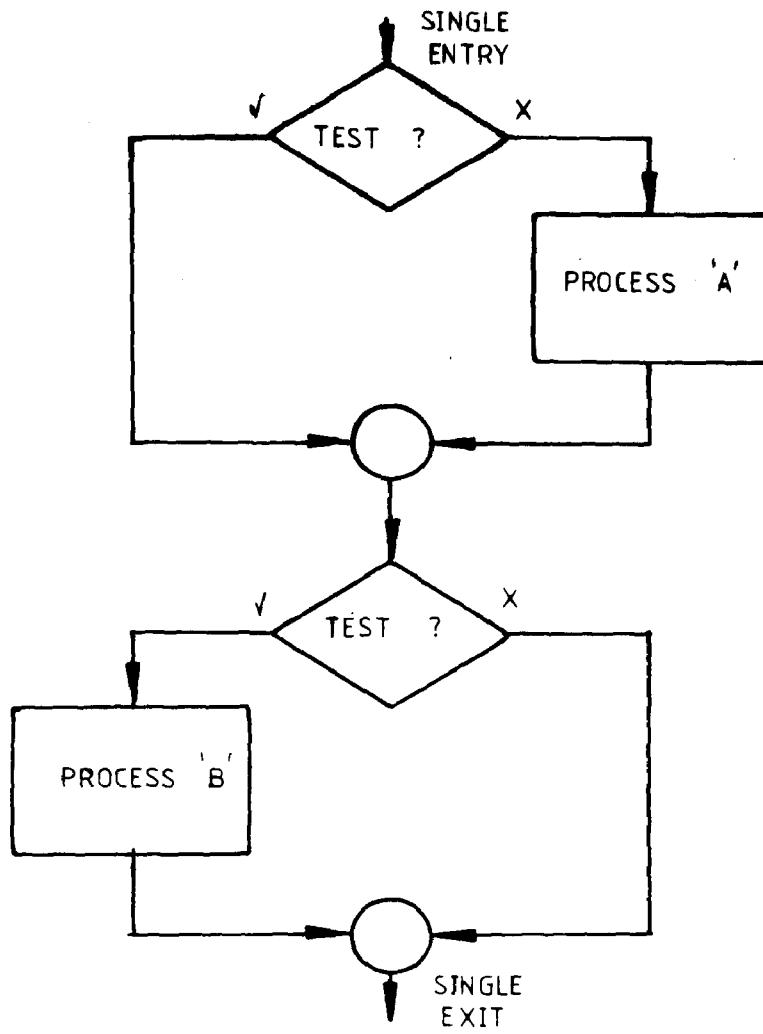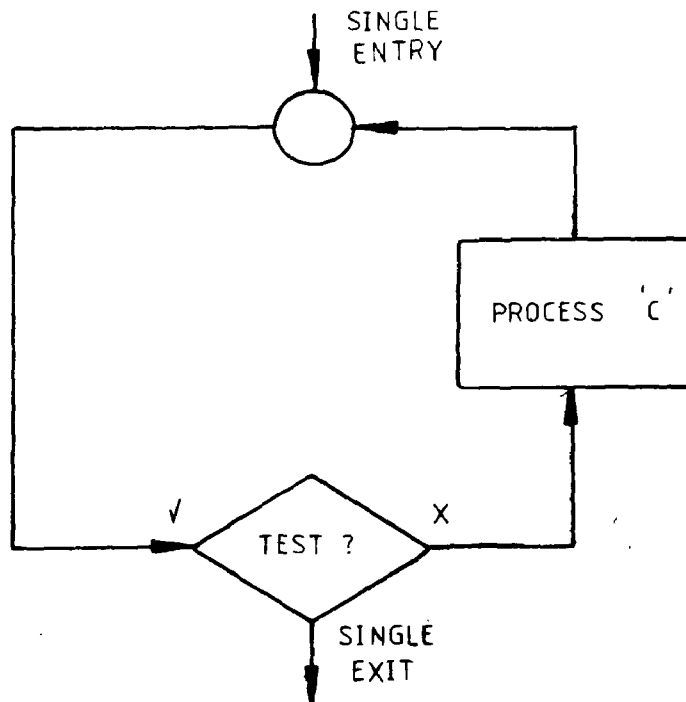
FIG 4-4

initially exist - in which case the process statements are never executed. The statements represented by the process box must modify the control variable affecting the test - otherwise the program will be an endless loop.

These basic structures can be combined, with each other, as required by the program i.e. wherever a rectangle appears in the diagrams it may be replaced by any of the basic structures Figure 4-5.

In this way these building blocks can be combined in endless variations to solve all types of program logic requirements.

It is important, with all modular programs, to maintain the vertical hierarchal structure of the implementation. Figure 4-6.

Since all of the conditional branch instructions of the 6800 microprocessor can only address a limited area of memory (approximately 128 bytes) then it must be accepted that fully structured programs cannot be written for most systems. However, the more structured and modular the program is, the easier it will be to read and de-bug.

4.4   Writing Programs [109,110,111,112]

It is not proposed to describe all 72 instructions in the M6800 instruction set since this information can be obtained elsewhere [112]. The important points to understand, before writing a program, are the differences in the addressing modes and to take care in the calculation of the address constant required in the relative address
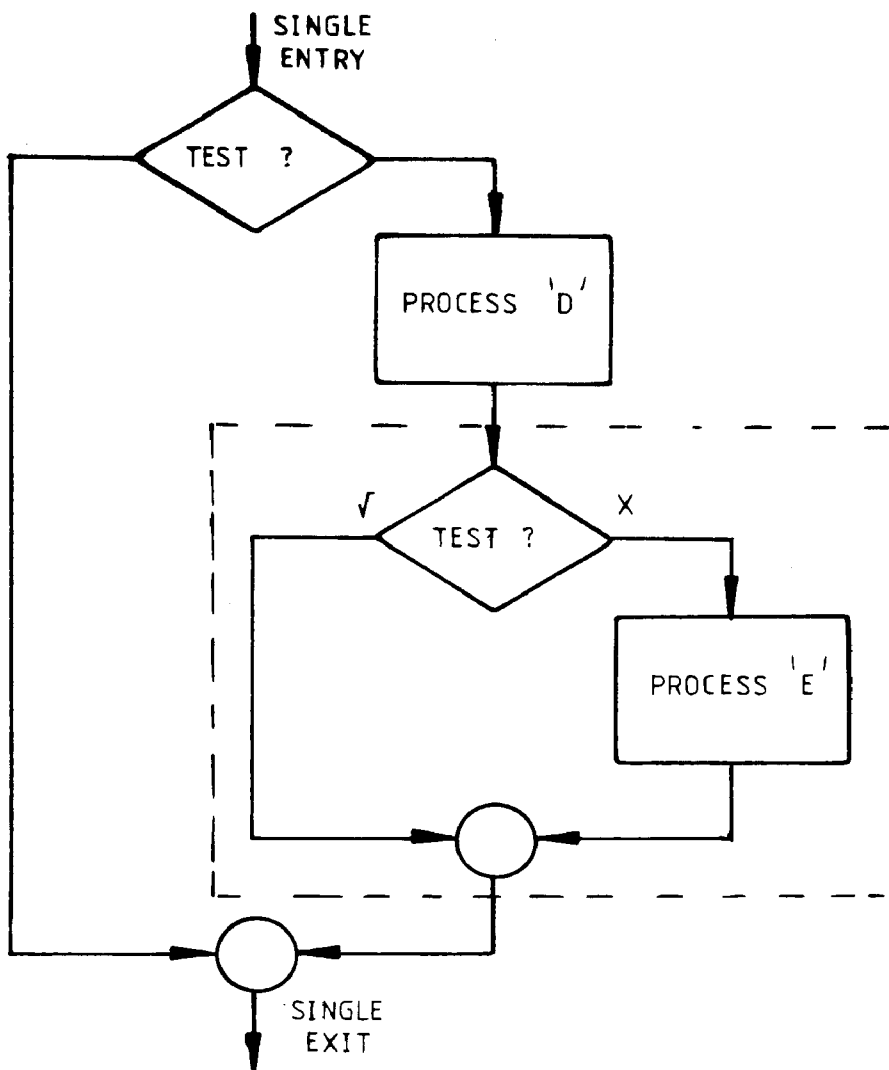
FIG 4-5
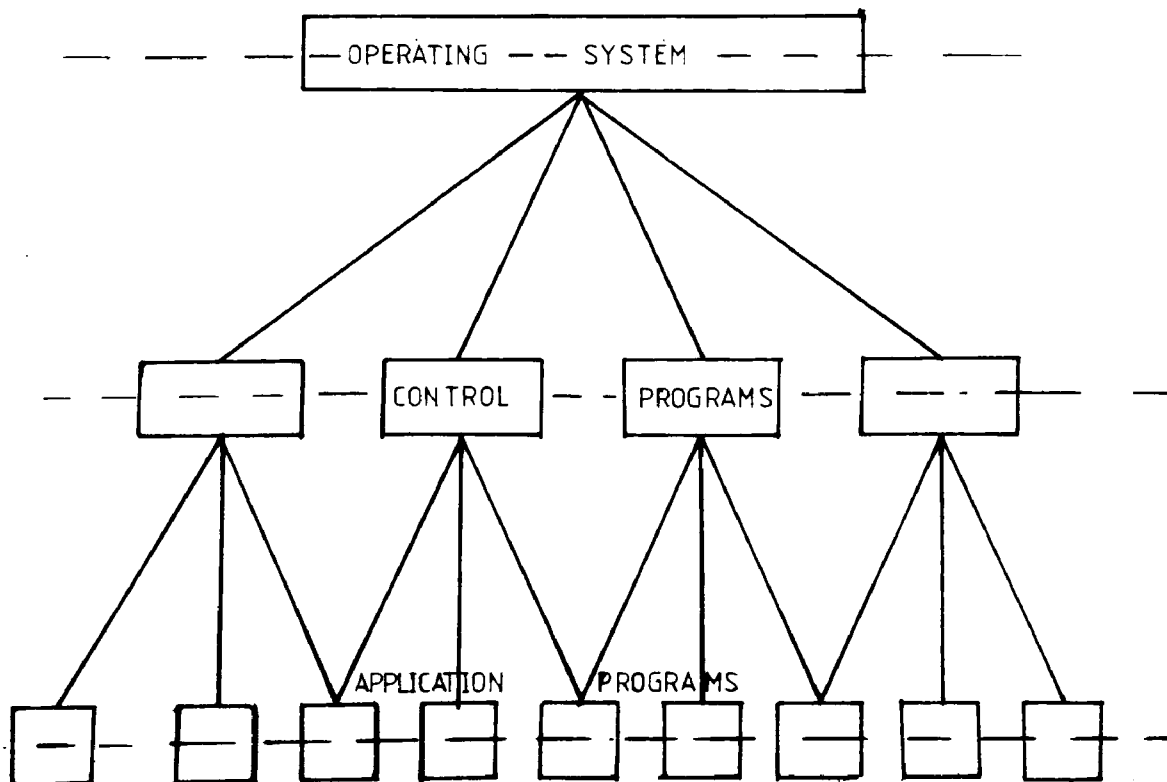
FIG 4-6

mode.

Further the instruction set divides, generally, into several
categories as follows :-

4.4.1   Register Transfer Instructions

These cause the microprocessor to transfer the contents
from one register to another. This type of instruction
specifies the addresses of the original and the destination
registers. One of the registers can be a word in the main
memory or in the input/output interface.

4.4.2   Arithmetic and Logic Instructions

These will cause the machine to perform operations of
either addition or subtraction, or logic AND, OR, compliment,
compare, and so on, on data in the accumulator with some data
in another specified register or location. These instructions
manipulate or modify data.

4.4.3   Skip, Jump or Branch Instructions

These will cause the machine to change or break the
program counter incrementing routine by skipping or fetching an
instruction located at a specified address. The 'jump' or
'branch' is either conditional or unconditional.

4.4.4 Machine Operational instruction

These will cause the machine to HALT, WAIT, or STOP the operations; normally they do not involve an operand - that is, the operation does not involve a register or an address.

4.4.5 Machine Status Testing Functions

Although it is possible to move the content of the accumulator to output for inspection, it is often desirable to know only the status of the accumulator or if the accumulator is zero, negative, or positive and so on. They are used to provide the premises for conditional jump instructions.

Further the 16 bit index register can be very useful, not only for loop counters and indexed addressing, but also for transferring data two bytes at a time. The M6800 will automatically store the higher byte first and the lower byte in the next address space. Further, when the Index Register is fully utilized, 16 bit additions can still be handled by concatenating the two 8 bit accumulators, A and B, since the necessary carry instructions are available. Another useful programming aid is that it is quite simple to divide or multiply by 2, 4, 8 and so on, this being achieved with the instructions ROR and ROL which shift the contents of the accumulator one place to the right or left as required. Further, it requires one less clock cycle to clear a register rather than to transfer a zero byte to that register although this does reduce the flexibility of the program (that is, if at a later stage you decide that you want to offset the data, then the program would have to be relocated if the

'clear' instruction has been used).

It is also advantageous to record that the use of the index register in program loops can radically increase the execution time and although it uses more memory space and can appear more unwieldly, it is often advisable to use the 8 bit byte registers and instructions in order to save computation time.

A further technique adopted in the testing of programs was to introduce, SWI, the software interrupt instruction. This command immediately causes the microprocessor to halt, in the execution of the program, and displays the contents of the internal accumulators and registers of the microprocessor. The contents could then be examined in order to ascertain the proper logical functioning of the program.

Although the finite state machines approach to design was not adopted during the design process, it was found useful to produce flow charts of the logic operation. This procedure often improved the clarity of the logical sequence of the program and enabled the appropriate corrections, where necessary, to be implemented.

4.5   The Choice of Microprocessor [113,114,115]

Choosing the appropriate microprocessor for the application is only part of the selection process. It is the whole family of support chips, which come with the microprocessor, which should be considered together with the systems and software backup facilities and equipment provided by the manufacturer. There are over thirty different kinds of microprocessors in the market. Selection can be based on the following considerations :-

4.5.1 Architecture

Features such as word size or the number of bits per word; arithmetic and logic operation properties; input/output capacities; stack/scratch pad registers; interrupt and direct-memory access capabilities should be considered individually.

4.5.2 Speed of Operation

It is important to note that mere comparison of machine code cycle times among microprocessors is sometimes misleading. There are instructions which require more than one machine cycle. A designer should therefore consider speeds based on how frequently instructions requiring more than one machine cycle occur, as well as the machine cycle time itself. Where speed is at a premium it is usually advisable to adopt bipolar devices, using the bit slice chips, stacked to achieve the appropriate word length.

4.5.3 The Instruction Set

It is not necessarily true that a processor is better if it has a larger instruction set compared to others. The designer should investigate whether he needs the extra instructions or whether extra instructions are included simply to overcome a poorly derived instruction set. Microprocessors usually have fixed instruction sets although some

microinstructions can be microprogrammable. In the latter case greater efficiencies can be achieved by designing sets of instructions tailored to specific applications.

4.5.4 Total Cost

· It is not sufficient to consider the cost of the microprocessor only. Some microprocessors demand more support circuitry than others, requiring additional power supplies or interface circuitry. It is the global effect on cost, of the choice of the microprocessor which needs to be considered, in particular, as hardware costs fall even further the cost of producing and debugging the software will dominate the total system cost of a microprocessor unit.

4.5.5 Software Support and Second Source

It is important to determine the degree of software support which can be obtained from the manufacturers. Software costs are now greater than hardware costs and although many manufacturers provide assemblers and high level language software, availability, cost, technical expertise and documentation, should be investigated. For production items it is essential that the components be second sourced to avoid the position where a single manufacturer may dictate volume price levels.

To this end the 4 bit microprocessors were considered inadequate on grounds of speed, accuracy and hardware support in achieving the numerical process of pulse width calculation. At the very least, it was decided that an 8-bit processor would be necessary. The 16 bit processors were very much more expensive than their 8 bit counterparts, availability, second sourcing and software/hardware support were all quite meagre at the start of the project. Further several individuals had voiced the opinion that the 68000 processor, in particular, was more difficult to operate which probably reflected the lack of information/backup from the manufacturers in the earlier period of their commercial development. It was known that a 16 bit word would be a requirement for numerical calculations, however due to the doubt surrounding the early history of 16 bit devices and the fact that it was known that limited 16 bit operations could be performed by stacking two 8 bit accumulators , a decision was made to consider the 8 bit processors only.

In addition the processors which required programming by the manufacturers were also eliminated from consideration. There remained the choice between the 6800, 6809, 8080 and the Z80 and 6502 systems — these are the more popular and well supported systems whilst others like the RCA, Ferranti and Texas Instruments devices were also available. Many comparisons have been made between differing devices whilst one author devised a piece of hardware into which could be substituted either a 6800 or 8080 and no noticeable operational difference could be observed in its control, given that the system was using a common high level language.

Another author [116] completed a monitor program on 5 different microprocessors and compared the memory requirements for each device - the results are given in Figure 4-7.

This form of memory measurement provides only, at best, a rough estimate of the individual performance of the processors and it was noted that each processor required a different software approach in order to optimise the program so as to take advantage of the unique characteristics of the particular devices being used. Further, for most processors, by taking advantage of the resources available, one can program almost anything in the same number of bytes. However, the issue of word size is a major factor - in the above, the 16 bit 9900 processor uses an estimated 20% fewer bytes, however, the key to a successful implementation is a good, firm specification of the application to be realised.

The previous discussion ignores the computational time of the microprocessor. It is to be noted that this is significantly altered by the clock rate (as well as word size) and several different clock rates can be obtained for each of the microprocessors mentioned. Eventually one is forced to the conclusion, on choice, as achieved by Waterfall [112] and that is

1. Of which microprocessor do you have experience?

2. What hardware and software development tools do you have?

3. Will a microprocessor satisfying (1) and (2) do the job? If yes - choose it. If no choose the most suitable one available and buy or rent support equipment.

In this case the answers to (1) and (2) were the 6800 system and the answer to (3) was yes and so the 6800 system was chosen for realisation of the microprocessor based PWM system. Further the bus system structure of microprocessor systems is standard whilst the hardware design philosophies divide between the low cost single board structure and the functional division of boards with a standardised bus wiring structure. The latter system was chosen in the adoption of an MSI 6800 system for hosting software and hardware development for the implementation of the numerical approach to the generation of the PWM waveforms.

4.6 The 6800 System

The 6800 is considered by many to be a more effective design with a more complete and less complex instruction set[117].Generally the 6800 needs fewer clock cycles than the Intel 8080, to execute a similar instruction. Design limitations were placed on the 8080 to remain compatible with the earlier 8008. No such constraint was placed on the M6800. However, in comparison to the 6800, the extra registers of the 8080 and the ability to handle multiple-precision (16 bit) values is an advantage, whilst the availability of only one accumulator is a limitation.

An advantage in adopting the 6800 is that it does not need unique I/O instructions. One of the major features of the 6800 family is the use of unrestricted memory - mapped, dynamically programmable I/O. Many of the features present in the 6800 system are based on those, as exhibited by the PDP 11 minicomputer whereas the 8008 was based on the earlier architecture of the PDP8. In addition, the 6800 system

PROCESSOR	MONITOR SIZE (BYTES)
INTEL 8080	979
MOTOROLA 6800	990
FAIRCHILD F8	1007
RCA COSMAC	1400
TI 9900	800

FIG 4-7
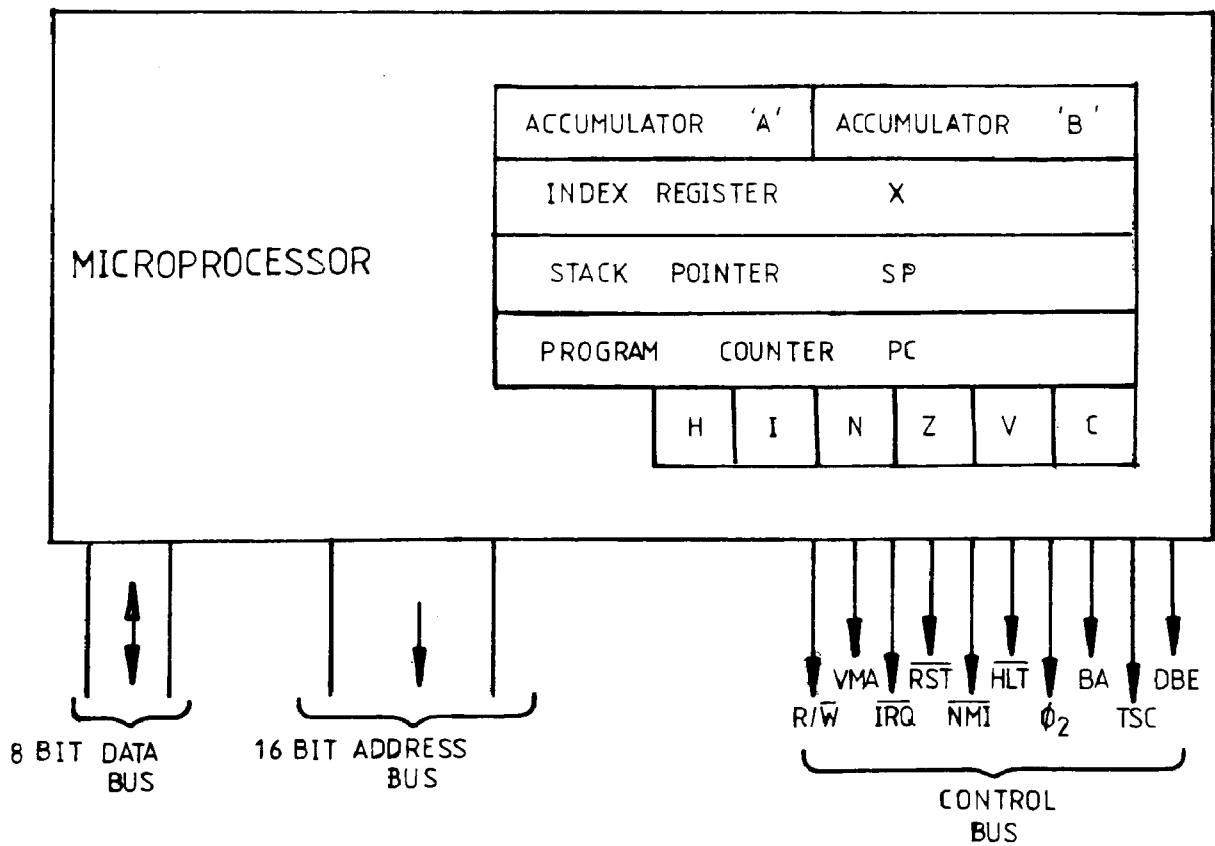
FIG 4-8

utilizes a 5 volt supply and the bus voltage levels are compatible with TTL. The 6800 system also has a direct addressing mode which requires less memory utilisation than other approaches.

The 6800 microprocessor is also upward source code compatible with the 6801 and software compatible with the 6809 system at the assembly language level.

All the components of the 6800 family are fabricated using MOS technology and the speeds remain low at 1.0MH, 1.5MHz or 2MHz. The comparative ease with which the 6800 can be programmed reflects the foresight, on behalf of the manufacturers, in assuming that the major cost of microprocessor systems would be incurred in their programming i.e. the software cost.

4.7   Bus System

All microprocessor systems utilize a bus structure. They can exist at several levels

1.   Internal - both microprocessor units and programmable peripheral chips have an internal bus. It enables inter-register transfers.

2.   Inter - unit - this is the main bus shown in Figure 4-8.

3.   Inter computer - multi-microprocessor systems involving co-operating and concurrent processes can have an additional bus to allow inter-computer transfers and shared data in a common area of store.

Within the system - bus are three groupings.

4.7.1 The Data Bus

In a typical system an 8 bit byte is transferred in parallel - that is there are 8 wires, one for each bit. Words of two or more bytes need to be transferred in byte serial form. The data bus is bi-directional and transfers information to and from all units in the microprocessor system.

4.7.2 The Control Bus

The meaning and purpose of signals on the data bus is determined by the control signals of the control bus. Other signals such as timing, validating and strobing signals, and which do not form part of the data or address bus, are usually combined under the title of the control-bus. Data transfers between peripheral chips, and their synchronisation, are regulated by the voltage levels on the control lines.

4.7.3 The Address Bus

For the 8 bit microprocessors the address bus has 16 lines allowing an address field of approximately 64K locations. The lines are in a particular order, the binary weighting of each line and the overall code being used to select chips or memory areas for the purpose of data transfer.

The use of the various control signals in combination with the addressing facilities and data bus is the end objective in the design of microprocessor systems.

4.8   Programmable Peripherals and the Interface Hardware Choice

The choice of the MSI 6800 system included the provision of the hardware and software interface for a keyboard, with visual display unit, and a tape recorder for loading and storing programs.Thus the requirement for a hardware/software interface to control the motor, via the inverter, was given due consideration.

The family of programmable peripherals for the 6800 system were studied and the techniques of producing three phase PWM waveforms given due attention. The use of software timing loops to produce the timing intervals necessary for realising PWM waveforms was considered unwieldly. Several loops would be required, with interrupts to update each phase so that each timing period would be unduly extended, since, whilst one phase was being updated the other phase would be unattended. In addition the provision of a feedback control system would have necessitated the use of a second microprocessor.

Thus a decision was taken to use some form of programmable hardware timer which could be used to produce the series of variable width pulses. If the timers were operated independently of each other, to produce the three phase output, the microprocessor could then be used to perform any control function required. In this way the limitations of the basic serial nature of the microprocessor is avoided by introducing hardware functions which can operate in

parallel. Both analogue and digital techniques of producing programmed pulse widths were compared and it became clear that the MC6840 [118] contained all the required functions in a single package. The device contained three independent timers, registers and control signals which greatly simplified the task of hardware design. Many extra chips and inter - unit wiring would have been necessary in alternative systems. The MC6840 was a truly programmable device designed especially for the MC6800 system and, in practice, proved to be ideally suited to the task involved. With hindsight, the only criticism which could be levelled at the functions provided were

1. The complexity and extent of knowledge required to operate the device.

2. The fact that the initial polarity of the pulse outputs could not be programmed to be either 1 or 0. the initial output was always high and necessitated the addition of an 'exclusive or' chip.

4.9   System Design - Hardware/Software Tradeoffs

The choice of the MC6840 was a relatively obvious decision as the alternatives proved significantly more complex. Other choices are not so obvious. There was a need for the provision of mathematical functions such as divide, multiply and sine. Calculator chips are readily available for these purposes. However, the speed of the sine calculation could be measured in seconds whilst that for the divide and multiply could be measured in microseconds. It was also noted that the high accuracy of all functions performed by the calculator,

was not needed in the numerical calculation of the pulse width. Although it was believed that 8 bits would be adequate it became clear that 16 bits would provide a necessary improvement in the accuracy of calculations. An 8 bit word provides about 2 decimal digits of accuracy which implies that sin 83.3 and sin 90 could not be distinguished whilst a 16 bit data word would provide about $4\frac{1}{2}$ decimal digits of accuracy.

Further it was found that the software routines for divide and multiply were about 100 times slower whilst the sine routine was 100 times faster (due to limited accuracy) than the hardware counterparts. This was considered quite acceptable in the circumstances as the hardware and software was so structured that the calculation of new input data was completed in parallel with the operation of controlling the motor. Thus the motor could still run whilst new data was being entered into the system. In addition the level of complexity of both multiply, divide and sine software algorithms was low enough to be able to assess that the routines could be designed within a reasonable period of time (2-4 weeks). The remaining ancillary routines were determined by the configuration in that basically the software option was the only practical technique of operating on the data. The one exception to this is probably the three phase routine.

It is perhaps less obvious that a simple hardware alternative exists for the three phase generation of PWM waveforms from a single phase input. Certainly it was not obvious that a fairly complicated software routine would be necessary. In practice, in order to realise the 120° phase shifts in the waveform, two separate software modules were required and this remains an area which could benefit from

further study.

Finally, it should be noted that the designer of a microprocessor system must remember that his system should perhaps have a general purpose basis to the hardware so that the system can support several different applications which may be envisaged by other designers in the department - which would reduce the need for the repetition of effort in the achievement of an overall solution to the design problems proposed.

CHAPTER 5   THE MICROPROCESSOR CIRCUIT SYSTEM DESIGN

5.1   Digital Implementation of P.W.M. Control Strategies

Because of the recent availability of large scale integrated (L.S.I.) circuits, considerable effort has been devoted to the development of digital p.w.m. control systems for power inverters, in order to eliminate the problems of drift and setting-up procedure associated with analogue control techniques. However, so far as the investigation described in this paper is concerned, it was also thought that these advantages should not be realised at the cost of deterioration in the harmonic spectra of the output p.w.m. voltage waveform, or loss of adaptability and flexibility of the power inverter. Therefore, it was decided to investigate the feasibility of implementing the preferred regular sampled asymmetrical p.w.m. process by means of a microprocessor, where the switching points of the three-phase width-modulated pulses were determined by the stored program in conjunction with the input data.

5.2   Microprocessor Control

It may be seen from the block diagram in Figure (5-1), that at present the system under investigation operates in an open loop mode of control. It may also be observed that the only difference between the proposed system and prior-art analogue p.w.m. controlled inverters, is that the three p.w.m. control signals are generated by means of a 6800 microprocessor, rather than by analogue circuit techniques.
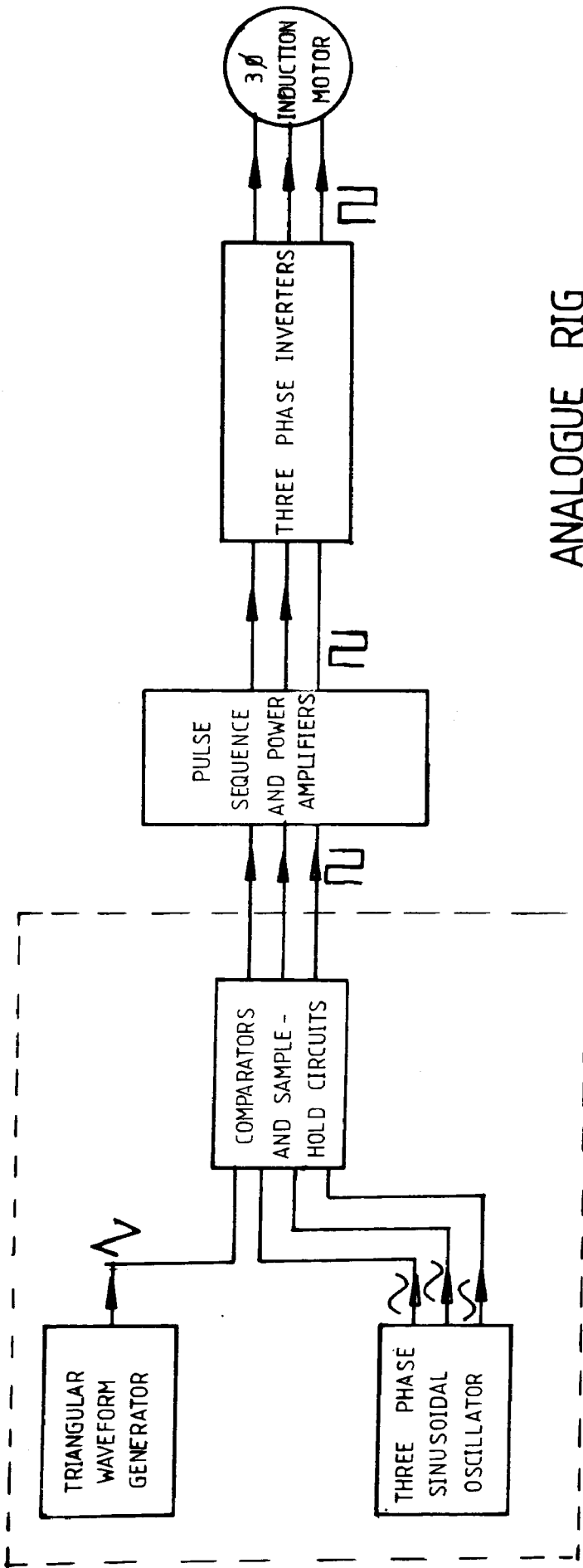
ANALOGUE RIG
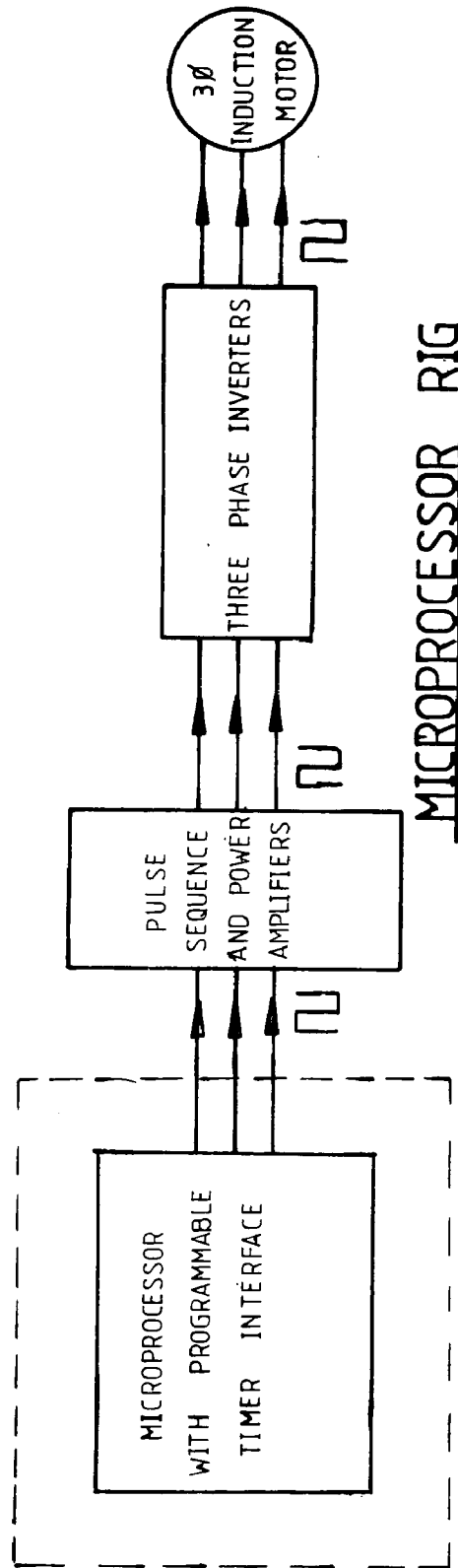
MICROPROCESSOR RIG

FIG 5-1

- 159 -

The decision to use the microprocessor for calculation of the switching points of the width-modulated pulses, rather than use read-only-memory (ROM), digital comparators and a clock was based on the following reasons :

1. The permanent storage of the program in ROM for a chosen range of frequency and voltage magnitude, imposes limitations on the adaptability of the inverter, and the flexibility of its control.

2. The non-iterative algebraic solution for the regular sampled p.w.m. process can be economically implemented in software without the need for large programs and long term calculations as would be required by the natural sampled p.w.m. process.

5.3   A Microprocessor Solution

In order to maintain flexibility in the design of the program for p.w.m. generation a decision was taken to adopt a numerical technique for the realisation of three-phase p.w.m., rather than to directly simulate the hardware design using up-down counters, sine tables and repeated "compare" instructions.

The pulse width of the perodic p.w.m. waveforms are calculated according to the formula $T_n = Tc/2(1+(-1)^{n-1}K/2(\sin\theta_n + \sin(\theta_{n-1}))$, where $\theta n = \pi n/R$, stored in a memory table and a routine for transferring the pulse width data to the Programmable Timer Module (PTM) is initiated.

Sub-routines were developed for division, multiplication, code conversion, scaling and for sinusoidal calculations. The principles of structured programming, functional division and modularity were incorporated into the program design, Figure 5-2. An MSI 6800 computer unit was utilized as the host microprocessor system and an input-output interface unit was designed for the application. A paper describing the early work has been published and a diagram of the functional software sequence is given in Figure 5-3.

The PTM generates the p.w.m. output wave by counting down the pulse width data stored in its programmable registers. As one pulse is timed out an interrupt is generated which then calls the next pulse. Background routines can be performed by the software in parallel with the hardware timing function thus allowing the entry of new data and system performance monitoring.

5.4   The Hardware/Software System Interface of The Programmable Timer

A complete specification of the signals and operating characteristics of the MC6840 timer is given in the Motorola manual. The MC6840 is a programmable, bus compatible subsystem component of the MC6800 family, designed to provide variable system time intervals.

The MC6840 has three independent, 16 bit binary counters, three corresponding 'write only' control registers and a 'read only' status register. The counters are under software control and may be used to cause system interrupt, and/or generate specialised pulse signal waveforms. The timer can be programmed to operate in one of several different modes, each of which can be accomplished by setting
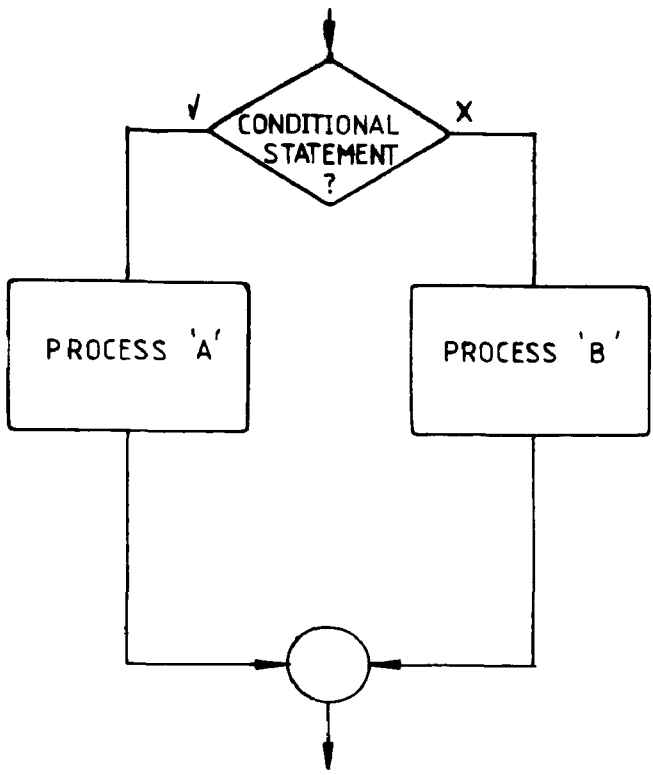
FIG 5-2(a)
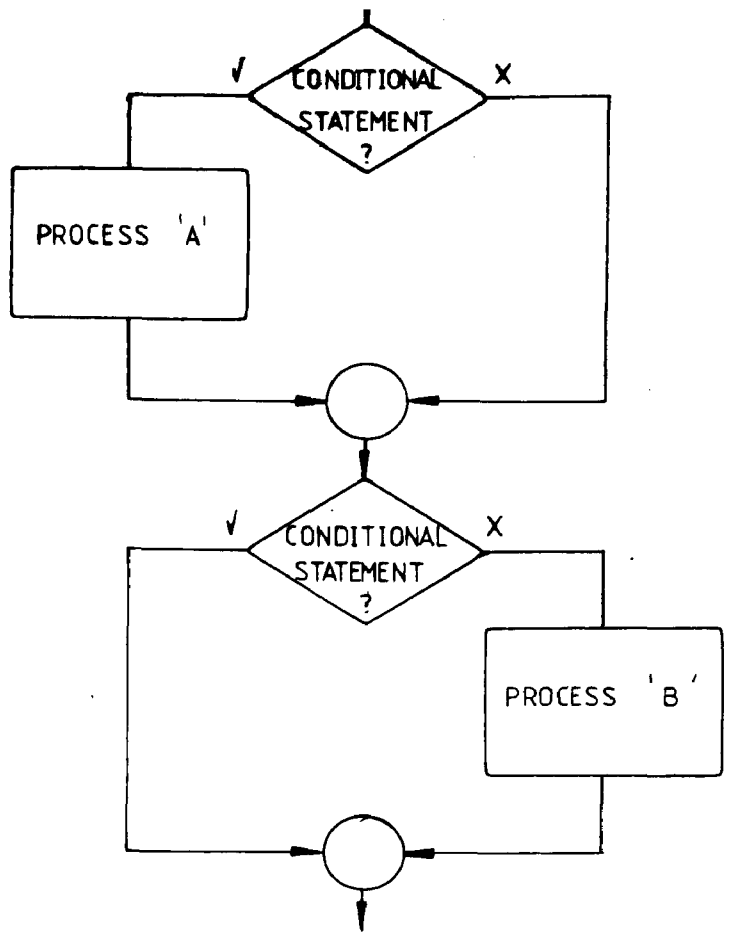
FIG 5-2(b)
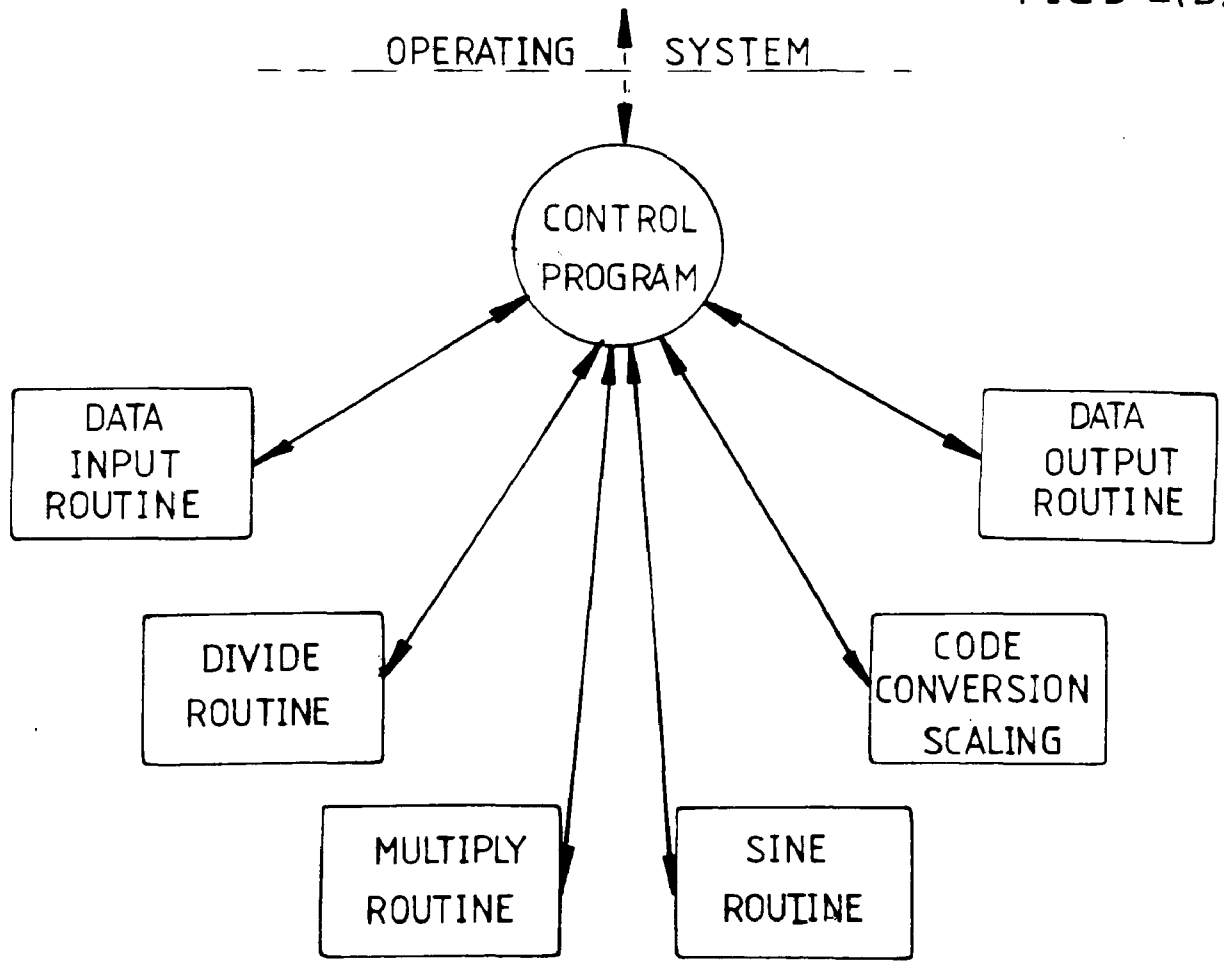
FIG 5-2(c)
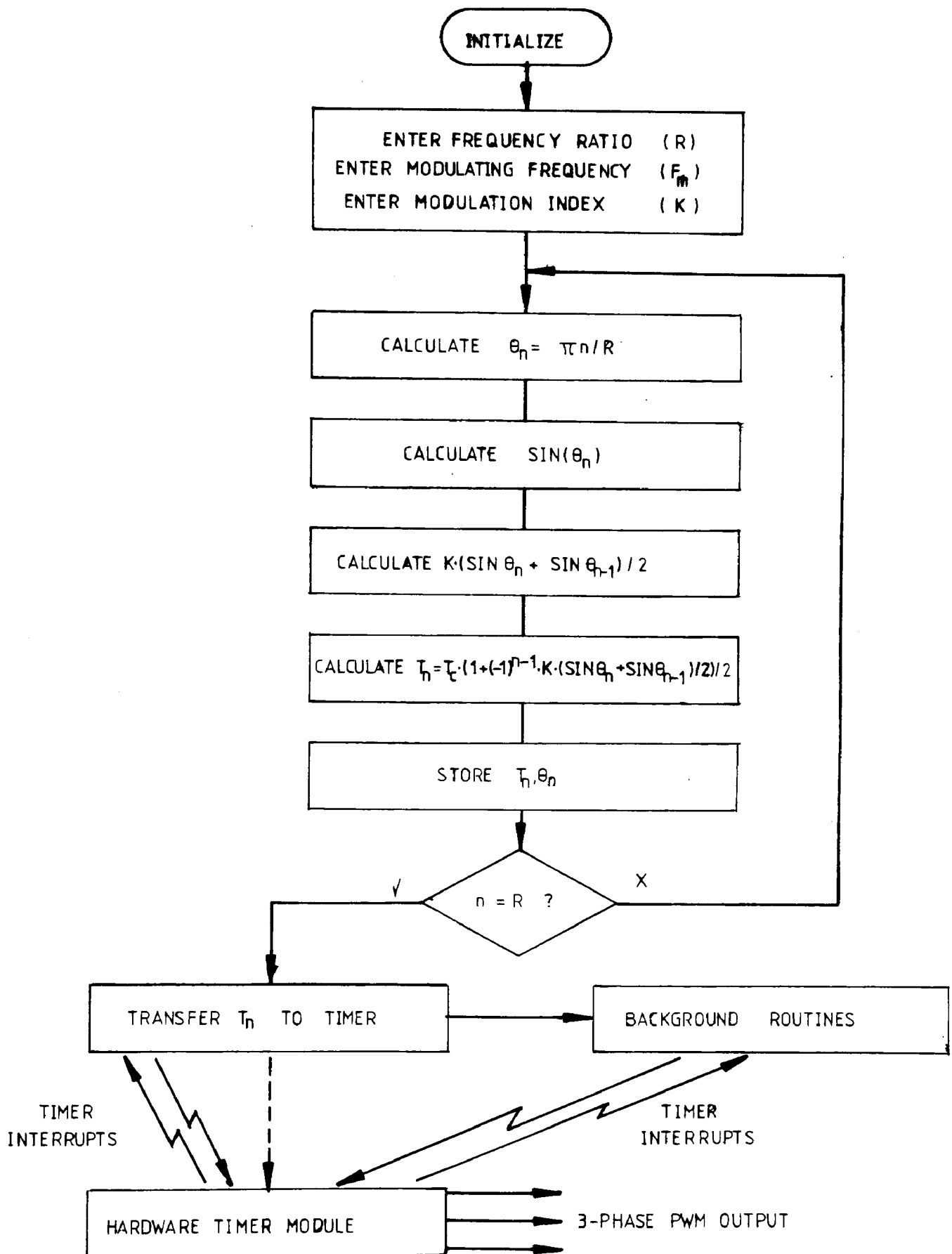
FIG 5-3

individual bits in the control register which can select :-

1. the continuous operating mode

2. the single shot timer mode

3. the time interval mode

4. the frequency comparison mode

5. the pulse width comparison mode.

The PTM is accessed by load and store operations, from the MPU, in much the same manner as a memory device and a counter is loaded by first storing two bytes of data into the appropriate counter latch. On the counter initialization cycle the data is immediately transferred to the counter which then decrements on each subsequent clock period. When the count reaches zero (or some other predetermined condition) the count halts, a new count is loaded (or the count recycles) and the interrupt line can be set depending on the timer mode selected.

5.4.1 Operation of timer

The system diagram for the programmable timer is shown in Figure 5-4. The software is used to control the timer in the followng manner. Initially the gates G1, G2, G3 are held positive and the address lines from the microprocessor to the timer register select unit, in parallel with the enable line (system ϕ_2), are actuated to provide a parallel pulse sequence giving an address code of A000 -

A007. In this way, individual registers such as the control registers, latches or counters are selected. Initially the control registers are selected. Digital information is then placed on the data bus and the R/W control line becomes '0'. At this point the data is then entered into the appropriate control register. The control registers, once programmed in this way, have now configured the timer to function in a precisely specified manner. That is, when a binary number is transmitted to the latches it is interpreted as either a 16 bit binary number or two separate 8 bit binary numbers, further, on counting this number down, the timer will initiate those control signals as determined by the binary code in the control registers.

The timer will only start counting down when the signals to the gates G1, G2 and G3 go low and will only continue counting if the gates remain low. The Reset line, when low, immediately stops the timer from operating and resets all the registers including the control registers. That is, the control registers have to be reprogrammed before further operation of the timer, in the selected mode, is possible.

Output signals are obtainable from 01 02 and 03 only if the timer has been configured to provide these outputs. Also, the polarity is always '0' at the start of any count. Programmable exclusive-or gates need to be provided if the designer requires the choice of a '0' or '1' output from 01, 02 and 03 at the start of the count.

Similarly IRQ will only operate, at the end of a count, if programmed to do so.
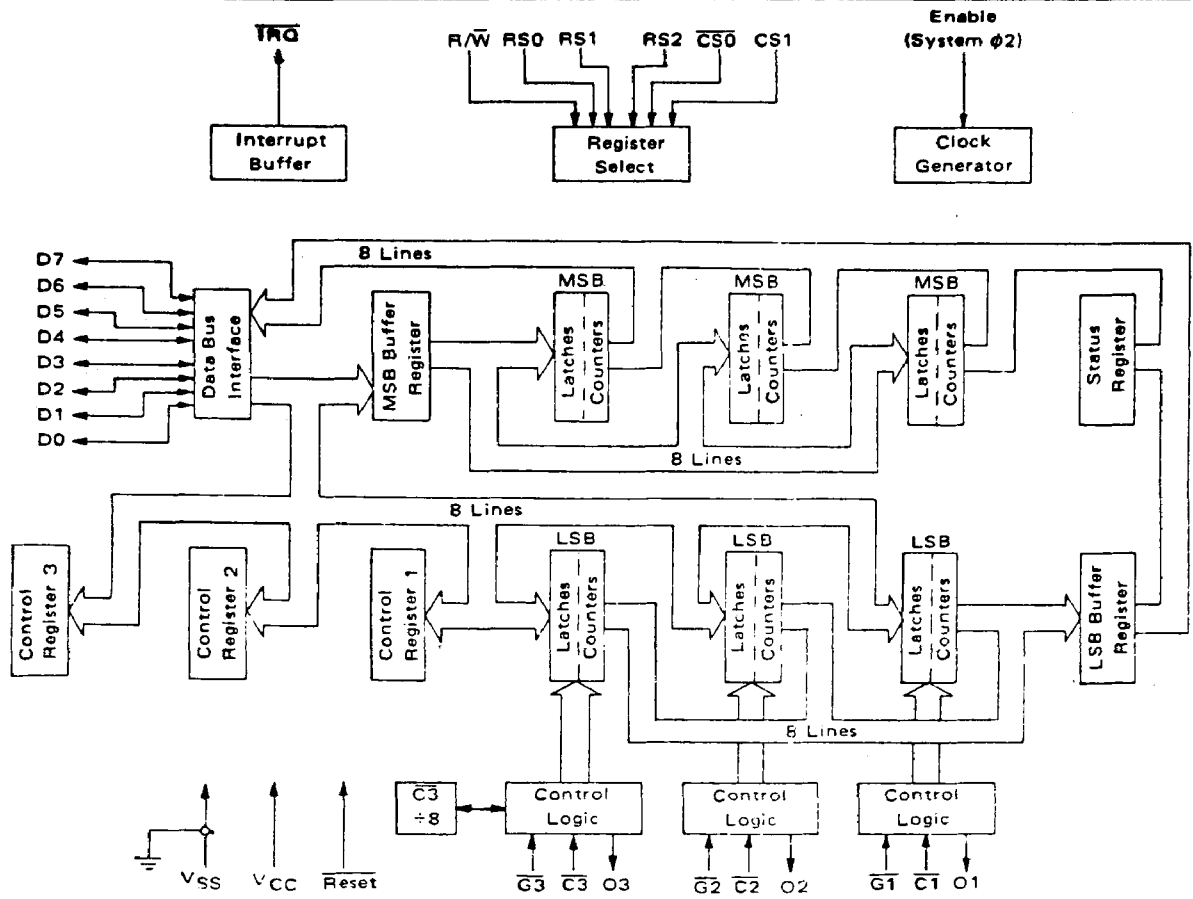
FIG 5-4

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
1	1	0	0	0	0	0	0

FIG 5-5

5.4.2 Timer Mode Selection

The PTM was configured by storing an eight bit control word in each of the three control registers, one for each of the three timers.

The control word is as shown in Figure 5-5.

This control word selects the continuous operating mode; it allows all timers to operate; it selects a 'divide by one' over a 'divide by eight' option; the normal 16 bit count mode is chosen; the interrupt flag is enabled and the Timer Output is also enabled.

5.4.3 The Continuous Operating Mode

The selection of the continuous operating mode, in combination with the normal 16 bit count mode, allows the timer to be used as follows :

1. The counter is enabled by a logic zero at the gate input provided, a Timer Reset condition does not exist.

2. When the counter time out occurs (that is the first clock after all counter bits reach zero) the Individual Interrupt Flag is set and the counter is re-initialized with data from the buffer latches associated with each individual counter.

3. The Individual Interrupt Flag contained in the Status Register (associated with that particular timer) remains set until a 'Write Timer Latches' command is recieved, for that timer. The 'Write Timer Latches' command also updates the information held in the latches so that the new data will be transferred to the timer as

it counts, the previous data (held in the counter register) down to zero.

5.4.4 Operation of Counters

For a given set of input data, the software system of the microprocessor calculates the individual pulse widths of the three phase output signals for a whole period of the PWM signal, according to a pre-determined formula. Now, these pulse widths, which define both the positive and negative pulse lengths over the period, are stored in a tabular form in the memory of the microprocessor. The pulse lengths are stored consecutively, in the table, in the same way as they would appear in the PWM signal.

If a single phase is considered then the system operates as follows :

1. The first timing pulse is stored in the counter.

2. The next timing pulse is stored in the latches related to that counter.

3. The gate signal is reduced to zero and the timer is activated.

4. The counter is now decremented by the clock input (which in this case, has a period of approximately 10µS).

5. The binary number of the counter goes on counting down until the number reaches zero.

6. The output polarity of the signal from the timer reverses at this point.

7. At zero, the interrupt Flag is also set, and the 'next pulse' data is automatically transferred from the latches to the counter register and the timer continues to count down the next pulse.

8. An interrupt routine is initiated by the interrupt Flag. This routine searches the software table containing the magnitudes of the PWM pulses, and obtains the value of the next pulse which the timer will require to count down at the next interrupt, this value is then stored in the timer latches associated with the appropriate counter. This process is repeated and, in this way, the PWM waveform is made up of a sequence of 'on-off' pulses whose widths are defined by the memory table of values.

5.5   The PTM Interface Unit Hardware

In reference to Figure 5-6the micropocessor bus provides the data, address and control signals shown on the left hand side of the diagram. The inverted data bus is re-inverted by the tri-state gates which are also controlled by the R/W signal so that data can be transferred to and from the appropriate memory areas in the PTM.

The Sixteen bit address lines are connected to a decoding network which sets the address space for the PTM counter registers, latches and control registers to A000 - A014.
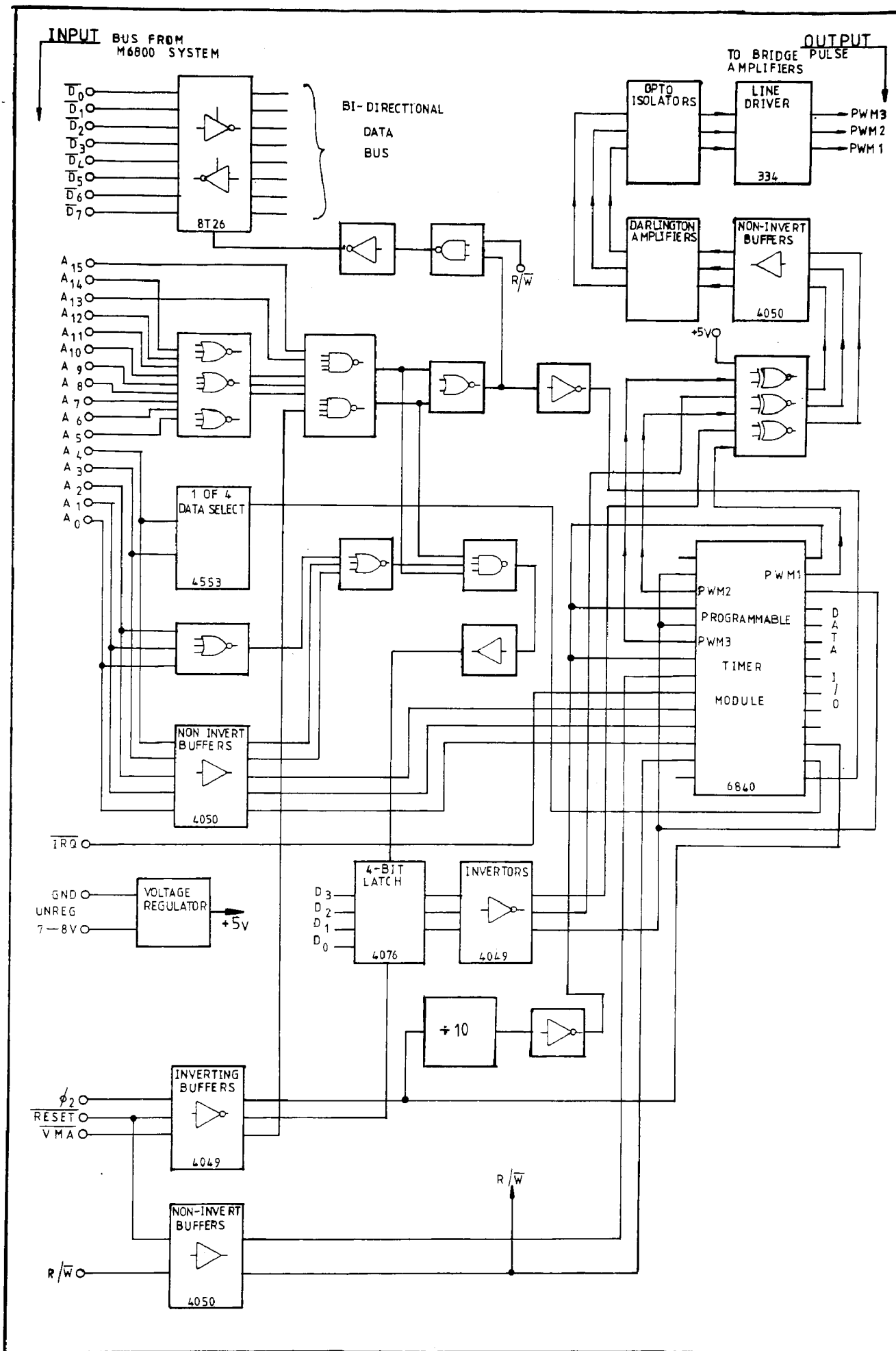
FIG 5-6(a)
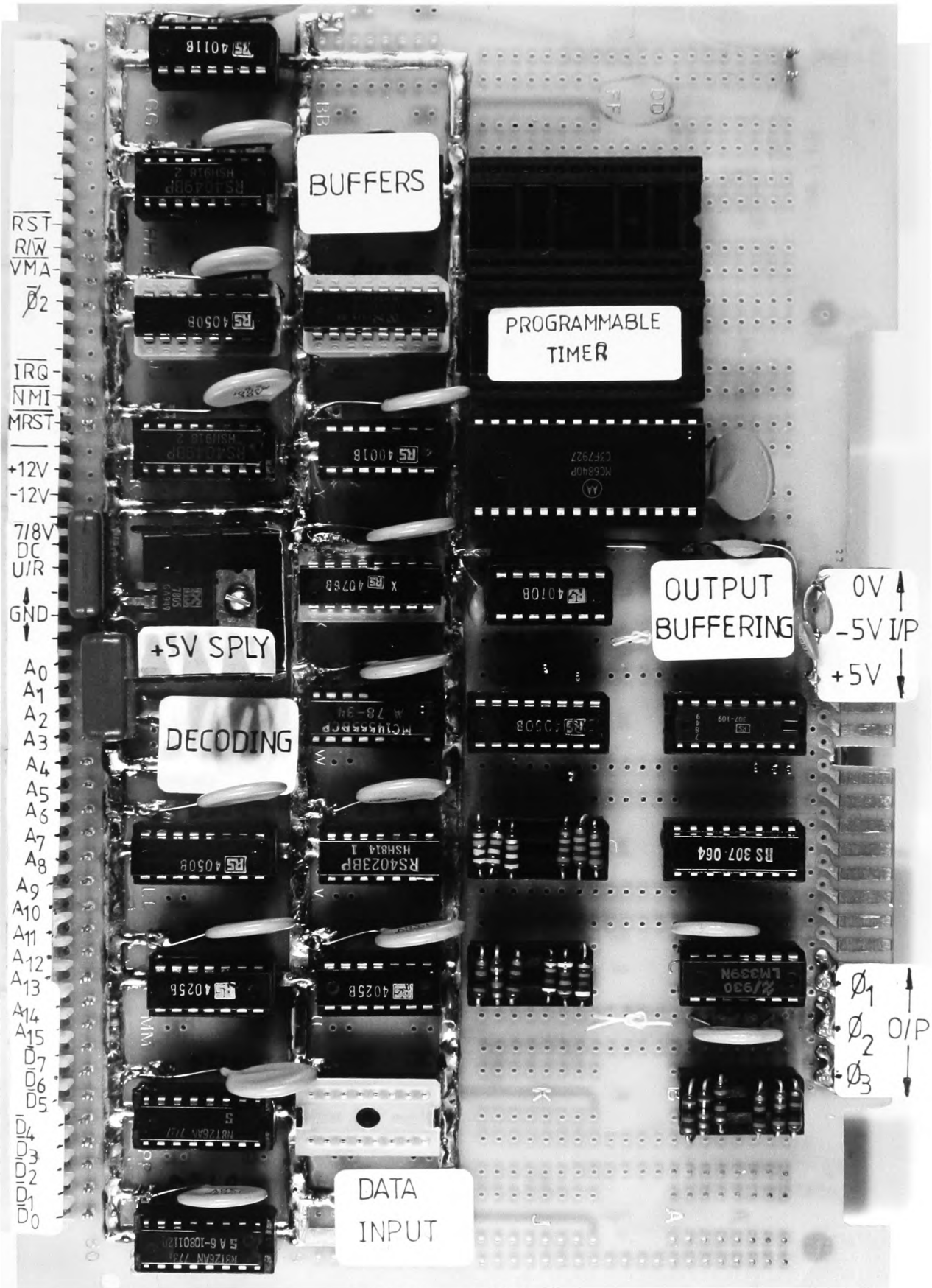
FIG 5-6(b)

An address is also provided for the logic network which inputs data to the EX-OR gates so that the initial polarity of the output pulses may be set for the three separate phases. This polarity setting is determined by the initialising routine of the software. Once set it remains in this state until the data for a new PWM waveform is entered into the system.

A divide by ten integrated circuit, uses the crystal clock of the microprocessor to provide a convenient timing signal for the counters. The inverting and non-inverting buffers serve to provide a minimal load on the microcomputer bus lines and to provide a low impedance source and appropriate polarity for the control signals.

5.6   The Microprocessor Software

The software was designed to implement the equation

$$T_n = T_c/2(1+(-1)^{n-1} \cdot K/2(\sin \theta_n + \sin \theta_{n-1})), \text{ for } n = 1 \text{ to } 2R$$

which can be used to define the PWM waveform in the time domain, by a sequence of pulses of differing lengths. As can be seen from the formulae the following routines were required :

1.   A data input routine

2.   A Binary Coded Decimal to binary routine

3.   A divide routine

4. A multiply routine

5. An add/subtract routine

6. Formatting or scaling of data

7. Sine routine

8. Primary 3 phase sort routine

9. Secondary 3 phase sort routine

10. Output routine

11. Control program

12. Interrupt routine.

Another routine was required for the initialisation of the timer. Initialisation of other registers is contained within the routines so that a new set of input data requirements are not corrupted by previously calculated data.

5.6.1   The Timer Initialisation Routine (0F00 - 0F14;   20 bytes)

This is a short routine intended to set the status or configuration of the timers so that they can be operated in the 'continuous mode' as required by the application software.

5.6.2   Input Data for 'Input Routine' (0100-0169;105 bytes)

This memory area contains ASCII coded data which is used by the
Input Routine to display alphanumeric information on the VDU terminal.
The ASCII code table is shown in Figure 5-7.

5.6.3   Input Routine (0200-0242);66 bytes)

The flow chart for this routine is shown in Figure 5-8.   Data,
contained in the previous routine is outputted to the VDU and appears
as a sentence requesting input data. A keyboard scan routine is then
initiated so that data may be inputted to the microprocessor system.
Three separate data inputs are obtained in this manner.

5.6.4   BCD To Binary Conversion (0300-0354; 84 bytes).

The input data is in binary coded decimal. That is, an 8 bit
byte is used to store each of the decimal numbers inputted. For
future calculation purposes the binary coded decimal equivalent is
required to be in a pure binary format. The first binary coded number
would need no change - the second needs to be multipied by 10 and then
added to the first to get the equivalent binary number. If there is a
third BCD number then it would need to be multiplied by 100 and added
to the sum of the previous two numbers. In this way a binary number
is obtained which is equivalent, in value, to that of the decimal
number. The flowchart of the operation is given in Figure 5-9.

American Standard Code for Information Interchange (ASCII) to Hexadecimal

Note: ASCII represents characters as a seven bit binary code which can be represented as two hexadecimal characters as follows:-

Most sig. digit:	0	1	2	3	4	5	6	7
Least sig.								
0	NUL	DLE	SP	0	@	P		p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	£ ( )	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K		k	
C	FF	FS	,		L		l	
D	CR	GS		=	M		m	
E	SO	RS	.		N		n	
F	SI	US	/	?	O		o	DEL

It should be noted that characters such as 'DC1' etc. are 'non-printing' but are often used to initiate various control functions in the teletype equipment for which this ASCII code was originally designed. When transmitted the codes are usually prefixed by a 'start' bit and terminated by 'stop' and 'parity' bits thus making a total of at least ten bits representing each character (serial transmission). Mechanical teletypes operating at ten characters per sec (e.g. ASR 33 type equipment) use ASCII codes with two stop bits instead of the usual one to ease syncrhonising problems. Thus they have eleven bits to represent each character and operate at a bit rate of $10 \times 11 = 110_{10}$ bits/sec. or 110 baud. Faster mechanical teleprinters (e.g. Digital Equipment Corporation LA 36 type machines) operate at 300 baud (30 characters/sec.).

Use of the table: K = 4B, 7 = 37, j = 6A etc.

FIG 5-7
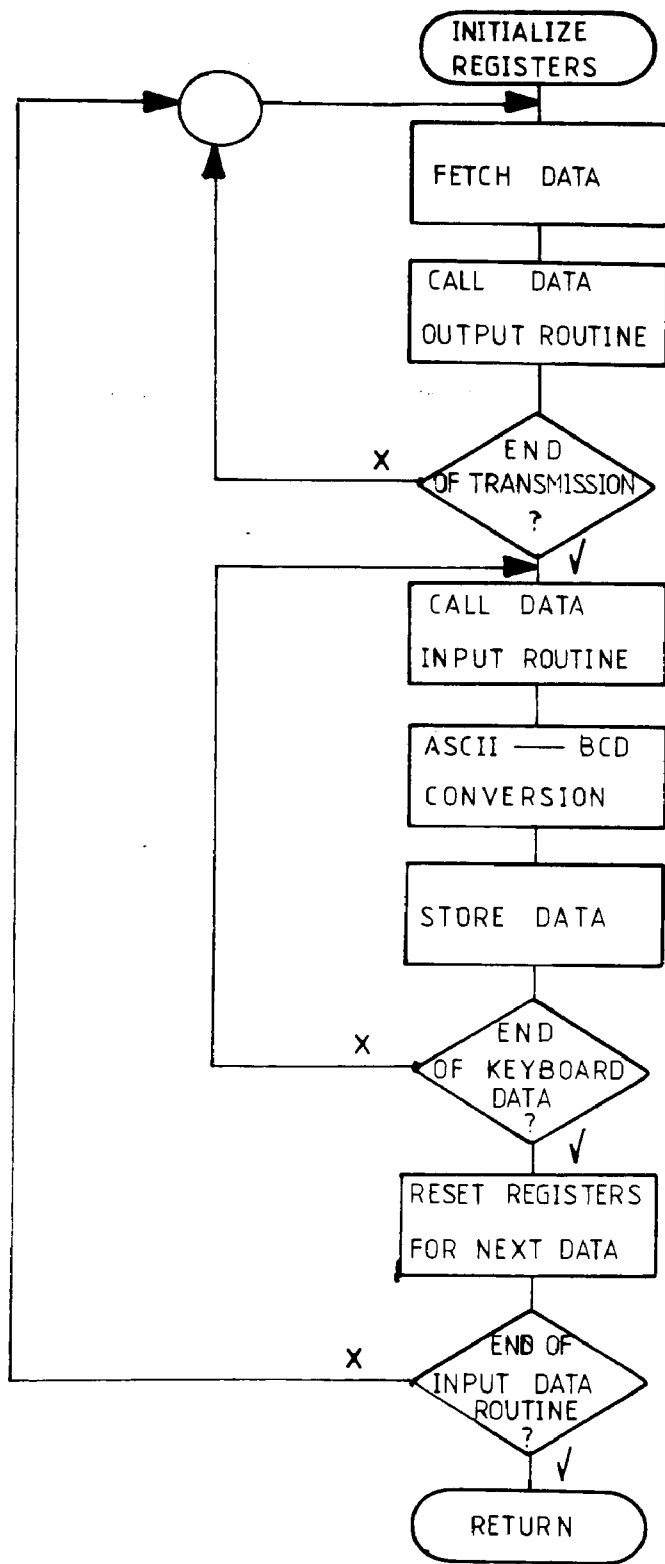
FIG 5-8   INPUT   ROUTINE
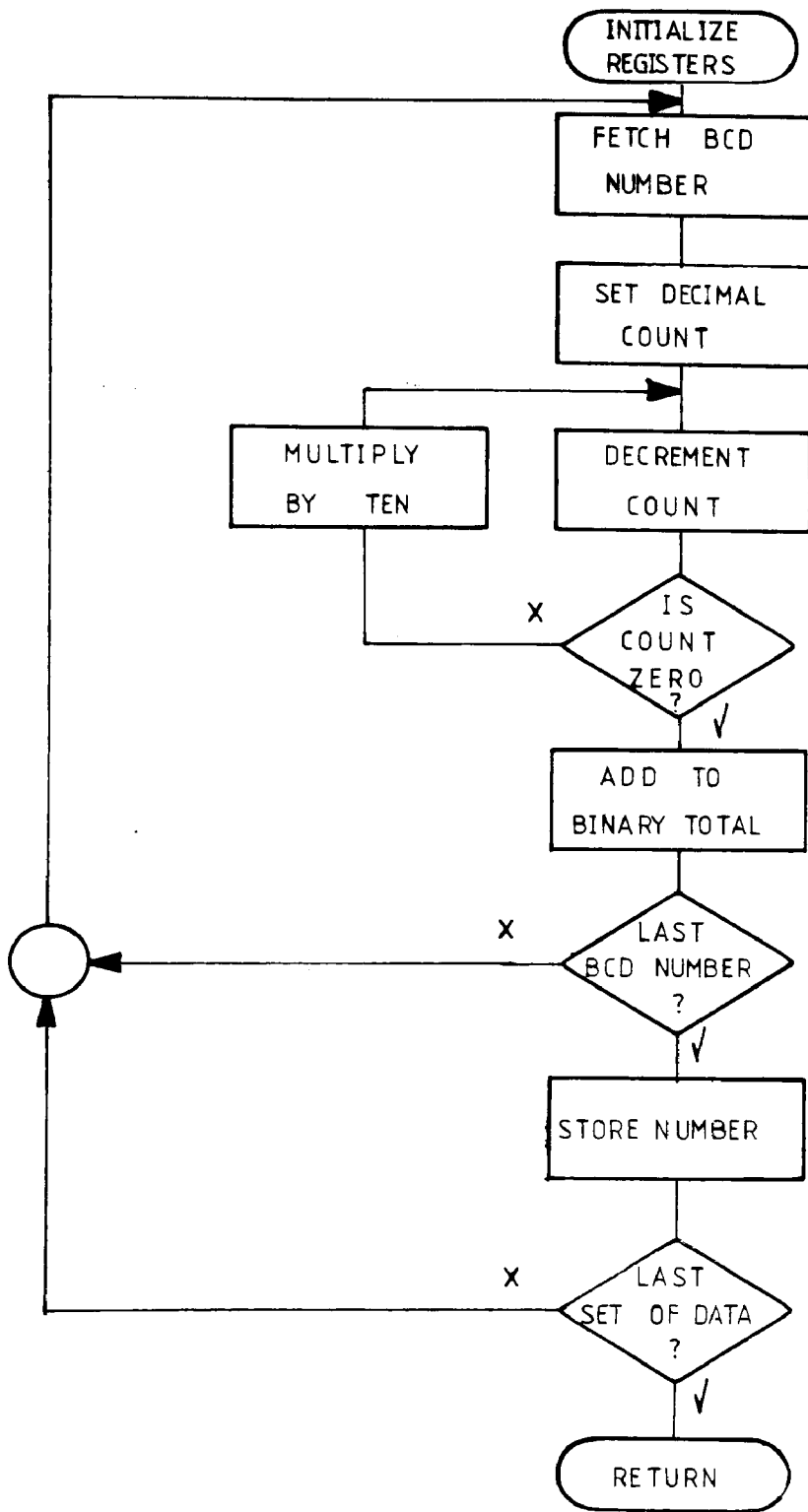
FIG 5-9   BCD TO BINARY

b.6.5   The Multiply Routine (0400-0454;   84 bytes).

The unsigned integer multiply routine Figure 5-10 can accommodate two sixteen bit numbers, multiplying them together, to give a 32 bit result. The routine first determines which quantity, of the two inputs, is the highest;   it then sums this, with itself, the specified number of times (as determined by the value of the lower multiplier). The final result is then the product of the two numbers. The general algorithm for the multiplication of the binary numbers is illustrated by the following example :-

11101	Multiplicand
1101	Multiplier
11101 (A)	The product of 1 and 11101
11101 (B)	Shift multiplicand left 1 bit
	Do not add since multiplier bit = '0'
11101 (C)	Shift multipler left 1 bit
10010001 (C)+(A)	Add product (C) to (A) since multiplier
	bit = 1
11101 (D)	Shift multiplicand left 1 bit

101111001(A)+(C)+(D) Add product (D) to (A) and (C) giving the

final answer.
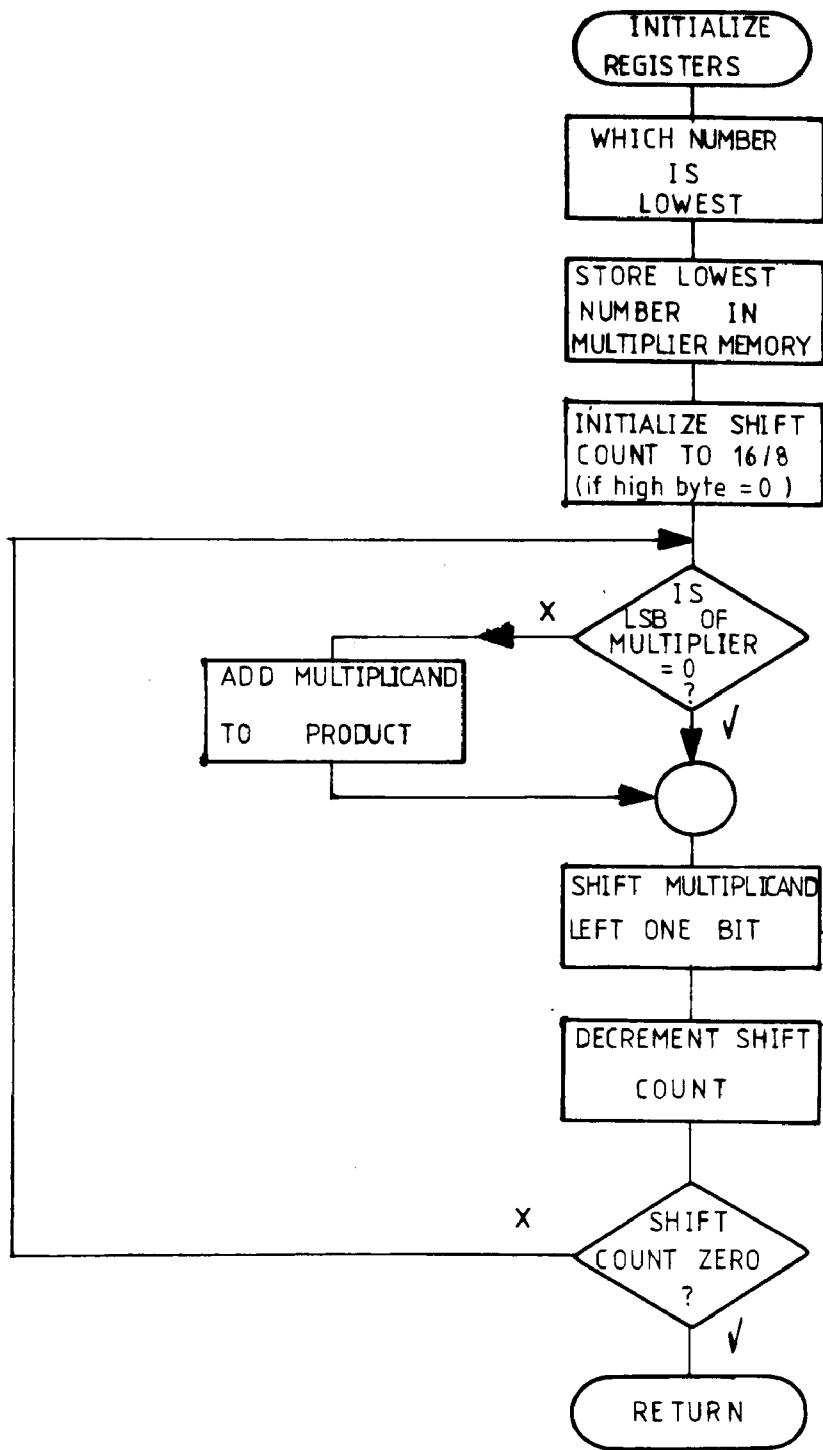
FIG 5-10   MULTIPLY   ROUTINE

5.6.6 Divide Routine (0500-0559; 89 bytes).

This routine Figure 5-11 is designed to divide an unsigned 24 bit binary number by an unsigned 16 bit binary number, the result being stored as a 16 bit binary number. Again the algorithm is best illustrated by the following example.

```
            011
         ┌─────────
  1101   │ 100111
         │ 1101          LEFT JUSTIFY DIVISOR
         │
                         DIVISOR GREATER THAN DIVIDEND

                         PLACE 'O' IN QUOTIENT

        10011(A)         AND SHIFT DIVIDEND LEFT 1 BIT

         1101(B)         (OR SHIFT DIVISOR RIGHT 1 BIT)

         0110            SUBTRACT (B) FROM (A) SINCE B>A

                         SHIFT QUOTIENT LEFT 1 BIT PLACE 1 IN QUOTIENT

         1101(C)         SHIFT DIVIDEND LEFT 1 BIT (OR

         1101(D)         SHIFT DIVISOR RIGHT 1 BIT)
         ───────

         0000            SUBTRACT (D) FROM (C) AND
         ────

                         SHIFT QUOTIENT LEFT 1 BIT AND

                         PLACE 1 IN QUOTIENT.
```

Add Subtract Routine (0600-062D; 45 bytes).

This routine simply adds or subtracts two 24 bit numbers. The function of the routine is set by a codeword stored in a 'flag' register. If it is odd then the routine adds the two numbers. If it is even the routine subtracts the two numbers.
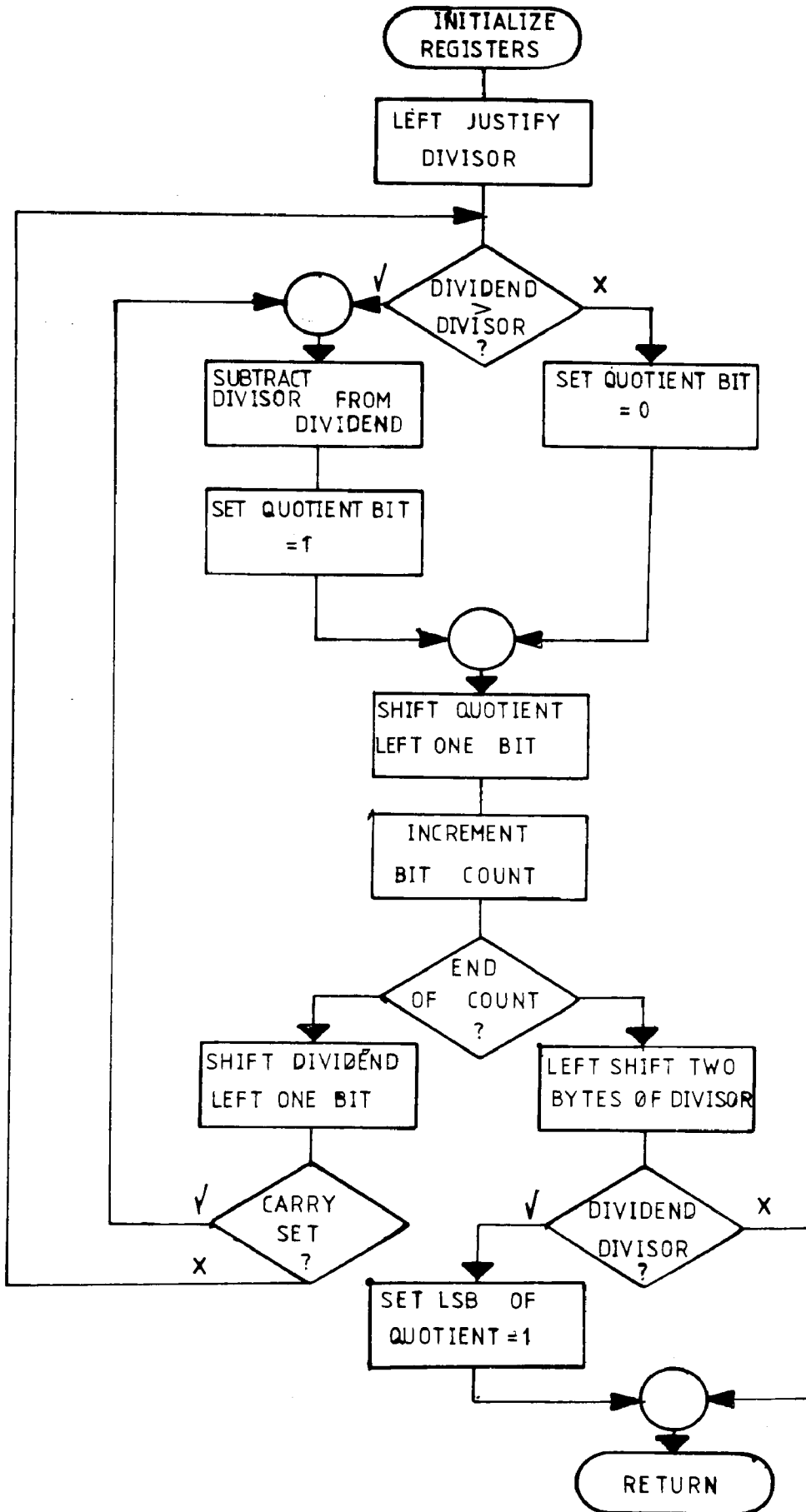
FIG 5-11 DIVIDE ROUTINE

5.6.7   16 BIT FORMATTING PROGRAM (0700-07C7;   199 bytes)

The binary numbers in the routine can reach lengths of 24 bits and this program, Figure 5-12 was introduced to rationalise numbers to a 16 bit format so that future data handling routines did not become unwieldly.   Further, the necessary accuracy was satisfied with 16 bit binary numbers. 8 bits provide only a 2 decimal digit accuracy preventing the program from differentiating between sin 83.3 and sin 90 whilst 16 bits provided a $4\frac{1}{2}$ decimal digit accuracy. Some degree of scaling is also necessary to prepare data for use in the following sine routine.

5.6.8   The CORDIC Algorithm Sine Routine (0800-08AF;   175 bytes)

For the present purposes the aim is to obtain $sin\theta$, of a given $angle\theta$.   Several techniques are available, including look-up tables, Taylor Series etc., (there are also H/W alternatives).   Here, an original, simple, technique [119, 120] using co-ordinate geometry, is adopted.

It has the significant advantage that the arithmetic requires only division by 2's, addition and/or subtraction. The required software then becomes far less complex than other approaches.   The technique is still relatively slow as compared to hardware alternatives, at least for multiplication, but not for SIN and COS, and takes about 8mS. to provide a result, thus limiting its appliction to 'offline' algorithms.

```
┌─────────────────┐                    ⬭
│ FETCH DATA FROM │                    │
│ DIVIDE REGISTERS│                    ▼
└────────┬────────┘           ┌─────────────────┐
         │                    │ STORE R2  IN    │
         ▼                    │ MULTIPLY        │
┌─────────────────┐           │ ROUTINE         │
│ STORE IN DIVIDE │           └────────┬────────┘
│ ROUTINE  AS     │                    │
│ DIVIDEND        │                    ▼
└────────┬────────┘           ┌─────────────────┐
         │                    │ MULTIPLY BY     │
         ▼                    │     654         │
┌─────────────────┐           │ (DECIMAL)       │
│ SET DIVISOR TO  │           └────────┬────────┘
│ 100 (DECIMAL)   │                    │
└────────┬────────┘                    ▼
         │                    ┌─────────────────┐
         ▼                    │ DIVIDE RESULT   │
┌─────────────────┐           │    BY   1000    │
│ JUMP TO DIVIDE  │           │   (DECIMAL)     │
│ SUBROUTINE      │           └────────┬────────┘
└────────┬────────┘                    │
         │                             ▼
         ▼                    ┌─────────────────┐
┌─────────────────┐           │ SET  TO  ADD    │
│ STORE RESULT R1 │           │ AND  ADD  PRIOR │
│ IN  MULTIPLY AND│           │    RESULTS      │
│ ADD/SUB ROUTINES│           └────────┬────────┘
└────────┬────────┘                    │
         │                             ▼
         ▼                    ┌─────────────────┐
┌─────────────────┐           │ STORE RESULT    │
│ MULTIPLY  BY    │           │ IN  ADD/SUB     │
│ 364 (DECIMAL)   │           │ INPUT REGISTERS │
└────────┬────────┘           └────────┬────────┘
         │                             │
         ▼                             ▼
┌─────────────────┐           ┌─────────────────┐
│ TRANSFER DATA   │           │ FETCH DATA FROM │
│ TO  DIVIDE      │           │ DIVIDE  INPUT   │
│      ROUTINE    │           │    REGISTERS    │
└────────┬────────┘           └────────┬────────┘
         │                             │
         ▼                             ▼
┌─────────────────┐           ┌─────────────────┐
│ DIVIDE  BY      │           │ ADD DATA  TO    │
│ 1000 (DECIMAL)  │           │   PREVIOUS      │
└────────┬────────┘           │    RESULT       │
         │                    └────────┬────────┘
         ▼                             │
┌─────────────────┐                    ▼
│ STORE  RESULT IN│           ┌─────────────────┐
│ ADD/SUB REGISTERS│          │ STORE  FINAL    │
└────────┬────────┘           │   RESULT        │
         │                    └────────┬────────┘
         ▼                             │
┌─────────────────┐                    ▼
│ STORE R1  DATA  │               ⬭ RETURN ⬭
│ IN  DIVIDE      │
│     REGISTERS   │
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│ DIVIDE BY  100  │
│ (DECIMAL) GIVING│
│ R2              │
└────────┬────────┘
         │
         ▼
         ⬭
```
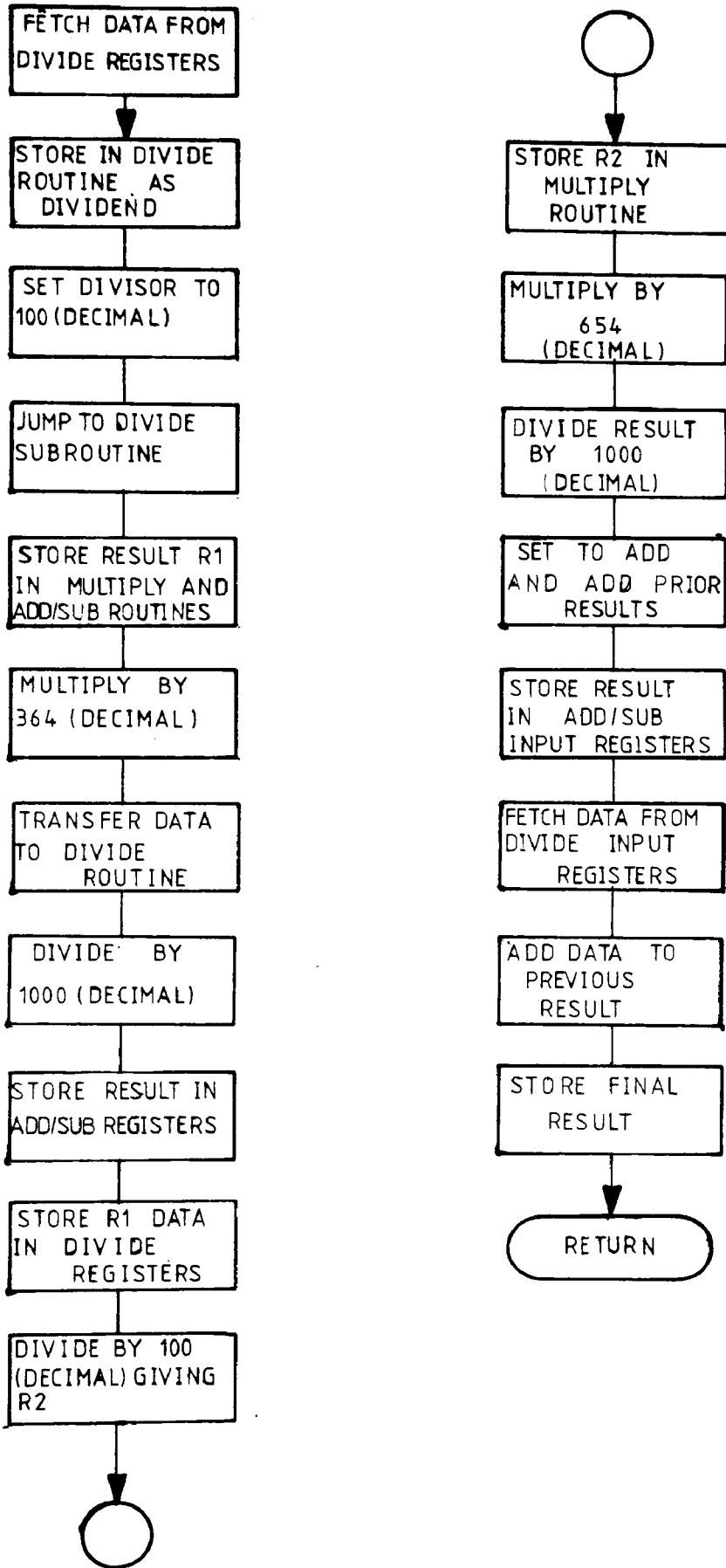
FIG 5-12   16 BIT FORMATTING/SCALING

Given the angle θ, it is assumed that a vector exists of magnitude 1 and angle θ. Figure 5-13. Thus, with this choice of magnitude, the X, Y co-ordinates of the vector give $\cos\theta$ and $\sin\theta$ directly - that is if these values can be determined.

Now, a vector of known magnitude, Mo and initial angle $\phi_o = 0$, is placed in the same X, Y place as the original unity vector. Figure 5-14.

Magnitude of vector, Mo = Mo

Initially, X co-ordinate, Xo = Mo

        Y co-ordinate, Yo = 0

        Vector angle, $\phi_o = 0$

The CORDIC technique is now applied and it involves two simultaneous operations on the vector Mo. First the vector is repeatedly rotated through an angle α, the rotation angle is gradually reduced in an almost binary fashion. After each angular rotation α, the resultant vector angle ϕ is compared to the unity vector angle θ. If it is greater, then ϕ is reduced by the next angle of α if it is smaller, then ϕ is increased so that a set of numbers of angular additions and subtractions takes place until ϕ is approximately equal to θ. Further the X and Y co-ordinates of ϕ are repeatedly adjusted to provide the new angular rotation in such a manner that the amplitude increases from Mo (which is chosen on the basis of the number of rotations) to a value of unity when $\phi = \theta$. Since the X and Y co-ordinates of the Mo vector are repeatedly calculated then their values will, after the final angular rotation, be equal to $\cos\theta$ and
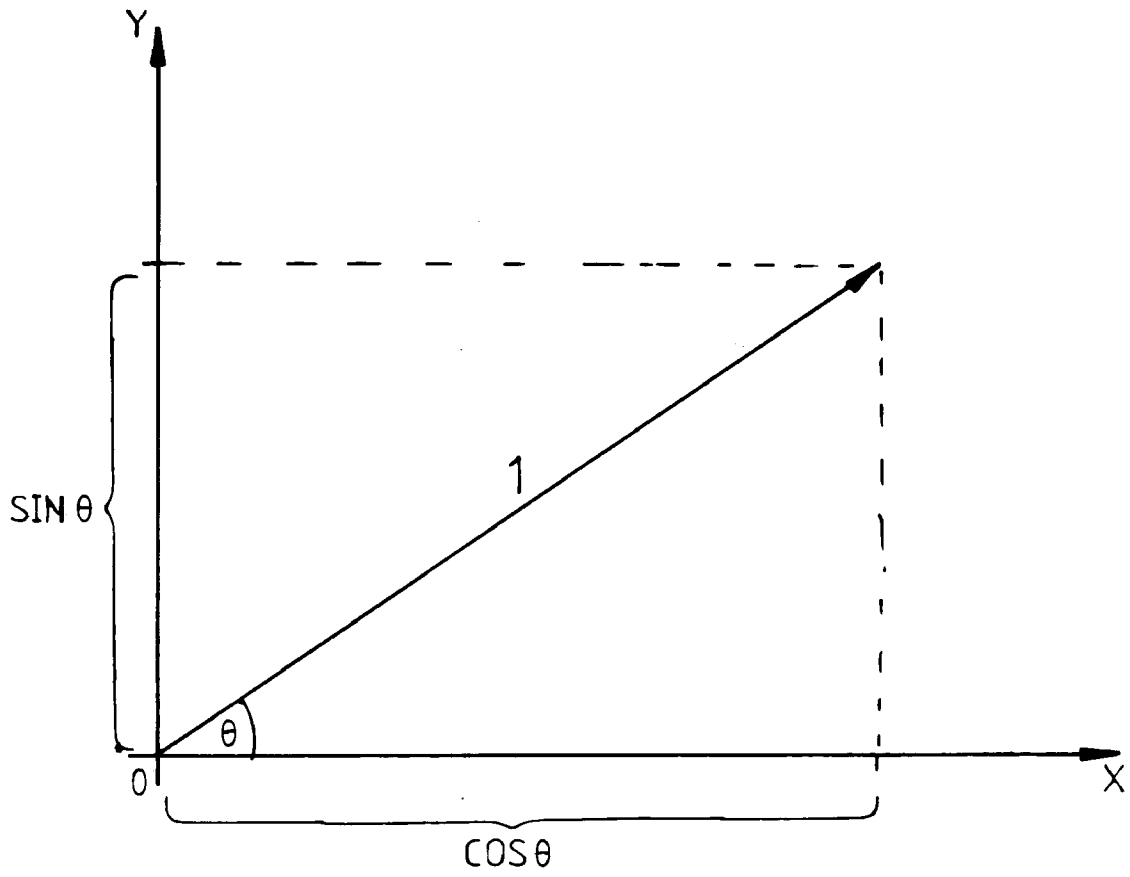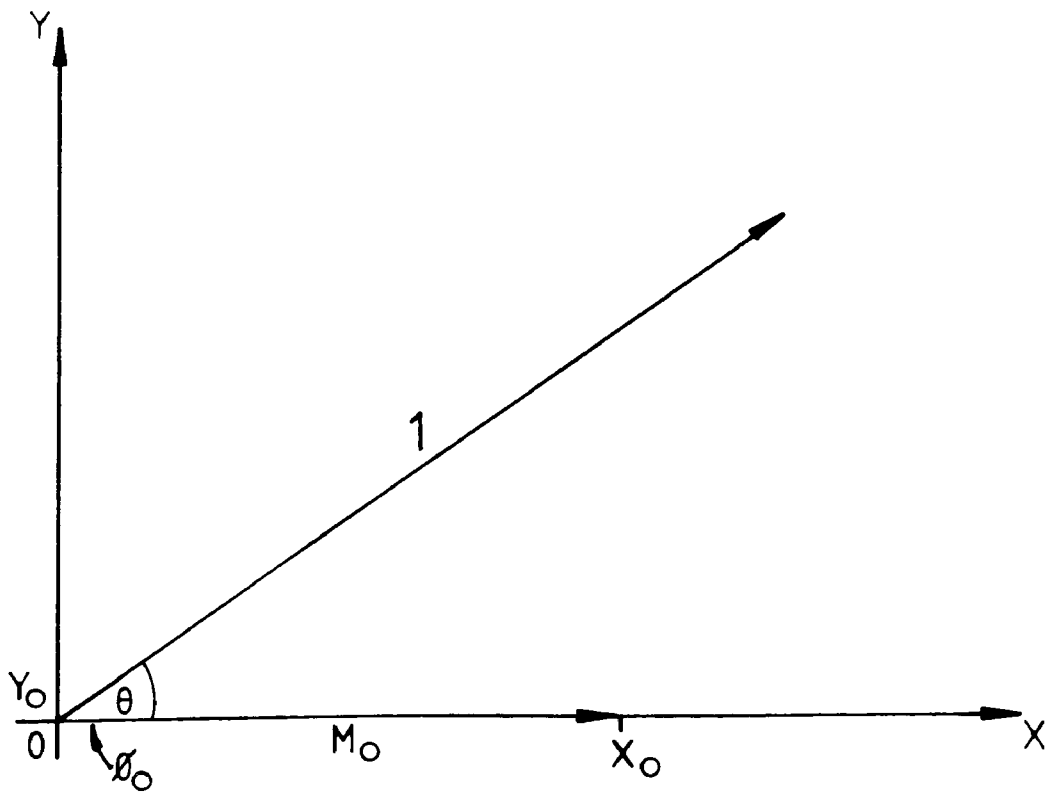
FIG 5-13

FIG 5-14

sin θ respectively.

Consider now the first rotation of the vector Mo Figure 5-15.

In this case :-

Magnitude of vector M_1 = $Mo/Cos \alpha_1$

$$X_1 = M_1 Cos (\phi_1)$$

$$X_2 = M_2 Sin (\phi_1)$$

Vector angle $\phi_1 = \alpha_1$

The magnitude of M_1 is such that it forms the hypotenuse of a right-angled triangle with the original vector Mo giving the resultant equations for the above quantities.

Now consider the next rotation. Figure 5-16.

Again, the magnitude of M_2 is such that it forms the hypotenuse of a right angled triangle with the previous vector in this case M_1. The equations become

$$M_2 = M_1/Cos \alpha_2 = Mo/(Cos \alpha_1 . Cos \alpha_2)$$

$$X_2 = M_2 Cos \phi_2 = M_2 Cos (\phi_1 - \alpha_2)$$

$$Y_2 = M_2 sin \phi_2 = M_2 sin (\phi_1 - \alpha_2)$$

Vector angle $\phi_2 = \alpha_0 + \alpha_1 - \alpha_2$

If we continue this procedure for the next vector then the form of the general equation describing the nth vector will be recognised. Figure 5-17.
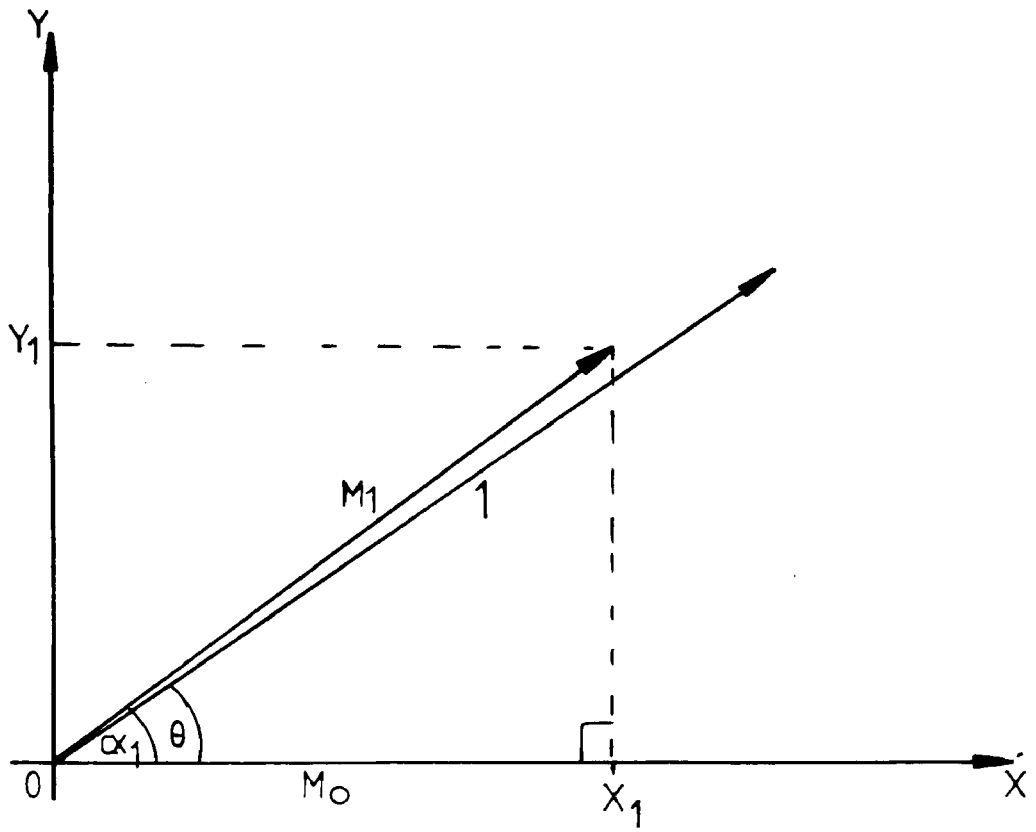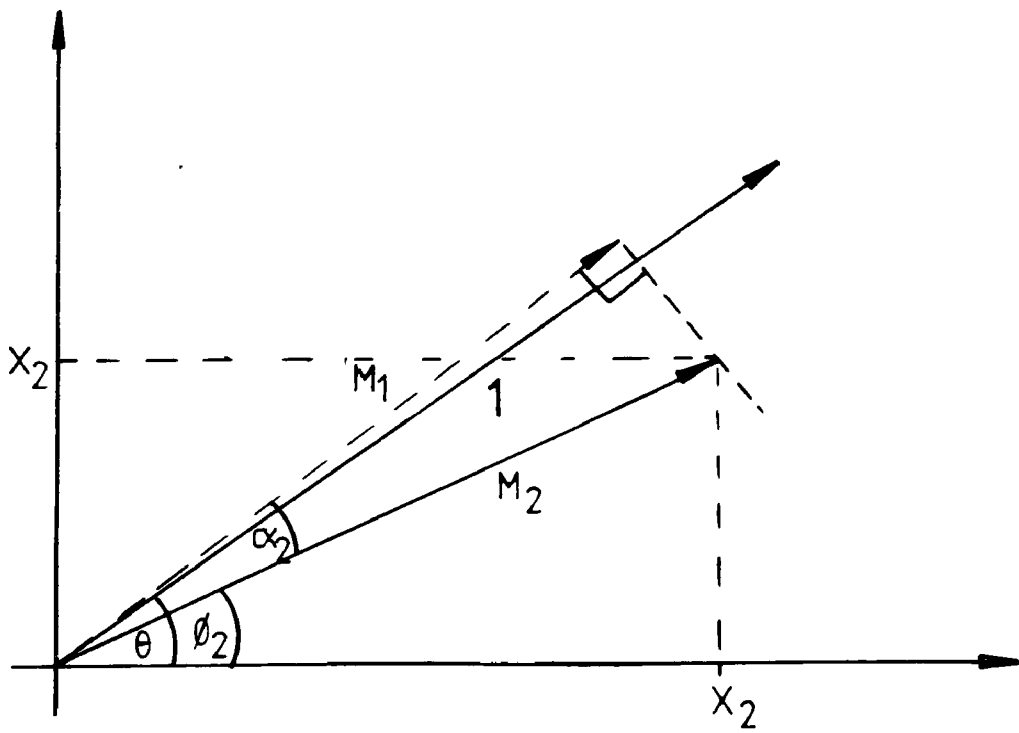
FIG 5-15

FIG 5-16

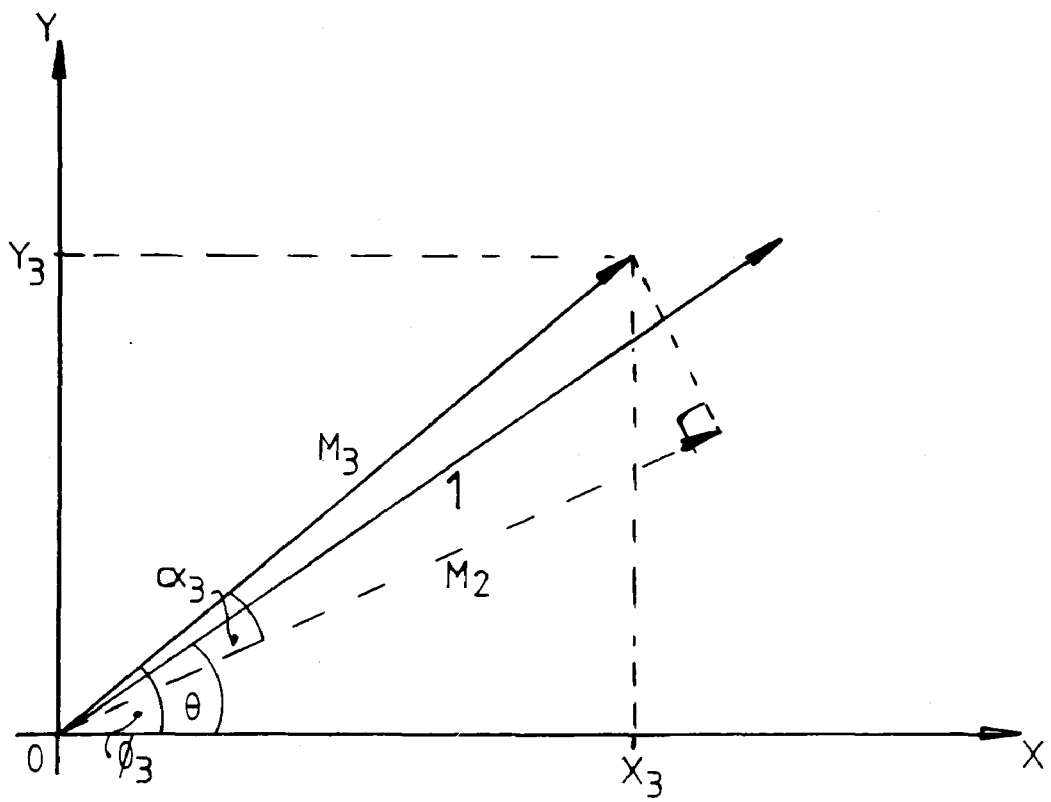FIG 5-17

Similarly

$$M_3 = M_2 \cos\alpha_3 = M_0/(\cos\alpha_1 \cdot \cos\alpha_2 \cdot \cos\alpha_3)$$

$$X_3 = M_3 \cos\phi_3 = M_3 \cos(\phi_2 + \alpha_3)$$

$$Y_3 = M_3 \sin\phi_3 = M_3 \sin(\phi_2 + \alpha_3)$$

Vector angle $\phi_3 = \alpha_0 + \alpha_1 - \alpha_2 + \alpha_3$

For the nth Vector

$$M_n = M_0/(\prod_{i=1}^{n} \cos\alpha_i)$$

$$X_n = M_n \cos(\phi_{n-1} \pm \alpha_n)$$

$$Y_n = M_n \sin(\phi_{n-1} \pm \alpha_n)$$

$$\phi_n = \sum_{i=1}^{n} \pm\alpha_i$$

Expanding X_n, Y_n

$$X_n = M_n (\cos\phi_{n-1} \cdot \cos\alpha_n \mp \sin\phi_{n-1} \cdot \sin\alpha_n)$$

$$= M_n \cos\alpha_n \cos\phi_{n-1} \mp M_n \sin\alpha_n \sin\phi_{n-1}$$

Now $M_n \cos\alpha_n = M_{n-1}$ and $M_n \sin\alpha_n = M_{n-1} \tan\alpha_n$

Thus $X_n = M_{n-1} \cos\phi_{n-1} \mp M_{n-1} \sin\phi_{n-1} \tan\alpha_n$

$$= X_{n-1} \mp Y_{n-1} \tan\alpha_n$$

Now $Y_n = M_n \sin\phi_{n-1} \cos\alpha_n \pm M_n \cos\phi_{n-1} \sin\alpha_n$

$$= M_{n-1} \sin\phi_{n-1} \pm M_{n-1} \cos\phi_{n-1} \tan\alpha_n$$
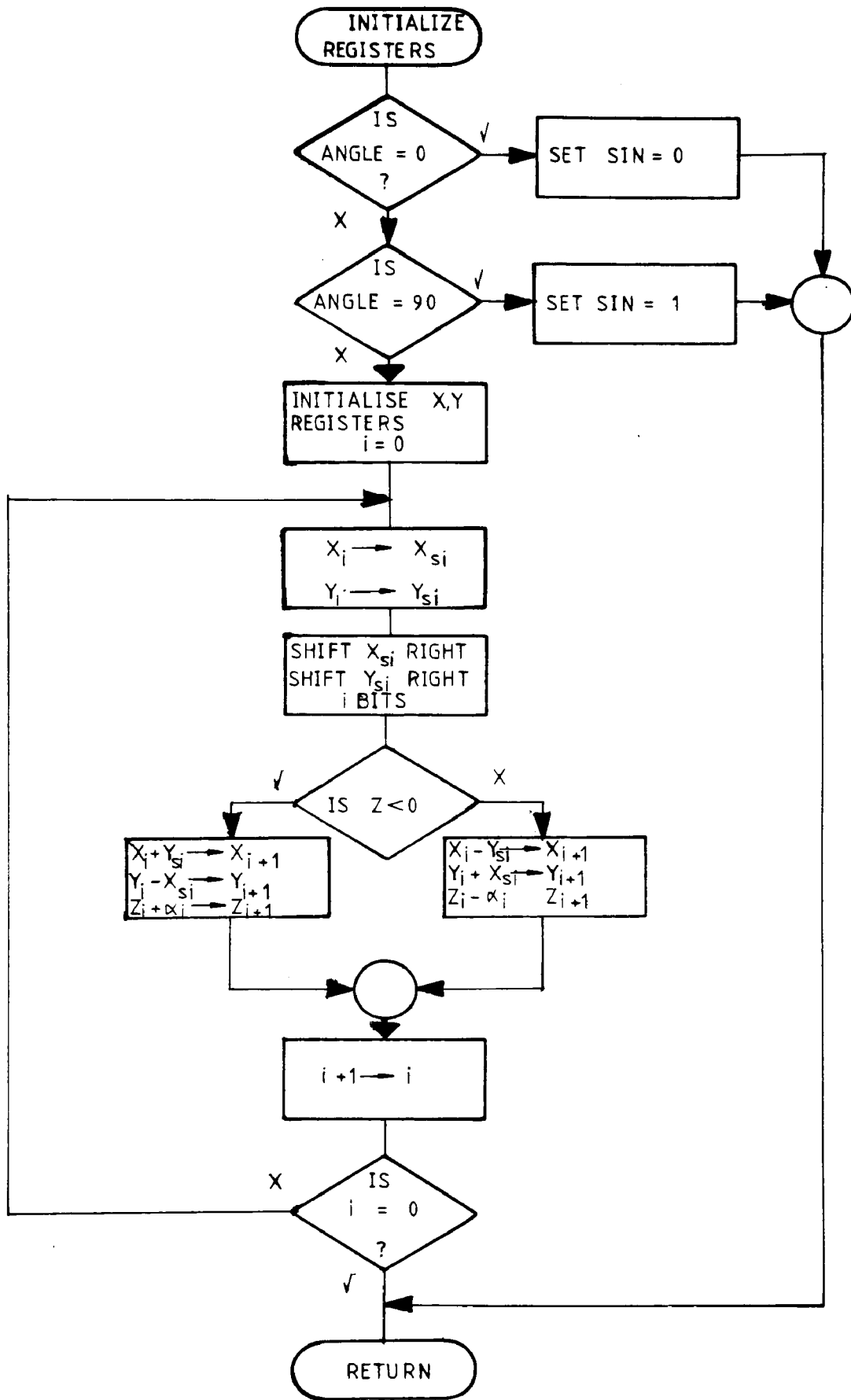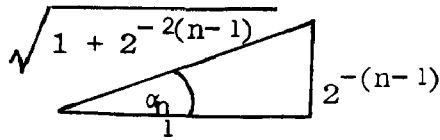
$$= Y_{n-1} \pm X_{n-1} \tan\alpha_n$$

FIG 5-18 SINE ROUTINE

If we now choose the expression for successive values of α to be given by

$$\alpha_n = \tan^{-1}(2^{-(n-1)})$$

Then

$$\cos \alpha_n = 1/(\sqrt{(1+2^{-2(n-1)})})$$

So that

$$M_n = M_0/(\prod_{i=1}^{n} 1/(\sqrt{(1+2^{-2(n-1)})})) = M_0 \prod_{i=1}^{n} \sqrt{(1+2^{-2(n-1)})}$$

And for $M_n = 1$, i.e. M_n is the final vector :-

$$M_0 = 1/(\prod_{i=1}^{n} \sqrt{(1+2^{-2(n-1)})}) \quad (1) \quad \text{(A constant pre-calculated)}$$

$$X_n = X_{n-1} \quad Y_{n-1} \cdot 2^{-(n-1)} \quad (2)$$

$$Y_n = Y_{n-1} \quad X_{n-1} \quad 2^{-(n-1)} \quad (3)$$

The flow chart for this program is shown in Figure 5-18.

5.6.9 Primary Three Phase Sort (0900-0990; 144 bytes)

The pulse width data has now been calculated and stored, in sequence, in a table. The object of this routine is now to set up the three table reference pointers which will be used by the interrupt routine to gain access to the correct pulse width data for the provision of a 3 phase output. Further, it is also necessary to store the values of the first pulses in a separate set of registers so that they can be accessed quickly, without the need for address pointers. This process allows the efficient transfer of data to the timer modules. Figure 5-19.
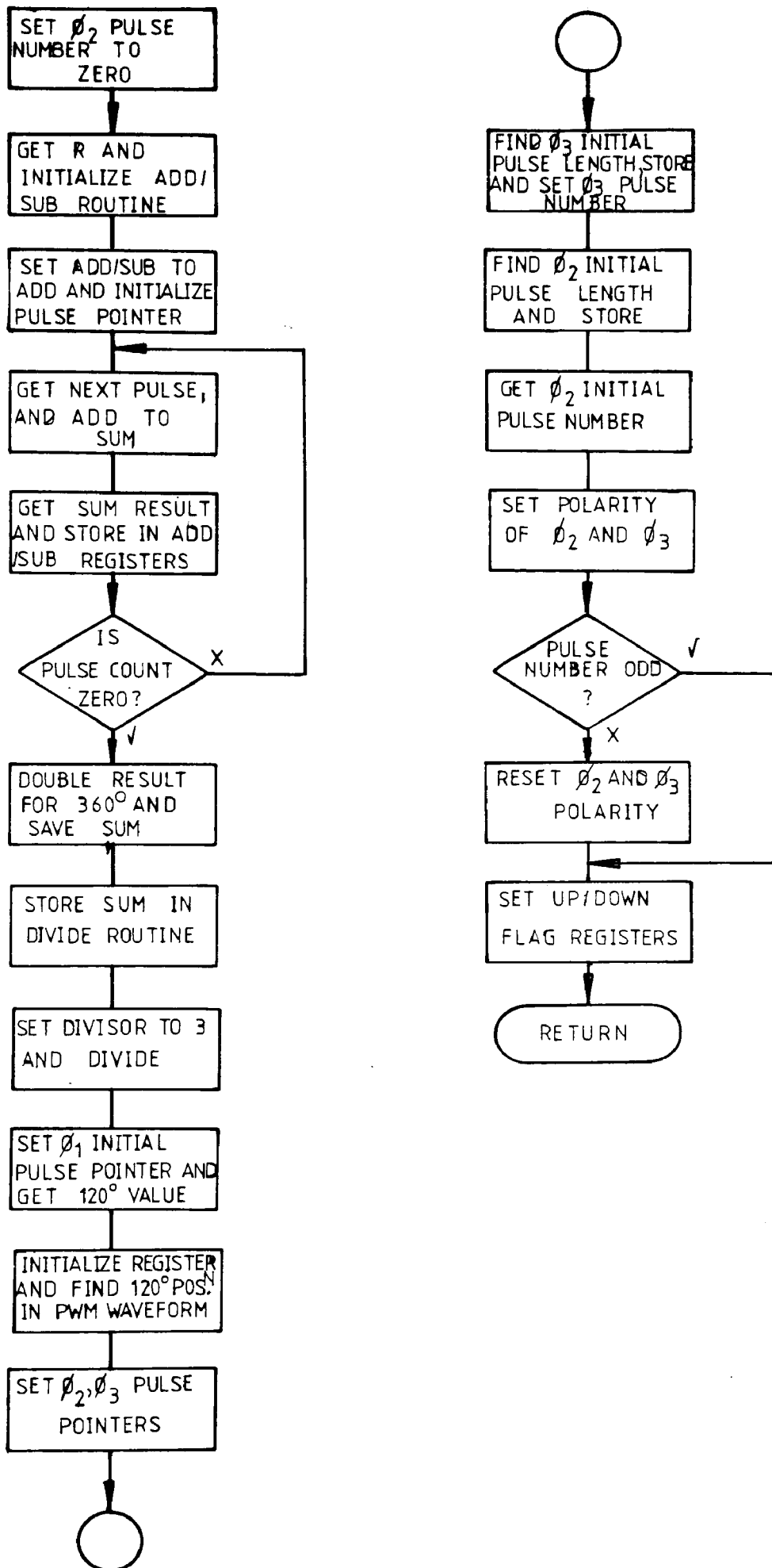
FIG 5-19

5.6.10   Secondary Three Phase Sort (0A00—0AD8; 216 bytes)

Initially we have a table which appears to provide all the required data for a 3 phase PWM-waveform generation program.

The object of this program Figure 5-20 is twofold. First, it is noted that the PTM has extra storage registers, outside the counters, which if utilized effectively, will allow a more efficient transfer of pulse width data without the need for the timer to wait for the Interrupt Routine to complete its task. Further, for unity ratios of carrier and modulating waveform, extra logical tests have to be formed in order that the correct phasing can be realised.

Each timer will require four bytes of data, two for the counter latches and another two, ready to store in this section just after the timer starts to count. That is, after the latch data has been transferred to the counter.

5.6.11   Data Output To Timer Routine (0B00—0B56; 86 bytes)

This routine Figure 5-21 is the last routine to be called by the control program.   The pulse width table and address pointers are all ready for operation. A second, identical table (used exclusively by the interrupt routine) is created. The timers are started and the appropriate pulse width values are transferred to the timer latches. The control of the microprocessor operation is then transferred from the central program back to the operating system of the microprocessor.
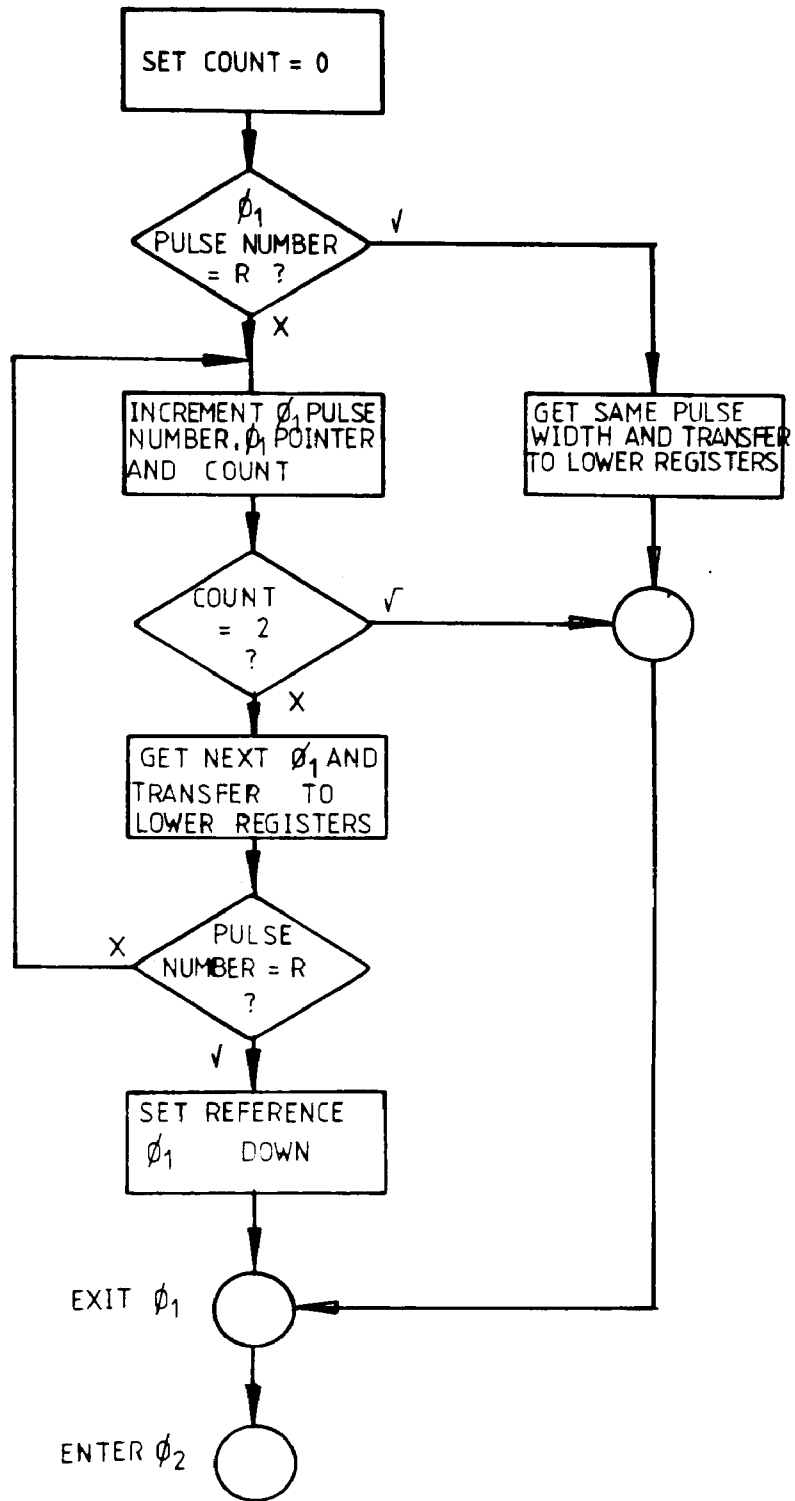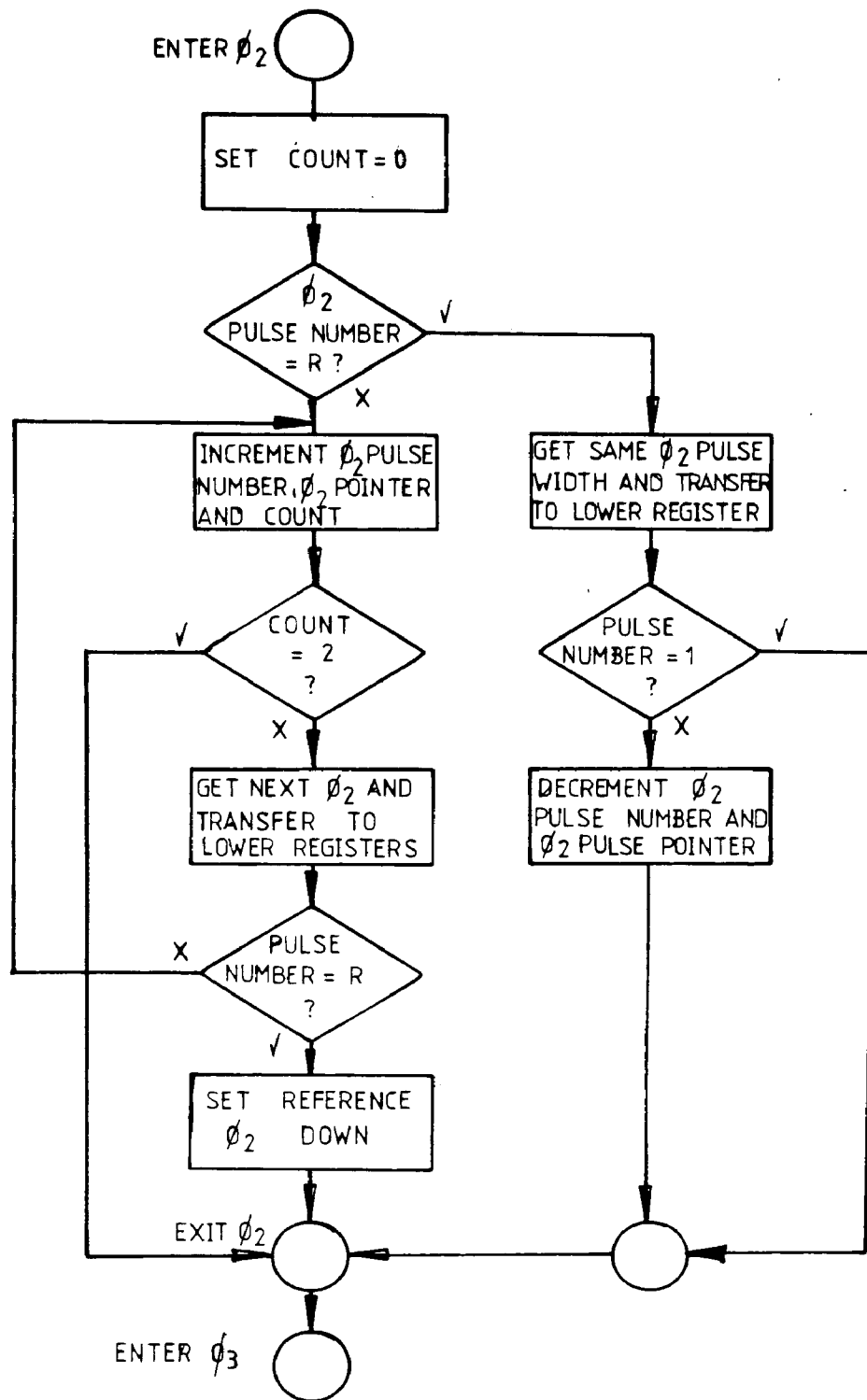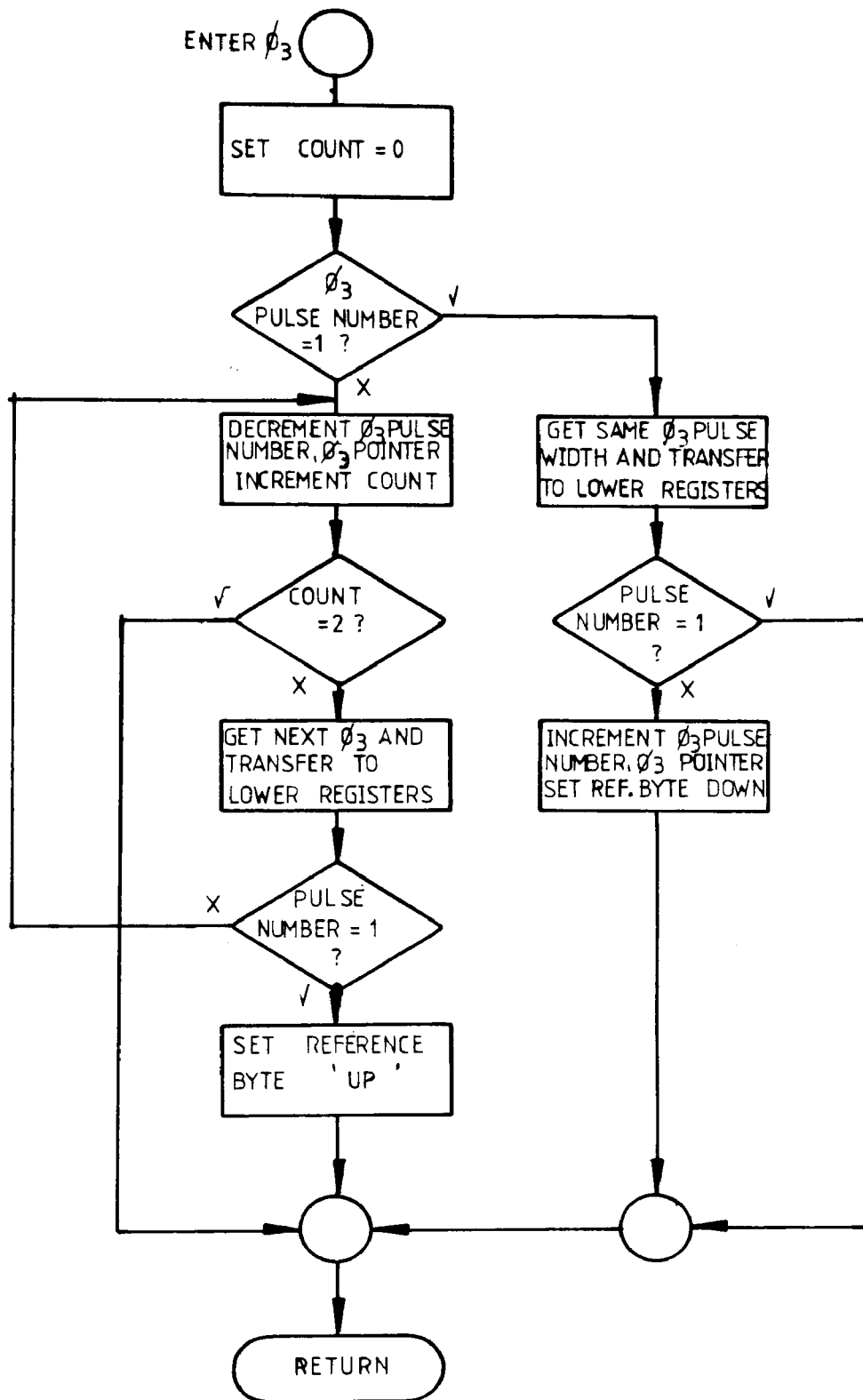
FIG 5-20(a)

FIG 5-20(b)

FIG 5-20(c)

```
                        ○

              ┌─────────────────┐
              │      SET        │
              │   INTERRUPT     │
              │     MASK        │
              └─────────────────┘

              ┌─────────────────┐
              │   SET OUTPUT    │
              │  POLARITIES OF  │
              │   Ø₁, Ø₂,Ø₃     │
              └─────────────────┘

              ┌─────────────────┐
              │ GET Ø₁,Ø₂,Ø₃ INITIAL │
              │ PULSE WIDTHS AND │
              │ STORE IN TIMER  │
              └─────────────────┘

                ┌─────────────┐
                │   START     │
                │   TIMER     │
                └─────────────┘

              ┌─────────────────┐
              │ GET NEXT Ø₁Ø₂Ø₃ │
              │ PULSE WIDTHS AND │
              │ STORE IN TIMER  │
              └─────────────────┘

              ┌─────────────────┐
              │TRANSFER PROGRAM │
              │ DATA TABLE  TO  │
              │ INTERRUPT  DATA │
              │      TABLE      │
              └─────────────────┘

              ┌─────────────────┐
              │ CLEAR INTERRUPT │
              │      MASK       │
              └─────────────────┘

                ╭─────────────╮
                │   RETURN    │
                ╰─────────────╯
```

$$\text{GET } \emptyset_1, \emptyset_2, \emptyset_3 \text{ INITIAL}$$

$$\text{GET NEXT } \emptyset_1 \emptyset_2 \emptyset_3$$

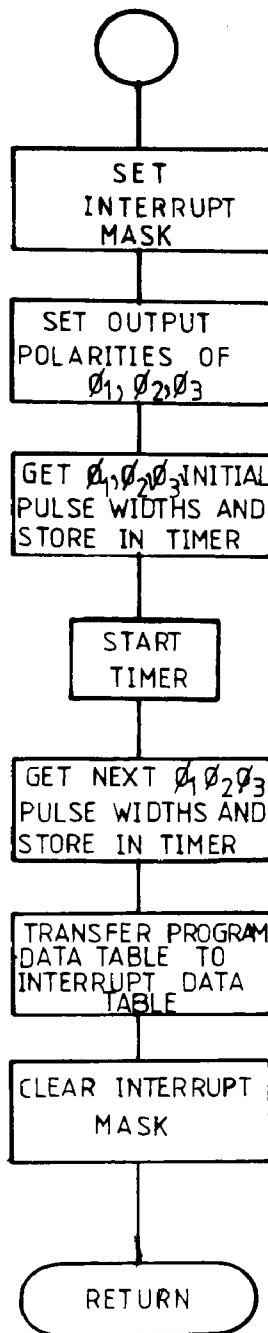FIG 5-21

5.6.12   The Control Program (0C00-0D11;   273 bytes)

This is the main program which is responsible for managing the flow of data from its input, into the system, to its final output, via the timers. This program selects each of the application programs (already decided) in the appropriate sequence in order to realise the numerical equation which determines the pulse widths. A Flow Chart of the control program is given in Figure 5-22.

5.6.13   The Interrupt Routine (0E00-0ED7;   215 bytes)

All the pulse width data, with the address pointers, have been calculated and the timer is now outputting pulses. The purpose of the interrupt routine is to update the information held in the timer counter latches and to update the pulse width address pointers (as a result of transferring pulse width data to the timers). The pulse width address pointers determine which pulse is counted next. An interrupt is generated every time the count in any register reaches zero. The interrupt routine Figure 5-23 is automatically called and it determines which timer needs servicing and supplies the appropriate data. At the end of the routine control is automatically transferred back to the operating system of the MSI 6800 system. The operating system, itself, remains unaware that an interrupt has occurred although the interrupt process is flagged by the control registers of the microprocessor.
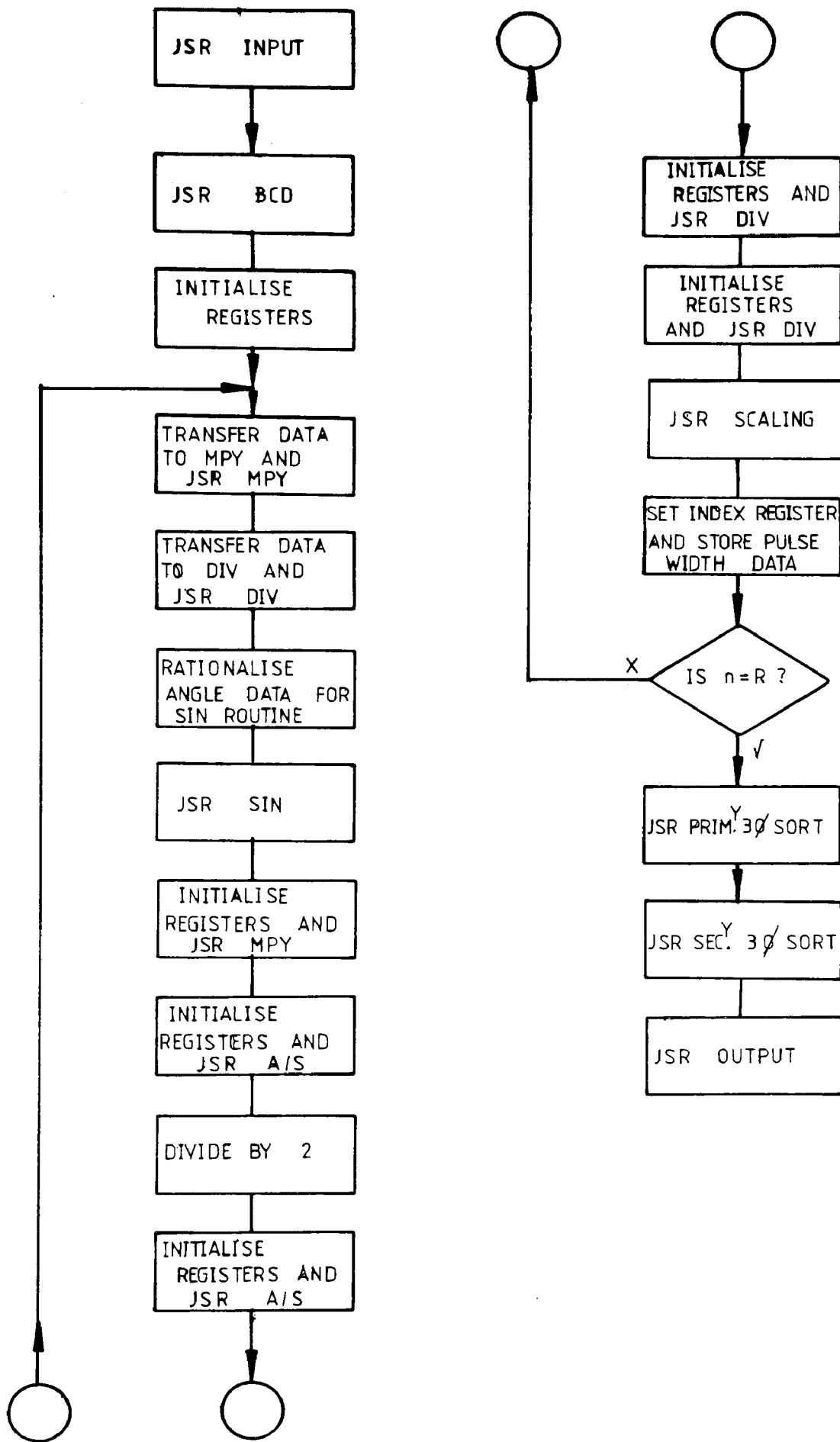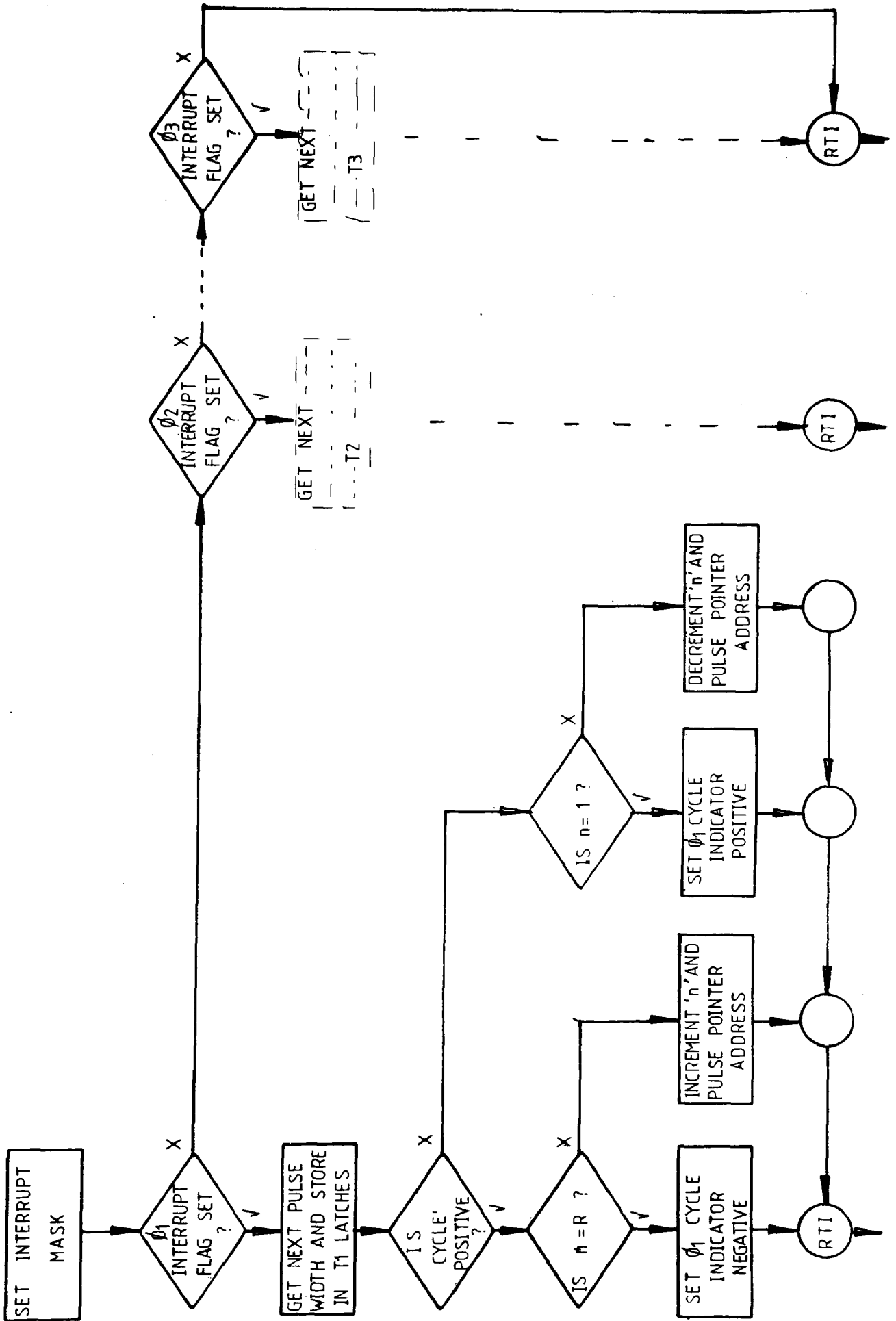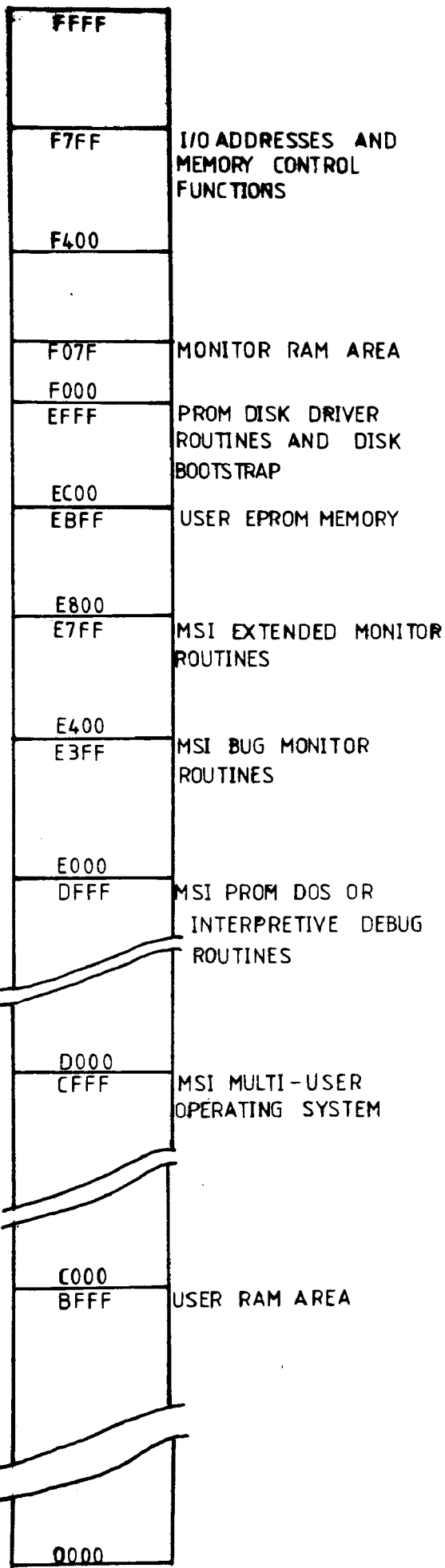
FIG 5-22

FIG 5-23

- 200 -

5.7   The Memory Map

The memory map of the program is shown in Figure 5-24. Now that the program has been developed it should be a straightforward process to incorporate all the programs in the first 2K bytes of memory - the program could be placed in a ROM. A second memory map, that of the MSI 6800 system is also included in order to demonstrate that the developed program can be incorporated in the MSI system without violating its memory areas.

5.8   Operating Method for Running the Microprocessor PWM Signals

The interrupt routine start address 0E00 is first entered in hex address F000,F001 (highest byte first). The timer is then initialised by the command G 0F00 which runs the short timer configuration routine. The timer is now ready for operation and will accept data into the latches and counters, the gating signals remaining in the 'off' state.

The main control program is called by typing in G 0C00 (0C00 being the start address (in hexadecimal) of the control program). The array of sub routines is now called in a pre-determined sequence, by the control program. A data request statement will appear on the VDU specifying the required information and range of input data. It is important to enter the specified number of decimal digits. That is, for a two digit answer, nine must be entered as 09 and so on. As this question is answered, another request will appear until the third request is answered. At this point the calculation routine will be automatically initiated and the PWM pulse times will be computed and

FFFF	
F7FF	I/O ADDRESSES AND MEMORY CONTROL FUNCTIONS
F400	
F07F	MONITOR RAM AREA
F000	
EFFF	PROM DISK DRIVER ROUTINES AND DISK BOOTSTRAP
EC00	
EBFF	USER EPROM MEMORY
E800	
E7FF	MSI EXTENDED MONITOR ROUTINES
E400	
E3FF	MSI BUG MONITOR ROUTINES
E000	
DFFF	MSI PROM DOS OR INTERPRETIVE DEBUG ROUTINES
D000	
CFFF	MSI MULTI-USER OPERATING SYSTEM
C000	
BFFF	USER RAM AREA
0000	

MSI 6800 MEMORY MAP

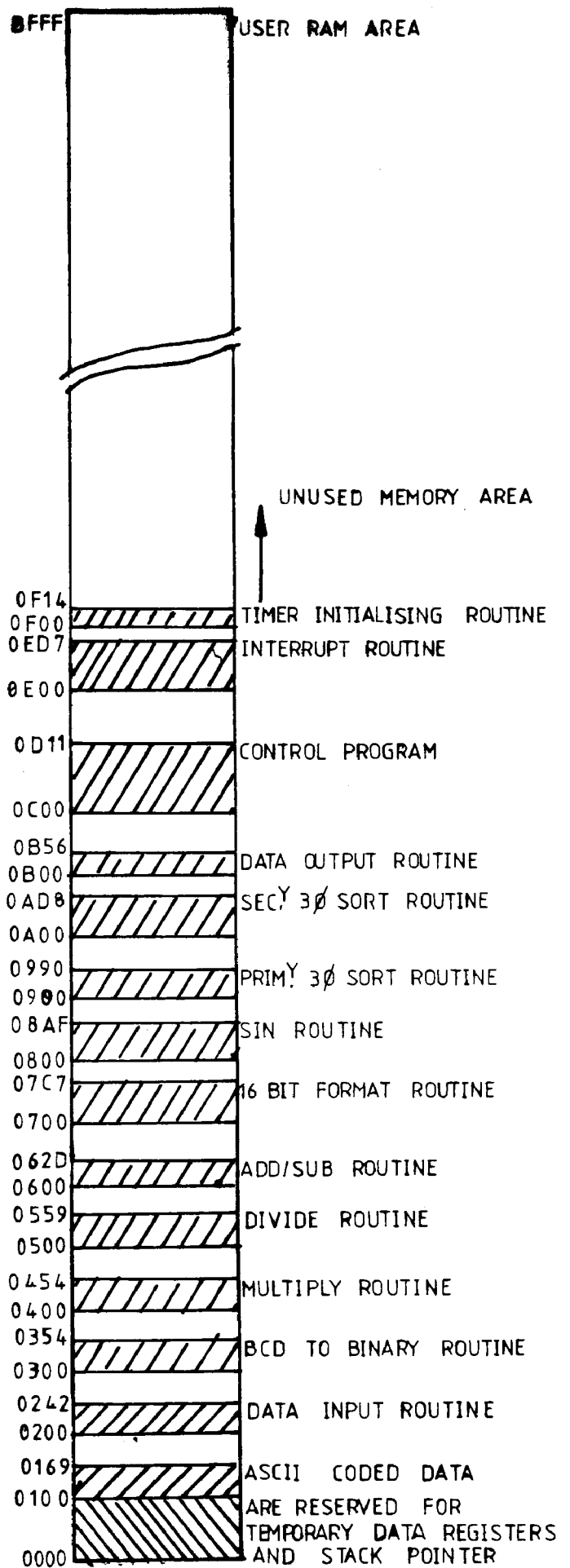|	
BFFF	USER RAM AREA
0F14	
0F00	TIMER INITIALISING ROUTINE
0ED7	INTERRUPT ROUTINE
0E00	
0D11	CONTROL PROGRAM
0C00	
0B56	
0B00	DATA OUTPUT ROUTINE
0AD8	SEC.Y 3∅ SORT ROUTINE
0A00	
0990	PRIM.Y 3∅ SORT ROUTINE
0900	
08AF	SIN ROUTINE
0800	
07C7	16 BIT FORMAT ROUTINE
0700	
062D	ADD/SUB ROUTINE
0600	
0559	DIVIDE ROUTINE
0500	
0454	MULTIPLY ROUTINE
0400	
0354	BCD TO BINARY ROUTINE
0300	
0242	DATA INPUT ROUTINE
0200	
0169	ASCII CODED DATA
0100	ARE RESERVED FOR
0000	TEMPORARY DATA REGISTERS AND STACK POINTER

UNUSED MEMORY AREA

FIG 5-24

stored in a table in memory. The table is constructed as illustrated in Figure 5-25.

Assume we have five pulses per half cycle (that is the frequency ratio is 5) - a total of 10 pulses in the period. The table will consist of five values of pulse times T1, T2, T3, T4, T5. Figure 5-26. These values will also appear in the output in that order, for the first half cycle, and then will be counted down, in reverse order in the second half cycle.

In Figure 5-25 and 5-26 ϕ_1, ϕ_2, ϕ_3 represent address pointers. If we consider ϕ_1 only, at the start ϕ_1 is pointing to T_2. When the count in the first counter of the programmable timer reaches 0 an interrupt is generated and the interrupt routine is called. A flag is set in the status register of the first counter, to indicate which timer has interrupted and needs updating. The routine accesses the table as shown. The address pointer ϕ_1 is pointing at pulse time T_1. This pulse value is therefore read and loaded into the first counter (C1). The ϕ_1 pointer value is now changed so that it points at T_2 (i.e. it is counting upwards). When T_1 is counted down to zero in C1 another interrupt is generated and the table is reaccessed - this time ϕ_1 will be pointing at T_2 and this is the pulse value transferred to the C1 counter. This continues until ϕ_1 points at T_5, at which juncture, the address pointer moves to the other side of the table and starts to count down. At each instant, when the count in C1 reduces to zero, the polarity reverses at the output ϕ_1 (this being controlled by the programmable timer).

FIG 5-25(a)
PWM POINTER ADDRESS TABLE

$\emptyset_1$ PHASE DATA

$\emptyset_2$ PHASE DATA

$\emptyset_3$ PHASE DATA

HEXADECIMAL ADDRESS

Address	Description	b_2	b_1	b_0
56	UP/DOWN REFERENCE BYTE	$\emptyset_3$	$\emptyset_2$	$\emptyset_1$
57	PULSE NUMBER FOR PHASE $\emptyset_1$			
58	PULSE WIDTH POINTER (HIGH BYTE)			
59	PULSE WIDTH POINTER (LOW BYTE)			
5A	PULSE NUMBER FOR PHASE $\emptyset_2$			
5B	PULSE WIDTH POINTER (HIGH BYTE)			
5C	PULSE WIDTH POINTER (LOW BYTE)			
5D	PULSE NUMBER FOR PHASE $\emptyset_3$			
5E	PULSE WIDTH POINTER (HIGH BYTE)			
5F	PULSE WIDTH POINTER (LOW BYTE)			
60	INITIAL PULSE WIDTH VALUE FOR $\emptyset_2$ (HIGH BYTE)			
61	(LOW BYTE)			
62	INITIAL PULSE WIDTH VALUE FOR $\emptyset_3$ (HIGH BYTE)			
63	(LOW BYTE)			
64	INITIAL PULSE WIDTH VALUE FOR $\emptyset_1$ (HIGH BYTE)			
65	(LOW BYTE)			

CYCLIC FLOW OF PULSE POINTER

$\emptyset_1$ POINTER

PULSE WIDTH OF FIRST PWM PULSE

PULSE WIDTH OF SECOND PWM PULSE

" " OF THIRD

120°

$\emptyset_2$ POINTER

PULSE WIDTH OF LAST PWM PULSE

120°

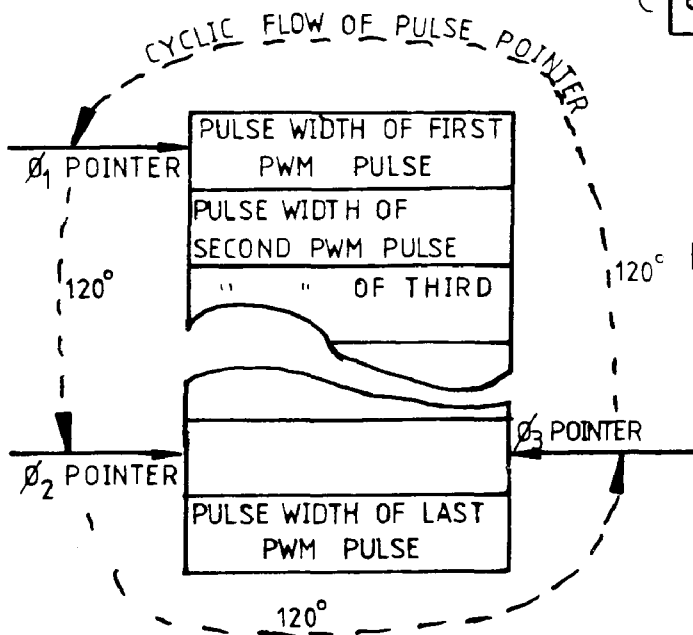$\emptyset_3$ POINTER

120°

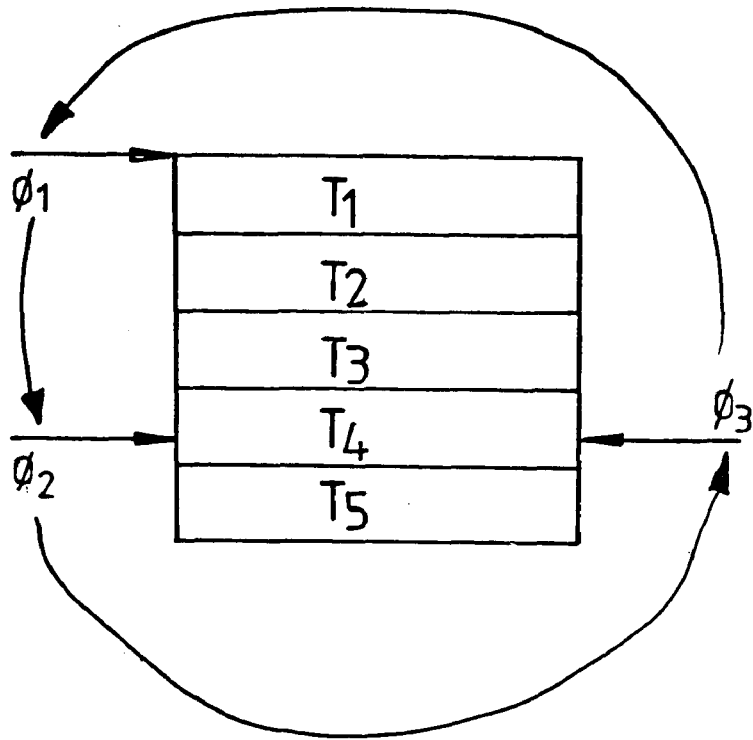# FIG 5-25(b) CYCLIC FLOW PWM PULSE WIDTH TABLE
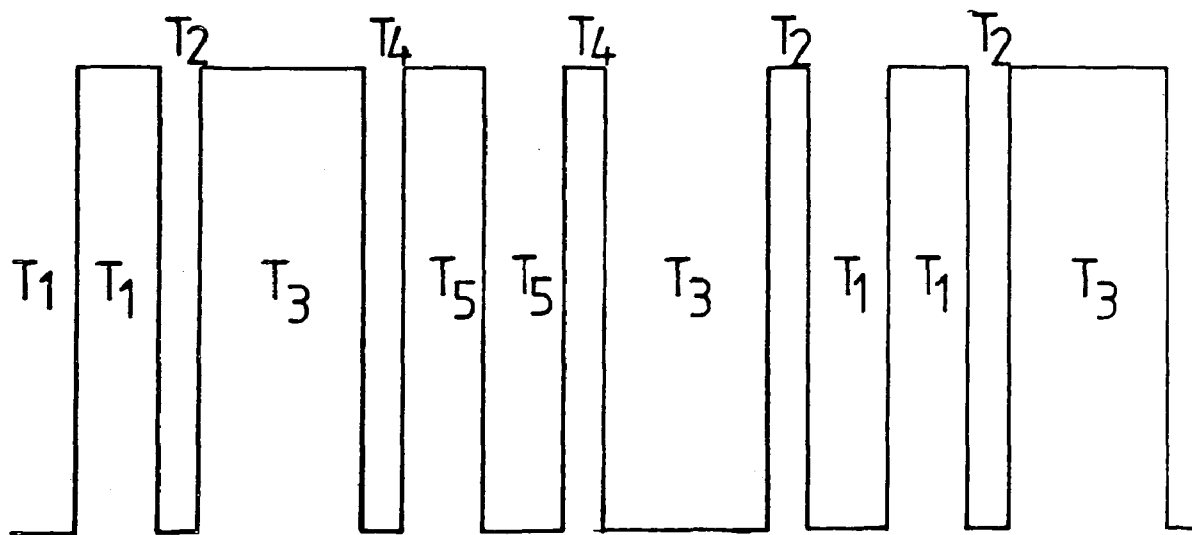
TABLE OF PULSE WIDTH VALUES

FIG 5-26

It can be seen that the pointer ϕ_1 circles around the tables. Similarly both ϕ_2 and ϕ_3 circle around the table each maintaining a 120° separation from the other. It is sometimes considered useful to view the action of the software as similar to the operation of a hardware ring counter with three stages - each stage being 120° removed from the previous stage.

Since timing data is entered via the interrupt routine new data can simply be entered by re-running the program, typing G 0C00. As the program is run and new data is entered so the microprocessor will continue to interrupt, when commanded by the timer, and update the timers so that it appears that parallel processing is being achieved.

The whole process can be halted simply by pressing the 'Reset' button on the MSI microcomputer. Both the control and status registers of the PTM are cleared by initiating the 'Reset' Line.

The output waveforms immediately disappear leaving all output terminals at zero. If system operation is to be resumed from this point, it is important to note that, first one must type G 0F00 before proceeding with G 0C00 since the timer registers have to be re-configured.

CHAPTER 6   Analysis of Results

6.1   Introduction

It was already clear from research reported in the literature that the use of an unsymmetrical carrier signal would increase the harmonics present in the PWM waveform. The use of a sinusoidal carrier has also been investigated and found to be inferior, in operation, to the use of a symmetrical triangular carrier and sinusiodal modulating waveform.

It was therefore concluded that initial investigations would concentrate on the comparison of the sinsoid/triangle PWM system with the stepped sinusoid, regular sampled symmetric and regular sampled asymmetric waveform/triangular carrier system.

6.2   Circuit Operation of Carrier/Modulating Signal Generator

Figure 6.1 shows a photograph of the triangular carrier waveform for a frequency of 100Hz. The sampling pulse, $50\,\mu$s wide and generated by a 555 timer, are shown beneath this waveform and it can be seen that they are synchronised to the apices of the carrier signal (as required in the regular sampled asymmetric mode of operation).

These pulses are used to sample the signal or modulating waveform, the result being shown in Figure 6-2 - a small phase shift has occurred, equivalent to one period of the sampling waveform. The frequency of the signal waveform is about 20 - 25Hz giving a frequency ratio of 4-5. That is, the triangular waveform will have 4-5 periods
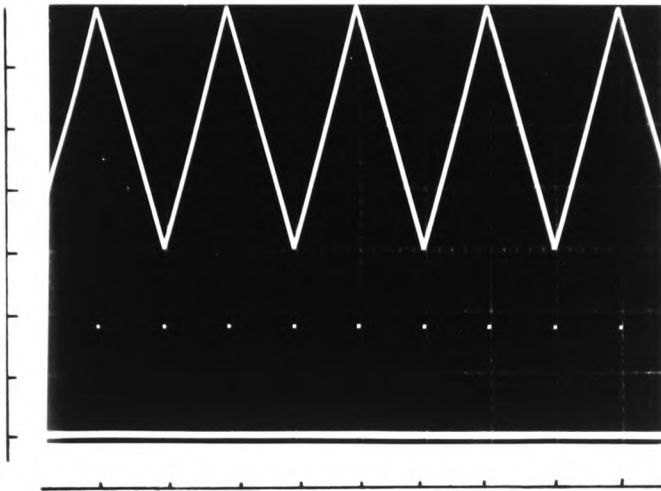
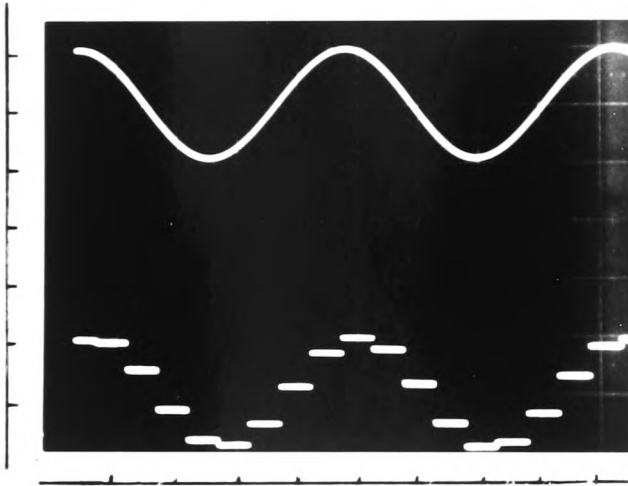FIG6-1 TRIANGULAR CARRIER AND SYNCHRO-NISED SAMPLING PULSES

SCALES:-

1Vlt./Cm

5mS/Cm

FIG6-2 NATURAL AND REGULAR SAMPLED SINUSOID MODULATION
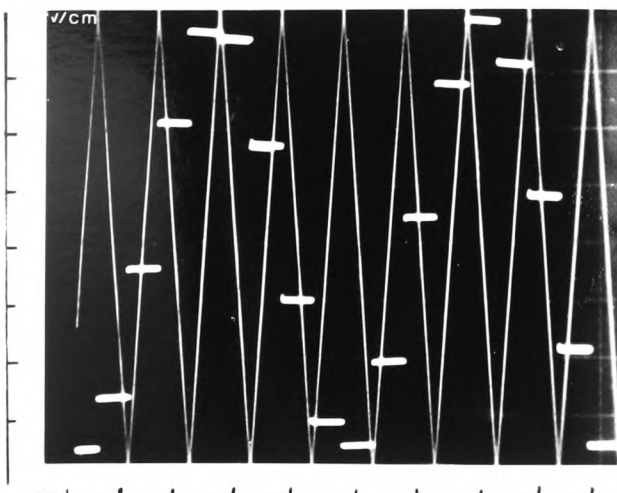
SCALES:-

2 Vlts/Cm

10mS/Cm

FIG6-3 COMPARISON OF MODULATION AND CARRIER SIGNALS

SCALES:-

0·5Vlts./Cm.

10mS/Cm.

for every one period of the signal waveform and the PWM waveform will have five pulses for every half period as shown in Figure 6 - 3 and 6 - 4. It can also be seen that the number of steps in a complete period of the regular sampled signal waveform is equal to twice the value of the frequency ratio. The two waveforms are shown, superimposed upon each other so that the switching points of the comparator can be estimated from the photograph. Figure 6 - 4 shows the signal and carrier waveforms as the input to the comparator and the PWM waveform as the resulting output. It can be seen that the switching points of the PWM waveform are synchronous with the crossover points between the triangular wavform and the stepped sinusoid waveform.

Figure 6 - 5 shows the four waveforms required to produce the PWM output whilst Figure 6 - 6 shows the triangular output from the integrator, the square wave input to the integrator and the switching pulse outputs of the comparators (which produce the squarewave) of the complete oscillator loop of the waveform generator board.

Figure 6 - 7 shows, in detail, the edge of one of the positive pulses of the PWM waveform (the first waveform) and the 100μs pulse (the third waveform) generated and synchronised to this edge. The second waveform shows the resultant PWM waveform showing that a 100μs period has been removed from the leading edge of the waveform. This delay allows 100μs for the recovery of the switching thyristors of the McMurray Bridge inverter. The fourth waveform of Figure 6 - 7 shows two 10μs pulses synchronised to the leading and trailing edges of the 100μs pulse. These pulses are necessary for operating the commutating thyristors of the bridge inverter, they initiate the turn on of the
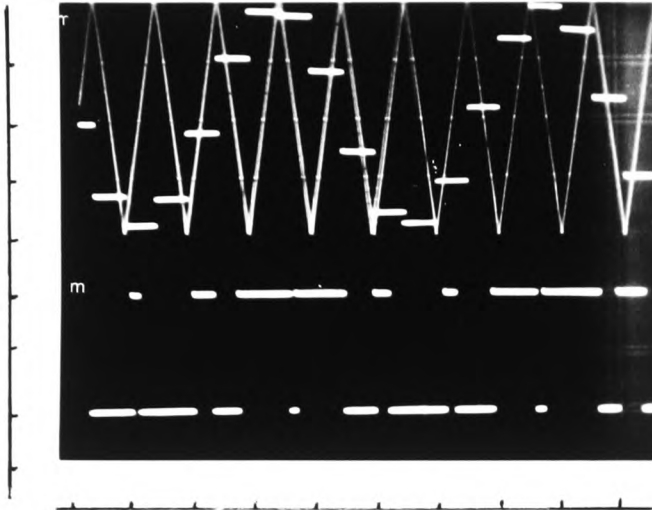
FIG 6-4 SHOWING THE
TWO SIGNAL INPUTS
AND THE PWM OUTPUT
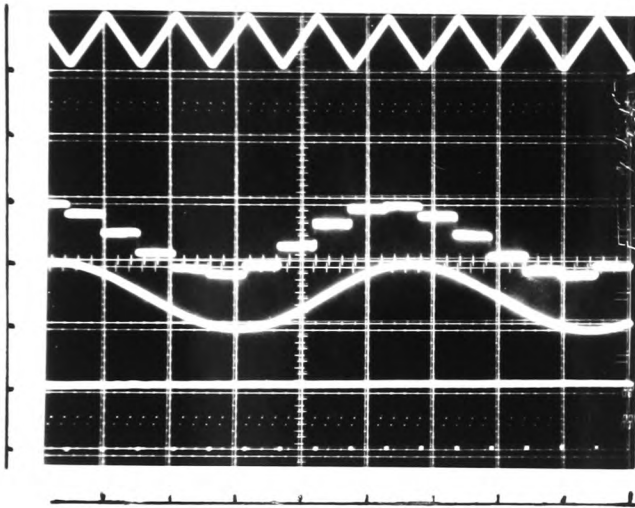OF THE COMPARATOR
SCALES:-
  1Vlt/Cm
  5Vlts/Cm
  10mS/Cm

FIG6-5 THE CARRIER,
MODULATION AND
SAMPLING SIGNALS
SCALES:-
  10Vlts/Cm
  2Vlts/Cm
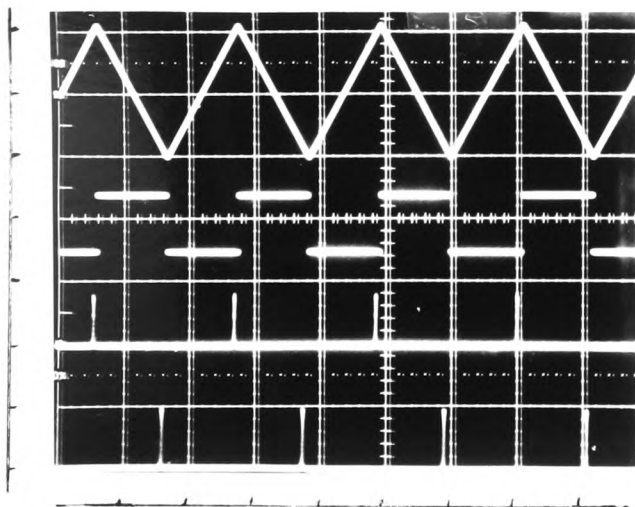 2Vlts/Cm
  10Vlts/Cm
  10mS/Cm

FIG 6-6 THE TRIANGULAR,
SQUARE AND PULSE
SIGNALS OF THE
WAVEFORM GENERATOR
SCALES:-
  2Vlts/Cm
  5Vlts/Cm
  5Vlts/Cm
  5Vlts/Cm
  5mS/Cm

auxiliary thyristors which then cause the appropriate thyristor of the McMurrary Bridge to turn off.

Figure 6 - 8 shows the four output waveforms obtained from the pulse sequencing network. These four signals are generated from a single phase PWM waveform and are necessary for the proper operation of one phase of the three phase thyristor bridge circuit. The other two phases have identical waveforms except that their phases differ (with respect to the first phase) by + 120° and - 120°.

The uppermost waveform of Figure 6 - 8 shows the pulse waveform to the commutating thyristor.

The pulses occur at the trailing edge of the waveform. The waveform below this is the signal which controls one of the two power thyristors in the bridge unit. Similarly the third waveform controls the next commutating thyristor, the pulses being at the leading edge of the lowest waveform - the complementary drive which controls the second power thyristor in the bridge. It is to be noted that the two waveforms controlling the power thyristors are complementary and do not overlap each other i.e. power shorts in the bridge are avoided.

The waveforms in Figure 6 - 9 show the voltage and current of the motor coil of the same phase (the lower and upper waveforms respectively). It can be seen that the lower waveform is a 5 - level waveform as opposed to the two level voltage input whilst the current would represent the integral of the voltage waveform - as the motor inductance would be the dominant factor in determining the current on no-load.
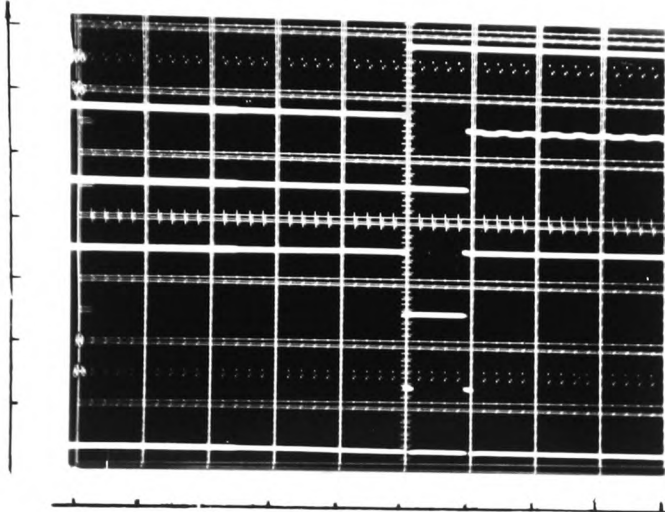
FIG6-7 SHOWING THE INPUT PWM SIGNAL BEING PROCESSED BY THE PULSE SEQUENCE NETWORK
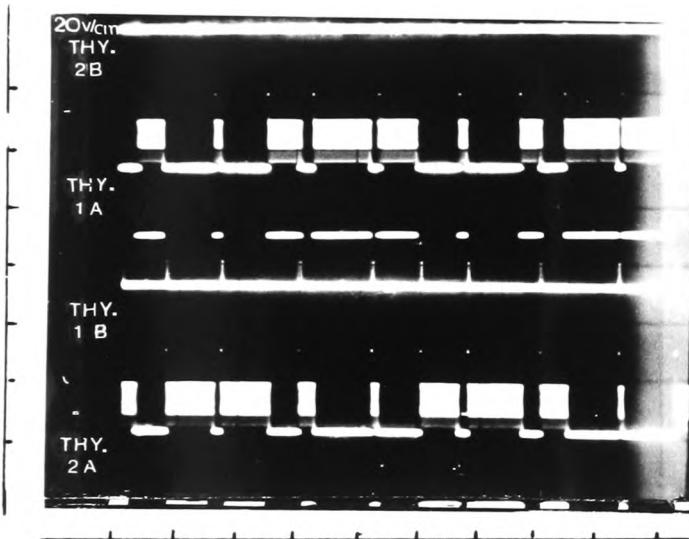
SCALES:-
100µS/Cm
10Vlts/Cm

FIG6-8 INVERTER BRIDGE WAVEFORMS FOR ONE OF THE PHASES

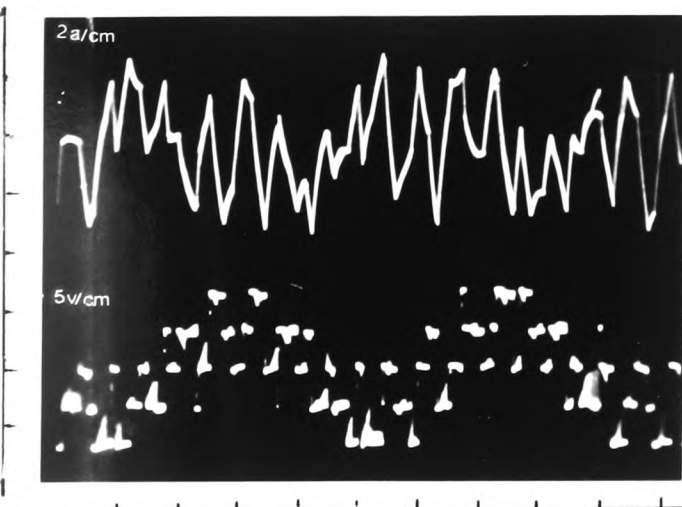SCALES:-
20Vlts/Cm
10 mS/Cm

FIG6-9 ONE OF THE PHASES OF THE THREE PHASE DRIVE TO THE MOTOR SHOWING CURRENT AND VOLTAGE

SCALES:-
2Amps/Cm
5Vlts/Cm
10 mS/Cm

## 6.3   PWM Run Test - The Analogue System

Motor run tests were performed for three differing types of PWM waveform :

1.   The 'Natural' PWM waveform.

2.   The Regular Sampled Symmetrical PWM waveform, and

3.   The Regular Sampled Asymmetric PWM waveform.

Other waveforms, such as those generated by the use of single sided sawtooth carrier waveforms, were not considered because of their inferior frequency spectrum characteristics.

With these three waveforms a total of five differing practical properties were obtained. Motor performance was measured by applying PWM waveforms of a particular type and fundamental frequency and then recording the speed of the rotor of the induction motor. It was found that on some occasions the final speed of the rotor would differ, dependent on whether the PWM waveform was applied when the motor was at rest or whether the PWM waveform was applied when the motor was already running at speed and only a small increment in speed was required.

In Figure 6 - 10 the operational characteristics for the different waveforms and for different starting conditions are shown for the 100Hz motor. It can be seen that the characteristic, in the case of natural PWM, is improved by operating the motor from speed rather than from rest. This can be accounted for in that the extra

FIG 6-10 PWM RUN TEST 100 HZ / 415 V MOTOR
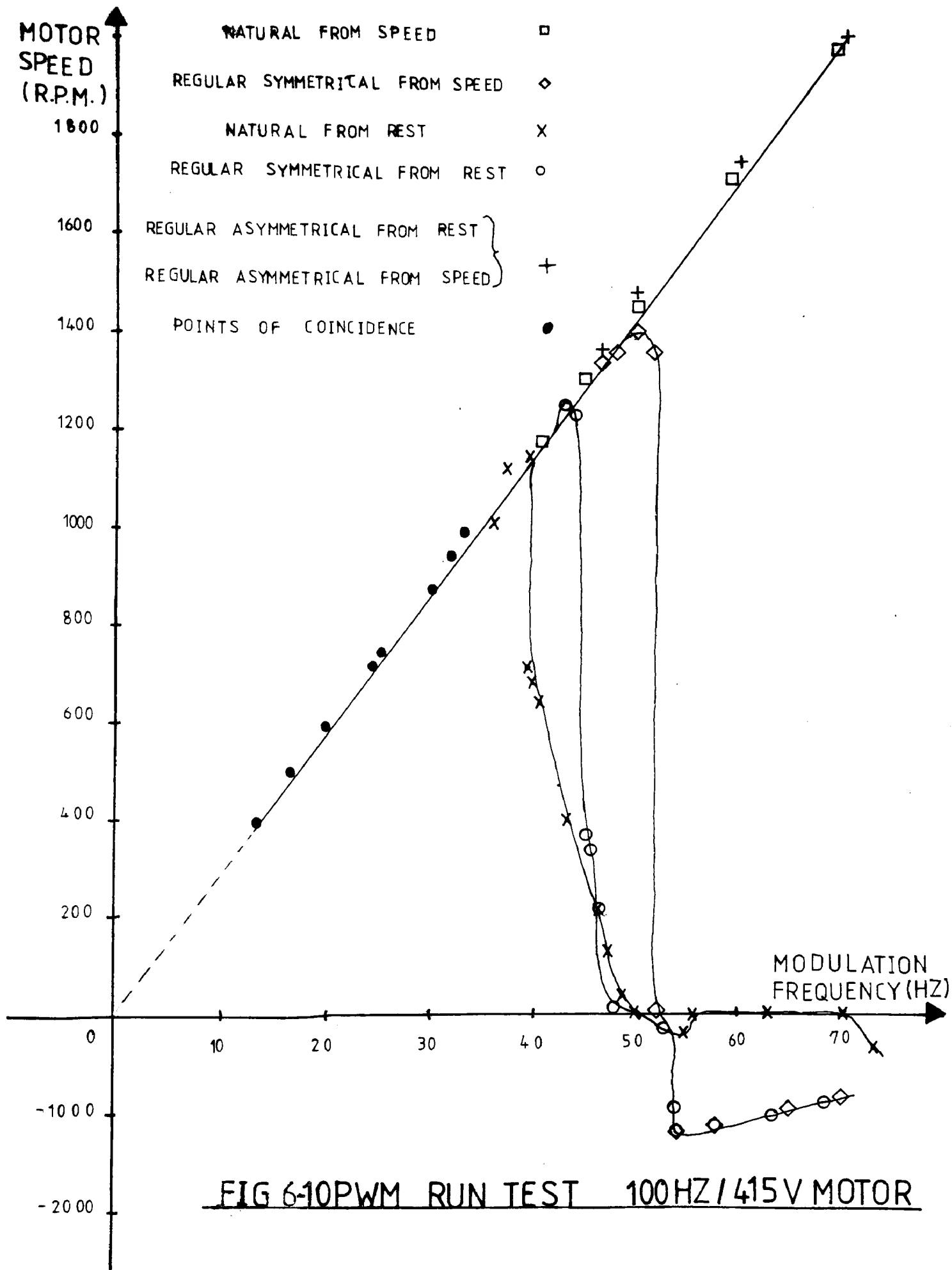
inertia of the motor produces a torque large enough to overcome the torque existing at the lower frequency which exists in the PWM waveform drive.

It is also clear from Figure 6 - 10, that the Regular Sampled Asymmertric PWM waveform drive is superior to all other modulation techniques considered (especially at low frequency ratios) giving about twice the speed control range.

A second run test with a 50Hz motor and the same maximum V/F ratio conditions was conducted and the results are shown in Figure 6 - 11. It can be concluded that the natural sampled modulation technique improves the range of speed control by 12% in this case. However, Figure 6 - 12 shows the results for the same conditions except that the maximum V/F ratio is increased - in this case the Regular Sampled Asymmetric form of modulation improves the range of speed control by some 40%.

It can therefore be concluded that the Regular Sampled Asymmetric form of PWM can improve the speed control range by some 40% over that of the Natural Sampled form of PWM given that the V/F ratio is properly controlled. This improvement is also obtained at low values of frequency ratio where the figure is of the order of 2 - 3.

The controlled speed range for the 100Hz and 50Hz motors, using Regular Sampled Asymmetric PWM is 5:1 and 9:1 respectively whilst the relationship is substantially linear. The motor current/speed relationships are defined by Figures 6 - 13 and 6 - 14. A set of balanced 1ohm resistors were placed in series with the stator coils in order to measure the current flow. Large values of current occur in
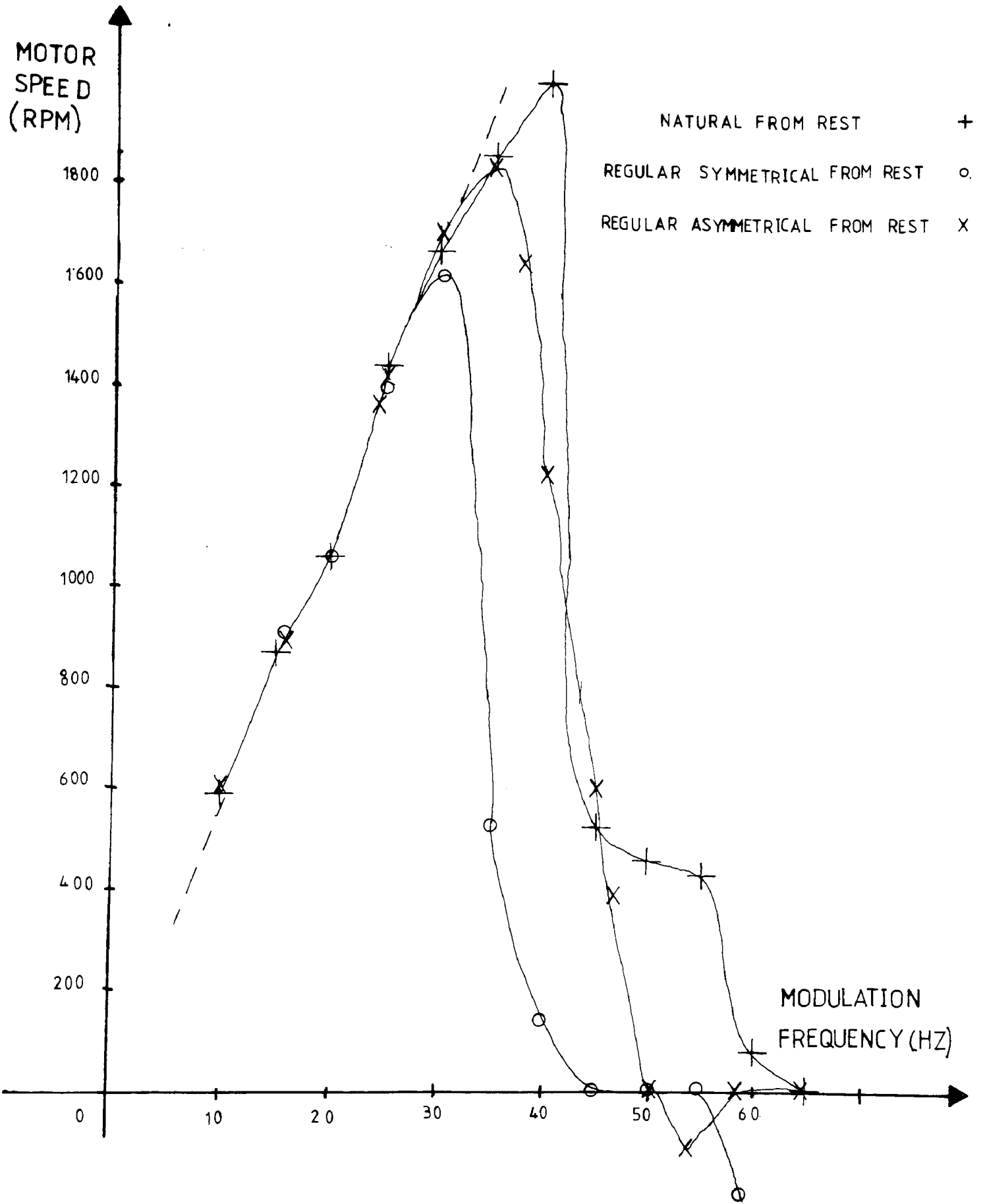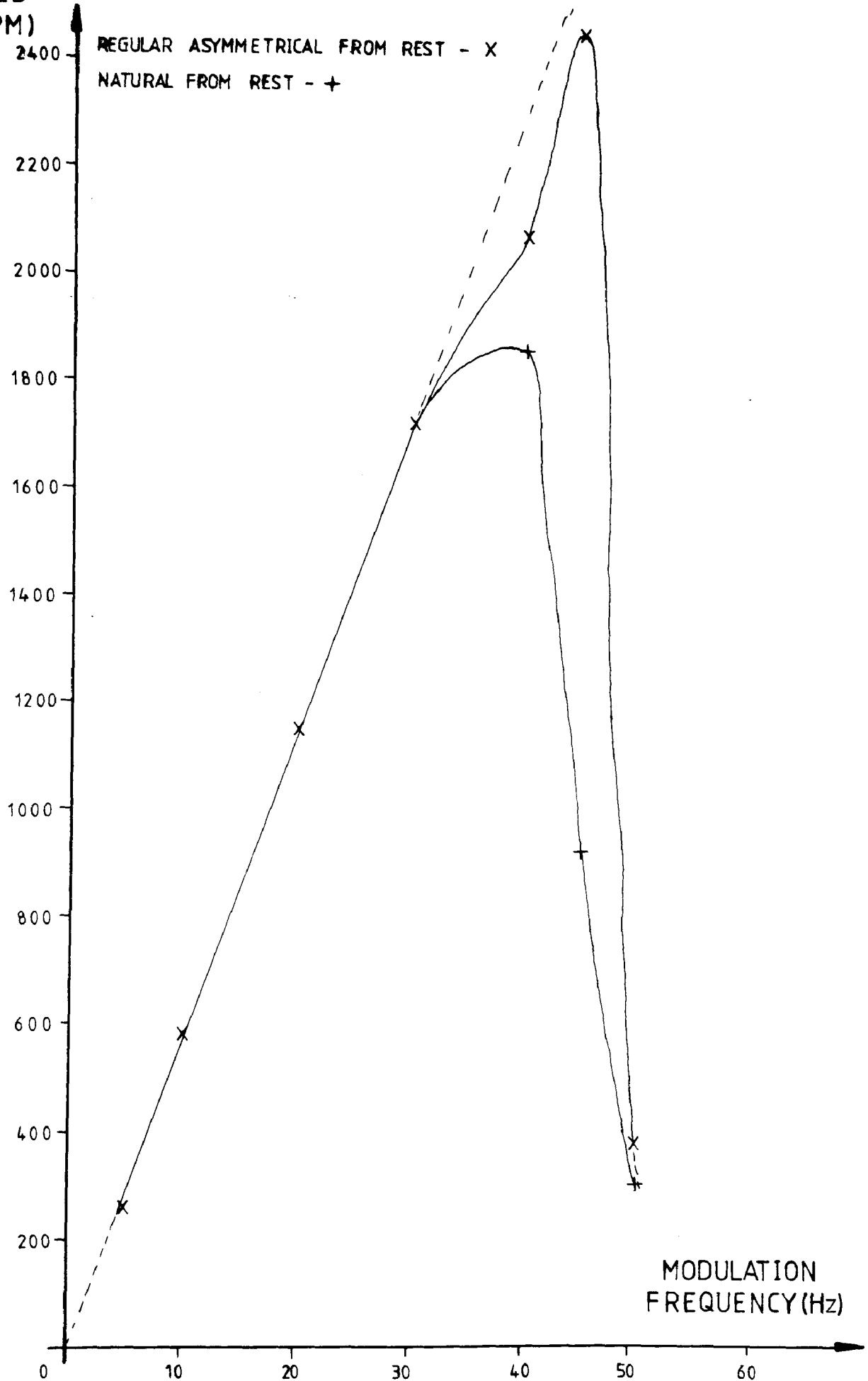
FIG 6-11 PWM RUN TEST - 50HZ / 415V MOTOR
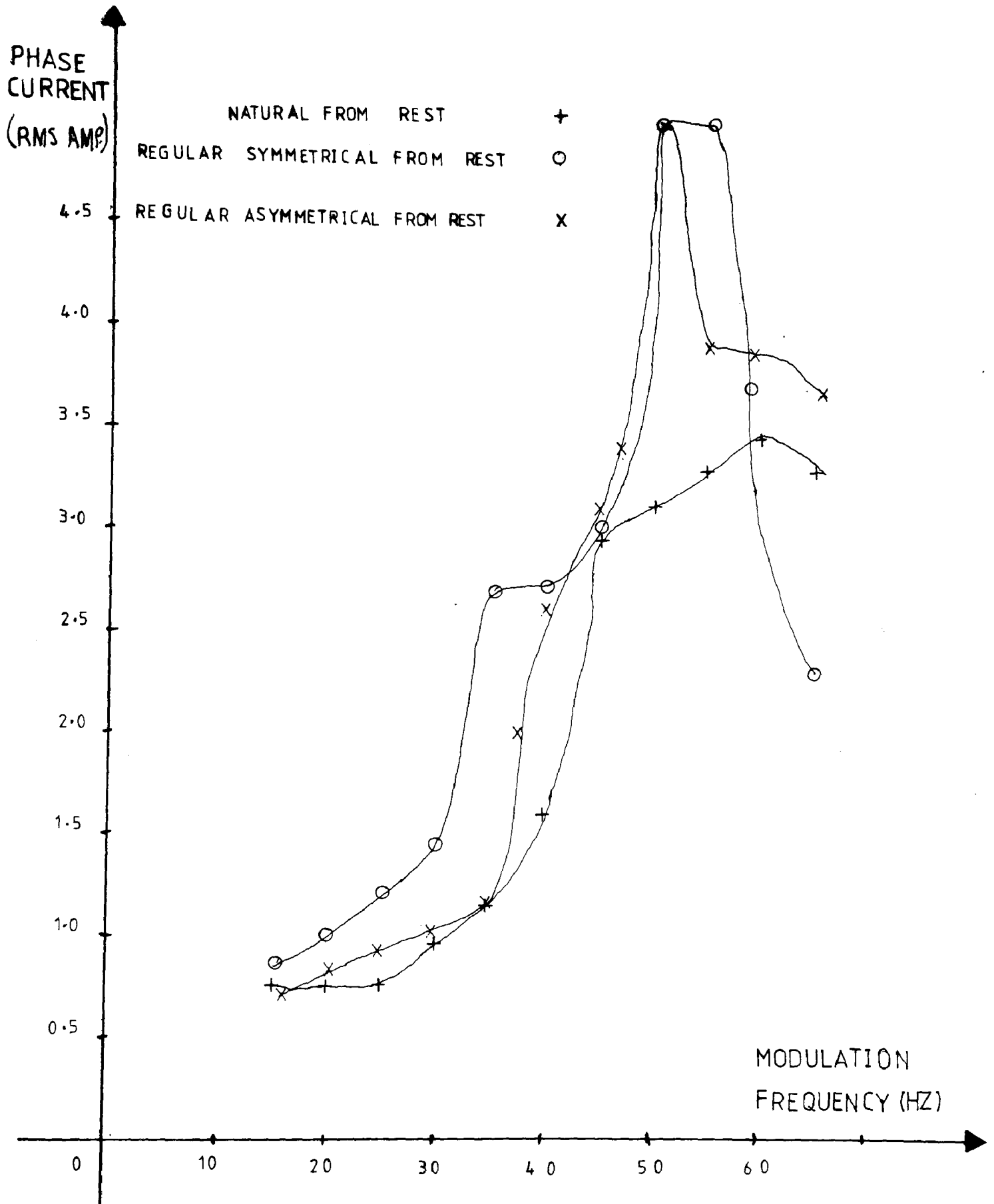
FIG 6-12   SECOND PWM RUN TEST –50Hz/415V MOTOR

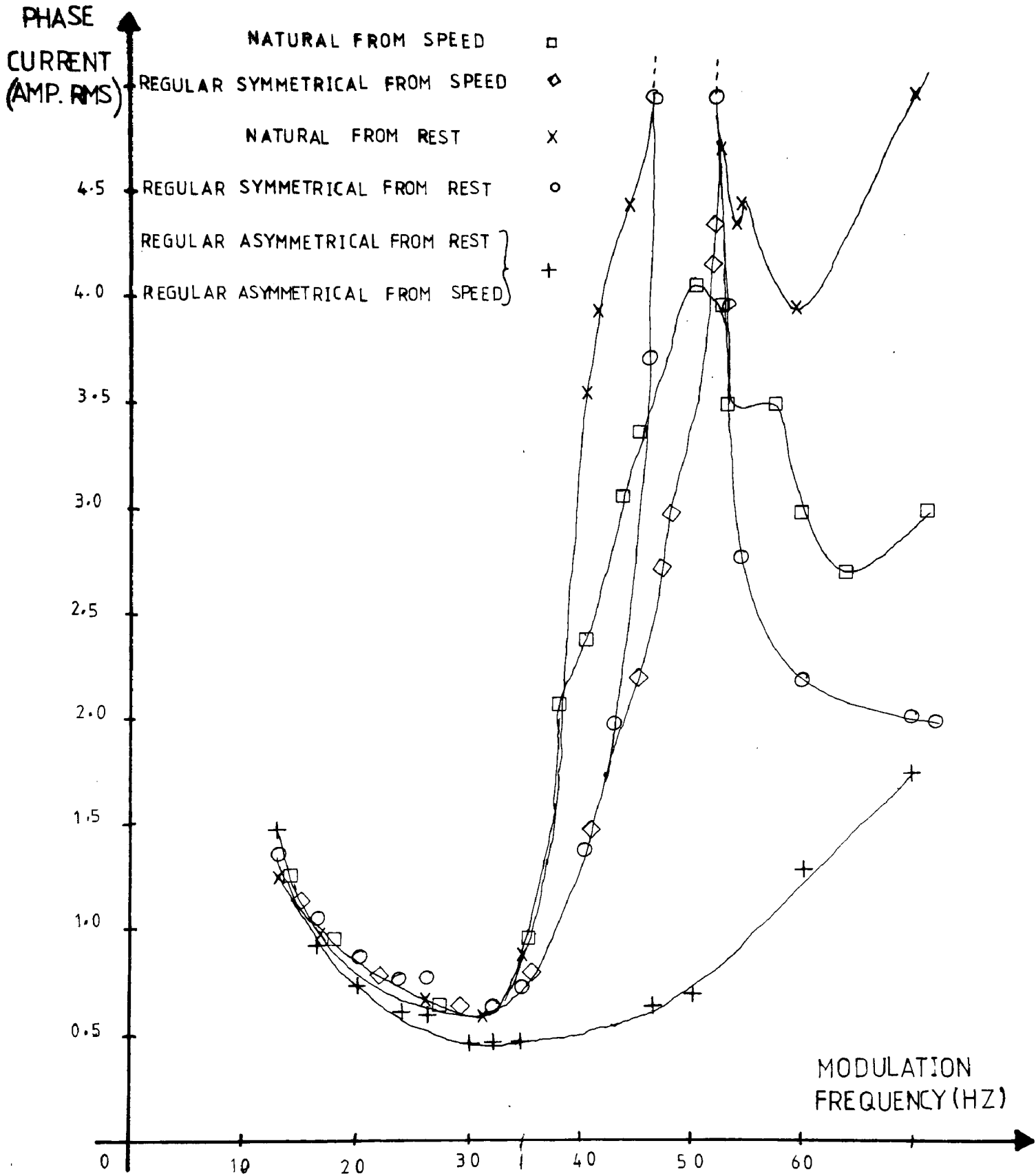FIG6-14 PWM RUN TEST-50HZ/415V MOTOR

FIG 6-13 RUN TEST — 100HZ/415V MOTOR

the stalled and cogging areas of motor operation.

6.4 Spectral Comparison

The performance of the R.S.A. PWM and the N.S.PWM differed considerably at the modulation frequency of 45Hz (the carrier being 100Hz). The spectral components of each waveform were investigated to determine whether there was some fundamental characteristic which could explain the operational differences of the PWM waveforms. The results are shown in Figure 6 - 15 for a modulation index of 66.7%. It is clear that both waveforms contain a sub-harmonic generated at 11Hz. However, the amplitude of this component is 18.6 dB greater in the N.S.PWM waveform. Thus it can be concluded that the R.S.A. technique of PWM generation inhibits the production of sub-harmonic components in the PWM output at low frequency ratios and is effective in extending the control speed range of the motor.

Figure 6 - 16, shows a more global comparison of the spectral components of the N.S.PWM and the R.S.A.PWM for the lowest triple integer frequency ratio of 3 where the modulation index varies from 0 - 90%. The graphs are broadly similar, for the most part they differ by less than 30% up to a modulation index of 0.50. Further the frequencies of all the harmonics measured are the same and no extra modulation products seem to be present, over this range, in either of the two PWM waveforms. At this frequency ratio the amplitude of the harmonic levels, although different, are of the same order - that is they do not differ by more than 10dB.

FIG 6-15 A GRAPH OF THE FREQUENCY SPECTRA OF TWO FORMS OF PWM SIGNALS

RELATIVE AMPLITUDE $(\propto V^2)$

MODULATION INDEX = 66·7%
CARRIER FREQUENCY = 100Hz
MODULATION FREQUENCY = 45Hz

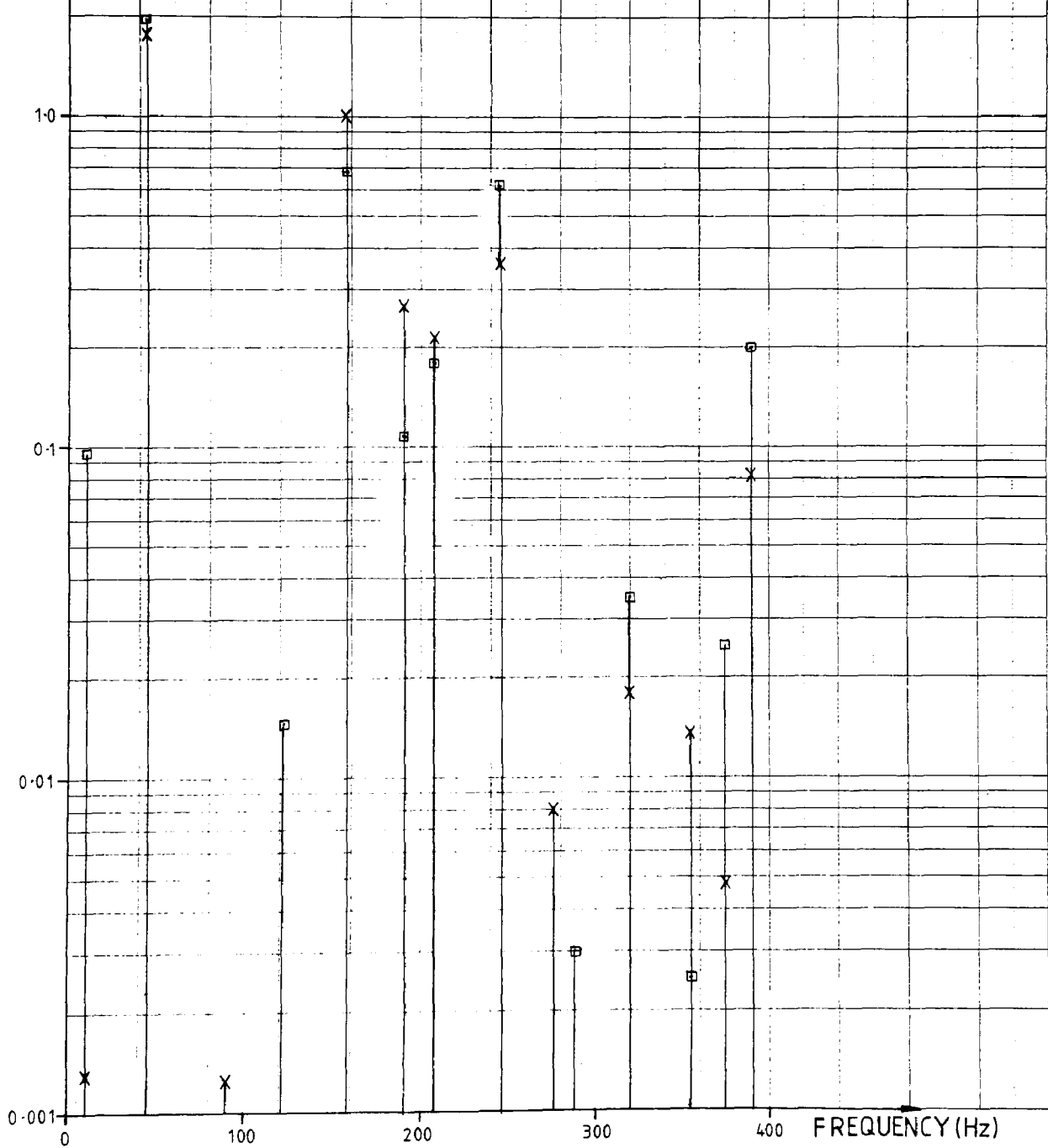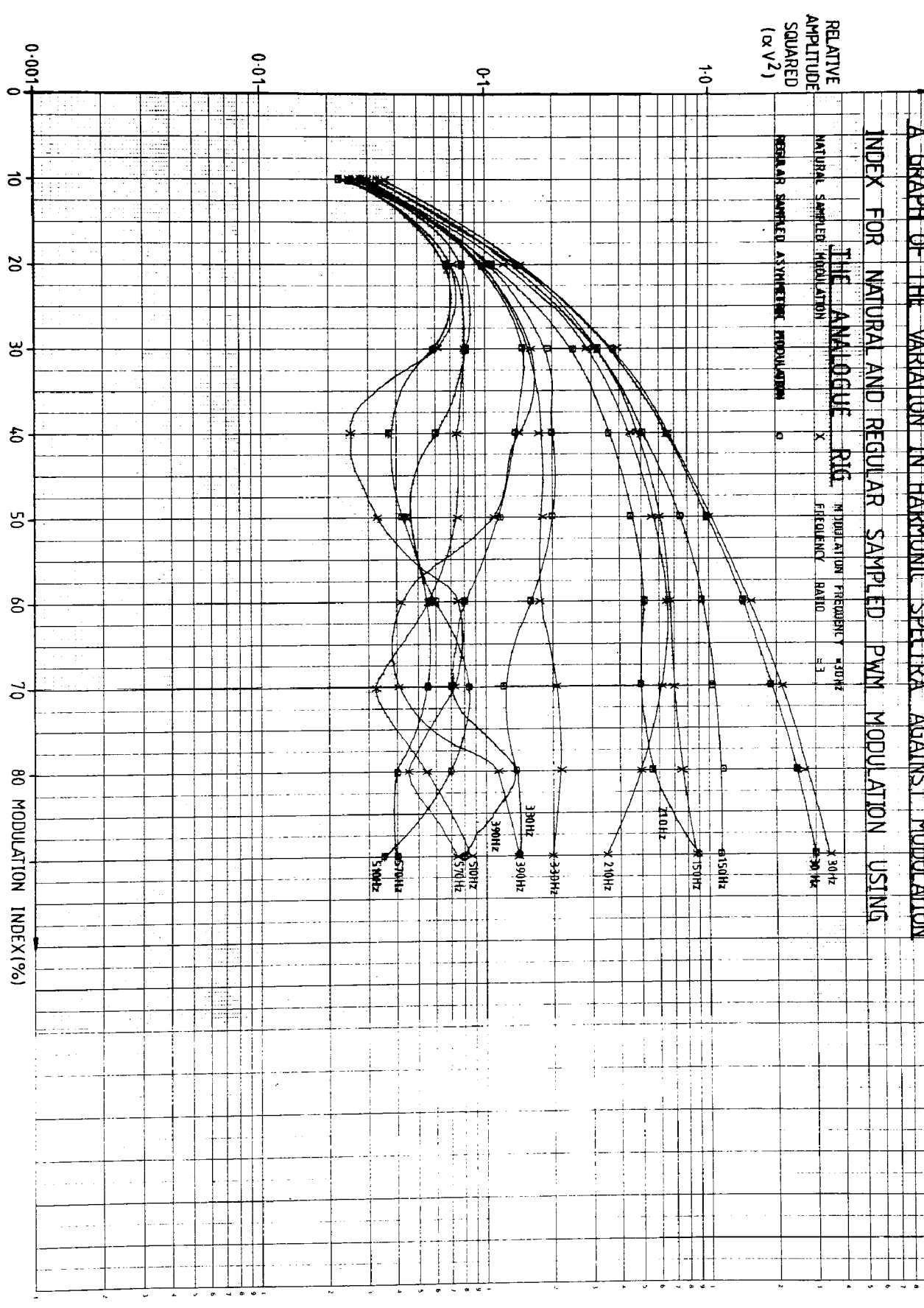REGULAR SAMPLED ASYMMETRIC PWM   X
NATURAL SAMPLED PWM

FREQUENCY (Hz)

FIG 6-16
A GRAPH OF THE VARIATION IN HARMONIC SPECTRA AGAINST MODULATION
INDEX FOR NATURAL AND REGULAR SAMPLED PWM MODULATION USING
THE ANALOGUE RIG.

Although the similarities are clear the spectra are perhaps different enough to recognise that a modified form of modulation is being used. It should be noted that as the frequency ratio, between the carrier and modulation signal, increases then the two modulation processes, the natural sampled and the Regular Sampled Asymmetric PWM, will produce waveform spectra which will become even more similar (see Figure 6 - 17 for a frequency ratio of 9) until, in the limit, the spectra will become identical. This result is different to that obtained when the frequency ratio reduces to less than 3. Large sub-harmonics, present in the NS PWM waveform are very much reduced in the R.S.A. PWM waveform which shows improved operational characteristics.

It should be noted that in the case considered (frequency ratio of 3) a fundamental power loss of 3dB appears in the R.S.A. PWM waveform when the modulation index reached 90%. Further the nearest harmonics are 2dB and 8dB larger although the higher harmonics are correspondingly larger in the N.S. PWM waveform. In practice this can produce a difference in operation in that the terminal voltage of the inverter would need to be increaed to obtain the same V/F ratio as for the natural sampled PWM waveform.

Figure 6 - 17 show a global comparison of the spectra of the N.S. PWM and R.S.A. PWM for a frequency ratio of 9. It can be seen that for the N.S. PWM the spectra seems to occur in almost identical pairs – apart from the fundamental frequency which is 10Hz in this case. In the R.S.A. PWM the harmonic pairs become separated by the modulation process, the main differences between the waveforms becoming more distinct as the modulation index is increased. At these levels of
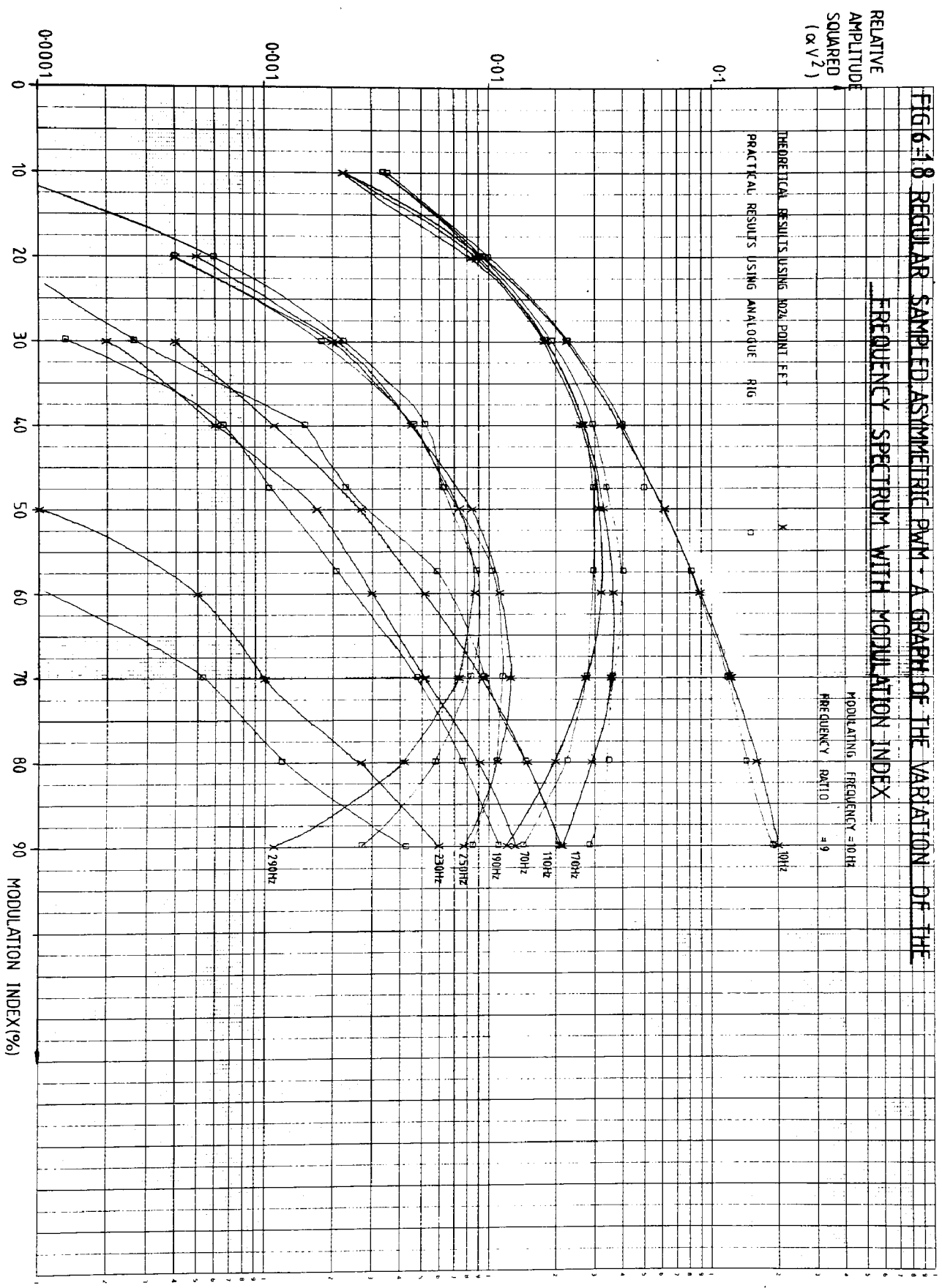
FIG 6-17 A GRAPH OF THE VARIATION OF HARMONIC SPETRA OF THE NATURAL AND REGULAR SAMPLED ASYMMETRIC PWM WAVEFORMS WITH THE MODULATION INDEX
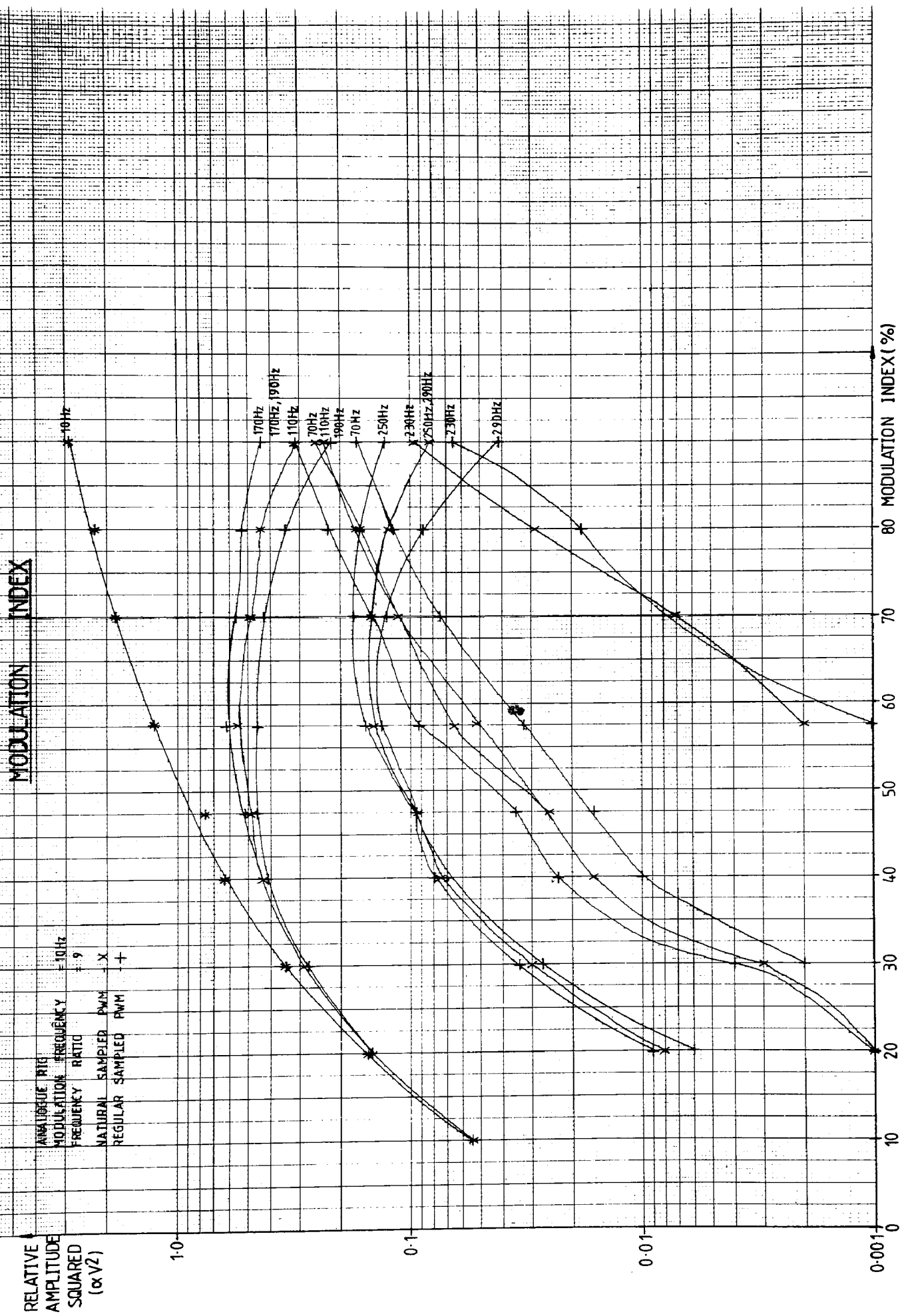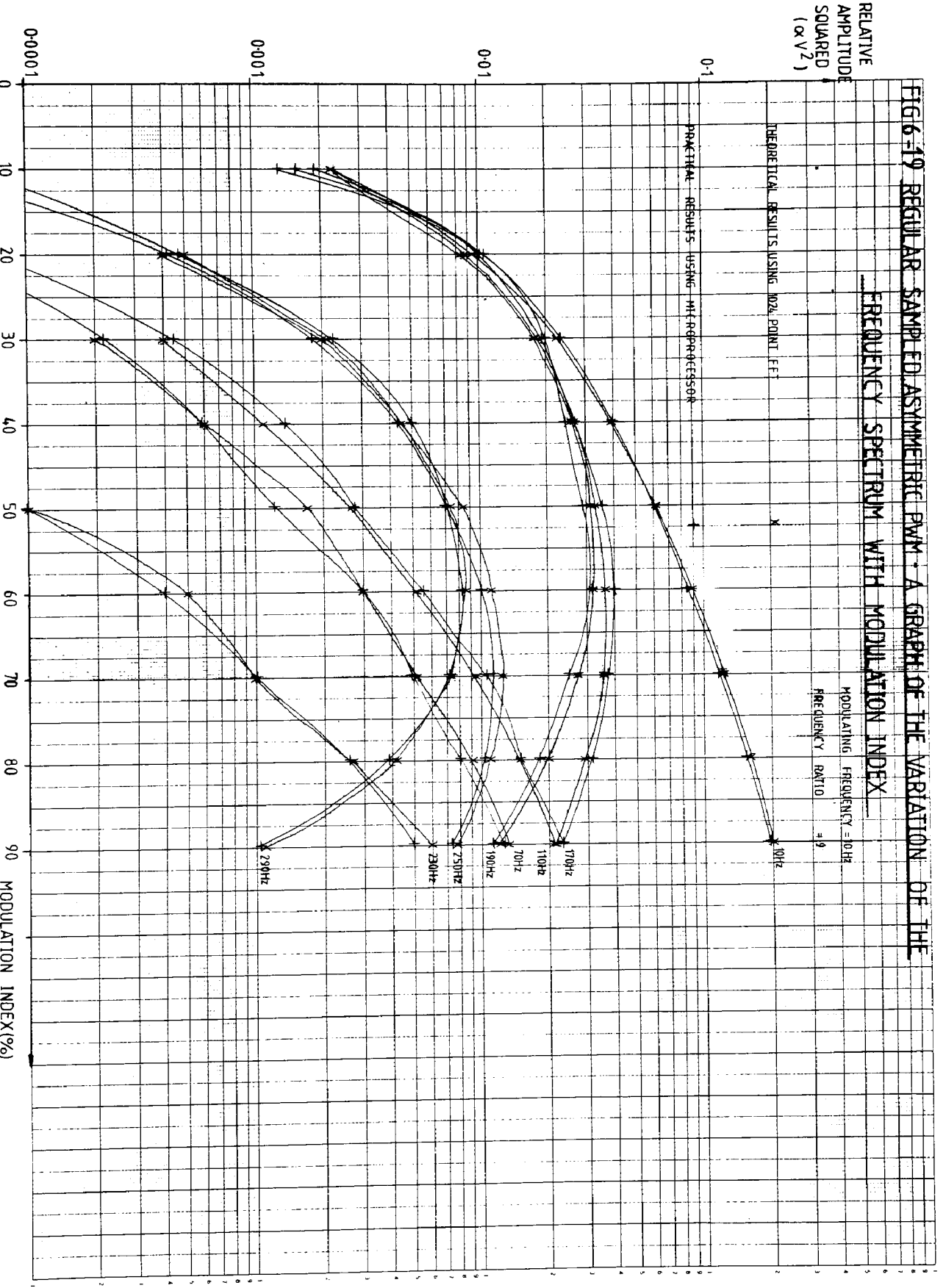
frequency ratio the differences between the harmonic spectra appear to have little effect on the operational performance of either PWM waveform.

6.5 Microprocessor Regular Sampled Asymmetric PWM Emulation

Figures 6 - 18 and 6 - 19 show the spectral comparison of R.S.A. PWM waveforms as predicted by the FFT program and as measured by a spectrum analyser. The predicted and measured results for a frequency ratio of 9, are almost identical and show that the PWM waveform obtained from the microprocessor is in fact that required - that is the R.S.A. PWM. A more global spectral comparison is given in Figures 6 - 22, 6 - 23 which provide the final conclusive evidence that this modulation process as executed by the microprocessor is in fact that as theoretically predicted by the FFT program, that it is much more accurate than the analogue R.S.A. PWM, which is also fairly close to the theoretical Figure 6 - 18. It is clear that at all modulation index values, the microprocessor equipment is producing a more accurate model of the R.S.A. PWM waveforms than that obtained with the analogue equipment. There could be several reasons for the inaccuracies present in the analogue generated PWM waveform. It was noted during measurement checks on the equipment that leakage current in the sample and hold network were causing a significant droop in the sampled voltage stored on the capacitors. This was improved by the use of high inpedance operational amplifiers but some droop still remained. Further no provision had been made for the compensation of DC offset voltages which would affect the resulting PWM waveform produced by the comparator. Another source of error is produced by

FIG 6-18 REGULAR SAMPLED ASYMMETRIC PWM - A GRAPH OF THE VARIATION OF THE
FREQUENCY SPECTRUM WITH MODULATION INDEX

- 226 -

FIG 6-19 REGULAR SAMPLED ASYMMETRIC PWM : A GRAPH OF THE VARIATION OF THE FREQUENCY SPECTRUM WITH MODULATION INDEX

FIG 6-22 A GRAPH OF THE PWM OUTPUT FREQUENCY AGAINST THE INDUCTION MOTOR SPEED
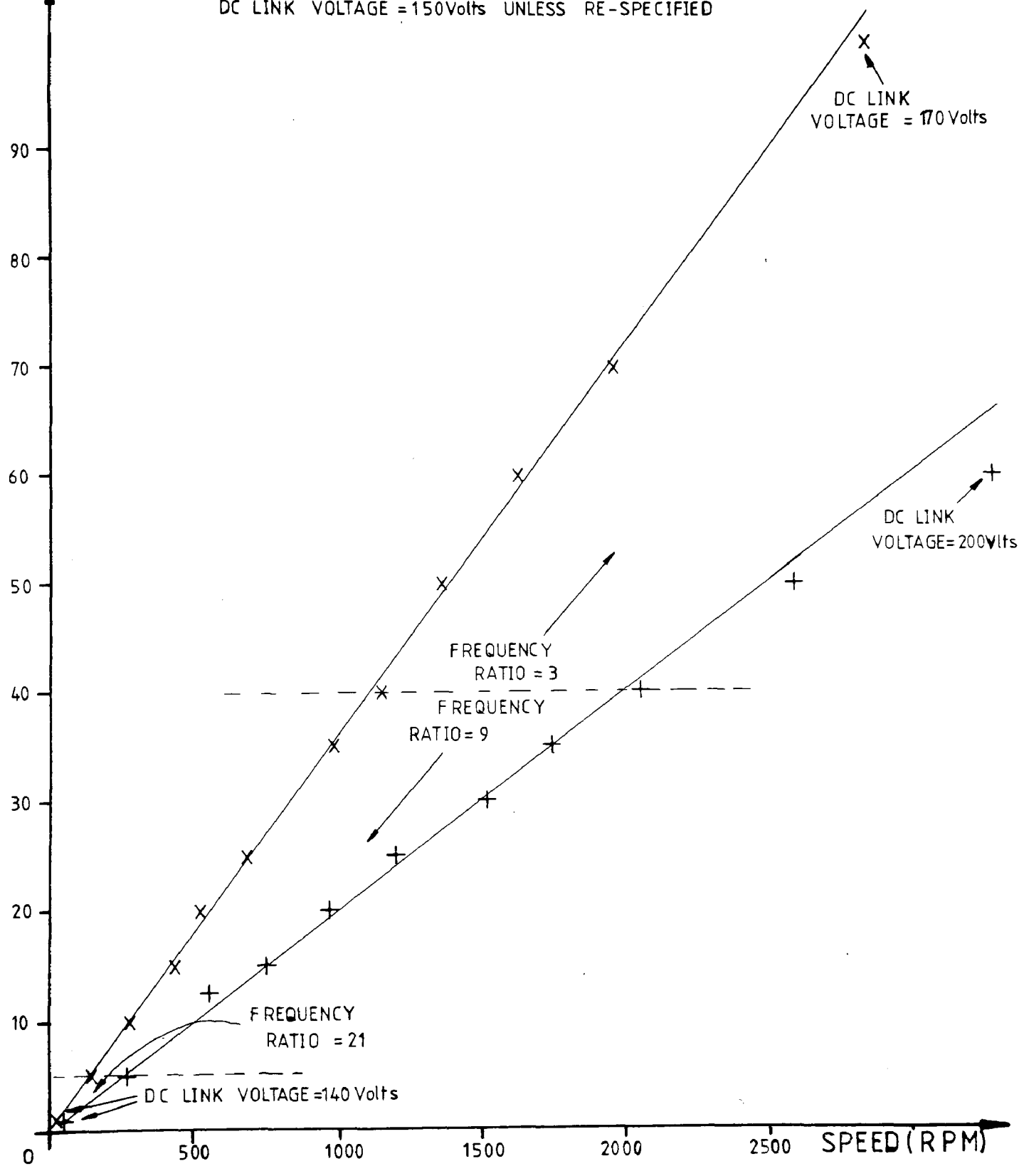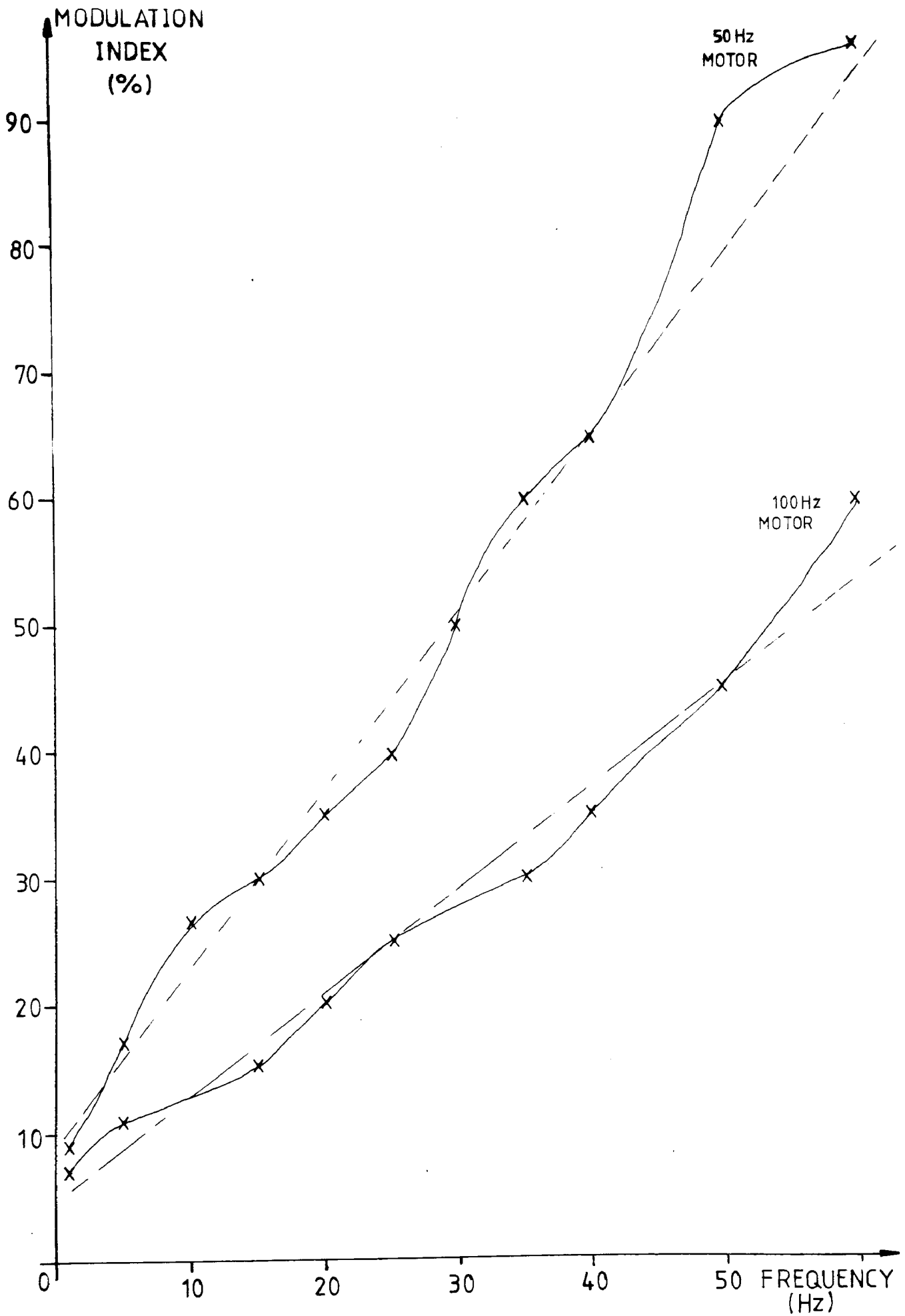
FIG-6-23.A GRAPH OF STARTING MODULATION INDEX
AGAINST FREQUENCY

the switching signal breakthrough from the MOSFET to the capacitor in the sample and hold network. This could be improved by designing a discrete sample and hold unit with capacitive feedthrough to compensate for the switching breakthrough. Another source of error, which was reduced by the use of a feedback resistor, was the presence of jitter in the output waveform from the comparators. This occurred at the switching points where noise and transient oscillations affected the sharpness of the switching pulse waveshape.

Further investigations into the operational performance of the microprocessor were completed. Figure 6 - 20 is a graph which shows the variation in the amplitude of the fundamental signal (for a fixed modulation index) as the pulse number is varied and for frequencies ranging from 1Hz to 100Hz. It is noticeable that at the higher frequencies the circuit malfunctions if high pulse numbers are demanded. That is, at 100Hz frequency ratios of 3 - 12 can be supported, however, ratios greater than this produce random results and the 3 - phase PWM output is not obtained. At the lower frequency of 50Hz frequency ratios up to 24 can be obtained whilst at 10Hz and 1Hz the full range of frequency ratios, up to 24, can be achieved.

It was noted that a single point error occurs in the 3 phase PWM output at the specific modulation index of 90% and a frequency ratio of 9. A 50% fall in amplitude was obtained. When either the modulation index or amplitude level or both were changed the error disappeared. On further investigation it was found that all of the three PWM waveforms were present and correct apart from the fact that one of the phases, although correct in waveshape, was incorrect in its phasing. This indicates that either the fault is occurring in the

FIG 6-20

RELATIVE POWER CHANGE (%)

MODULATION INDEX = 85%

1Hz,10Hz,50Hz,100Hz

1Hz,10Hz

FREQUENCY RATIO

100Hz

X RANDOM RESULTS

50Hz

FIG 6-21

RELATIVE FREQUENCY CHANGE (%)

MODULATION INDEX = 85%

1Hz

FREQUENCY RATIO

10Hz

100Hz

50Hz
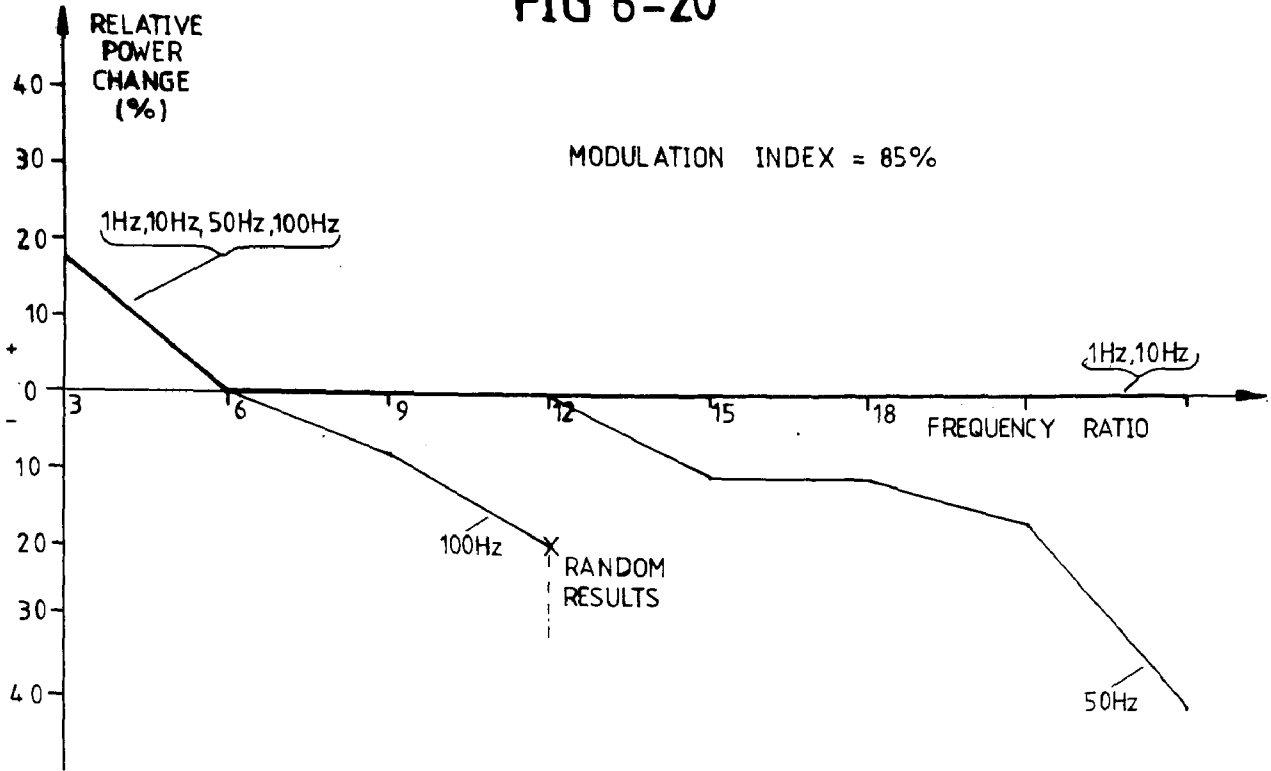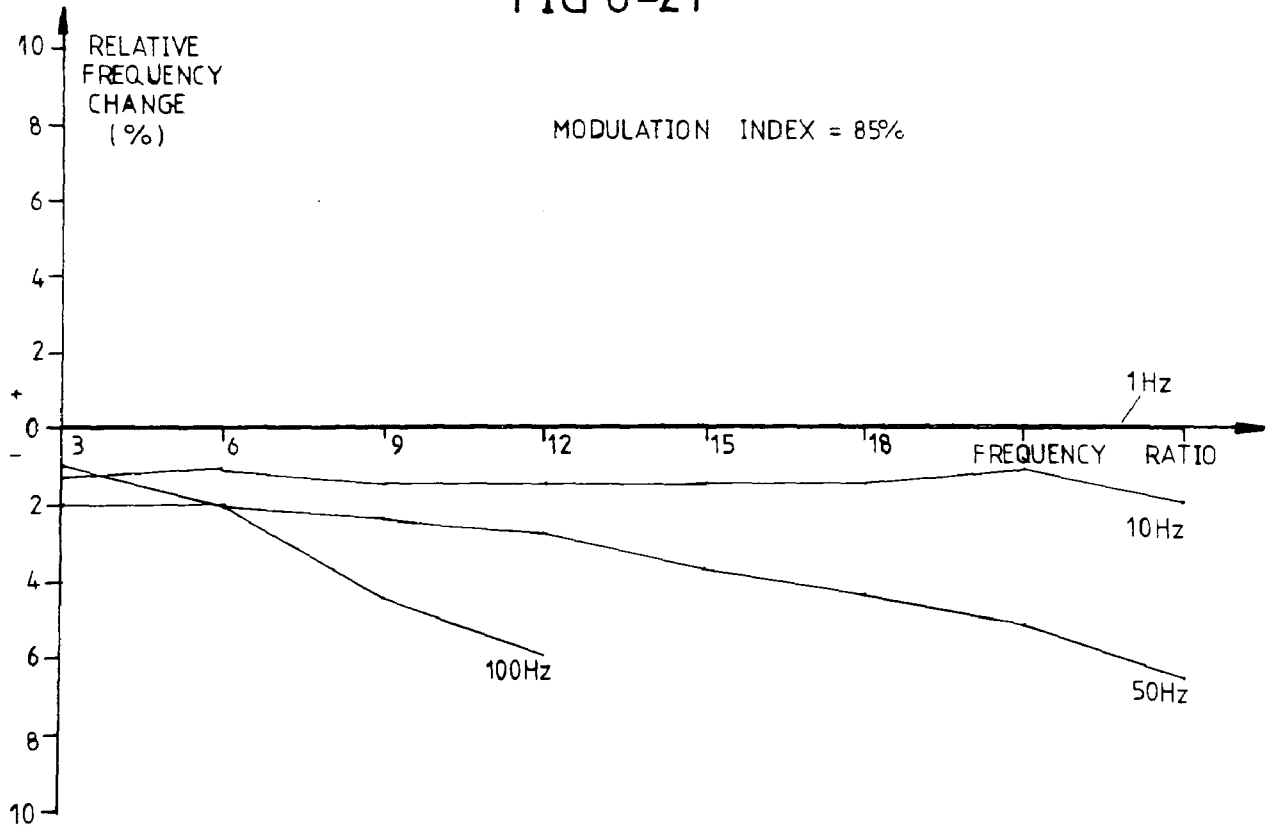
GRAPHS OF THE VARIATION IN POWER AND FREQUENCY AGAINST FREQUENCY RATIO

phase shift routine or that at the initial start up the pulse sequencing fails due to the fact that minimum pulse restrictions have not been placed in the computer program. That is, pulse widths of unity value (equivalent to a 10μs step) may be placed in the pulse length storage table. On start up the other two phases may demand servicing thus causing an extra delay of a magnitude of several hundred microseconds. The latter explanation could not account for such a large phase shift (of the order of 300ms) and it is more likely that an interference pulse is generated which resets the timer gate causing a delay in its start-up time. This particular fault may require further investigation if it recurs at other levels; at this level of modulation index for the operating frequency of 1Hz the fault can be ignored since the motor will never be operated at this level. This is due to the fact that the V/F ratio would be significantly exceeded causing saturation of the iron core resulting in the flow of large currents which would then fuse the inverter. At low frequency ratios an amplitude error of approximately 10% occurs and this is a fundamental property of R.S.A. PWM. This could only be overcome by the use of a different modulation process or the use of a 10% decrease in the terminal voltage of the invertor. At the frequency ratio of 6 and above the amplitude variation is small (less than 1% for 1Hz and 10Hz) except for the higher frequencies of 50Hz and 100Hz which remain within 25%. The reduction in amplitude produced at the higher modulating frequencies and higher pulse ratios is caused by the extra delays introduced into the waveform as a result of the inherent delay introduced into each pulse by the timer and the extra delays caused by the 100μs interrupt routine (that is where the minimum pulse width to be counted is less than 100μs). It is perhaps fortunate that in

operating the motor over a range from 1Hz to 100Hz the frequency ratios necessary for operation varied from 21 at 1Hz to 3 at 100Hz so that the timer was operated well within the limits of its capabilities.

Figure 6 - 21 gives an indication of the percentage change in fundamental frequency as a function of frequency demand and frequency ratio. It can be seen that the fundamental frequency of operation remains well within 1% for the 1Hz waveform rising to about 1% for the 10Hz waveform whereas the maximum deviations for the 50Hz and 100Hz waveforms do not exceed 6%. Again this error can be attributed to the inherent delays of the timer and the pulse lengthening caused by the delay introduced by the interrupt routine.

Figure 6 - 22 shows the relationships between the fundamental frequency of the PWM waveform, as produced by the microprocessor, and the speed of the motors. It is to be noted that in order to achieve the speed range the frequency ratio was decreased from 21 at 1Hz through 9 at 10Hz to 3 at 40Hz. Further, for each speed the modulation index was increased until the motor developed enough torque to reach its proper operating speed. At the extremeties of the control speed range it was necessary to modify the terminal voltage of the inverter and at the lowest frequency of operation of the 50Hz motor the voltage was reduced from 150 to 140 volts, whereas, at the highest frequency of 60Hz, the voltage was increased to 200volts. For the case of the 100Hz motor the voltage was reduced to 140 volts at 1Hz and increased to 170 volts at the operating frequency of 100Hz. Both frequency/speed relationships were substantially linear over the whole of the operating range of the motor.

During the speed test run for the motor, it was noticed that in order to run up the motor from rest, at each increment in frequency (or speed), the modulation index had to be raised in order that the motor may achieve its appropriate speed level (otherwise cogging, crawling torques and sub-speed running was obtained in some cases). If it is assumed that the starting torque required at each new speed is essentially the same then the necessary starting V/F ratio should remain substantially constant. That is, there should be a linear relationship between the modulation index and the frequency demand assuming that :

1. a linear relationship between the Modulation Index and the fundamental voltage output, which has already been demonstrated, and

2. there is a direct relationship between frequency demand and the frequency of the PWM output as supported by previous results.

The graphs shown in Figure 6 - 23 support the premise that the V/F ratio does remain substantially constant. More accurate results could have been achieved by setting a constant motor torque on the motor shaft and increasing the modulation index in unity steps to the point where the motor just achieves its operating speed.

Figures 6 - 24, 6 - 25, 6 - 26 show graphs of the comparison of the theoretical PWM waveform phase current spectra and the waveform spectra, as measured when the motor is running at its synchronous speed, for operating frequencies of, 10Hz, 50Hz and 100Hz. The results show clearly that when the inverter voltage source is

FIG 6-24. A GRAPH COMPARING THE THEORETICAL FFT PHASE CURRENT SPECTRUM WITH THAT MEASURED AT THE INVERTER OUTPUT WHEN RUNNING THE 100Hz MOTOR

SPEED OF MOTOR = 850 RPM
TERMINAL VOLTAGE = 150 VOLTS
FREQUENCY RATIO = 9
MODULATION INDEX = 30
MODULATION FREQ'Y = 10Hz

RELATIVE POWER (∝ I²)

FREQUENCY (Hz)

FIG 6-25 A GRAPH COMPARING THE THEORETICAL FFT PHASE CURRENT SPECTRUM WITH THAT AS MEASURED WHEN RUNNING THE 100Hz MOTOR ON NO LOAD

SPEED OF MOTOR = 1360RPM
TERMINAL VOLTAGE = 150 VOLTS
FREQUENCY RATIO = 3
MODULATION INDEX = 50
MODULATION FREQ = 50Hz

FFT SPECTRUM — x
MEASURED SPECTRUM — .
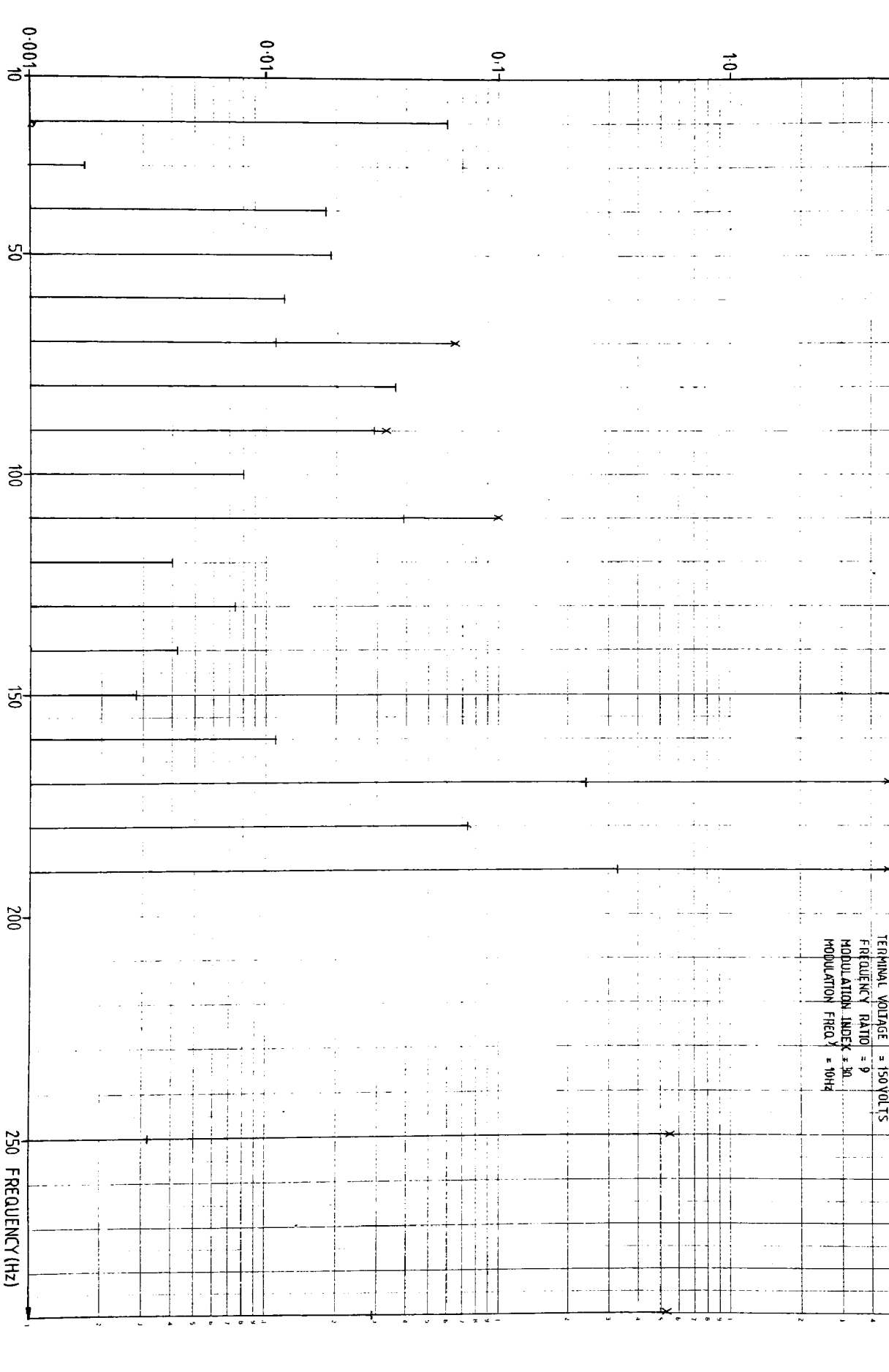
FIG 6-26 A GRAPH COMPARING THE THEORETICAL FFT PHASE CURRENT SPECTRUM WITH THAT MEASURED AT THE INVERTER OUTPUT WHEN RUNNING THE 100Hz MOTOR

SPEED OF MOTOR = 2850 RPM
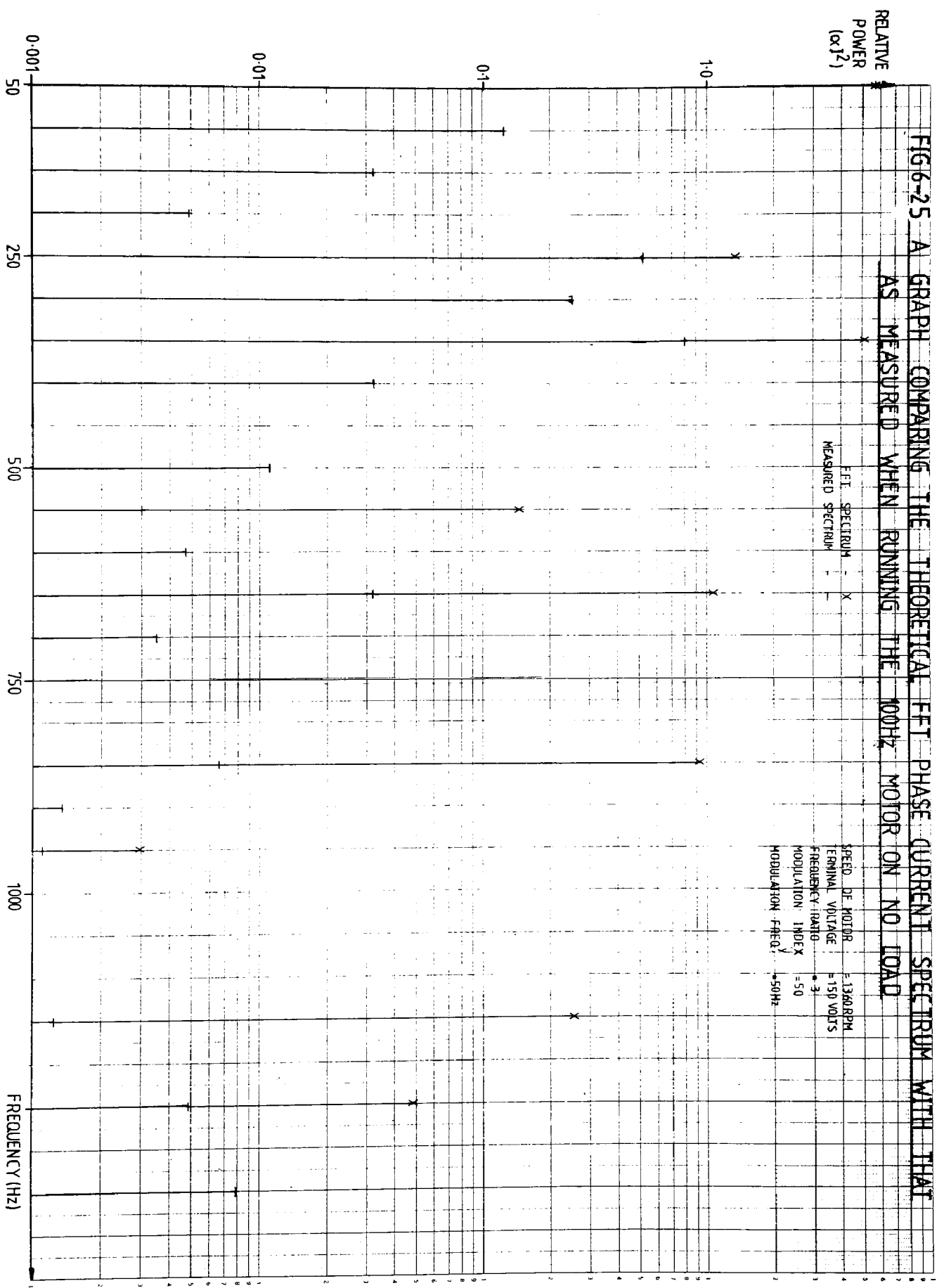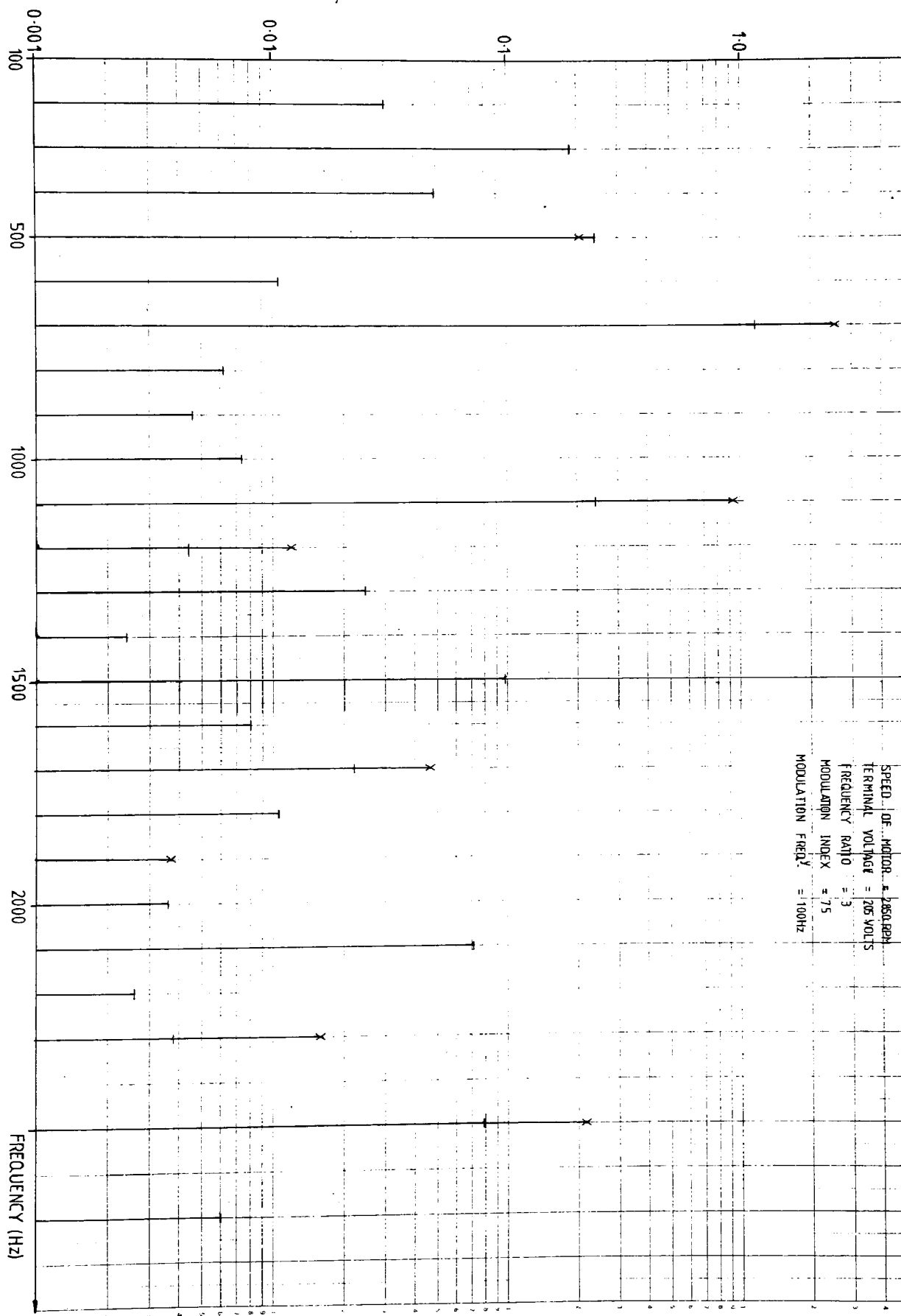TERMINAL VOLTAGE = 205 VOLTS
FREQUENCY RATIO = 3
MODULATION INDEX = 75
MODULATION FREQ = 100Hz

connected to the motor the B-H characteristic loop of the magnetic material introduces non-linearities causing the generation of even and odd harmonics. Some of the harmonics introduced are of the same order as the origianl harmonics present in the waveform. However, these harmonics were often 20dB below the fundamental frequency of the PWM waveform and did not appear to affect the operating speed of the motor.

Figures 6 - 27, 6 - 28, 6 - 29 show photographs of the phase current of the motor for operating frequencies of 1Hz, 10Hz and 100Hz. The motor current requirement at 100Hz was almost double the motor peak to peak current requirement at 10Hz and 1Hz. This can be accounted for by the extra iron losses (due to the high frequency of operation).

Figure 6 - 30 shows the VDU display of the data entry program requests of the microprocessor whilst Figure 6 - 31 shows a typical three phase PWM output from the microprocessor together with the signal waveform on the interrupt line of the M6800. These short pulses give the frequency and duration of the interrupt program since each new pulse is entered at the end of each previous pulse. Thus the short pulses on the interrupt line should be synchronised to the negative and positive edges of the three phase output PWM waveforms. The expanded photograph of Figure 6 - 32 confirms this as being the case and each pulse is synchronised to the pulse edges of the three phase output.

FIG 6-27
PHASE CURRENT
WAVEFORM AT 1Hz
MOTOR SPEED = 22 RPM
FREQUENCY RATIO = 21
TERMINAL VOLTS = 140 Vlts
MODULATION INDEX = 5%
SCALE:-
1 Amp / Cm. ; 0·1 Secs / Cm.
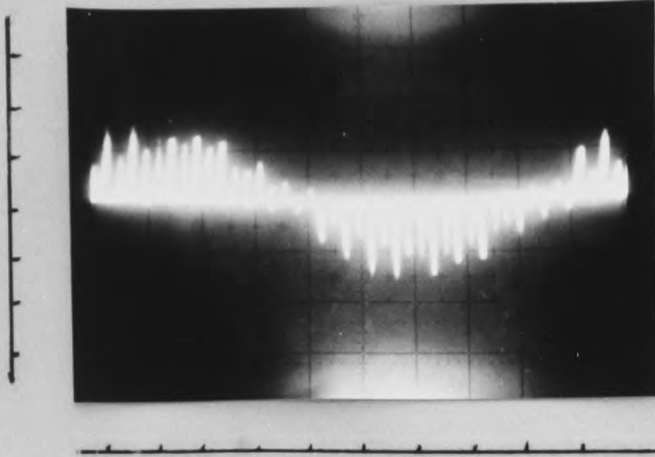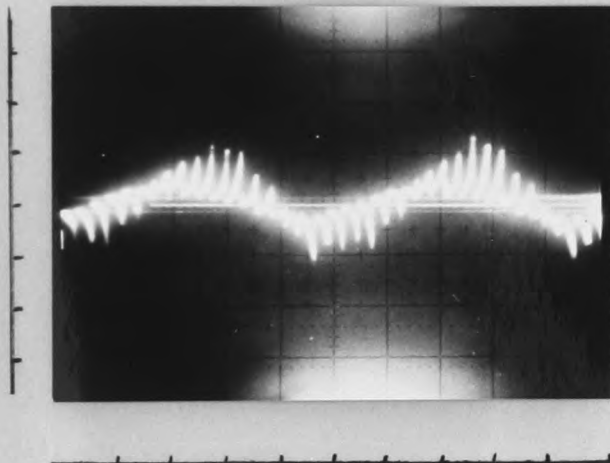

FIG 6-28
PHASE CURRENT
WAVEFORM AT 10 Hz
MOTOR SPEED = 280 RPM
FREQUENCY RATIO = 9
TERMINAL VOLTS = 150 Vlts
MODULATION INDEX = 15%
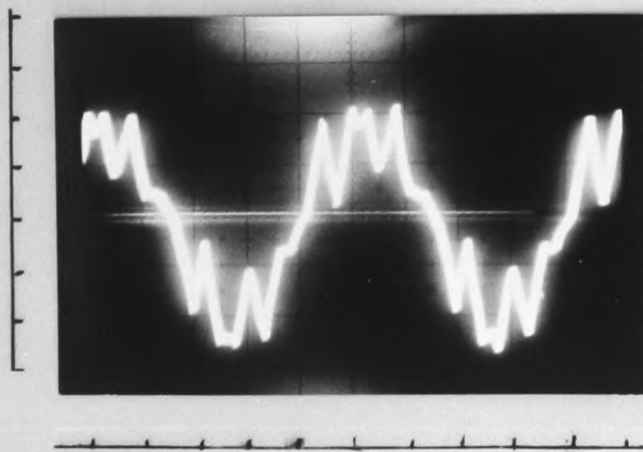SCALE:-
1 Amp/Cm ; 20 mSecs / Cm.

FIG 6-29
PHASE CURRENT
WAVEFORM AT 100 Hz
MOTOR SPEED = 2850 RPM
FREQUENCY RATIO = 3
TERMINAL VOLTS = 200 Vlts
MODULATION INDEX = 83%
SCALE:-
1 Amp/Cm ; 2 mSecs / Cm·
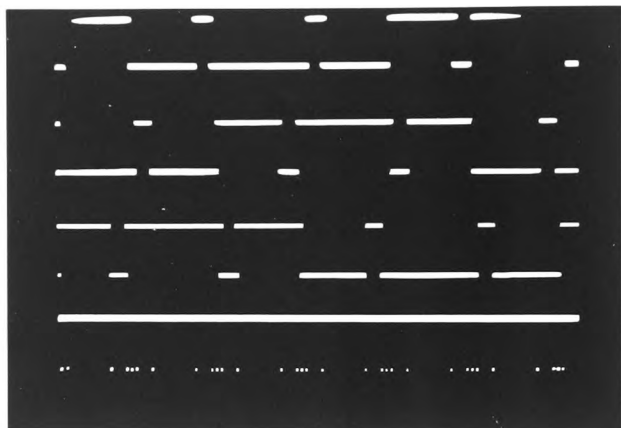
FIG 6-30

FIG6-31 5mS/Cm

FIG6-32 1mS/Cm

CHAPTER 7   CONCLUSIONS
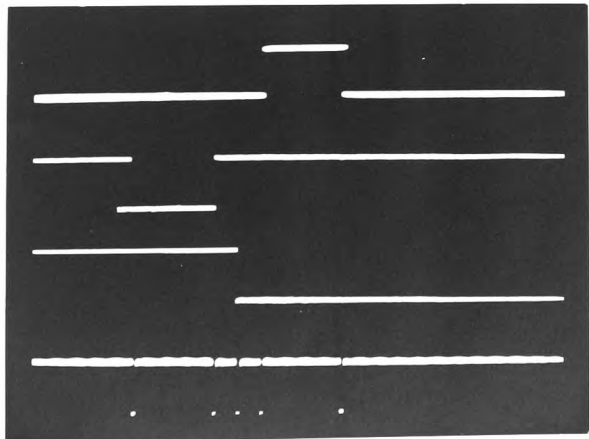
7.1   The Analogue and Digital Equipment - A Comparison

The object of this research has been to study, design, engineer and evaluate the analogue and digital approaches to the generation of PWM waveforms for the purpose of the speed control of a squirrel cage induction motor. In particular, the asynchronous regular sampled, asymmetric form of PWM generation has been considered in detail and it has been shown that at low non-integer frequency ratios (below 3), sub-harmonic frequency components, present in other PWM techiques, are substantially reduced in this approach, to the point where they do not interfere with motor operation. This property has improved the range of speed control using the analogue rig by some 40% over that of the natural sampled PWM waveform.

It was clear from measured spectrum comparisons with the theoretically calculated FFT spectra, that the accuracy of the microprocessor emulation of the synchronous, regular sampled, asymmetric PWM waveform was much greater than that of the analogue rig. Maximum errors in output spectrum amplitude of about 3% compared to maximum errors of some 60% in the microprocessor and analogue rigs respectively. Although these large errors did not appear to affect performance it does make the microprocessor rig more reliable and predictable.

In this particular implementation the microprocessor rig proved far more flexible than the analogue rig in that frequency ratios, and hence the number of pulses per half cycle, could be selected at will

to provide the optimum drive waveform for the motor. However, it is believed that the analogue rig can also be designed to incorporate this facility merely by providing an external control for the carrier frequency or by the provision of a phase locked loop, with programmable divider, so that integer ratios can be selected. Whilst the analogue rig provides smooth, continuous control of motor speed, the digital rig increases frequency in discrete steps-although these can be made small enough, so as to be negligable, whilst voltage control of the basic clock frequency of the programmable timers would provide a smoother change of speed. Amplitude control is also achieved in discrete steps - however, these can also be made small enough so that the step changes in torque can be tolerated. DC drift in analogue equipment can cause large braking torques in the motor due to the low DC impedance levels involved - a problem which is not present in the digital rig. However, it is clear from the commercial availability of the analogue rigs that problems of DC drift have been overcome. The digital rig can introduce DC offsets through the round off errors present in calculating pulse widths over the modulation cycle - these were found to be negligable. Finally, it is clear that there are many more sources of possible error in the analogue rig - the linearity of the triangular wave, distortion of the modulating wave, DC drift of the waveform generator, DC drift of the sinuisoidal generator, DC drift in DC power supplies and comparator circuits and leakage effects in the sample and hold circuitry. The only factors affecting the digital rig are the round-off error which is determined by the word size used in calculations - in this case 16 bits were found to provide the necessary accuracy - the delay in reloading the counter registers of the programmable timer and the time for which the

interrupt routine was operational.

In terms of its operating performance, in the open loop mode of control, the microprocessor realisation does not appear to offer any significant advantages over the analogue rig. What the microprocessor rig does achieve however, is to offer significant scope for the inclusion of new modulation strategies incorporating feedback control. Control algorithms can be incorporated which could hardly be realised using analogue equipment. Further, the addition of routines for self-testing, with diagnostic capabilities, would have important effects upon maintenance requirements.

With the advent of VLSI, peripheral chips such as the programmable timer, could be included in a single chip microprocessor system at low cost whilst linear circuits of increasing complexity are also becoming available in a single package for the analogue rig. At this juncture, it is considered that the microprocessor development system could be reduced to a single board controller which would meet the cost of equivalent analogue systems.

7.2   The Bridge Inverter

A rugged, reliable McMurray bridge inverter was designed with the techiques as outlined by Penkowski. This unit operated over a very wide frequency range (1Hz to 100Hz) and over a voltage range of 100 – 200 volts without malfunctioning even though it was actually designed for a constant voltage of 200 volts. The current is not controlled and is allowed to change with the variations in load. Thus, if there is a momentary short across the DC link, a large current flows, which

can cause the fuses to blow. Some inductance can be included in the DC link to limit the rate of change of current; thus momentary shorts can be ignored. One could also include an overcurrent detector which would automaticaly commutate the offending thyristor. The approach used here was to thoroughly screen signal leads whilst maintaining signal line impedances as low as possible. Although this proved adequate for research investigation, for commercial purposes, the inclusion of an active overcurrent control network is considered essential.

If the inclusion of inductance in the DC link is taken to its inevitable conclusion the development of the constant current inverter results. Short circuit conditions can be ruggedly tolerated for larger periods. However it is the voltage which is now allowed to vary and it will change according to the relationship $e = - Ldi/dt$. That is, the polarity of the voltage will swing positive and negative as the current/time gradient changes from negative to positive. Further, if the rate of change of current is fast enough, large voltage spikes will be induced around the network so that now a voltage limiting network would be required. The claims, for the current fed inverter, of ruggedness and lower distortion have been well publicised in the literature. To some extent, this must be true since (because the current is constant) any transientry shorts have little effect on the performance of the bridge. The occurence and effect of voltage variations and the size of the required inductor has not been as well documented as the effect of the constant current properties. Further, whereas a single voltage inverter can be used in multi- motor drives a separate current inverter would be required for each individual motor. It should also be noted that the current

harmonics in a voltage inverter will always be lower than those in the current inverter - for any given frequency ratio. Comments made by Brush of Loughborough indicated that the current inverter was more suited to high power pump drives where speed ranges were limited to about 2:1 and the problems of instability at high speed/low torque conditions were avoided. The use of either approach will depend on the application, however, if signal lines are properly terminated and a current limit network introduced then the voltage inverter will be free of induced transients and should prove as rugged as the current inverter.

The use of transistors and gate turn off devices, for the control of induction motors, has already been considered by other authors, certainly if their costs fall, then they will become economically competitive with thyristors. This will result in the reduction in the size of the inverters since no auxiliary commutating components will be required.

7.3   The Microprocessor Implementation

7.3.1   The Hardware

An MSI 6800 system was utilized for the realisation of the microprocessor function. An extra interface board was designed to connect to the SS50 bus which was then connected, via opto-isolators, to the pulse amplifier sections controlling the inverter. Certainly, this represents an expensive item which, with its present function, would be too costly when compared to its analogue counterpart.

However costs can be reduced by the design or purchase of a dedicated controller unit, incorporating a microprocessor. That is the serial interface unit would not be required, only 2K of memory would be necessary and further cost savings could be achieved in the design of the power unit. The final cost could be of the order of £100 which is a more economic proposition. Further if a more sophisticated control system is to be incorporated, the microprocessor device would offer a lower cost alternative to that of the equivalent analogue controller.

7.3.2. The Microprocessor

The implementation of the microprocessor system used a standard 6800 device as the main processor component. This microprocessor is widely used, is abundantly second sourced and has become a de- facto industry standard. Further, the 6800 is noted for the completeness of its arithmetic, logical and branch instructions and one of the major features of the whole of the 6800 family is the provision of unrestricted, memory mapped, dynamically programmable Input/Output.

However, both the 6801 and the 6809 device offer a significant improvement over the 6800 in terms of both memory efficiency and execution time of any coded module. The 6801 is a third generation microprocessor and offers software productivity improvements with architectural and instruction enhancements, whilst maintaining 100% object code compatibility with the 6800. The 6801 differs from the 6800 in that the A and B accumulators can be concatenated to form a single, 16 bit 'D' accumulator and a fast, unsigned hardware multiply instruction is also included. The 6801 also has 10 additional

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instructions not available to the 6800 system. Six of these instructions are arithmetic and logic instructions associated with the 'D' register whilst three of the remainder are for controlling the index register. The last instruction is a completely new one and multiplies the contents of accumulator 'A' by accumulator 'B' and places the result in 'D'.

In addition the cycle time for certain key instructions such as store, branch and index register commands, have been reduced by one half.

The 6809 also offers further scope for improvement in the system response time. it has the same multiply and concatenation of accumulators A and B together with an extra 16 bit index register and another stack pointer. Software features also include new addressing modes. It was often required, in the development of earlier programs, to offset the index register (containing an address) by a variable number held in an accumulator - this can now be achieved with the 6809 allowing the design of position independent code.

Direct interfacing with 6800 components is also possible so that the 6840 timer can be supported by the 6809. Both address and stack flexibility have been structured to support both real time efficiencies and the needs of high level language compilers, in terms of the generation of structured software which utilizes modular re-entrant programs with position independent code.

The 6809 is probably the most powerful of all 8 bit processors and is compatible with the 6800 systems at the mnemonic level. The more unique instructions include 'load effective address',

synchronization with interrupt and exchange registers, whilst the rest cover all those used in the 6801.

The three new addressing modes compromise extended, indirect, indexed indirect and long relative addressing, whilst two extra bits are introduced into the condition codes register - one is a mask for the fast interrupt request whilst the second bit indicates whether the entire processor state was stacked on an interrupt.

Basically the 6809 is an advanced processor of the 6800 family which offers greater throughput, improved byte efficiency, and the ability to handle new software methods. These include position independent code, re-entrancy, recursion, block structuring and high level language generation.

7.3.3   The Programmable Timer

This unit was a key addition to the microprocessor realisation. it allowed a large degree of freedom in the design, essential to the eventual realisation of a sophisticated control system. The ability to provide 3 parallel outputs under only interrupt control, had proved a significant advantage in allowing the design philosophy to proceed towards the incorporation of a control and monitoring system.

7.3.4   Hardware Software Trade-offs

With hindsight it is possible to pinpoint aspects of the operation of the microprocessor system that need further consideration. The phase shifting of the output waveforms was only achieved at the

expense of the design of two modules of software coding. This could be considered unwieldy for simply shifting the phase of the basic PWM waveform, whose pulse width parameters have already been defined. If this could be completed with say three or four hardware chips then this would be an advantage. Further, now that the overall system has been proved, the subroutines could be studied in order to determine whether further economies could be made in the use of the memory space. Early on in the design of the microcomputer system, the use of a priority interrupt controller was considered. This would have given faster access to interrupt routines than the polling technique utilised. Since the inverter was designed for a minimum pulse width of $100\mu s$ the polling technique was adopted since it was considered that the extra time involved, would not cause significant time delays. This decision would have to be reconsidered where time delays are to be minimised. The use of direct memory access (DMA) techniques of data handling would also prove to be useful in reducing minimum pulse width levels below $100\mu s$.

The numerical software approach (as opposed to direct software simulation of hardware items in real time PWM generation) has proved successful in the implementation of the wide range (1Hz − 100Hz) speed control of the induction motor. However it was noted that the time required to update the output PWM waveforms to a new demand was of the order of 1 second. It is considered that if the multiply routine is replaced by a hardware equivalent and other steps, already mentioned, are adopted then the update time could probably be reduced to the order of 10ms.

7.4   Microprocessor System Performance

A further malfunction was also noted after operating the equipment over a long period.   It was found that on some occasions the output waveform to the motor would change as new data was being entered into the system.   The change would be enough to cause the fuses to blow in the inverter.   After some consideration a hardware malfunction was ruled out and it was believed that a software bug existed in the input routine.   Unlike all the other routines the input routine actually jumps to software routines contained in the monitor program of the MSI 6800 system.   These routines had not been studied but it would not have been difficult to write ones own routines ensuring that no interrupts are used.

This was done and little change was observed in the malfunction previously described.   The final conclusion is that the error must occur in the CMOS logic controlling access to the PTM.   Problems, experienced early on in the design were overcome, however, it is considered that if all CMOS logic is replaced by TTL logic then the problem of PTM malfunction during the data entry phase will be solved.

Further improvements in the software could be included such as a monitor routine which maintains a specified V/F ratio;   perhaps a routine which will specifiy the frequency ratio (or pulse number) for the particular speed demanded — a modulation strategy, since it was found during testing that a frequency ratio of 21 was required at 1Hz whilst a frequency ratio of 3 was required at 100Hz.   The crossover points should be given a 'window' or overlap so as to avoid ' hunting' or oscillation at these points of discontinuity.

It was also noted that an advantage of the microprocessor system, as designed, is its inherent accuracy in timing the pulses of the PWM waveforms. This increase in performance is due to the fact that each of the 16 bit counter timer registers has associated with it, a 16 bit latch. The next numerical figure to be counted down is actually stored in the latch and this figure is automatically transferred to the counter timer registers at the instant that the figure in the registers reaches zero. There is only a small delay, therefore, in updating the registers - whereas, in other techniques an interrupt routine has first to search for the next number to be counted down - before the counter timer registers can be updated. In the technique described in Chapter 5 the interrupt routine is used to update the latch - not the counter timer registers. Although the interrupt routine does determine the length of the minimum pulse width to be about $100\mu S$ the error in timing the pulse is minimised by this approach.

Future Work
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It would be a useful addition to this research if the effect of the pulse number (i.e. the harmonic content), of the PWM waveform, upon the torque/speed characteristics of the induction motor in order to rationalise the conflicting approaches adopted in the literature where, generally, the American papers suggest that 24 pulses, per half cycle, is adequate for low frequency operation whilst Mullard uses up to 128 pulses, per half cycle, for low frequency operation. This will allow optimum efficiencies to be achieved as the number of switching transitions per half cycle determine the inverter efficiency. Optimum

triple integer ratios (of carrier to modulating frequency) have already been established in the literature and should be noted during the course of this investigation.

Research could also be directed to establish the maximum step changes in amplitude and frequency that can be tolerated by the motor drive system without causing large transients in the motor current - a step which causes less than a 10% change of full load current might be adopted as the initial criteria and the motor performance evaluated. It was noted, during system evaluation cycles, that at low frequencies (1Hz), 1% changes in voltage amplitude produced significant torque changes whilst at the higher frequencies (100Hz) 20% changes in voltage amplitude had little effect on torque.

It should be observed that it is the voltage integral over one half cycle which must be maintained proportional to the stator supply frequency so that maximum volt-time products for the individual pulses of the PWM waveform should be established for use in maintaining a constant V/F ratio. It is also suggested that the range of the digital equipment be extended to a 0.1Hz capability which may be needed for some systems. In the literature a need was noted for the operation of induction motors down to 0.5Hz. In response to this suggestion it should be noted that either very small (about 0.1%) changes in amplitude will have to be allowed by the digital rig or some method of terminal voltage control, across the inverters, will have to be included in the overall design.

It is important to note that the microprocessor approach to the realisation of a variable speed drive for an induction motor offers a new degree of freedom in the control of induction motor torque, which

was not previously available on a practical basis. It is now economically feasible to use a microprocessor to vary the relative phase-shifts between the three voltage supplies to the motor. That is, instead of maintaining the phase-shifts constant at 0°, $+120^{\circ}$ and -120°, the phase-shifts may be varied, linearly or non-linearly, from 0° to $+120^{\circ}$ and 0° to -120°. Thus the output motor torque will vary from zero (when all three voltage supplies are in phase) to a maximum when the three phases are displaced by 120°. If required the phase-shifts could be varied beyond the 120° stage, after which, the torque would again decrease. This approach offers a new technique for the 'soft' starting of induction motors and the characteristics of the drive could be determined by further research, as the speed will also be affected by the reduction in torque (assuming loaded conditions).

This change in phase-shift is achieved, in practice, by gradually changing the position of the reference phase pointers described in Chapter 5. This can be executed by the use of an interrupt routine if required.

7.5   Future Trends

Within the limitations, already described, the performance of the unit is satisfactory with a speed control range of 100:1 being achieved. It was essential to adopt a modulation strategy in order to operate over this range. That is a decrease in the frequency ratio (or pulse number) is required as the speed is increased.

The rapid change in LSI technology and pricing make it mandatory to include an estimate of future trends in any comprehensive plan for a new system design. The most significant trends at present seem to be the availability of higher speed microprocessors, lower cost high speed RAM's, more cost effective and flexible, programmable I/O devices, and modified microprocessors with direct I/O capabilities. The last two developments will have a significant impact on the architecture of small scale systems where the main objective is to design systems which have the minimum number of parts (as in this case).

This application and many others, will have a significant effect on microprocessor controlled, variable speed drive systems in the next decade. The increased complexity of individual hardware components will place a greater emphasis on software development, such that increasingly efficient software techniques, through the use of structured programming, structured design, high level languages and modular concepts, will lead to greater standardisation of combined hardware and software modules. Applications will be designed around famillies of systemized components to give reduced costs and higher reliability in meeting the functional specifications of variable speed AC drives.

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APPENDIX 1

BRIDGE PROTECTION

di/dt Protection

The maximum current rating for the thyristor was $100A/\mu S$.

$$e = -L\, di/dt$$

$$-L = e/(di/dt)$$

The terminal voltage maximum is 240 volts and $di/dt = 30A/\mu S$

$$L = 240/100 \quad x \quad 10^{-12}$$
$$= 2.4\mu H$$

In practice the inductor was wound to $10\mu H$.

dv/dt Protection

At switch on, if it is assumed that C is equivalent to a short circuit, then $i = V/R$

Now $i = C\, dV/dt$

where dV/dt = 200V/μS and V =240

$$RC = 240/200 \times 10^{-12} = 1.2 \times 10^{-12}$$

APPENDIX 2

COMMUTATING COMPONENTS CALCULATIONS

When the thyristor switches on the capacitor will discharge through the resistor and thyristor. If the resistor is 33 ohms then the peak current will be approximately 8 amps – which is reasonable.

Thus $C = 1.2/33 \times 10^{-12}$

$$= .04 \mu F$$

In practice C was set to $0.1 \mu F$ which afforded extra protection limiting the rate of rise to approximately $100V/\mu S$.

Selection of the L – C components

From [77] $C.Ed/(Io.to) = 0.9$

$to = 30 \mu S$, $I_o = 34 AMPS$ $\hat{E}d = 240 \times 1.35$ volts

$$C = 0.9 \times 34 \times 30 \times 10^{-6}/(240 \times 0.45)$$

$$= 5.1/1.8 \times 10^{-6}$$

$$= 2.88 \mu F$$

In practice a value of $C = 3 \mu F$ was used.

From [77]

$$L.Io/(\hat{E}d.to) = 0.45$$

$$L = 0.45 \times 240 \times 1.35 \times 30 \times 10^{-6}/34$$

$$= 123 \mu H$$

In practice a value of L = 100μH was used. If we consider the maximum load current Io and capacitor current Ic, then, on commutation we should have
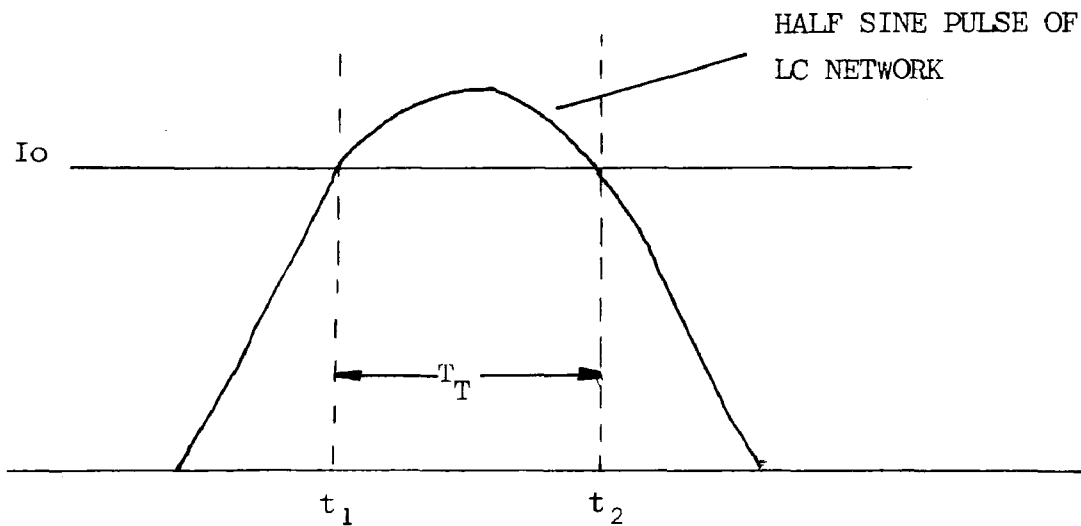
Under these conditions the thyristor will switch off at t_1 and must regain its blocking ability before t_2. For maximum load, the value of T_T should not be less than the reverse recovery time of the thyristor. For the device used this is of the order of 20μS - in practice this was assumed to be 30μS (for the purpose of calculation).

```
5 PRINT"□□"
10 INPUT"MODULATION INDEX(0-1)";M
15 INPUT"WHICH CARRIER HARMONIC,FC,(0-N)";FC
20 INPUT"WHICH MODULATION SIDEBAND,B,(0-N)";B
23 DIMF(B,F)
25 IFFC>0THENGOTO40
30 IFB<>1THENJ=0:GOTO290
35 J=M:GOTO290
40 I=INT(FC/2)
45 IFFC/2>ITHENGOTO75
47 PRINT"FREQUENCY = FC*FUND.L+(H.S.)-(L.S.)((2*B-1)*FUND.L
50 R=FC/2
55 F(B,F)=(-1)↑(B+1)*(-1)↑R*4/(R*π)
60 N=2*B-1
65 X=R*π*M
70 GOTO130
75 R=(FC+1)/2
77 PRINT"FREQUENCY = FC*FUND.L+(H.S.)-(L.S.)(2*B*FUND.L/)"
80 F(B,F)=(-1)↑B*(-1)↑(R+1)*8/(FC*π)
85 N=2*B
90 X=FC*π*M/2
130 IFABS(X)<1.E-6THENX=1.E-10
140 Y=X
150 IFN>XTHENY=N
160 N9=INT(Y+3*SQR(X)+9)
170 J9=0
180 J8=1.E-30
190 S=0
200 FORI=N9TO0STEP-1
210 J7=2*I/X*J8-J9
220 J9=J8
230 J8=J7
240 IFINT(I/2)=I/2THENS=S+2*J9
250 IFI=NTHENJ=J9
260 NEXTI
270 S=S-J9
280 J=J/S*F(B,F)
290 PRINTJ
300 END
READY.
```

```
100 REM***FAST FOURIER TRANSFORM***
110 INPUT"POWER OF 2(N=2↑L)";L
120 N=2↑L
130 DIMA(N-1),B(N-1)
140 PRINT"NUMBER OF POINTS=";N
150 REM**GENERATE PWM WAVEFORM**
160 INPUT"ENTER MODULATING FREQUENCY(1-300)HZ";F
170 INPUT"ENTER FREQUENCY RATIO(1-24)";R
180 INPUT"ENTER MODULATION INDEX(1-99)";K
190 PRINT"GENERATING WAVEFORM SAMPLES"
200 DIMTN(2*R),WT(2*R)
210 WT(1)=π/R
220 TC=1000/(F*R)
230 TN(1)=TC/2*(1+K/200*SIN(WT(1)))
240 TN(R+1)=TN(1)
250 FORI=2TOR
260 WT(I)=π*I/R
270 TN(I)=TC/2*(1+(-1)↑(I+1)*K/200*(SIN(WT(I))+SIN(WT(I-1))))
280 TN(R+I)=TN(I)
290 NEXTI
300 FORJ=2TO2*R
310 TN(J)=TN(J)+TN(J-1)
320 NEXTJ
330 J=1
340 FORI=0TON-1
350 MT=TN(2*R)*(I/(N-1))
360 IFMT>TN(J)THENGOTO470
370 IFMT=TN(J)THENGOTO450
380 A=J/2
390 B=INT(J/2)
400 IFA>BTHENGOTO430
410 B(I)=-1
420 GOTO490
430 B(I)=1
440 GOTO490
450 B(I)=0
460 GOTO490
470 J=J+1
480 GOTO360
490 PRINTB(I)
500 NEXT
510 INPUT"VOLTAGE OR CURRENT SPECTRA(VORI)█";A$
520 IFA$="V"THENGOTO730
530 Q2=INT((N-1)/3:Q3=INT((N-1)*2/3)
540 DIMC(N-1),D(N-1)
550 FORI=0TOQ2
560 C(I)=A(N-1-Q2+I)
570 NEXTI
580 FORI=Q2+1TON-1
590 C(I)=A(I-Q2-1)
600 NEXTI
610 FORI=0TOQ3
620 D(I)=A(N-1-Q3+I)
630 NEXT(I)
640 FORI=Q3+1TON-1
650 D(I)=A(I-Q3-1)
660 NEXTI                    A2 - 4
```

```
670 FORI=0TON-1
680 PRINTA(I);TAB(3);C(I);TAB(3);D(I)
690 NEXTI
700 FORI=0TON-1
710 B(I)=(2*B(I)-C(I)-D(I))/3
720 NEXTI
730 REM**NORMALISATION**
740 X=0
750 FORI=0TON-1
760 B(I)=B(I)/N
770 NEXTI
780 REM**BINARY REVERSAL**
790 PRINT"BINARY REVERSAL"
800 FORJ=1TON-1
810 FORK=1TOL
820 IFX*2↑K/N)=1THENGOTO850
830 X=X+N/(2↑K)
840 GOTO870
850 X=X-N/(2↑K)
860 NEXTK
870 A(J)=B(X)
880 NEXTJ
890 FORI=0TON-1
900 B(I)=0
910 NEXT
920 REM**FFT CALCULATION**
930 PRINT"FFT BEING CALCULATED"
940 FORI=1TOL
950 Y=2↑(L-I)
960 Z=2↑(I-1)
970 FORK=1TOY
980 FORM=1TOZ
990 X=(M-1)+(K-1)*2↑I
1000 Q=A(X)
1010 P=B(X)
1020 W=2*π*(M-1)*Y/N
1030 XX=X+Z
1040 T=A(XX)*COS(W)+B(XX)*SIN(W)
1050 S=B(XX)*COS(W)-A(XX)*SIN(W)
1060 A(X)=Q+T
1070 B(X)=P+S
1080 A(XX)=Q-T
1090 B(XX)=P-S
1100 NEXT
1110 NEXT
1120 NEXT
1130 REM**CALCULATE MAGNITUDE+PHASE**
1140 PRINT"MAGNITUDE+PHASE CALCULATION IN PROGRESS
1150 FORI=0TON/2
1160 A1=SQR(A(I)*A(I)+B(I)*B(I))
1170 IFA(I)=0THENA(I)=1.E-6
1180 A2=ATN(B(I)/A(I))*180/π
1190 PRINTI;A1;A2
1200 U=U+1
1210 IFU<=9THENGOTO1250
1220 U=0
1230 PRINT"PRESS ANY KEY TO CONTINUE"
1240 GETA$:IFA$=""THEN1240
1250 NEXTI
1260 END
READY.
```

```
  F 1 0100 0165   ECHO? Y
S11301000DF00454E544552204D4F44554C41544490F
S11301104E472046524355454E435920283_2DCE
S113012033303C293F20040A0D454E544552204FB1
S113013052455454E4359205241544940F202B68
S1130140312D32342B3F20040A0D454E544552204C3
S1130150D4F44354C41544F4E20494E44455B17
S10D0160DBAF4D0B04)CFEF44A21
  *
```

```
  F 1 0400 0273   ECHO? Y
S11302000EB8E717E7CE7C2CE0CE0EF0CE0100FL
S11302104A0C0E8D14BB1C42SF0F0RDE05B0B1EE
S11302208D46F700087A000128B6DF05E00BEF1
S11302300E8701B40022807851AEDE1D1BBC00C3TE
S11302424E1D8D047DEBB1877EB7C1B335787D21
S11302507AFE0FE0D71CBFF7DF8BDF83F3FBBB3
S11302600E001D70F28FD1BFF3FD74FB3AE0B1BB1
S11027084F0DFBD
```

```
  F 1 0300 0360   ECHO?
S11308108D0F0002477E7A0BEF0011BBT1ETBB
S11308107BB1E3B7B00BET7E7E4FA70CF7EB
S11308C0B4BD4BF6+BBB0AB0BB10ABC1ET7007ABI
S11309000D8BFF0DBBE100BF7DC1BBTBBELT
S11309108E7400ED8DEB73J4T0BB0ET7A0B7BB1E
S11809C07140D1AB33BE41
  *
```

```
  F 1 0400 0450   ECHO? Y
S11304000CE0000F08BF0EDF10B010B702DE0CE0AC
S11304100020E0ABB0CB70CB601E70DDF007D00001C
S11304202B04B60BB7C2EB00DB10C4456870CL7FB
S11304300012415B80CB0DDB11D7118B10E7108630
S11304400AD80ED80FD70FBB0EB70E0C79000D7BBB
S1110450000007B0000B79000A7A00022BC9309E3
  *
```

DIVIDE ROUTINE

```
 P 1 0500 0559  ECHO? Y
S11305008B78970055140613 7F00157F00167F0017
S1130510177A00005B4924F9465667144D713961AA7
S11305200519005911425000113250E0CD013921450
S11305300D20010C7900157E00167B00177C000054
S11305402B0B78001B5B4825E220D700594825068A
S10B0550D013E21425037C00153E22
*
```


ADD/SUBTRACT ROUTINE

```
 P 1 0600 062D  ECHO? Y
S113060088015B827140C963283537383B8B018189
S11306103467376830663397383B0C8329035870D
S11306208BB31B2146737B330B2337383B44
*
```


16 BIT FORMAT ROUTINE

```
 P 1 0700 07DD  ECHO? Y
S113070088178714BB18E71BB13B71BBB48744
S11307113BBB0B714B0B4B8B0B7B0B7336180C
S11307128B7B11BB07327CD71BB0187006BB07L
S11307308B71BB1941BB1871ABB1B71BB1AB772
S11307418BB13B714BB7BB713B1B5008318730405
S113075088DB8B73BB1157LABB0B71BBB0BB71BBB
S113076BB1187L4BBB4713B1C500B1BB7100BDB
S113077L8D71BB01B713BBBB71B70418BB1F4B
S1130781BB1C071B1B1B71BBB178714BB101L
S11307908B1BBB10B01BB11B73BBDLB00B73B73L34
S1130711BBBBB73283005730B73BBB1BB74B137B
S113078B8738B501B73BB00B00BB37B60FBBBB101
S10B07D100L41BBB0B73B3B5D
*
```


SIN ROUTINE

```
 P 1 0800 08AF  ECHO? Y
S11308000E00000DF22DF24DEB000E6282604DF22DD
S11308102006817F1B05DF247E0BAFCE0B6BDF2CDF
S11308200E403ADF25FD721DE22DF3ADE24DF2BE5
S11308300E0020D3A0B0EBD3B4C9720A600E6018C
S11308407D00202E157D00266D317D00202E0FE7AB
S113085001A700B087A00202E2DE2C20E7E72272
S11308603727030EDF2CD6215CC10F274220B7E67C
S113087021270767066084A20F73B2E0A7D00200B
S113088027AE007A206B7D00202F6EB07A60610
S113089039400250B13F60A2205160280014B00C8
S11308A0A30051002E0014000A00050002000139C8
*
```

PRIMARY 3Ø SORT ROUTINE

P 1 0900 09E0   ECHO? Y
S1130E004F975ADE55973097319732405739CE0F2E
S1130E10FE0E08860057336005734AE0197352BDD4
S1130E20060085369730863797315E3887325A267E
S1130E30E0780038790037790036963887194863770
S1130E40E718EE3E97184F971486038719E8D050087
S1130E50E801E757FE1000DF64CE1000DF58EE160C
S1130E60DE15050500CE0E7C005AE001A20024F5FE
S1130E70DF52DF5EEB01AE0097E2D7639E5A975DE0
S1130EE0AE00E5C1D0E38262E760D7318303975600
S1040EE03E2E
*

SECONDARY SORT ROUTINE

P 1 0A00 0A7E   ECHO? Y
S1130A007F0000E86381572727700857700057C80
S1130A1000E8E7C001E802E1002718DE8E8A8008731
S1130A2068AE11873E8538157260E7A0056E0004E8
S1130A30DEE40F64770000E6585154262108568856
S1130A40001738E8C1D7E7E558A81012736740057EA
S1130A507A0115D7A013C1E86C4FDD75E20087C0005
S1130A6058A7D1150710057C00001802E100271EEE
S1130A70E8580117E6E011D7E7E5538154626018
S1130A80E16E1BE4FDE7E67F00CE8E0E1012810E8EA
S1130A90DE81D7E88117C1E85338100273070E1
S1130AA0DE8E184F57E87F00068310010E10DF
S1130AB07A0117A115F70085770006E328000C
S1130AC0E07E8000E88E01785820010EE
S1040AD0E8E148138E786574

DATA OUTPUT ROUTINE

P 1 0E00 0E58   ECHO? Y
S1130E000F88028458468E858E401270785157A0E3
S1130E101820158308E7A013DE84FFA0020E80FF78
S1130E20A004DE82FFA00640408B7A018D138AFFA04A
S1130E3002DE88FFA004DE88FFA00E0E58DF88DE88
S1130E40158DF88DE8ADF8ADE80DF80DE8E0FEE865D
S10A0E50335783CE7EE0E8DE
*

CONTROL PROGRAM ROUTINE

    P 1 0C00 0D11   ECHO? Y
S1130C0016DF36DF16CB2BDF128F3FDBD2AB9FCB4S
S1130C1017EA76ED129F168B2ECB66C2F7CA9A6BE3
S1130C20F7B79BCB1ECB368B1ECF1A8F16CBBEEFFE
S1130C303FEAB2CB26CF76CB17CF16CA22CB6ACAED
S1130C40C154D100A51DC830CCC1EC1CE120C0109B
S1130C500DB5CE10B53CCC14CE2BB500C034A9143E
S1130C6040 14E034E5145B34CB3DCC34E534CD3472
S1130C70B100DD34E13449B0B514E.70B534CB3C2B
S1130C80GBE34AAA2ACB3ACFD7CB7C732CB4FCB5B
S1130C90E3FF7FDB76EEEFBFBECB578B2ECB77CB04
S1130CA037BB9BCF3BCBEAEF1ACF3BDB37BB3BCEB4
S1130CB0B6GCBEB5B33CEA6DB76CB17CF77CFFECA77
S1130CC049B45D73453348B34D174FB347B14C1BDC1
S1130CD0E434E17DA914CBA7B9B5C43061BCAB313B
S1130CE0DCBEQB070E434CB35E9E4DB35D51BCB3DB3
S1130CF0A1B5AB3CBB74B13CCCC2DBD300D75C434 17
S1130D00BBCB72CB3BCB33CB1ABFCBEB1BCB3ACB9F
S1050D0L05ED4A5
→

INTERRUPT ROUTINE

    P 1 0E00 0F17   ECHO? Y
S1130E0089DB74A.CFB763DBEB4500EB3DB7B.DBB3
S1130E1CF7A0D39BBBEB112712BBB3BCB72B.B7A3D
S1130E2D0CBB201F7C0DB7EBEBEB0BB7BB2114B3B0
S1130E3CB7B1C12BCB7C1DBB3D0CB7A0DB7BFBBBCB1
S1130E4D0BB7EB3BB6CB4AC.1274BDBBBABCCBB0B
S1130E500187A0CCF7A013BBBEBBD2271BBBCBCD1A
S1130E61BADB0BBB1BBCC187BBDC22TCC0BABBBD1A
S1130E71BB12B7B0DC(17BB9A610123DBBBBBB1B1F
S1130EBCB7BBCB0BT0C1BBEBBCB0CCB7BCBBBBDCBB
S1130EBC1BABC1B274CDBBBABCCBBC1B7400B77CBA3
S1130EA1C7BBBBBD.42T1BB1BCBCBBBCB3BBBBBCB3
S1130EB0CKBTBBB0CCB7CCBDBB6FBB0CB7BFB1.7BG
S1130EC1BBBBCCC1BB1BBBBBBBC4ETBB000B7A0DB.
S1130ED018DBBBFBD0BBTBFBBBC

INITIALISE TIMER MODULE

    P 1 0F00 0F14   ECHO? Y
S1130F00CEA000BB0BB7A01BB3D0A701A7CC4DAT0B
S1030F10014A4701BF07
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