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Grounded capacitor-based new floating inductor simulators and a stability test

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Abstract: In this paper, two new floating inductor simulators (FISs), both using two differential difference current conveyors, are considered. The proposed FISs do not suffer from passive component matching constraints and employ a minimum number of passive elements. They use a grounded capacitor; accordingly, they are suitable for integrated circuit technology. They have good low- and high-frequency performances. Simulations are performed with the SPICE program to verify the claimed theory. Moreover, for the first FIS used in a second-order low-pass filter, a stability test is performed as an example.

Key words: Floating inductor simulator, differential difference current conveyor, stability test

1. Introduction

The use of current-mode active devices has some potential advantages over their voltage-mode counterparts such as operational amplifiers (OAs) [1]. These advantages are wider bandwidth, higher linearity, greater dynamic range, freedom from slew-rate limitations, freedom from trade-off between speed and bandwidth, usage of less number of active devices, etc. [1].

Floating inductor simulators (FISs) [2–28] are basic building blocks for analog signal processing systems because implementing spiral inductors in integrated circuit (IC) technology is still difficult due to some of their drawbacks, such as large silicon area, high cost, lack of electronic tunability, and low quality factor. A single active device is used in [2–4], whereas their internal structures are complex. The devices in [3–16] are made up of only grounded passive components, but only [14] has the property of improved low-frequency performance. Furthermore, [2], [17], [20], [24], and [26] do not have the property of improved low-frequency performances. The devices in [10] and [16–18] require critical passive component matching condition(s). The ones in [18], [19], and [25] use a floating capacitor, while [18] and [23] employ two capacitors. The devices in [14] and [21–23] cannot be operated at higher frequencies because they have capacitor(s) connected in series to the X terminal of the active device(s). The devices in [9–12], [15–17], [21], [23], and [24] are composed of more than two active devices. Finally, the devices in [25] and [28] consist of OAs and [5] and [6] include operational transconductance amplifiers, which have limited high-frequency performances.

A differential difference current conveyor (DDCC) has the advantages of a second-generation current conveyor and a differential difference amplifier, which possesses high input impedances and arithmetic operation

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capability [29]. On the other hand, a grounded capacitor, when compared to a floating one, is simpler to implement in IC fabrication. Furthermore, the floating capacitor has substantial parasitic capacitances [30].

In this study, two new FIS circuits are proposed. Both FISs have the properties of improved low-frequency performances because they do not suffer from Z terminal parasitic resistors [27]. Both are composed of two DDCCs as active components and a minimum number of passive components. Both proposed FIS circuits are devoid of component matching constraints and use a grounded capacitor, which makes them suitable for IC process [31]. Electronically tunable FISs can be easily obtained by replacing only the current-controlled DDCC [32] instead of both DDCCs of the proposed FISs and removing both resistors. Computer simulation results using the SPICE program are compared with ideal ones for confirmation. Furthermore, a stability test for the first FIS used in a second-order low-pass filter example is performed as an example.

2. Suggested circuits

Using standard notation, a six-terminal DDCC whose electrical symbol is shown in Figure 1 can be characterized by the following matrix equation:

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ I_{z+} \\ I_{z-} \\ V_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ -\gamma & 0 & 0 & 0 \\ 0 & \beta_{1k} & -\beta_{2k} & \beta_{3k} \end{bmatrix} \begin{bmatrix} I_x \\ V_{y1} \\ V_{y2} \\ V_{y3} \end{bmatrix}, \tag{1}$$

where $k = 1, 2$ denotes the kth active device. In Figure 1, α and γ are frequency-dependent nonideal current gains and β is frequency-dependent nonideal voltage gain, which are all ideally equal to unity.

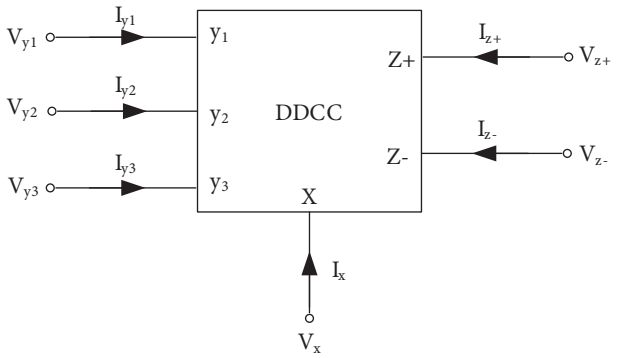

Figure 1. Electrical symbol of the six-terminal DDCC.

Applying straightforward analysis to the FIS topologies in Figures 2 and 3, the following matrix equation is ideally found to be:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sCR_1R_2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{2}$$

Note that the FIS topologies in Figures 2 and 3 have only resistors but no capacitors connected in series to the X terminals of the DDCCs; thus, they can be operated at higher frequencies [33], which is one of the most important properties of the proposed FISs. The high-frequency performance of both of the proposed FISs can

be further increased by the method given in [34]. Ideal and nonideal representations of an FIS are respectively given in Figures 4a and 4b. In Figure 5, representation of the first proposed FIS for the stability test is given.

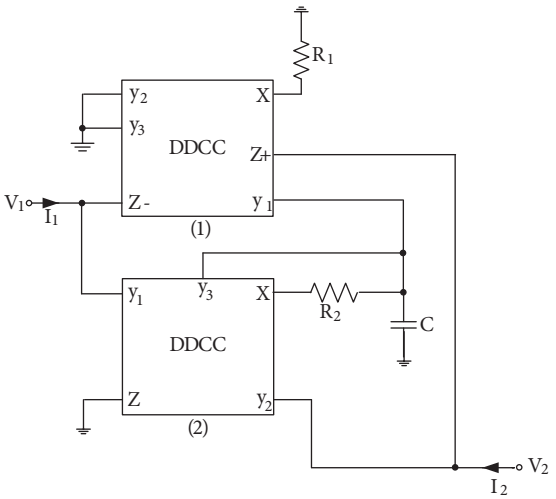

Figure 2. The first proposed floating inductor simulator circuit.

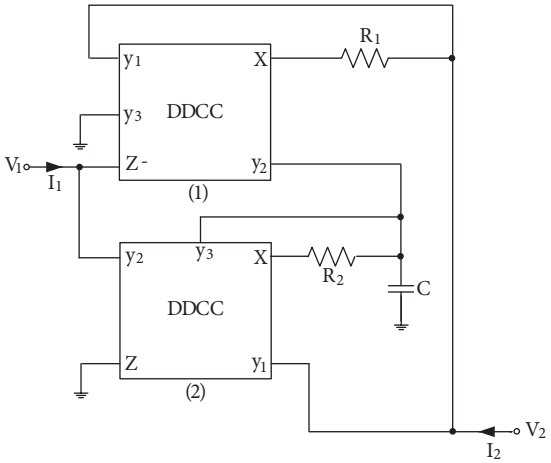

Figure 3. The second proposed floating inductor simulator circuit.

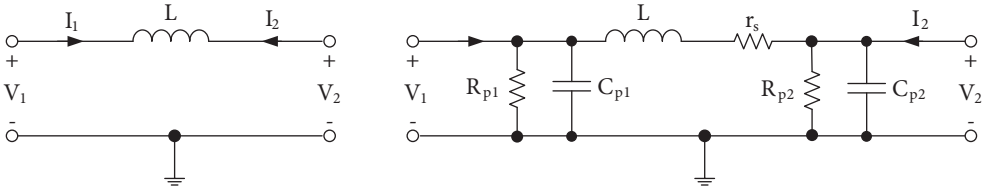

Figure 4. Representation of the FISs given in Figures 2 and 3: a) ideal, b) nonideal.

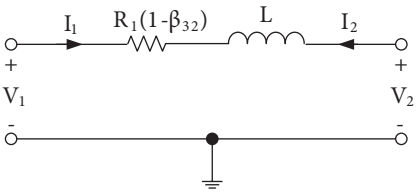

Figure 5. Floating inductor simulator representation of Figure 2 for stability test.

If nonideal gains are considered, the first proposed FIS in Figure 2 can be expressed by the following matrix equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{\beta_{11}}{sCR_1R_2 + R_1(1-\beta_{32})} \begin{bmatrix} \beta_{12}\gamma_1 & -\beta_{22}\gamma_1 \\ -\alpha_1\beta_{12} & \alpha_1\beta_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{3}$$

For simplicity, it is assumed that all the nonideal gains except β_{11} and β_{32} are equal to unity. Then matrix equation in Eq. (3) turns into

$$\begin{aligned} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} &= \frac{\beta_{11}}{sCR_1R_2+R_1(1-\beta_{32})} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \\ &= \frac{1}{sL_{eq}+R_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \end{aligned}. \tag{4}$$

Here, $L_{eq} = CR_1R_2/\beta_{11}$ and $R_{eq} = R_1(1-\beta_{32})/\beta_{11}$. Therefore, active and passive sensitivities are calculated as:

$$\begin{array}{l} S_C^{L_{eq}} = S_{R_1}^{L_{eq}} = S_{R_2}^{L_{eq}} = -S_{\beta_{11}}^{L_{eq}} = 1 \\ S_{R_1}^{R_{eq}} = -S_{\beta_{11}}^{R_{eq}} = 1 \\ S_{\beta_{32}}^{R_{eq}} = \frac{\beta_{32}}{\beta_{32}-1} \end{array} . \tag{5}$$

The FIS in Figure 3 can be expressed as:

$$I_1 = \frac{\beta_{21}\beta_{22}V_1 + (-1 + sCR_2(\beta_{11}-1) - \beta_{12}\beta_{21} - \beta_{11}(\beta_{32}-1) + \beta_{32})V_2}{sCR_1R_2 + R_1(1-\beta_{32})}\gamma_1, \tag{6}$$

$$I_2 = \frac{-\beta_{21}\beta_{22}V_1 + (1 - sCR_2(\beta_{11}-1) + \beta_{12}\beta_{21} + \beta_{11}(\beta_{32}-1) - \beta_{32})V_2}{sCR_1R_2 + R_1(1-\beta_{32})}. \tag{7}$$

3. Simulation results

To verify the theoretical results, the FIS circuits were simulated with SPICE program using 0.13 μm IBM CMOS technology parameters (http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ibm-013/t97f_8hp_5lm-params.txt), where ± 0.75 V DC power supply voltages and bias voltage $V_B = 168$ mV were chosen. The DDCC in Figure 6 was derived from the structure reported in [29]. The dimensions of the CMOS transistors employed in DDCC structure are given in Table 1. Parasitic impedances of both proposed FISs are given in Table 2, where the passive components $R_1 = R_2 = 1$ kΩ (X terminal parasitic resistor $R_x = 80$ Ω is included) and $C = 5$ pF were chosen to obtain $L_{eq} = CR_1R_2 = 5$ μH.

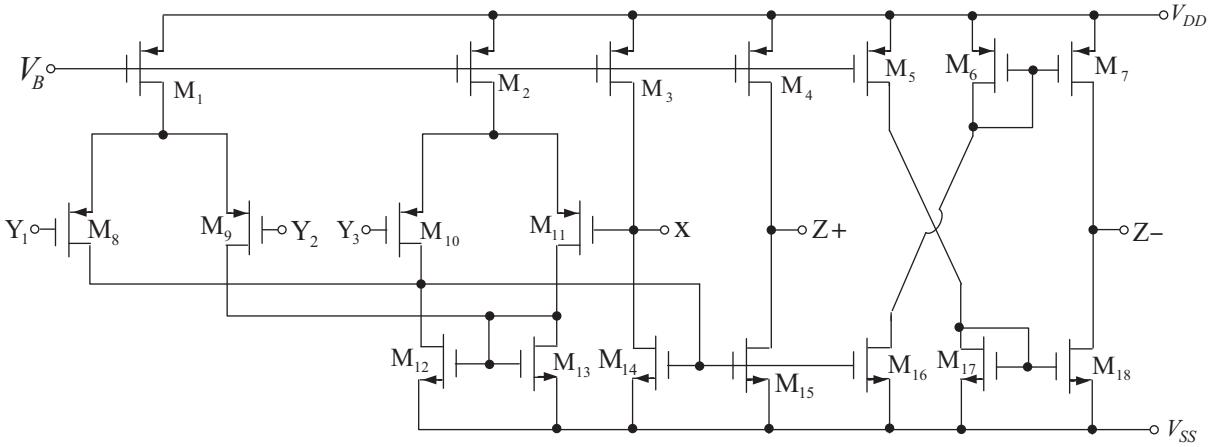

Figure 6. Internal structure of the DDCC derived from [29].

Table 1. Aspect ratios of the CMOS transistor of the DDCC in Figure 6.

PMOS transistors	W (μm) / L (μm)
M_1–M_{11}	41.6/0.52
NMOS transistors	W (μm) / L (μm)
M_{12}–M_{18}	4.55 / 0.52

Both ideal and simulated magnitudes and phases of the proposed FISs in Figures 2 and 3 are respectively shown in Figures 7 and 8, where the second terminals of the FISs are grounded (400 nH $\leq L \leq$ 10 mH). As an

Table 2. Parasitic impedances of the proposed FISs.

The first proposed FIS	The second proposed FIS
r_s =0.7 Ω	r_s =0.9 Ω
R_{p1} = 12.7 kΩ	R_{p1} = 12.9 kΩ
R_{p2} = 9 kΩ	R_{p2} = 50.6 kΩ
C_{p1} = 168 fF	C_{p1} = 155 fF
C_{p2} = 138 fF	C_{p2} = 310 fF

example, the passive components $R_1 = R_2 = 1$ kΩ (X terminal parasitic resistor $R_x = 80$ Ω is included) and $C = 5$ pF were chosen to obtain $L_{eq} = CR_1R_2 = 5$ μH. Additionally, the frequency performance comparison graph of the proposed FISs with the FIS given in [14] is given as an example in Figure 9. Time domain responses of FISs in Figures 2 and 3 are respectively given in Figures 10 and 11, where triangular-wave input currents are applied to obtain corresponding square-wave output voltages. Power dissipations of the FISs in Figures 2 and 3 were approximately 6.9 mW. A fourth-order band-pass filter example to demonstrate the performance of the proposed FISs is given in Figure 12. The transfer function (TF) of the fourth-order band-pass filter in Figure 12 is evaluated as

$$H(s) = \frac{V_{BP}}{V_{in}} = \frac{s\frac{R_1}{L_1}}{s^2 + s\frac{R_1}{L_1} + \frac{1}{L_1C_1}} \times \frac{s\frac{R_2}{L_2}}{s^2 + s\frac{R_2}{L_2} + \frac{1}{L_2C_2}}, \tag{8}$$

where angular resonance frequencies are computed as

$$\omega_{O1} = \sqrt{\frac{1}{L_1C_1}}, \tag{9}$$

$$\omega_{O2} = \sqrt{\frac{1}{L_2C_2}}. \tag{10}$$

Quality factors are found as follows:

$$Q_1 = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}}, \tag{11}$$

$$Q_2 = \frac{1}{R_2}\sqrt{\frac{L_2}{C_2}}. \tag{12}$$

As an example, the passive components $R_1 = R_2 = 1$ kΩ (X terminal parasitic resistor $R_x = 80$ Ω is included) and $C = 25$ pF yielding $L_1 = L_2 = CR_1R_2 = 25$ μH are selected for both of the proposed FISs. Additionally, $R_1 = R_2 = 1$ kΩ and $C_1 = C_2 = 100$ pF resulting in $\omega_{o1} = \omega_{o2} = 20$ Mrad/s and $Q_1 = Q_2 = 2$ are chosen for the fourth-order band-pass filter in Figure 12. The gain responses of the fourth-order band-pass filter in Figure 12 are shown in Figure 13 where the first and second proposed FISs are separately employed. The total harmonic distortion variations at $f = 3.18$ MHz versus applied peak values of the sinusoidal voltage signal are given in Figure 14, where the first and second proposed FISs are separately employed. It is observed from Figure 14 that the first proposed FIS employed in the filter has a good performance when compared to the second one. Output and input noises with respect to frequency are given in Figure 15, in which the first and second proposed FISs are separately employed. As an example, the passive components $R_1 = R_2 = 1$ kΩ with 10% variations and $C = 5$ pF were selected for both of the proposed FISs to perform Monte Carlo analysis with fifty runs. The results for the first and second FISs are respectively given in Figures 16 and 17.

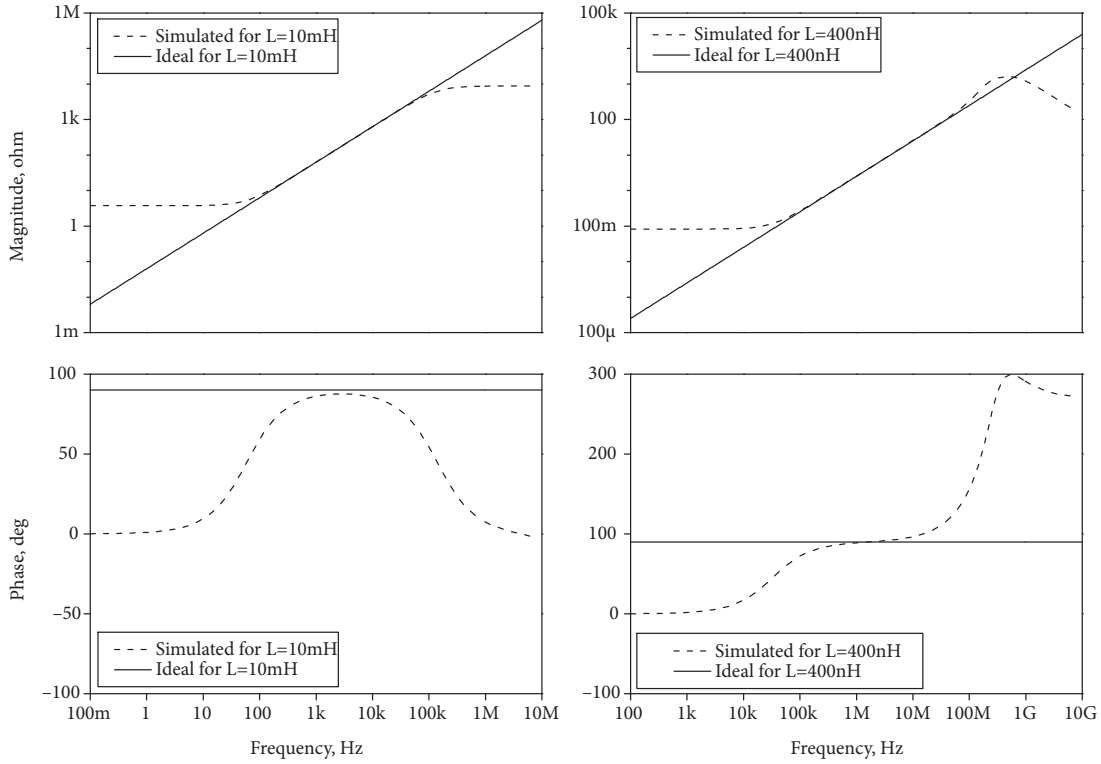

Figure 7. Impedance and phase of the floating inductor simulator in Figure 2 with respect to frequency.

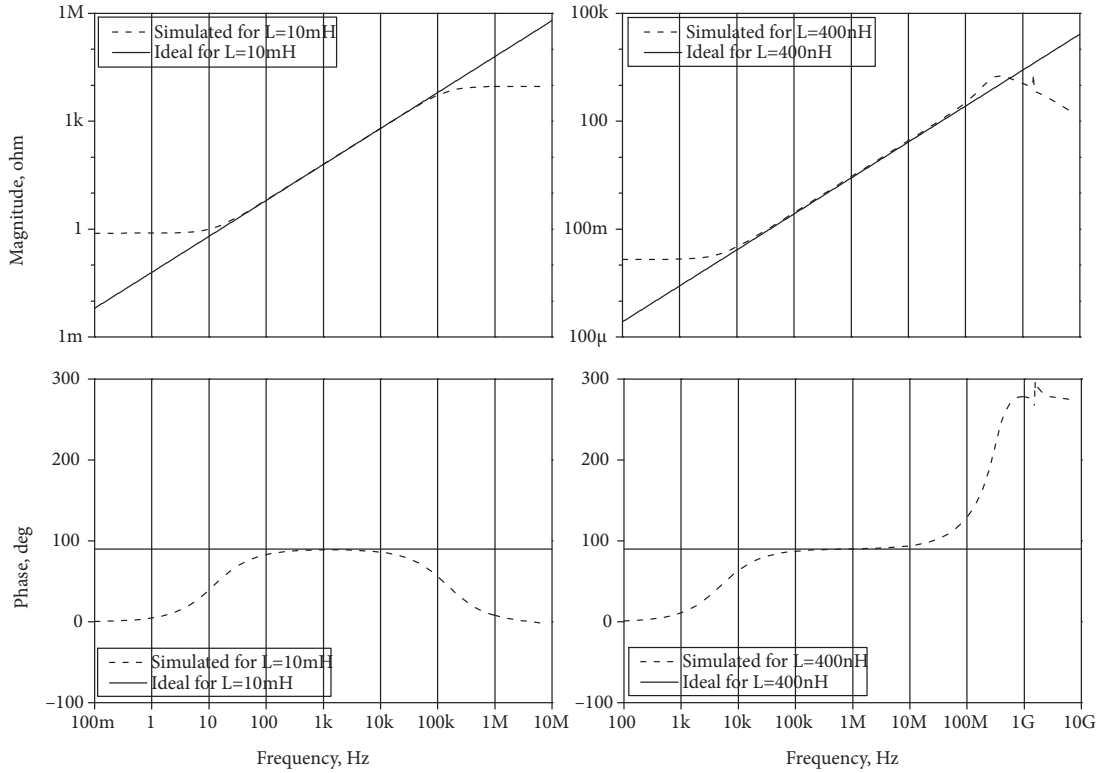

Figure 8. Impedance and phase of the floating inductor simulator in Figure 3 with respect to frequency.

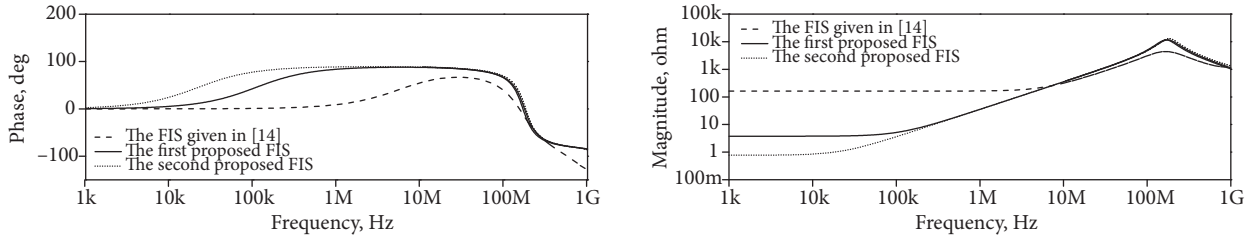

Figure 9. The comparison graph with FIS given in [14].

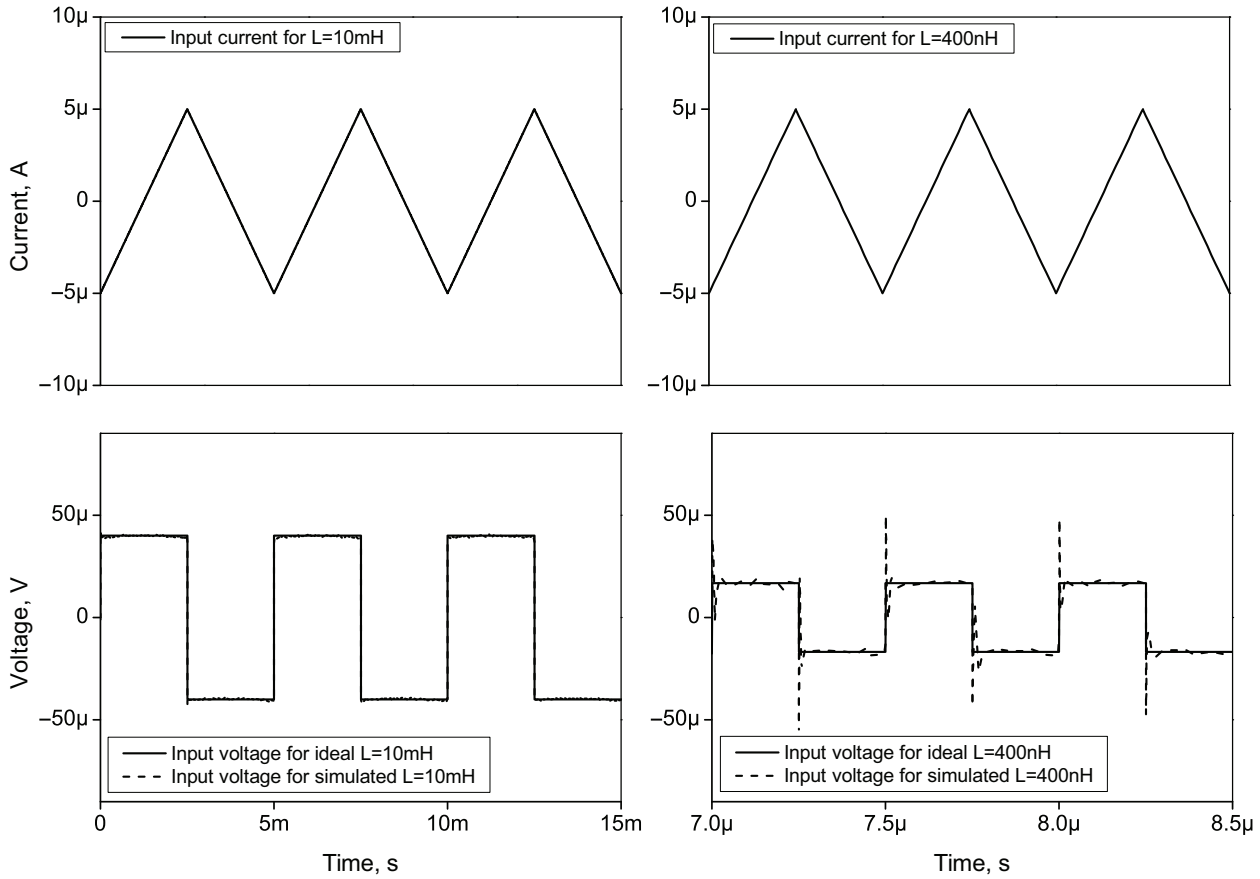

Figure 10. Ideal and simulated time domain responses of the floating inductor simulator in Figure 2.

Note that, as expected, simulation results agreed quite well with the theoretical ones. The discrepancy between ideal and simulated ones, however, mainly arises from nonideal gain and parasitic impedance effects of the DDCCs as well as signal limitations of the floating simulator configurations.

4. Stability analysis

Stability analysis was given for the filters in [35] and [36] before. Similarly, FISs have stability problems due to both poles and zeros of their impedances, which are affected by frequency-dependent nonideal gains [37]. In this paper, it is assumed that all the poles of frequency-dependent nonideal gains are sufficiently large; accordingly, their effects except DC gains are ignored. All the DC gains except β_{32} of the first proposed circuit are assumed

to be equal to unity. For the first proposed FIS, if $\beta_{32} \leq 1$, it is stable. Otherwise, it is unstable. However, if we replace the first proposed FIS in the second-order low-pass filter in Figure 18, the stability condition changes. Hence, the stability test for the second-order low-pass filter in Figure 19 is accomplished. Stability regions with respect to R_1 and β_{32} are given in Figure 19. It is important to note that $C = 100$ pF, $R_2 = 1$ kΩ, and $L = 10^{-7}R_1$ H are chosen in Figure 18 to draw the stable and unstable regions in Figure 19.

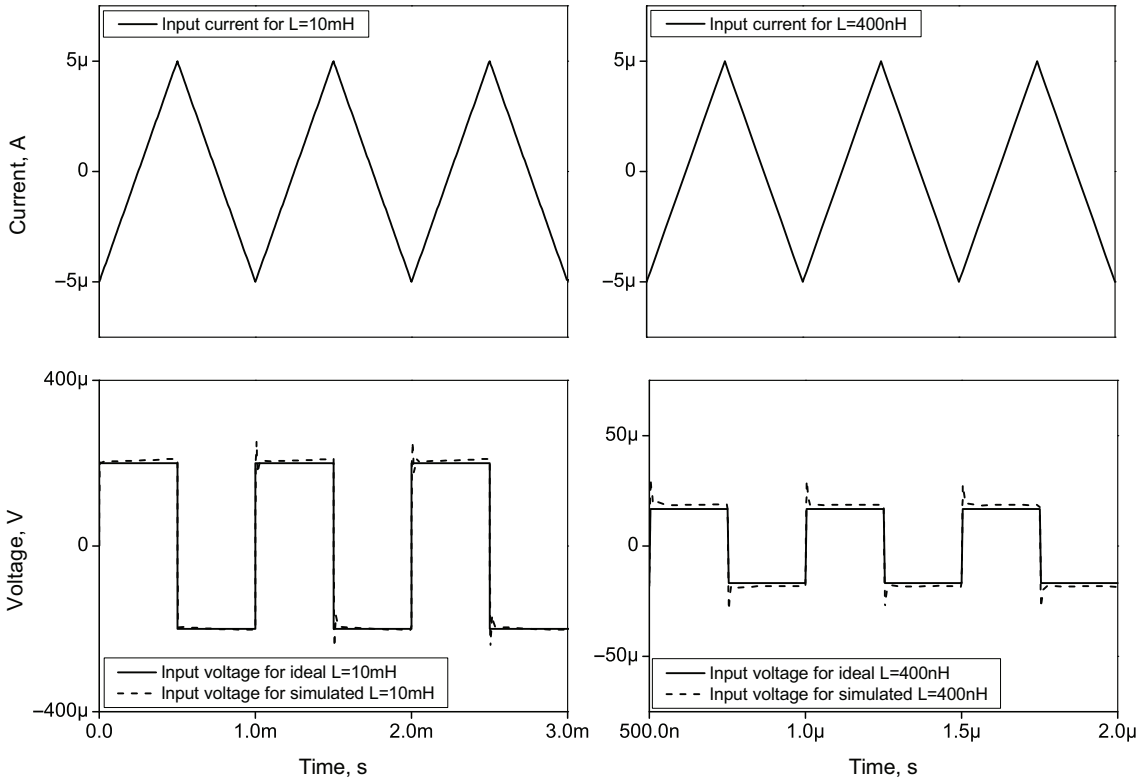

Figure 11. Ideal and simulated time domain responses of the floating inductor simulator in Figure 3.

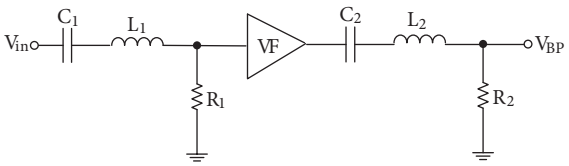

Figure 12. Fourth-order band-pass filter example to show performance of the proposed FISs.

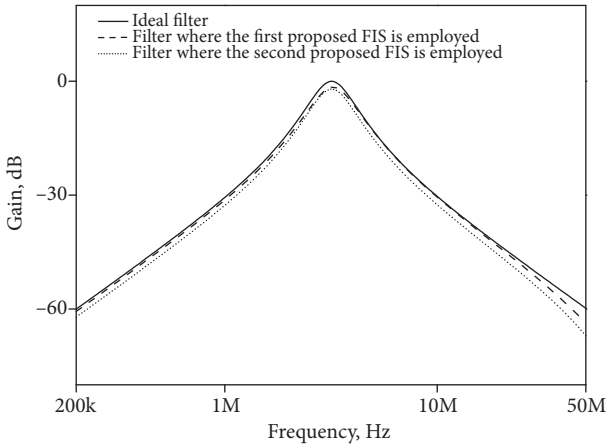

Figure 13. Gain responses of the fourth-order band-pass filter in Figure 11.

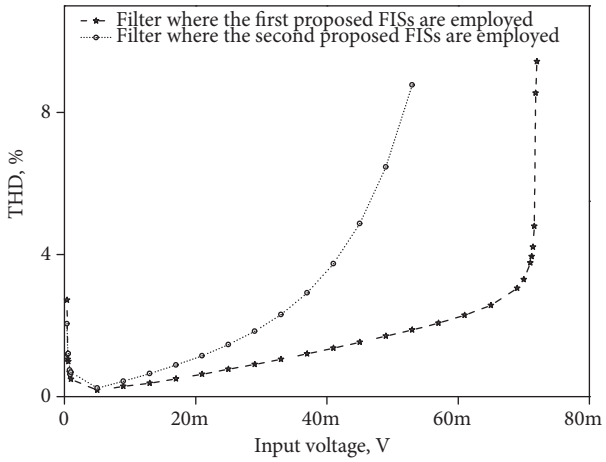

Figure 14. Total harmonic distortion variations at f = 3.18 MHz with respect to applied peak values of the sinusoidal voltage signals.

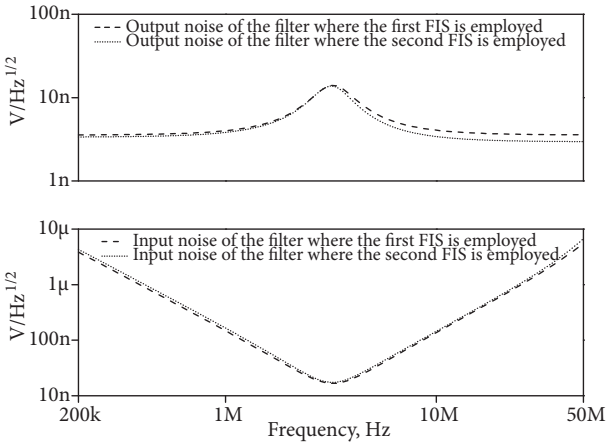

Figure 15. Output and input noises with respect to frequency.

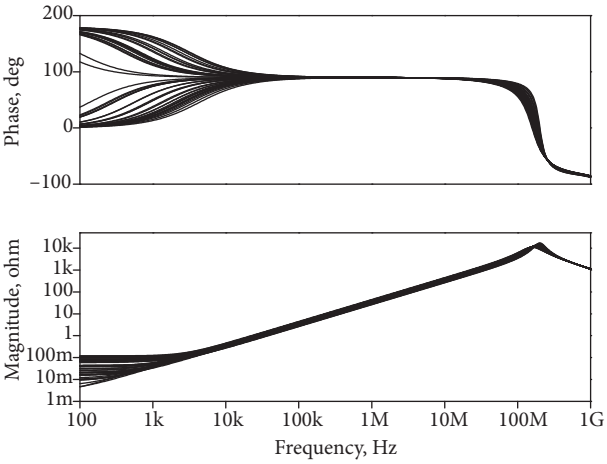

Figure 16. Monte Carlo analysis for the first proposed FIS.

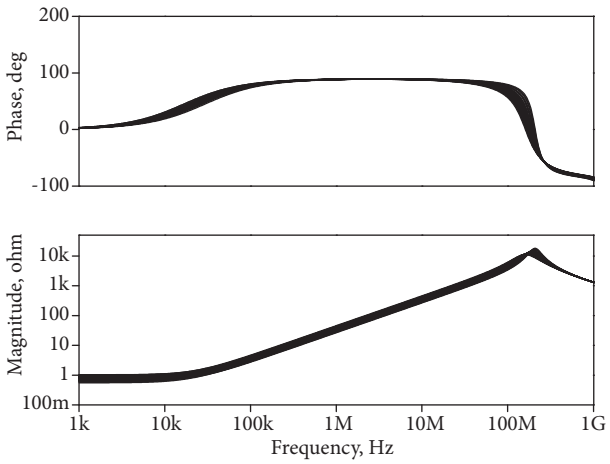

Figure 17. Monte Carlo analysis for the second proposed FIS.

The TF of the filter in Figure 18 is calculated as:

$$H(s) = \frac{V_{LP}}{V_{in}} = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{1}{RC} + \frac{R_1(1-\beta_{32})}{L}\right) + \frac{1}{LC}\left(1 + \frac{R_1(1-\beta_{32})}{R}\right)}. \tag{13}$$

Here, the angular resonance frequency and quality factor are respectively evaluated as follows:

$$\omega_o = \sqrt{\frac{1}{LC}\left(1 + \frac{R_1(1-\beta_{32})}{R}\right)}, \tag{14}$$

$$Q = \frac{\omega_o}{\frac{1}{RC} + \frac{R_1(1-\beta_{32})}{L}}. \tag{15}$$

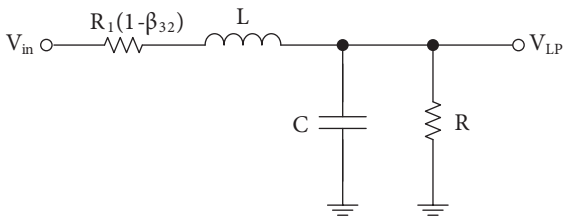

Figure 18. Second-order low-pass filter example for the stability test.

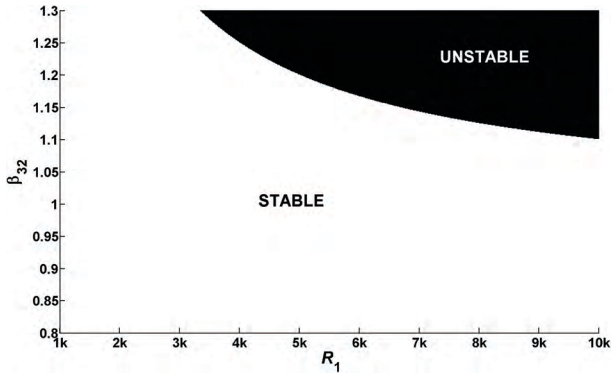

Figure 19. Stability regions with respect to R_1 and β_{32}.

5. Conclusion

In this study, two new FIS circuits employing two DDCCs are given. Neither of the proposed configurations in this work suffer from critical passive component matching conditions and they both consist of a canonical number of passive elements. In addition to these, both of the proposed FISs contain a grounded capacitor; thus, they are suitable for IC fabrication. Simulations performed with the SPICE program confirmed the proposed theory. Furthermore, a stability test was performed for the first FIS used in a second-order low-pass filter in order to provide a way for the analog circuit designers to determine the parameters of the circuits.

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