Trabajo Fin de Máster
"Máster Universitario en Microelectrónica: Diseño y Aplicaciones de Sistemas Micro/Nanométricos"

Study of the impact of lithography techniques and the current fabrication processes on the design rules of tridimensional fabrication technologies

Author: Miguel Gaitero Pérez

Advisor: Juan Antonio Leñero Bardallo

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❖ Acknowledgments

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❖ List of figures and tables

Throughout the document some figures and tables are cross-referenced. The reader may find below an index with all the used figures and tables for convenience.

❖ List of abbreviations

As other technical sectors, circuit manufacturing is full of abbreviations. A list of them (also the ones used at equations), properly sorted alphabetically with their signification, is included to allow the reader to always come back to check the meaning.

- ***%:*** per cent
- ***2D:*** Two Dimensional
- ***3D-IC:*** Three Dimensional Integrated Circuit
- A_{eff}***:*** cross sectional area of the *TSV*
- ***Al:*** Aluminium
- ***AMD:*** Advanced Micro Devices (company)
- ***APA:*** American Psychological Association
- ***Ar:*** Argon
- ***ArF:*** Argon FLuoride
- ***ASIC:*** Application-Specific Integrated Circuit
- ***ASML:*** Advanced Semiconductors Materials Lithography (company)
- ***Be:*** Beryllium
- ***BEOL:*** Back-End-Of-Line
- ***BGA:*** Ball Grid Array
- ***BSI:*** Backside Imager
- ***C:*** capacitance
- ***c:*** light speed in vacuum
- C_4F_8***:*** Octafluorocycloebutane
- ***CAD:*** Computer-Aided Design
- CaF_2***:*** Calcium Fluoride
- ***CD:*** Critical Dimension
- ***CFET:*** Complementary Field-Effect Transistor
- ***cm:*** centimeter
- cm^2***:*** square centimeter
- ***CMOS:*** Complementary Metal-Oxide-Semiconductor
- ***CMP:*** Chemical Mechanical Planarization
- ***CoC:*** Chip on Chip
- ***CoCoS:*** Chip on Chip on Substrate
- ***CoW:*** Chip on Wafer
- ***CoW:*** Chip on Wafer
- ***CoWoS:*** Chip on Wafer on Substrate
- ***CSP:*** Chip Scale Packaging
- ***CTE:*** Coefficient of Thermal Expansion
- ***Cu:*** copper
- Cu_3Sn***:*** no formal chemical name, represents the compound in the copper-tin phase diagram (Intermetallic Compound)

- ***CVP:*** Chemical Vapor Deposition
- ***D:*** diameter
- ***D2D:*** Die to Die
- ***D2W:*** Die to Wafer
- ***DB:*** Direct Bonding
- ***DBI:*** Direct BOnd Interface
- ***DfR:*** Design for Reliability
- ***DfY:*** Design for Yield
- ***DoF:*** Depth of Focus
- ***DPP:*** Discharge-Produced Plasma
- ***DR:*** Design Rule
- ***DRAM:*** Dynamic Random Access Memory
- ***DRIE:*** Deep Reactive Ion Etching
- ***DUT:*** Device Under Test
- ***DUV:*** Deep UltraViolet
- ***E:*** Energy
- ***e.g.:*** exempli gratia (for instance)
- ***ECD:*** Electrochemically Deposited
- ***ECTS:*** European Credit Transfer System
- ***ED:*** Electrical Discharge
- ***EM:*** Electromigration
- ***EUV:*** Extreme UltraViolet
- ***f:*** focal distance
- ***f:*** frequency
- ***FDSOI:*** Fully Depleted Silicon-On-Insulator
- ***FEOL:*** Front-End-Of-Line
- ***fF:*** femtofarad (s)
- ***FIB:*** Focused Ion Beam
- ***FPGA:*** Field Programmable Gate Array
- ***g*:*** complex optical transmittance
- ***GaAs:*** Gallium Arsenide
- ***GB:*** GigaByte
- ***GHz:*** GigaHertz (s)
- ***GPU:*** Graphics Processing Unit
- ***h:*** Planck constant
- ***h:*** TSV height
- ***H_2O:*** dihydrogen monoxide (water)
- ***HBM:*** High Bandwidth Memory
- ***HEBS:*** High-Energy Beam-Sensitive
- ***Hg:*** mercury
- ***HMC:*** Hybrid stacked Memory Device or Hybrid Memory Cube
- ***HVM:*** High-Volume Manufacturing

- ***I/O:*** Input/Output
- ***i.e.:*** id est (in other words)
- ***IC:*** Integrated Circuit
- ***ICP:*** Inductively Coupled Plasma
- ***ID:*** Identification
- ***IF:*** Intermediate Focus
- ***IH:*** Immersion Hood
- ***IL:*** Interference Lithography
- ***ILD:*** Interlayer Dielectric
- ***IMP:*** Ionized Metal Plasma
- ***In:*** Indium
- ***IP:*** Image Placement
- ***J:*** Joule
- ***K:*** Kelvin (s)
- k_1***:*** Rayleigh Resolution constant
- k_2***:*** Rayleigh Depth of Focus constant
- ***KOZ:*** Keep Out Zone
- ***KPI:*** Key Performance INdicator
- ***KrF:*** Krypton Fluoride
- ***LCD:*** Liquid Crystal Display
- ***LED:*** Light Emitter Diode
- ***LPP:*** Laser-Produced Plasma
- M_1***:*** first metal layer
- M_2***:*** second metal layer
- m^2***:*** square meter
- ***MEMS:*** Micro-Electro-Mechanical System
- ***MIT:*** Massachusetts Institute of Technology
- ***mJ:*** millijoule (s)
- ***mK:*** millikelvin (s)
- ***mm:*** millimeter
- ***Mo:*** Molybdenum
- ***MOCVD:*** Metallo-Organic Chemical Vapor Deposition
- ***MOSFET:*** Metal Oxide Semiconductor Field Effect Transistor
- ***mW:*** milli Watts
- ***mΩ:*** milliohm(s)
- ***n:*** index of refraction
- ***n:*** refraction index
- ***NA:*** Numerical Aperture
- ***NAND:*** type of flash memory based on NAND-gates (no real abbreviation)
- N_f***:*** number of exposure fields per wafer
- ***nm:*** nanometer
- ***O:*** overlay

- ***O/O_2:*** oxygen
- ***O_3:*** ozone
- ***OH:*** hydroxide
- ***P_1:*** vector position of the corresponding point
- ***P_2:*** vector position of a substrate geometry
- ***PCB:*** Printed Circuit Board
- ***PECVD:*** Plasma-Enhanced Chemical Vapor Deposition
- ***pH:*** picohenry (s)
- ***PMMA:*** Polymethyl Methacrylate
- ***poly-Si:*** Polysilicon
- ***PoP:*** Package-on-Package
- ***PSM:*** Phase Shift Mask
- ***R:*** resistor/resistance
- ***R:*** Resolution
- ***RC:*** Resistor Capacitor
- ***RET:*** Resolution Enhancement Technique
- ***RF:*** Radio Frequency
- ***RLC:*** Resistor Inductor Capacitor (refers to a the circuit modelling using those elements)
- ***RMS:*** Root Mean Square
- ***s:*** second (s)
- ***S_a:*** sidewall area of a TSV
- ***SACVD:*** Subatmospheric Chemical Vapor Deposition
- ***SAM:*** Scanning Acoustic Microscopy
- ***SEM***: Scanning Electron Microscopy
- ***SF_6:*** Sulfur Hexafluoride
- ***Si:*** silicon
- ***SiO_2:*** Silicon Dioxide
- ***SiP:*** System in Package
- ***SiP:*** System-in-Package
- ***SLID:*** Solid-Liquid Interdiffusion
- ***Sn:*** tin
- ***Sn:*** tin
- ***SoC:*** System on a Chip
- ***SOI:*** Silicon On Insulator
- ***SPIE:*** Society of Photographic Instrumentation Engineers
- ***T:*** throughput
- ***TaN:*** Tantalum Nitride
- ***TEM:*** Transmission Electron Microscopy
- ***TEOS:*** tetraethyl orthosilicate
- ***t_{exp}:*** exposure time
- ***t_{foh}:*** overhead time per exposure field
- ***t_{ILD}:*** dielectric liner thickness

- ***TiN:*** Titanium Nitride
- ***TSMC:*** Taiwan Semiconductor Manufacturing Company
- ***TSV:*** Through Silicon Via
- ***TTL:*** Through-The-Lens
- ***TTV:*** Total Thickness Variation
- ***TV:*** Television
- t_{woh}***:*** overhead time per wafer
- ***UV:*** UltraViolet
- ***V:*** Volt (s)
- ***VFET:*** Vertical Field-Effect Transistor
- ***Vs.:*** versus
- ***W:*** tungsten
- ***W:*** Watt (s)
- ***W2W:*** Wafer to Wafer
- ***WLCSP:*** Wafer Level Chip Scale Packaging
- ***WoW:*** Wafer on Wafer
- ***x:*** distance (typically in horizontal axis)
- ***y:*** distance (typically in vertical axis with two dimensions)
- ***Z:*** distance (typically in vertical axis with three dimensions)
- ***º:*** degree
- ***ºC:*** degree Celsius
- ***Θ:*** angle
- ε_0***:*** free space permittivity
- ε_r***:*** relative permittivity
- ***λ:*** wavelength
- ***μm:*** micrometer/micron
- ***ρ:*** distance (in polar coordinates)
- ρ_m***:*** material resistivity

❖ List of equations

Throughout the document some formulae are used to illustrate the concept. They are number out with the section where they are mentioned and a number in latin numbers which is an ascendent counter.

❖ Key words

Some important concepts which will be used throughout the thesis are briefly defined, in order for the reader to get familiar with the most relevant and recurrent terms. The words are sorted alphabetically, thus providing an easy overview, always allowing the reader to come back to remember what the word means.

- ***2D*-circuits/devices:** conventional *IC*s which do not stack different layers.
- ***2.5D*-interposer:** predecessor of the *3D*-integration consisting on linking various layers by means of a silicon interposer.
- ***3D*-circuit/integration**: alternative to conventional circuits manufacturing, consisting on stacking various layers (also known as tiers) to increase the efficiency of the system and decrease the interconnection length.
- **(Optical) aberration**: flaw or distortion in the patterned image (at the wafer), compared to the original pattern. It is produced by the optical lens.
- **Back-End-Of-Line (*BEOL*):** term used at the manufacturing industry to describe the last processes during circuit manufacturing. It includes the process steps after the first metal layer, including the interconnections between layers for *3D*-Integrated Circuits.
- **Chemical Mechanical Planarization (*CMP*):** process used in circuit manufacturing, consisting in making the wafer more flat in order to avoid issues during expose, material deposition or etching.
- **Chip-on Chip (*CoC*)/Die-to-Die (*D2D*):** sort of *3D*-bonding technique consisting of stacking a chip (die) into another chip (die).
- **Chip-on Wafer (*CoW*)/ Die to Wafer (*D2W*):** sort of *3D*-bonding technique consisting of stacking a chip (die) into a wafer.
- **Critical Dimension (*CD*)/Feature size/linewidth**: refers to the size (width) of the pattern imaged onto the wafer. The control of the Critical Dimension is key in the photolithography process, since it defines the performance of the circuit.
- ***Cu* protrusion:** effect consisting on having hillocks formed during the heating process, being a reliability concern for thermomechanical failures in subsequent layers which is usually addressed by adding the extra process of *TSV* annealing.
- **Depth of Focus (*DoF*)**: figure which represents the tolerance of the distance between the lens and the wafer that can be modified in order to still achieve a correct patterning process. It can be calculated with the Rayleigh equation.
- **Direct Bonding:** *3D*-circuits manufacturing process consisting on attaching two similar or dissimilar materials without anything between them.
- **Dry lithography/tool**: using air surrounding the lens instead of water. It is used by the conventional photolithography.
- **Etching:** process used in circuit manufacturing, consisting on removing by means of chemical products a layer or substance from the top surface of a wafer.
- **Extreme UltraViolet (*EUV*) light/lithography**: light with a wavelength in a range between 11 and 14 nanometers. In photolithography, it is used a wavelength of 13.5 *nm*

for *EUV* lithography, which has improved the resolution of the pioneer systems, in opposition to the conventional Deep UltraViolet (*DUV*) lithography, which typically uses wavelengths between 193 and 365 *nm*.

- **Fab/factory:** utility where the circuits are manufactured.
- **Front-End-Of-Line *(FEOL):*** term used at the manufacturing industry to describe the first processes during circuit manufacturing. It includes the process steps preceding the first metal layer.
- **Holographic/interference lithography:** alternative lithography technique consisting on using various coherent laser to create a interferences so that an inclined pattern is printed into the surface of the wafer. Used for *3D*-lithography novel techniques.
- **Hybrid bonding:** *3D*-circuits manufacturing process consisting on attaching two materials with the help of an added material in one of the bonding surfaces, forming the electrical connection.
- **Immersion (wet) lithography/tool**: using liquid -concretely water- surrounding the lens instead of air, in order to improve the resolution of the photolithography process.
- **Inclined mask/lithography:** alternative lithography technique consisting on tilting the reticle and the wafer so that inclined/*3D*-patterns can be printed into the wafer. Used for *3D*-lithography novel techniques.
- **Indirect Bonding:** *3D*-circuits manufacturing process consisting on attaching two materials by means of an intermediate material which makes the connection.
- **Integrated Circuit (*IC*)**: electronic circuit formed on a small piece of semiconducting material (typically silicon) which performs different functionalities.
- **Keep Out Zone (*KOZ*):** area surrounding *TSV* to create a safe distance between *TSV*s and active devices in order to eliminate proximity effects.
- **Key Performance Indicator (*KPI*)**: figure which specifies the quality/performance of a process. It is specific of the process, being the most common for photolithography the overlay.
- **(Excimer) laser**: ultraviolet light generator used in the production of microelectronics among others. It is the light source for the photolithography tool.
- **(Optical/projection) lens**: single, optically transparent device which enhances the transmission and refraction of light. In photolithography, it allows the light generated by the laser to pass through, so that the pattern can be imaged onto the wafer.
- **(Alignment) marks/keys/targets/fiducials**: distinguishable patterns used as reference point for the photolithography tool to establish the coordinate system at the wafer level.
- **Modulated/*3D*-lithography:** alternative lithography techniques not consisting on using optical means, but other processes able print *3D*-patterns.
- **Moore's law**: observation and prediction made in 1965 by Gordon Moore, co-founder of Intel, postulating that the number of transistors per square inch on integrated circuits had doubled (and will double) every two years.
- **Multilayer Mirror/Bragg Mirror**: type of mirrors used at *EUV* lithography since they are able to reflect the light, thus achieving larger incident angles that conventional mirrors.

- **Numerical Aperture (*NA*)**: dimensionless number that measures the ability to gather light and to print a pattern at a fixed distance. It is a lens feature which is to be enlarged, in order to allow more light to pass through.
- **Overlay/alignment**: figure which indicates how well the stack-up between layers is done (in terms of relative position). The alignment is the process performed at the photolithography tool in order to achieve better overlay.
- **Pattern**: pre-defined model or shape which is used in photolithography to build the circuits by imaging it onto the wafer.
- **Pattern generator**: photolithography tool which uses as input data a database to directly create a physical image on the wafer.
- **Pattern replicator**: photolithography tool which creates a master pattern image in the form of a reticle and them replicates the pattern in a massively parallel fashion onto the wafer by means of a projection lens. It is the most common type of photolithography tool.
- **Phase Shift Mask (*PSM*)**: a technique based on the principle of light interference with the goal of creating destructive interferences between the light from the adjacent openings, so that the resolution of the photolithography tool is improved.
- **Photolithography/optical lithography/conventional/*UV* lithography**: process of imaging a pattern onto a wafer by means of light. It is a key process in the electronic manufacturing, since its quality defines the performance of the circuit.
- **(Wafer) processing**: all the methods performed at the track. It includes coating and baking among others, which are needed to condition the wafer in order to perform the photolithography process.
- **Rayleigh equation**: mathematical relationship between the resolution of the photolithography process with respect to the Numerical Aperture of the lens and the wavelength of the inciding light. It also specifies the Depth of Focus used by the image lens.
- **Refraction index *n***: dimensionless number which describes how fast the light propagates through the material. It is characteristic of each medium, thus defining the optical features in that environment.
- **Reliability:** concept to describe how well a product will behave in the long run. It is a key feature on a product, since has to be tested during product verification to guarantee the customer that the functionality will be kept throughout the time.
- **(Photo)resist**: organic material which consists of a polymer base resin. It is coated at the track to the wafer surface, allowing a certain wavelength to pass through to print the pattern into the wafer.
- **Resolution/accuracy**: figure which defines the ability to distinguish different components within a group of objects. Whereas the Critical Dimension or pattern size is more related to the circuit (the result of the photolithography process), the resolution/accuracy refers more to the photolithography tool itself.
- **Resolution Enhancement Techniques (*RET*s)**: methodologies which improves the imaging performance (better resolution) by wavefront, mask or resist process engineering, thus reducing the Rayleigh constant k_1.

- **Reticle/photomask**: both terms are identical, defining an opaque element with a "written" pattern on it. Physically it is a thin sheet with some holes which allows the light to pass through, thus replicating the patterns into the wafer.
- **Scallop:** small ridges formed during *TSV* etching, being a well-known pattern as a result of that process.
- **Scanner/step-and-scan tool/(photo) lithography tool/exposure tool**: it is the system (machine) which performs the photolithography process. The three concepts will be used as synonyms throughout the thesis, consisting in the most advanced system types, where both the reticle and wafer are moving at the same time to improve accuracy and throughput.
- **Silicon (*Si*):** semiconductor material which is mainly used at the electronic industry due to its properties. It is provided to the factories in small rounded-pieces called wafers.
- **System in Package (*SiP*):** concept used to describe numeral *IC*s integrated in one single chip carrier package.
- **Throughput**: indicator of the amount of parts (in photolithography, wafers) that can be processed in a certain amount of time (typically one hour).
- **Through Silicon Via (*TSV*)**: vertical electrical interconnection in the 3D-Integrated Circuits, which passes through the different layers of the die.
- **Tier/layer:** each of the strata for *3D*-Integrated Circuit. Typically interconnected by *TSV*s.
- **Track**: system or machine which performs the processing of the wafer, *i.e.* the chemical treatments before and after the photolithography process to condition the wafer.
- ***TSV*-first:** process flow for *3D*-Integrated Circuits, consisting on creating the via before the *FEOL*.
- ***TSV*-last:** process flow for *3D*-Integrated Circuits, consisting on creating the via during or after the *BEOL*. Two variants exist depending on where the interconnection is done: backside or frontside.
- ***TSV*-middle:** process flow for *3D*-Integrated Circuits, consisting on creating the via after the *FEOL* but before the *BEOL*.
- **Voids:** concept which describes the absence of material at *3D*-bonding, being a reliability concern since the electrical connection and the junction robustness are degraded.
- **Wafer**: a thin slice of semiconductor used as substrate for electronics manufacturing. It is conventionally made on a circular shape with a diameter of 200 or 300 *mm*.
- **Wafer-on-Wafer (*WoW*)/Wafer to Wafer (*W2W*):** sort of *3D*-bonding technique consisting on stacking a wafer into another wafer.
- **Wavelength**: physics feature which represents the distance between two consecutive points on a wave shape, where the same state is achieved. In photolithography, it is used to characterize the light source, thus defining the resolution of the tool by means of the Rayleigh equation.
- **Yield:** figure to show how well a process performs. Typically represents the ratio between the good (based on one or multiple criteria) manufactured parts out of the total manufactured parts.

- **Zernike coefficients**: mathematical invention which consists on numeral polynomials describing an optical tool. They are used to easily observe the aberrations in optical systems.

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1. Introduction

Electronic market has experienced an incredible growth during the past century, thus being nowadays one of the leading economies at the industry. The semiconductor companies, which customize the conductivity of the raw piece of silicon to fabricate the microchips, have generated sales in 2018 equivalent to 477.94 billion U.S. dollars *[1]*, proving the increasing importance of the market as shown in figure 1.

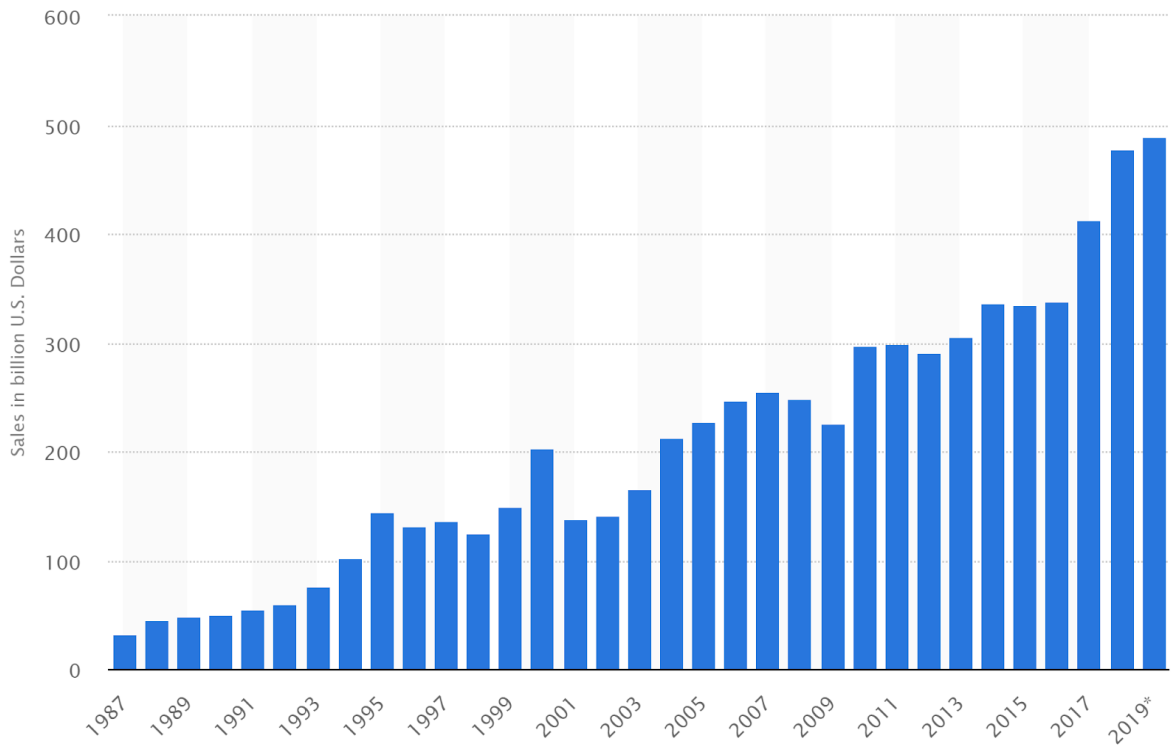


Figure 1: *Yearly sales for the semiconductor industry [1].*

The origin of that revolution, the seed that caused this “big-bang” of electronics, was a grain of germanium on which the point contact transistor was fabricated for the first time in 1947 by J. Bardeen, W. Brattain, and W. Shockley *[2]*. That was the trigger for an unending race on continuous improvement to look for the “perfect transistor” which has the best physical and mechanical features to makes the chips of today. The evolution throughout history is depicted in figure 2, where different paths have been explored by the researchers community.

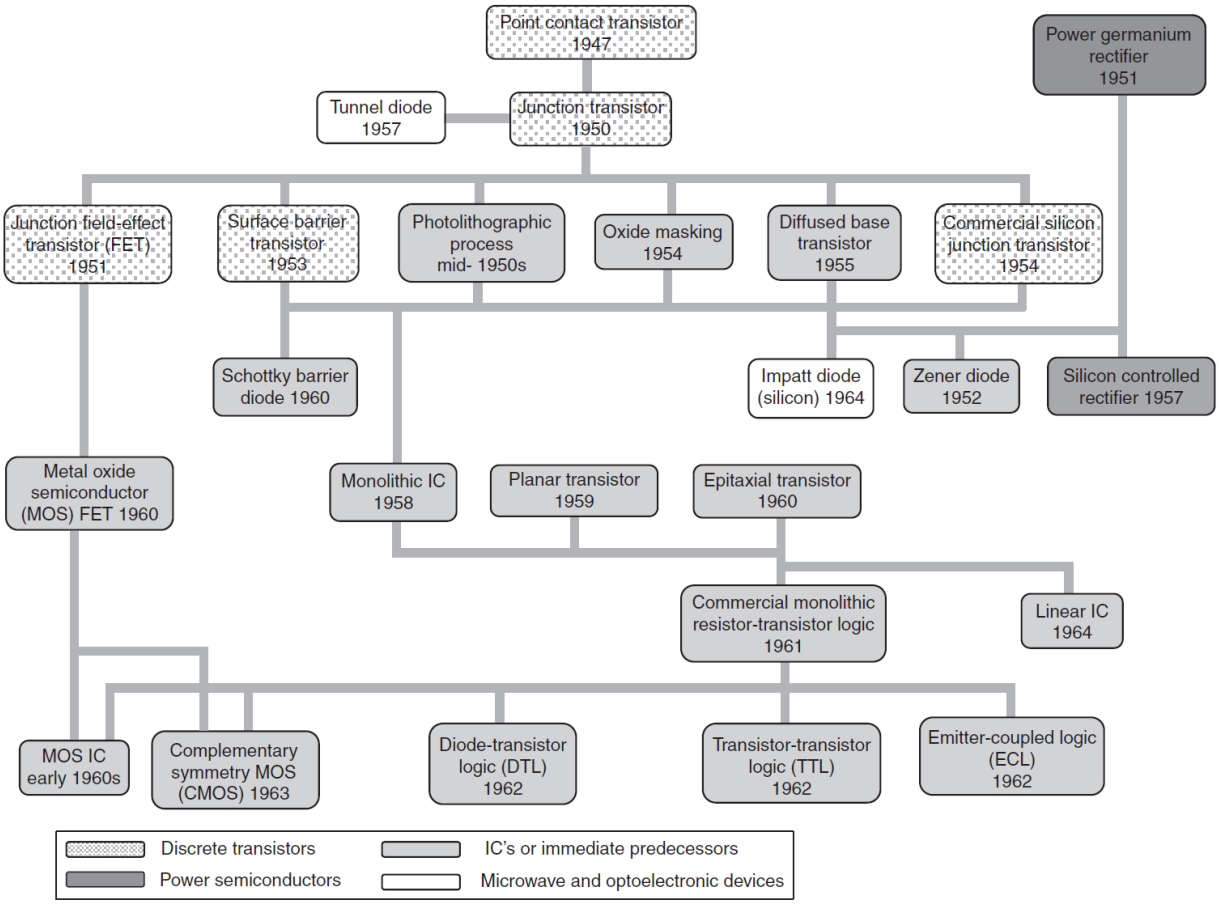


Figure 2: *History of transistor generations and logic styles [3].*

The boom of the robust *MOSFET* as preferred option, empowered the semiconductor market throughout the years, where the chips manufacturing was considerably advanced due to automation, reducing the cost and time to market and offering more reliable products, while increasing employee safety through highly sophisticated electronic security systems that can recognize and warn of critical equipment failures [4]. Electronics appeared then as an easy solution for storing media, making communication faster and better with each other (the Internet), improving medical procedures with noninvasive techniques or helping the science to advance by making computational tasks ultra fast.

Using electronics today is so much a part of our daily lives we hardly think of the way the world would be without electronics *[5]*. Everything from cooking to music uses electronics or electronic components in some way. Our family car has many electronic components, as does our cooking stove, laptop and cell phone. Cell phones are everywhere to take and send pictures, play music, text messages or just checking whe weather forecast. The Internet is used by almost everyone, from companies to send emails or store the information, to the personal usage such as online shopping or checking the bank statement. Music is a prime user of electronics, both in recording and in playback mode: music players, head- or earphones and speakers would not be existing without the electronic revolution. Television as main pastime fully incorporates the latest advances in electronics, being now able to get connected to the Internet and to other devices. Cameras of today are affordable, being included in the cell phone or as individual device, with the pictures easily to be easily edited through the marvel of electronics. Electronics devices are being used in the health field, not only to assist in diagnosis and determination of medical problems, but also to assist in the research that is providing treatment and cures for illnesses and even genetic anomalies, thus being pacemakers or similar equipment implanted in the body as almost a routine activity.

It is clear that today's lives are impossible to conceive without the electronics. How is that progress possible and for how long can withstand? Well, the electronic evolution through the years is known as the Moore's law, who stated that the amount of transistors on a chip doubles every two years. But the implication is not only about that figure, but also about the feature size, cost or power, as the figure 3 suggests, resulting in smaller, cheaper and more power microchips, respectively.

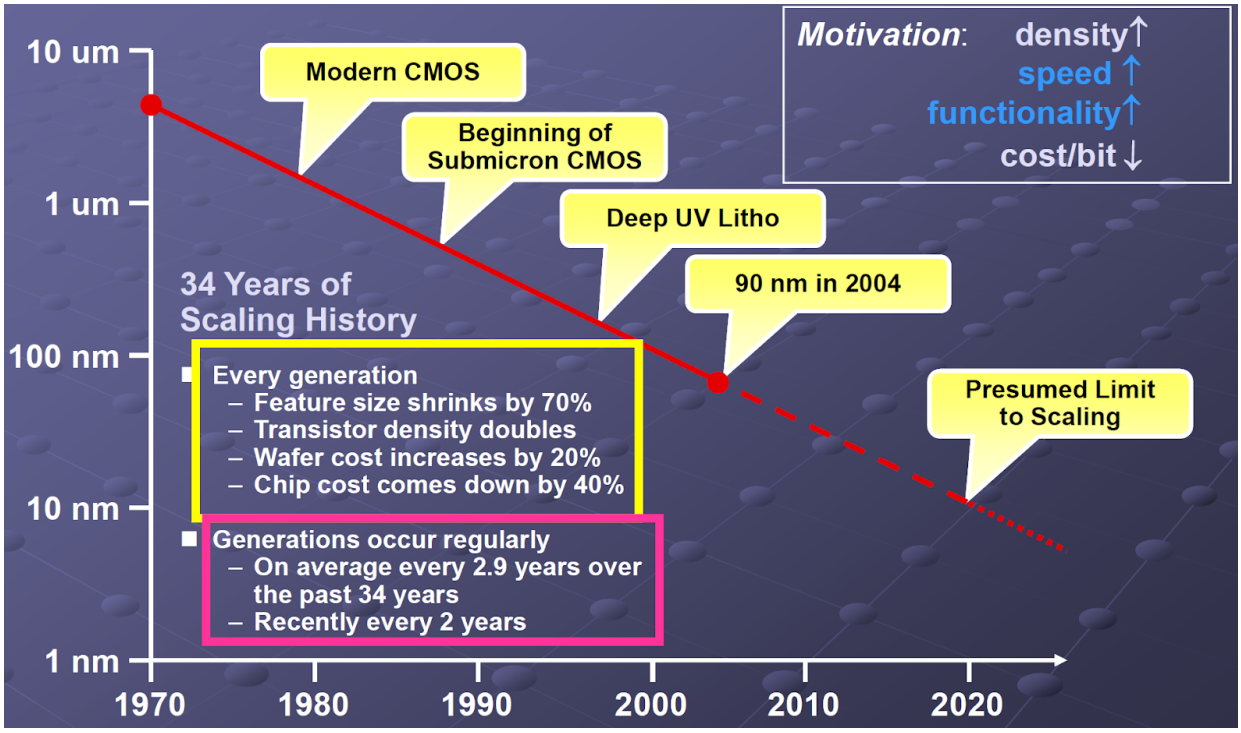


Figure 3: *Patterning size evolution throughout the years [6].*

This is where the photolithography came to the play, being the main process of the chip manufacturing. Its process quality, cost and cycle time are the main figures for the factories to take into account at the chip production. The evolution of the transistor size has gone hand-by-hand with the photolithography progress: the smaller the feature size printed by the photolithography tool, the faster and smaller the microchip. Advances in lithography have been possible thanks to good understanding of the optics and physics behind the process, as well as material properties, making possible to keep Moore's law valid until nowadays.

However, the size shrinking can not long forever: even with the most advanced lithographic techniques, it is expected that physical limitations will impide the transistor size to be decreased. Some alternatives have appeared with the goal of replacing the conventional photolithographic process to drive the future of the semiconductor industry. Concretely, the approach of stacking-up different layers to create a *3D*-integrated device, has recently gained a lot of weight at some electronic applications, since it allows to integrate different functionalities at a chip without increasing the power dissipation which is one of the main factors braking the scaling progress. *3D*-integration seems as a valid candidate for certain applications, but it is not yet used for mass production due to some technological challenges.

The present is clear: using the photolithography breakthroughs is allowing to continue with the trends to improve our daily lives with smaller microchips. The future is uncertain though: will the *3D*-integration the solution for the chip of tomorrow? It is difficult to predict the market evolution, but at least knowing the state-of-the-art of both technologies will help to have a better understanding of the current issues and how the industry is tackling them to improve our lives with better chips.

1.1. Motivation

Working for the photolithography tool manufacturer leader sometimes gives me the impression of how complex and specific is the sector I am working on. This master thesis topic came with the goal of getting the overall picture of the state-of-the-art: stepping out and trying to get a helicopter view usually helps to understand where a process is in the productive chain, or what other firms and markets are doing to continue improving.

So, I came across with the idea of researching about the photolithography cutting edge, linking the particular vision I have from the company with the adds-on of the available literature. The ultimate goal was to allow the thesis reader to follow the progress of the photolithography throughout the history, understanding the basic concepts of the technology to explore how the industry is reinventing itself. On that way, it would also help to understand the overall picture: too often some concepts are daily used but we do not have the knowledge or know-how to grab what is behind or why it has revolutionized the market. With this thesis, I aim to understand those daily concepts and allow the thesis reviewer to get familiar with the background, so that a trajectory through the history can be easily followed. Take for instance a practical example, the news about faster microchips using Extreme UltraViolet (*EUV)* lithography (light source with wavelength of 13.5 *nm*): the user may have read that without really knowing what the breakthrough is about it. Rather than going directly to explain what the *EUV* is, through this thesis one can feel driven to need to know why it came up: the photolithography evolution, the basic equations and concepts, and the understanding of the more mature technologies. In that way, the *EUV* is considered a natural consequence -the evolution- of the photolithography history, having a solid know-how of how is working now at the industry, but also a subjective inside in the tool manufacturers which can help to understand how the market will evolve.

When I first proposed the topic for this thesis that was the main goal, getting the overall picture and being able to provide it: it is said that when you explain something it is finally when you understand it. But not only this, also my intention was to research some alternatives at the current market, and the professor has proposed to do that with the *3D*-integration technology. Something that for me was quite new: I have sometimes heard about it but never worked or deepened into that. The goal thus was to understand the basics and see how mature the technology is, providing an objective and comprehensive knowledge that helps to grow a subjective point of view to “forecast” the technology roadmap. Information is power, therefore rather than saying that new technologies such as the *3D*-integration will never work on the market, first let us try to understand what is behind, the current limitations and the different market solutions, to later say how good or bad they will fit in our lives.

I expect that after writing -and reading- this thesis, talking about photolithography and *3D*-integration market trend will be based on facts and solid understanding of the basic concepts, rather than simply speculating without any criteria where the market goes.

1.2. Summary

The Moore's law has been driving the roadmap of the electronic manufacturing to reduce the transistor size, but now it seems about to hit their physical limitations. The main process that has allowed that progress is the photolithography, which consists on patterning by means of a light source into the wafer, thus creating the patterns in one layer which will form the transistors. The photolithography evolution through the history is key to understand the breakthroughs of today's industry. Describing the process concept, the physics and optics behind, allows to create a know-how of the standard lithography process, which is vital to understand the latest inventions by the tool manufacturers. From simple to complex, from standard to new, the concepts are being presented to lead to the two main technologies at the market: the immersion lithography and the *EUV* lithography. Those inventions are the responsible of keeping valid the Moore's law for the moment, being in different scales of maturity. The challenges to continue decreasing the patterning size are numerous, but the companies roadmaps are clearly defined to tackle those and keep on surprising the world with faster and smaller microchips.

On the other hand, other approach with a new process, called *3D*-manufacturing, is explored as an alternative to the conventional *2D*-manufacturing. By that emergent technology, wafers or tiers are vertically interconnected, thus decreasing the dissipated power and providing a solution to the current power increase. This approach is increasing the market share for some applications and sectors, which has the need to move into the *3D*-integration to find new or improved chip functionalities. Different alternatives are available at the market, having in common the main two processes: Through Silicon Vias forming and bonding. Their requirements, in terms of materials and process limitations, make the technology not yet implemented in mass production, but the good progress in the processes comprehension makes the *3D*-approach more than promising as an alternative, or maybe as an evolution, of the conventional photolithography-based circuit manufacturing.

3D-integration still needs from the photolithography process to form each circuit layer, but the enhancements of the lithography tool are not needed since the size is more limited by the specific integration processes. However, new alternatives at the market are appearing, which try to integrate both processes in the so-called *3D*-lithography, which consists on having lithography variants to print *3D*-patterns, not anymore only patterning one layer at a time. If that would work, the cycle time to manufacture a three dimensional-integrated circuit will drastically reduce and so, maybe, the *3D*-approach will become cost-wise effective to be used in serial production.

1.3. Goal

The ultimate goal of this thesis is to generate an opinion based on facts about the current status of the circuit manufacturing, particularly focused on the photolithography process, and how this one has overcome the challenges to be in its maturity phase currently with techniques such as immersion lithography. The future of the conventional lithography techniques is also discussed, particularly explaining why it is expected the usage of *EUV* lithography for the upcoming years and the current challenges of that technology. On the other hand, the conventional circuit manufacturing is expected to finish at some day, therefore an overview of one of the most appealing alternatives, the *3D*-integration, is discussed to keep the reader up to date with this potential solution, which would reduce the dissipated power and reduced the interconnect delays, among others. Researches about how lithography for generating 3D-patterns are included with the target of providing additional information of what the industry is considering as potential alternatives for the upcoming years.

To do so, an analysis of the historical evolution of photolithography is included, mainly pointing out the breakthroughs that allowed to continue the Moore's lay validity. The theory behind the process is also explained, highlighting the physics and optics nature of lithography tools. The remaining challenges for the upcoming years for the *EUV* are also discussed, thus providing the reader a view of what is the industry currently working on and how the process in some year is expected to be developed.

With regards to the *3D*-integration circuits, the goal is to provide a clear overview of which products and market segments may take advantage of its implementation. The main two processes, *TSV* formation and bonding are also described, since their understanding will allow the reader to figure out what the current challenges are and guess whether the technique may have a successful development in upcoming years. As information, the *3D*-lithography will provide the reader an interesting starting point for further investigations of novel techniques, which will enrich the knowledge and open the mind of the avid reader to look into different directions for the market evolution.

1.4. Scope

It is important to mention that this master thesis cannot cover the whole circuit manufacturing description, it is more aim to provide an overall vision of the cutting-edge for photolithography processes. Therefore, it is convenient to highlight what will be covered throughout the document and what will not be. It is **in scope**:

- Photolithography historic evolution
- Photolithography process description from physics and optics point of view
- Photolithography tool and process errors
- Photolithographic processes which enhances the accuracy, particularly focused on immersion lithography and *EUV* lithography
- Challenges for photolithography in the upcoming years
- *3D*-integration market and applications
- *TSV:* classification, process description and challenges
- Bonding: classification, process description and challenges
- *3D*-patterning by modulated lithography techniques examples and description
- Objective overview of what market trends
- Subjective opinion of present and future market trends

It is **not in scope**:

- Track processing description
- Overall circuit manufacturing flowchart
- Deepening on the transition from *2D* to *3D*-integration through the *2.5D*-interposers
- Simulations or validations of a *3D*-Integrated Circuit
- Design Rules for circuit manufacturing

1.5. Methodology

To successfully write this master thesis, the main task was to be based on the existing literature with the most up to-date papers and books to illustrate the current trends and challenges on the market. Since the University of Seville has some collaborations with important entities, *e.g.* the Society of Photographic Instrumentation Engineers (*SPIE*), and the online library allows the student to download some e-books, the collaborative work between the professor and the student consisted on looking for the right sources of information so that the student use the university rights to download the available documentation or the professor could send the student the information source via email.

Once that was available, the student has started to deep into the literature and then extract his own conclusions, which have been written in forms of a thesis previously having agreed with the professor about the content. The student has sent regularly his progress to the professor, who has quickly provided feedback about content and format, thus allowing the student for some improvements to achieve this final result.

To mention the usefulness of the online modality of the master, since otherwise the student could have not finished the thesis. The communication between professor and student have been via conference call (Skype) and email exchange, therefore a physical face-to-face was not needed (not possible either).

1.6. Planning

At the figure 4 an overview of the overall planning is shown by means of a Gantt chart. The planning shows also the presentation preparation, even when it has not been done at the moment of submitting the master thesis. The past dates represented are the real ones, trying to stick as much as possible to the reality, where some gaps can be seen due to holidays or other business tasks.

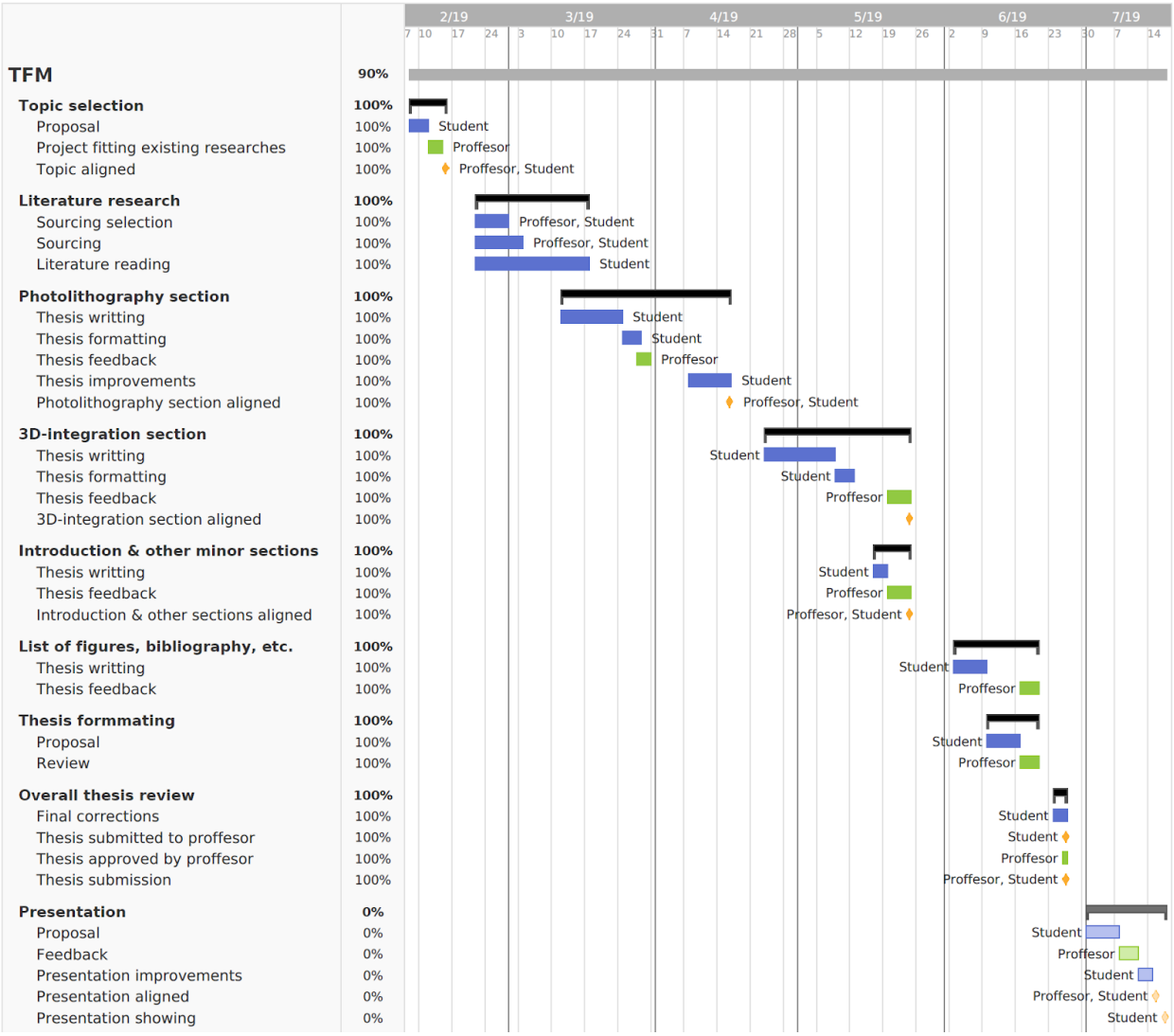


Figure 4: *Master thesis Gantt chart. Source: own, with Team Gantt tool.*

The total realization of the master thesis comprehends 12.0 *ECTS* which are equivalent to 300 hours. The total spent time at the whole master thesis by the student was approximately 97 days, with an average of 3 hours/day, thus making a total of approximately 291 hours (only by the student), which is within the budget. In terms of cost, since there was no finished products to provide and the access to all the literature has been granted through the university collaborations and internal sources, it was limited to the amount of working time.

2. State-of-the-art

Since the beginning of the circuits manufacturing, the key process to determine the performance of the chip was to perform the patterning, *i.e.* to replicate a predefined pattern into the circuit so that the different regions are created. This process, called photolithography, continues with the natural trend of doubling the transistor size every two years predicted by Gordon Moore, thanks to the manufacturer innovations to continue decreasing the pattern size. Despite the fact that this process seems to crash soon against physical limitations of the conventional physics, based on analysis of various reports, press announcements, news stories, and technical articles written in the past 20 years, it has been forecasted that the optical lithography can long until 2024 [7].

2.1. Process evolution

Up to the early 1970s, the most common process to perform the patterning was to use proximity printing or even printing by contact, in which blue and near UltraViolet (*UV)* light was passed through a photomask onto a photoresist-coated semiconductor substrate *[8]*. However, this fashion was replaced in the 1970s by the projection printing tools manufactured by Perkin-Elmer, the so-called Micralign projection aligners. The main difference for those tools was the performance enhancement, since they scan and image only a portion of the wafer, whereas the previous tools cover the whole wafer at the patterning, as shown in figure 5. Using this methodology, also the optical resolution was improved, since the printed details could be more specified having less field to expose.

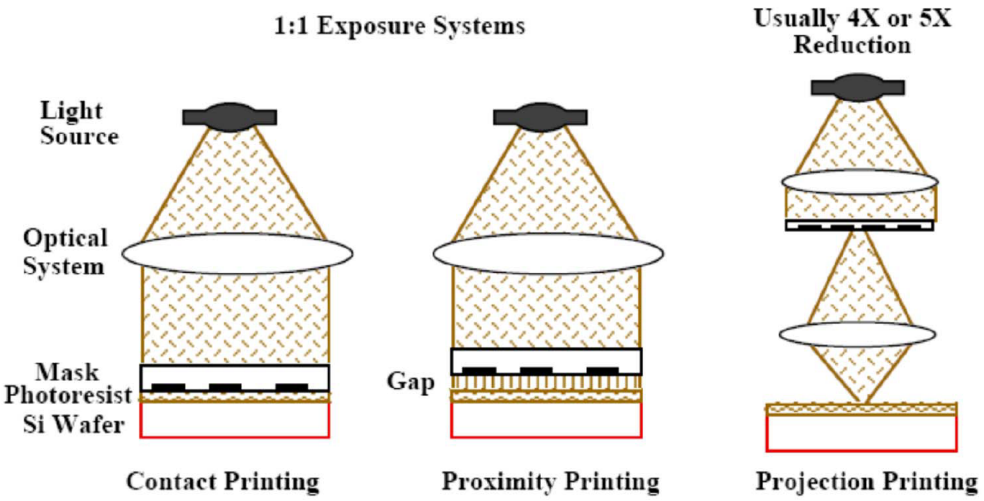


Figure 5: *Different approaches for printing tools [9].*

But the main breakthrough in terms of accuracy and performance happened in the early 1980s, where the **steppers** were introduced *[10]*. The revolution of those new systems was that only one single chip was patterned at a time, performing many times the “stepping-and-repeating” process to cover the whole wafer, which movement is easy to be understood by checking the stepper sketch in figure 6. This has a huge impact on the photomask (also called reticle throughout this thesis) and the lens, since the size of the first one could be enlarged whereas the lens would reduce the size (and thus the accuracy improves) by not augmenting the complexity of the reticle. Another implication of this new process is the improving overlay, in other words, the accuracy of a printed layer versus the previous one (how well they are stacked up), since the small printed areas are controlled independently from each other, allowing correction for wafer- and lens-induced distortion.

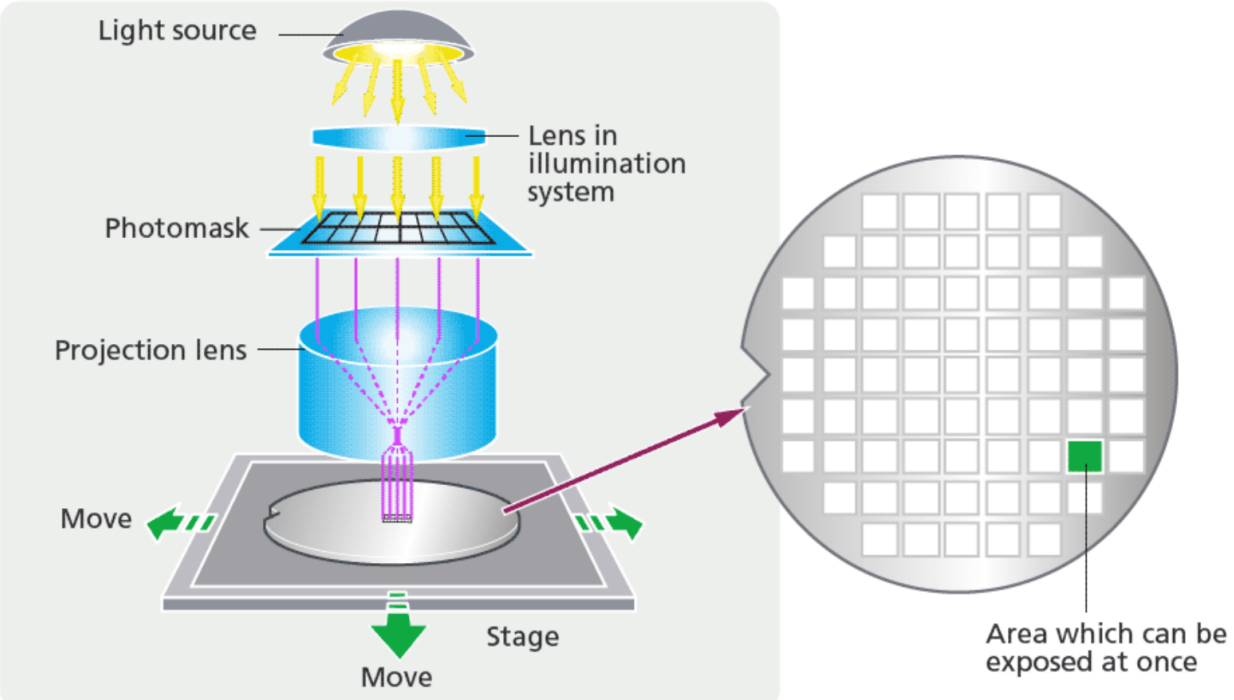


Figure 6: *Stepper sketch [11].*

So far it has been described the reticle movement (scanning) and the wafer movement (stepping), but what about mixing both methodologies? Well, that was the main idea introduced in the mid-1990s with the first tool Microscan by the manufacturer Silicon Valley Group, where both the reticle stage and the wafer stage moved at the same time, thus improving the accuracy and utmost the throughput of the tools. This is also called step-and-scan tool or simply scanner, which is nowadays the most common accepted strategy since it combines all the benefits of the previous invented processes.

2.2. Classification based on the source element

In terms of the element which creates the pattern, one differentiates between pattern generators and pattern replicators, which can be also subdivided depending on the source that they use, in accordance to figure 7.

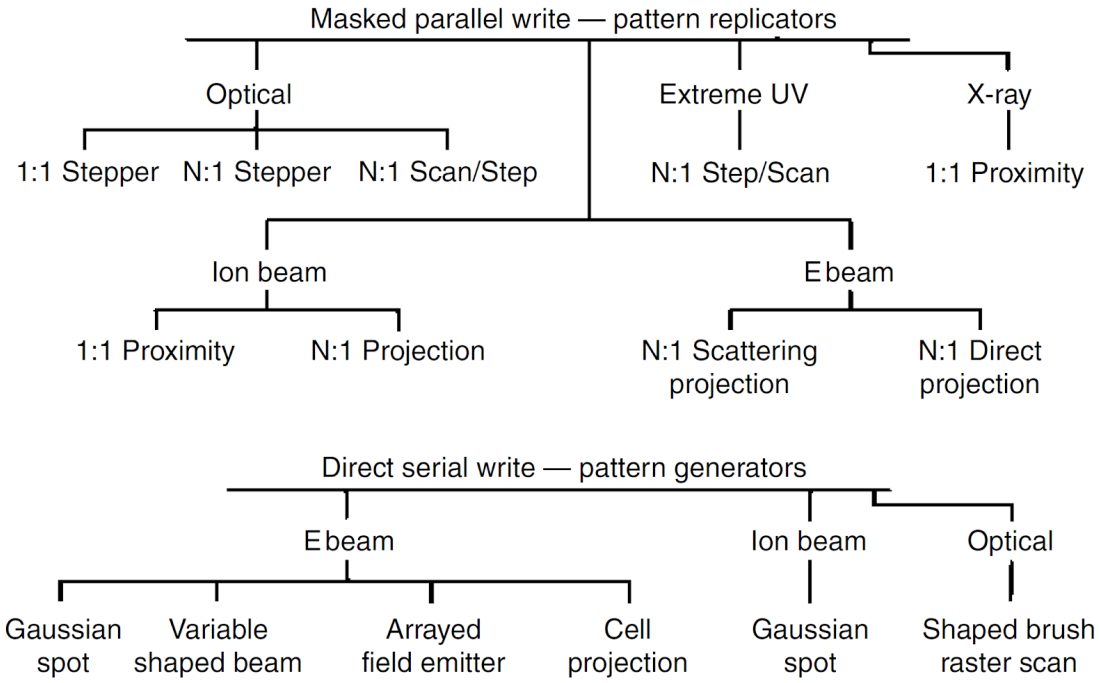


Figure 7: *Photolithography tool classification depending on the source element [12].*

-The **pattern generators** use as input data a database to directly create a physical image on the wafer. They utilize either charged particles or photons to create the image. The photomask fabrication is done with electron or photon beam tools, while the mask pattern defects are repaired with ion and photon beam tools. Their main disadvantage is the throughput (the speed to perform the process), only reaching one single 200 *mm*-wafer per hour, obviously not being that enough to cope with the actual chips demand.

-The **pattern replicators**, on the other hand, create a master pattern image in the form of a reticle and then replicate the pattern in a massively parallel fashion onto the wafer by means of a projection lens. A variety of image transfer techniques can be used, such as photons and charged particles, having a throughput -depending on the accuracy and extra software packages- on the range of 220-260 wafers/hour for a 300 *mm*-wafer size (one can imagine the amount of difference in terms of money of producing one versus 240 wafers/hour). The most common pattern transfer agent is a well-conditioned beam of monochromatic photons, whose wavelength is in the range of ultraviolet spectrum. The wavelength, in fact, has been decreased in the photolithography history to achieve greater resolution or, in other words, better accuracy

by reducing the pattern size. This has to do with the Rayleigh equation, which will be further explained in the main body of the thesis. Throughout the photolithography history, one can differentiate different element sources, each one with a corresponding wavelength.

- The most basic approach uses mercury as source (also called as *g*-line of mercury), with a 436 *nm*-light source.

- The second generation reduces the wavelength until **365 *nm***, being called the *i*-line of mercury.

- The main change in terms of the source was to introduce the excimer lasers to replace the High Pressure lamps of mercury, having then very high intensity and a narrower bandwidth, thus reaching the **248 *nm* wavelength** using Krypton Fluoride (*KrF*) as source element. This light wavelength -and the following generations with even smaller λ- is already at the ultraviolet region, which spectrum is shown in figure 8.

- The fourth generation uses an Argon Fluoride (*ArF*) excimer laser, with a wavelength of **193 *nm***.

- Some trends researched to go down to a source of 157 *nm* with Calcium Fluoride (CaF_2) as lens material. However, it needs as required environment the vacuum, and the CaF_2 large intrinsic birefringence complicates the design and manufacturing of high-quality optical lenses *[13]*.

- The previous three sources are in the region of the Deep UltraViolet (*DUV*), whereas the new breakthroughs use vacuum and Extreme UltraViolet (*EUV*) light, reducing the wavelength to an impressive 13 *nm* (**13.5 *nm*** indeed).

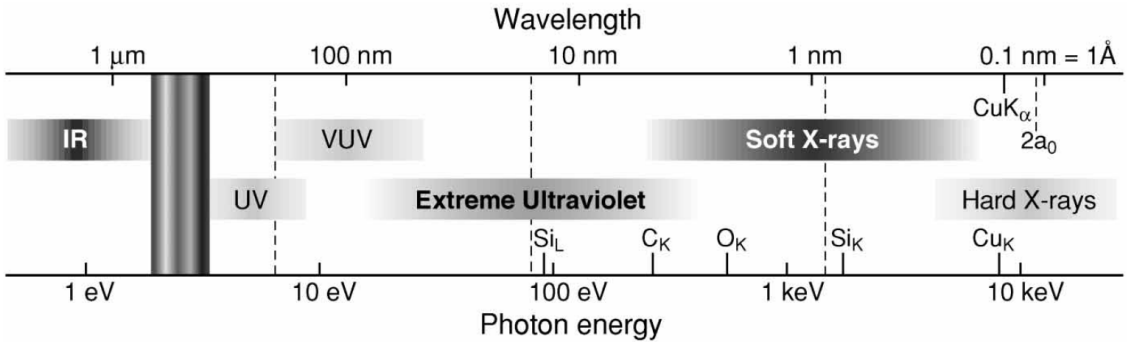


Figure 8: *Ultraviolet light spectrum [14].*

The resolution of each generation has been improved by techniques which will be discussed in the body of this thesis, but one can already observe the correspondence between decreasing the wavelength with the improvement in resolution (the minimum feature size is reduced). The table 1 establishes the correspondence between the light source wavelength and the minimum feature size achieved with that lithography tool.

Table 1: *Patterning resolution and photolithography source wavelength [14].*

Minimum feature size (nm)	7000–1000	1000–350	350–180	180–32	32 and below
Lithography wavelength (nm)	436 (G-line)	365 (I-line)	248 (DUV)	193 (DUV)	13 (EUV)

2.3. Market trends and cutting-edge

The outstanding evolution of the photolithography, with impressive breakthroughs as the immersion lithography and now the *EUV* lithography, is continuing to reduce the pattern size. At the figure 9 the trend can be easily identified, reducing from a pattern of 1.5 microns (*μm*) in the early eighties, until the current 7 *nm*:

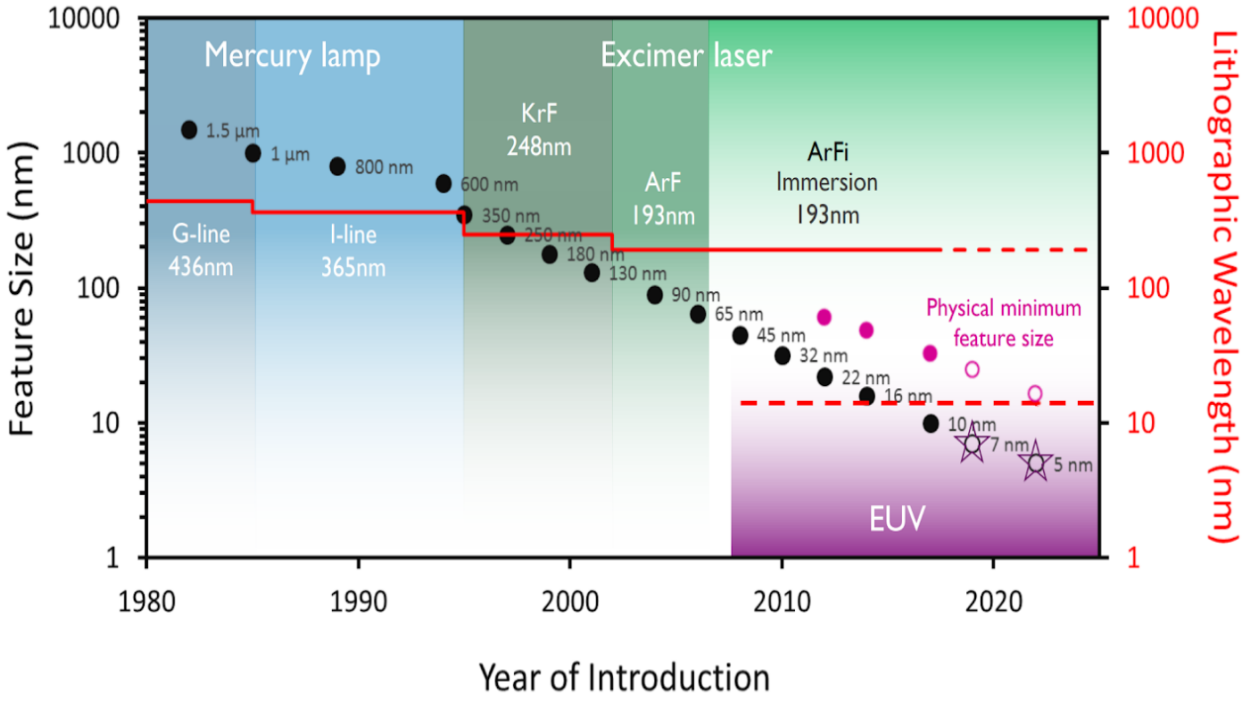


Figure 9: *Resolution and wavelength trends in lithography [15].*

The trend is clear: the Moore's law remains applicable. Every time the microprocessor scaling trend was about to be cut off, anyhow new inventions -such as the *EUV* lithography- came up to continue reducing the patterning size, as sketched in figure 10. But what about the future? Well, the Numerical Aperture (*NA*) of the lens, which defines how good is the resolution at the printed pattern, has become a clear limitation: if the *NA* cannot be further improved (increased) for *EUV*, it is expected to reach a theoretical limitation at 3 *nm*. New devices, such as the Complementary Field-Effect Transistors (*CFETs*) or the Vertical Field-Effect Transistors (*VFETs*), or the integration of three-dimensional (*3D*)-logic at *EUV* lithography with higher *NA*, can make the Moore's law still valid with the von Neumann architecture.

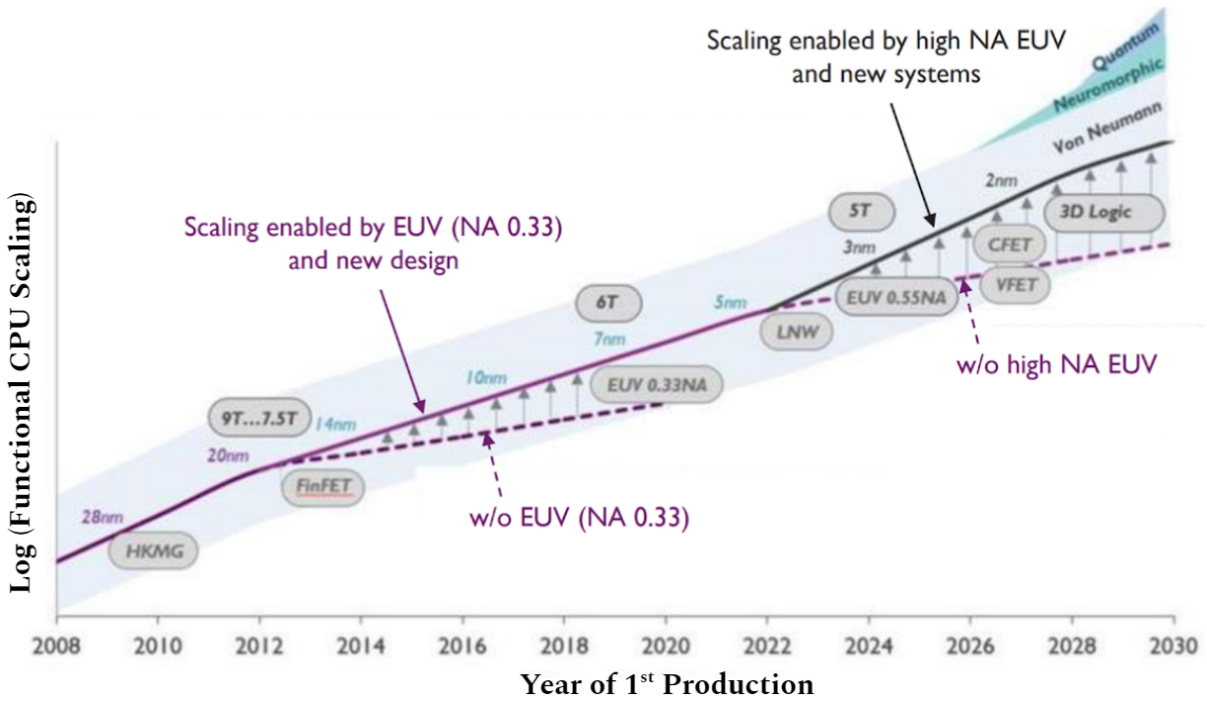


Figure 10: *Microprocessors scaling timeline [16].*

What is currently in the market? The leading foundries are in mass production using both dry and wet tools (for the most demanding applications). Dry tools are the conventional ones, thus using air surrounding the lens, whereas the wet tools uses water to improve the resolution of the system even further.

But the revolution does not stop there: the transition into the *EUV* lithography is a reality: Samsung is using now the *EUV* light as source to manufacture nodes with 7 *nm* sizes, and it is rumoured *[17]* that their cell phones for 2021 will include a 3 *nm*-technology node.

The main manufacturer for microprocessors at the cell phone industry, the Taiwan Semiconductor Manufacturing Company (*TSMC*), is more than certain *[17]* of reducing their pattern size from their current 7 *nm* to 5 *nm*-nodes for the new iPhone to be released in 2020.

At the computer microprocessors, Intel is taking a more safe approach since Global Foundries is not going to use *EUV* in the near future. Intel current nodes of 14 *nm* are expected *[18]* to shift into *EUV* lithography by mid-2021, when they expect to introduce at the market a 7 *nm*-node.

Other foundries are not using the *EUV* yet (the cost of the tools is hundreds of million euros), since not all the market needs the ultra high accuracy of that technology. Even if a circuit requires that precision in the critical layers, conventional production lines accomplish multiple photolithography tools for different patterning sizes.

2.4. Physical limitations

Even with all the advances in lithography, the current manufacturing process as we know it nowadays must finish some day. The semiconductors physics applied to devices of few nanometers is no longer valid, but **quantum physics** has to be considered as well. The physical limitations are almost there:

- **High electrics fields:** they can create avalanche processes increasing the current passing through the transistor, and thus getting to a chip malfunctioning.

- **Interconnection delays:** the parasitic *RC*-network effect is huge for small dimensions, thus having problems with the signal integrity to operate at high frequencies.

- **Heat/power dissipation:** the faster the microchip, the more power is dissipated. The figure 11 illustrates that trend, showing that for smaller interconnect delays, the power is increased. Even using very powerful fans the generated heat it is a well-known issue, such as the incident with the batteries for the cell phone Samsung Galaxy Note 7. The only real solution is to completely rethink chip packaging and cooling, for instance having microfluidic channels that increase the effective surface area for heat transfer *[19]*. The power dissipation is one of the main bottlenecks for keeping on scaling the transistor size, thus the market looking already for packages alternatives such as the *3D*-integration. In fact, even when that approach is considered as a potential alternative to mitigate the issue, the heat dissipation at each individual layer remains as one of the major headaches of the industry.

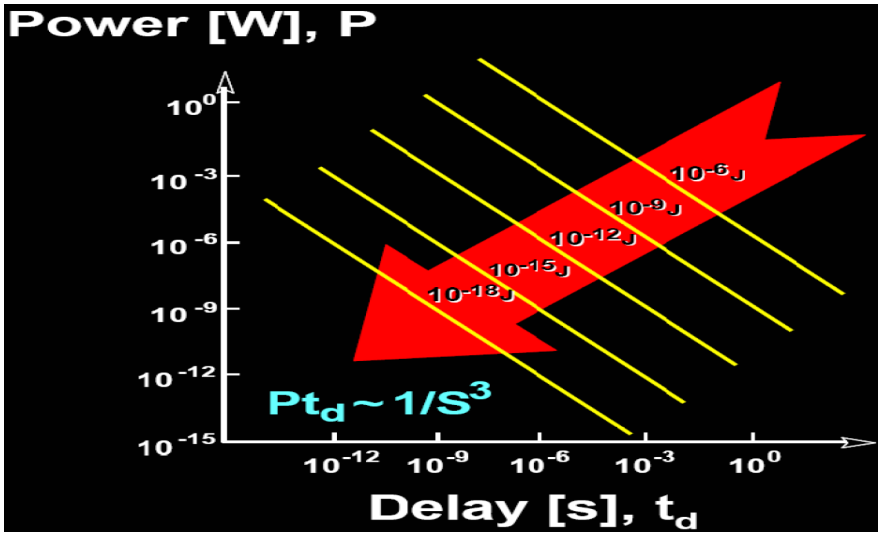


Figure 11: *Dissipated power for different interconnect delays [20].*

- **Non-uniform doping:** due to the small dimensions it is very difficult to control the amount of free electrons and electron holes. Obviously that affects the transistor performance and may drive to a failing device.

- **Oxide thickness:** the oxide thickness of the Metal Oxide Semiconductor Field Effect Transistor (*MOSFET*) determines the size and the leakage current of the transistor, which is approaching atomic levels, thus imposing a practical bound on the leakage current and hence limits transistor sizes [21, 22]. In fact, the maximum current per cross-sectional area generated by the transistor is inversely proportional to the oxide thickness, clearly showing that for small oxide thicknesses, the transistor current will reach an upper limit. The reduced oxide-thickness may also lead to the tunnel-effect at the transistor's gates.

- **Reliability and fault tolerance:** with decreasing size, some threats may affect the transistor life. Leakages are present at the nanometer level, particularly the gate and subthreshold leakage, since the transistor channel can no longer contain the electrical current for small dimensions. The device parameters utilized for modelling may also fluctuate, thus causing the device to fail unexpectedly. The signal integrity is also degraded for high-speed and high-integrated circuits due to the coupling, power-supply noise or the propagation delays.

The physical limitations are just referred to the devices themselves. But one has to think also about the manufacturing limitations: the cost to set up a foundry is exponentially increasing, thus posing a threat to the fiability of future technology scaling [23]. And obviously the cost of having less yield due to the beforehand reasons may cause a circuit manufacturing not to be cost-wise efficient. Every device limitation can be translated into extra money for the foundry to tackle the issue: from design and validation, passing by the cost of the equipment, and of course to the non-quality cost associated to devices malfunctioning. The table 2 summarizes the constraints at different levels threatening further development of the Moore's law.

Table 2: *The Moore's law limits [24].*

Limits	Engineering	Design and Validation	Energy, time	Space, time	Information, Complexity
Funda-mental	Abbe (diffraction) Amdahl Gustafson	Error-corr. & dense codes Fault-tolerance thresholds	Einstein $E=mc^2$ Heisenberg $\Delta E \Delta t$ Landauer kT ln2 Bremermann Adiabatic thrms	Speed of light Planck scale Bekenstein Fisher $T(n)^{1/(d+1)}$	Shannon Holevo NC, NP, #P Turing (decidability)
Mate-rial	Dielectric constant Carrier mobility Surface morphology Fabrication-related	Analytical & numerical modeling	Conductivity Permittivity Bandgap Heat flow	Propagation speed Atomic spacing No gravitational collapse	Information transfer between carriers
Device	Gate dielectric Channel charge ctrl Leakage, Latency Crosstalk, Aging	Compact modeling Parameter selection	CMOS, quantum Charge-centric Signal to noise Energy conversion	Entropy density Entropy flow Interfaces & contacts Size & delay variation	Universality
Circuit	Delay, Inductance Thermal-related Yield, Reliability, IO	Interconnect Test Validation	Dark, darker, dim and gray silicon Cooling efficiency Power density/supply	Interconnect 2D or 3D	Circuit complexity bounds
System +SW	Specification, Implementation Validation, Cost		Synchronization, Physical integration Parallelism, *Ab initio* limits (Lloyd)		The CAP theorem

2.5. Alternatives

Due to the physical limitations -and maybe due to the market dominance of the photolithography processes-, researches and small/medium companies have decided to go in different directions. It seems that in the current future, **new technologies** (such as spintronics [25]) **and/or different materials** (*GaAs*, carbon nanotubes, etc.) might be used: quantum dots [26] or neuromorphic networks can be some solutions to continue decreasing the size, not anymore using the photolithography and -maybe- without the silicon-based wafers that we know so far. A summary of the alternatives with regards to technologies and materials is plotted in figure 12.

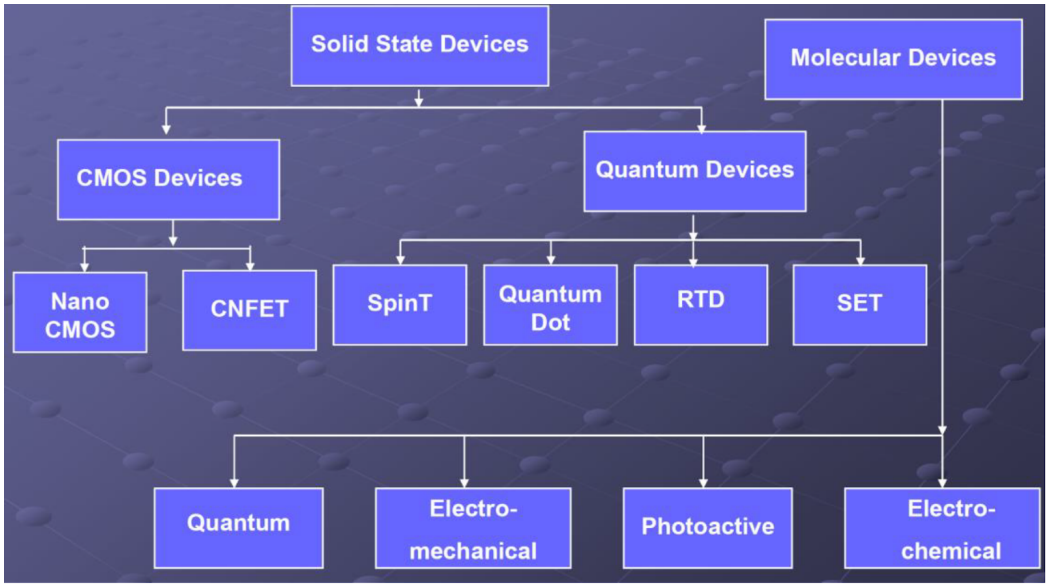


Figure 12: *New technologies and materials roadmap [20].*

On the other hand, there is a totally different approach that will be addressed throughout this thesis, which is to integrate the conventional circuit in three dimensions. The also known as three-dimensional integrated circuits (*3D-IC*s) integrate multiple functional *IC* chips vertically, instead of packing a single chip or multiple chips into a *2D* package, as the figure 13 suggests. The different chips are made at different layers, also known as tiers, being connected by vias which makes the connection between the different levels [27].

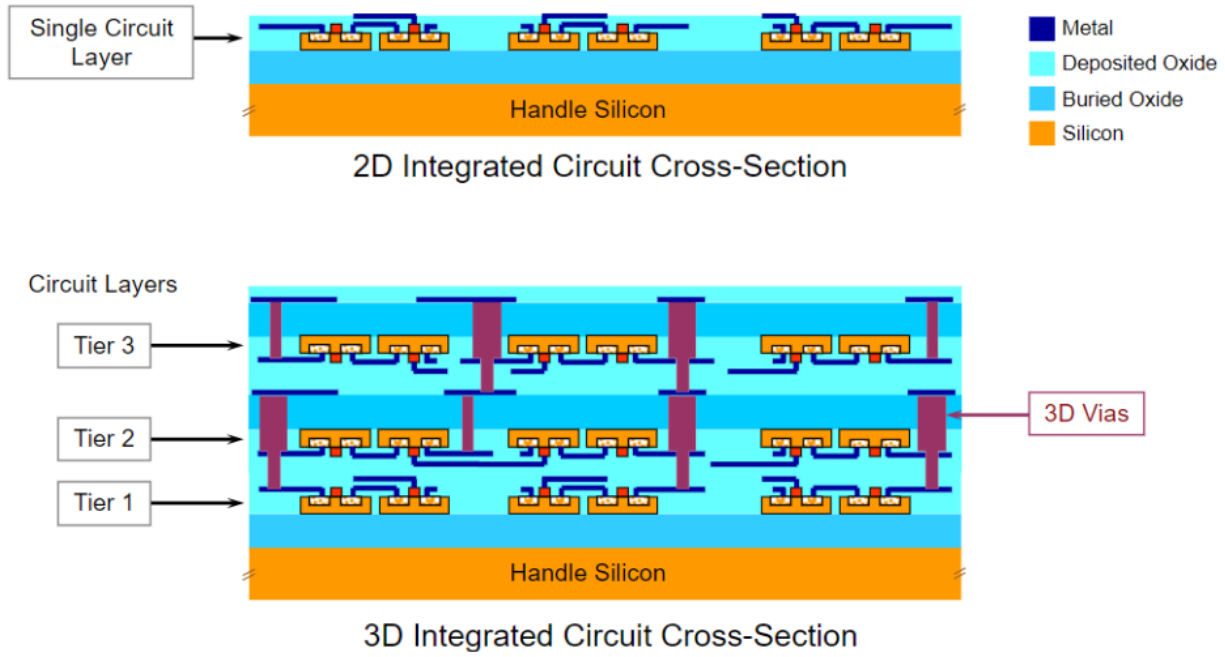


Figure 13: *2D vs. 3D-Integrated Circuits cross section [28].*

The advantages of this new technology is that it enables heterogeneous integration of materials, processes and functional *IC* chips *[29]*. In addition to that, the length of the longest interconnects across an integrated circuit is drastically decreased, thus offering unique opportunities for highly heterogeneous and multifunctional systems *[30]*. *3D-IC* technology is not only capable of increase device-density [31], but also offers heterogeneous integration of dies from disparate technologies (analog, digital, mixed signal, sensors, antenna and power storage) and from different technology nodes (65, 32, 22 *nm*, etc.). Other advantages *[32]* versus the traditional Systems on a Chip (*SoC*s) are shown in figure 14, which include lower cost (if High Volume Manufacturing implemented), flexibility by manufacturing different devices by different organizations and higher performance, without unnecessary costs or yield losses due to complexity of simultaneous processing or need to increase silicon space to horizontally accommodate all the devices. On the other hand, also *3D*-integration faces some challenges: current manufacturing cost, lack of design availability, lack of *DRAM* stack availability and thermal management (being the latest the reason why the most-consuming tiers are usually placed at both sides of the whole stacking) .

The question is now: is the *3D*-integration the evolution of traditional methodologies or a revolution which will replace it?

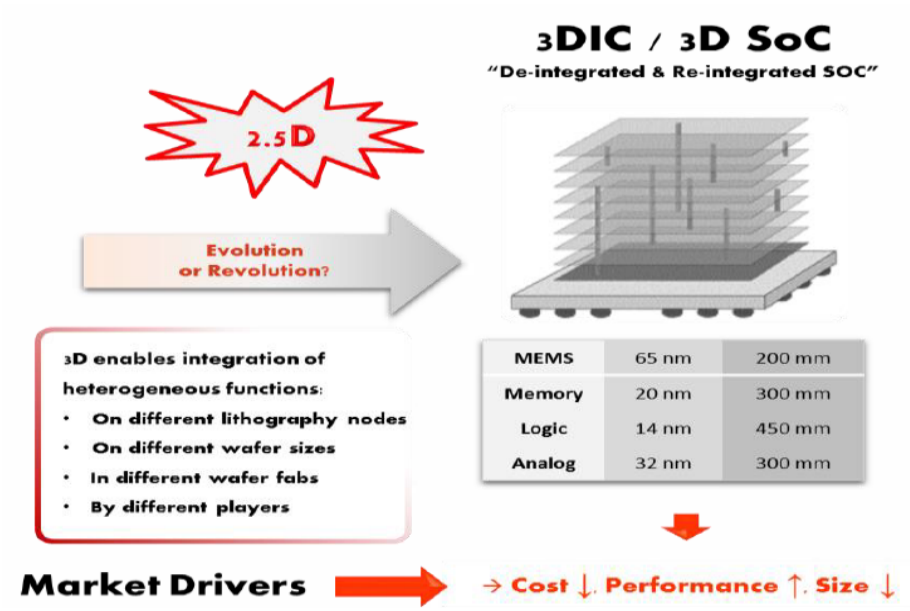


Figure 14: *3D-ICs advantages [33].*

3. Body

The main focus of this thesis is the photolithography process, which will cover the main section of the thesis.

Firstly, the process will be described using the Rayleigh equations as starting-point, thus providing the reader the basic physics behind to fully understand the core process. As photolithography is also called optical lithography, an extensive section about optics is needed: the lens behaviour will be explained and the main issues, the optical aberrations, will be addressed and described.

Once the basic concepts have been developed, the main Key Performance Indicator (*KPI*) for the process will be mentioned: the overlay. That figure will be fully explained and, the most important thing, the contributors to its potential failures will be described. The reader may then, by just reading the alignment and overlay subsection, come up with a critical perception of what the basic troubleshooting in moderne circuit manufacturing looks like. A small section about the photolithography tool throughput is also included, trying to convey the approach on the current industry of not only caring about quality but also time and cost.

To finish up the lithography part, an interesting section about the current trends to improve accuracy is added. The idea is to provide an understandable overview of the latest breakthroughs in the process, so that basic know-how of the latests techniques in circuit manufacturing is acquired. Concretely, based on the Rayleigh equations, advances in three fields will be distinguished: working on reducing the Rayleigh constant, increasing the Numerical Aperture and reducing the source wavelength, all of them with the goal of reducing the patterning size.

As mentioned in the introduction, even if the photolithography is the mainstream at the market, potential new solutions need to be used, therefore a different part of the thesis will review the *3D*-integration of the circuits as a serious alternative to the conventional *2D* manufacturing.

With respect to the *3D*-approach, the reader will be firstly presented the market and applications. After that, the main two processes will be described: the Through Silicon Vias (*TSV*s) formation and the bonding. Each process will be firstly described, continuing by highlighting their advantages versus the traditional *2D*-circuits (using photolithography). The cutting-edge of the two processes will be also shown, with a research in the latest applications and market trends.

Despite the fact that both trends seem to work in different directions, *i.e.* lithography on reducing the patterning size and *3D* in reducing the dissipated power, the *3D*-Integrated Circuits need of photolithography process for manufacturing, but not the latest techniques with the best accuracy. However, what would happen if the solution for the future is to combine both techniques to reduce cycle time and cost for *3D*-circuits manufacturing? The last part of the thesis body will research about different novel techniques which are trying to merge both techniques.

3.1. Photolithography

Photolithography is the process of defining useful shapes on the surface of a wafer, thus creating the different regions where the physics will act -by means of electrons/holes balance- by building different functionalities and, in the end, composing the whole semiconductor device. The main component for the process is the reticle, which has the patterns to be printed into the substrate, also called wafer.

The **reticle** (also called photomask) is depicted in figure 15, being an opaque element with a "written" pattern on it. It consists of a thin sheet with some holes which allows the light to pass through, thus replicating the patterns into the wafer. As the reticle will be used to generate million of Integrated Circuits (*IC*s), one can imagine that if some contamination is found on it, the result will be that the patterned circuits will be wrong, therefore utmost cleanliness of the photolithography tool and, in particular, of the reticle, is mandatory for the circuit manufacturing. To ensure that, a transparent polymer film known as pellicle, protects the printed pattern.

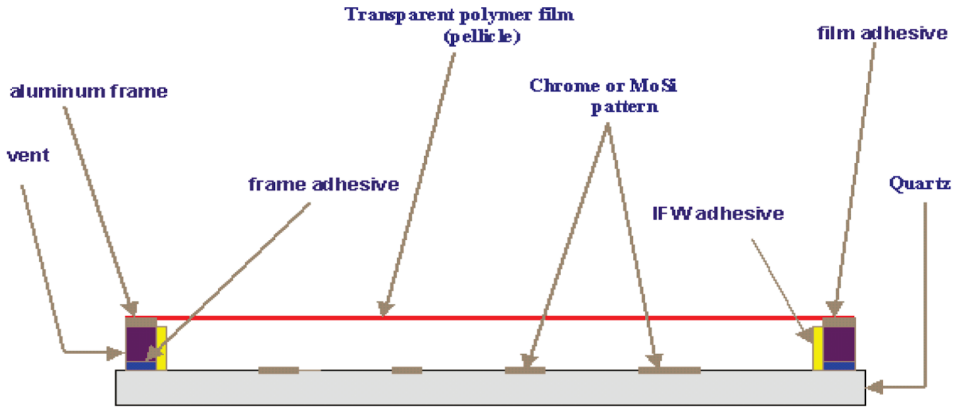


Figure 15: *Reticle with pellicle and its rest of components [34].*

Not only perfection in terms of cleanliness for the reticle handling is needed but also, due to the fact that they are light sensitive, the lighting used at the clean rooms needs to be yellow (not absorbed by the reticle) in order to avoid chemical reactions with the film which may alter the pattern.

If handling and preservation are critical for the reticle life, one can also infer that the reticles manufacturing has to be at utmost perfection (in terms of accuracy) and taking into account the "well-known" issues which have been learned by trial-error and complex studies, therefore Design Rules (*DR*s) are common in its manufacturing. Reticle cost is therefore very expensive (not talking about its manufacturing lead times), thus being considered by the foundries as "holy" reticles.

A **wafer**, a thin slice of semiconductor *e.g.* crystalline silicon, whose conductivity properties are explained with the energy levels, which represents the silicon -and other semiconductors- as quantized levels of energy forming energy bands. One can differentiate between the conduction and the valence band, which represents the first and the last energy band to be filled by electrons, respectively *[35]*. Between them it appears the bandgap, where the electrons are forbidden to stay due to their energy. The difference in terms of energy between the conduction and the valence band represents the bandgap energy. An electron can step between levels if its energy is greater than the bandgap energy of the material. The energy is calculated with the Planck's equation, where *h* represents Planck's constant and *f* the incident light frequency, which is also related to *c* (the light speed in vacuum) and *lambda* (the light wavelength).

$$E = h\gamma = h\frac{c}{\lambda} \qquad (3.1.1)$$

On this way, a balance between generated electrons-holes can be chemically -artificially- implemented, where the properties of the silicon makes it ideal to build the electronics that is nowadays used.

The wafer is coated (covered) by a photosensitive material known as **photoresist**, which is an organic material which consists of a polymer base resin with additional components to provide photosensitivity and other properties. Its sensitivity range has to match the wavelength of the light source, thus absorbing only that wavelength allowing the pattern to trespass the coating, so that the pattern is replicated onto the wafer.

The main photoresist figures of merit are the resolution, the process latitudes and the reactive ion etch resistance. The previous features are also photolithography tool-dependent, therefore every change in the process parameters will affect the exposure, as well as using a different coating for the wafers *[36]*. Additional intrinsic parameters for the photoresist are the sensitivity, the compatibility with industrial standard developers, the adhesion to the substrate, the environmental stability and the shelf life. Obviously each generation of the photolithography process has implied a matching counterpart in the used photoresist, which is summarized at the figure 16.

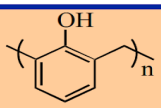
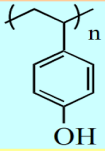
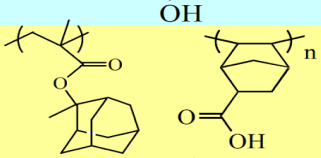
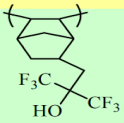
Technology Node	Exposure Technology	Polymer Platform
0.8 - 0.35 um	I-Line (365nm)	
0.25 - 0.15 um	DUV (248nm)	
130 - 65 nm	DUV (193nm)	
45 - 32 nm	DUV (157nm)	
= 25 nm	EUV (13nm)	?

Figure 16: *Major polymer platforms for the different photolithography generations [36].*

3.1.a. Physics

The main physical property behind the photolithography is the use of the wave nature of the light. Its wavelength (λ) is related to the projection system (defined by the Numerical Aperture *NA*, the Resolution *R* and the Depth of Focus *DoF*) by means of two constants: k_1 (Rayleigh Resolution) and k_2 (Rayleigh Depth of Focus). The basic relationships are known as **Rayleigh equations**, thus defining the Resolution and the *DoF* as follows:

$$R = k_1 \frac{\lambda}{NA} \qquad (3.1.a.1)$$

$$DoF = k_2 \frac{\lambda}{NA^2} = \frac{k_2}{{k_1}^2} * \frac{R^2}{\lambda} \qquad (3.1.a.2)$$

- The **Numerical Aperture** is defined as:

$$NA = N * sin(\theta) \qquad (3.1.a.3)$$

  where *n* is the index of refraction of the medium surrounding the lens (in case of vacuum will be 1 and for air it is usually simplified to 1). It is a dimensionless number that measures the ability to gather light and to resolve fine specimen detail while working at a fixed object (or specimen) distance *[37]*.

- The **Resolution** defines the ability to distinguish different components within a group of objects.
- The **Depth of Focus** (*DoF*) determines the tolerance of the distance between the lens and the wafer which can be modified in order to still achieve a correct patterning process.

Using those basic equations, the figures of table 3 are obtained for the different photolithography technologies:

Table 3: *Basic relationships on photolithography technology generations. Source: own, based on [12].*

Light source	Light wavelength [*nm*]	*NA*	k_1	Resolution [*nm*]	*DoF* [*nm*]
i-line (*Hg*)	365	0.62	0.48	280	950
KrF	248	0.82	0.36	110	370
ArF	193	0.92	0.41	65	230
KrF_2	157	0.85	0.41	57	220

When the maximum angle of the light rays is relatively small or, in other words, when the *NA* is small, *sin (Θ)* can be considered to be simply *Θ*. For larger angles and values of the Numerical Aperture, the error in using this simple approximation grows unacceptably large *[38]*, thus becoming the Rayleigh equations for large angles:

$$R = k_1 \frac{\lambda}{\sin(\theta)} \qquad (3.1.a.4)$$

$$DoF = k_3 \frac{\lambda}{sin^2\left(\frac{\theta}{2}\right)} \qquad (3.1.a.5)$$

To finish up the physics analysis, let us remark that so far we have considered that all the light is passing through the space defined by the Numerical Aperture of the lens, without having any attenuation. However, in an actual projection imaging process, the simple copy of the reticle pattern is not achieved, but some diffractions and imperfections appear in the projection system, since the projected image is altered as shown at the figure 17 on the right hand side.

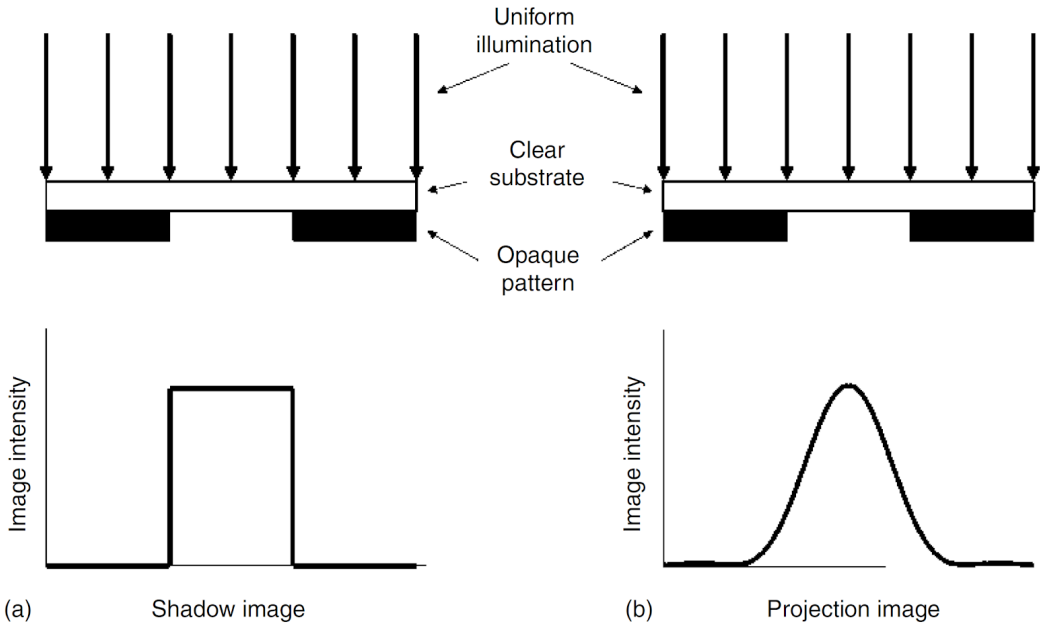


Figure 17: *Projection image. (a) Ideal situation. (b) Diffraction-broadened projection imaging [12].*

The spreading of the image profile has been deeply investigated for the last two centuries, thus concluding that it is a consequence of the wave nature of the light and thus effectively limits the resolution capability of the optical imaging systems. Its characteristic was well studied by G.B. Airy, who first plotted in 1835 *[39]* the dependence on the intensity with respect to the distance *x* between the object and the image, with a defined pattern illustrated at the figure 18.

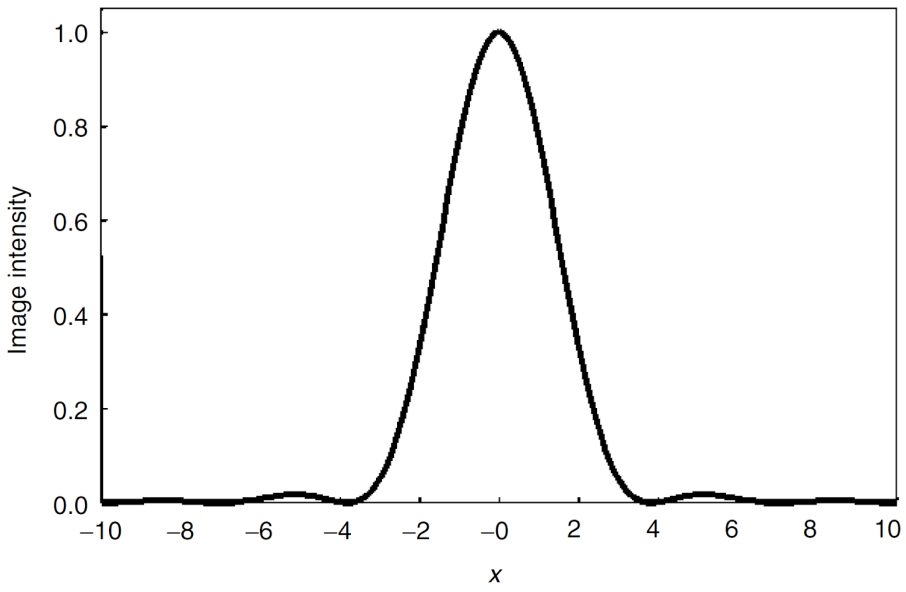


Figure 18: *Light intensity distribution from a point source projected through a circular imaging lens [12].*

3.1.b. Optics: lens components, aberrations

The key component for the "magic" to happen is the **projection lens**: its goal is to replicate a pattern into the wafer. Usually it reduces the size of the image -by a factor of 4:1 nowadays *[40]*- and costs the most in the lithography tool (a couple of millions euro), therefore only the main optics manufacturer (such as Nikon, Canon or Zeiss) are in the lead for its manufacturing.

Mainly contributor of the patterning resolution, the design of the lens is based on projection principles. The pattern printed on the reticle will be passed through the lens, being the light rays distributed in a conical shape to converge in the image plane, *i.e.* where the image is located, in case of the photolithography the wafer surface. The conventional lens has a circular shape, and can be very easily plotted with a basic schematic such the figure 19.

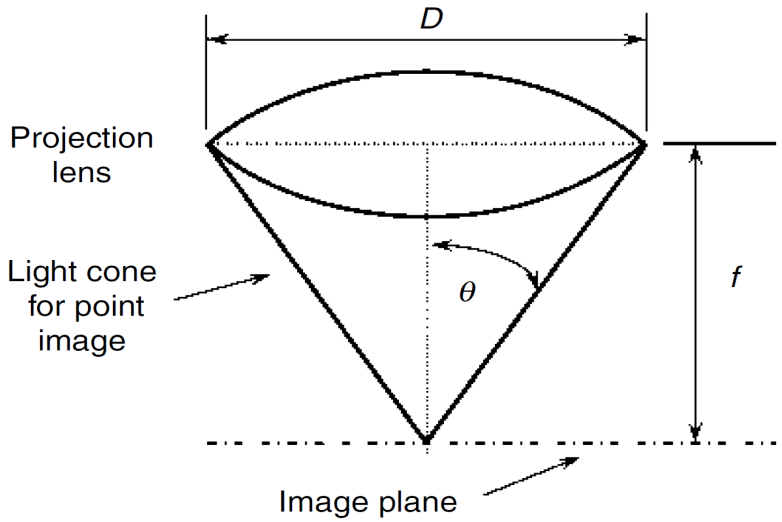


Figure 19: *Projection lens basic sketch [12].*

Some elements are highlighted:

- **Diameter** *D*: will impact the accuracy on the patterning. It has to be designed in accordance to the reticle size too.
- **Focal distance** *f*: it is the distance between the lens itself and the image plane, which in photolithography is the surface of the wafer.
- **Angle** *Θ*: it defines the *NA* of the lens, which will have a direct impact on the accuracy. The empirical meaning is that the *NA* is a feature to understand how many light rays (light orders) may pass through the lens, thus allowing the light to be printed onto the wafer. Therefore, the greater the *NA*, the better the resolution, since more orders of lights can traverse through the lens to recompose the image at the image plane.

While the previous analysis the reader may have got acquainted with the basic concepts of optics, the conventional lens used in optical lithography are much more complex that a simple mirror though. In particular, the lens has to control the Critical Dimension (*CD*), alignment (overlay), reticle errors and many other details. But in addition to that, the lens can be breakdown into multiple mirrors: it is not just a thin piece of glass anymore. It is beyond the scope of this thesis to deep into the optics breakdown, since the focus is more oriented to the potential issues that the lens can introduce (*e.g.* optical aberrations), rather than the whole light ray-study traversing all the mirrors to reshape the original pattern. The **optical aberration** can then be defined for photolithography as a flaw or distortion in the patterned image (at the wafer level) versus the original image at the reticle, being generated by the optical lens.

Nevertheless, it will be pointed out that the mainstream at the industry is using refractive imaging lens working at a monochromatic wavelength. To build it up, up to 30 separate lens elements are used *[41]* with the goal of reducing the aberrations to less than 1% of the wavelength, having evolved the complexity through the main technology nodes. The figure 20 shows the complexity evolution throughout the years.

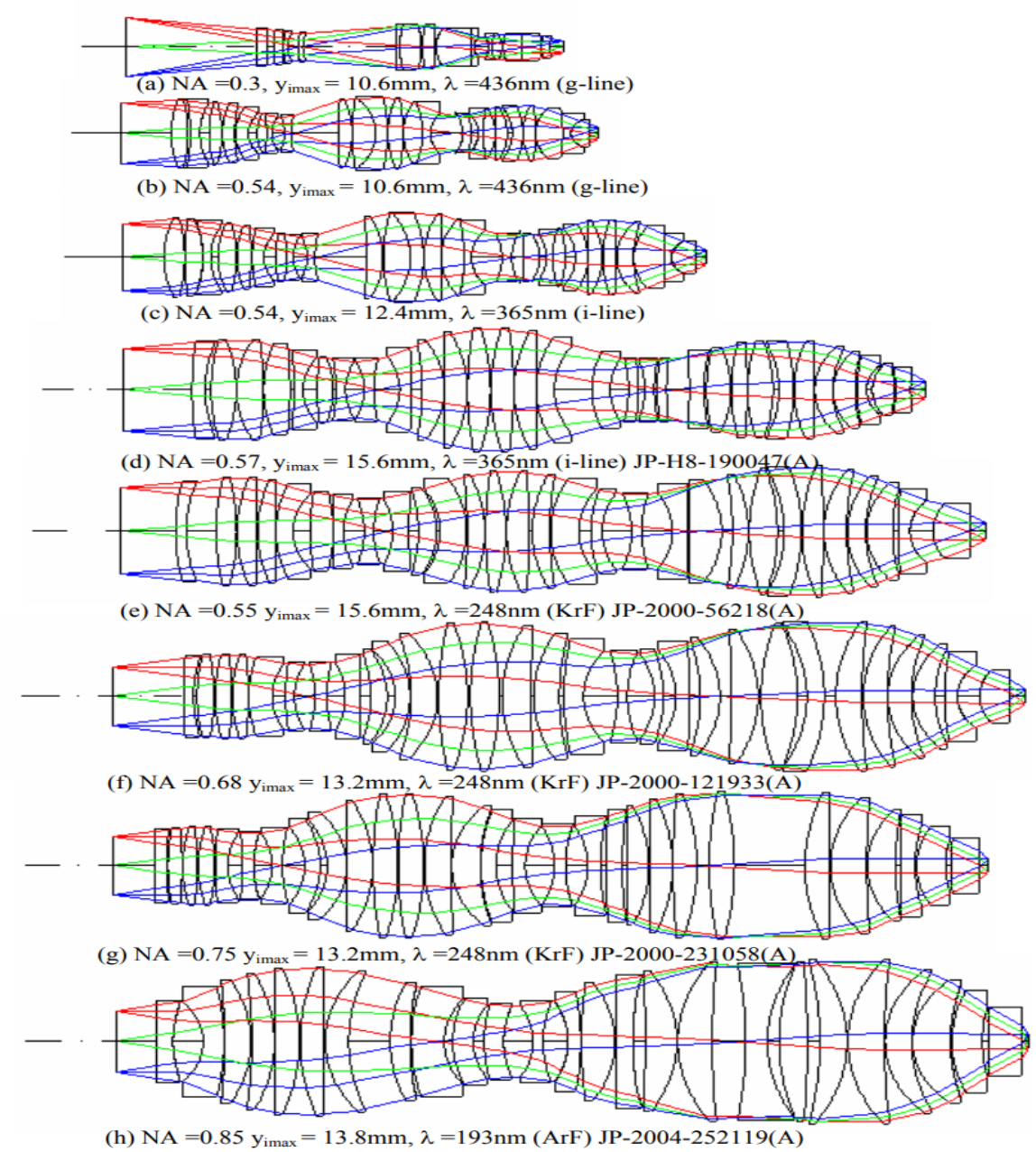


Figure 20: *Optical configurations for different photolithography generations [41].*

It has been already mentioned before the main issues on the lens: the aberrations. How do they affect the patterning process? To answer this question, one has to talk first about the wavefront, which is shown at the figure 21, being defined as the surface over which an optical disturbance has a constant phase. In addition to that, the rays are defined as lines normal to the wavefronts at every point of intersection *[42]*.

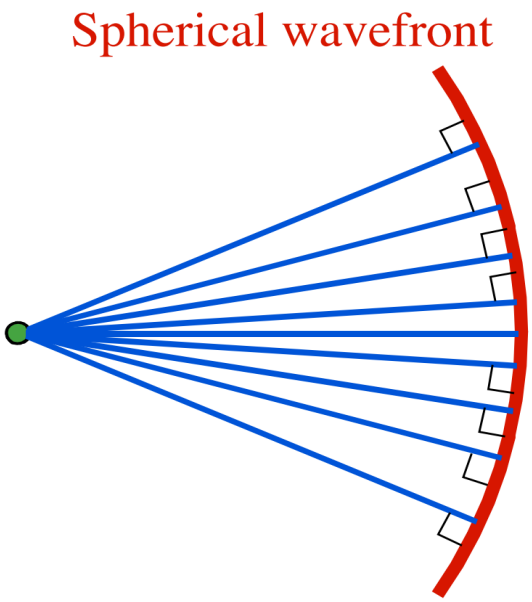


Figure 21: *Rays and wavefront at a spherical lens [42].*

One simple definition of the aberrations effect would be that they change the wavefront of the light. One step higher in terms of complexity, the aberrations causes differences versus the expected mathematical approach defined by paraxial optics for small angles [43], since the light rays are not converging at a unique focal point, but rather spread out over a region of space.

It is out of scope to study the root cause of the aberrations, although the reader is encouraged to read further researches [44, 45] about the design and manufacturing causes.

The classic primary aberrations were first analyzed by Seidel in the mid-nineteenth century *[46]*, and can be classified, depending on their produced effects, on unclear image (spherical, coma and astigmatism) or deformation of image (field curvature and distortion). They all are considered as monochromatic aberrations, since the light source has a unique wavelength (as the one used in photolithography) in opposition to the chromatic aberrations, which are no further discussed in this thesis since are not within the photolithography scope. Let us try to understand what are the differences between them, as well as their effects in terms of produced image.

- The **sphericals aberrations** are described as an imaging defect consisting on having a different focal position of the imaging rays traversing through the center of the projection lens aperture versus the focal position of the rays traversing near the edge of the aperture. The non-converging rays are shown at the figure 22 for better understanding. The resulting image has lower contrast (it is blurred) than the original pattern, and the focal plane position will change for slight differences of the projection lens *NA*.

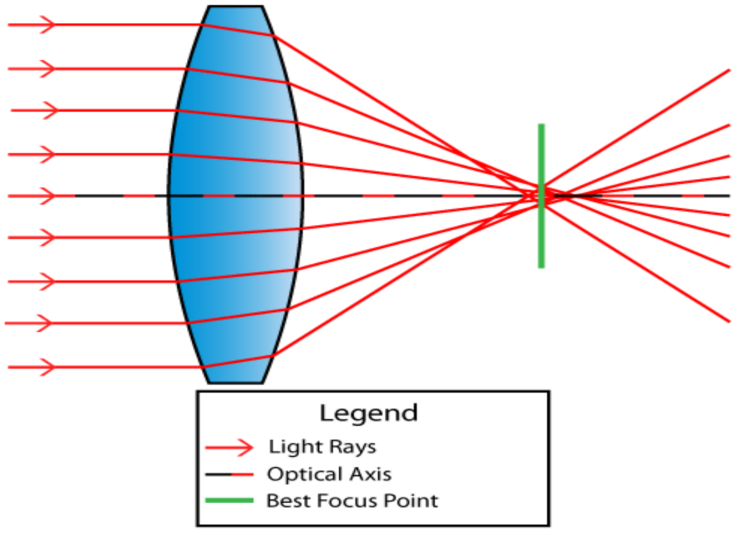


Figure 22: *Spherical aberration [47].*

To observe its consequences, one typical approach at the photolithography industry is to plot a family of Critical Dimensions (*CD*s) versus focus curves for different exposure energies as the one represented at the figure 23, also known as Bossung curves in honor of his deep analysis *[48]*.

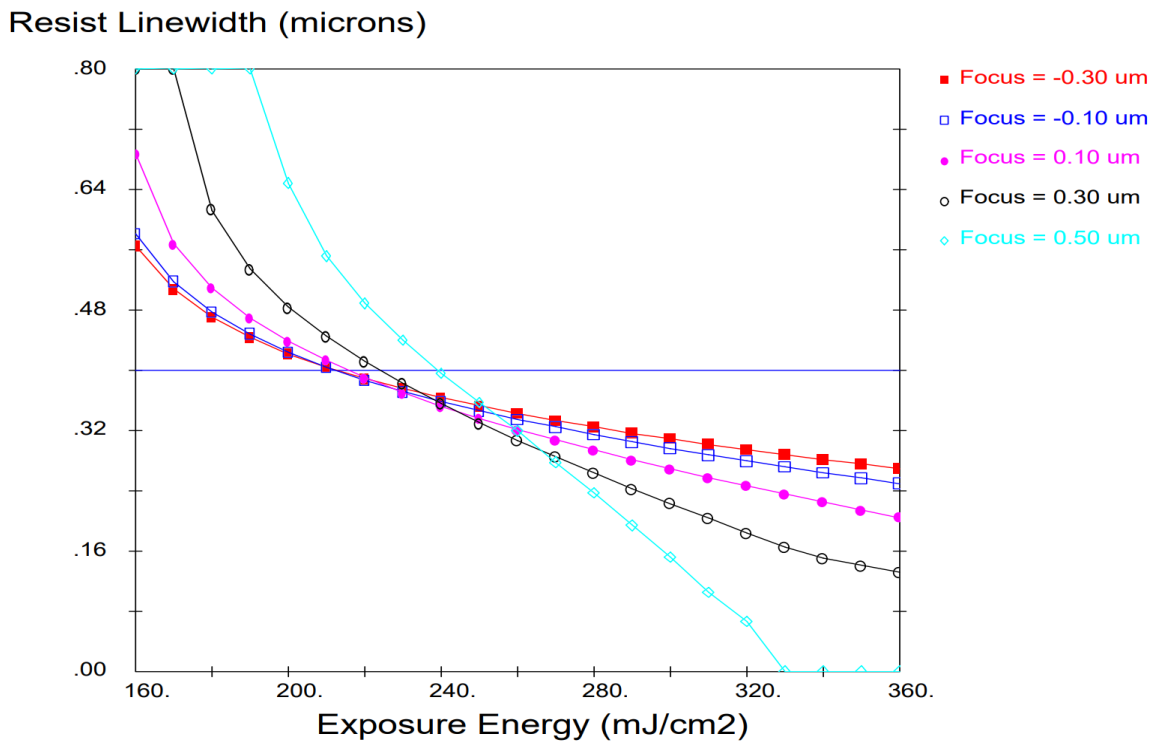


Figure 23: *Critical Dimension (linewidth) versus Exposure Energy for different focus [49].*

- The **coma aberration** describes an imaging defect where the image magnification varies with the location of the imaging rays in the aperture of the projection lens. Its consequence is to create a “comet tail”, formed with the rays from an off-axis point of light in the object plane, which are directed away from the optical axis (considering that this is positive coma). Coma is shape-dependent, so a lens shape can be found with zero coma for a given object distance, but that lens would not be optimum for other object distances *[50]*. The figure 24 shows the physical effect of the coma aberration, being produced a sharp image in the center of the exposure field, but the image becomes increasingly blurred toward the image edge. For photolithography, the practical implication is that the resist pattern feature become asymmetric and misshapen at the wafer level.

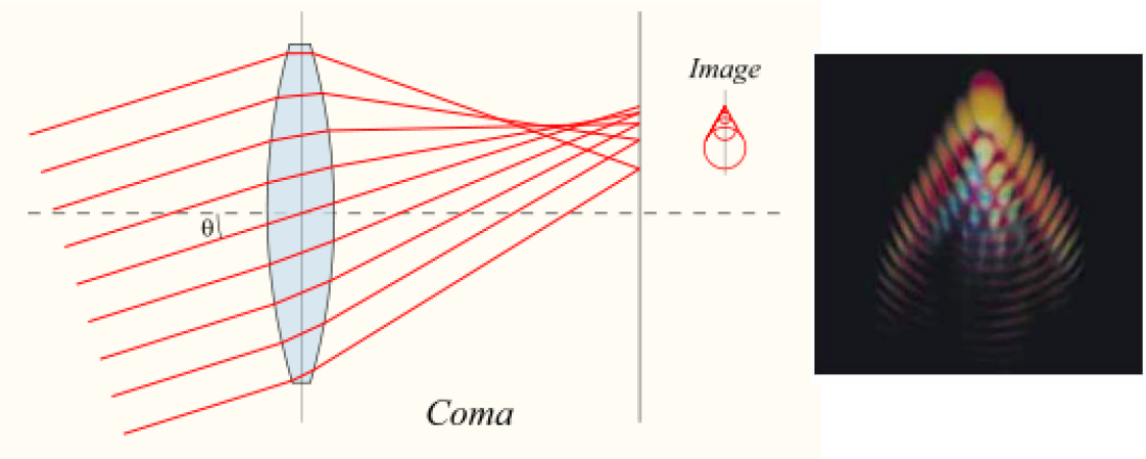


Figure 24: *Coma aberration and result [51].*

To analyze its effect, it is typical to measure the linewidth difference across an array of closely spaced lines, thus being the linewidth different between the two sides of the array, if there is a coma aberration.

- **Astigmatism** arises due to the fact that it exists different lens curvatures in different planes (or in the different mirrors), thus creating an imaging defect since lines are separated in different orientations at different focal plane positions. The figure 25 can be used as a reference to better apprehend the concept. With regards to the consequences, one can distinguish between having a line segment perpendicular to the radial line or in the sagittal plane: if the object consists of a short line segment perpendicular to the radial line from the optic axis (like a segment tangential to a circle centered at the optic axis in the object plane), then that line segment will image sharply in the tangential image plane. If, on the other hand, an object consists of a short segment in the sagittal plane, like a short radial segment in the object plane, it will image sharply in the sagittal image plane.

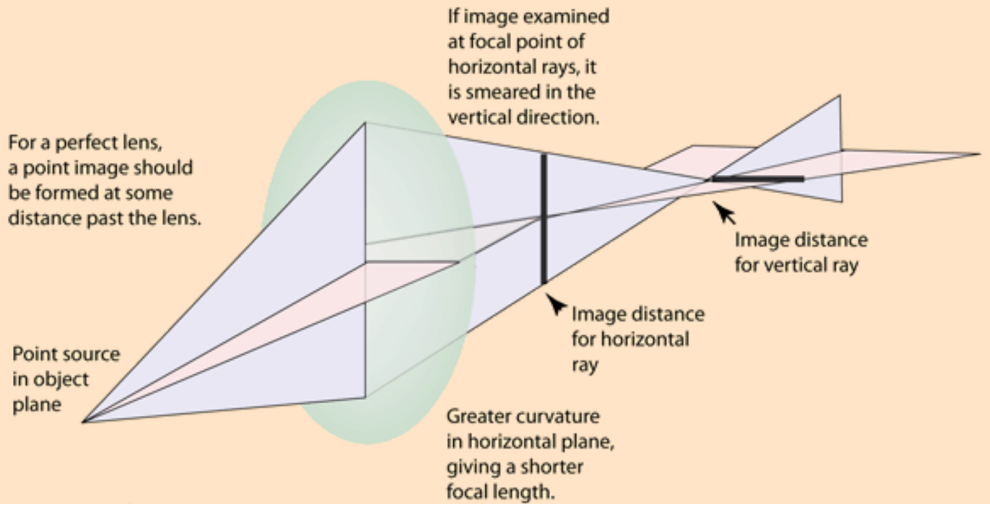


Figure 25: *Astigmatism aberration [52].*

In practical lithography, the astigmatism is typically described in terms of *x*- and *y*-orientation of the lines. Another approach to visualize the effects of oblique astigmatism on the image is by plotting each image point by a "circle of least confusion" where the overall best focus for the object is obtained *[53]*.

- The **field curvature** is an imaging defect depicted at the figure 26, consisting on a variation of the focal plane position with respect to the distance of the axis of the optical projection system to the object/image. It consequence is to project a curved (nonplanar) image from a planar original object.

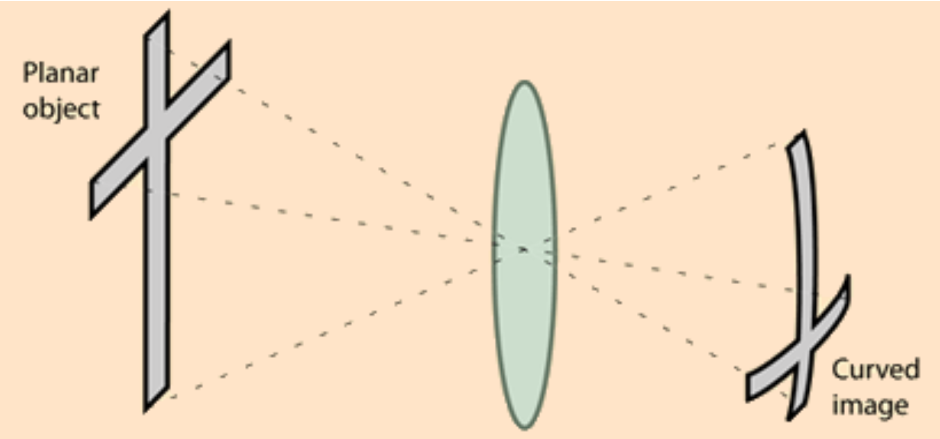


Figure 26: *Field curvature aberration and result [54].*

It is believed to be caused by a “power error” produced by rays with a large incident angle. The effect is similar to have a smaller diameter at the lens with an effectively higher power, forming the image of the off axis points closer to the lens [55]. The practical impact of field curvature on lithography is the reduction in the usable focus and degradation of the linewidth control.

- **Distortion** is an imaging defect consisting in the dependance of the distance from the object to the axis of the optical projection system with respect to the magnification of the wafer image. It occurs when the linear magnification is a function of the off-axis distance. In the absence of other aberrations, it effect is that all parts of the image are sharply focused, but show distortion across the whole image because of the varying magnification. The figure 27 illustrates the two different types of distortions: if there is a positive change in the magnification with distance, then the image will be distorted outward with the most distant parts of the image displaced the most, being typically called "pincushion distortion". The other sort is the “barrel distortion”, consisting in a negative distortion thus decreasing the magnification. In this case, the most distant points are more affected by the aberration.

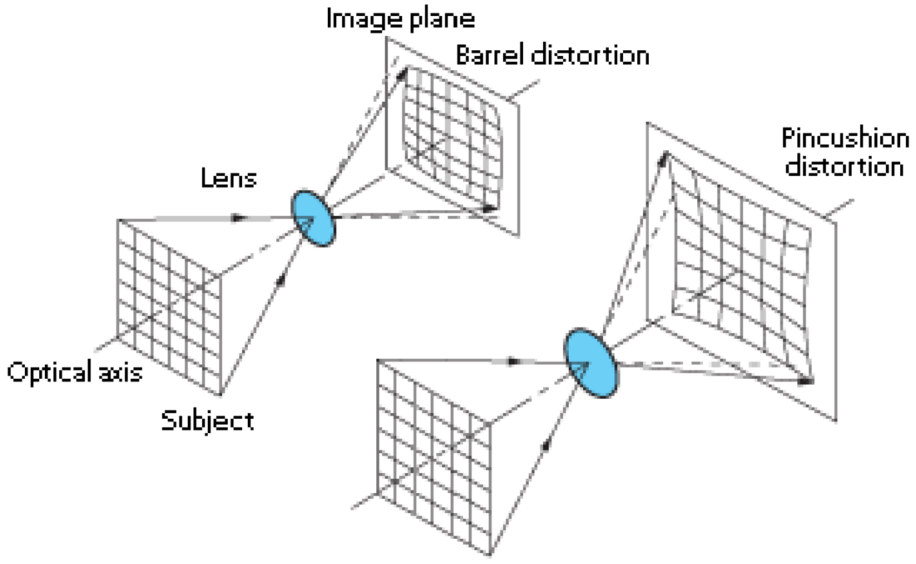


Figure 27: *Distortion aberration [52].*

The significant impact at photolithography is the reduction of image placement (*IP*) accuracy, leading to an overall overlay degradation. Distortion is one of the major challenges to effectively matching two or more lithography tools (from the same or different tool supplier) due to the different accuracy requirements on the same wafers, therefore it is one of the main *KPI*s reviewed at the acceptance of photolithography systems.

To describe the aberrations, a mathematical tool is used to make calculations easier. The most common representation of aberrations in use by lithographers is in the form of so-called **Zernike polynomials and coefficients**, named after the studies in 1934 of Frits Zernike. They are polynomials, which makes the mathematical calculations relatively easy, since they have helpful mathematical properties such as being orthogonal over the continuous unit circle and being all their derivatives continuous.

There are overall a total of 37 Zernike terms generally used, and it has become customary to describe the overall projection system quality as the Root Mean Square (*RMS*) value of those 37 terms. A related quantity, the so-called Strehl ratio, is also used to describe optical systems. For the low aberration levels of interest to lithography, the Strehl ratio can be expressed as a simple function of the Zernike coefficients using the following expression:

$$S = exp\left(-4\pi^2 \sum_{j=2}^{37} {a_j}^2\right) \qquad (3.1.b.1)$$

And if the aberrations are very small, the *RMS* value can be expressed in units of wavelengths *[56]*:

$$S = \left(1 - \frac{(2\pi RMS)^2}{2}\right)^2 \qquad (3.1.b.2)$$

Mathematically speaking, the Zernike coefficients can be also defined in terms of polar coordinates using two variables, ρ and θ', which are a distance and an angle (counterclockwise measured), respectively. If one looks into the unit circle at the figure 28, it is easy to understand the polar representation of the Zernike polynomials:

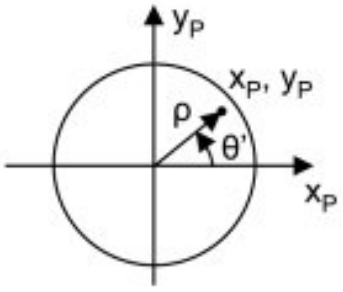


Figure 28: *Polar representation of Zernike polynomials [57].*

$$x_p = \rho * \cos(\theta') \qquad (3.1.b.3)$$

$$x_p = \rho * \sin(\theta') \qquad (3.1.b.4)$$

$$\rho = \sqrt{x_p + y_p} \qquad (3.1.b.5)$$

The low orders of the Zernike coefficients clearly show the astigmatism, coma and spherical aberrations and, what is more, they show a complete set so that they can represent arbitrarily complex continuous surfaces giving enough terms [58]. The figure 29 represents the aberrations obtained for different Zernike orders.

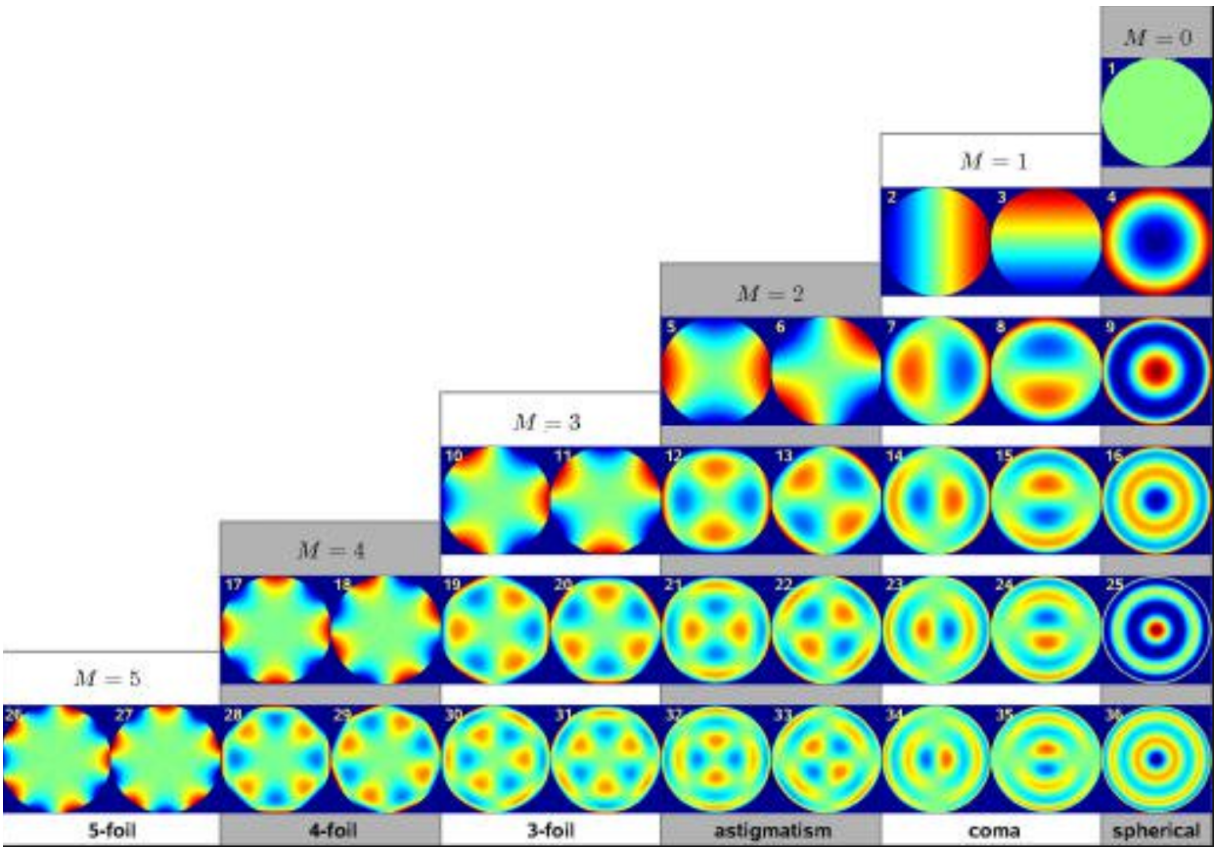


Figure 29: *First five orders of Zernike coefficients and their related aberrations [59].*

3.1.c. Alignment and overlay: process and tool systematic errors

The analysis of the lens and its characterization provided the reader the understanding of the potential issues of non-properly exposing the wafer due to the aberrations. However, even if the light is properly aligned and the rays are converging in a point in the *Z*-axis, how can we make sure that the exposing process is centered in *X* and *Y* coordinates? Well, it comes now to the alignment and overlay.

Thinking about a transistor, that semiconductor element will only work if the contacts have sufficient overlap with the appropriate parts of the transistors and do not contact the parts of the transistor from which they are supposed to be electrically isolated. On the contrary, if there are overlay errors such as the ones at the figure 30, it may well happen that the transistor malfunctions.

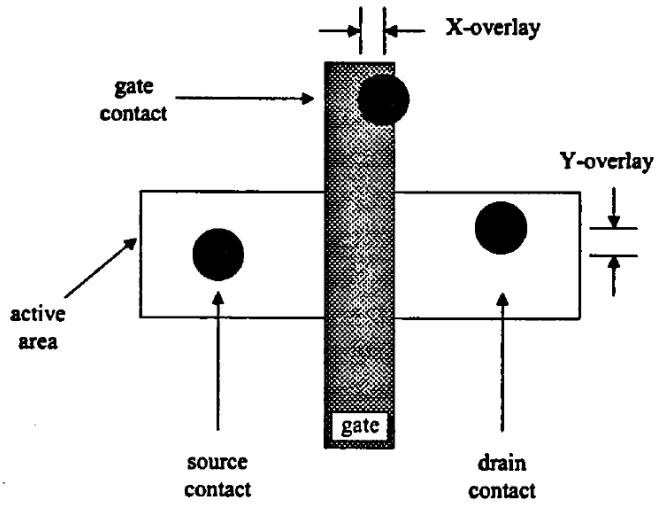


Figure 30: *Example of overlays errors in a transistor [60].*

The **alignment** is defined as the proper position of the photolithographic pattern relative to prior reference patterns, which are “commercial” marks conventionally known as fiducials, wafer or **alignment marks**. The fiducials are typically printed at the zero layer of the wafer (indeed it is the first printed layer) and at every added layer, prior or more usual at the photolithography tool, being an adequate shape in order to be detected via pattern recognition processes or laser beams.

Once the fiducial mark is detected, the mask and wafer positions are properly re-positioned so that the projected image from the reticle and projection lens falls as close as possible onto the desired location on the wafer.

Having defined the alignment as a process, the result of that “fine tuning” versus the fiducial is the **overlay**, *i.e.* how well the stack-up is done in terms of relative position between the different layers. The most accurate definition of overlay is: a vector quantity defined at every point on the wafer *[61]*. It is the difference, $\overline{O}$, between the vector position, $\overline{P}_2$, of a substrate geometry and the vector position of the corresponding point, $\overline{P}_1$, in an overlaying pattern, which may consist of photoresist:

$$\bar{O} = \bar{P}_2 - \bar{P}_1 \qquad (3.1.c.1)$$

The reader may notice that the definition of overlay is a relative one, since it relates the tolerances between layers and not versus a zero-reference. A similar definition, known as registration, defines the overlay but this time versus a reference grid. In fact, it is just a matter of references: even if the wafer has its own mark who represents its absolute zero, the wafer coordinates are also referenced to the wafer chuck (and stage) coordinates, which are at the photolithography tool.

To achieve the best overlay, just detecting the fiducial mark will not be accurate enough, since some misalignment still can occur between the stage and the wafer, therefore the alignment process takes several steps:

1) The wafer stage is firstly zeroed using encoders to detect its position. By means of the zeroing process, the interferometers take over the control on the wafer stage since it starts from a “well-known” position (the zero position), thus being more accurate than just measuring by means of encoders.

2) The next step is the pre-alignment, where a small wafer feature (typically a wafer notch) is detected to pre-align the wafer on the stage, thus providing a suitable range for the fine alignment.

3) By this moment, the photolithography tool already knows the position of the wafer stage, and more or less the relative position of the wafer within the wafer stage. Now it is time to very accurately locate the wafer within the wafer chuck, which is the place where the wafer is vacuum-clamped at the photolithography tool. To do so, some marks (which varies between the different tool manufacturers) are in the chuck, so that the photolithography tool knows, now by means of laser optics, where the chuck is located.

4) The last process would be to pattern (or read) the fiducial or alignment marks on the wafer, so that their positions are related to the wafer chuck marks, which have been previously referenced to the position of the wafer stage.

The basic measurement of gratings (or marks) could be done by one light source and using two reference marks, thus correcting rotation and translation. However, due to the nanometer-required accuracy, more marks are needed to correct the potential expansion (wafer contractions) in the two axes (*X* and *Y*) if the alignment marks are not all collinear on a single axis. There is also a measurement in the *Z*-direction, since the non-flatness would imply also errors in the other coordinates.

The methodology to detect the marks and perform the alignment process can be classified into three different criteria, as the table 4 specifies:

Table 4: *Classification of alignment methods for photolithography. Source: own, based on [60].*

Alignment classification	Types
Optical method	Bright-field
	Dark-field
	Diffraction
Referencing of wafer to reticle	On-axis or Through-The-Lens (TTL)
	Off-axis
Number of alignment sites	Global
	Enhanced global
	Die-by-die

The photolithography tool manufacturers have been using the different approaches mentioned on the table 4, sometimes utilizing different combinations or even evolving from one technique to another. It is beyond this thesis to deepen in each and every single technique, but the reader is strongly encouraged to research further *[61]*.

As reference, the technology used by the tool manufacturer Advanced Semiconductor Materials Lithography (*ASML*) will be described. Concretely, their steppers use a phase grating alignment system to directly align reticle and wafer images through the main stepper lens *[62]*, a process sketched in figure 31:

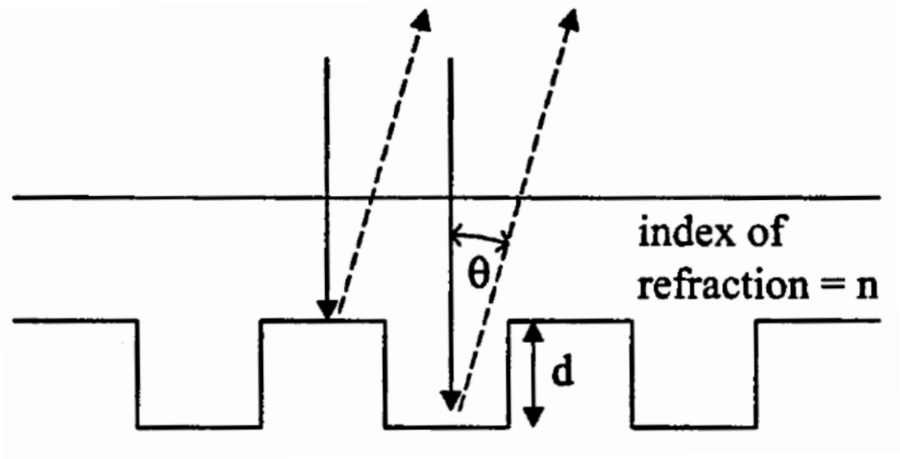


Figure 31: *Phase grating alignment mark [60].*

The maximum alignment signal results when the two phases differ by 180 degrees, having auxiliary optics (minimum two laser sources) to compensate for optical path differences. By not detecting the edge, the resolution requirements of the alignment optics are considerably relaxed, also achieving an excellent signal-to-noise ratio.

Instead of using the mainstream technique of having wafer marks in each layer, *ASML* just etches the alignment marks in the zero layer, thus using this reference for building up the whole wafer layers by aligning the subsequent reticles to this zero layer. That approach has to use a wavelength suitable to trespass the coating without any damaging and uses extra time, but it has good advantages such as maintaining marks integrity throughout all the layers and avoiding lens offsets (the offset will be placed in all the layers but its total overlay will be null).

Enough talked about the ideal world of the alignment process to achieve the best overlay. The real world means that there are a lot of mechanical limitations that will make the overlay to not achieve the targeted result. There are two categories of overlay errors: intrafield, which involve the variation of overlay errors within exposure fields, and interfield, which are the ones that vary from exposure field to exposure field across wafers. For its analysis, a hierarchical model is used, where three main categories are defined as summarized at the figure 32:

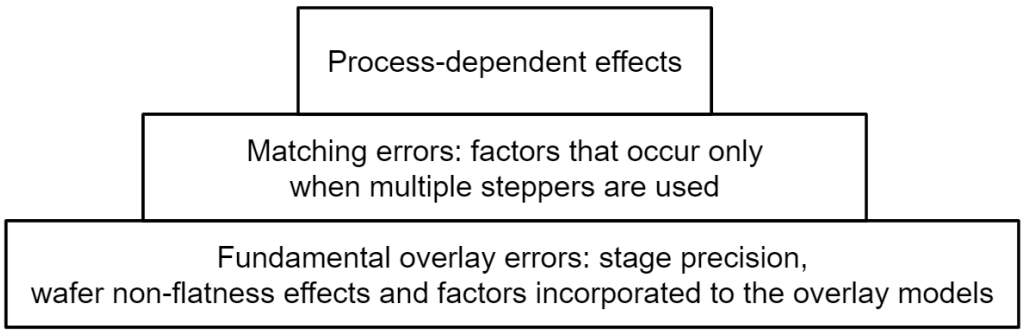


Figure 32: *Hierarchy of overlay errors. Source: own, based on [60].*

a) Process-dependent effects: this category refers to the problems introduced by the track, *i.e.* the tool responsible for processing the wafer before (and after) the exposure at the photolithography tool. Numeral processes can go wrong before the exposure, such as film depositions, resist coatings, etches or polishes. To overcome those issues, the lithography tool has to be optimized depending on the previous process parameters, for instance by adjusting the dose and the energy of the exposure. Typical failures that are observed in this category are:

- Addition and removal of highly stressed films causing wafer distortion. The stress (compressive or tensile) of the deposited film layers might change the wafer dimensions once the wafer is chucked (clamped) into the wafer chuck. Usually it is a linear dimensional change, which can be read and automatically compensated by the magnification control of the exposure tool. But, if the highly-stressed film were partially removed from the wafer, the distortion might not be linear and would be almost impossible to be corrected *[63, 64]*.

- Sputter deposition of metals causing asymmetries in overlay targets, since metal ions are partially shadowed by the alignment mark topography. That might lead to apparent shifts in the position of the alignment marks, therefore the exposure control will be degraded.

- Asymmetrical resist coating can cause apparent displacement on the wafer alignment marks, since they consist typically of raised or depressed features in the underlying pattern layers. The consequence for the overlay will depend upon the alignment detection system used *[65]*. The Chemical-Mechanical Polishing (*CMP*) process can help to reduce that asymmetry, but also might lead to other issues as described in the following paragraph.

- Chemical-mechanical polishing (*CMP*) process can reduce the alignment target contrast by rounding the alignment marks more on one side than on the other, therefore they become invisible when the planarization process is completed. Thus, accompanied with the polishing, often produces asymmetries particularly when the pattern width is large.

- Not only related to the process done on the track, but also appearing at the photolithography tool itself, contamination is one of the main root causes of exposure defects. Therefore an extreme clean environment is mandatory at the fab in order to avoid contamination in the wafer, the reticle and the photolithography tool environment. The figure 33 allows the reader to understand the consequences in the image formation of having a contaminant particle before the lens.

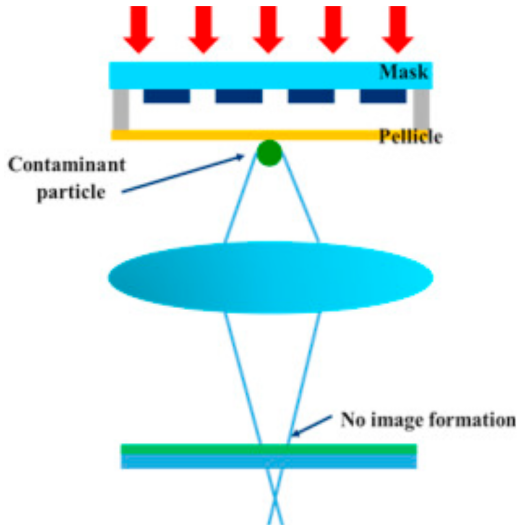


Figure 33: *Effect of a contaminant particle in the image formation [66].*

b) Matching errors: they are the consequence of using different steppers for the same Integrated Circuit (*IC*). In common manufacturing processes, many steppers can appear, sometimes even from different brands, since in the same circuit different accuracies might be required (not always the tool with best accuracy is the most used, since throughput and cost also have an influential weight for the decision). Therefore, even if the accuracy of one stepper seems to be within specifications, its relatively small error, converging with another inaccuracy from a different stepper, might make the circuit to fail. This type of failures are related with the elements of the stepper itself, such as the lens or the reticle:

- Mask errors: even if they are manufactured by an electron beam or a laser beam writer, still residual errors exist. Furthermore some mechanical errors are added at the chucking (clamping) of the reticle into the exposure tool (which might fit better at the fundamental overlay errors), thus leading to apparent distortion in the printed pattern. It is generally accepted a reticle error below or equal to 40% of the overall error caused by the photolithography tool.

- Lens distortion and magnification: they have been discussed at the optics subchapter with the aberrations before. But on top of that, let us remember that the distortion is usual at any optical projection system, and that telecentricity at the lens may also lead to magnification errors. Typically all exposure tools have control systems to maintain the magnification (reduction ratio of the pattern) corrected by every wafer, therefore the magnification error tends to be random and not characteristic of any tool in a matched set.

c) Fundamental overlay errors: they are related to the photolithography tool mechanical limitations, and also due to the substrate non-flatness within the tool. One can highlight:

- Wafer chucking errors: when the wafer is clamped at the wafer, it is flattened and clamped by means of vacuum to the chuck. This might lead to the well-known “hot-spot” issue, which makes the wafer has more elevated parts at its surface, which will cause resolution failures and Critical Dimension errors. In addition to that, the effective locations of wafer features with respect to the optical column are slightly changed due to local tilt of the wafer, as it rests on the contamination. The opposite effect is the “cold-spot”, which is obviously appearing a lowered/depressed part at the wafer. To avoid those issues, extremely careful control of the air pressure for clamping, temperature, stage motions and contamination is required at the scanner.

- Stage errors: the reticle and wafer stages are basically manipulators with limited accuracy, since they have to step with determined precision, being affected by dynamic forces such as friction, stiction, hysteresis and/or vibrational modes. They are tracked by encoders (coarse tracking) and laser interferometer gauges with measurement resolution of less than 1 *nm* (for the fine positioning control), but even so it can obtain false measurements due to turbulences or temperature non-uniformity of the air in the region of the stage. Therefore, extreme care is needed for the design and manufacturing of the airflow and thermal control around the stages (improper heating of silicon wafers leads to non-flatness and to a slippery silicon surface). The high speeds increasing the throughput will create and augmentation on the vibrations, thus leading to secondary errors *[67, 68]*.

As appendix of this subsection, one has to mention that the overlay of the tool is always measured with an equipment, which can be internal or external to the photolithography tool. Even if the photolithography process looks good (by the internal feedback of the photolithography tool), the metrology tool introduces also an error at the measurement, therefore sometimes may exist a false negative or a false positive. The metrology errors can come from different sources: for instance the metrology offset and shift itself, which is usually below 2 *nm*. Particularly critic is the methodology of measuring, which is usually done with a large (10 *mm*) box pattern, but that size has to be optimized and customized to the pattern size on the wafer. The metrology tool also has a lens, which can suffer from aberrations, therefore a study of that optics is needed too.

3.1.d. Throughput: cycle time breakdown

Obviously the industry is always focusing on the cutting edge in terms of accuracy, thus finding news like the latest information by the taiwanese manufacturer *TSMC* which announced the 5 *nm*-technology node mass production from the second half of 2019 (the reader may refer to the section state-of-the-art for manufacturers comparison). But accuracy has literally a price: not always it is needed to have the most precise system since the price of the tool can be ridiculously high. But, what if a manufacturer makes the best chips of the market but they are only able to produce one *IC* per hour, in comparison to another foundry which produces hundred of less accurate chips at a reduced price? It comes obvious that the concept of throughput/productivity is enormously important for the photolithography. Indeed, the wafer throughput is the most prominent factor in advanced cost of ownership models, even more important than the price of the tools.

Photolithography is generally the most used process in the wafer fab, typically accounting for 30%–35% of the total process cost. Therefore, most fabs are designed so that the photolithography area will be fully loaded at all times. This, in turn, drives very high importance to the productivity of photolithography tools.

To analyze the throughput, some definitions are needed. The easiest one is the so called "sprint rate", which defines the maximum run rate, *i.e.* how fast the tool can expose in optimal conditions.

$$T(wafer\ per\ hour, wph) = \frac{3600\ (\frac{seconds}{hour})}{wafer\ proceess\ time\ (s)} \qquad (3.1.d.1)$$

The previous figure defines one measurement of **throughput**, *i.e.* an indicator of the amount of parts (in our case wafers) that can be processed in a certain amount of time (one hour). The wafer process time can be also breakdown into the following components:

$$t_{wafer} = t_{woh} + N_f\left(t_{exp} + t_{foh}\right) \qquad (3.1.d.2)$$

Let us describe the meaning of each term:

- t_{woh} is the **overhead time per wafer**: its first contributor is the time to load and unload the wafer, which is system-dependent and has typical figures of few seconds or less. The other factor is the alignment time, which depends on the alignment strategy: no alignment, two or three marks, or the most common nowadays having between 8 and 10 positions on the wafer (takes generally a few seconds). One very interesting approach to reduce the overhead time per wafer is the one used by *ASML*, which employs two interchangeable wafer chucks running in parallel: during exposure of one wafer, the other wafer is being measured, and then they are swapped [69], thus reducing the cycle time.

- t_{foh} is the **overhead time per exposure field**, which represents the movements between consecutive exposures. It includes stepping time, settling time, scan acceleration time, die-by-die alignment time (if used by the tool manufacturer) and shutter delay times. The overall figure is typically between 100 and 200 *ms*.

- t_{exp} is the actual **exposure time** during which the actinic radiation is exposing the resist. For a typical 193 *nm* chemically amplified resist, with an exposure sensitivity in the 20–30 mJ/cm^2 range, and an exposure power density of 2000 mW/cm^2 at the wafer, the resist-limited scan rate is 30–80 *cm/s*, which spans the mechanical scanning rate specification [12]. The relative throughput can be plotted as a function of the field size and the resist sensitivity, as represented at the figure 34:

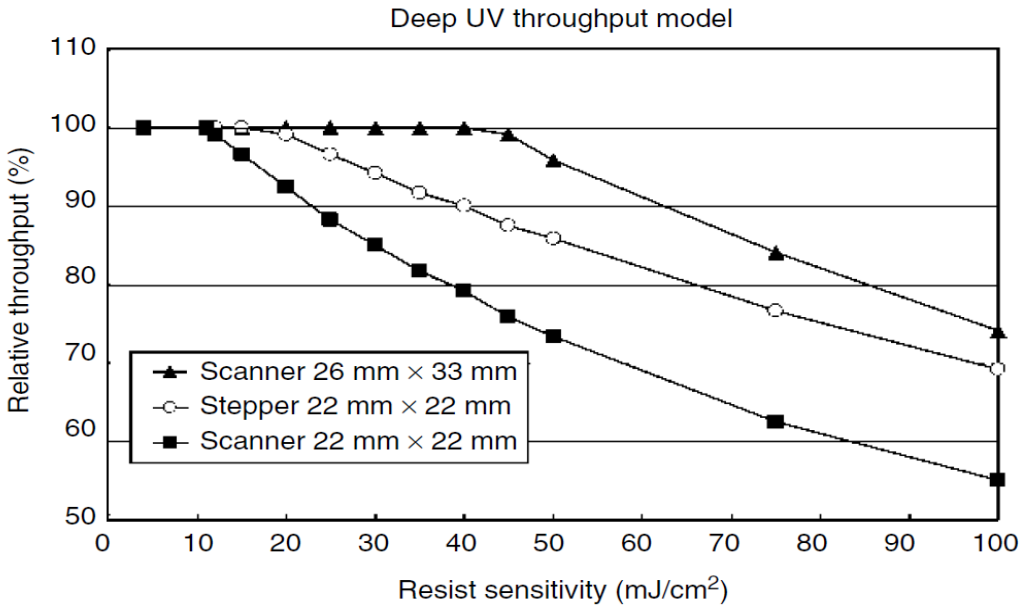


Figure 34: *Throughput model for steppers and scanners for different field sizes and resist sensitivities [12].*

- ❖ N_f is the **number of exposure fields per wafer**. Obviously that depends on the lens size, the reticle size, the wafer size (nowadays 300 *mm* whereas previously the standard one was 200 *mm*) and the die size.

Processes not run for every exposure are not included in the previous basic calculation, but they have to be provided by the photolithography tool manufacturer, since the wafer cycle of life (see figure 35 for reference) includes also the interaction with the track, and the reticle might be changed for different layers (or products) within the same scanner.

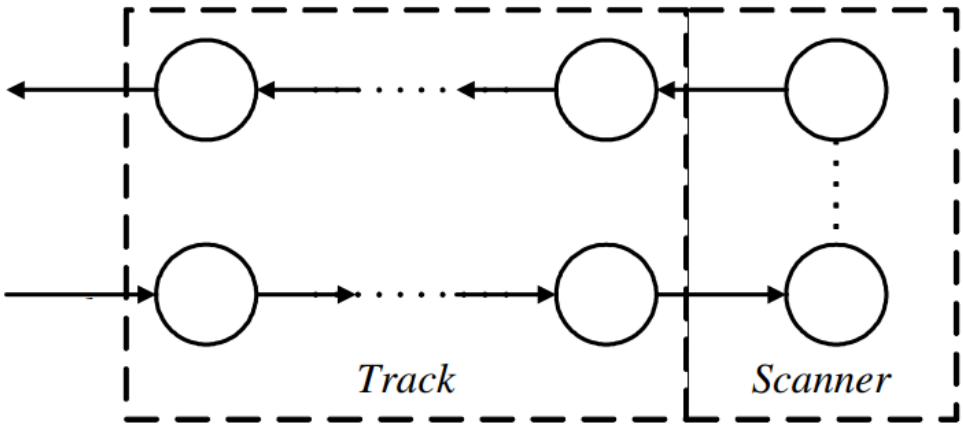


Figure 35: *Wafer cycle of life between the track and the photolithography tool (scanner) [70].*

Therefore the throughput does not consider only the measurement and exposure processes at the scanner, but also requiring some new figures:

- **Lot setup times**: when a new lot is introduced into the tool, some extra steps are usually needed, such as reading the lot identification (*ID)* -to include traceability at the process- or changing the program.
- **Reticle change times**: how long takes the exposure tools to change over the reticle.
- **Time for indexing the wafers** from the processing track.

Last but not least, one should mention that the maintenance time (downtimes) are not included in any of the calculations, since they usually depend upon the sort and the status of the tool itself, but also on the maintenance frequency used by the chip manufacturer. What is more, it varies from person to person, therefore skill levels can make a huge difference in terms of maintenance times. They are considered as part of an overall factory capacity model by the circuit manufacturer and no longer by the tool manufacturer, which only provides standard times of the operations to be performed and the maintenance frequency that they recommend.

3.1.e. Current trends to improve accuracy

The actual level of optical exposure tool manufacturing is in a very mature phase, where the dry environment approach leads to a maximum *NA* for conventional projection lenses. If one looks back to the original Rayleigh equation, in order to improve the resolution (decreasing *R* in fact), one can opt either for reducing k_1 or the wavelength, or for increasing the *NA*. To address each of these options, three different methodologies have arisen to continue shrinking the transistors size:

- The first approach, the so-called **Resolution Enhancement Techniques** (*RET*s), are currently included at the tool manufacturers *[71]*. They consist on improving the imaging performance by wavefront, mask or resist process engineering, thus reducing the constant k_1.

- The second option is to use a **wet environment** (with water) for the lens instead of dry (air), so that a better resolution is achieved by improving the *NA*. Nowadays -2019- this approach is used in High-Volume Manufacturing *(HVM)* by the major foundries *[72]*.

- The third strategy, which has had a complex way to being developed, it is utilizing a different light source with less wavelength: the **Extreme UltraViolet *(EUV) light***, which is photon-based. Only the major foundries (*TSMC*, Samsung and Intel) have started using it *[73]*, since just one tool manufacturer (*ASML*) provides those systems and the complexity and cost are enormous, but it is well assumed that it is the direction where the market goes.

All the three approaches will be described from a technical point of view, understanding what their improvement consists on.

3.1.e.I. The Resolution Enhancement Techniques (*RET*s)

The Resolution Enhancement Techniques *(RET*s*)* enhance the performance with three different sort of tricks: the first option is to include wavefront engineering, which customs tailor the aerial image to provide an increase in terms of resolution *[74]*. The second solution is focused on mask engineering, optimizing the exact shape of reticle pattern by observing the desired (actual) patterns on the wafer. And the last approach is to work on the resist process, thus allowing the resist to receive the aerial image.

The three approaches can work together, having also different techniques depending on the tool manufacturer, since all of them have both pros and cons. The table 5 summarizes the different methodologies, also mentioning the advantages and disadvantages of each approach.

Table 5: *Resolution Enhancement Techniques (RETs) [12].*

RET	Type	Advantages	Disadvantages
Phase shift masks	Wavefront engineering	Improves DoF and exposure latitude	High mask cost, inspection and repair difficult
Modified illumination	Wavefront engineering	Improved DoF for dense line/space features	Less improvement for holes or isolated lines affected by lens aberrations
Optical proximity correction (OPC)	Mask engineering	Improved critical dimension (CD) control for various size patterns	Additional design data processing masks more complex and expensive
Wafer control—antireflective layers	Resist engineering	Improved CD control reduces notching	Increased cost and process complexity may complicate etch
Pupil filtering	Wavefront engineering	Improved CD control and exposure latitude	Pattern-specific capability must be designed in by lens manufacturer
Multilayer and surface imaging resists	Resist engineering	Improved CD control, improved resolution, includes antireflective functionality	Increased process complexity and cost, generally requires plasma etch capability as part of photolithography

Rather than reviewing shortly every single option, the most commonly used (Phase Shift Masks) will be described in quite detail.

The ***PSM*** technique is based on the principle of light interference: as a consequence of the wave nature of the light, with opposite phases (shifted by 180 degrees) the light waves will create a destructive interference between the light from the adjacent openings. That will result in a darker image between the open features than with conventional lithography, where the light from adjacent openings overlaps in the dark region. The goal is to maximize the sum of intensity slopes at the transition region of a mask, subject to inequality constraints associated with non-transition areas *[75]*. Under incoherent illumination, this criterion results in a linear binary

programming problem with linear constraints, which can be solved via the well known branch and bound algorithm [76]. As demonstrated [77], this criterion results in sharper output intensity contours than using the mean squared error criterion (the conventional lithography techniques).

The *PSM* concept can be easily understood by looking at the intensity wave comparisons shown at the figure 36, where resolution (contrast between the higher and lower intensity) with this technique is greater than with a conventional approach.

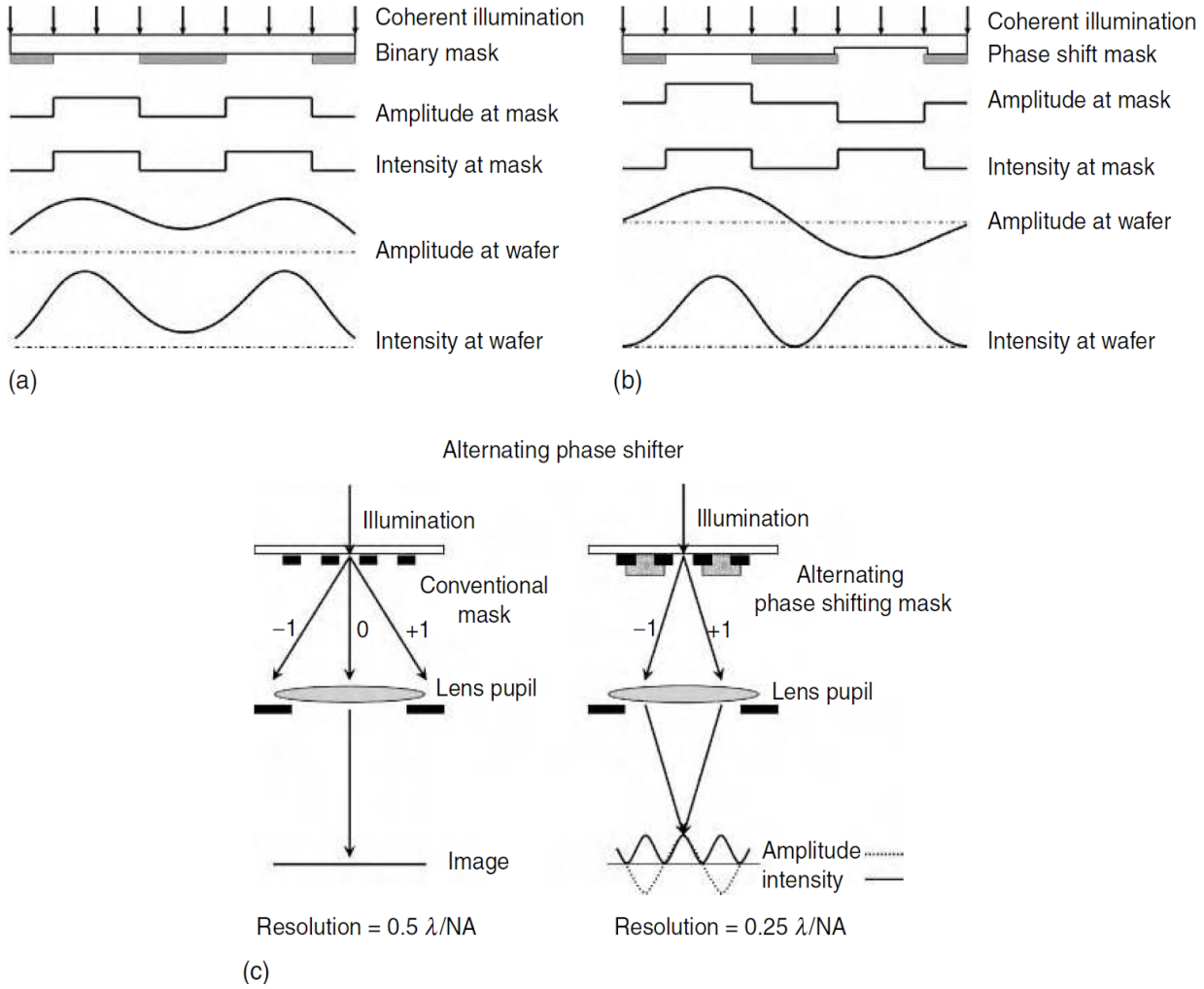


Figure 36: *Alternating phase shift masks [12]. (a) Superposition of aerial images amplitude for conventional lithography. (b) Superposition of aerial images amplitude for PSM. (c) Comparison of conventional and PSM image and resolution.*

As one can realise looking into the figure 36, a thin layer has been added to the mask. This is manufactured of a transparent material, typically spin-on glass, having a thickness so that the optical path length is exactly one-half wavelength longer than it would be in air (simplifying the air index refraction *n* from 1.0003 to 1 which is equivalent to use the value of the wavelength in vacuum):

$$t = \frac{\lambda}{2(n-1)} \qquad (3.1.e.I.1)$$

For typical conditions, *i.e.* when the index of refraction *n* of the shifter material is 1.5, the thickness to be used is the same size as the exposure wavelength.

Since the accuracy of the typical spin-on films is not that good, the natural evolution was to etch directly the required phase-shifted pattern onto the reticle substrate. On this way, properties-control is better, since the etching in the high-quality fused silica at the reticle is a well-known and mature process.

However, some issues arise in real practising: inequalities appear with different feature sizes and focus. Electromagnetic wave modelling of the optical behavior shows that it is necessary to adjust the etch sidewall profiles and/or bias the size of the pattern features to achieve the full benefit of the phase shift effect [78]. Obviously this has an impact on the cost and lead time of manufacturing the phase-shift reticles. Another concern is the limitation on applying the *PSM* to an arbitrary circuit pattern layout, since there are cases where there is an ambiguity to select the phase to be applied to specific openings, or for instance when two adjacent openings have the same phase. To cope with that, major advances in software programs have been developed, which assign phases and adjust pattern positions where phase ambiguities exist [79].

3.1.e.II. Immersion tools

Using a dry environment (exposure through air), the Numerical Aperture is limited to 1.0, since any attempt to increase the optical ray angles further -thereby increasing *NA*- would simply lead to a total internal reflection of the light back into the lens. The workaround to increase the *NA* is to introduce a **wet environment**, in this case by means of water, that allowing the rays to pass on to the resist. The figure 37 shows a comparison between both dry and wet environments: a light ray with *NA*=1.3 is totally reflected onto the lens in an air medium, whereas at the water medium (between the lens and the resist, *n*=1.44), the same light ray passes through and hits the wafer:

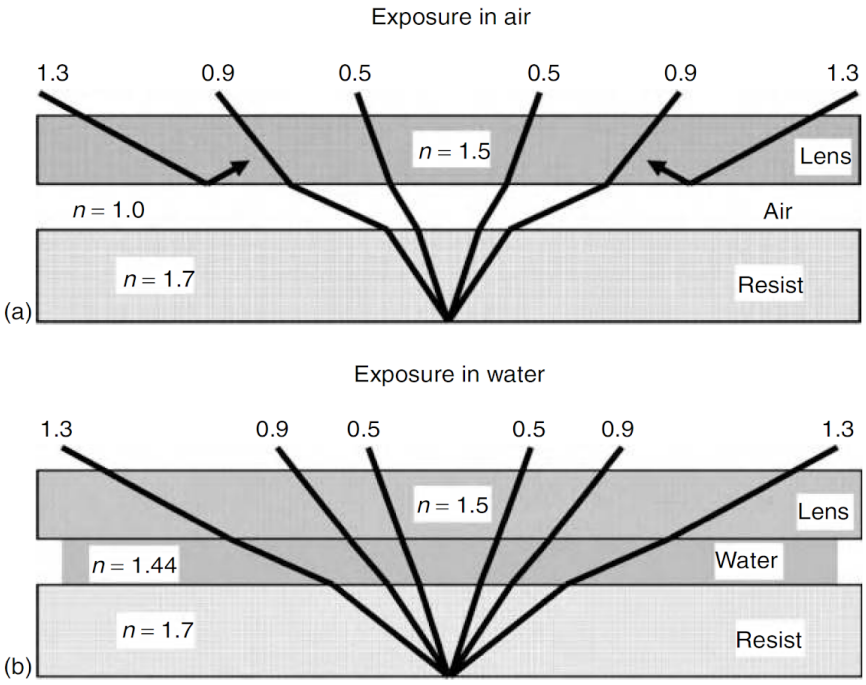


Figure 37: *Optical rays for different NAs [12]. (a) Dry. (b) Wet environment.*

If one comes back to the original Rayleigh equations, the *NA* will be no longer *sin Θ*, but this value has to be multiplied by the refractive index *n* of water, which is 1.44 (not any longer 1), thus becoming the Rayleigh equations with water as environment for immersion tools:

$$R = k_1 \frac{\lambda}{n * sin(\theta)} \qquad (3.1.e.II.1)$$

$$DoF = n * k_2 \frac{\lambda}{NA^2} \qquad (3.1.e.II.2)$$

The result is that the resolution is improved by a factor of 1.44, and also the *DoF* is increased by that factor *n*. In fact, some analysis [38] has proven that the Depth of Focus can be increased even more than by the factor 1.44.

How the implementation of the water medium is implemented at the tool depends on the manufacturer. Different approaches have been considered: the first one was to completely immerse the wafer, wafer stage and the bottom of the lens. Due to the rapid stepping and scanning motions, the mechanical difficulties make abandoned this approach. The second one consisted on limiting the water to a smaller region at the wafer stage (like a small pool), thus having no need for the stage itself to travel through a large bath of water [80]. This approach is also not used nowadays by the manufacturers. The most accepted one consists on creating a film of water between the bottom of the lens and the wafer, in an area called Immersion Hood (*IH*). That film is constantly refreshed by the flow of water from a fill port to a removal port [81, 82], being its cleanliness and temperature control key for a proper patterning.

The implementation of the wet tools have some extra challenges for practical implementation though:

- **Optical design of projection lens**: larger *NA* greatly increases the required size of the individual lens elements, impacting both cost and manufacturing difficulties [83]. The alternative choice is to use a catadioptric lens design, employing a small number of reflective elements (which provides the imaging power) in addition to refractive elements (responsible for correcting the aberrations). For instance, once can use three mirrors as sketched the figure 38: two would be simple folding mirrors and the third one (curved) is responsible for providing a substantial portion of the imaging power of the lens, whereas refractive lens elements correct the aberrations and provide some of the imaging power of the lens.

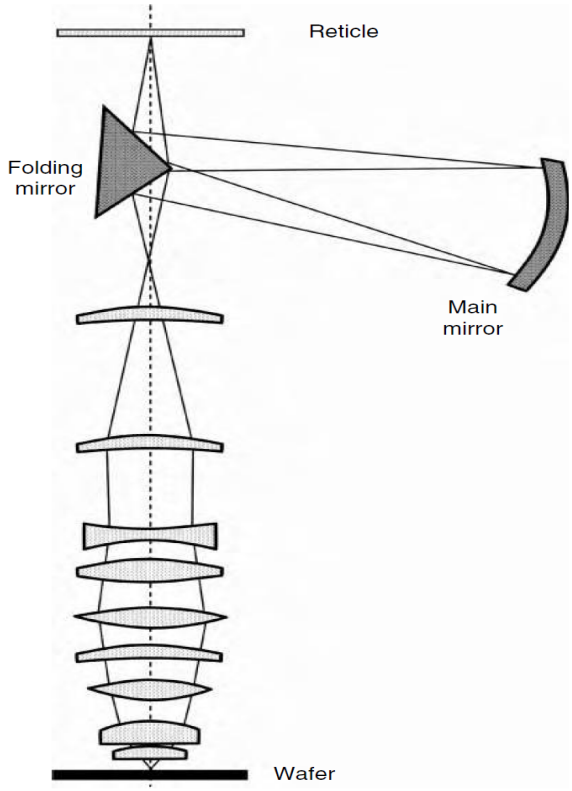


Figure 38: *Example of an advanced catadioptric projection lens [12].*

By using this approach it is possible to increase the *NA* up to 1.30 or even more, while maintaining the overall lens size. The complexity also remains similar to the largest possible all-refractive designs *[84]*.

- **Mechanical system design**: in order to maintain high productivity and accuracy, it is essential that the wafer stage motion will not be degraded by the immersion environment. To avoid so, the thin film of water (around 1 *mm* thick) has to be maintained in position by surface tension properties of the nozzle materials. To do so, a typical approach is to use an air curtain to keep the water in the proper position *[85]*.

- **Additional wafer defects**: the existence of air bubbles or floating particles at the wafer sheet may block or scatter the imaging light from the lens, therefore it is important to filter and properly handle the extremely high-pure water at the fab. Large bubbles (diameter greater than 1 micron) must be avoided since they will block the light, whereas smaller bubbles (smaller than 100 *nm*) can be tolerated unless they are close to the wafer surface, since there they can create a distortion of the patterned image on the wafer *[86]*. Also the interaction between the water and the resist can create potential defects such as different pattern density across the wafer, therefore the solution is to add topcoat or using extra processes such as pre- and/or post-soaking, having as drawback extra cycle time -therefore cost- at the processing on the track.

- **Control of the wafer-resist surface effects**: it is important to locate properly the nozzle around the periphery of the exposure field at the bottom of the lens. The optimum angle between the water and the resist has been determined to be 70 degrees or higher *[87]*, to allow containment of the water film under the lens. In terms of the resist surface, creating an extra hydrophobic coating would help to avoid that the resist would draw water from the Immersion Hood, as well as improving the mechanical performance of the resist. Consequently, a hydrophilic surface is to be avoided (to not pull out droplets from the water film).

- **Thermal control of the water**: the ultra-high accuracy required for the optical and mechanical components of modern tools required extra attention to the thermal expansion of materials and the alteration on optical properties due to temperature drifts. Adding the water as new element introduces two new difficulties: the first one is that the water heats easier than air, therefore the change in the refractive index (10^{-4} per K) will lead to degrade imaging, consequently the water temperature has to be within a 10 mK range *[88]*. The second concern has to do with the evaporation of the water: it is essential that the flow is recovered and none of it evaporates, since otherwise it can result in residual water films or droplets imaged onto the wafer.

3.1.e.III. Extreme UltraViolet (*EUV*) lithography

The Extreme UltraViolet *(EUV)* lithography uses a different light source, having nowadays an **extremely short wavelength** of 13.5 *nm*. The first experiment with such short wavelength was done with Molibdenum (*Mo*) and Beryllium (*Be*) as element sources, using a wavelength of 11.3 *nm*. The reflection optic used was composed of multiple multilayer mirrors, each one absorbing around 70% of the light. However, in 1999-2000, the international semiconductor community abandoned that approach due to health and safety issues with the very toxic *Be* particles [89] and went for the 13.5 *nm* approach.

Further experimentation [90] drove to use tin (*Sn*) as source element due to the **high reflectivity**: a comparison of that feature for different element is plotted at the figure 39. It is also important to notice that *EUV* radiation is strongly absorbed in virtually all materials, even gases [40], therefore a vacuum environment is to be used.

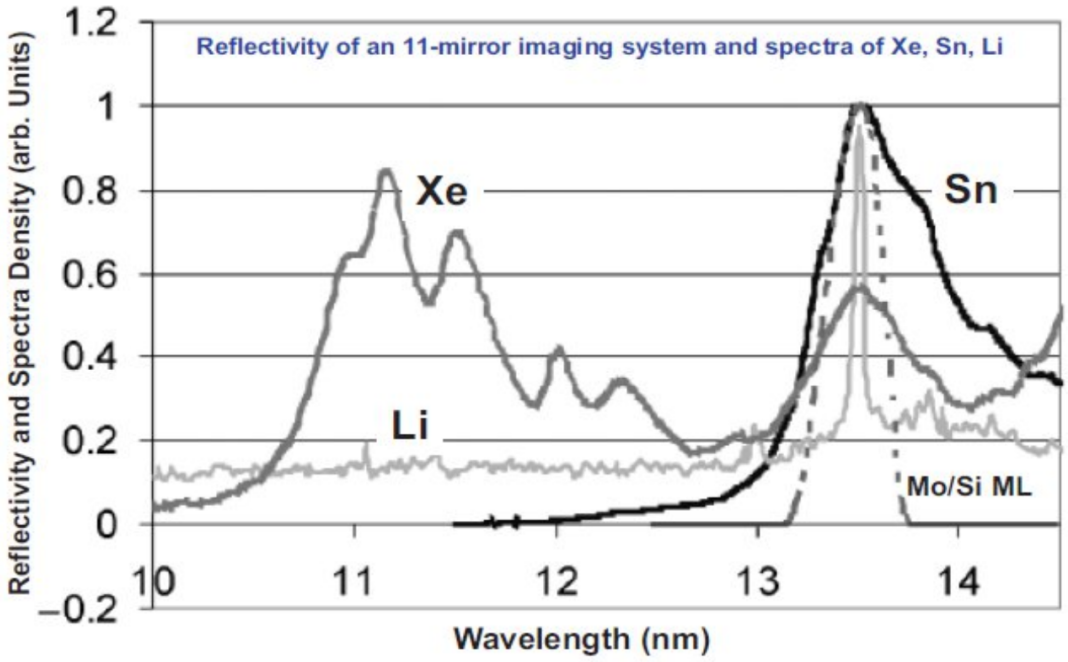


Figure 39: *Reflectivity and spectra density for different source elements [90].*

For *EUV* lithography, the generation of the light is no longer by an excimer laser (or *Hg* source at the old-fashioned high pressure lamps), but generated by a high-temperature and high-density plasma. There are basically two methods [91] to generate it: the Laser-Produced Plasma (*LPP*), which condenses a strong laser beam onto a certain material, and the Discharge-Produced Plasma (*DPP*), that uses a pulsed high-current discharge between electrodes in an atmosphere of certain materials. The *EUV* laser light source becomes much more complex, as the figure 40 depicted, needing in addition more space and cost to be generated.

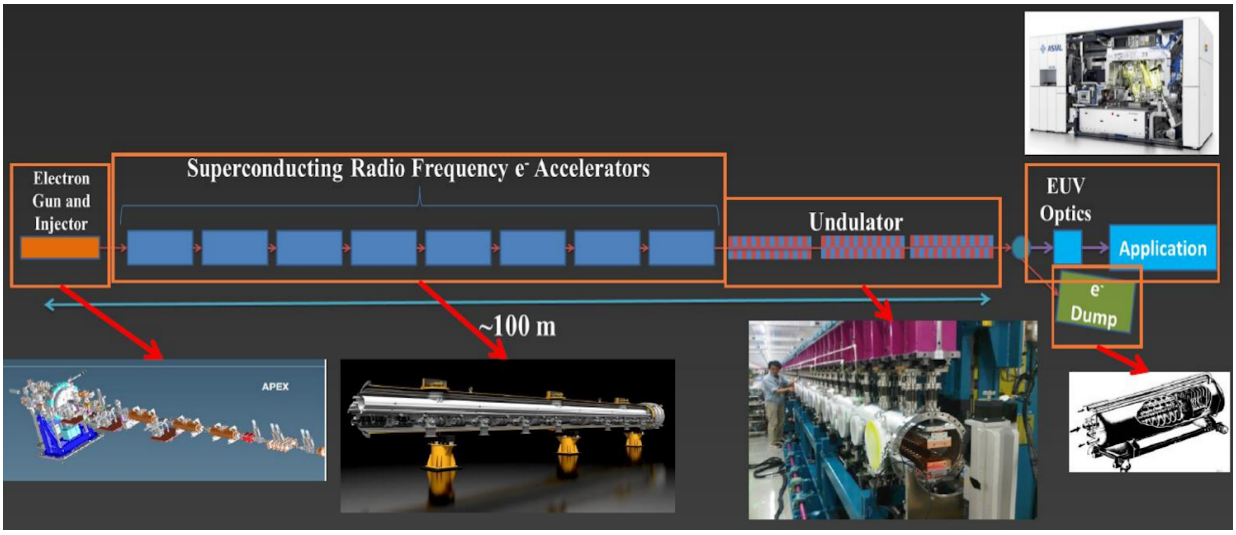


Figure 40: *EUV laser light source [91].*

But the major difference introduced by this new light generation for the lithography tool is the use of reflection optics. It is implemented by means of **multilayer mirrors** -also called Bragg mirrors since their properties are described by Bragg's law- instead of the transmission optics (lenses) used for the conventional *DUV* lithography. The multilayer mirrors are able to reflect the light, achieving larger incident angles for nearly monochromatic light than with conventional mirrors *[92]*. The alternating layers have dissimilar *EUV* optical constant, thus providing a resonant reflectivity when the period of the layers is approximately half times the wavelength *[40]*.

The *EUV* beam follows a well-studied path, first exiting from the plasma to be collected by a condensing mirror, then passing through a point called the intermediate focus (*IF*), and lately illuminating a reflection-type mask after it is reshaped by the illumination optics *[93]*. The *EUV* beam reflected by the mask is exposed then by the projection optics (notice that there is no longer a direct path between the reticle and the wafer through a lens), forming a pattern on the wafer surface. The figure 41 represents the whole *EUV* light path.

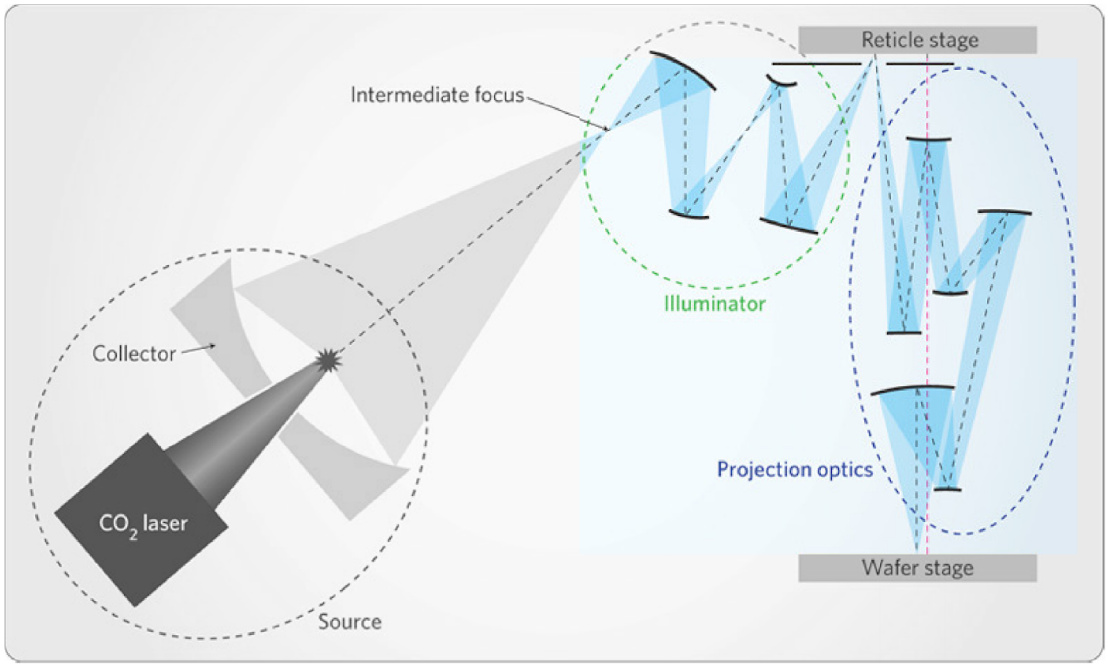


Figure 41: *EUV lithography light path [94].*

If resolution is improved with *EUV* light, the metrology has also to accompany this progress. Therefore, to measure the wafer positions, new inventions have appeared, such as the Sommargren interferometer, which has achieved by using visible light an unprecedented accuracy *[95]*. It measures the wavefront, compared to a highly accurate spherical wave generated by an optical fiber, or by an accurate small pinhole. The resolution achieved is 0.25 *nm RMS* and it is expected to be reduced by an extra 50% *[40]*.

Other differences of the *EUV* lithography versus conventional lithography arise from the masks: they are reflective and not transmissive. They consist of a patterned absorber of *EUV* radiation placed on top of a multilayer reflector deposited on a robust and solid substrate, such as a silicon wafer. The mask reflectance spectrum needs to match with the one from the multilayer-coated mirrors at the optic system *[40]*. The resists are also affected by this absorption-difference, therefore they are structured so that printing occurs in a thin imaging layer at their surface.

3.2. *3D*-integration

Driving in another direction than the concept of reducing the photolithography patterning size, the *3D*-integration appears as a major candidate to meet the performance and cost demands of the new generation-devices. The *3D*-integration, in addition to allow to mix disparate technologies in a stacked chip, offers more choices in terms of process flows [96]: Chip-on-Chip (*CoC*), Chip-on-Wafer (*CoW*) and Wafer-on-Wafer (*WoW*). Making the same distinctions, but using different names -replacing 'chip' by 'die' and inciding more in the bonding connection from a circuit to another circuit, not highlighting the fact that a circuit is mounted on another circuit-, three similar names can be found in the literature [97]: Die-to-Die (*D2D*), Die-to-Wafer (*D2W*) or Wafer-to-Wafer (*W2W*). Despite the terminology discussion, it is clear the cost advantage that can be achieved in *3D*-Integrated Circuits fabrication, therefore the use of the *WoW* (*W2W*) is expected to be inevitable [98]. The three different process flows are shown at the figure 42.

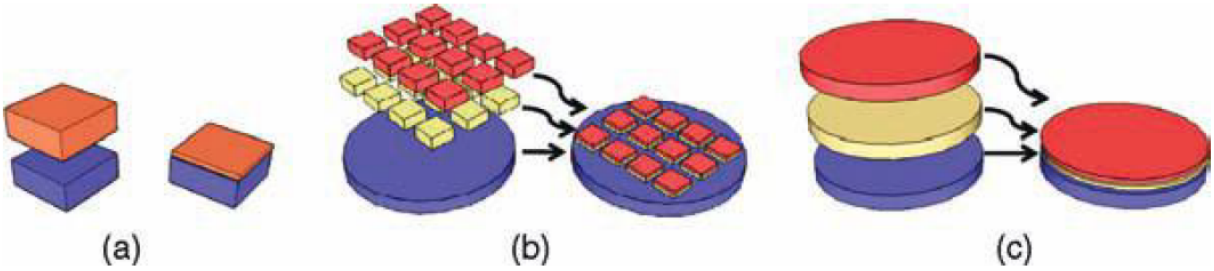


Figure 42: *Major 3D-integration technology platforms [96]. (a) Chip-on-Chip (CoC). (b) Chip-on-Wafer (CoW). (c) Wafer-on-Wafer (WoW) vertical integration.*

Before trying to understand the new technology, let us ask ourselves for the origins of the *3D*-integration: why did it appear? Well, whereas significant advancements were done on the miniaturization of the patterning size, the reduction in feature sizes on the Printed Circuit Board (*PCB*) side has evolved at a much lower rate, thus creating a gap between the features, pitch sizes achievable on the silicon and *PCB* substrates [94]. In order to bridge this gap, several packaging technologies have been developed over the years, as the figure 43 reflects: for instance the through-hole in the 1970s or the surface mount in the 1980s. On the 1990s, new technologies appear such as the Ball Grid Array (*BGA*), System-in-Package (*SiP*) and Chip Scale Packaging (*CSP*), whereas around 2000 the trends were fan-in or Wafer Level *CSP* (*WLCSP*), flip chip *BGA* and package on package. Due to continuous increase in requirements of more performing packages, the need for **advanced packaging** technologies has raised in importance, therefore appearing recently the *2.5D*-interposers (using an intermediary interposer, typically silicon or glass, which is included in the package) and, there we are, the *3D*-integration (stacking-up without that interposer).

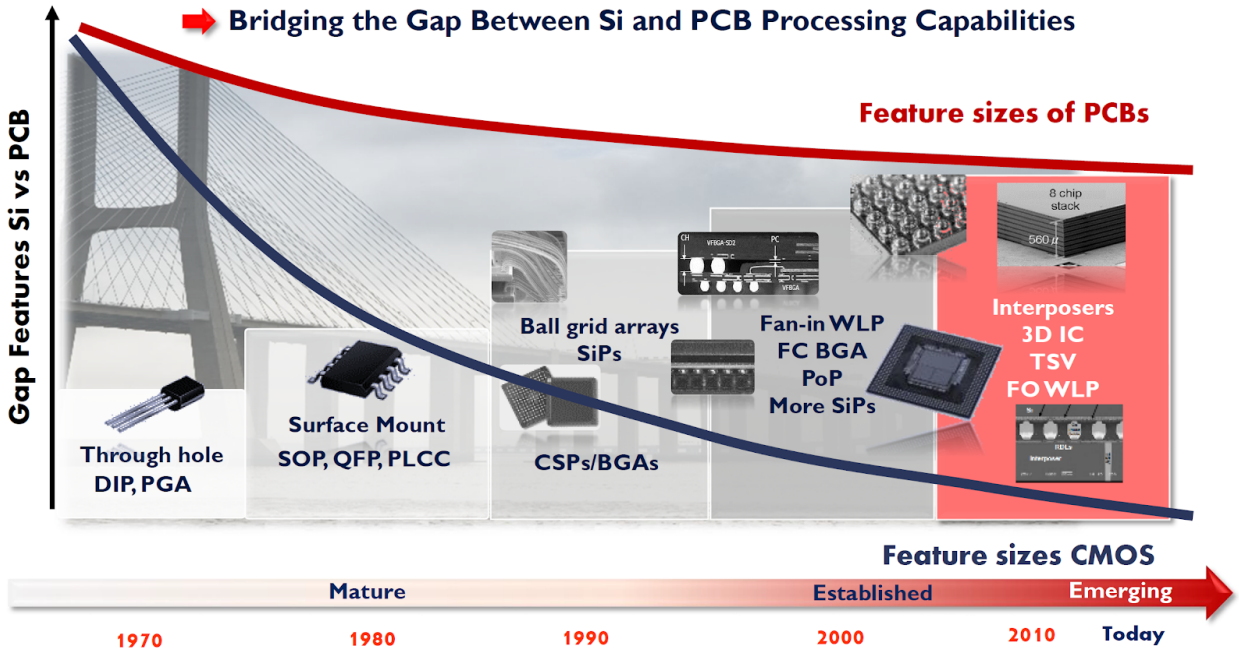


Figure 43: *Microelectronics packaging evolution [99].*

The current society demands for the advance packaging (*e.g. 3D*-integration) include among others *[94]*:

- Reduced cost.
- Small form factor (thinner packages, smaller footprint).
- Lightweight packages.
- Increased Input/Output (*I/O*) density (enabled by smaller pitch sizes).
- Increased integration capabilities.
- Increased electrical performance.
- Reduced thermal performance.
- Increased reliability.

There is no technology that can fit all the current packaging needs, but each market segment will have its own requirements depending on the application. In other words, depending on the functionality and the end-user, some of the previous needs will have more importance than the others. The first section on the *3D*-coverage at this thesis will be focused on the different market segments which are used the *3D*-integration, also showing the cutting-edge by the main producer in each application.

After that, the reader will be driven to the processes to form the *3D*-integration, To achieve the vertical stacking of the layers (also known as tiers), basically two main processes are required, being their features compiled at the figure 44: **bonding** directly the layers over the others and **creating vias to connect all the layers**. Indeed, the whole process for stacking up can be subdivided in four unique sub-processes: Through-Silicon Via (*TSV*) formation, alignment, bonding and thinning *[96]*.

Through silicon via (*TSV*) technology is the most mature approach *[100, 101]* but it is not always suitable for high-density integration for via sizes of 5 *μm* or less. Nevertheless, it performs the electrical (among others) connection between the layers, thus occupying the second subsection in this part about *3D*-integration.

Bonding is closely related to alignment and thinning, even including those sub-processes for some assembly processes (*e.g.* microbump bonding between chips), therefore the third subchapter will be dedicated to analyze its main process variants, as well as the requirements, materials and limitations.

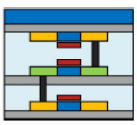
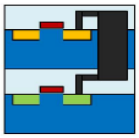
	(a) Direct bonding with Au electrodes	(b) TSV
Bonding medium	Au/SiO_2	Cu - Cu
Circuit density	Highest	Lower
Stackable > 2 layers	Yes	Yes
Interconnect	< 5 μm Smallest	> 5 μm Largest
Schematic		

Figure 44: *Features and schematic of the main 3D-integration processes/technologies [102].*

To finish up with the *3D*-integration section, an insight on the advanced lithography for *3D*-circuits (also known as modulated-lithography) is given. Trying to link with the main core of the thesis, that subsection will review the trends and current technologies at the market, exploring the possibilities of integrating both technologies state-of-the-art for the future user demands.

3.2.a. Market and applications

Even if the reader may think that the whole electronic market is full of *2D*-devices, with regards to the market and products the advanced packaging can be found across various segments *[94]*: from end-user (smartphones, cameras, personal computers, tablets, gaming, set-up box, *TV*s, etc.) to industrial applications (network, high performance computers, servers), transportation (automotive, trains, hybrid and electrical vehicles), medical, military, aerospace, telecommunication and renewable energy. The figure 45 provides an overview of the different market segments used for advanced packaging.

***Figure 45**: Market segments for advanced packaging (e.g. 3D-integration) [103].*

The *3D*-Integrated Circuits have been tested across several of those applications, from *CMOS* image sensors to Micro-Electro-Mechanical Systems (*MEMS)*, Radio Frequency (*RF)*/Power/Analog/Mixed- signal processors, memories, photonics and even *LED*s. Some of those applications are furthered explained below:

- ***CMOS* image sensors**: the first application of *3D*-Integrated Circuits for image sensors was done by electrodeposition (lining) of copper as *TSV*s on a 150 *mm*-wafers. That process was relatively simple, using larger via sizes and small aspect ratios of via diameter to via depth, and a via last type integration *[94]* (the *TSV* is formed from the backside of the wafer after the front-side process is finished). From there, the industry has transitioned to backside imagers (*BSI*) and then to hybrid *3D*-stacked *BSI* with the introduction by Sony of via-middle type integration (*TSV* formation is inserted after *FEOL* but before *BEOL Cu* interconnect) using a full filled *TSV*. The evolution throughout history is represented at the figure 46, achieving Sony with the latest inventions a more efficient utilization of the silicon space by occupying 90% of it with the pixel area. The die

size has significantly reduced, thus enabling processing a higher number of dies at wafer level than previous generations or competing products, consequently reducing manufacturing costs through increased parallel processing [94]. Other way to see the advantages of the *3D*-integration for the image sensors is the possibility of adding extra processing levels within the pixel, but without increasing the pixel size, thus clearly being this segment one of the drivers of the promising development of the *3D-IC*s.

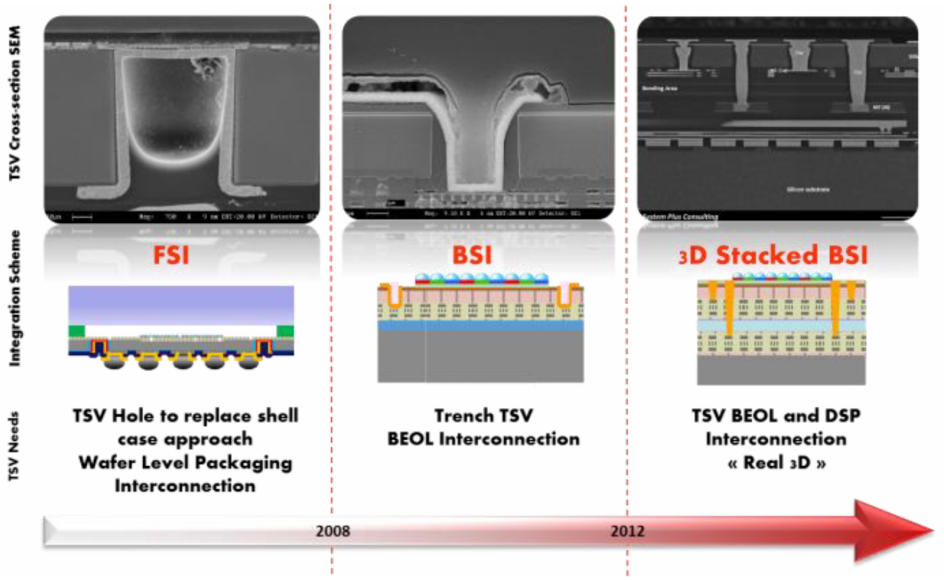


Figure 46: *Evolution of 3D-CMOS image sensors using TSVs [104].*

- ***MEMS***: for those applications, the sensor package cost is relatively high (40-60% of the total cost) in addition to the large size of the package, therefore it is needed a high level of integration to reduce both the form factor and the cost. The *3D*-integration has been adopted for *MEMS* devices, such as gyroscopes and accelerometers, pressure and fingerprint sensors, *RF MEMs* as well as medical sensors such as microfluidic and micro-probes [94]. The standard application was using copper or tungsten electroplated *TSV*s, but Bosch brought into the market in 2014 an integrated *MEMS* sensor with the Application-Specific Integrated Circuit (*ASIC)* based on a via middle *TSV* approach, whose photographs are available at the figure 47. On that device, the *TSV*s were formed through copper electroplating, using 10x100 *μm* vias (10:1 aspect ratio), thus significantly reducing the surface and thickness of the package in comparison to other leading *MEMS TSV* integrated packages [94].

Figure 47: *Bosch accelerometer package using TSV integration [94].*

- **Logic devices:** higher end applications such as Field Programmable Gate Arrays *(FPGA*s), application and graphic processors are also using the *3D*-integration approach. The first device used at the market was the Virtex 7-2000T *[94]*, brought to the market in 2011 by Xilinx. It was built on 28 *nm* technology (the current version uses 20 *nm*), having the *FPGA* partitioned and stacked on a *2.5D*-interposer. The assembly process is Chip on Wafer on Substrate (*CoWoS*) developed by *TSMC [104]*. Another example of the *3D*-integration on the logic devices is the *FPGAs* generation 10 by Xilinx (Arria 10 and Stratix 10) shown at the figure 48: it is used for both wireless communications and military applications, integrating the *FPGA* device, side-by-side with a Hybrid stacked Memory Device (*HMC*) manufactured by Micron. With those devices, Altera has reported a 15% improvement in performance, two times performance increase and up to 70% lower power consumption *[94]*.

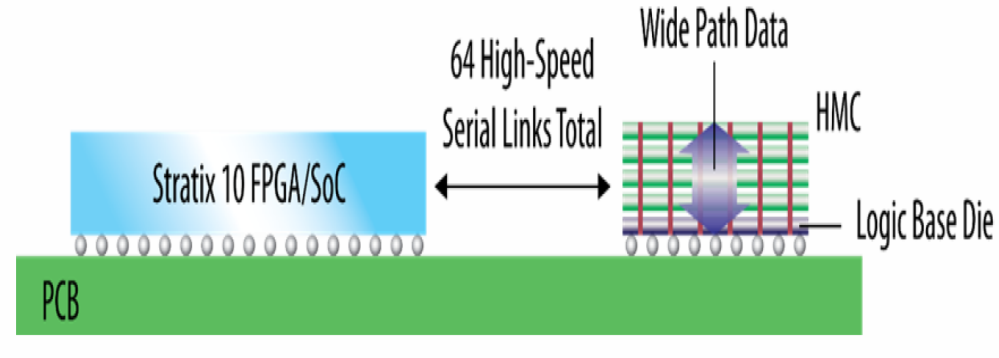


Figure 48: *Schematic of logic devices Arria 10 and Stratis 10 by Altera [105].*

Intel did not want to stay behind in the *3D*-race, thus announcing their first *3D*-processor starting in 2016. By using a stack of 16 *GB* Hybrid Memory Cube (*HMC*) from Micron on a 14 *nm* technology, the processor was said *[106]* to have a bandwidth four times higher, a package 67% smaller and being five times more efficient than competitors.

❖ **Memories:** all the major memory manufacturers in the market (Micron, Samsung, SK Hynix and Toshiba) are currently developing memory products using *3D*-stacking, having started a small volume production for high-end applications (high performance computers, servers and enterprise storage) *[94]*. The figure 49 illustrates the concept launched by Micron in 2014: the Hybrid Memory Cube (*HMC*), which is a package incorporating a high speed logic layer with a stack of memories, offering fifteen times higher performance, 90% reduced form factor and 70% less power consumption *[104]*.

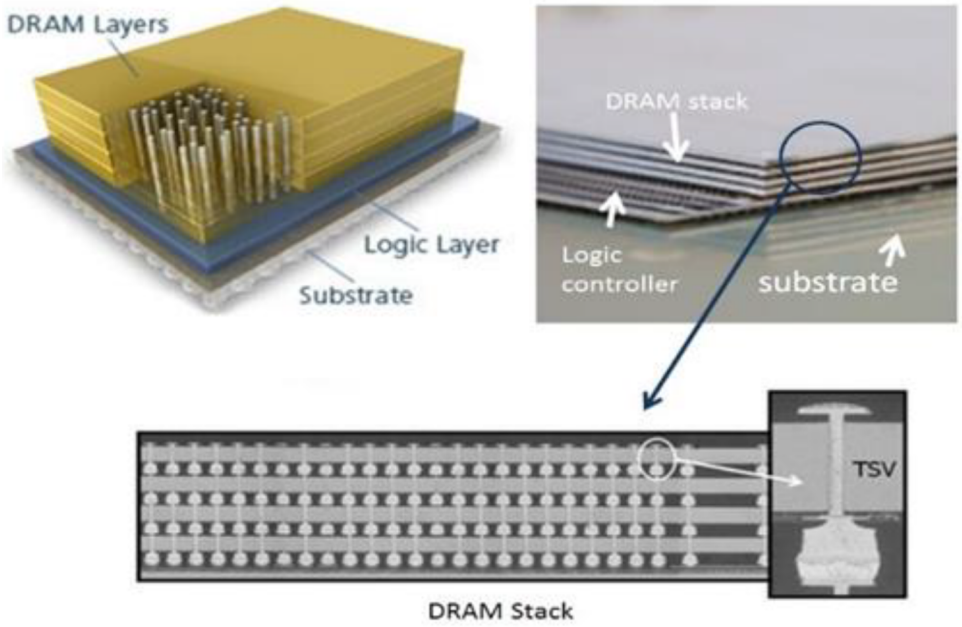


Figure 49: *Hybrid Memory Cube (HMC) by Micron [104].*

Samsung, also in 2014, started the mass production of its *DDR4 DRAM* package module, which is comprised of 36 of 4 stacked *DRAM* chips fabricated in a 20 *nm* technology node and using 7x50 *μm TSV*s for stacking. Performance has been reported *[107]* to be two times faster and having 50% lower power consumption than the traditional packaged *DRAM* using wire bonding. SK Hynix offers the High Bandwidth Memory (*HBM*), which is a stacked memory package built to support the graphics applications for supercomputers and servers. It is used, for instance, in the Graphics Processing Unit (*GPU*) of *AMD* which is built on a 20 *nm* process using a *2.5D*-interposer. It has been reported *[95]* to provide 65% increased performance with 50% less power consumption. With respect to Toshiba, they incorporated a *NAND* flash with 8 and 16-die *NAND* flash memories stacked using *TSV*s. They are targeted for flash storage applications, including high-end enterprise sector, having been reported *[108]* to reduce by 60% the power consumption achieving 256 *GB* capacity.

Even if the high-end memory products is a big business for manufacturers such as *SK* Hynix or Samsung, they are also working on developing solutions for the consumer markets, such as smartphone processors by using package-on-package (*PoP*) type integration, but for the moment the high cost for manufacturing that approach makes that a no-go for High-Volume Manufacturing.

3.2.b. Through Silicon Vias (*TSV*s)

Through-silicon vias (*TSV*s) are the foundation of today's emerging *3D*-integration (and *2.5D-Si* interposer technologies) by connecting multiple dies within a *3D*-Integrated Circuit. These interconnects extend through the silicon substrate, enabling vertical integration and shortened interconnect lengths for reduced size, weight, and power consumption [109, 110]. But not only this, the *TSV*s can also be used to route inter-die signals, deliver power to each die, and extract heat from dies further away from the heat sink [111, 112, 113]. An overall view of a *3D-IC* is shown at the figure 50, where the position abit the chip of the *TSV*s can be seen.

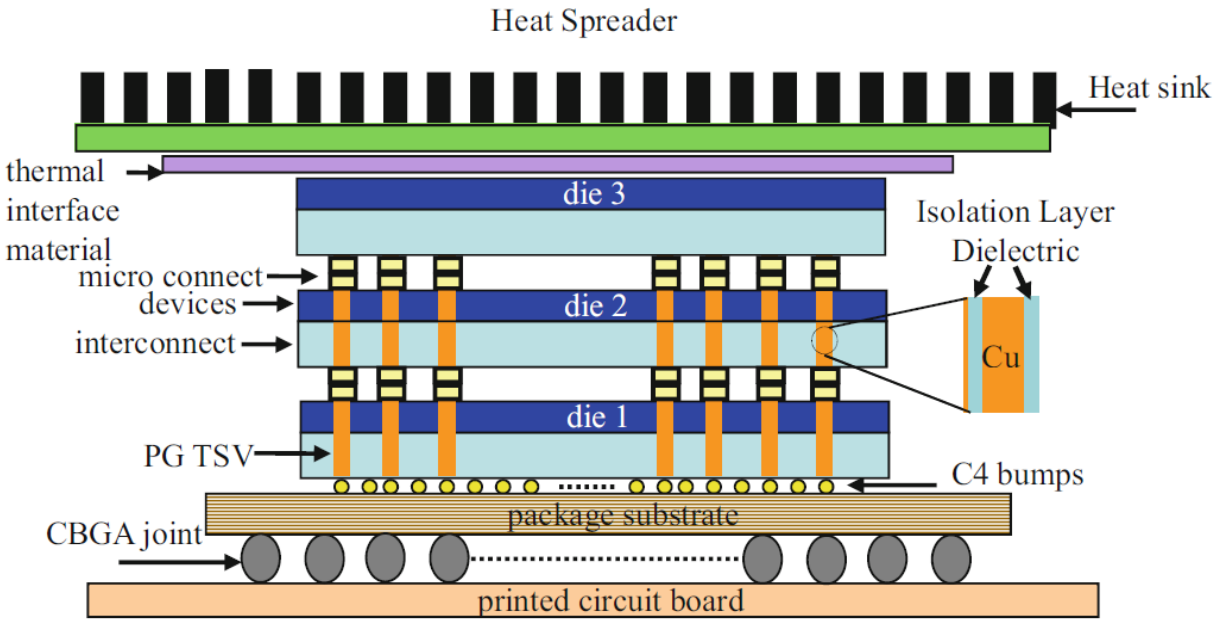


Figure 50: *A 3D-IC with different components such as TSVs [31].*

This chapter will start discussing about the different types of *TSV*s. Not only a classification is done depending on the *TSV*s lay-out, but also upon where the *TSV* formation would be integrated with the *IC* fabrication and assembly (when will be performed the *TSV* in the process, and also if at the foundry or at an outsourcing fab), thus conditioning the overall *TSV* manufacturing process.

Secondly, the process itself will be reviewed. The *TSV* design and process considerations differ slightly for *3D-IC* applications versus the *2.5D*-interposers: the focus will be placed on the *3D*-applications, where a common range of 1-5 *mm* in diameter and 10-50 *mm* in depth (determined by the final substrate) is used [114]. The typical material to build those *TSV*s is the copper, due to its lower resistivity, but Tungsten (*W*) and Polysilicon *TSV*s have also been proposed [115]. Rather than doing the content hugely extensive, the most-conventional *TSV* manufacturing process steps will be developed, letting the avid reader look for variants which are not mainstream at the moment.

Recently, *TSV* reliability and manufacturability (cost, throughput, and yield) have seen increased focus, as these ultimately will determine the potential for *TSV* technology to be implemented commercially on a widespread basis. The last part of the *TSV* section will describe the qualification of the vias, particularly the reliability issues that the *3D-TSV*s encounters. The thermal issue will be addressed, since the *TSV* process steps must be compatible with the *IC* layers already fabricated, generally limiting the processing to a maximum temperature of 400 *ºC* *[114]*. Also, the device proximity effects will be reviewed, thus analyzing how the *TSV* place at the circuit may impact the *IC* performance if near the active circuitry, due to induced stress in the region around the vias *[116]*.

3.2.b.I. Classification

During the last years, different types of *TSV*s fabrication processes have been proposed. The first distinction can be done in terms of the lay-out or shape of the via, whereas the second distinguishes where in the process the *TSV* is done, not only determining the manufacturing process but also the process requirements.

For the first classification, each *TSV* type has associated a material choice, thus fixing the properties and also the application of those vias, each of them having benefits but also technological challenges. One can distinguish different shapes:

- **Regular (square or cylindrical) *TSV***: the most common shape is cylindrical, using metals such as *Cu*, plated *Cu*, tungsten or doped Polysilicon (*poly-Si*), thus resulting in a wide range of resistivities *[31]*. The design is depicted at the figure 51, being simpler than other types, having a dielectric surrounding the metal. As main challenges, the regular *TSV*s have the substrate noise and the thermo-mechanical stress. An advantage of the square shape with regards to the cylindrical one is that the first one allows more uniform insulation layer, thus having a higher breakdown voltage *[117]*.

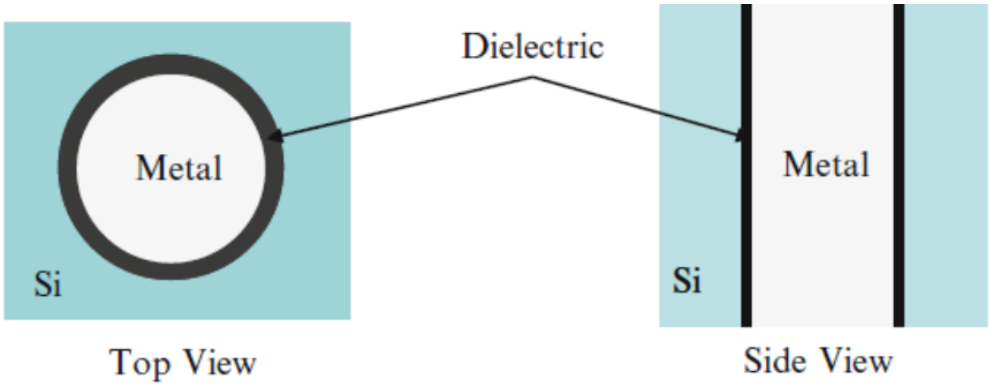


Figure 51: *Regular TSV top and side view [31].*

- **Annular *TSV***: it consists of a polymer-filled core surrounded by a metallic annulus (usually copper), which is separated from the substrate by means of a dielectric layer (conventionally SiO_2). The figure 52 illustrates the differences versus the previous type: the polymer is now replacing the metal at the via core, whereas the inclusion of the last one is sandwiched between the polymer and dielectric. The invention of this type of *TSV* was to overcome manufacturing challenges of cylindrical *TSV*s *[118]*, thus using a simple manufacturing process at a lower cost. Another advantage is the conductivity: to achieve the same conductivity than a regular *TSV*, the required cross sectional area is smaller, thus resulting in improved thermomechanical stability *[119]*.

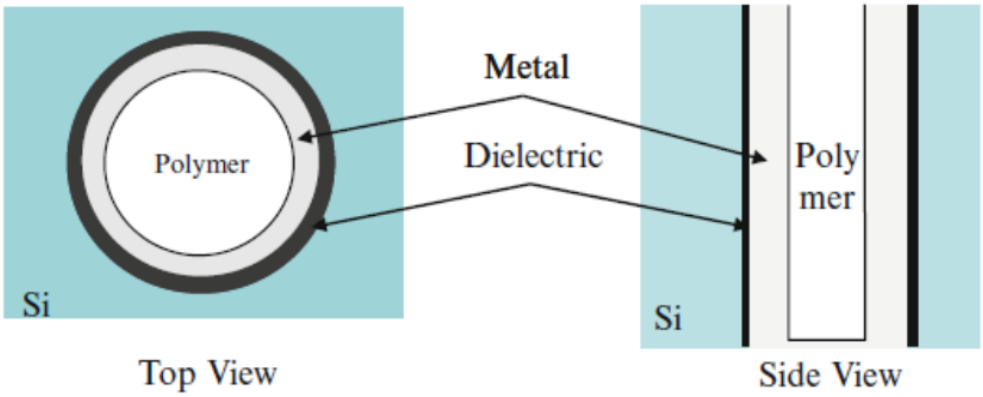


Figure 52: *Annular TSV top and side view [31].*

- **Tapered *TSV***: it is made of a metal and a dielectric, like the regular *TSV*s. However, their side view (see figure 53 for reference) has a different cross section. Introduced by *MIT* Lincoln Laboratory, this type of *TSV*s are built in *SOI* technology *[120]*. As advantages, they do not require insulation, have lower capacitance and a simpler fabrication process *[121]* than the resular *TSV*s. On the other hand, this type of vias are more resistive when compared to a non-tapered one with the same maximal cross sectional area. The control of tapering is also more difficult to be controlled: excessive tapering can lead to *V*-shaped vias, the via slope process has to be optimized *[122]* and a specific interconnect pitch control is required at the bottom side of the tapered *TSV*s.

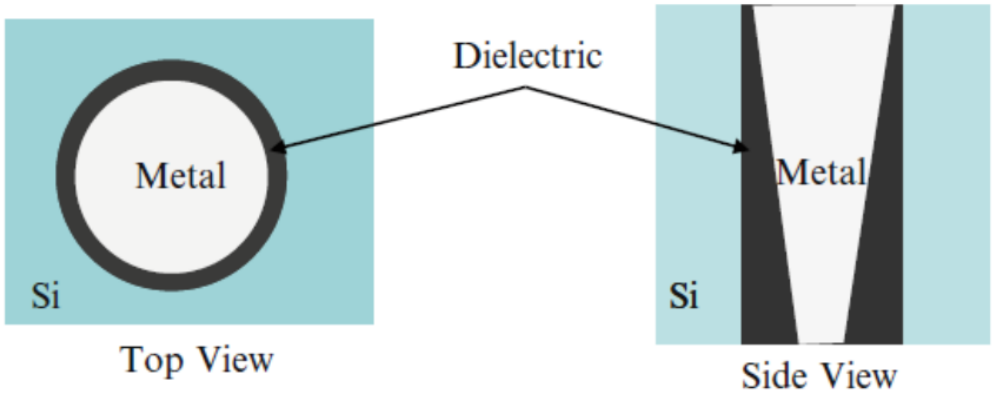


Figure 53: *Tapered TSV top and side view [31].*

- **Coaxial *TSV***: first proposed by Sparks *[123]*, this type of vias have the same structure than a regular *TSV* but with an added surrounding metal layer, as illustrated in figure 54. On that way, they have the main core (inner metal, used for signal transmission) surrounded by an annulus of outer metal (connected to the circuit ground to provide shielding) and the last layer of dielectric. Although few processes have been proposed to fabricate coaxial *TSV*s *[124, 125, 126]*, no mature technology currently exists to fabricate them, having in addition disadvantages such as electrical coupling and critical substrate noise in neighboring active devices *[127]* due to the extensive dielectric liner.

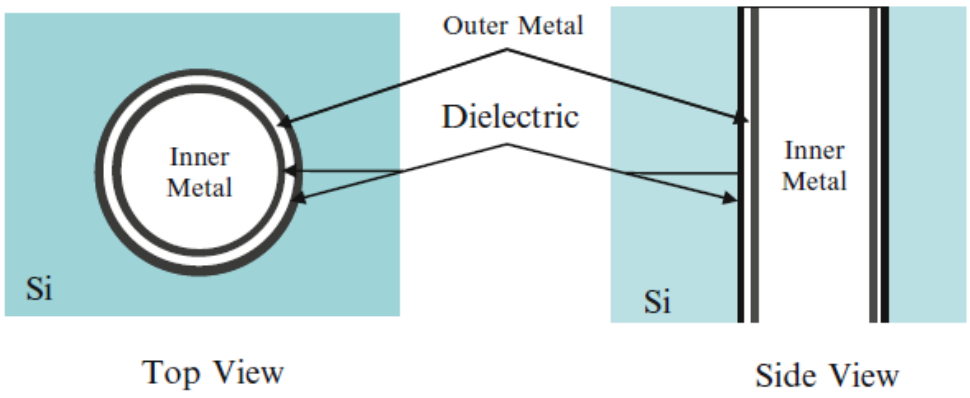


Figure 54: *Coaxial TSV top and side view [31].*

The previous list allowed the reader to understand the different types of *TSV*s in terms of their layout and composition. However, it is even more important the classification of table 6 depending on when, in the overall manufacturing process, the *TSV*s are manufactured, since that is determining the manufacturing line layout, the process constraints and even the physical place where the *TSV*s is done: there are alternatives of performing all the *3D*-integration and then send out the circuit to an external foundry which creates only the *TSV*s.

Table 6: *TSVs fabrication processes classification [31].*

	Via first	Via middle	Via last
TSV manufacturing source	Foundry, IDM	Foundry, IDM	Foundry, IDM, OSAT
Etched materials	Silicon	Oxide, Silicon	Oxide, Silicon
TSV fill material	Poly-silicon	Copper, Tungsten	Copper
TSV fill method	CVD	CVD, ED Cu	Sputter, ED Cu
Temperature restrictions	None	<450°C	<450°C
Applications	Memory	Generic	Image sensors

To understand the "timing" of the *TSV*s within the foundry, let us understand the context of the vias fabrication. The *IC* fabrication from a helicopter view can be divided into two major stages: the **front-end-of-line** (*FEOL*) processes and the **back-end-of-line** (*BEOL*) steps. The first one, the *FEOL*, include the processing steps preceding the first metal layer, whereas the rest of the methods lie in the *BEOL*. The *TSV*s classification is done bearing in mind if the vias manufacturing is done prior to the *FEOL* (*TSV*-first), in between *FEOL* and *BEOL* (*TSV*-middle) or after *BEOL* (*TSV*-last). For the third option, there is a distinction between backside *TSV*-last and front-side *TSV*-last, whereas the backside one is the more common approach. Throughout the last years, the three (or four considering the distinction between the *TSV*-last options) approaches have been used, but the viewpoint of the *3D*-community for most commercial applications is to use the *TSV*-middle *[114]*.

- ***TSV*-first**: this is the simplest process, consisting on fabricating the *TSV*s in the bulk substrate before any devices or interconnect layers are formed *[128]*. The necessary steps are sketched in figure 55. This approach does not require any backside lithography and it is compatible with all the *FEOL*-processes, including high temperature thermal oxidation, therefore can be used to deposit *TSV* insulation (under the condition that the *TSV* conducting material is *poly-Si*). Being a highly reliable (electrically and mechanically) process, those types of vias can be formed with densities larger than 100000 per cm^2 and aspect ratios of 25:1 *[129]*. However, since the limitation of only using the *poly-Si* as the *TSV* conductor, and the inherent limitations such as the via resistance, the *TSV*-first approach is no longer viewed as a viable option for *3D-IC* manufacturing *[114]*.

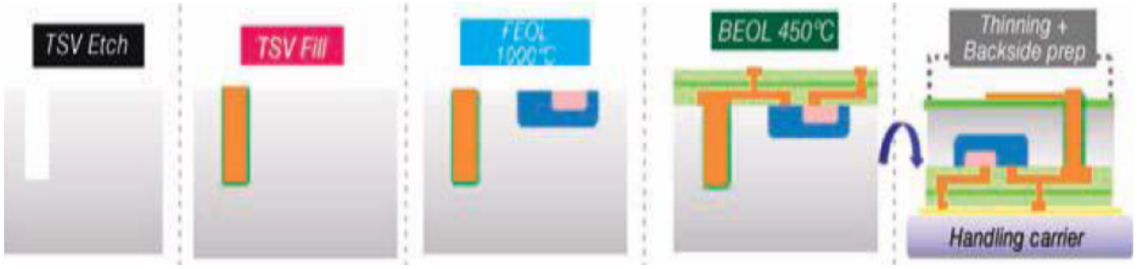


Figure 55: *TSV-first approach process flow [114].*

- ***TSV*-middle**: at this approach whose steps are depicted in the figure 56, the vias are made at the *IC* fabrication facility (or at the own foundry for large *IC* foundries) after the *FEOL* active device layers have been created, and prior to the *BEOL* interconnect wiring layers. With regards to the materials used, at this approach the vias are conventionally fabricated with *Cu* or *W* deposited by Chemical Vapor Deposition (*CVP*) or Electric Discharge (*ED*) *[129]*. To build them up, the *TSV*s are initially formed as blind vias, being revealed later in the process from the back during wafer thinning to allow the backside interconnection and routing. Typically solder bumps or microbumps are added for interconnecting to another tier or substrate. One advantage of the *TSV*-middle is the lowest consumption of real estate, since they can be made small while with high accuracy, being the *BEOL* metal layers routed over the *TSV*s *[114]*. Another advantage, making this approach the most used nowadays, is the compatibility with the rest of processes (wafer thinning, *TSV* reveal , etc.), since a lot of progress has been recently done in temporary carrier wafer bonding.

Figure 56: *TSV-middle approach process flow [114].*

- ***TSV*-last**: this approach allows the whole *FEOL* to be finished, and then build the vias at anytime during and after *BEOL* [130, 131], being the steps illustrated in figure 57. As mentioned before, the *TSV*-last approach has two different possibilities, depending on the side where the vias are formed: either at the back or at the front side.

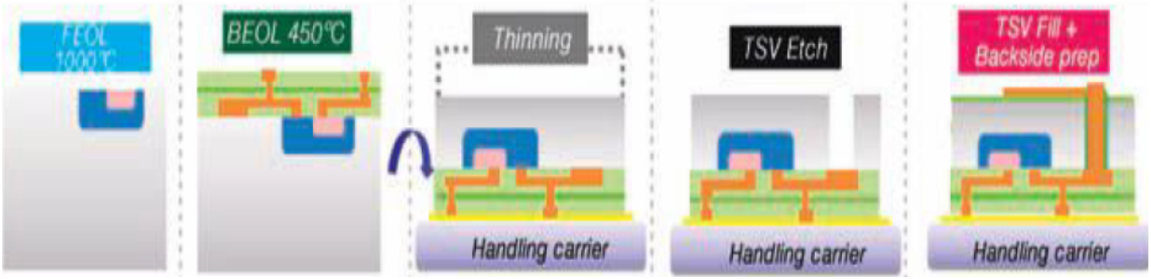


Figure 57: *TSV-last approach process flow [114].*

  - **Backside *TSV*-last**: on this approach the vias are formed from the backside of the substrate after the wafer has been thinned, landing the vias on the front-side metal. The figure 58 illustrates the overall process flows: a handle-wafer is attached to the front side, and the *TSV*s are connected to the lower metal layers (M_1 or M_2) of the die to avoid etching through the higher metal layers. This approach has been adopted for producing *CMOS* image sensors (used at mobile devices), since they use relative low aspect ratio periphery *TSV*s [132, 133], often with sloped sidewalls and a conformal metallization layer (unfilled *TSV*s). However, the backside *TSV*-last approach has numeral drawbacks: first of all, this process requires a low temperature *TSV* insulation technique to minimize thermal effects on already fabricated devices and interconnect [31]. Secondly, it requires back-to-front lithography alignment capability. Not only that extra process is needed, but also a specialized etch step -sometimes called a "bottom-clear etch"- is required to reopen the metal at the base of the via, while not removing the deposited insulator from the *TSV* sidewalls [114]. Furthermore, still some other manufacturing challenges have to be mastered, such as wafer-thinning and handling, and properly opening the insulation at the vias base to make reliable electrical connections. Last, but not least disadvantage of this

approach, is that the metal surface can be affected by exposure of the numeral etching plasmas, thus being difficult to restore using standard sputter etch techniques since it is as the bottom of a deep via. Having all the highlighted issues in mind, this process flow is unlikely to see widespread use for higher density, higher aspect ratio *TSV* applications [114].

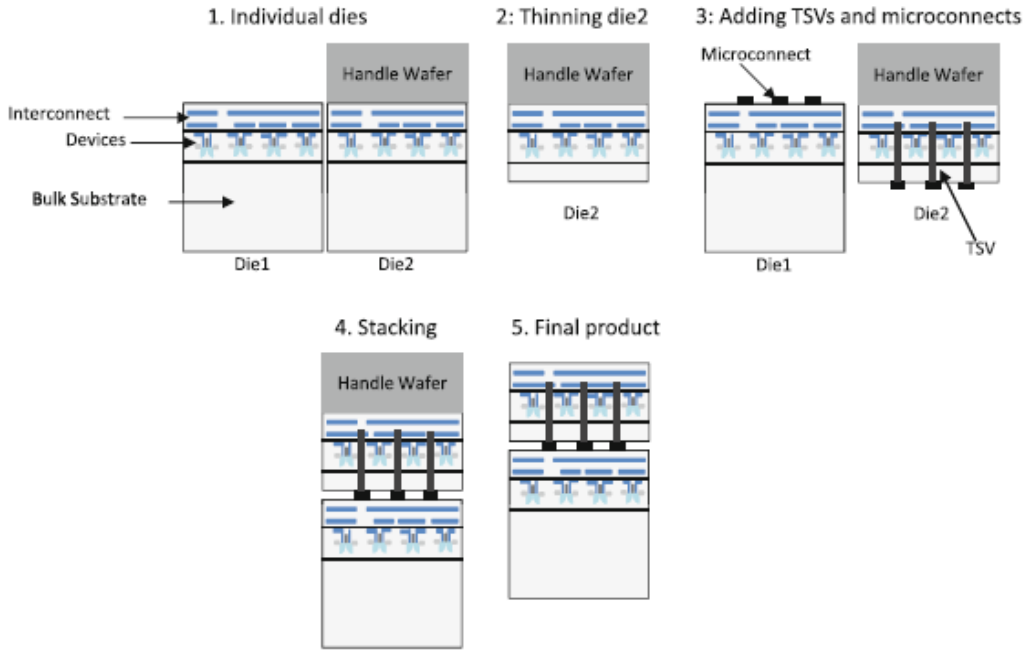


Figure 58: *Backside TSV-last process flow [114].*

➢ **Frontside *TSV*-last**: in this approach, the blind vias are formed from the front of the wafer, and then the rest of the process flow is similar to the *TSV*-middle methodology, including the backside *TSV* reveal and metallization. The complete process flow is depicted in figure 59 for reference. This approach is mostly used for defense and aerospace applications as well as for advanced medical imaging, since those sectors need a high-performance *TSV* caring less about the cost and product volumes. As concern -apart from the price- this approach needs the wafers to be designed and fabricated with "*TSV* exclusion" areas, free of metal and active circuitry. On those areas, the *TSV*s can be etched through the Interlayer Dielectric (*ILD*) stack and the *Si* layer, without obstructing the metal or damaging the active circuitry [31].

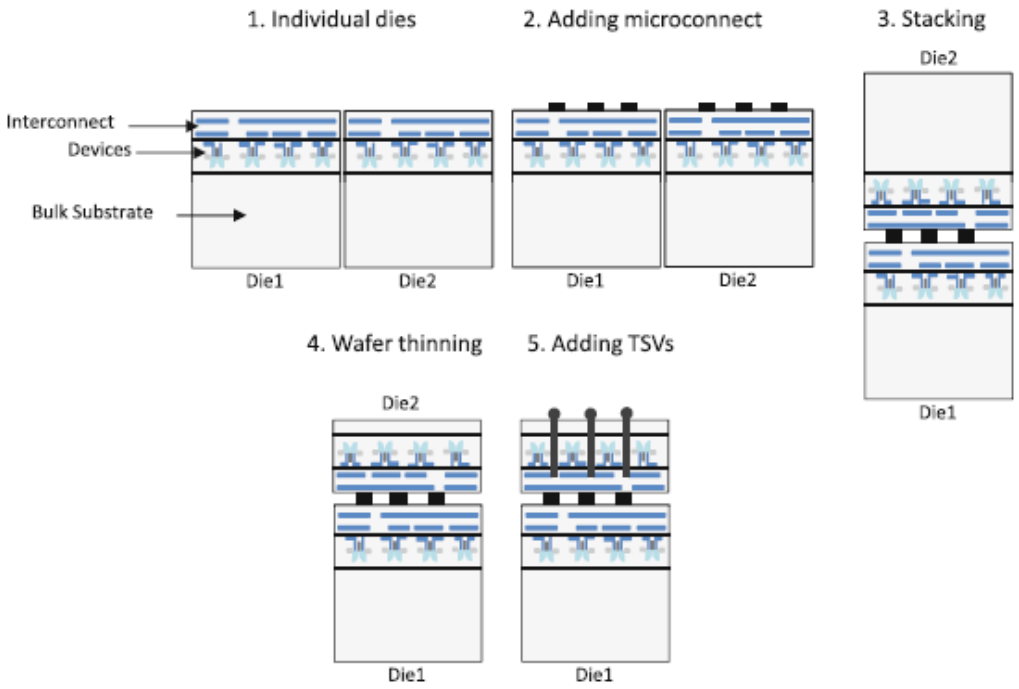


Figure 59: *Frontside TSV-last process flow [114].*

3.2.b.II. Process description

The different steps required to form a *TSV* depends upon the approach taken by the factory, *i.e.* there would be some differences in the flowchart (and/or at the process parameters/materials) if a *TSV*-first would be chosen instead of a *TSV*-last. Due to the fact that the most common approach nowadays is the *TSV*-middle, and *3D* took the advantage over the *2.5D*-interposers, that combination would be used for the process steps description at this section. It is beyond the scope of this thesis to really deep into every single process, but it is more oriented to give the reader an overall understanding of the necessary steps to achieve the vias formation. Each process step will be characterized, mentioning also the requirements and the main challenges to get the *TSV* in mass production.

1) ***TSV* etching/patterning:** the process is performed by Deep Reactive Ion Etching (*DRIE*), which was introduced by Bosch in the mid- 1990s and is widely used in *MEMS* fabrication *[134]*. The technique alternates steps of etching and passivation to enable etching of deep features in *Si* with vertical sidewalls, thus providing high selectivity to the photoresist or the SiO_2 mask layers. To achieve that, an Inductively Coupled Plasma (*ICP*) source is used, firstly using SF_6 as element source to etch in the *Si*, and later using C_4F_8 for the sidewall passivation. The process is cyclical, where the four steps sketched in figure 60 are repeated: in each etching step, a small amount of *Si* is removed, and then the passivation layer is applied over all of the surfaces. After that, the passivation is removed from the bottom of the feature, allowing the *Si* etch to continue downward, but still remaining on the sidewall and protecting it from further etching.

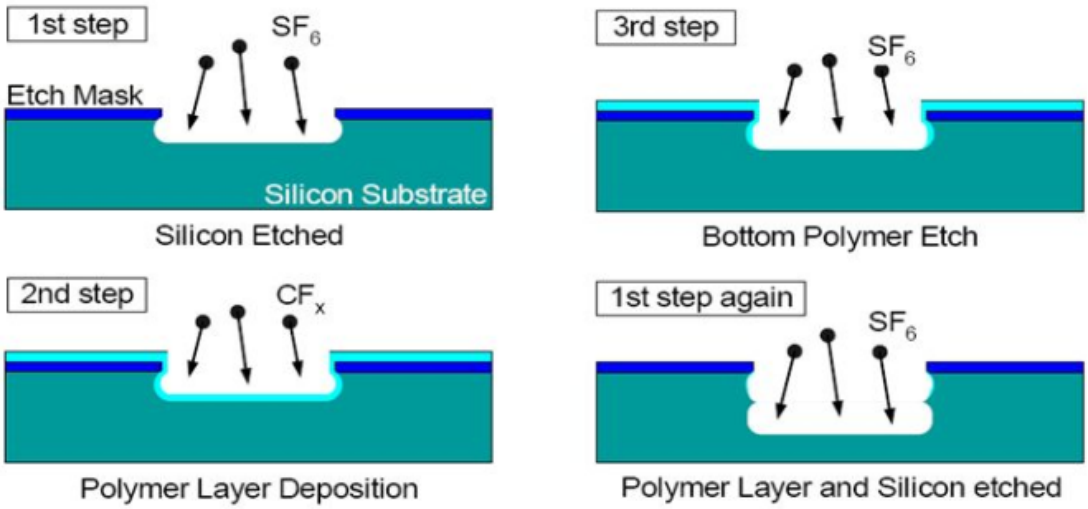


Figure 60: *DRIE process steps [135].*

The process repetition generates a easy-to-recognize pattern which results in a vertical feature sidewall, made up of a series of small ridges, also known as “scallops”. Since it is required to etch small vias with high throughput and minimal sidewall roughness, the trends today go into the direction of reducing the scallops to enable sufficient coverage of *TSV* insulation and seed metal in high aspect ratio vias [31]. The advancements in plasma source has allowed to shorten the process cycles, appearing at the market alternatives which are “scallop-free”. The figure 61 plots both structures: with and without scallops.

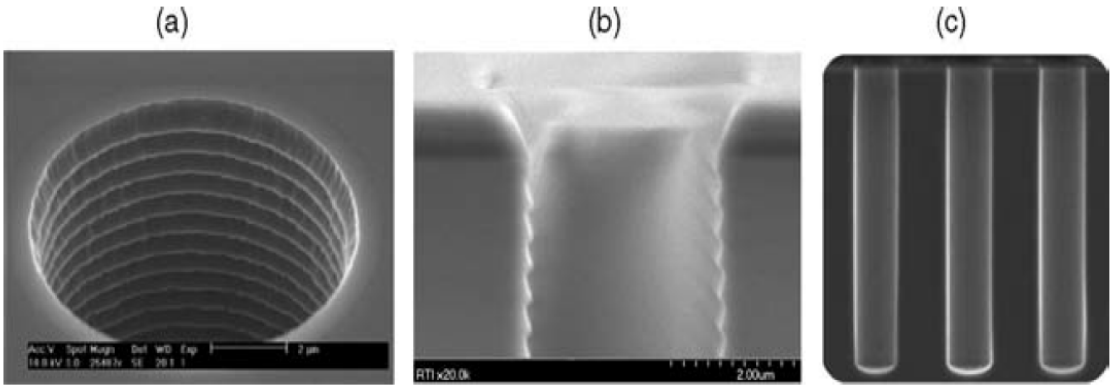


Figure 61: *DRIE features etched in Si [31]. (a) Top view of TSV with sidewall scallops. (b) Cross section of scallops in Si trench. (c) “Scallop-free” TSV etch.*

2) ***TSV* insulation:** this step is accomplished by deposition of a highly conformal SiO_2 layer. Three processes are needed for insulation, as depicted at figure 62: firstly an etching is performed on the top surface, followed by the SiO_2 layer deposition which later will be etched away at the *TSV* itself. For the deposition, the most conventional process is Subatmospheric Chemical Vapor Deposition (*SACVD*) using O_3/*TEOS* or, when lower temperatures are required, the used of Plasma-Enhanced Chemical Vapor Deposition (*PECVD*) is typically used.

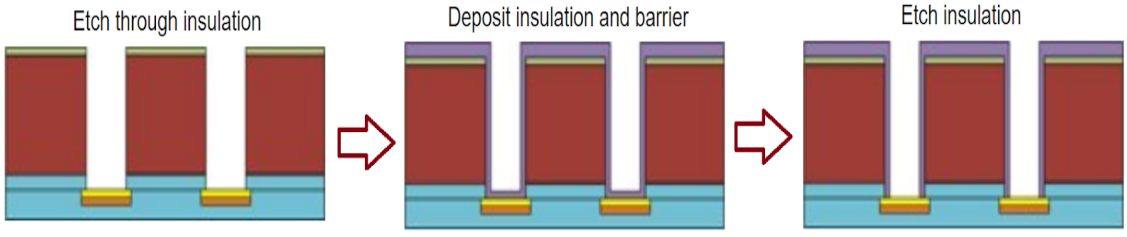


Figure 62: *TSV insulation process steps. Source: own, based on [136].*

Since the layer is deposited after the *FEOL* (to bear in mind that this description is for *TSV*-middle approach and also in this case would be applicable for *TSV*-last, but not for *TSV*-first), the deposition temperature has to be limited to a range of 400 *ºC* maximum. Achieving conformal insulator coverage can be a challenge without using high-temperatures, specially for high aspect ratio vias, vertical profiles and sidewall roughness. Other requirement for the *TSV* insulator films is to have suitable electrical insulation properties, such as dielectric constant, leakage current or breakdown voltage.

3) ***TSV* metallization**: after the via has been isolated, the metal layer is deposited (see figure 63 for reference). The most common approaches nowadays are based on a "bottom-up" growth process Electrochemically Deposited (*ECD*) of copper [135, 137], although *CVD* of tungsten is still used for small-diameter holes or annular vias [31]. For the *Cu* metallization schemes, it is necessary to deposit a thin *Cu* seed layer prior to the metallization, typically by Ionized Metal Plasma (*IMP*) sputtering, achieving continuous coverage along the via walls to enable uniform and void-free fill deposition. Furthermore for this process approach, after the *Cu* metallization, it is needed to add a barrier metal between the copper and the SiO_2 layers, typically being *TiN* or *TaN* deposited by *IMP* sputtering or Metallo-Organic (*MO*) *CVD* processes [138]. An alternative appeared recently at the market consisting of using *MOCVD Cu*, since it can produce nearly 100% conformal deposition in high aspect ratio features and can be used to fill small *TSV*s [139, 140]. However, it is not very practical for using at large vias due to limited deposition rates, having the process a high cost and being the throughput too low for a much wider adoption by the semiconductor industry.

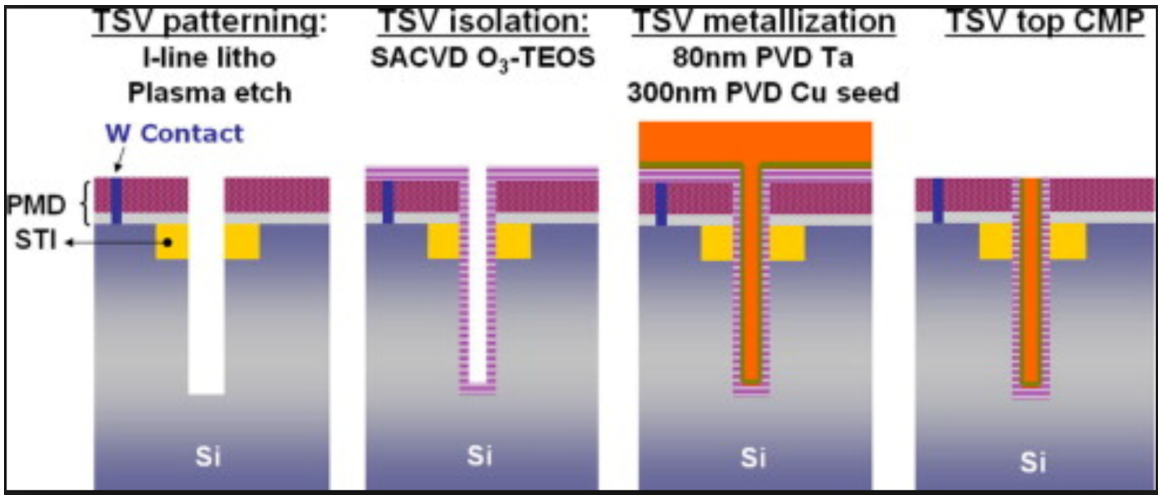


Figure 63: *Typical TSV formation process steps. Metallization comes after the isolation [141].*

As main challenges for the metallization appears the film stress and the wafer bow, limiting the thickness of the metal to be deposited. Another concern is the plating voids which can lead to yield problems during subsequent fabrication steps, thus requiring the addition of chemistries to accelerate, suppress or level the chemical process. By adjusting these, it is possible to slow plating at the surface and top portion of the via, while promoting plating near the bottom of the via, resulting in a bottom-up *TSV* fill profile [135, 137], having also importance to maintain the additive levels to keep consistent the *TSV* filling. As last concern one can mention the throughput, since the fill time has to improve to make the process cost viable for commercial production use.

4) **Overburden removal by *CMP***: the last step on the *TSV* formation is to remove the excess of deposited metal. This is typically done by *CMP*, which is a process well established due to the emergence of *Cu* dual-damascene *IC* metallization [31]. The process is illustrated in figure 64, typically using a chemical component which is poured by a polishing slurry into the wafer, in order to soften the material, and after that a pressure is applied in vertical direction so that the top surface is polished at the same time that the wafer is spun at a high speed.

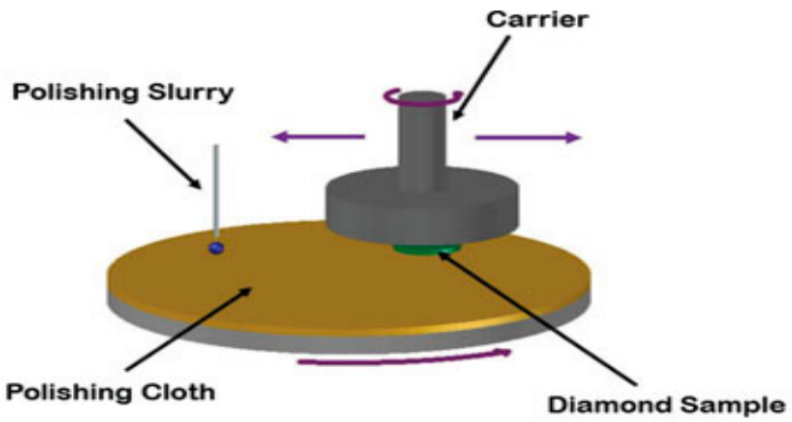


Figure 64: *CMP process [142].*

The main concern for the process is the throughput, since larger size of the *TSV*s -with regards to the *BEOL* interconnects- means thicker overburden layer and longer polishing times, thus becoming one of the bottlenecks of the overall *TSV* formation process. Reductions in *TSV* size, high-rate *Cu CMP* slurries and development of bottom-up *Cu* plating approaches are helping to minimize the thickness and, consequently, the polishing time to make the process more competitive at today's market.

5) ***TSV* annealing:** even if this process is not mandatorily needed for the *TSV* formation, it is nowadays added with the goal of reducing the *Cu* protrusion effect, which can induce stress in metal and dielectric layers above the *TSV*s even causing mechanical failures [143, 144]. Therefore, the *TSV* annealing has been reported [145] as a solution to stabilize the effect (check the figure 65 for comparison of the effect with and without annealing) being the process established after plating and *CMP*, and before depositing additional layers. The annealing consists of heating the *TSV*s to temperatures or 400 *ºC* or more, thus stopping the extrusion and becoming the via "stabilized" for further processing. If the observed effect is already significant, a brief "touch-up" *CMP* may be used to restore planarity [31].

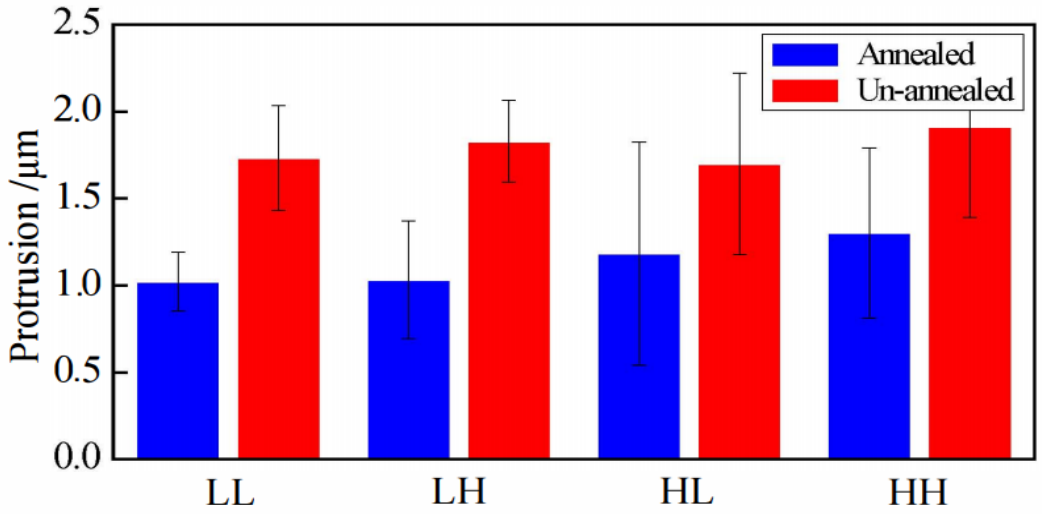


Figure 65: *Comparison of protrusions between annealed and unannealed TSV-Cu after ten thermal cycles [146].*

6) **Temporary carrier wafer bonding/debonding, wafer thinning and *TSV* reveal:** even if the processes depicted at figure 66 do not contribute to the *TSV* formation itself, it is important to mention them since they are necessary to make the later interconnection between the tiers. The first step is to attach a temporary carrier wafer (or interposer substrate for *2.5D*), which provides the mechanical support during thinning and processing of backside layers. After that, the wafer is thinned to its final target thickness by a combination of backgrind (process to reduce the thickness) and *CMP*. In order to control the device wafer Total Thickness Variation (*TTV*), it is important at this step that the thickness of the carrier wafer and adhesive are minimized during the wafer bonding. Careful measurements must be made of each layer and the full stack prior to thinning, so that the *TTV* induced by the thinning processes can be determined and controlled [31]. To finish up the cycle, the *TSV*s are revealed from the backside for later *3D*-interconnection, by means of a plasma etch process which removes the remaining *Si* and reveal the vias, which are still encapsulated in the via dielectric layers.

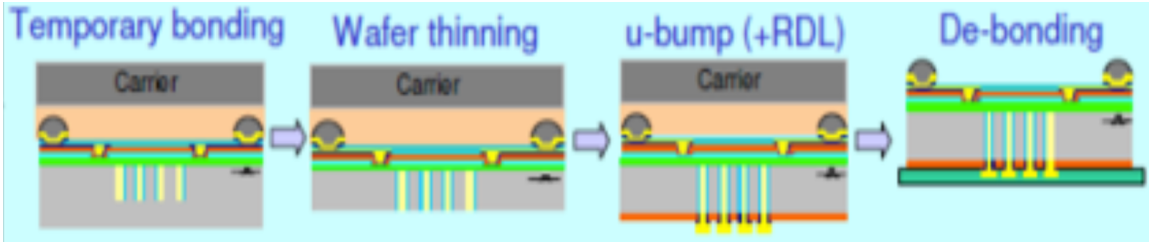


Figure 66: *Temporary bonding/bonding, wafer thinning and TSV reveal process flow for conventional 3D-integration [147].*

3.2.b.III. Process characterization: yield and reliability concerns

Now that the reader is acquainted with the different types of vias that exist, and the process flow for their formation, it is time to understand how the *TSV*s can be characterized. At the very end, as other processes, it has to be modelled, quantified and tested.

First of all let us talk about the **modelling**: how is represented a *TSV* in a conventional circuit and with which parameters? Well, the convention is to use traditional resistive, inductive and capacitive elements thus translating the *TSV* into a conventional circuit. Its performance -characterized by the signal delay and the power dissipation- is determined by those *RLC* elements. Different approaches have been described to estimate the parameters: the first one uses simple formulas and three-dimensional electrostatic simulations *[148]*:

$$R = \frac{\rho_m h}{A_{eff}} \qquad (3.2.b.III.1)$$

$$C = \frac{\varepsilon_0 \varepsilon_r S_a}{t_{ILD}} \qquad (3.2.b.III.2)$$

At the previous equations, h represents the *TSV* height, A_{eff} the cross section area of the via, S_a is the sidewall area, t_{ILD} the dielectric liner thickness, ρ_m the material resistivity, and ε_r and ε_0 the relative permittivity of SiO_2 and of free space, respectively. With this model, for a 50 *μm* high square *TSV* of diameter 5 *μm* and 1 *μm* sidewall thickness, R_{via0} is 43 *mΩ and* C_{via0} is 40 *fF [114]*.

Another approach to model the *TSV* was to fabricate a ground-signal-ground *TSV* circuit as the one in figure 67, in order to obtain the *S*-parameters by micro-probing. The circuit parameters are determined by fitting the *S*-parameters from the model to the measured ones at the fabricated *TSV*s, thus obtaining R_{via0}=12 *mΩ and* L_{via0}=35 *pH* at a frequency of 0.1 *GHz for a* 50 *μm* high square *TSV* of diameter 55 *μm* and pitch 150 *μm [149]*.

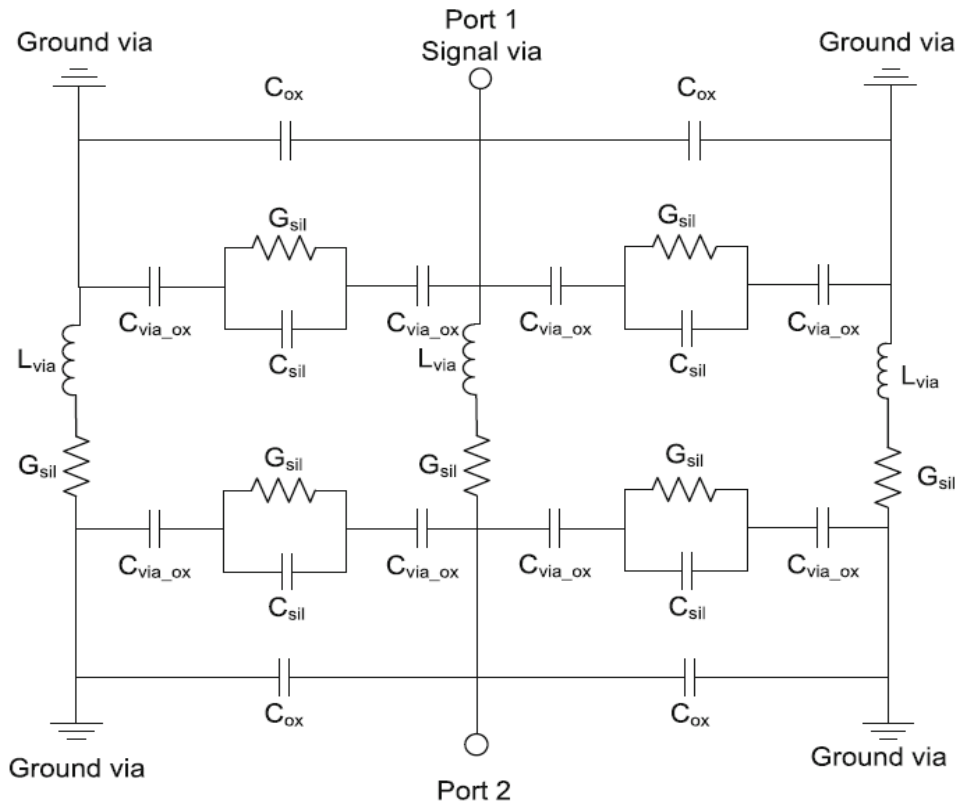


Figure 67: *Electrical circuit model of TSV [114].*

A third approach to model the *TSV*s was to fabricate different types of blind vias to study the electrical characteristics of dielectric liner *[117]*. The measurement was a breakdown voltage of 40 *V* and a capacitance of 50-60 *fF* for real-built square and cylindrical *TSV*s with height 80 *μm* and thickness between 20 and 100 *μm.*

The last approach is to accurately characterize the inductance. To do so, it is essential to include a return path directly based on the design and layout of specific interface circuitry, having been demonstrated *[150, 151]* that the *TSV* inductance is low, in the range of 0.3 to 0.9 *pH/μm.*

Having the vias modelling, the next step is to check how good the *TSV* is. To do so, the importance figure of **yield** appears, defining the ratio between the "good" (in accordance to a criterium) *TSV*s with respect to the total manufactured vias. The yield for the whole *TSV*s obviously depends upon each individual process step yield, therefore quality in each sub process has to be achieved in order to get good overall yield. Starting by the etching, that process is relatively well established once optimized for a specific rate and desired sidewall characteristic, thus achieving a very repeatable process provided that the chamber is properly maintained for etch consistency. Following by the *TSV* liner steps, the main considerations in terms of yield are related to achieving a continuous and conformal film coverage, while maintaining a consistent electrical insulation and barrier properties, which is usually achievable,

thus getting a reliable and consistent process. The filling of *TSV*s by *Cu ECD* is a very critical process, thus needing careful control to maintain consistency, not only by regular bath chemical analysis, but also by additive adjustments and bath replenishment [31]. With regards to the plating step, the main yield risk is the formation of voids in the *Cu* via fill due to pinch-off in the *Cu* plating near the top of the *TSV*, being somewhat difficult to be detected using non-destructive methods unless high-resolution *X*-ray imaging or microwave acoustic microscopy are used. Once the *TSV* is successfully formed, it is not yet time to define a *TSV* as valid, since the attention drops into the control of *TTV* in the temporary carrier bonding and thinning process, so that the device wafer is thinned uniformly to its target thickness.

Yield and reliability are very correlated: whereas the first one defines the functionality of the circuit at a first moment, some failures may appear after usage. The **reliability** figure thus is trying to detect potential defects at the factory which can end in a failure, thus protecting the potential customer of the application. The main reliability *TSV*s concern is the Coefficient of Thermal Expansion (*CTE*) mismatch between the copper and the silicium. This can result in stress around the *TSV*s, being shown figure 68, creating potential device proximity effects that can impact the performance of active devices. To avoid this, the *TSV* dimensions are trying to be kept as small as possible, and also around the *TSV*s it is implemented the so-called Keep Out Zones (*KOZ*), creating a safe distance between *TSV*s and active devices [116]. To design the *KOZ* size in order to eliminate the proximity effects, the dependencies with *TSV* diameter and the particular device technology have to be analyzed.

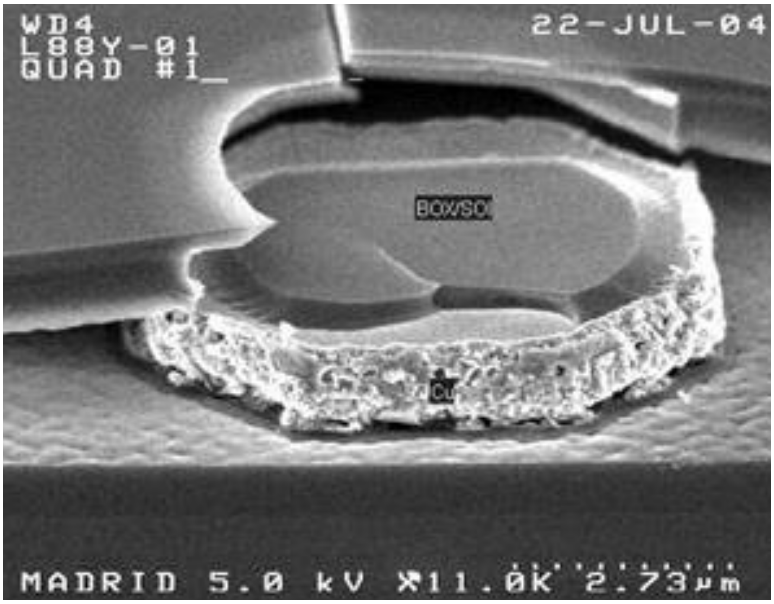


Figure 68: *Induced stress at TSV due to CTE mismatch [152].*

Another concern is the issue highlighted in figure 69: the *Cu* protrusion effect, which arises at the *TSV* anneal process, consisting in having hillocks formed during the heating process, thus resulting in a permanent surface topography *[153]*, creating a potential for thermomechanical failures in subsequent layers. To address this issue, the solution is to limitate the via size, optimize the *ECD* chemistries and perform a stabilization anneal prior to building up additional layers of metal and dielectric over the *TSV*s *[31]*.

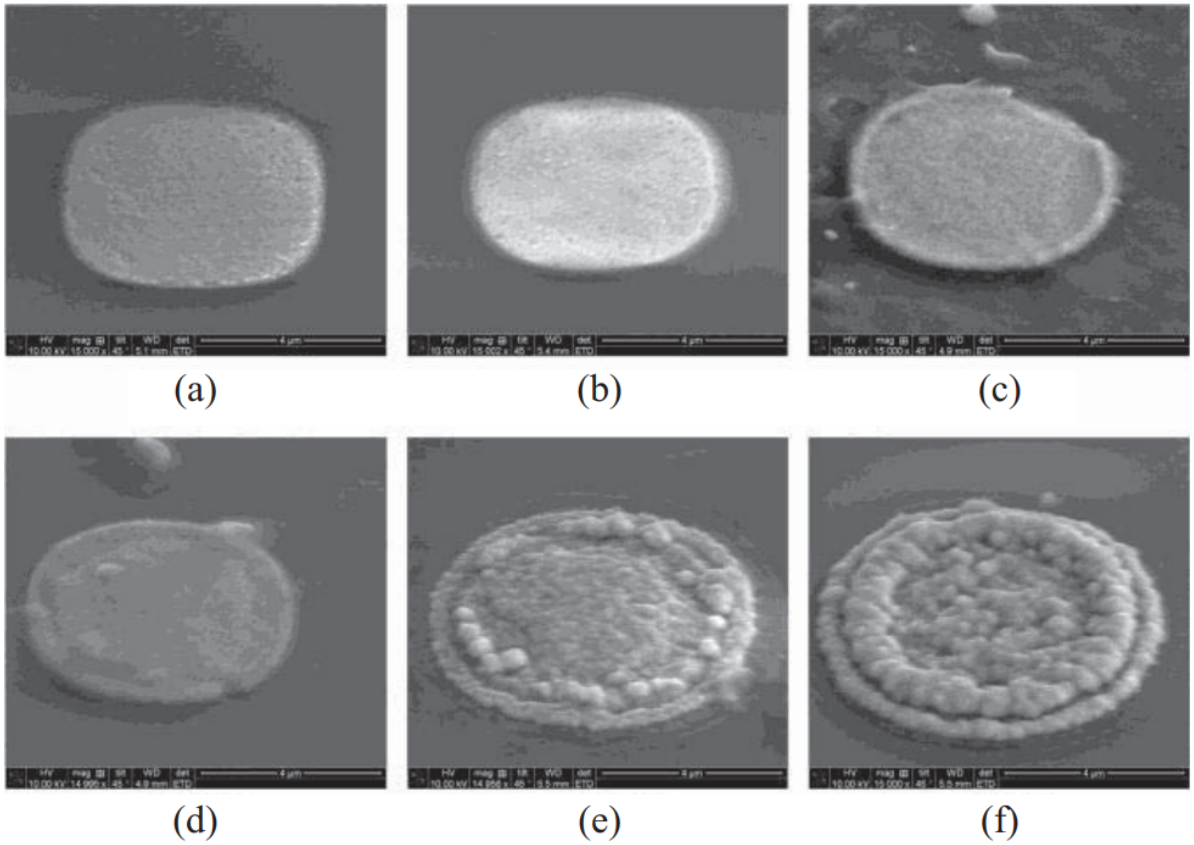


Figure 69: *SEM images showing Cu protrusion for different annealing conditions [154]. (a) 25ºC. (b) 250 ºC. (c) 300 ºC. (d) 350 ºC. (e) 400 ºC. (f) 450 ºC.*

To mention as well as major reliability issue the plating voids, since they can trap chemicals which can lead to contamination or corrosion. To eliminate their effect it is necessary to use optimal *ECD* techniques and process monitoring, ideally using non-destructive void-detection methods.

The last two reliability concerns are the insulator integrity and the interconnect degradation. The first one can makes the current to leak as a consequence of insufficient sidewall coverage, thus potentially damaging the quality in further steps such as *TSV* reveal or die bonding. For the interconnect degradation, the concern is about the electromigration, which have to be addressed through proper materials selection and process controls.

Even if good progress has been done in the last year at understanding the *TSV* formation process, still the yield and reliability issues make the cost too high to continue scaling the *3D*-circuits. Therefore, a better know-how of the process will allow the integrated circuits using three dimensional approaches to become more competitive.

3.2.c. Bonding

The bonding process is the key to enable technology for *3D*-integration: it glues multiple functional *IC* chips vertically, thus providing mechanical, thermal, electrical and optical connections between the chips and the wafers permanently. The process consists of attaching two substrate materials, either directly or indirectly.

The first section will explain the different types of bonding that exists nowadays for the *3D*-integration, also explaining the necessary steps with some real applications.

Secondly, the process requirements will be described. The limitations in terms of process applies to the chosen material, and vice versa, therefore an excellent know-how of the material features is needed to clearly understand compatibility between them and with different process techniques.

Following the analogy with the *TSV* section, the last point consists of an overview of the process quality: the main reliability concerns will be described, showing with real examples which are the current problems in the industry, and how the fabs come up with different solutions to get a continuous improvement in the process.

3.2.c.I. Classification and direct bonding process description

Depending on the type of contact between the materials, one classifies the process in three different bonding types, differentiated at figure 70:

- **Direct bonding**: when the attachment is done between two similar or dissimilar materials without using anything in between them. Examples of used materials are the junction *Si-Si* hydrophobic (with identical or different properties, *e.g.* crystal orientation and impurity) [155], *Si–SiO$_2$* bonding [156], Plasma-Enhanced Chemical Vapor Deposition (*PECVD*) *SiO$_2$–SiO$_2$* bonding [120], *Cu–Cu* bonding (or metal bonding in general) [157, 158] and benzocyclobutene (*BCB*) to *BCB* bonding (or adhesive bonding in general) [159].

- **Indirect bonding**: it uses an intermediate material to link the two surfaces. Examples of indirect bonding includes *Si-Si* hydrophilic bonding (notice it is no longer hydrophobic) where a thin oxide layer is formed at the bonding interface [160], *BCB* and a variety of polymers or polyimides to bond two other materials (such as *Si* chips or wafers [159]), metal layer (such a thin *Ti* film) to bond two *Si* wafers [161] and intermetallic compounds (*IMC*s) to bond two chips or wafers [162, 163].

- **Hybrid bonding**: there is an added material in one of the bonding surface. It is mainly used to form electrical connections between two materials, with non-metal bonding to provide additional thermal/mechanical support [164]. The metal patterns are often formed within an insulator matrix on each side of the bonding surface, such as copper pads within an oxide matrix (*Cu*–oxide) [165] or a *BCB* matrix (*Cu–BCB*) [166], microbumps within an underfill [167]. Other polymers may be used as the insulator matrix material.

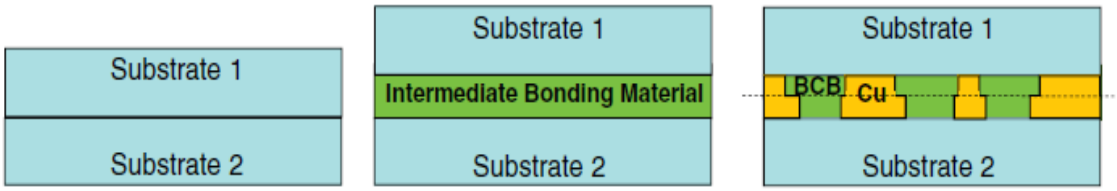


Figure 70: *Major 3D-bonding approaches: direct, indirect and hybrid bonding [102].*

The more extended use of direct bonding, explained by the cost saving without using any extra material, makes that approach the one selected to be discussed in this thesis. From all the available literature, two interesting applications were chosen in order for the reader to visually understand that bonding itself occupies only a part of the whole *3D*-integration.

The first one is represented in figure 71, consisting on direct bonding of Silicon-On-Insulator (*SOI*) layers using *Au* electrodes to connect with *SiO$_2$* [102].

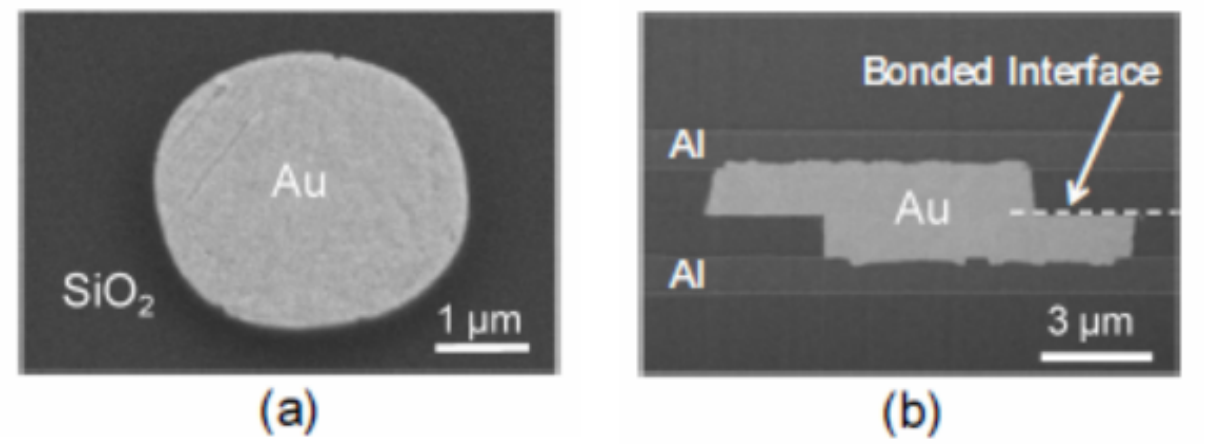


Figure 71: *Direct bonding between Au electrodes into SiO_2. (a): Top view. (b): Cross section [102].*

The process consists of various steps, as the figure 72 illustrates:

a) Some *FET*s are formed on a Fully Depleted Silicon-On-Insulator (*FDSOI*) wafer and an *Al* wiring layer is created.
b) After a SiO_2 intermediate layer is patterned, an *Au* thin layer is electroplated in the top surface.
c) Damascene process by Chemical-Mechanical Polishing (*CMP*) is applied to form embedded *Au* electrodes, removing the *Au* thin layer where not needed.
d) Chips are diced into a 20 *mm* square size, and the surface is activated by *Ar* and O_2 plasma.
e) The direct bonding is performed at 200 degrees Celsius.

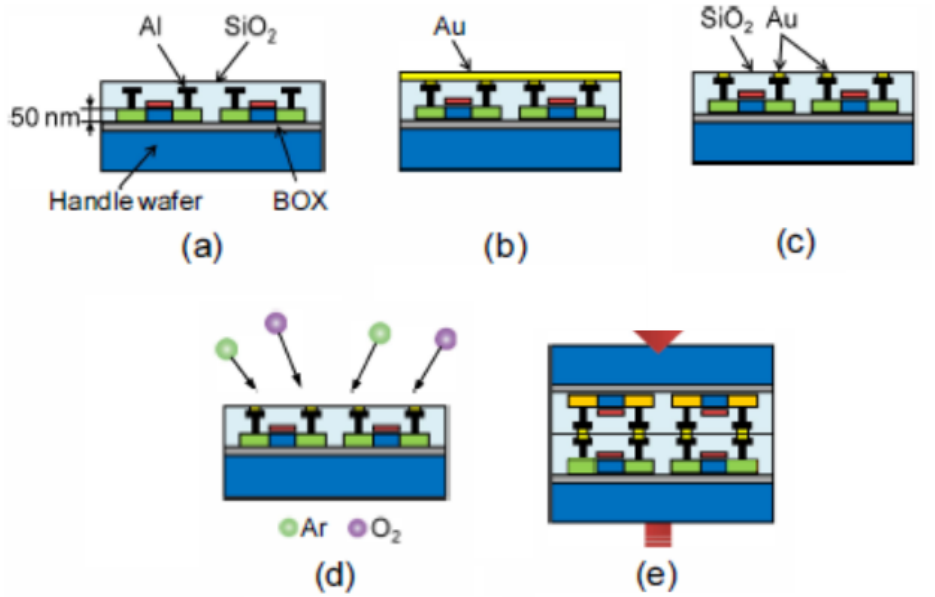


Figure 72: *Process flow of the 3D-Direct Bonding using Au electrodes to connect with SiO_2 [168].*

The result is to have the *Au* electrodes embedded into the SiO_2 surfaces after *CMP*, as can be shown in both the top view and the cross section of the bonding interface (figure 71).

The second example (figure 73) is the so-called Direct Bond Interface (*DBI*), which uses oxide bonding to solder planarized wafers with embedded metal contacts *[169]*. This technique uses standard fab processes at low temperatures (for both the initial bonding and the subsequent annealing) and can be utilised for *W2W* or *C2W* bonding.

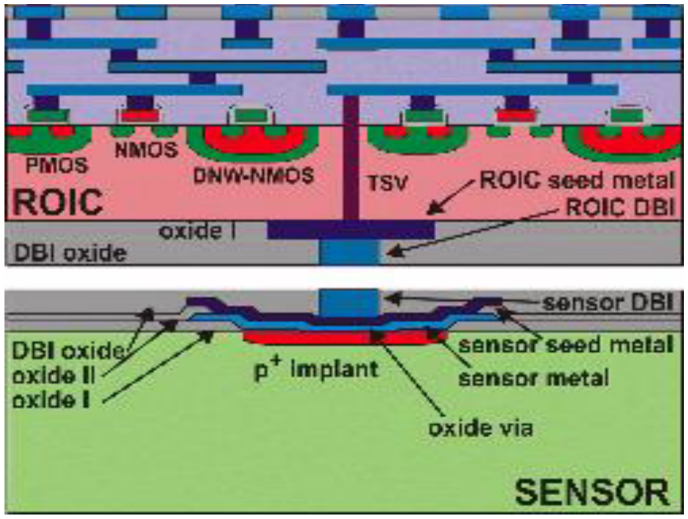


Figure 73: *Direct Bonding Interface (DBI) for a sensor [169].*

The whole circuit is not only made of this *DBI* process, but also uses typical direct bondinge and *TSV*s. The overall packaging manufacturing process is shown at figure 74, and could be described as follows:

1) *W2W* bonding.
2) Exposure of the *TSV*s and patterning in the top of the *Al* side.
3) Oxide bonding the previous subassembly with a so-called handle wafer.
4) Exposure of the *TSV*s at the sensor side and patterning the *DBI* structures.
5) Dicing of the chip.
6) *DBI* between the chip and the sensor wafer.
7) Grinding and etching for top connection exposure.

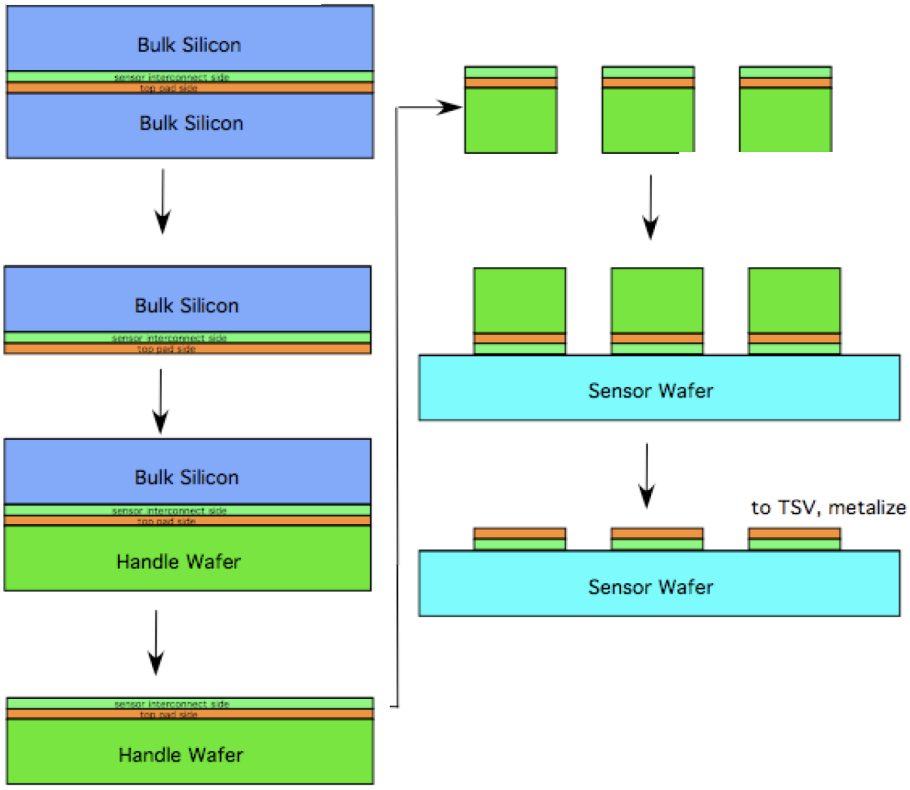


Figure 74: *Sensor manufacturing by using direct bonding, TSVs and DBI [169].*

3.2.c.II. Process requirements-materials

One does not have to forget that the bonding is only one of the processes of the *3D*-integration, therefore the frond-end-of-line (*FEOL*) and back-end-of-line (*BEOL*) processes have to be taken into account with regard to the bonding conditions to be used. For that reason, numeral requirements are included for the bonding, so that the overall process quality is not being degraded:

- Temperature lower than 400 degrees Celsius to be compatible with *BEOL*, thus using bonding materials which are relatively thin and of low stress.

- High thermal and mechanical stability of the bonding interface over the ranges of *BEOL* and packaging processing conditions. The heat distribution has to be carefully controlled in order to avoid defects at bonding or while thermo-compressing the wafer [97].

- No outgassing -or having outgassing channels- to avoid voids formation during the bonding process.

- Seamless bonding interface having high bond strength to prevent delamination.

- Angstrom-scale (10^{-10} *m*) flatness to achieve strong chemical bonds. This feature is especially important for rigid bonding surfaces such as *Si-Si* or SiO_2-SiO_2 bonding [156, 160], being not that relevant for soft bonding surfaces such as *Cu-Cu* or *BCB-BCB* [159, 170]. Nevertheless, for rigid bonding surfaces there are some solutions at the market: using surface deformation (by affixing the wafer to a wafer holder) [97], interface diffusion or an intermediate material. The figure 75 compares the impact at rigid bonding without and with an intermediate material.

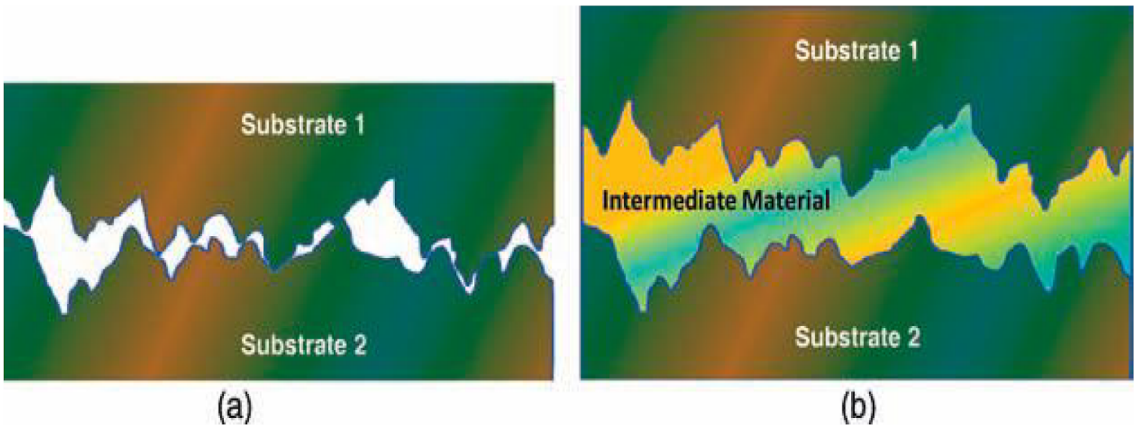


Figure 75: *Impact of bonding surfaces-roughness [96]. (a): Rigid bonding surfaces preventing bonding. (b): Rigid bonding surfaces using an intermediate material to allow bonding.*

- Diffusion of massive atoms across the bonding interface during bonding or post-bond annealing.

- A surface extremely clean, *i.e.* totally free of particles and defects. This is extremely important for rigid bonding surfaces, whereas soft bonding surfaces (*e.g. Cu-Cu* or *BCB-BCB* bonding) can tolerate some level of contamination *[156]*.

For all the previous requirements, some materials combination performs better than others. However, on top of the previous conditions, depending on the applications some extra requirements can be added. For instance, some circuits would imply more focus on the thermal or electrical connections, whereas others would require more mechanical or optical connections between the functional chips or wafers or even a temporary mechanical support for wafer thinning. Nevertheless, the preferred combination of materials nowadays can be summarized as follows:

- *Cu-Cu* and *BCB-BCB* bonding, as well as *PECVD* oxide bonding are said *[171]* to satisfy all the requirements.

- The *Cu-Cu* bonding at temperatures higher than 350 degrees Celsius leads to high bonding strength, since the copper diffusion across the bonding interface with *Cu* grain regrowth *[96]*. In addition to that, using further thermal processes may enhance the bonding strength with more copper interdiffusion at the bonding interface *[171]*.

- *BCB-BCB* reflows at 180 degrees Celsius and forms cross-link networks rapidly at 250 *ºC* without outgassing, leading to very strong bonds, which can be further enhanced by thermal processes up to 400 *ºC* *[172]*.

- *PECVD* oxide, despite the fact that requires better surface flatness and cleanliness compared to the previous methods, but with *Si-OH* bonds at thermal annealing at 275 *ºC* creates strong *Si-O-Si* bonds, but releasing a small amount of H_2O which can easily diffuse in oxide *[173]*.

- *Cu-Sn* can work well for *CoC* and *CoW* bonding if conducted in air atmosphere *[174]*, thus being called as Solid-Liquid Interdiffusion (*SLID*) or Intermetallic Compound (*IMC*) bonding. The substrates to be bonded are deposited in layers at a temperature range between 240 and 270 degrees Celsius, being the deposited tin completely transformed into the Cu_3Sn intermetallic compound. It is important to use the appropriate film thicknesses, so that the tin is consumed and the solidification takes place within few minutes. The *SLID* technology has the advantage of forming simultaneously the mechanical and the electrical interconnects (*i.e.* no post-processing is required) but the materials might melt during the bonding process *[96]*. An example of *SLID* bonding and *TSV*s is provided at figure 76.

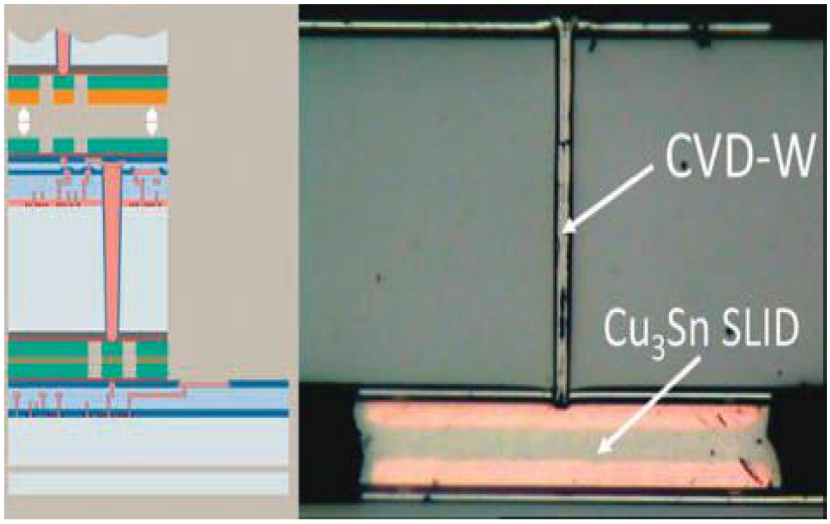


Figure 76: *Combination of SLID bonding process and TSVs [175].*

- Another good combination is the *Au-In* using eutectic bonding at low temperatures. However, it is very difficult to control the lateral size of the bonding pad and the vertical height of the bonding bump, therefore requiring large bond pads. One important reliability concern is that after bonding the solder joints are usually brittle *[174]*.

3.2.c.III. Bonding quality characterization

After having understood the requirements needed for the process, it is time to review how one can quantify how good the bonding is. To do so, multiple methods have been developed to characterize the bonding quality, not only covering the mechanical properties, but also structural, thermal and electrical features of the bonding interface. In order to ensure the right functionality, it is said *[176]* that the bonding quality has to fulfil the void/defect, bonding strength, electrical resistance and reliability requirements.

- **Voids and defects** are to be avoided at the bonding interface, since they directly affect the bonding quality and reliability. However, it is inevitable that some voids and/or defects arise at the bonding interface during the bonding process development, therefore the realistic goal is to reduce the size and density of those voids/defects as much as possible. The goal is not that easy, since their appearance depends on numerous factors, such as the surface roughness, outgassing at the bonding interface, contamination or metal grain regrowth.

  To check their presence, different effective methods have been developed, being differentiated in the ones that does not destroy the junction (non-destructive methods) versus the one that actually do it (destructive tests). The non-destructive methods have obviously the advantage of not breaking the chip, but they have a limited resolution. Examples of them are the infrared imaging or the Scanning Acoustic Microscopy (*SAM*). The destructive methods, on the other hand, have a higher resolution, appearing varieties as the Focused Ion Beam (*FIB*), the Transmission Electron Microscopy (*TEM*) or the Scanning Electron Microscopy (*SEM*). An example of a *TEM* cross section can be found at the figure 77.

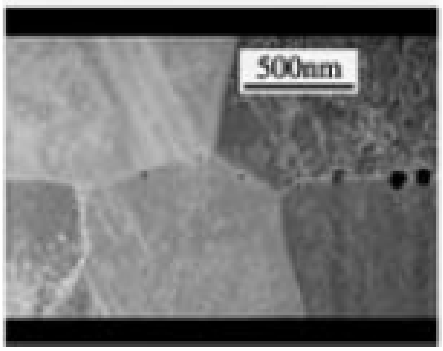


Figure 77: *TEM cross section of Cu-Cu bonding at 40 degrees Celsius [177].*

❖ **Bonding strength** is not only an indicator of the structural and mechanical bonding quality, but also provides hints with regards to the thermal, mechanical and electrical properties as well as for the overall bonding reliability. A high bond strength (typically 1 J/m^2 or higher) is required for permanent bonding to avoid delamination of the bonding interface [96], and also the figure has to be high enough for temporary bonds to hold wafers for wafer thinning and polishing but low enough for debonding [178].

Three major characterization methods are nowadays used in the industry. The first one, the so-called razor blade test, is a simple but effective method to quickly check the bond strength by inserting a sharp razor blade at the edge of a bonding interface: if the bonded wafer pair cannot be separated easily or is shattered to pieces, the bonding passes the test [96]. The second technique is the crack opening method (also called cantilever beam test), which is a quantitative-evolution of the previous one, consisting on inserting a razor blade of a specific thickness between the bonded wafer pair, obtaining the surface energy by recording the time-dependency of the crack length of the bond connection split-up [179, 180]. The latest methodology is the four-point bending technique, which is based on the theory of fracture mechanics in which delamination is modeled as a crack propagating along the interface between two bonded materials [172, 181]. With this test, a load cell quantifies the applied load and an actuator measures the displacement of the Device Under Test (*DUT*), which is placed and hold in a customized fixture. The bonding strength, measured by the critical adhesion energy, can be determined from the load versus displacement curve [181]. A measurement of the critical adhesion energy for different *BCB* thicknesses at figure 78.

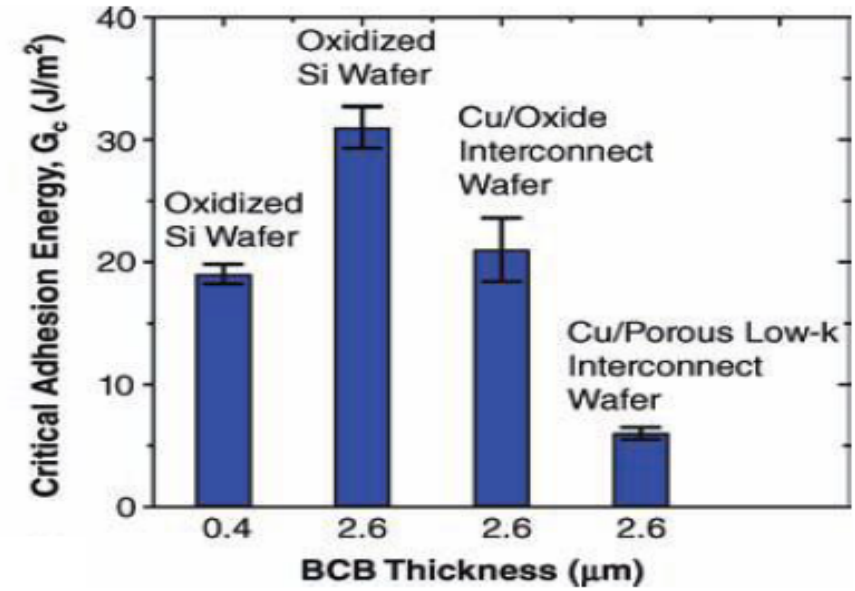


Figure 78: *Critical adhesion energy measured by a four-points bending technique for wafers with oxide, Cu-oxide and Cu-low-k interconnects, bonded to an oxidized Si wafer using BCB [182].*

❖ **Electrical resistance** indicates also how well the junction is done. Typical devices such as ohmmeters cannot be used to measure the resistance of those micro-junctions, therefore customized gauges have to be developed for each particular circuit. For instance, a daisy-chain device can be used [182], so that multiples junctions (such as *Au* electrodes making the connection with SiO_2) can be wired in series (by means of small *Al* wires with known resistance) and their overall chain resistance be measured (figure 79).

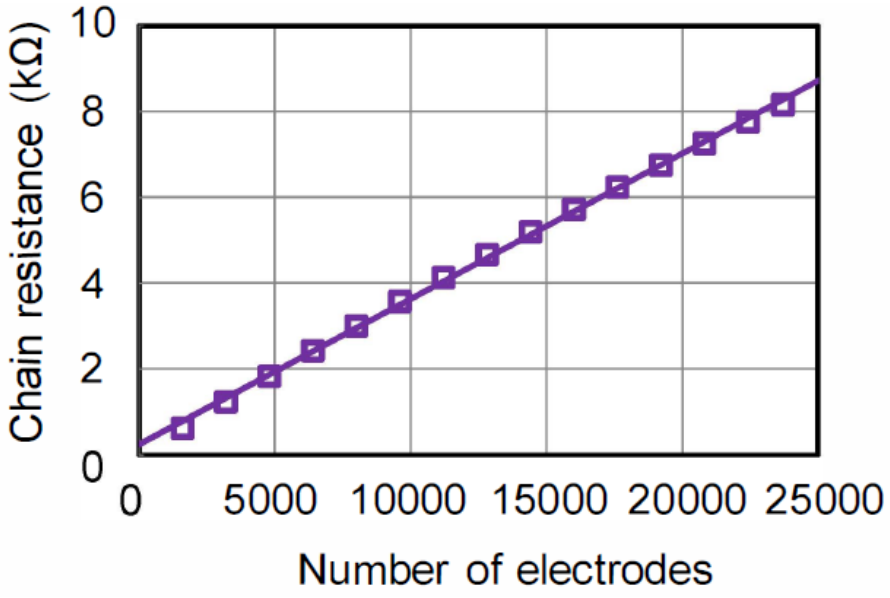


Figure 79: *Measured chain resistance by using daisy-chain device in an Au (electrodes)-SiO_2 junction [102].*

❖ **Reliability requirements** is increasingly important for *3D-IC*s with volume production in progress. Those requisites have to do with the behaviour of the chip in the long run, in other words, ensure that if a chip functions from the very first moment, it will continue working throughout its whole expected lifetime. The reliability tests have recently focused on bonding using *IMC*s [183], because *IMC* bonding is said [184] to be the choice for mass production of the wide *I/O DRAM*. Relatively fewer reliability tests are reported for other bonding systems such as *Si-Si*, *Cu-Cu* or *BCB-BCB*, partially because they are quite reliable once they are well bonded [182] and the semiconductor industry has not yet been focusing on those systems for volume production of *3D-IC*s [96].

The tests include a variety of destructive methodologies with the goal of exposing the circuit to extreme environments which could encounter throughout its life weakening its performance. For instance, thermal shocks and cycling tests are common in the industry, thus keeping the circuit in extremely high and low temperatures cyclically to see how well is preserved after the cycles. The figure 80 depicts the evolution of voids after applying thermal shocks.

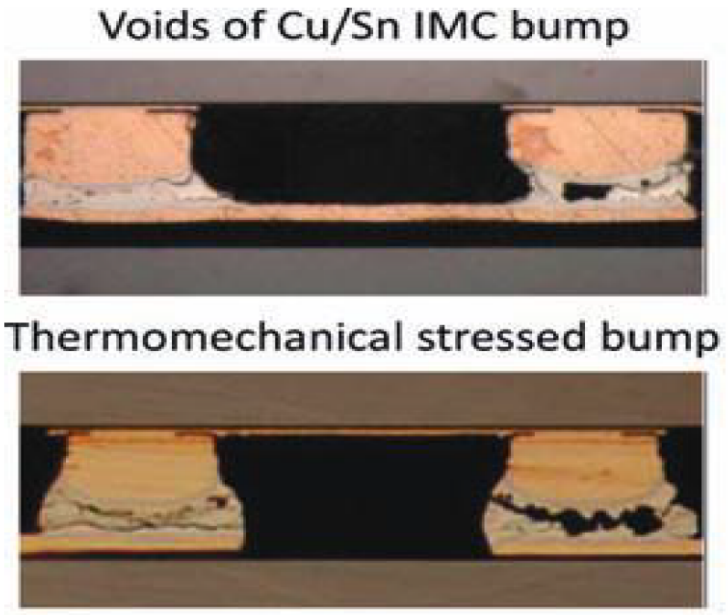


Figure 80: *Cu-Sn IMC bonding cross section. Before (top) and after thermomechanical stressed (bottom), where voids can be seen to enlarge [185].*

More methodologies include traditional reliability tests such as mechanical shock tests, electromigration (*EM*) tests and other electrical tests *[186]*. Particularly interesting is the shear test, consisting on pushing in horizontal direction the junction with a special tool, so that a measurement of the force which the junction breaks is automatically recorded, also extracting information about the bonding quality by checking how much residue of the bonding is still left after the break. Shear test can also be performed in combination with the standard thermomechanical/aging tests to check how the shear force is degraded after the adverse environment conditions, providing an indication of how clean (plasma treatments may help) is the bonding surface and how well the bonding will continue sticking in the future. An example of shear strength for different plasma treatments is shown at figure 81 for convenience.

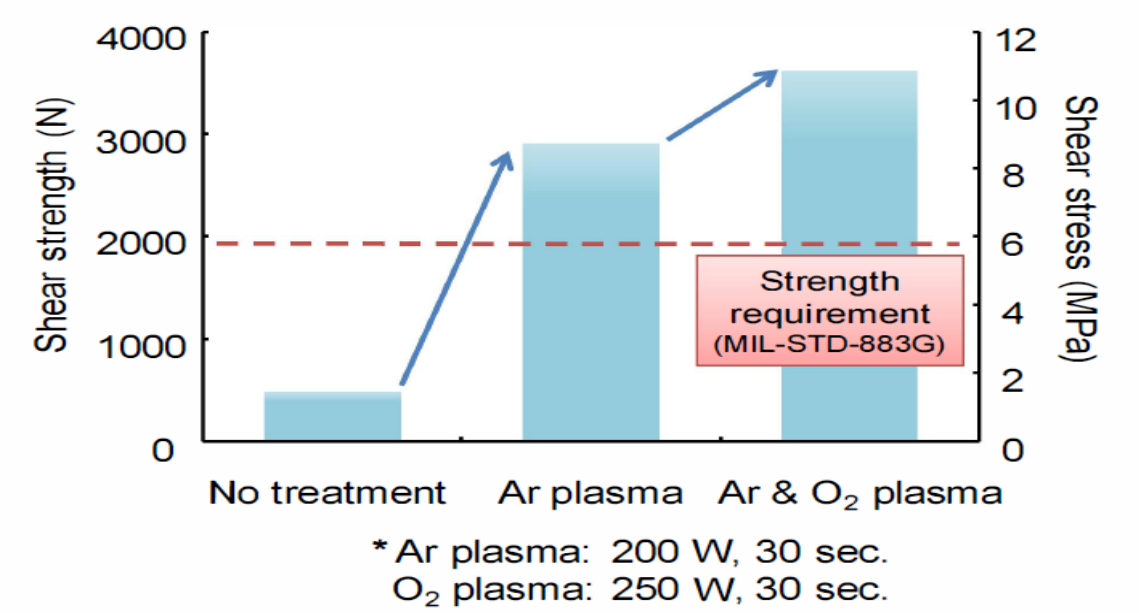


Figure 81: *Shear strengths for direct bonding Au/SiO_2 without and with plasma treatments [102].*

3.2.d. *3D*-patterning by modulated lithography

The *3D*-integration previously discussed consists on basic photolithography and using *TSV* and bonding to make the connection between the different layers. However, to print the pattern in each layer, conventional lithography is used, with a limited accuracy (no *EUV* required nor other complex enhancements) since the precision of the vias or connections would be indeed lower than the one that could be achieved with the most-advanced photolithography techniques.

Patterning each layer and then integrating the circuit in three dimensions implies a lot of extra processing, since not only the lithography is performed but also the connection between the different layers has to be done. Wouldn't it be fantastic to print directly the *3D*-features by means of a lens using a kind of *3D*-reticle? That idea, indeed, would greatly reduce the cycle time for manufacturing the *3D*-circuits, requiring reticle re-design and modifications on the photolithography tool though. There are currently different directions for that potential implementation, which will be addressed in this section.

3.2.d.I. Tilted patterns by inclined/rotated lithography

This first approach is an intermediate step between the conventional lithography and the *3D*-lithography that one can imagine. In conventional lithography, the mask and the resist form an angle of 90 degrees versus the illumination source (the excimer laser). The light on this way is shadowed by the reticle, who is in charge of making the binary-contrast lithography patterns. However, if the reticle and the resist at the wafer are both being tilted (see figure 82 for reference) with respect to the beam by tilting the stage, inclined structures can be produced *[187]*.

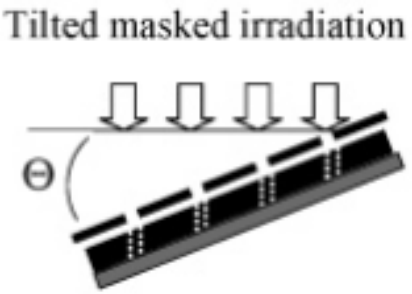


Figure 82: *Tilted patterning by inclined lithography [188].*

By these means, oblique cylinders, embedded channels, bridges, *V*-grooves, and truncated cones with aspect ratios greater than 4 times have been fabricated using 100 *μm* thick *SU-8* layers and a conventional *UV* mask aligner *[187]*, as the figure 83 illustrates.

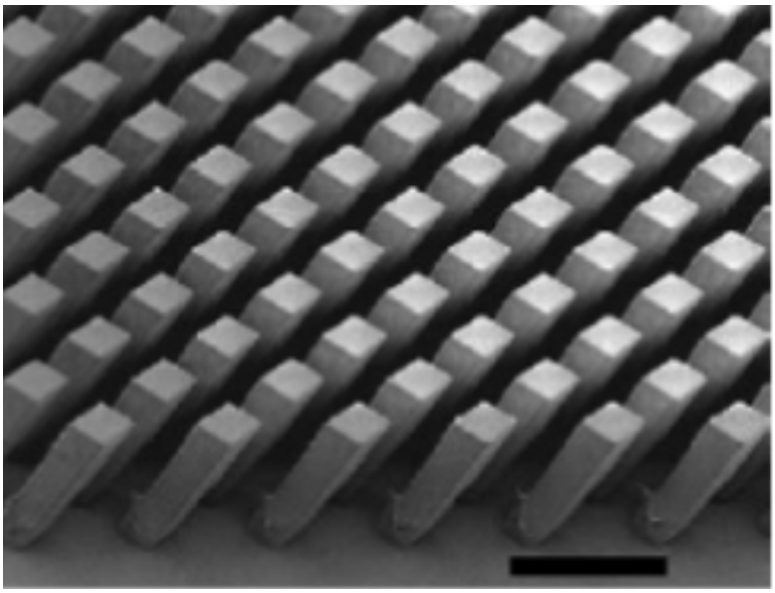


Figure 83: *Tilted pillars by inclined lithography [187]. Scale bar corresponds to 100 μm.*

Even more complicated *3D*-structures can be generated using multiple inclined *UV* exposures along different axes [189, 190]. Another more advanced option would be to combine tilted exposure with conventional photolithography to create asymmetric pillars with vertical and inclined sidewalls [191], being represented at figure 84.

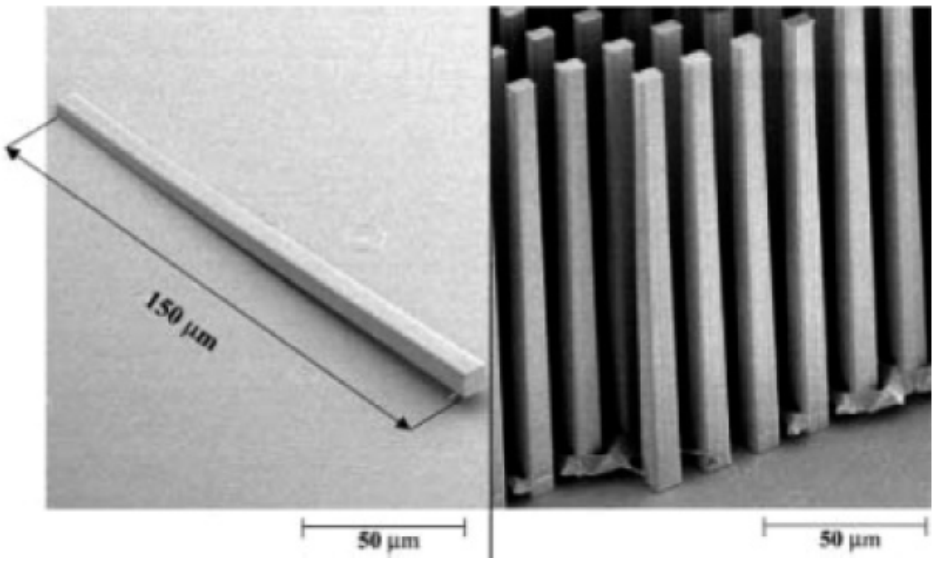


Figure 84: *Asymmetric pillars with aspect ratio=10 by combining X-ray vertical and tilted exposure [191].*

So far only the tilting has been described. However, there is another enhanced option showed figure 85, which is to tilt and simultaneously rotate the photomask and the wafer.

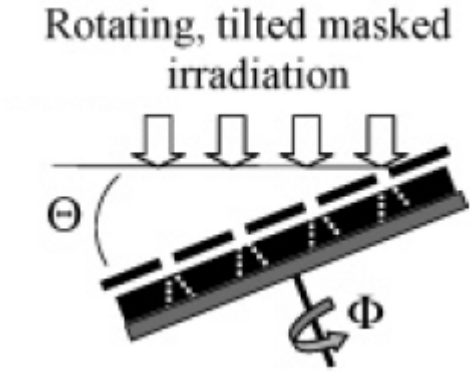


Figure 85: *Tilted and rotated patterning by inclined lithography [188].*

On that way, also tapered structured with non-vertical sidewalls can be generated [192], such as the ones in figure 86. Those structures are very useful when a master for subsequent replications are needed, since they provide a draft angle and facilitate a posterior process called demoulding. A combination of multiple *X*-ray exposures, tilting, and rotation with *PMMA* reticles can be achieved to pattern tilted and crossed features [193, 194, 195].

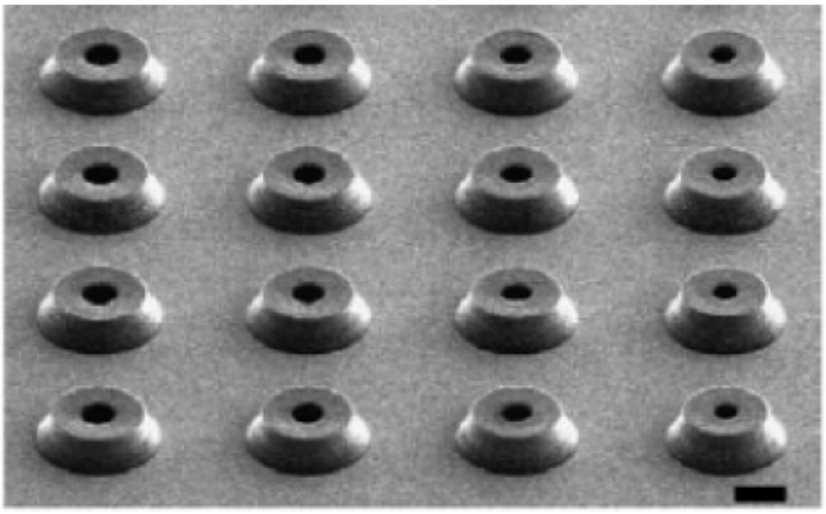


Figure 86: *Tapered structures by tilted and rotated UV exposure [187]. Scale bar corresponds to 50 µm.*

The process parameters for exposure have to be changed, because otherwise the incident light would be reflected by the photoresist on the wafer, since the energy of the reflected *UV* light is too low to initiate cross-linking of the resist. Therefore, the dose used to expose (or the exposure time) has to be increased, or reflective substrates have to be used, so that cross-linking is initiated *[188]*. The figure 87 compares the structures obtained after single tilted exposure with a normal silicon wafer (left hand side) and with reflective aluminium-coated silicon wafer (right hand side), where the irradiation conditions remain the same but not the printed pattern.

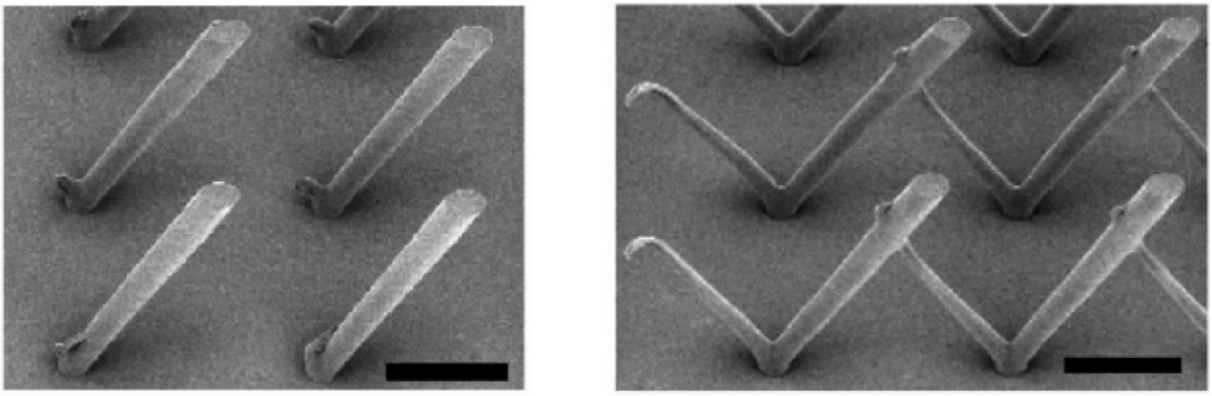


Figure 87: *Structures fabricated by tilted UV on nonreflective (silicon, left hand side), and reflective (aluminum-coated silicon, right hand side) substrates [187]. Scale bar corresponds to 100 µm.*

3.2.d.II. Patterns by modulated exposure

Instead of tilting and rotating the reticle and the wafer, numeral *3D*-approaches are under investigation to generate multilevel structures from single resist layers. On that way, it would avoid cycle time since no (or few) multiple exposures would be required.
To do so, special masks and projection optics are needed, needing the photolithography tool to be able to modulate the exposure dose on the resist. On that way, multiple depths of exposure photoresist would be achieved and, consequently, different heights of the photoresist structure would remain after wafer development. One can make an analogy to having incident lights with different energies, therefore some of the light would only trespass the first reticle film layer, whereas some other light would continue its path, therefore multiple layers patterning may be achieved with one single exposure. Different options exist:

- **The "gray scale" lithography**: it uses special reticles which modulate the light intensity in accordance to their gray levels. Two different types of masks exist: the first one, the halftone chrome masks, are binary chrome masks with gray levels simulated by different densities of opaque pixels on a transparent background. The second option is the High-Energy Beam-Sensitive (*HEBS*) glass masks, which are fabricated by exposing this glass to controlled doses of a high-energy electron beam, causing the reduction of silver ions in the glass *[188]*. The areas of the mask with high concentrations of reduced silver ions correspond to high levels of gray shading. This method has been used to produce 10 *μm* thick grid structures on the top of 15-100 *μm* pillars *[196]*, which can be seen at the figure 88.

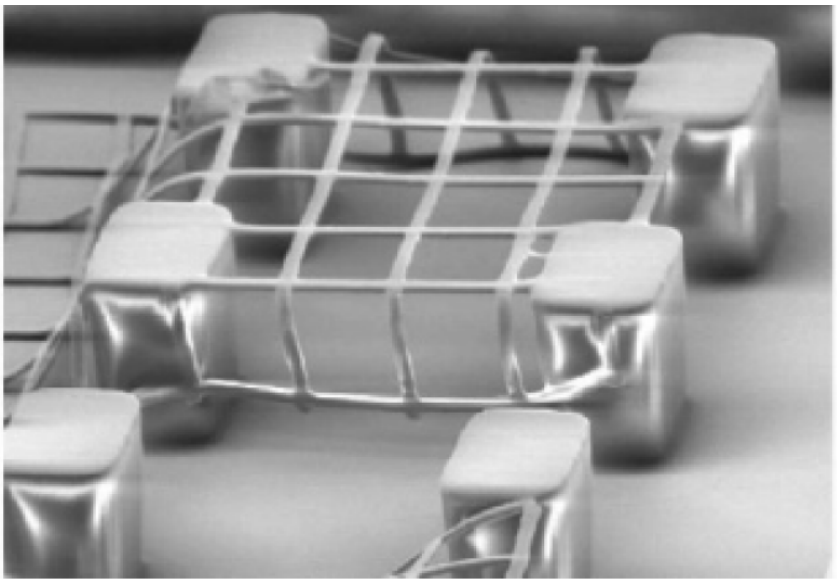


Figure 88: *Suspended 10 μm thick grid structures made by gray scale lithography [196].*

- **Proximity lithography**: it consists on inducing diffraction patterns from a conventional chrome-on-glass mask by leaving a controlled air gap between the resist film and the mask *[197]*. This type of lithography was also used at the beginning of optical lithography (see figure 5 for reference), but in this case the use is enhanced for the *3D*-patterns. The diffraction process creates a modulated intensity pattern across the surface of the waver, something similar to the *PSM*. The intensity pattern would depend upon the mask features (size, geometry and spacing) and the gap between the mask and the resist layer.

- Other ways of generating ranges of exposure levels include **microlens arrays** *[198]* or **conformable phase-shift edge masks** *[199, 200]*. This last option, the phase-shift edge masks, uses the *PSM* technique with the help of a topographical relief at the mask. The geometry of the intensity pattern would depend not only upon the design (depth and layout of the relief structures and refraction index) of the mask, but also on the exposure light features (wavelength, coherence and polarization).

3.2.d.III. Periodic *3D*-patterns by holographic lithography

The **holographic lithography**, also known as **interference lithography** (*IL*), is based on the interferences produced by multiple coherent laser beams, which form a periodic and sinusoidal intensity pattern in space *[201]*, as the figure 89 illustrates The main difference of this type of lithography is that not only one excimer lasers is used, but the beams of many of them are used to produce the interference between the light rays.

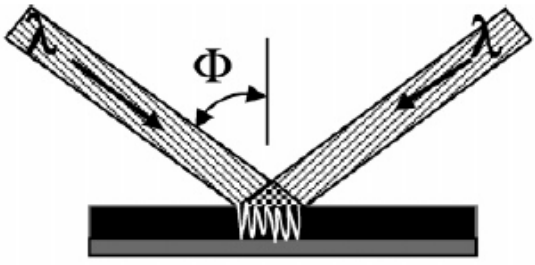


Figure 89: *Interference lithography with two laser beams [201].*

The lasers expose a photosensitive material, thus creating periodic structures of various symmetries after development of the wafer. The pattern is periodic, whose period (to bear in mind that it is a spatial periodicity and not in terms of time) is determined by the light wavelength (*λ)* and the angle of intersection of the beams (*Φ*):

$$P = \frac{\lambda}{2} * sin(\Phi) \qquad (3.2.d.III.1)$$

According to the previous equation, the spatial resolution that can be achieved with the interference lithography far exceeds that of conventional projection lithography using the same irradiation wavelength (typically *λ*/4) *[188]*. The depth of focus is not only determined by the angle of intersection, but also by the beam diameter and the intensity profile, being typically so large that it is considered to be infinite.

By adjusting the number, amplitude, phase, wave vector and polarization of the interfering beams, different symmetry patterns can be generated. Take for instance the surface gratings produced by three beams while overlaying two sequential exposures with an angle of 90 degrees *[202, 203]*. Another examples *[204, 205, 206]* are the *3D*-periodic structures fabricated by using additional beams in a single exposure -or overlaying multiple exposures- as the ones at figure 90. Different shapes like a spiral microstructure are possible, by using six equally spaced circumpolar linear polarized side beams and a circular polarized central beam, whose pitch and separation of the spirals was varied by changing the angle between the side beam and the central beam *[207]*.

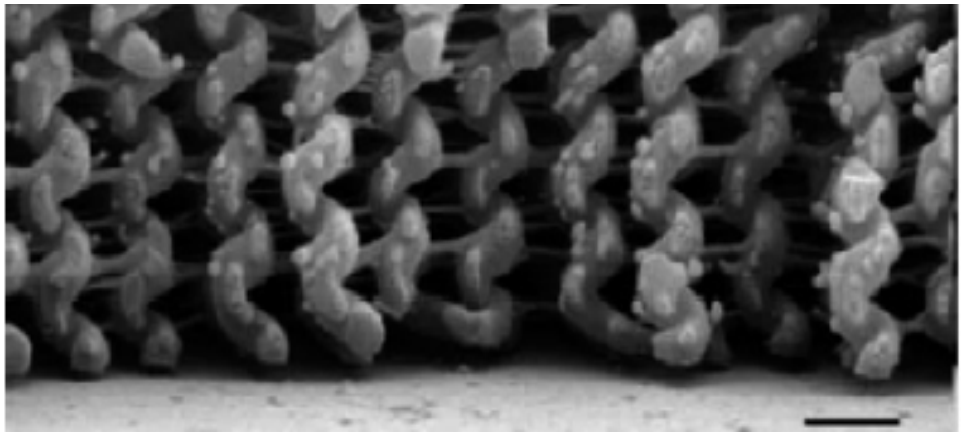


Figure 90: *Chiral 3D-structures (spirals) produced by holographic lithography [207]. Scale bar corresponds to 1 µm.*

Interference Lithography offers numerous advantages over the previously discussed *3D*-lithographic strategies: it is both maskless and lense-less, thus minimizing cost and eliminating the optical aberrations associated with complex lens systems. As drawback, holographic lithography is limited to the fabrication of periodic structures and combinations thereof *[208]*.

3.2.d.IV. Built-in lens mask lithography

This novel technique integrates the reticle directly at the lens, therefore no more lens is needed. The figure 91 sketches the concept: the pattern is already built-into the lens mark, having a complex optical transmittance *g**, where the incident coherent light is focused on the focal plane for arbitrary shaped pattern *[209]*.

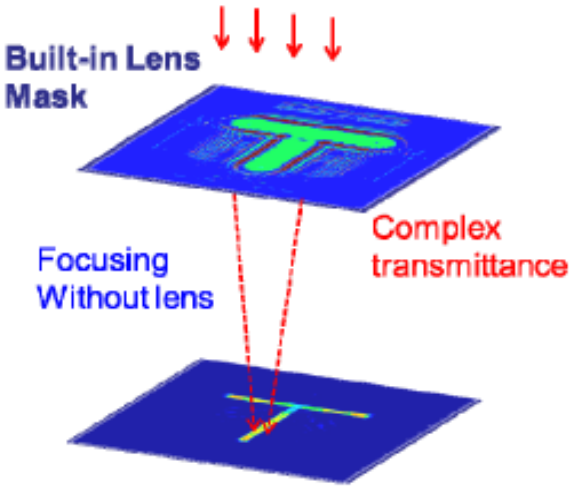


Figure 91: *Basic concept of the built-in lens mask having complex optical transmittance g* [209].*

At the previous figure 91 it is shown a single layer but, in reality, the built-in lens mask consists of multiple layers which will be able to provide the *3D*-integration at wafer level, with a multi-level structure superpositioning pre-designed patterns in different focal planes. To eliminate the interference between layers, phases are shifted in each layer, and the complex amplitudes are superposed to design the built-in lens mask for seed patterns in voluntary focal depths *[209]*, thus resulting the overall complex transmittance the sum of the complex transmittance per layer. A breakdown of the focal planes is depicted at figure 92.

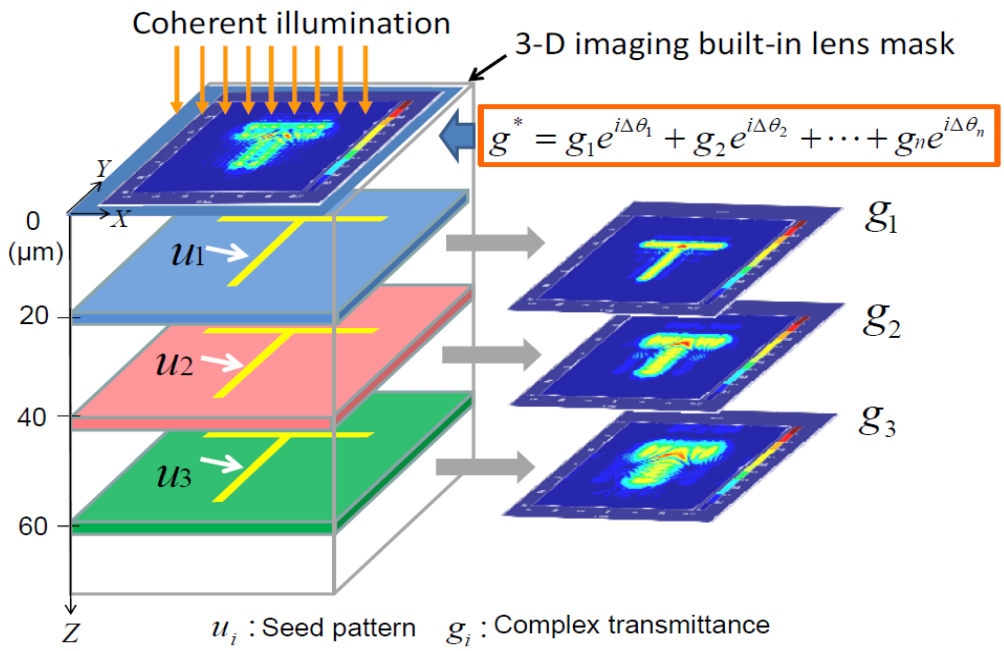


Figure 92: *3-dimensional imaging by superposing complex amplitudes of the seed patterns in various focal planes [209].*

The deep focal length imaging was confirmed for this technique *[210]*. It has been reported *[209]* its effectiveness by both computational lithography and experimental works using 5 seed layers, an illumination light of 365 *nm* wavelength (*i*-line of Mercury), a 1.0 *μm* seed pattern and 60 *μm* as focal depth. With the help of the phase shifted superposition, the 3-dimensional projection images were successfully obtained including parallel tubes in spaces, *T*-shaped connection of tubes and tilted tubes, which may result in essential components for *3D*-Integrated Circuits. The figure 93 depicts the result for the pattern "*S*" by that technique.

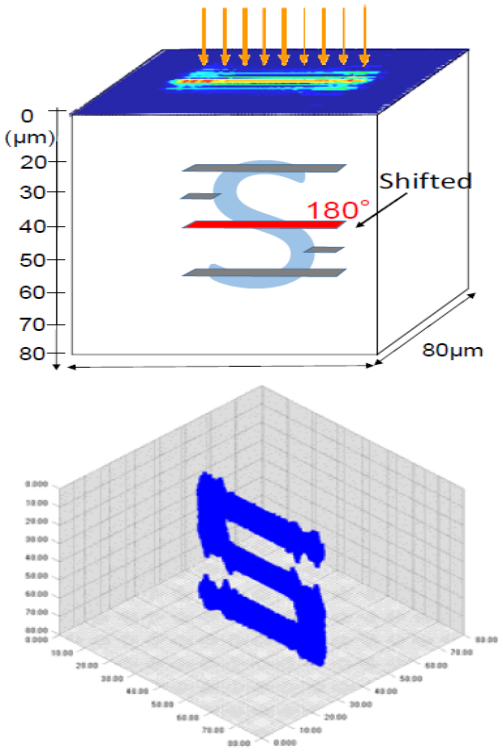


Figure 93: *3-dimensional imaging of a pattern "S" by computational lithography [209].*

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4. Challenges

Having understood the whole history of photolithography and what the cutting-edge is, it is time to present what are the main challenges for continuing shrinking the pattern size.

The main challenges for further *EUV* improvements and implementation in *HVM* are summarized in figure 94. They involve both the tools manufacturers -together with their optic suppliers- and the foundries, which are in parallel collaborating to continue developing the new technology.

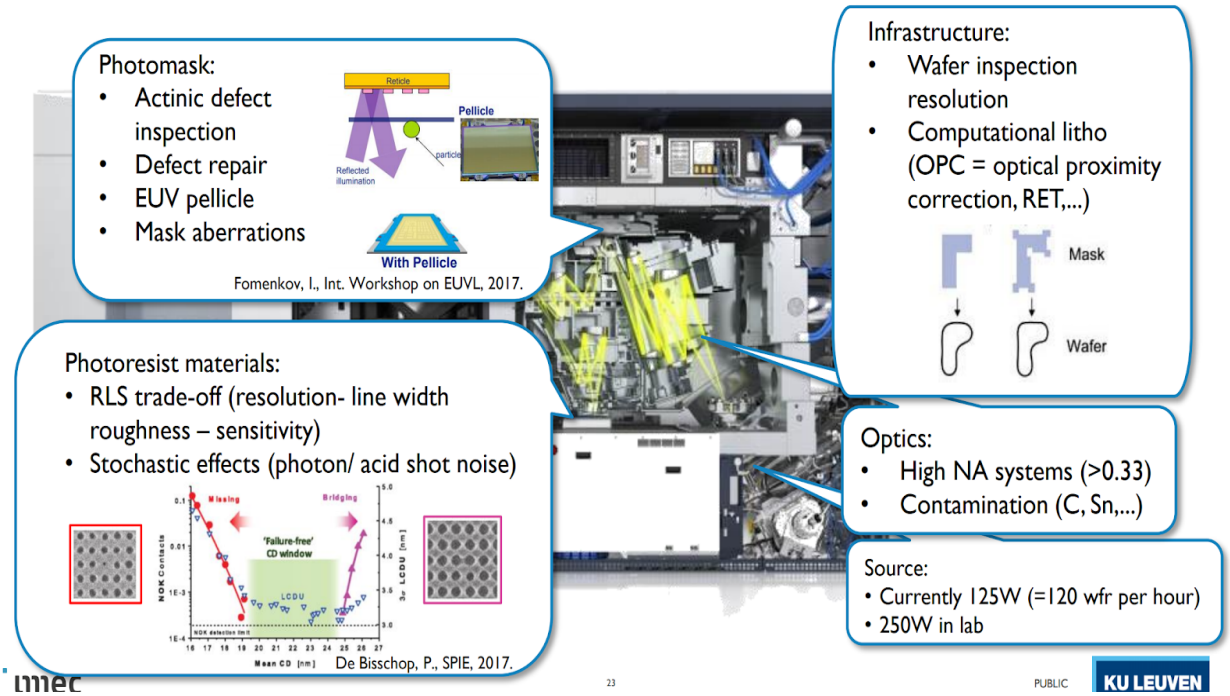

Figure 94: *Challenges for EUV lithography [211].*

From the foundries point of view (left hand side of the figure 94), their concerns are the **materials used for the reticles and photoresists**, therefore they are impulsing their suppliers to adapt quickly to *EUV* lithography challenges. An example of concerns from a circuit manufacturer is found at figure 95.

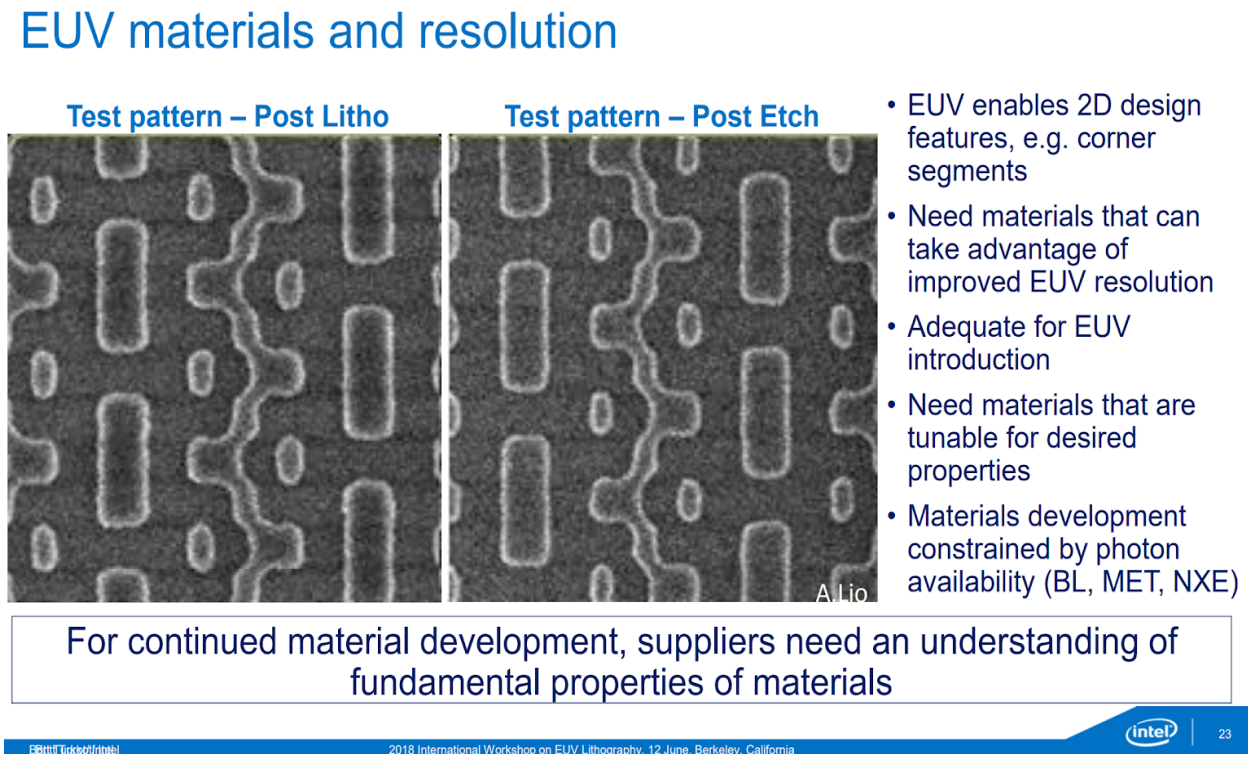

***Figure 95**: Example of EUV materials and resolution concerns for a circuit manufacturer [212].*

Particularly, challenges with regards to the reticle are in trend. The use of pellicles to avoid contamination is to be avoided, because of the undesirable absorption that would be encountered *[40]*, therefore another technique has to be researched able to prevent further contamination. Furthermore the defects induced at the Multilayer coating makes the reticle useless since it can not be repaired, therefore a much cleaner deposition system that uses ion beam sputtering is to be used. With regards to the photoresists, the investigations go in the direction of improving the contrast and sensitivity, as well as having an excellent etch resistance.

In parallel, the photolithography tool manufacturers (right hand side of figure 94) are more focused on **increasing the Numerical Aperture and the power**, thus collaborating with their lens and laser suppliers, respectively. The figure 96 shows the roadmap of a lithography tool supplier, where the before mentioned concerns are clearly identified.

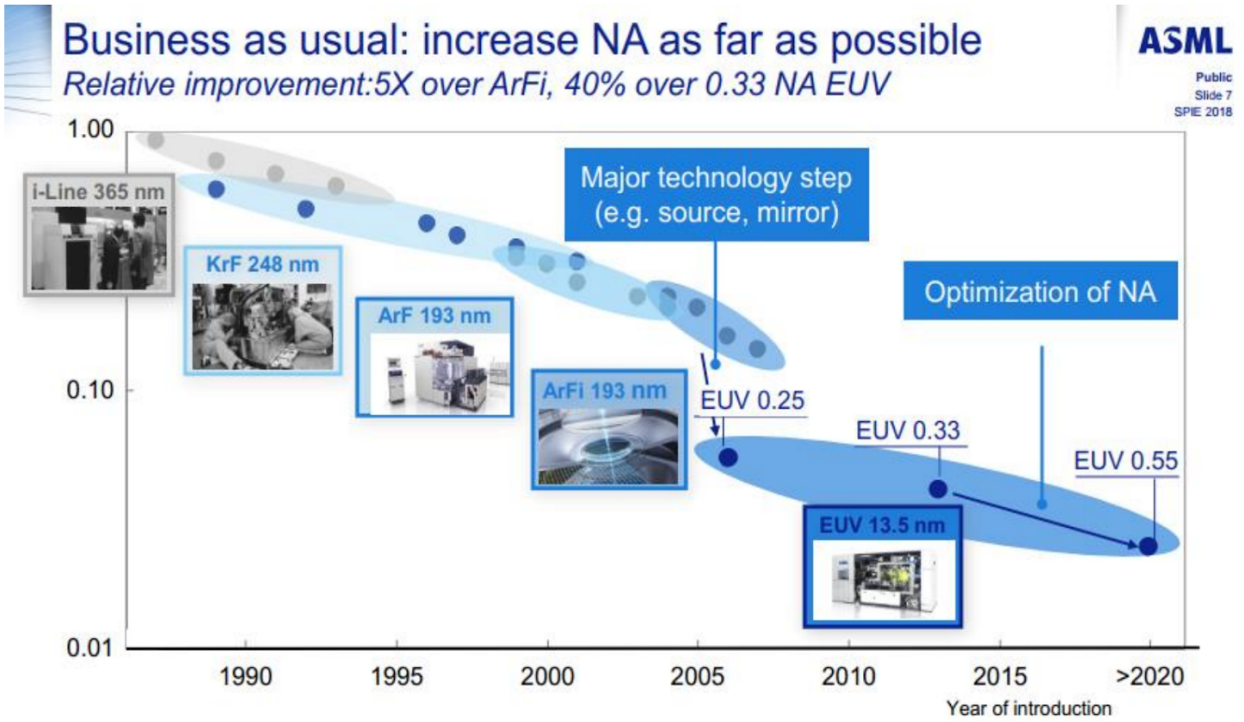

Figure 96: *Lithography tool supplier roadmap [213].*

The main concern for *ASML* is the optimization of *NA*, since with *EUV* lithography requires all kinds of computational lithography to reduce the aberrations *[214]*, which are more pronounced than with conventional lithography. Concerning the laser suppliers, it seems that they are making good progress to achieve the target of generating 200 *W*, but still they face some challenges such as stability, debris mitigation, power scaling and conversion efficiency *[215]*.

Moving onto the *3D*-integration as a potential alternative to the conventional lithography, still numeral challenges are open in order to get the implementation on a real and mature *HVM* basis:

- **Technological/manufacturing limitations:** the stacking process should not degrade the performance of the individual planes, therefore it is of fundamental importance to provide high-quality and high dense vertical interconnects, otherwise the performance or power gains achieved by the third dimension will diminish *[216]*. Etching defects, out-diffusion or voids are typical manufacturing issues which can ruin the complete *3D*-circuit functionality. The reader can find at figure 97 an example of numeral defects as well as an illustration of a good *TSV* formation.

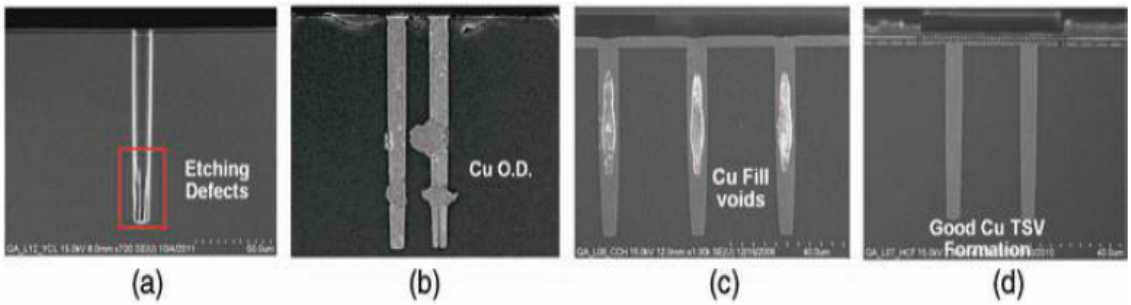

Figure 97: *TSV formation manufacturing defects [217]. (a) Etching defects. (b) Cu out-diffusion. (c) Cu fill voids. (d) Good TSV formation.*

- **Testing:** since conventional *2D*-manufacturing techniques do not include stacking different layers, the *3D*-integration requires novel testing methodologies at wafer and die level. The testing techniques only check part of the functionality of the system at a given time (typically, only one plane is tested at a time), thus requiring additional items, such as scan registers embedded within each plane *[217]*. Moreover, additional interconnect resources are necessary, such as power/ground pads to supply power to the plane during testing.

- **Interconnect design:** due to the inherent heterogeneity of these systems, models that consider particularly the *3D*-approach are needed. Particularly special focus is needed in clock and power distribution, as well as in mitigating the noise caused by capacitive and inductive coupling between adjacent planes *[218]*.

- **Thermal issues:** although the power consumption of these circuits is expected to decrease due to the considerably shorter interconnects, the power density greatly increases since there is a larger number of devices per unit area compared to a planar *2D*-circuit *[217]*. As the power density increases, the temperature of the planes not adjacent to the heatsink of the package will rise too, thus degrading the chip performance or accelerating wear-out mechanisms. Good design practices, packaging solutions and more effective heatsinks are therefore needed to alleviate thermal effects issues at *3D*-integration.

- **Computer-Aided Design *(CAD)* algorithms and tools:** whereas classic approaches for *2D*-circuits (such as partitioning, floorplanning, placement or routing) are in a mature phase, the extra complexity of the stacking requires new tools to help with the time-to-market and yield optimization. Design entry tools, algorithms, computational power and simulation tools have to be mastered in order to efficiently evaluate the performance of the entire *3D*-integrated system.

The consequence of those challenges is that cost-, reliability- and yieldwise, the *3D*-approach is not yet feasible to be run for mass production:

- **Yield:** it needs to be almost near perfection for each of the very many process steps, in order to cumulatively obtain reasonable high yield for the final *3D*-assembly [217]. An important investment in test simulation and optimization (illustrations at figure 98) is necessary, and also further understanding of the manufacturing errors is required, particularly optimizing the process flow, such as the discoveries done on *CoWoS* process which now results in a better yield (less warpages than with *CoCoS*) if chip stacking on a wafer (*CoW*) is done with a silicon-to-silicon joint first [219].

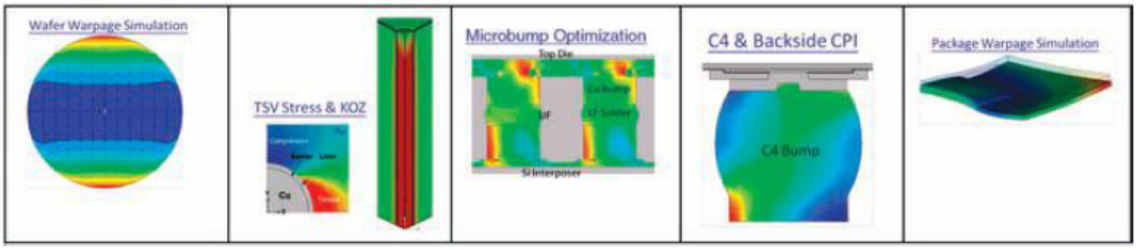

Figure 98: *3D-integration simulation and optimization prior to the manufacturing [219].*

- **Reliability:** the main two differences for the *3D*-integration are that they include new building blocks (*e.g. TSV*s, interposers or microbump joints) and that the stacking introduces new mechanical/thermal/electrical/environmental stresses caused by different geometric and structural designs of the new package. To prevent that, advances in Design for Reliability (*DfR*) and Design for Yield (*DfY*) are very needed, as well as improvements in the process know-how, such as the discovery [220] of the better electromigration using much smaller solder microbumps.

- **Cost:** this is the main hardstop nowadays for this technology, since the introduction of various sophisticated process steps (*TSV*, microbumping, etc.) are extra cost for the manufacturing. The cost has to be reduced in numeral aspects: from basic materials and chemicals, covering also equipment/process optimization, integration, stacking, packaging and assembly, to the final product testing, yield improvement and reliability. Removing the intermittent product shipping and testing is one important aspect (particularly when these semi-products are thin and fragile) to achieve the cost reduction. Using integrated design and production flow is another. And clear ownership on the production yield and cost control is the final [217].

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5. Conclusions

The Moore's law is not only the analysis of the electronics evolution, but also the driving force to guide new breakthroughs to continue scaling the transistor size. Some years ago, no one would have bet to have the current technology: smartphones able to fold, biometric identification, smart wearables, *3D*-printing, domotics or Artificial Intelligence, among others. But the reality is that technology continues to surprise us with new ways of re-inventing the way to interact with the environment, making easier for the user to gather information to improve his/her quality of life -that is how they sell it. Even what we think that nowadays is normal, in a couple of years will be obsolete, and our pioneer technology will be considered primitive.

The reader has been driven through the evolution of the photolithography, understanding the process behind to better comprehend how it has evolved thanks to improvements with respect to physics and optics. What some years ago, the *DUV*, was considered the innovation, has been improved by the immersion lithography, and after that by the *EUV*. But one does not have to forget that all new technologies need a lot of validation to get costwise effective. There are even technologies who were thought to be the future but suddenly disappeared: would you remember the Blackberry phones which was trendy for some years in the 2000s? They bet for one solution which resulted to not appeal to the market (versus the *LCD*-smartphones), thus becoming bankrupt after some years.

The bottom line is here: we are all impressed about the news of releasing a phone with a microprocessor built in 5 *nm* technology-node, how good and fast must be, but the cost and the time to market is very important too, not talking about the marketing. So the conclusion is: even if we are delighted by the capabilities of this new technologies -e.g. *EUV*-, what is currently providing money to the market is the *DUV*, both wet and dry tools. In five years, it is expected that the trends will be leading to *EUV*, where the majority of the foundries will adopt those systems but, for the moment, the driven force -the one which sustains the microelectronics market and the preference for the consumers in terms of used devices- is the safe approach, the *DUV*.

And in parallel there is that *3D*-integration, also fascinating us with the potential of improving efficiency while enhancing the systems. What is -literally- the price for that? It is true that some market applications, such as the *NAND* memories, are increasingly adopting the *3D*-approach to get it into the market. For that concrete example, the whole industry is moving to the *3D*-integration, even the photolithography tool manufacturers are investing in that -or at least trying to keep up with the metrology systems for those applications. Furthermore, the image sensors segment have showed a clear increase in the *3D* adoption by allowing to add some processing functions keeping the same pixel size. But for the rest, what is the real implementation of the *3D*-circuits? For the moment, almost null, and the reason being is rather simple: money. *3D*-integration is not yet costwise efficient, the yield and reliability issues which has been highlighted during this thesis makes the foundries not able to get it into *HVM* making a

profit from that. What will happen in a couple of years, it is still unknown but, roughly speaking, the *3D*-integration is not a serious alternative for the moment to the conventional lithography.

Thinking about the *3D*-photolithography as doable alternative to integrate both advancements, seems to me something to far away. It is clear that there are some results, do not get my wrong, but one thing is to manufacture a prototype and another call is to make money in a mass production-manner. It sounds as all those new materials -such as the carbon nanotubes- or technologies -quantum cells- with spectacular results, which are all said to be the future, but only the intrepid investors are going to put some money on that, not still affordable -or accessible- to the general public.

Bearing in mind all the above arguments, in my opinion nowadays it is clear that the mainstream is continuing using *DUV*, increasingly the market share for wet tools since they have been demonstrated to improve the patterning size in a costly-effective way. *EUV* is promising, true, but so far only manufactured by one supplier, which is investing a lot of money on that. Nevertheless, also influenced by my subjective experience of currently being working for that supplier, I am convinced that the *EUV* is the way to go for the industry during some years. The major foundries are convinced on that, as well as *ASML* collaborators, and the *HVM* for *EUV* is now there: it is just a matter of years to get it more mature to dominate the market versus the *DUV*. With respect to the *3D*-integration, I admit there are some market lines moving quickly to that direction, and I am sure that they well know why: the performance improvement must have been demonstrated expecting to make money from that. But do not forget this is only some products where the *3D*-integration may fit better: it is more an alternative for new products -with enhanced features- than a sustitutive. With that I mean: do not imagine a microprocessor for the new iPhone built with *3D*-Integrated Circuits, do imagine a microprocessor built with the most powerful -and costly-efficient demonstrated- *EUV* photolithography tool.

But of course, there are some facts and opinions in the previous quote. Do remember what happened to Blackberry for being focus in one application, or how Microsoft was laughing at Apple when they proposed their disruptive concept of phones. The future looks fascinating: new materials, new technologies and new devices, and everything comes in a world which demands more and more technology to the daily lives. What will the human being be able to achieve? Nothing seems impossible…

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