Enhancement of the Dynamic Performance of Electrolyte-Gated Transistors: Toward Fast-Switching, Low-Operating Voltage Printed Electronics

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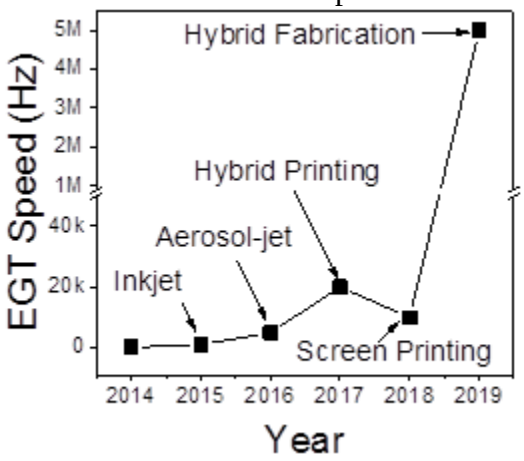
Dedicated to my uncle "Dayi Mehdi" whose memory has been always with us.

Abstract

A transistor is an electrical circuit element which acts as a switch, can tune the current in an electrical circuit, and can amplify input signals. Fast switching with low-operating voltage and high amplification are desired characteristics for transistors but are not readily achieved by printed electronics. Electrolyte-gated transistors (EGTs) are a specific class of transistors with an electrolyte as the gate dielectric. Using electrolyte as the gate dielectric enables low-operating voltage, high amplification (gain), and relaxed fabrication requirements. Electrolytes have a huge capacitance which is thickness independent thanks to the formation of electrical double layers (EDL) at the interfaces of the electrolyte with the electrodes. Ion gel is a type of electrolyte consisting of an ionic liquid and a triblock copolymer. The polymer is responsible for providing the mechanical integrity, whereas the ionic liquid is responsible for the gating mechanism with great electrical, physical, chemical, and electrochemical properties. Ion gels pave the way for miniaturizing EGTs and their use in printed electronics. Despite all the promising properties of printed EGTs including low-operating voltage, ease of printing, flexibility, and low-toxicity, fast EGTs have not yet been demonstrated. Similarly, higher EGT gain is also required to improve the sensitivity and computational power of devices. In this thesis, the EGT working principles have been investigated, as well as the effects of EGT architectures, materials, components, printing resolution, and precision on the EGT operating speed and gain. New architectures have been designed to produce fast and high-performance EGTs.



Modification of EGT architectures and components enabled us to achieve 5 MHz operation with an order of magnitude increase in gain and amplification. In order to fabricate different architectures, a variety of techniques including inkjet, aerosol-jet, and screen printing have been employed. Screen-printed, UV-cured ion gels with a line width resolution of 10 μm have been demonstrated. In conclusion, in this thesis, the performance of printed ion gel-based electrolyte-gated transistors has been investigated and improved by relating the device dynamic and static characteristics to its material components and architecture.

Table of content

List of Figures

Chapter 1 Introduction

1.1 Motivation of Thesis

EGTs with ion gels as the dielectrics have been demonstrated for many great potential applications including printed electronics and floating-gate transistors due to their superior properties-i.e. high reproducibility, ease of printing, robustness, electrochemical and physical stability, low-power consumption, high transconductance, high sensitivity, and miniaturizability.[1–8] These great quasi-static qualities make EGTs very promising for sensing applications where the time scale is on the order of seconds.[9]

Despite all the great potential applications for EGTs in fields including printed electronics and biosensing, their response time or switching frequency has been a challenge and limited their utilization for the last 15 years.[2,10,11] Speed is important for applications such as displays or computation centers. A small foldable liquid crystal display (LCD) requires a transistor switching speed of ~100 kHz whereas most EGTs hardly achieve a dynamic performance of hundreds of Hz.[12]

The goal of this thesis is to investigate the dynamic and static performance of EGTs. First, the parameters that affect the dynamic performance are explored to determine the limiting factor for switching speed. Then, strategies are developed to resolve the dynamic problem while improving the quasi-static performance as well. In the end of this thesis, EGTs with the best reported static and dynamic performance are presented.

1.2 Overview of Thesis

Chapter 2 introduces the basic aspects of field-effect transistors (FETs) and printed electronics. The physics of field-effect transistors and their components are included.

Special focus is on the pros and cons of printed electronics in comparison to Si technology. Printed electronics are believed to be a good candidate for flexible, large-area, low-cost applications. Different printing techniques are introduced for fabricating electronics and the challenges forced by printed electronics are discussed.

Chapter 3 introduces the basic aspects of electrolyte gating. This chapter discusses working principles of electrolyte gating, electrolyte materials, ion gel, applications of electrolyte-gated transistors and their requirements, and challenges for electrolyte-gated transistors.

Chapter 4 summarizes the experimental methods used in this thesis, aerosol-jet printing, inkjet printing, atomic layer deposition, micro fabrication, and different electrical characterization techniques.

Chapter 5 summarizes work done to better understand the dynamic performance of electrolyte-gated transistor by studying poly(3-hexylthiophene) electrolyte-gated transistors as the well-established electrolyte-gated platform. Resistor loaded inverter circuits were investigated with square-wave input. Channel length is shown to not be the limiting factor for the electrolyte-gated transistor performance. Further studies showed that ion gel overlap with the source/drain electrodes, "*parasitic capacitance*" causes voltage overshoots which ruin the dynamic performance. This work has been published as F. Zare Bidoky and C. D. Frisbie, "Parasitic Capacitance Effect on Dynamic Performance of Aerosol-Jet-Printed Sub 2 V Poly(3-Hexylthiophene) Electrolyte-Gated Transistors." *ACS Appl. Mater. Interfaces* **2016**, *8* (40), 27012–27017.

Chapter 6 summarizes work done to further study parasitic capacitance effects on printed poly(3-hexylthiophene) electrolyte gated transistors. A combination of different printing

and coating systems were employed to cover the top surfaces of source/drain electrodes with an ion-impermeable polymer to minimized parasitic capacitance. Three orders of magnitude gain in the dynamic performance of resistor-loaded inverters is reported. This work has been published as F. Zare Bidoky, W. J. Hyun, D. Song, C. D. Frisbie, "Printed, 1 V Electrolyte-Gated Transistors Based on Poly(3-Hexylthiophene) Operating at >10 kHz on Plastic." *Appl. Phys. Lett.* **2018**, *113* (5), 53301.

Chapter 7 summarizes work done to fabricate and characterize all photo-patterned ZnO electrolyte-gated transistors. This chapter includes an extensive fabrication process to produce the most precise electrolyte-gated transistors with improved semiconductor quality and thus device performance. The semiconductor mobility as the major metric of semiconductor quality is improved 10 times in comparison to polymeric semiconductors which yields in 5 times better sensitivity in the final device. Further studies on dynamic performance of photo-patterned ion gel-base transistors show slight improvement to previously reported non-crosslinked ion gel devices. The photo-patterned ion gel resistance, "*parasitic series resistance*", measured through impedance analysis, is shown to be responsible for limiting the dynamic performance. This work has been published as F. Zare Bidoky, B. Tang, R. Ma, K. S. Jochem, W. J. Hyun, D. Song, S. J. Koester, T. P. Lodge, and C. D. Frisbie, "Sub-3 V ZnO Electrolyte-Gated Transistors and Circuits with Screen-Printed and Photo-Crosslinked Ion Gel Gate Dielectrics: New Routes to Improved Performance", *Adv. Funct. Mater.* Just Accepted.

Chapter 8 summarizes some of the ongoing research and proposes potential directions for future research based on the above findings. It summarizes work done to explore the speed limit of ZnO electrolyte-gated transistors by minimizing all the parasitic effects. The

semiconductor and device architecture are borrowed from Chapter 7 where the parasitic capacitance is minimized, and the ion gel and gate deposition are from Chapters 6 and 5 where the ion gel has maximum ionic conductivity. The final devices have shown stage-switching speeds of 8 MHz in the 5-stage ring oscillator platform which is close to the theoretical limits of the ion gel gating speed. This work is under preparation for publication as F. Zare Bidoky and C. D. Frisbie, “10 MHz class printed ion gel-base thin film transistors”. Finally, future avenues for further studies on electrolyte-gating mechanisms and improved printed electrolyte-gated transistors are described.

Chapter 2 Printed Electronics as a Complementary Fabrication Method to Traditional Si Technology

Printed electronics is a growing industry with many applications evolving including large-area displays, foldable LCDs, flexible and wearable electronics, and fabrication of electronics on the curved surfaces.[12–14] In order to develop these attractive applications, the building blocks of electronic circuitries must be printed. Transistors are one of the main components of each electronic devices.

2.1 Transistors

Transistors are electric switches which act like gate valves in a pipe line or an amplifier, Figure 2.1.[15] Transistors have 3 terminals called source, drain, and gate, Figure 2.1.a. The current between source and drain is controlled by the gate voltage, Figure 2.1.b-d. Field effect transistors consist of 3 main materials, namely conductor, semiconductor, and insulator, Figure 2.1.e. The terminals are conductive. The source and drain are connected by a semiconductor channel. The gate is insulated from them by the insulator dielectric. Field effect transistors use the electric field applied by a gate potential, V_G, over the dielectric to control the amount of charge floating between the source and drain, Is_D, passing through the semiconductor. When the semiconductor is conductive, Figure 2.1.b, the transistor is acting as open valve, Figure 2.1.c, which is called the ON state, Figure 2.1.d.

2.1.1 Transistor Components

Every transistor has at least 3 different materials, as depicted in Figure 2.1.e. Conductors, semiconductors, and insulators are the necessary electronic materials. In the

following section examples of these materials and compatibility with different fabrication processes are discussed.

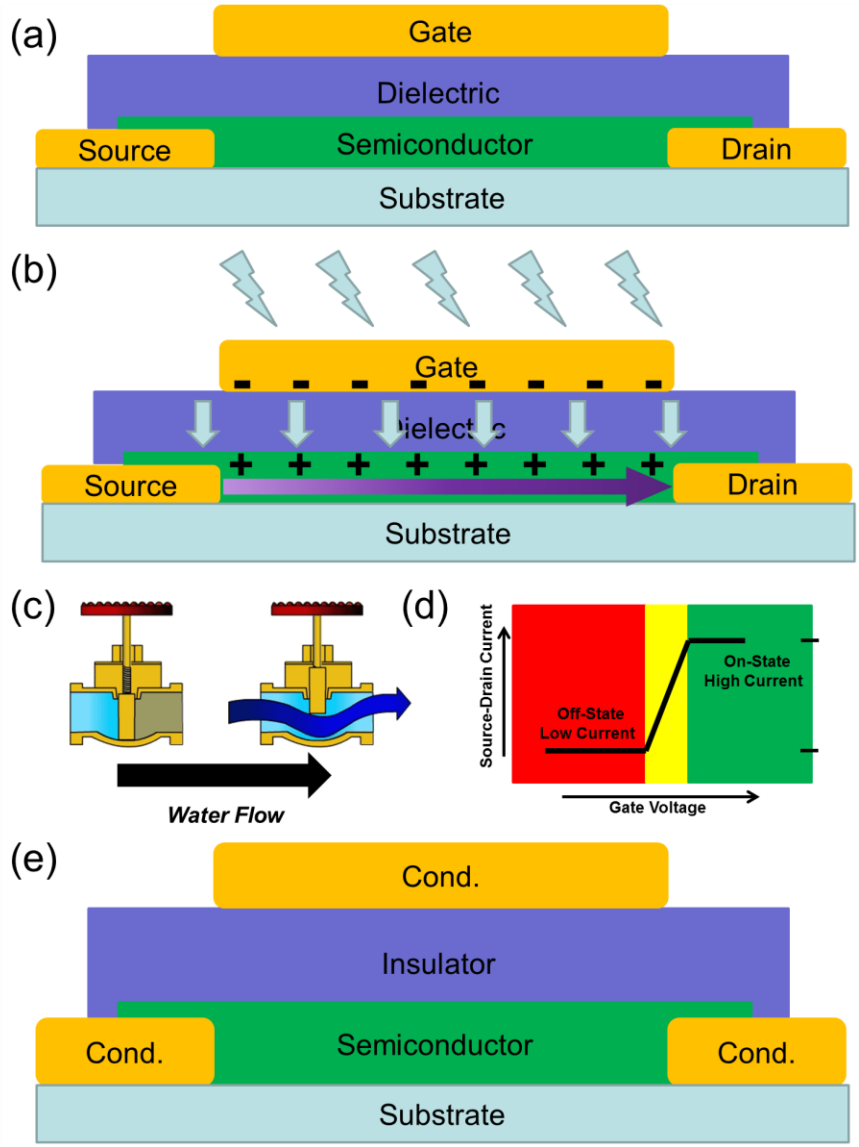


Figure 2.1. Field effect transistors. a) Schematic drawing, b) working principle of field effect transistor. c) transistor acts as a pipeline valve. d) source-drain current (I_{DS}) is controlled by gate voltage (V_G). e) The electronic materials required for field effect transistors are displayed.

2.1.1.1 Conductors and Metals

Metals such as Au and Cu are known for their high conductivity. In Si technology, physical vapor deposition methods are usually used to evaporate metals and deposit them on the substrate. Conductive polymers, nano particle based, and reactive metalic inks are developed for other fabrication process such as additive manufacturing, Figure 2.2. Poly(3,4-thylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) is a commonly used conductive material for solution-based fabrication methods, Figure 2.2.a and b.[16] Reactive silver ink is another conductive ink which leaves a thin conductive layer which is often followed by electroless plating, Figure 2.2 c.[17–19] Electroless plating is also used to improve the metal conductivity in many industries including electronics fabrication.[18]

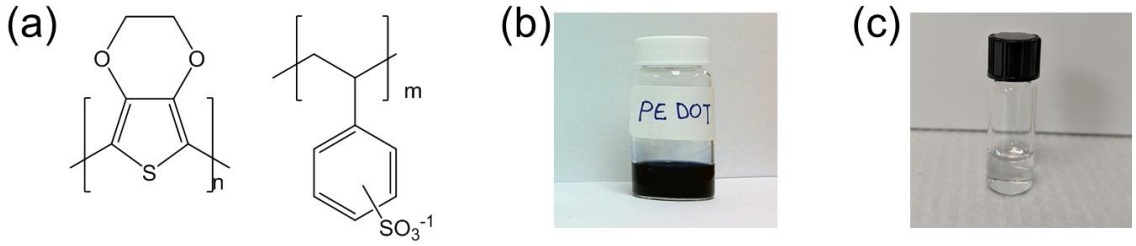


Figure 2.2. Conductive inks. Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate a) chemical structure,[20] b) ink in aqueous solution. c) Silver reactive ink prepared in house. Reproduced with permission from Reference 20.

2.1.1.2 Semiconductors

Semiconductors are materials whose conductivity can be tuned over a wide range by applying some input, which in this thesis could be chemical or electrical. Si is the main semiconductor which almost all the electronics applications are based on. In micro and nano fabrication, the process starts with a Si substrate and the circuit components are built

upon it by doping the Si, growing an oxide on the silicon, or chemical and physical deposition on the silicon. Other semiconductors such as ZnO are developed for different applications including solar cells and displays.[21] Polymeric semiconductors such poly(3-hexylthiophene), metal oxide inks, and carbon nano tube solutions are developed for solution based fabrication, Figure 2.3.[20,22–25]

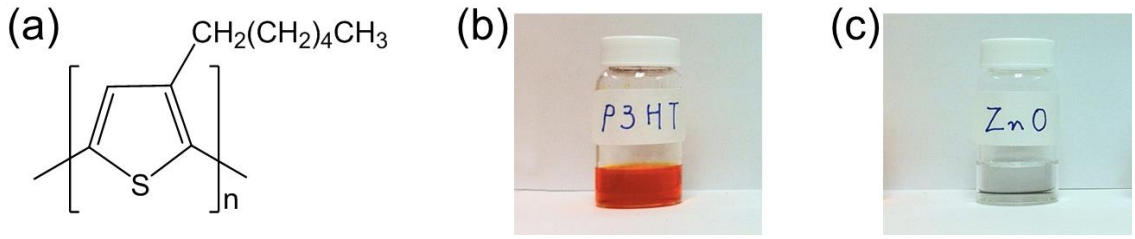


Figure 2.3. Semiconductor inks. Poly(3-hexylthiophene) a) chemical structure, b) ink in chloroform (1mg/ml) solution. c) ZnO ink prepared in house.[20] Reproduced with permission from Reference 20.

2.1.1.3 Insulators and Dielectrics

The last but not least component of transistors is the dielectric which is an insulating material responsible for inducing charge in the semiconductor channel. SiO_2 is the most common dielectric used in electronics which has a relative dielectric constant, κ, of 3.9.[26] A normal polymer such as polystyrene has a κ of ~2.5.[27,28] The importance of the dielectric constant and the dielectric thickness can be seen from the Equation 2.1:

$$I_{SD} \propto C_{dielectric} V_G \tag{2.1}$$

Where I_{SD} is the current passing through the semiconductor from the source to the drain electrode, $C_{dielectric}$ is the insulator dielectric, and the V_G is the applied gate voltage. $C_{dielectric}$ is defined by Equation 2.2.

$$C_{dielectric} \propto \kappa/t \tag{2.2}$$

t is the thickness of the dielectric. By lowering t, operating voltage is reduced. Depending on the fabrication method there is a limit on *t*. Changing the dielectric to a high-κ dielectrics such as HfO_2, with 4-6 times higher dielectric constant compares to SiO_2, allows further reduction of operating voltage in Si-based thin film transistors (TFTs).[29]

2.2 Flexible Electronics

Si technology has been developed over more than 50 years and optimized into a mature technology that enables many fantastic applications from smart phones to super computers. New applications including wearable electronics,[30–32] E-skins,[33] and foldable displays[34] require mechanical flexibility in the circuits. However, making flexible circuits from brittle Si wafers is not easy. In order to make Si flexible, it must be etched to less than 20 μm thick and all the fabrication states, including photolithography and depositions, should be done on the thinned wafer. Therefore, Si technology is very expensive to make flexible.[35]

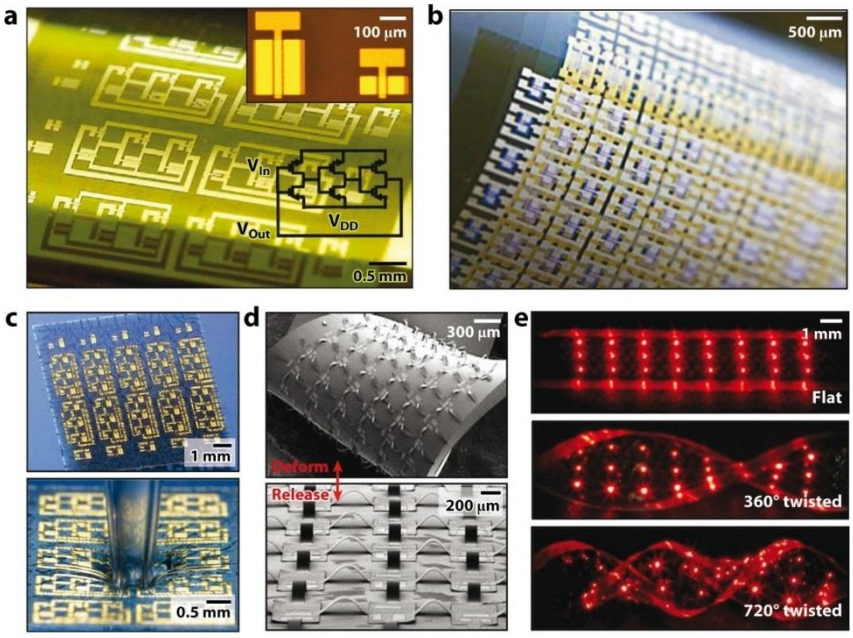


Figure 2.4. Examples of flexible thinned silicon-based electronics for different applications.[35] Reproduced with permission from Reference 35.

There is a need for inherently flexible materials which are easy to process and enable cost effective fabrication of flexible electronics.

2.3 Organic Electronics

Organic electronic materials are the complementary functional materials to inorganic materials. Although the electronic properties of organic electronics are not as good as those of inorganic electronic materials, there are flexibilities in fabrication, material processing, mechanical properties, and synthesis routes which make organic electronic materials a suitable candidate to be used for flexible electronics.[36] Examples of organic semiconductors which have been developed and studied include rubrene single crystals with charge carrier mobility, μ, as high as 15 cm^2/Vs.[37–41] Organic dielectrics have been investigated and high-κ polymeric dielectric such as poly(vinylidene fluoride-co-trifluoroethylene) with κ as high of 50 and high hydrophobicity have been developed.[42–44] For conductive materials, PEDOT:PSS is the most commonly used organic conductive material.

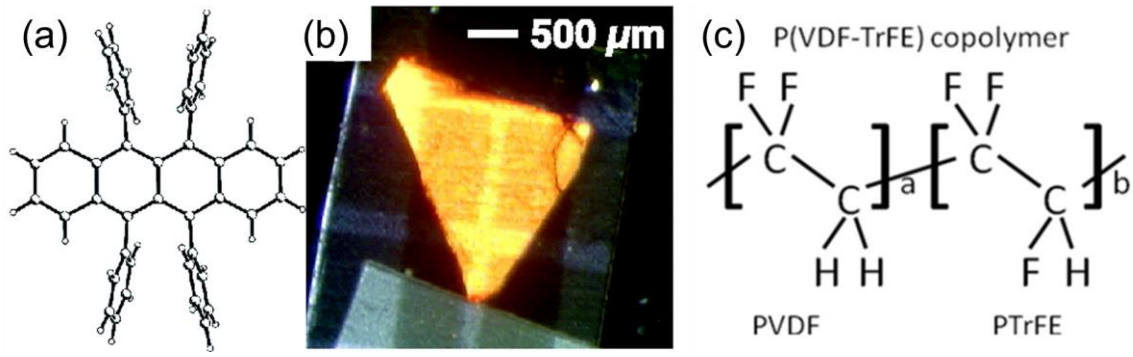


Figure 2.5. Organic electronic examples. a) chemical structure and b) optical image of rubrene single crystal.[41] c) chemical structure of poly (vinylidene fluoride-co-trifluoro ethylene)[44]. Reproduced with permission from Reference 41.

2.4 Printed Electronics

Printing electronics is an alternative to Si technology for the fabrication of flexible electronic devices.[13] Printing is an additive manufacturing process where the functional material is only added where it is required in comparison to etch-based silicon technology in which functional material is first deposited everywhere and then patterned by an etching or lift-off process.[12] Consequently, printing electronics produces less electronic waste. Printed electronics do not need the high-vacuum chambers and high temperature evaporation systems for material deposition which makes it more energy efficient over Si technology.

Printed electronics are compatible with variety of substrate materials including plastic substrates. Printer head can deliver ink on the curved surfaces, which also makes printed electronics viable for applications such as antenna fabrication on the car bodies or sensors on human skin.

2.4.1 Solution Process

Most organic electronic materials are soluble in organic solvents and consequently, there are many electronic inks prepared for printed electronics. This allows printing different layers in sequential order to fabricate transistors and make circuits.

2.4.2. High Throughput Fabrication

Printed electronics can be adopted to high throughput manufacturing such as roll-to-roll systems and make circuit fabrication as fast as news press printing. This

compatibility, in principle, should make large-area, low-cost, printed, flexible application available, especially for large displays or solar cell panels.

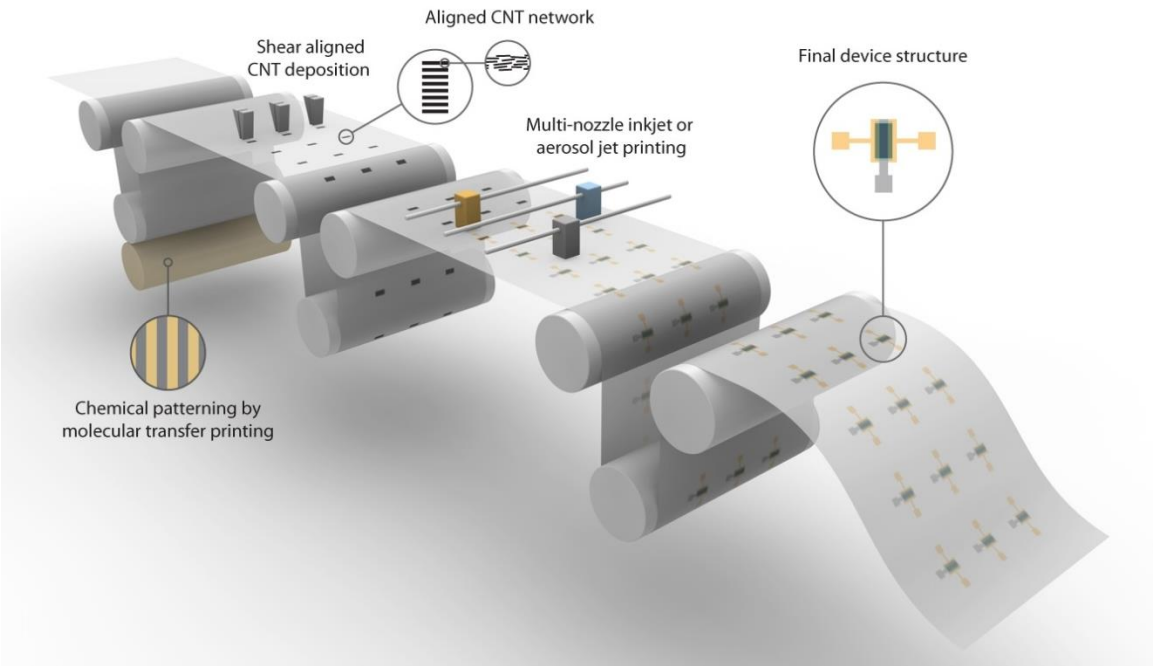


Figure 2.6. Printed electronic illustration as a compatible fabrication method with high-throughput manufacturing such as roll-to-roll process.[45]

2.4.3 Printing Techniques:

Screen printing, inkjet printing, and aerosol-jet printing are the common printing techniques used for printed electronics and each one has its own pros and cons.

2.4.3.1 Screen Printing

Screen printing is the most common printing technique in industry with minimum resolution of 50 μm and high viscosity ink requirements (>1000 cpoise) which limits available inks.[46] Screen printing is a reliable method for deposition large conductive pads and lines. Alignment of sequential layers and limited electronics inks availability are the problems for fabricating thin film transistors by screen printing.

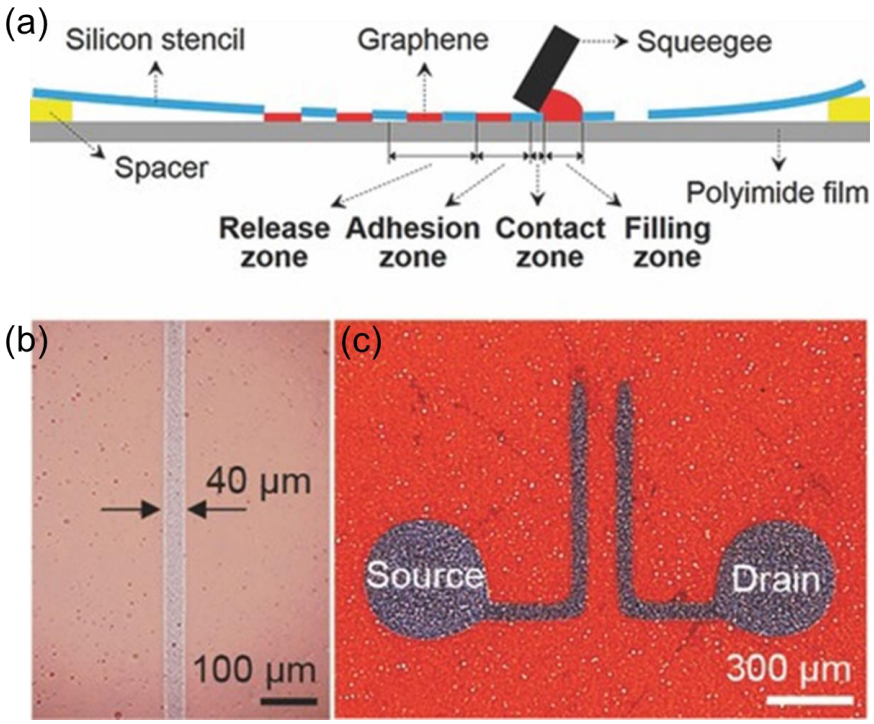


Figure 2.7. Screen Printing.[46] a) The scheme of screen printing used for high resolution graphene printed lines. Silicon stencil, squeegee, and the spacer are shown as the main components of the printer. The resolution of the printed line is defined by the stencil resolution and ink viscosity. The optical image of b) a printed line and c) electrodes for EGTs fabrication. Reproduced with permission from Reference 46.

2.4.3.2 Inkjet Printing

Inkjet printing is the second most common type of printing electronics in the industry, which works with lower viscosity inks (~1-20 cpoise).[24,47,48] Nano particle based (NPB) and particle free inks have been developed for inkjet printing. Inkjet printing is a nozzle-based printing method with a minimum line width resolution of 2 µm. Drop-on-a-demand is type of inkjet printer which delivers a certain number of droplets to a specified area. The drop-on-a-demand inkjet printer has 3 main parts, ink reservoir, piezoelectric actuator,[49,50] and nozzle. The nozzle head is shown in Figure 2.6.

Figure 2.8. Piezoelectric inkjet head. The piezoelectric actuator pushs the droplets out of the nozzles.[24] Reproduced with permission from Reference 24.

Recent reports on inkjet printing on prepatterned substrates have shown resolutions of printing down to 500 nm.[51]

2.4.3.3 Aerosol-Jet Printing

Aerosol-jet printing (AJP) is another nozzle-based printing technique which is readily applicable for printing on curved surfaces or for making prototype devices. The viscosity range for AJP is wider than inkjet printing (1-50 cpoise). Commercial AJPs have resolutions of ~5 μm. Figure 2.7 shows the main components of the AJP.[24]

2.4.4 Printed Electronics Challenges

Despite all the benefits of printed electronics, there are shortcomings as well including low resolution, non-precise alignment, loose control on the film thickness, and

poor reproducibility. These limitations in fabrication limit the printed device performances, which are discussed in the following sections.

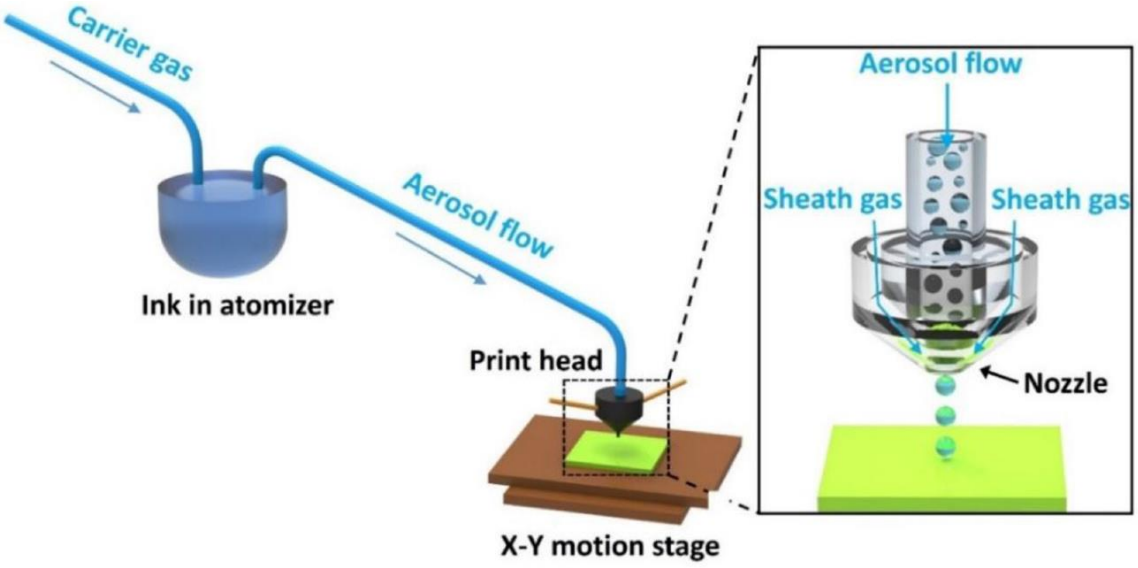


Figure 2.9. Aerosol-jet printer. The ink is atomized in the ink bank which is carried by inert gas (carrier gas) to print head. In the print head another flow, sheath flow, focuses the aerosols on the substrate.[24] Reproduced with permission from Reference 24.

2.4.4.1 Operating Voltage

In order to prevent pinhole formation in the dielectric layer for printed TFTs, the printed dielectric is a couple of hundreds of nanometers thick with variance of at least 10%. Considering Equations 1 and 2, the operating voltage for printed thin film transistors is more than 20 V.[28] This power cannot be supplied by printed batteries or commonly available commercial batteries.[52–56] Channel current at fixed gate voltage also has a huge variation due to thickness variation. Consequently, the reproducibility of the printed transistors is poor which makes circuit design and manufacturability almost impossible.

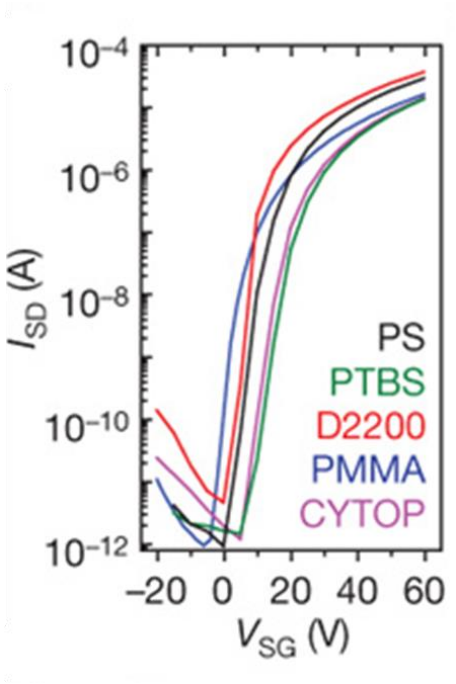


Figure 2.10. Printed organic transistor transfer curve. Different polymers are used as dielectric and a 20 V gate voltage is required to turn the device ON.[28] Reproduced with permission from Reference 28.

2.4.3.2 Working Frequency

Applications such as foldable displays or the computing units for wearable electronics need printed transistors to operate at high frequencies (100 kHz to some MHz).[12,54] However, most printed electronics circuitry cannot satisfy this TFT switching frequency, and even those which work at high frequencies require high operating voltage and have low fabrication yield.

Therefore, there is a clear need for low-operating voltage, fast-switching, printed thin film transistors.

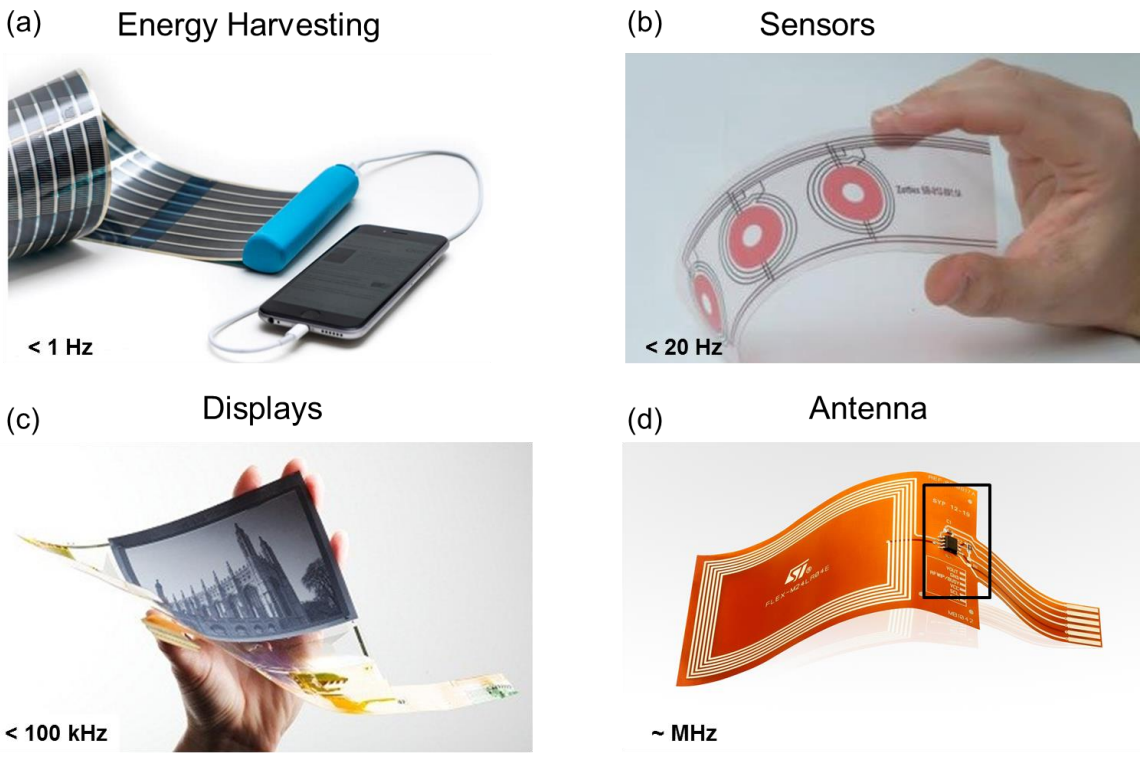


Figure 2.11. Examples of switching speed requirement for printed and flexible electronics. a) Foldable solar cells with almost no switching speed requirements,[57] b) Biosensors with working frequencies lower than 20 Hz,[58] c) foldable display with required frequencies of kHz,[59] and d) computing system for flexible antennae which requires high speed data processing are shown as examples of flexible electronics applications.[60]

Chapter 3 Electrolyte Gating

3.1 Electrolytes

Electrolytes are solutions with mobile ions such as aqueous solution of rock salt or ionic liquids.[61–63] Unlike traditional dielectrics, electrolytes have interesting electrical properties including thickness independent capacitance.[64] This is very important when it comes to thick films or when using fabrication methods with relaxed thickness resolution. For example, a 1 μm thick ionic liquid film has 10^3 to 10^6 times higher capacitance than SiO_2.[1] This in turn facilitates much lower power requirements for charging, for example in a capacitor.[65] Therefore, it is of interest to utilize electrolytes as dielectrics, especially in transistors.[1]

3.2 Electrolyte-Gating and Capacitance Mechanism

Electrolyte gating is caused by ion migration to the interfaces upon the application of an electrical field. [1] Ions will either form an electrical double layer (EDL)[66] at the interface of electrolyte and semiconductor/conductor or penetrate into semiconductor/conductor organic film and electrochemically dope the film (ECD). [1,67] Figure 3.1 shows the electrolyte gating effect for both ion-permeable and ion-impermeable organic layers. For EDL, the specific capacitance is on the order of 1-10 $\mu F/cm^2$, whereas for ECD it is 100 $\mu F/cm^2$.[1]

3.3 Ionic Liquids as Electrolytes

Ionic liquids are room temperature molten salts with negligible vapor pressure. Ionic liquids have high ionic conductivity (~mS μm^{-1}), are electrochemically stable to3 V, and are physically and chemically stable.[62,68,69] Ionic liquids have an EDL capacitance of

~50 μF/cm^2. [66] Ionic liquids consist of an anion and cation that cannot make a solid crystal. An example of ionic liquids that has commonly been used in this research is EMI TFSI, Figure 3.2.

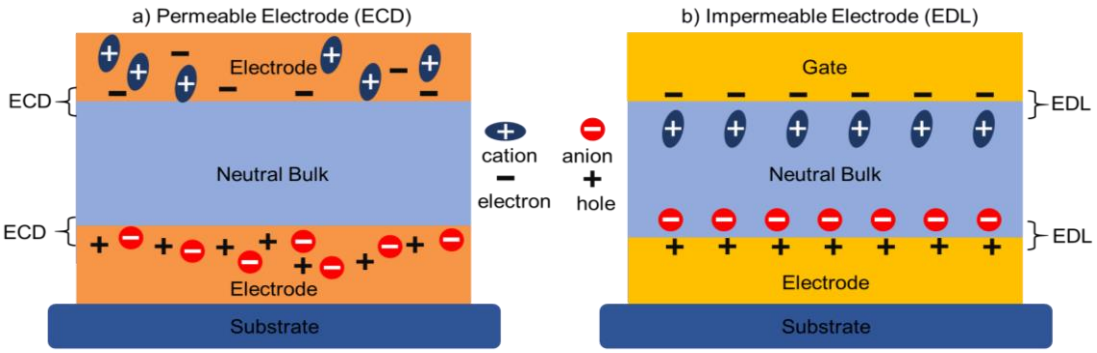


Figure 3.1. Charge accumulation mechanisms in electrolyte capacitors. a) Electrochemical doping in ion-permeable electrode such as amorphous polymeric film. b) Electrical double layer formation (electrostatic charging) at the interface of ion-impermeable electrodes such as Au.

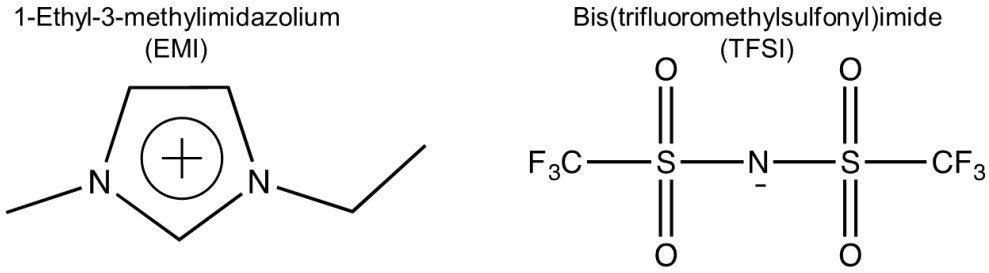


Figure 3.2. Example of ionic liquid. Chemical structure of 1-ethyl-3-methlimidazolium (EMI) bis(trifluoromethulsulfonyl)imide is drawn.

These great properties make ionic liquids a potential candidate as a dielectric especially for printed electronics. However, it is not easy to maintain liquids especially sandwiched in the thin film transistor architecture.

3.4 Ion Gels

Ion gels are a mixture of ionic liquids with polymers which give mechanical robustness to the ionic liquids when used in thin film transistor applications.[70] Tri-block polymers with midblocks and endblocks soluble and non-soluble in ionic liquid,

respectively, are a commonly used polymer in ion gel formulations.[2] The polymer is usually a triblock copolymer where the endblocks are not soluble and make nodes whereas the midblock is dissolved in the ionic liquid and responsible for holding up the ionic liquid in the ion gel.[71] The endblocks phase separate and form nodes which are responsible for holding the 3D structure of the gel whereas the midblocks are responsible for holding ionic liquids in the ion gel.[72] Examples of tri-block copolymer are polystyrene-*b*-polymethylacrylate-*b*-polystyrene (SMS) and polystyrene-*b*-polyethylacrylate-*b*-polystyrene (SEAS), Figure 3.3.[3]

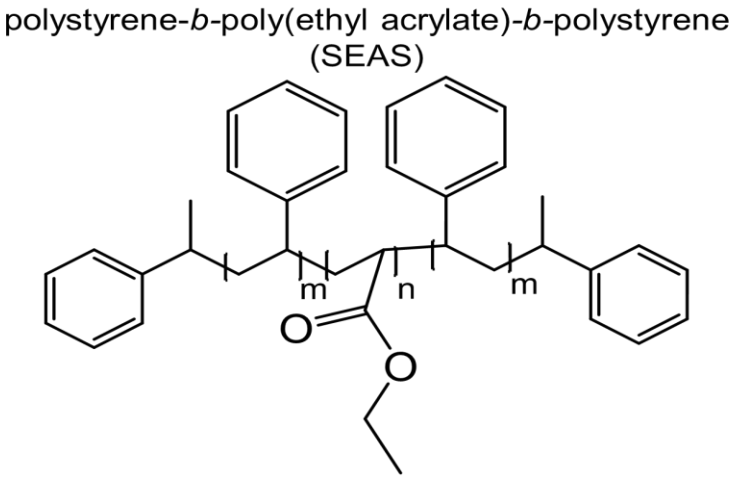


Figure 3.3. Chemical structure of ABA triblock polymer polystyrene-*b*-poly(ethyl acrylate)-*b*-polystyrene which is an optimized polymer for ion gel solution with high ionic conductivity.

Ion gels have electrochemical stability window of ~±3 V and high ionic conductivity. In order to make ion gels, ionic liquids are often mixed with 10-20 w% polymer. An example illustration of the ion gel has been shown in Figure 3.4.[72–74]

Ion gels also have other applications besides dielectrics in thin film transistors, such as iono-elastomers that can be used as strain sensing elements. This application is further discussed in Apendix A1 as it is not the main focus of this thesis.[75,76]

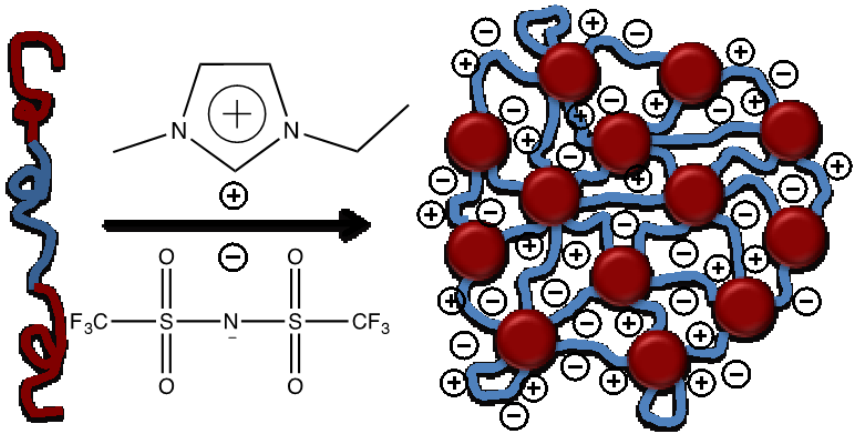


Figure 3.4. Ion gel formation by an ABA triblock polymer with soluble midblock (B) and insoluble end blocks (A) and ionic liquid is shown with + and – symbols indicating respective ions.[77,78]

3.5 Electrolyte-Gated Transistors

Electrolyte-gated transistors (EGTs) are also called ion gel-gated transistors and consists of two main categories, electrical double layers transistors (EDLTs) and organic electrochemical transistors (OECTs).[1] In both categories, the ions are responsible for charging the semiconductor. As is implied by the names, in EDLTs, ions make an electrical double layer at the interface of electrolyte and the semiconductor/conductive materials, whereas in OECTs ions electrochemically dope the organic functional film. The charging/gating mechanism is shown in Figure 3.5.[1]

OECTs main application is in biosensing where the electrolyte or the semiconductor is exposed to the analyte and changes in the current are plotted as the signal and calibrated vs. the concentration.[79] EDLTs are often used for semiconductor and charge transport mechanism studies with more focused on the science and physics.[66] Nonetheless, EGTs have found their way into thin film transistor applications mainly after the application of the ion gel as the dielectric.[2]

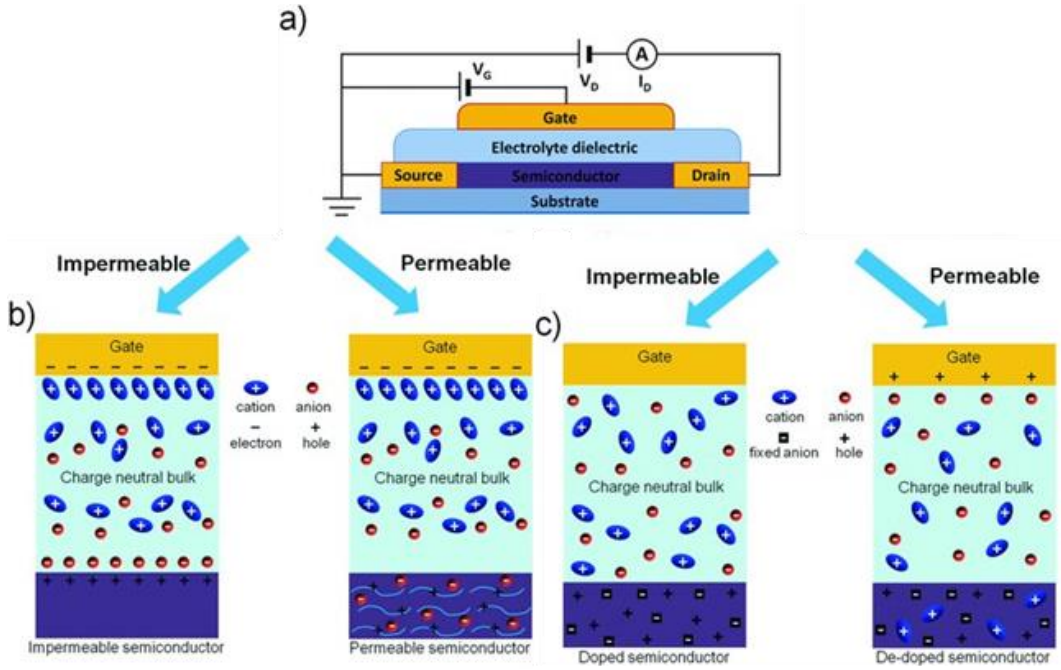


Figure 3.5. (a) Cross-section of an EGT. (b) Carrier accumulation-mode operation of an EGT for un-doped ion-impermeable (left) and permeable semiconductors (right) and (c) depletion-mode operation for degenerately doped semiconductors without (left) and with (right).[1] Reproduced with permission from Reference 1.

3.6 Quasi-Static Performance

In comparison to other printed TFTs, EGTs have excellent and reproducible electrical properties including low-operating voltage (threshold voltage, $|V_{th}|$ <1V), high ON/OFF current ratios (I_{ON}/I_{OFF} ~ 10^6),[1] high width-normalized transconductance (g_m/W ~ 400 S m^{-1}),[80] high charge carrier mobility (μ ~ 10 cm^2/Vs), small power dissipation (~ 1 nwatt),[1] and ultra-low contact resistance (~ 20 Ω/cm).[81] These properties are characterized from the quasi-static measurements of the EGTs (transfer curves (I_D-V_G), output characteristics (I_D-V_D), and displacement (I_G-V_G) current measurements, Figure 3.6.

$$I_{DS} = \mu \frac{W}{2L} C[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \qquad V_{DS} < V_{GS} - V_T \tag{4.1}$$

$$I_{DS} = \mu \frac{W}{2L} C(V_{GS} - V_T)^2 \qquad V_{DS} > V_{GS} - V_T \tag{4.2}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}\mu\, C_G V_D \qquad V_{DS} > V_{GS} - V_T \qquad (4.3)$$

Equations 4.1-3 defines I_{SD} and transconductance (g_m). g_m is important for sensing application and is proportional to the sensor sensitivity.[82]

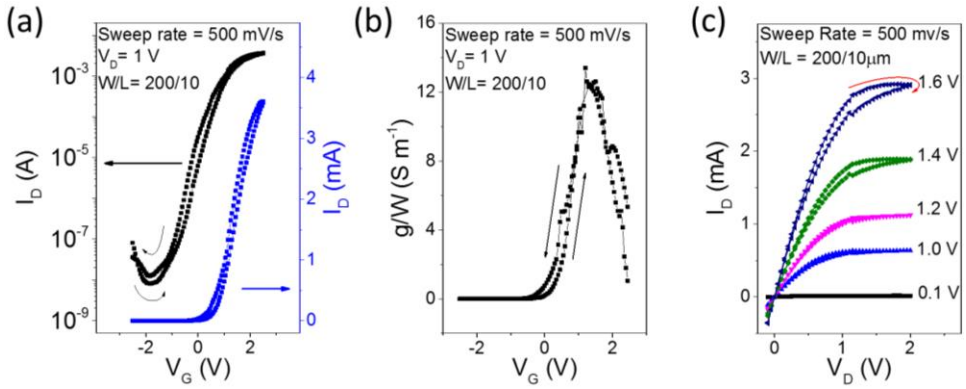


Figure 3.6. ZnO electrolyte-gated transistor quasi-static performance. The transfer curve for EGT with W/L = 200 µm/10 µm at 500 mV/s gate voltage sweep rate and V_D = 1 V. d) The channel-width-normalized transconductance of the device. e) The output characteristics of the EGT at different V_G's.

3.6.1 Floating Gate Electrolyte-Gated Transistor Bio-sensors

The great electrical characteristics of EGTs and the favorable aspects including, biocompatibility and ease of fabrication make EGTs a potential candidate for biosensor applications.

Floating gate EGT biosensors (FGEGTs) (Figure 3.7) consist of an EGT which has a floating gate capacitively coupled with the transistor gate and the input.[4,9,83,84] The sensing happens on the surface of the floating gate where the interface of the electrode is decorated with functionalized molecules, and in the presence of the analyte the capacitance changes resulting in a change of gate voltage measured by the transistor. Tracking changes in the channel current, I_{SD}, vs. the analyte concentration create a calibration curve. These

sensors are cost effective and easy to make which leads to a great potential for online quality controls in food and other industries.

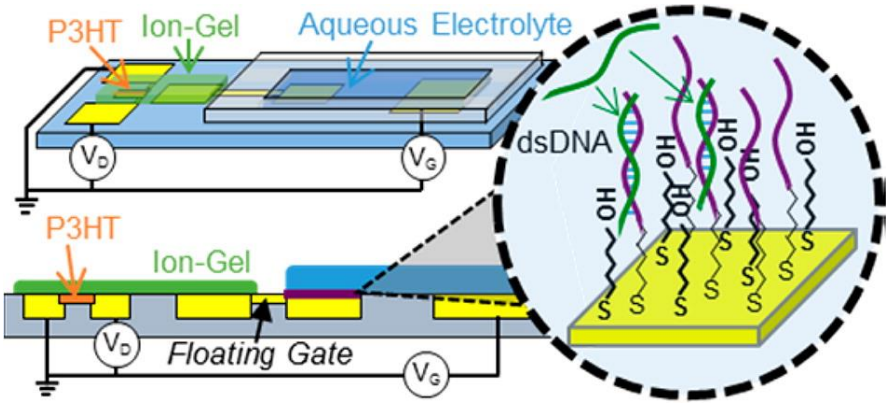


Figure 3.7. Biosensor application based on EGT and floating gate for sensing of bio-active molecules.[4] Reproduced with permission from Reference 4.

3.7 Dynamic Performance

EGTs have shown great quasi-static performance. However, their dynamic performance does not match the predicted values from their materials properties. One approach is to look at the semiconductor channel and see how fast a charge carrier can travel the channel length, Equation 4.4.[85]

$$f_{switching} \approx \frac{\mu V_D}{2\pi L^2} \tag{4.4}$$

Where the $f_{switching}$ is the switching frequency which is 1 Mhz for a semiconductor with mobility of 1 cm^2/Vs and printing resolution of 10 µm at 1 V. The other approach is to see how fast ions in the ion gel can make the EDL and open/close the semiconductor channel which is the gel $R_{ion\ gel}C_{ion\ gel}$ time constant. This is 0.1 µs for the SEAS/EMI TFSA (1:9 w/w) ion gel system. In principle, EGTs should be able to run at MHz.[3]

3.7.1 Computing power and high frequency applications

The need for dynamic performance becomes clear when computational power is required, and huge amounts of data needs to be processed in a short period of time. Applications where this is necessary are in antennae or displays where higher frequencies translate to higher resolutions, larger displays, and higher signal qualities.[12] In order to facilitate the internet of things (IoT), foldable displays, wearable electronics, and many other applications of flexible electronics, switching frequencies of 100 kHz to GHz are required.

3.8 Challenges for electrolyte-gated transistors

Considering all the aspects of EGTs including low-operating voltage, great electrical properties, reproducibility, and flexibility, EGTs are a great candidate for flexible/printed electronics applications. However, previous reports of EGTs to this thesis were limited to 5 kHz.[86] The main focus of this thesis is to improve the dynamic performance of EGTs. Also, this thesis tries to improve the quasi-static performances to further improve the dynamic performance and push the limits of EGTs. The quasi-static performance improvement also paves the way for better biosensing with improved limit of detections for sensors.

Chapter 4 Experimental Methods: Device Fabrication and Characterization

This chapter outlines the device structure, fabrication, and experimental techniques used in this dissertation project. Specific experimental details in sample preparations and measurements are described in the respective sections of the following chapters.

5.1 ZnO atomic layer deposition:

ZnO films were grown on clean SiO2/*p*-Si substrates using an ALD system (Savannah Series, Cambridge Nano Tech) with diethylzinc (DEZ) and water vapor as precursors which undergo the following reaction mechanism:[87]

$$Zn(C2H5)2* + H2O(g) \longrightarrow ZnO* + 2C2H6(g) \qquad \text{Equation 5.1}$$

where $*$ denotes a surface species. Since this reaction is quite exothermic, ZnO film can be grown at relatively low temperatures in the range of 100−200 °C. The film growth condition used in this work is as follows:

ALD Film Growth Procedure

1. Clean up a SiO2/*p*-Si wafer, on which the ZnO film is to be deposited, with isopropyl alcohol and dry it.
2. Load the wafer in the ALD chamber and pump down the chamber.
3. Set the temperature of the chamber at 235 °C and wait until the temperature is stabilized.
4. Set the flow rate of the carrier gas (N2) to 20 sccm and wait for 60 sec.
5. Pulse water vapor for 15 ms and wait for 5 sec.

6. Pulse DEZ for 15 ms and wait for 5 sec.

7. Repeat step 5 and 6 for desired number of cycles.

8. Unload the wafer from the chamber.

The thickness of the ZnO films was measured using a variable angle spectroscopic ellipsometer (VASE, J.A. Woollam) with monochromatic polarized light (500-1100 nm in wavelength). The obtained data was fitted to the Cauchy model,84 which showed the growth rate of ZnO films at the given condition was observed to be ~1.32 Å per cycle. We used the samples with a 50-nm-thick ZnO film to fabricate electrolyte-gated transistors. Before device fabrication, the 50 nm sample was annealed in N2 at 300 ^{o}C and in O2 at 400 ^{o}C each for 15 min in a rapid thermal annealer (RTP-600S, Modular Process Technology). We observed no changes in thickness after the annealing processes.

Patterning ZnO. The ZnO films on the substrates were patterned into a rectangular shape via photolithography. After preheating the samples at 105 ^{o}C for 1 min, the photoresist (Microposit S1813, Dow Electronic Materials) was spin-coated onto the wafer at 3000 rpm for 30 s. After soft baking at 105 °C for 1 min, we exposed the wafer to UV light (12 mW/cm^2) for 5 s through a photomask using contact mask aligner (MA6, SUSS MicroTec Inc.). The wafer was then baked at 105 °C for 1 min, developed in Shipley 351:H2O=1:5 (v/v) solution for 20 s, and thoroughly rinsed with deionized water. The exposed ZnO area was removed by wet etching with HCl solution (3% v/v)

5.2 Integration of Metal Contacts and Passivation Layers

Metal contacts and passivation layers are integrated on the prepared samples (i.e., the SiO2/p-Si substrates with the ZnO films on top) through a series of photolithography processes followed by etching or deposition steps[87–90] To kill the parasitic capacitance in

chapter 7 and 8, the source/drain electrode deposition was followed by SiO_2 deposition. All the depositions were done in e-beam thermal evaporator and patterned through lift-off using Shipley photo-resist 1800 series.

For organic semiconductor, the electrodes were deposited first. For printed electrodes, the fabrication is explained in the Chapter 7 thoroughly.

5.3 Electrical characterization

The electrical measurements of EGTs are carried out in a glovebox filled with N2. Transistor *I-V* measurements are taken using a variety of Keithley source-measure units (SMUs) and multimeters (236, 237, 6517A, 2612) and an Agilent B1500A semiconductor parameter analyzer (C_s-R_s configuration) in combination with a motorized probe station in a N_2-filled glovebox and a Desert Cryogenics (Lakeshore CPX-VF) vacuum probe station, respectively. For the dynamic performance, an Agilent 33500B waveform generator generated the input signal for inverters and a Tektronix TDS1002B digital oscilloscope was used to measure dynamic output voltage.

For the dynamic performance it is noteworthy that the internal resistance of the scope is 1 MΩ which is good for transistor measurements with resistivity of $\leq$10 kΩ in order to have error $\leq$ 1%. There are probes of 10X and 100X which increase the scope resistance in series by the same factor and can be used for more resistive transistors.

Chapter 5 Parasitic Capacitance Effect on Dynamic Performance of Aerosol-Jet-Printed Sub 2 V Poly (3-hexylthiophene) Electrolyte-Gated Transistors

This work has been published as F. Zare Bidoky and C. D. Frisbie, "Parasitic Capacitance Effect on Dynamic Performance of Aerosol-Jet-Printed Sub 2 V Poly (3-hexylthiophene) Electrolyte-Gated Transistors", *ACS Appl. Mater. Interfaces*, **2016**, *8 (40)*, pp 27012–27017. Reproduced with permission from the publisher.

5.1 Introduction:

Electrolyte-gated transistors (EGTs, Figure 5.1) have favorable characteristics for printed electronics, such as solution processability, low-voltage switching,[91,92] and relaxed layer-to-layer alignment requirements.[93,94] Consequently, they are being developed for applications in strain sensors,[95] biosensors,[96–102] printed circuitry,[103–106] e-textiles,[107,108] and antennas.[109] EGTs can, in principle, operate at speeds higher than 1 MHz, but currently are known to operate only at a few kHz with polymer semiconductors.[10,104] As we demonstrate here, the limitations are not due to intrinsic material properties but rather parasitic effects.

The crucial aspect of EGTs is the use of electrolytes, such as an ion gel dielectric, as a high capacitance gate insulator.[94] Ion gels are mixtures of an ionic liquid such as 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMI][TFSI]) and a triblock copolymer matrix material such as poly(styrene-*b*-methyl methacrylate-*b*-styrene) (PS-PMMA-PS).[94] Sandwiched between electrodes, these materials (and other electrolytes)

exhibit very high specific capacitances of order 10 μF/cm^2, due to the formation of nanometer-thick electrical double layers at the gel/electrode interfaces. When employed as gate dielectrics in EGTs, the high capacitance of ion gels provides devices that can be switched on and off with very low gate voltages, typically < 2V, which is an advantage for printed circuits that are powered by thin film batteries.

Here we examine dynamic performance of aerosol-jet printed, top-gated EGT inverters featuring a poly(3-hexylthiophene) (P3HT) channel, an ion gel dielectric and a poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) gate in series with a 100 ± 25 kΩ PEDOT:PSS resistor. Figure 5.1 shows the structure for the resistor-loaded EGT inverter. To fabricate this structure, the P3HT, ion gel, and PEDOT:PSS were aerosol-jet printed on conventionally microfabricated gold source and drain electrodes and contact pads.

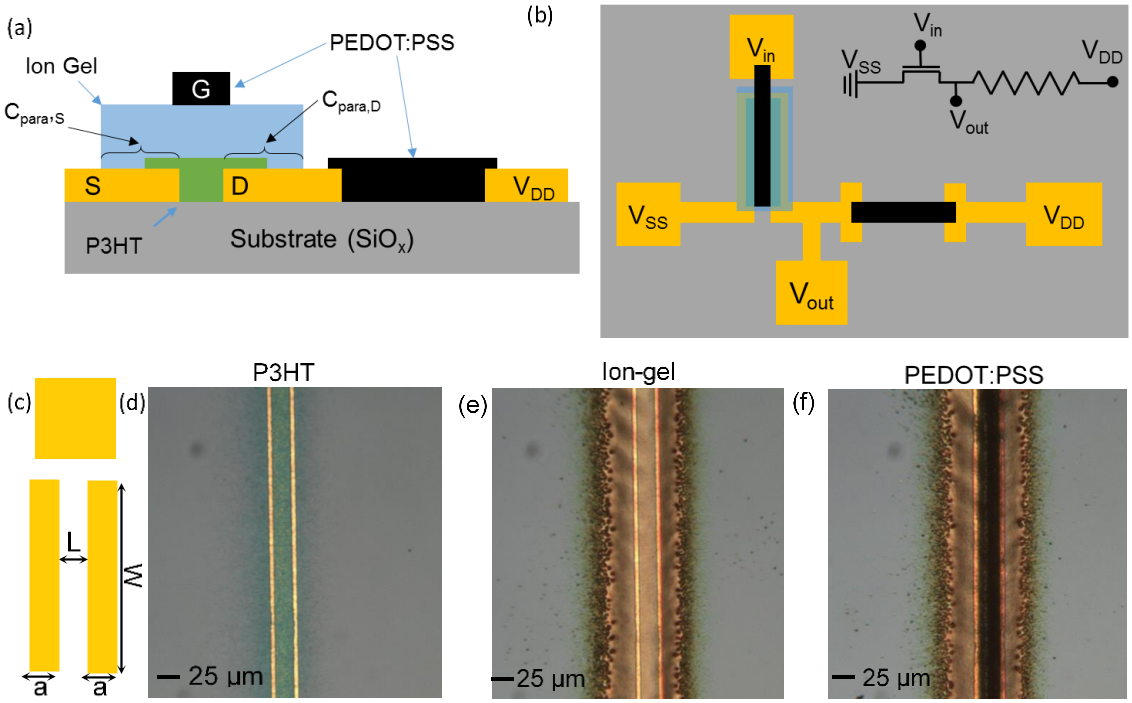


Figure 5.1. Aerosol-jet printed inverter. (a) and (b) Side and top view of a resistor-loaded EGT inverter with a P3HT semiconductor channel and PEDOT:PSS resistor. The electrodes were patterned with photolithography on a Si/SiO_2 (300 nm) wafer. The other

layers were deposited by aerosol-jet printing. The parasitic capacitance is shown as the overlap of ion gel on the source/drain electrodes. c) Geometry of the channel and electrodes. The channel length (L), the channel width (W), and the electrode width (a_D) are shown. Identical source/drain electrode areas are used unless otherwise specified. d) The deposited P3HT film with 30 nm thickness. e) Printed ion-gel on top of P3HT film, and f) Aerosol-jet printed PEDOT:PSS on the ion-gel/P3HT film as a gate. The channel length is 25 µm and the electrode width is 5 µm.

P-type P3HT EGTs investigated here display hole mobilities (μ) of ~1 cm^2/Vs.[10,94] Thus, for a 2.5 µm channel length, the switching frequency (f_{switch}) for a P3HT EGT should be on the order of 10 MHz, as shown by Equation (5.1).

$$f_{switch} = \mu \frac{V_D}{L^2} \tag{5.1}$$

where V_D is the drain voltage and L is the channel length. However, it has been shown that P3HT EGTs do not achieve this switching speed.[10] Equation 5.1 assumes that the limiting step in switching the EGT is transport of holes in the P3HT channel (i.e., transport of holes into P3HT between source and drain electrodes upon the application of gate voltage). Nonetheless, other factors can also limit the speed of an EGT (or any thin film transistor) and it has been claimed that parasitic capacitance is a major limiting factor.[104] Parasitic capacitance refers to capacitive coupling of the gate electrode to the source and drain, Figure 5.1a, which is in parallel with capacitive coupling to the semiconductor channel, and it is undesirable because it degrades dynamic performance.[110] Here we systematically investigate the role of parasitic capacitance in aerosol-jet printed EGT inverters.

5.2 Results and Discussion:

Figures 5.2a and 5.2b show the quasi-static response of a P3HT EGT with a fixed channel aspect ratio (width/length or W/L) of 500 µm/25 µm. The slightly negative threshold voltage, 10^6 ON/OFF ratio, and carrier mobility (µ) of 1 cm^2/Vs[94,111] are typical

characteristics of the transistor.[94] Figure 5.2c displays the quasi-static response of a resistor loaded P3HT EGT inverter. The inverter step can be seen for different bias voltages in which V_{out}reaches 98% of V_{DD}.

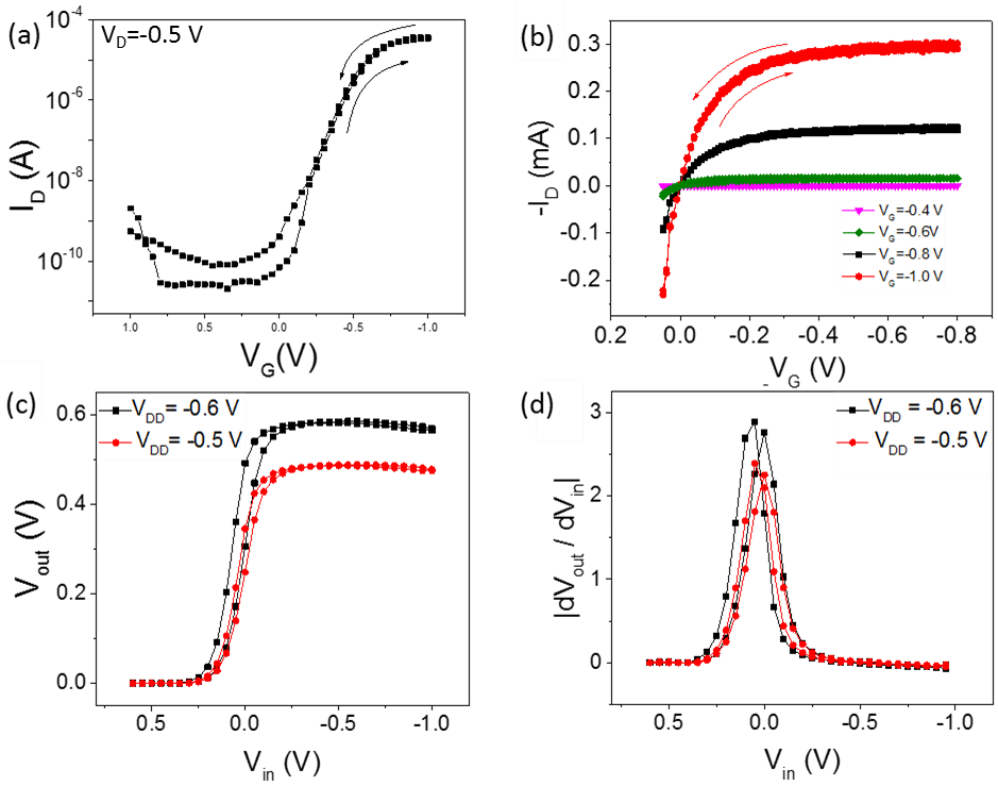


Figure 5.2. Quasi-static measurement for a P3HT EGT with W=500 µm, L=25 µm, and a_S=a_D=a=5 µm. a) Aerosol-jet printed P3HT EGT transfer curve at V_D= -0.5 V with V_t= -0.34 V, µ=1.2 cm^2/Vs, ON/OFF=5 × 10^5, OFF current of 100 pA. b) Output characteristic of the P3HT EGT. c) The inverter step and d) inverter quasi-static gain for the same device which shows V_{out}/V_{DD}=0.98. The sweep rate is 50 mV/s.

Figure 5.3a displays the low frequency (10 Hz) quasi-dynamic measurement of a P3HT EGT with channel dimensions of W= 50 µm, L= 2.5 µm, and a=5 µm in which a square-wave voltage is applied to the input (gate) electrode and the output voltage at the drain electrode is measured. The behavior is essentially ideal in that the input signal is nearly perfectly inverted. Figure 3b exhibits the response at 5 kHz which reveals noticeable

non-idealities; the output signal slightly lags the input and there is a voltage overshoot (spike) every time the input voltage changes.

Figure 5.3c displays the response at 10 kHz where non-idealities are more significant. Referring to Figure 3c, the non-ideal or spike time (t_{spike}) is defined as the time required for the output response (V_{out}) to match the ideal response value (V_{ideal}) in a given period, whereas the ideal time (t_{ideal}) is the time that the output response is at the expected ideal value in the period. The spike height (V_{spike}) is the voltage overshoot from the ideal output response value ($V_{spike} = Max|V_{out} - V_{ideal}|$). Increasing the input frequency further increases the deviation from the ideal output response. We define the experimental cut-off frequency ($f_{cut\text{-}off}$) as the frequency at which the ideal and non-ideal output responses are equal, $t_{spike} = t_{ideal}$ (see Supporting Information for conversion between different terminologies of inverter working frequencies, Figure S1). Figures 3c and S4 show that the resistor-loaded inverter has $f_{cut\text{-}off}$ ~10 kHz, which is significantly smaller than the expected cut-off frequency from Equation (5.1).

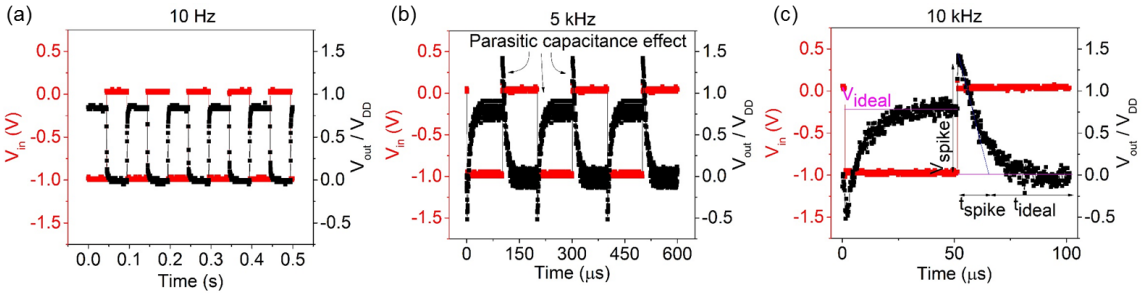


Figure 5.3. Dynamic performance for an EGT with W =50 μm, L=2.5 μm, and $a_S = a_D = a$ =5 μm at V_{DD}= -1V. a) The low frequency quasi-dynamic response to 10 Hz square-wave input, with $\frac{V_{out}}{V_{DD}} = 0.9$. b) The dynamic response to 5 kHz square-wave input with $\frac{V_{out}}{V_{DD}} = 0.87$. c) The dynamic response at 10 kHz. The spike height (V_{spike}), spike time (t_{spike}), and ideal response time (t_{ideal}) are shown on the figure. At cut-off frequency

($f_{cut-off}$) the spike time and ideal response output time are equal. The spike time and normalized spike height ($\frac{V_{spike}}{V_{DD}}$) here are 20.9 μs and 1.42.

Note that Equation (5.1) predicts that cut-off frequency ($f_{cut\text{-}off}$) is independent of channel width (W). However, our systematic measurements reveal completely different scaling. Notably, Figures 5.4a and 5.4b show that the cut-off frequency ($f_{cut\text{-}off}$) is independent of channel length (L) and directly proportional to $1/W$; $f_{cut\text{-}off}$ increases with decreasing the channel width. Suspecting the importance of gate-source/drain overlap, we measured the dependence of $f_{cut\text{-}off}$ on source/drain electrode width, a. Figure 5.4c reveals that $f_{cut-off} \propto 1/a$, i.e. smaller electrodes result in faster devices. Consequently, the device dynamic performance is not limited by channel length or transport properties, but rather by the electrode area ($A = W \times a$).

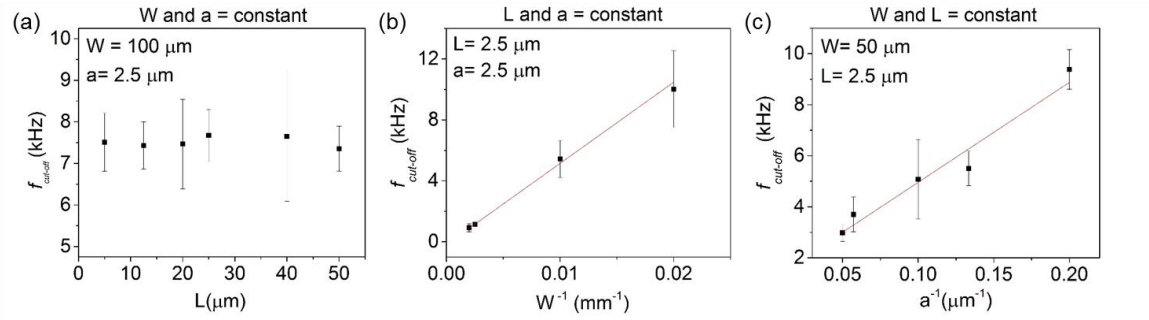


Figure 5.4. Geometrical dependence of cut-off frequency ($f_{cut-off}$). a) L dependence of $f_{cut\text{-}off}$ with W and a held constant. b) W dependence of $f_{cut\text{-}off}$ with L and a held constant. c) a dependence of $f_{cut\text{-}off}$ with W and L held constant. The error bars represent one standard deviation.

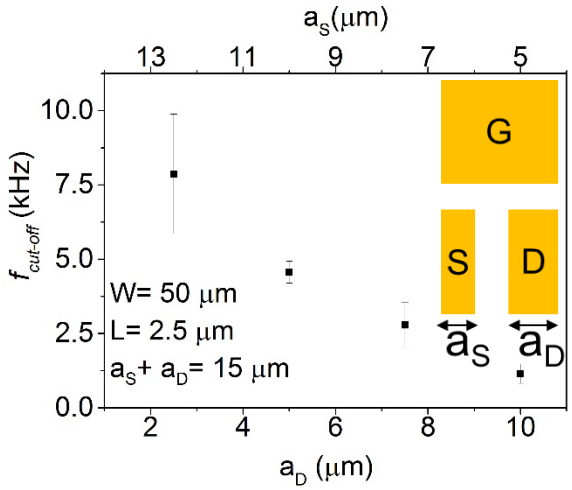


Figure 5.5. $f_{cut\text{-}off}$ dependence on source and drain electrode width. The inset shows a top view of geometry of the channel and electrodes including the source width (a_S), and the drain width (a_D). The channel width (W), the channel length (L), and the total electrode width ($a_D + a_S = a_T$) are constant at 50 µm, 2.5 µm, and 15 µm, respectively. The drain electrode width (a_D) is varying between 2.5 µm to 12.5 µm. It shows the higher cut-off frequencies ($f_{cut-off}$) for the smaller drain electrode widths (a_D) with the larger source electrode widths (a_S). The error bars represent one standard deviation.

As shown in Figure 5.1, the EGT source electrode is grounded and the output response is measured at the (floating) drain electrode. With the output voltage measured at the drain electrode, the drain electrode area is expected to show a higher impact on $f_{cut\text{-}off}$ compared to the source electrode area. Figure 5.5 shows the dependence of $f_{cut\text{-}off}$ on the drain electrode area ($A_D = W \times a_D$) in comparison to the source electrode area ($A_S = W \times a_S$). For a constant total electrode width ($a_D + a_S = a_T$) of 15 µm, Figure 5 exhibits a clear frequency dependence on the drain electrode area; the device with the smallest drain electrode width is the fastest. If the total parasitic capacitance ($A_T = A_D + A_S$) was the key variable, a flat line in Figure 5.5 would have been expected.

With a good general understanding of the cause for reduced switching frequency, we can turn attention to quantitative analysis. As derived in the Supporting Information (Figure A2.3 and Equations A2.1-8), for a P3HT-EGT operating under parasitic

capacitance limitations, the voltage spike due to a square wave input is expected to be independent of frequency, but directly proportional to the abruptness of the voltage step ($\Delta V_{GD}/\tau$), i.e.,

$$V_{spike} \approx R_L C_{para,D} \frac{\Delta V_{GD}}{\tau} \tag{5.2}$$

where R_L is the inverter load resistance, $C_{\text{para,D}}$ is the total parasitic capacitance of the drain ($C_{para,D} = C_{ion\ gel} \times A_D$). $R_L C_{para,D}$ is the characteristic relaxation time of the inverter, and thus,

$$f_{cut-off} \approx \frac{1}{12 R_L C_{para,D}} \tag{5.3}$$

where the factor of 1/12 is defined in the Supporting Information (Figure A2.4 and Equations A2.9-A2.11).

Considering the specific capacitance of the ion gel in contact with P3HT ($C_{ion\ gel}$ ~10-100 μF/cm^2), $C_{para,D} \sim 1.25 - 12.5 \times 10^{-11}$F,[112] and $\Delta V_{GD}/\tau$ = 2 x 10^7 V/s, then V_{spike}= 1.25 V, which is roughly consistent with the measured value of 1.4 V. The calculated $R_L C_{para,D}$ is 1.25-12.5 μs, giving $f_{cut\text{-}off}$= 6.7-67 kHz which brackets the measured value of 10 kHz. It should be noted from previous work that the ion gel specific capacitance is time dependent,[113] which is why we estimate the value is between 10 μF/cm^2 and 100 μF/cm^2.

As previously mentioned, the important role of the parasitic capacitance suggests that the drain electrode area should be minimized. The drain can be made narrower (smaller a_D), but also shorter (smaller W). Thus, we anticipate that EGTs with small a_D and small W will have higher cut-off frequencies (Figure 5.4b). However, W also impacts the channel resistance R_{EGT} ($R_{EGT} \propto L/W$) and thus W cannot be shrunk arbitrarily without an adverse

effect on the inverter performance. Specifically, smaller *W* at a fixed *L* means larger R_{EGT} in the ON-state and thus smaller "maximum voltage output" ($\frac{V_{out}}{V_{DD}} = \frac{R_L}{R_L+R_{EGT}}$) for the inverter output. To maintain the maximum voltage output, smaller *L* or larger R_L values are required, yet larger R_L results in a higher spike, (Equation 5.2) and lower $f_{cut\text{-}off}$ (Equation 5.3). That is, there is a trade-off between operating frequency and inverter output.

This trade-off is quantified by the "dynamic range-bandwidth" (DBW) (similar to gain bandwidth) which is defined as the product of the f_{cutoff} and the maximum voltage output at the cut-off frequency (i.e., DBW = f_{cutoff} x V_{out}/V_{DD} (@ $f_{cut\text{-}off}$)). V_{out}/V_{DD} and f_{cutoff} both depend on *W*. Increasing or decreasing *W* does not affect the DBW. However, the electrode width only affects $f_{cut\text{-}off}$, and *L* only affects the maximum voltage output. Thus, to achieve highest cut-off frequency, maximum voltage output and DBW, the electrode width (a_D) and channel length (*L)* need to be minimized simultaneously (Figures 4a, 4c and S2). The fastest EGT fabricated is observed in Figure 3 (also see Figure S5), with an aspect ratio of $\frac{50\ \mu m}{2.5\ \mu m}$ and electrode width of 2.5 µm. Here, R_{EGT} for the ON state and *W/L=20* is ~10 kΩ, (Figure 2a), and the printed R_L is 100±25 kΩ which lead to maximum voltage output of 0.9. The $f_{cut\text{-}off}$ is 11 kHz and the DBW is 10 kHz.

Parameters other than the parasitic capacitance like ion mass transfer in the ion gel matrix and in P3HT can become important limiting factors for frequencies higher than 10 – 20 kHz.

5.3 Conclusion:

In conclusion, the effect of different geometrical parameters on dynamic performance of P3HT EGT inverters was systematically studied. The electrode area and the parasitic capacitance are shown as primary factors limiting the speed of printed P3HT EGTs. By minimizing the electrode area, we demonstrated an EGT invertor operating at 10 kHz. It was shown that to optimize the dynamic performance, the electrode area should be minimized while maximizing the EGT *W/L* ratio. Therefore, higher resolution for the source/drain electrode width and channel length is required to increase the cut-off frequency. These considerations are valuable to ongoing efforts to improve the dynamic performance of low voltage, printed EGTs.

5.4 Experimental Section:

Materials. P3HT was purchased from Sigma-Aldrich and 1mg/1ml solution of P3HT in chloroform was made by stirring overnight on a hotplate at 55^{o}C. To produce longer-lived aerosols, terpineol was added to the P3HT solution prior to printing (10% volume). In order to make the ion gel, a solution with the mass ratio of 1/9/90 for PS-PMMA-PS/[EMI][TFSI]/ethyl acetate was made. The PS-PMMA-PS polymer was synthesized in house using a previously reported procedure.[72] [EMI][TFSI] ionic liquid was purchased from EMD Chemicals and stored in inert atmosphere. For the PEDOT:PSS ink, PH1000 was purchased from Heraeus, and 6% volume ethylene glycol was added to the ink to enhance the conductivity. <100> orientation 500 μm thick silicon wafer substrates with 300 nm thermal oxide were purchased from Silicon Valley.

Device Fabrication. Gold contacts were patterned on the Si/SiO_2 wafers using photolithography followed by e-beam/thermal evaporation of Cr(2nm)/Au(28nm) metal

layers. Then the organic semiconductor (P3HT), gate dielectric (ion gel) and gate contact (PEDOT:PSS) were sequentially printed with an Aerosol Jet Printer (AJ 100, Optomec Inc) (Figure 1d, e and f). A 150 μm diameter nozzle was used to print the P3HT and ion gel layers and a 100 μm nozzle for PEDOT:PSS. The sheath/feed gas flow rate (measured in standard cubic centimeter per minutes) for P3HT, ion gel, and PEDOT:PSS were 32/12, 28/8 and 17/12, respectively. A 1 cm long line of PEDOT:PSS was also printed as the 100 kΩ resistor.

Electrical Characterization. To avoid humidity effects on the devices, all the measurements were accomplished in a glove box under N_2 ambient. For the quasi-static electrical characterization of EGTs and inverters, two source meters (Keithley 236 & 237) were connected to the source/drain/output electrodes and an electrometer (Keithley 6517A) to the gate/input electrode. Agilent 33512B waveform generator was used to generate the input signal for inverters in the quasi-dynamic measurements. The quasi-dynamic responses of inverters were acquired with a Tektronix TDS3014C digital oscilloscope.

Supporting Information. Cut-off frequency terminology, aspect ratio (*W/L*) effect on dynamic performance, equivalent circuit analysis, equation derivations, t_{spike}, V_{spike}, *and* $f_{cut\text{-}off}$ calculation, and best optimized device dynamic performance are included in a separate Supporting Information document. This material is available free of charge via the Internet at http://pubs.acs.org and also presented as Appendix 2 of this thesis.

Chapter 6 Printed, 1 V Electrolyte-Gated Transistors Based on Poly(3-hexylthiophene) Operating at >10 kHz on Plastic

This work has been published as F. Zare Bidoky, W. J. Hyun, D. Song, and C. D. Frisbie, "Printed, 1 V Electrolyte-Gated Transistors Based on Poly(3-hexylthiophene) Operating at >10 kHz on Plastic", *Appl. Phys. Lett.*, **2018**, *113*, 053301. Reproduced with permission from the publisher.

6.1 Introduction:

Electrolyte-gated transistors (EGTs)[94] have applications in biosensors,[114–122] light emitting devices,[123] logic gates,[124,125] tunable antennae,[126] and studies of fundamental semiconductor physics.[127–129] EGTs characteristically have low-operating voltages (<2 V),[10] large width normalized transconductances (~400 S m^{-1}),[8,80,130] large ON/OFF current ratios (10^6), and low contact resistances (~1-10 Ω cm)[81] by virtue of the ultra-high capacitance gating of the semiconductor channel (SC).[127] The gate electrolyte capacitance, typically 10-100 μF/cm^2 depending on whether the mechanism is electrochemical or double layer charging, is $10^3 – 10^4$ times higher than traditional polymeric dielectrics which leads to the favorable characteristics mentioned above.[131–133] A variety of different electrolytes may be used for EGTs, but ionic liquids are popular due to their large specific capacitance, high ionic conductivity, wide electrochemical stability windows, and low-volatility.[134] To incorporate ionic liquids into solid state-devices, polymers may be added to create solid films known as ion gels.[2,70] Ion gels maintain most of the electrical properties of ionic liquids and yet have the characteristics of a rubbery solid[2] and they are physically,

chemically, and electrochemically stable, compatible with different semiconductors, and easy to print from common solvents. [3,74,94]

For applications such as sensing and wearable electronics, transistors with switching speeds of at least a few kHz at low-operating voltage are required.[135,136] Previously, we have reported robust EGTs employing poly(3-hexylthiophene) (P3HT) as the p-type channel material.[6,10,137,138] Of the various channel materials we have incorporated in EGTs, P3HT devices are exceptional in terms of stability and overall device performance.[6] Figure A3.1 depicts the gating mechanism in P3HT EGTs in which the P3HT film is electrochemically doped and ions penetrate the film. The kinetics of electrochemical doping can in principle control dynamic switching times. We have intentionally used P3HT films only 100 nm thick as we have demonstrated in previous work that films of this thickness yield hysteresis free *I-V* characteristics [94,137,139–141]. Rather than ion penetration, we have found that parasitic capacitance typically limits the switching speed to less than 1 kHz, Figures 6.1a and b.[138] The parasitic capacitance arises from overlap of the ion gel with the P3HT-coated source and drain electrodes, Figure 6.1a. [138,142] Electric double layer (EDL) formation and electrochemical doping on the electrodes results in a dynamic capacitance of ~100 nF for an EGT with source and drain electrodes 500 µm long and 15 µm wide, as reported in Figure A3.2.[137] This parasitic capacitance is greater than the dynamic channel capacitance (~1 nF for a 25 µm × 500 µm channel) thus limiting the cut-off frequency. Parasitic capacitance is expected to be an even larger problem for printed EGTs, because the electrode widths are typically wider than 20 µm due to limited resolution associated with inkjet, aerosol-jet, or screen printing.[143]

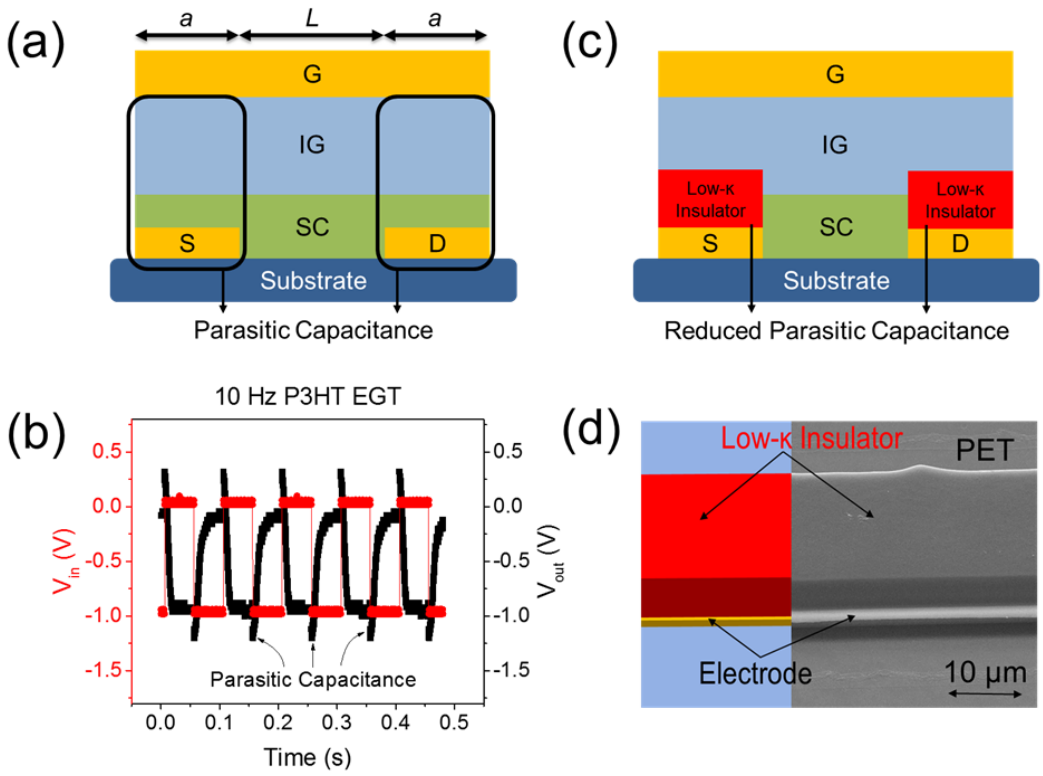


Figure 6.1. Device architecture and parasitic effects. (a) Top-gated P3HT EGT with parasitic capacitance emphasized. Device dimensions L and a are defined as shown. W is the channel width into the page. (b) The unwanted parasitic capacitance limits the dynamic performance of a top-gated EGT (W×(L+2a) = 500 μm×(25 μm + 2×15 μm)) with spikes (voltage overshoots) and delay, (c) Target architecture for fast switching P3HT EGT. Thick polymeric low-κ insulator layer with 1000 times lower capacitance[144] than the ion gel covers the source and drain electrodes to prevent EDL formation. (d) Tilted SEM image of the covered electrode on PET.

Here we demonstrate an approach for printing P3HT EGTs with minimal parasitic capacitance. Our strategy is to cover the top surfaces of the source and drain electrodes with a dielectric that dramatically reduces the capacitance associated with the ion gel/metal interfaces, Figure 6.1c.[144] The semiconductor remains in contact with the electrode sidewalls. Following this approach, we achieve operating frequencies >10 kHz for printed P3HT EGTs.

6.2 Results and Discussion:

The ion gel used here consists of a triblock copolymer, polystyrene-b-poly(ethyl acrylate)-b-polystyrene (SEAS)[3] and an ionic liquid, 1-ethyl-3-methylimidazolium

bis(trifluoromethylsulfonyl)imide ([EMI][TFSI]). The SEAS/[EMI][TFSI] ion gel system has excellent ionic conductivity (~10^{-2} S/cm), specific capacitance (1-100 μF/cm^2), and Young's modulus (10 kPa) at only 10 wt % of the added polymer. Fig. S3 demonstrates the fabrication scheme for parasitic capacitance-reduced, printed P3HT EGTs. The detailed experimental conditions are described in Appendix 3. First, the resolution (i.e., narrowness) of the source and drain electrodes was enhanced by combining photopatterning with capillarity-assisted printing.[145] This is a variation of the imprint lithography plus capillarity-assisted printing that we have reported previously, termed SCALE (self-aligned capillarity-assisted lithography for electronics).[51,146] As shown in Figures A3.3a and b we exposed photoresist coated on the polyester substrate to UV light through a conventional photomask, followed by development to produce 15 μm wide capillary channels connected to large (400 μm diameter) reservoirs. An ink jet printer was then used to deliver Ag ink[17] to the reservoirs and capillarity drew the ink into the capillary channels, coating them with nm thick Ag metal, Figure A3.3c. These channels are the source and drain electrodes. The entire substrate was immersed in an electroless Cu-plating solution to build up a 500 nm thick layer of Cu on the Ag seed layers to fully form the source and drain electrodes. The Cu-plating solution was highly basic and also removed the photoresist. Thus, after Cu-plating, raised metal electrodes, clear of photoresist, remained on the substrates, Figure A3.3d. Next, the whole substrate was covered with positive tone photoresist and the backside was exposed to UV light, following the "backside-exposure strategy" in Figure A3.3e.[46] The electrodes on the front blocked the UV light so the photoresist was exposed everywhere except on the electrodes. The backside exposure method has been widely used in self-aligned fabrication of TFTs usually to pattern the gate electrode and minimize the

overlap with the source and drain electrodes. [47–50] The method here is rather different in that the capacitance is minimized by adding a thick photoresist layer over the source and drain electrodes because the dominant parasitic capacitance comes from electrolyte contact with these electrodes. Figure A3.3f shows raised electrodes covered by photoresist after development. Then, aerosol-jet printing (AJP) was employed to deposit the next layers of functional materials (P3HT, ion gel, and gate material PEDOT:PSS) on top of the channel to form fully-printed, top-gated EGTs (Figures A3.3g-i).

Figure A3.4a displays an optical micrograph of the empty capillary channels in the photoresist before Ag ink delivery. In the capillary channel design, smooth U-turns were implemented in order to minimize ink overflow out of the capillary channel caused by ink momentum at the turns. Figure A3.4b shows the SEM image of a focused ion beam (FIB) cross-section of the Ag film in the capillary channel. Figure A3.4c is the SEM FIB cross-section of the raised metal electrode on PET indicating uniform continuous metal after 2 min of Cu-plating and photoresist removal. More complex geometries like spirals with a resolution of 5 μm can be made by this method that have potential applications including antenna fabrication, Figure A3.4d.[152] Figure 6.1d is the tilted SEM image of the covered electrode after UV backside-exposure and photoresist development. The SEM and backscattered SEM FIB cross section of the covered electrode are depicted in Figure A3.5, revealing uniform continuous metal and photoresist after the exposed photoresist has been removed. Figure A3.6 shows the topographic profile of the covered electrode.

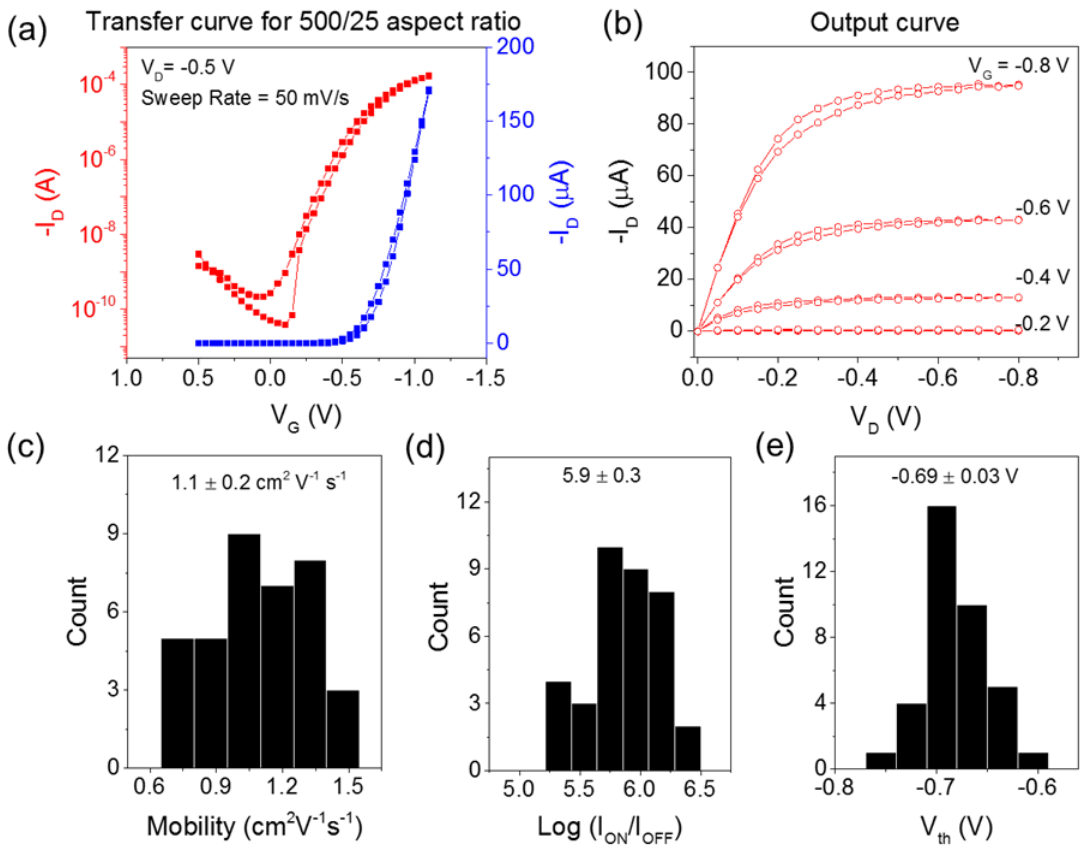


Figure 6.2. Performance metrics on plastic. Printed poly(3-hexylthiophene) EGT (W/L=500 µm/25 µm) (a) transfer and (b) output curves. Histograms of device metrics for 37 devices, including (c) the charge carrier mobility (μ), (d) ON/OFF-current ratio (I_{ON}/I_{OFF}), (e) threshold voltage (V_{th}).

The quasi-static electrical characterization of the P3HT EGT with covered electrodes is visible in Figure 6.2. The transfer curve (I_D-V_G) for the p-type semiconductor P3HT is plotted in Figure 6.2a. The drain current, I_D, increases with gate voltage, V_G, as the gate voltage is swept from 0.5 V to -1.1 V at V_D = -0.5 V. The transfer curve shows a V_{th} of -0.7 V, an I_{ON}/I_{OFF} ratio of 10^6, and little hysteresis between forward and backward sweeps. The quasi-static output characteristics (I_D-V_D) are displayed in Figure 6.2b. Figure 6.2b shows a large increase in I_D with increased gating power and negligible hysteresis. From the increase in saturation I_D with V_G one can see that the current follows the expected square law ($I_D \propto (V_G - V_{th})^2$). The statistical distribution of μ, I_{ON}/I_{OFF}, and V_{th} for 37 working, printed P3HT EGTs (out of a total of 40) are plotted in Figures 6.2c-e,

respectively. The average differential field effect carrier mobility, μ, is 1.1 ± 0.2 $cm^2\ V^{-1}\ s^{-1}$, which is consistent with previously reported printed P3HT EGTs,[6,94,153–155] and is determined from Equation 6.1,[82]

$$\frac{\partial I_D}{\partial V_G} = \frac{W}{L}\, C_{ion\ gel}\, \mu\, V_D \tag{6.1}$$

where ion gel capacitance $C_{ion\ gel}$ is 63 μF cm^{-2} (at V_G = -1 V) from displacement current measurements, Figure A3.7, and the *W/L* ratio is 20. The log I_{ON}/I_{OFF} average is calculated based on Equation A3.1 and is 5.9 ± 0.3 over a 1 V change in the V_G. The average V_{th} is -0.69 ± 0.03 V reflecting the very narrow distribution in this parameter. Importantly, covering the electrode with low-κ dielectric decreased ON current only 30% while it reduced the parasitic capacitance by a couple orders of magnitude (see Figure A3.2).

Figures 6.3a and b show the dynamic performance for a printed, resistor-loaded P3HT EGT inverter working at 12.5 kHz. The average and best experimental cut-off frequencies[138] were measured to be 12.5 kHz and 26 kHz, respectively. The theoretical $f_{cut\text{-}off}$ is calculated based on Equation 6.2 derived by Klauk, et al for a sine wave input:[110,156,157]

$$f_{cut-off} = \frac{\mu}{1+\frac{\mu}{L}R_C\, WC_{ion\ gel}\left(V_G - V_{th} - \frac{V_D}{2}\right)} \frac{V_D}{2\pi L\left(L + L_{para,D} + L_{para,S}\right)} \tag{6.2}$$

where the contact resistance R_C is 10 Ω cm,[81] and the parasitic ion gel overlap lengths with source and drain, $L_{para,S}$ and $L_{para,D}$, are 0.6 μm measured from Figure A3.5. Equation 6.2 leads to $f_{cut\text{-}off}$ of 28 kHz, roughly consistent with the experimental results.

The absence of the spikes in the dynamic output supports the conclusion that the parasitic effect is significantly reduced. To further improve the device performance, higher mobilities are required and less electrochemical doping which suggests impermeable inorganic semiconductors would be great candidates.[132,158,159] Reducing device area while

maintaining constant *W/L* would also help with both reducing parasitic capacitance and decreasing channel carrier travel length.[110,155,160]

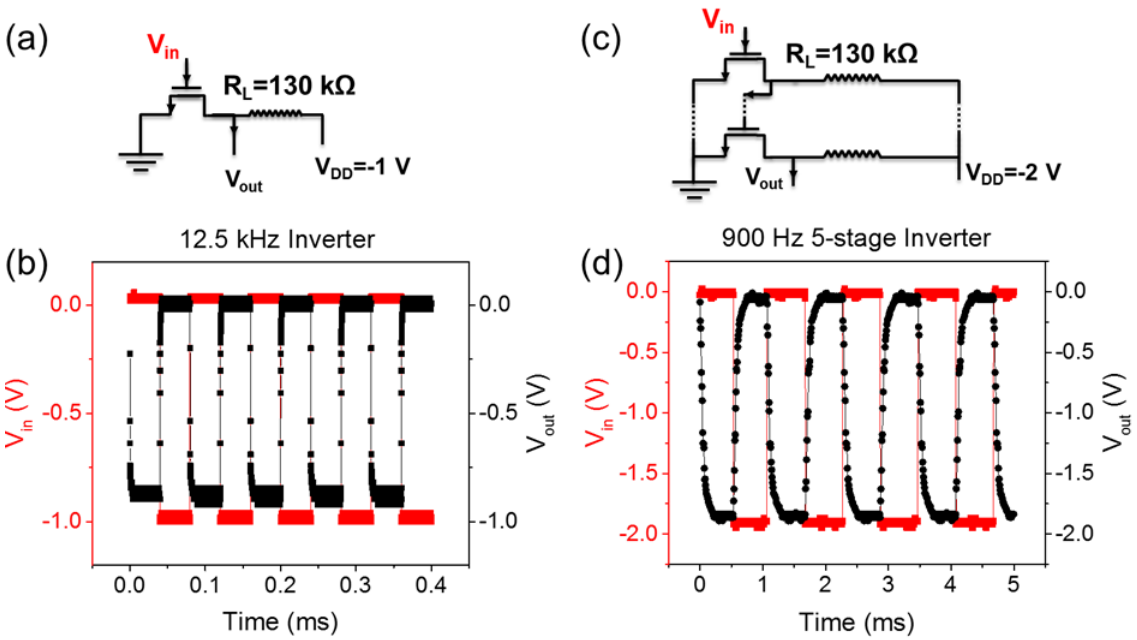


Figure 6.3. P3HT EGT dynamic performance. Resistor-loaded inverter (a) scheme and (b) output response curve for best device (*W/L*=500 µm/25 µm) at 12.5 kHz. Typical devices also switch at 12.5 kHz but the output waveform is somewhat less square. 5-stage resistor-loaded inverter (c) scheme and (d) output response curves at 900 Hz.

The high yields of the photolithography, inkjet and aerosol-jet printing steps combined with the yield of the Cu-plating process results in a total working device yield of 93% for the entire fabrication process (printing steps were not completed in a cleanroom). This yield is sufficient for building simple circuits. The scheme for a 5-stage inverter is shown in Figure 6.3c and the dynamic performance is evident in Figure 6.3d. The 900 Hz frequency is roughly consistent with expectations (2 kHz) based on the average performance of a single inverter.

6.3 Conclusion:

In conclusion, we have demonstrated here that systematic reduction of the source and drain contact area with the electrolyte increases the operating frequency of P3HT-

based EGTs by 10-fold. We have accomplished this by using a backside exposure strategy that is also compatible with printing techniques. While 10 kHz switching frequency has been achieved here, simple calculations suggest that by scaling down the footprint of the device, 100 kHz operation should be possible. Experiments to demonstrate this are underway.

See Appendix 3 for experimental details, device fabrication and characterization, images of raised metal electrodes patterns, backscattered electron microscopy, covered electrode profilometry, displacement current measurement, and log I_{ON}/I_{OFF} calculation.

Chapter 7 Sub-3 V ZnO Electrolyte-Gated Transistors and Circuits with Screen-Printed and Photo-Crosslinked Ion Gel Gate Dielectrics: New Routes to Improved Performance

This work has been accepted for publication as F. Zare Bidoky, B. Tang, R. Ma, K. S. Jochem, W. J. Hyun, D. Song, S. J. Koester, T. P. Lodge, and C. D. Frisbie, "Sub-3 V ZnO Electrolyte-Gated Transistors and Circuits with Screen-Printed and Photo-Crosslinked Ion Gel Gate Dielectrics: New Routes to Improved Performance", *Adv. Funct. Mater.*, **2019**, 1902028. Reproduced with permission from the publisher.

7.1 Introduction

Electrolyte-gated transistors (EGTs), including electric double layer transistors (EDLTs) and organic electrochemical transistors (OECTs), are being developed by a number of research groups for applications in sensing and printed electronics.[8,80,91,94,99,107,161–170] Attractive features of EGTs are their very high transconductances and low voltage characteristics, both of which derive from the huge specific capacitance of the electrolyte gate dielectrics that they employ, which varies from ~10 μF/cm^2 in the double layer operating regime to over 100 μF/cm^2 in the electrochemical regime.[12,94,127,171–177]

Applications of EGTs, with the exception of some types of sensing, require that these devices be integrated into circuits and thus there must be robust approaches for patterning all three materials: metals, semiconductors, and the solid-state electrolyte. The metal and semiconductor components can be patterned easily using photolithography, but

the solid-state electrolytes, which are often soft gel materials, present some challenges. Photolithographic patterning using conventional photoresists coated on top of gel electrolytes can be difficult because of the softness of the gel and poor solvent orthogonality between the gel electrolyte and the exposed (or unexposed) resist. Correspondingly, non-contact, nozzle-based printing techniques such as aerosol jet or ink jet printing have been employed extensively in the literature to pattern gel electrolytes, but these printing approaches often suffer from less than desirable spatial resolution and thickness control.[24,131] These techniques are also not standard in conventional clean rooms.

In this work our goal was to create discrete EGT devices and circuits entirely by conventional photolithography[178] and stenciling techniques. In parallel, we aimed to improve EGT switching times by minimizing parasitic capacitance effects,[148–151] which we have shown can dominate in EGTs,[138,179] and by employing high electron mobility ZnO semiconductor films grown by atomic layer deposition (ALD) in combination with short (10 μm) source-drain channel lengths. This work required the synthesis of an improved version of a photopatternable gel electrolyte, or ion gel, that we reported previously based on a cross-linkable triblock copolymer and a common ionic liquid.[3,180] We show here that these collective strategies have allowed us to fabricate photopatterned and stenciled EGT circuits operating with sub-3V supplies and inverter stage delays of close to 50 μs. Importantly, analysis of these results suggests that with further optimization, particularly with respect to the ion gel ionic conductance, stage delays could be shortened to the order of 1 μs, greatly expanding the spectrum of potential applications for EGT circuits.

7.2 Results and Discussion

Figure 7.1 shows the screen-printing and photo-crosslinking steps that we employed for ion gel patterning. A silicon stencil was fabricated from a thinned silicon wafer as described previously by Hyun, et al.[46] A custom-made stencil holder was fashioned from a 5-mm thick acrylic plate with an opening in the center to hold the silicon stencil; the holder was designed with the same dimensions as photomasks employed in a photolithography mask aligner. The stencil was attached to the holder and the combination was installed in the mask aligner in order to precisely align the stencil to the substrate electrode features. Upon completion of optical alignment, a controlled volume (1 mL) of cold ion gel ink (viscosity ~7 cP at 5 ˚C), with composition described below, was delivered to the surface of the stencil and a doctor blade was used to squeeze the ink through the stencil opening, Figure 7.1a, in a process that is thoroughly described in the Experimental section and in Supporting Information. After printing, the stenciled gel was crosslinked by exposure to 254 nm UV light for 3 min. The stencil was removed, and the aligned, crosslinked ion gel film on the substrate was compatible with further processing steps. This procedure produced ion gel films with thicknesses of 500-1000 nm and lateral dimensions set by the stencil as small as 10 μm, Figures 1b and 1c.

The ion gel ink was composed of a 1:9 weight ratio mixture of poly(styrene)-*b*-poly(ethylacrylate)-*b*-poly(styrene) triblock copolymer (SEAS) and the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMI TFSI) in ethyl acetate solvent.[70] Pendant photocrosslinkable azide ($-N_3$) functional groups were installed in the sidegroups along the polystyrene endblocks of the SEAS polymer following previously reported synthesis routes, as described in Supporting Information Figures A4.1 and

A4.2.[3,180] Figures 7.1d and 7.1e display the chemical structures of the ion gel components. UV exposure crosslinked the polymer, primarily within the polystyrene blocks, which tend to microphase separate from the polar ionic liquid and poly(ethylacrylate) blocks.[71,181–183] The extent of crosslinking increases with UV exposure time, making the gel a permanently crosslinked network. [180] We found 3 min exposure times produced gels with suitable adhesion to the substrate and excellent tolerance to Au vapor deposition without causing electrical shorts.

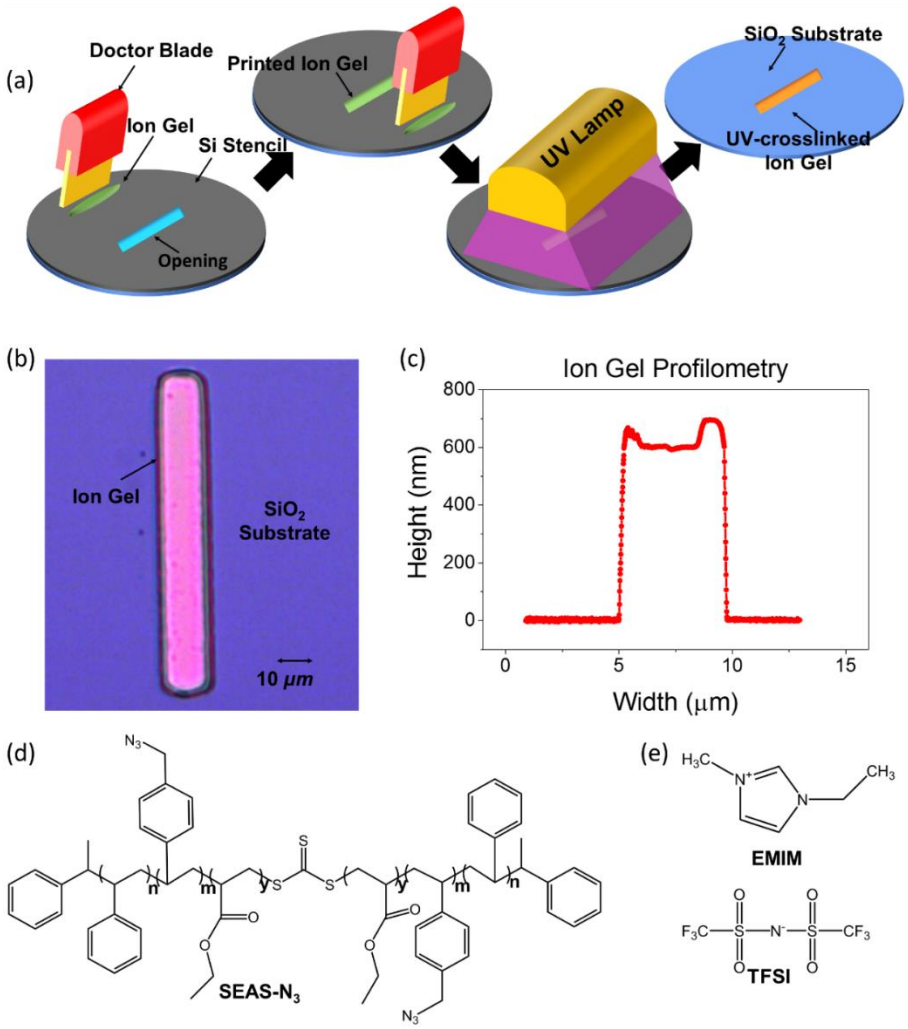


Figure 7.1. Screen-printing and UV-crosslinking of ion gel. a) A doctor blade squeezes the ion gel on the stencil. Then ion gel is UV-crosslinked, followed by the stencil removal. b) A stencil printed, UV-crosslinked ion gel on SiO_2. c) Profilometry of crosslinked ion gel with 20% wt SEAS shows the gel is 600 nm-thick. d) SEAS-N_3 polymer and e) EMIM TFSI ionic liquid.

To measure the quasi-static capacitance of the gels we constructed metal/ion gel/metal (MIM) capacitor structures, Figure 7.2a and 7.2b. The optical micrograph in Figure 2b shows that the stenciled ion gel dimensions were 30 x 200 μm^2. The capacitance was measured by recording the displacement current as a function of voltage sweep rate, Figures 7.2c and 7.2d. The extracted ion gel specific capacitance of 24 $\mu F/cm^2$ is comparable to previously reported MIM structures based on ionic liquids and gels,[66] and it is essentially independent of applied voltage, Figure 7.2e, as expected.

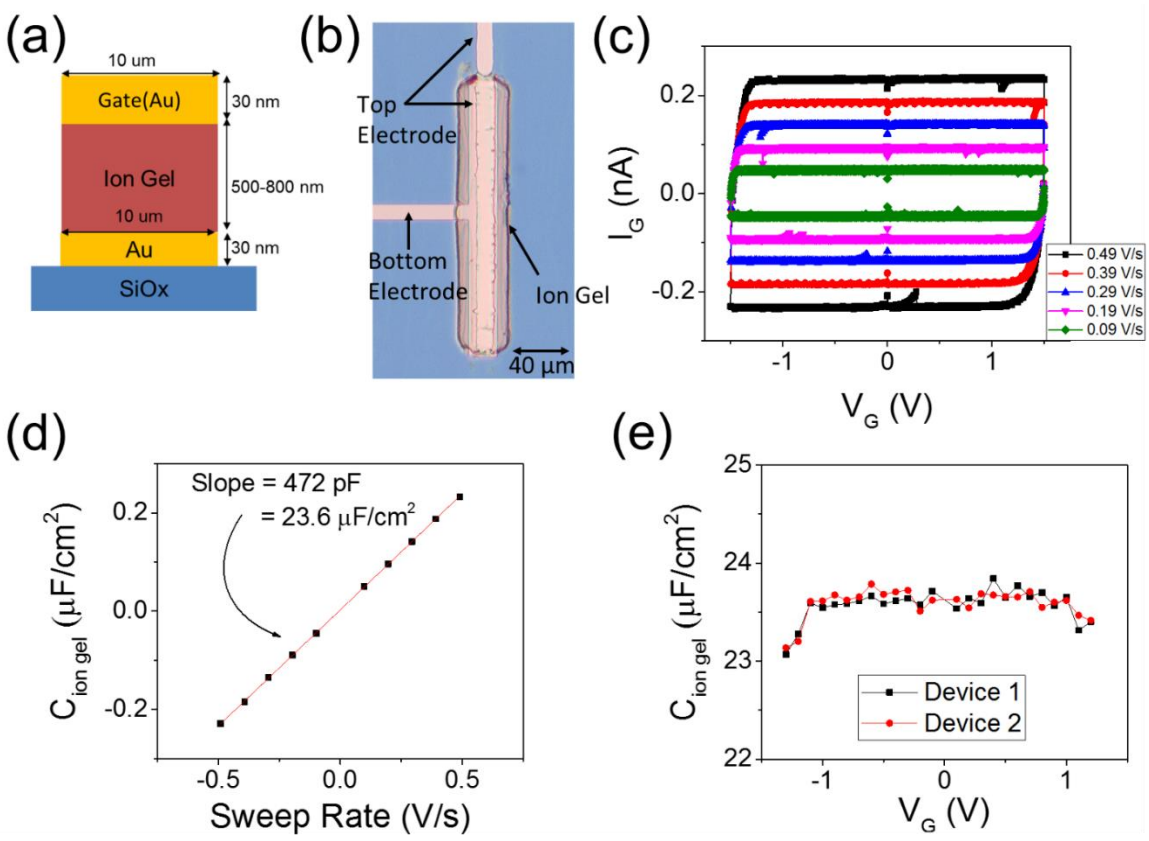


Figure 7.2. (a) Scheme of metal-ion gel-metal (MIM) capacitor and (b) corresponding optical micrograph. (c) Capacitor displacement current measurement at different voltage sweep rates. d) Capacitor displacement current at 0.5 V versus sweep rate; the slope gives the quasi-static capacitance. e) Quasi-static capacitance values for two different MIM devices as a function of voltage. The capacitor electrode areas are 200 µm×10 µm.

Figure 7.3a depicts a scheme of the top-gate EGT structure that we employed. The fabrication process is described in detail in the Supporting Information and illustrated in Figures A4.3 and A4.4. Briefly, the ZnO semiconductor film was first deposited on the SiO_2 substrate by ALD and patterned by photolithography and HCl etching. The Au source and drain electrodes with Ti adhesion layers and SiO_2 passivation overlayers were patterned by photolithography and lift-off. Importantly, the SiO_2 passivation layer reduced the contact area of the ion gel with the source and drain electrodes, thereby reducing parasitic, or so-called overlap capacitance, which can increase switching times.[11,19] The ion gel was screen-printed as described above with good alignment over the source-drain channel, and then another stencil was aligned to the gel and used as a mask for the vapor deposition of a Au top gate electrode.

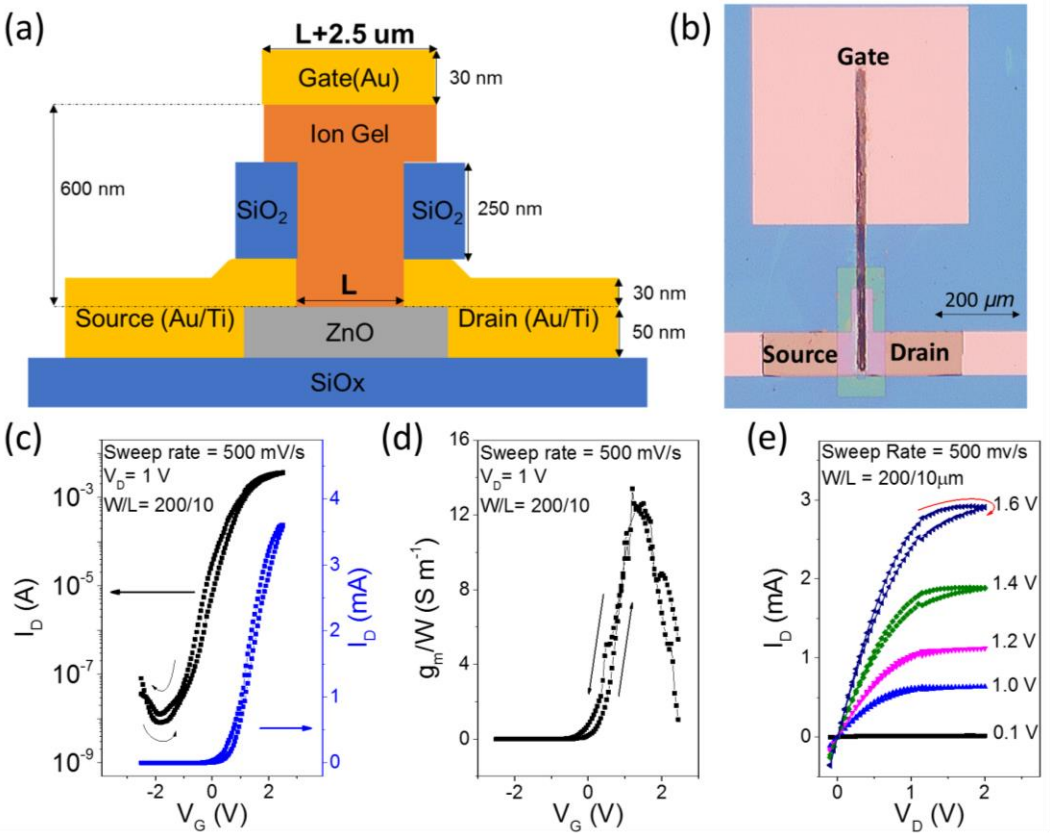


Figure 7.3. ZnO electrolyte-gated transistor quasi-static performance. a) The device schematic architecture. b) Optical image of the final EGT. c) The transfer curve for EGT

with W/L = 200 μm/10 μm at 500 mV/s gate voltage sweep rate and V_D = 1 V. d) The channel-width-normalized transconductance of the device. e) The output characteristics of the EGT at different V_G's.

Figure 7.3b displays an optical image of a completed ZnO EGT with channel aspect ratio width (W)/length (L) = 200 μm/10 μm. The patterned ion gel and Au top-gate have a resolution of 12.5 μm. Figures 7.3c and A4.5a reveal the quasi-static drain current (I_D) vs. gate voltage (V_G) characteristics at two different drain voltage values (V_D = 1 and 0.1 V, respectively) for a ZnO EGT with W/L = 200 μm/10 μm. The expected n-channel behavior is evident, and ON/OFF current ratios of $>10^5$ were achieved with positive threshold voltages,[155] V_{th} ~ 0.5 V.

The V_G dependences of the channel-width-normalized transconductance (g_m/W) at V_D = 1 and 0.1 V, respectively, for the same device are shown in Figures 7.3d and A4.5b. For an ideal transistor, g_m/W should be independent of V_G beyond threshold, but as is typical for EGTs,[80,167,168] g_m/W is peaked, as discussed further below. Maximum channel-width-normalized transconductance $(g_m/W)_{max}$ is the peak value of the Figure 7.3d plot. Further analysis is given in Figures A4.6a and A4.6b, which show plots of $(g_m/W)_{max}$ vs V_D and $(g_m/W)_{max}$ vs $1/L$.[82,184,185] As expected according to Equation 7.1,

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \mu \, C_G V_D \tag{7.1}$$

g_m/W increases linearly with V_D, Figure A4.6a, and is also linear with $1/L$, Figure A4.6b. For an EGT with W/L = 200 μm/10 μm, $(g_m/W)_{max}$ reaches 19 S/m at V_D = 1.5 V, Figure A4.6a, which is ~10 times higher than the previously reported values for solution-processed ZnO EGTs,[186,187] and which compares favorably to electrolyte-gated polycrystalline Si thin film transistors where g_m/W < 1 S m^{-1}.[11] The high value of

$(g_m/W)_{max}$ is due to a combination of the high channel charge density (~10 μC/cm^2 or 10^{14} carriers/cm^2) and the good electron mobility of ALD ZnO, estimated below.

The peaked g_m/W vs V_G behavior evident in Figures 7.3d and A4.5b suggests that the electron mobility is V_G dependent. Estimation of the mobility requires knowledge of the quasi-static gate capacitance C_G. We have measured the quasi-static C_G using the displacement current method (I_G-V_G) that we have reported previously, Figure A4.7a,b.[43] The C_G-V_G behavior is shown in Figure A4.7c. Using Equation 1, the linear regime (small V_D) transconductance data in Figure A4.5b, and the C_G-V_G behavior in Figure A4.7c, we have estimated the linear regime electron mobility vs V_G, Figure A4.7c. The mobility is indeed V_G dependent and ranges from ~2-9 cm^2/Vs. This compares favorably with our previous report of electron mobility in EGTs with solution processed ZnO (~1 cm^2/Vs).[186] However, this result also emphasizes a typical complication for thin film EGTs, namely that there isn't a single mobility value that captures the behavior of the device.

Figure A4.7c also shows very plainly why g_m/W vs V_G is peaked. The transconductance is directly proportional to both C_G and μ, Equation 7.1, which have opposite trends with V_G. Much more work is needed to fully understand the underlying causes of these trends, though we note that the decrease of μ with V_G may well be related to ion-induced disorder at the ZnO/electrolyte interface.[128]

Figure 7.3e displays the output characteristics (I_D-V_D) of the ZnO EGT, which follow the expected square law dependence on V_G. The linearity of the I_D-V_D traces near V_D=0 suggest that contact effects are minimal.[110,157,188,189]

Figures 7.4a and b display a scheme and optical micrograph of a ZnO EGT-based inverter. The load transistor is biased with an internal feedback loop as depicted in Figure

4a, in which the output voltage (V_{out}) is connected to the load transistor gate terminal. The quasi-static performance of the 200 µm/10 µm EGT inverter (V_{out} vs V_{in}) is shown in Figure 7.4c at V_{DD} = 3V and a sweep rate of 500 mV/s. The inverter curve has a sharp step with corresponding gain, $dV_{out}/dV_{in} > 20$, as shown in Figure 7.4d.[103,190,191] The high gain of these ZnO EGT-based inverters underscores their potential for further applications in low voltage bio-sensing, for example, where sensitivity is determined by inverter gain.[5,191,192] The gain dependence on drain voltage, V_D is displayed in Figure 7.4e. Higher operating voltage also leads to higher gain for ZnO EGT-based inverters, as expected.

The dynamic performance of the inverter was initially investigated using a square wave input. Typical devices reveal an ideal dynamic response up to 2.5 kHz, as depicted in Figure 4f. [124,185,193–195] We have estimated stage delays by measuring the time between the input falling edge (time = 0) and the point where $V_{out} = V_{SS}$ or V_{DD}. The stage delay is plotted as a function of device size (channel length L) for a constant W/L aspect ratio of 20 in Figure A4.6c. The trend clearly reveals that smaller device footprint leads to smaller delays, as expected. A stage delay of ~60 µs was achieved for the smallest channels.

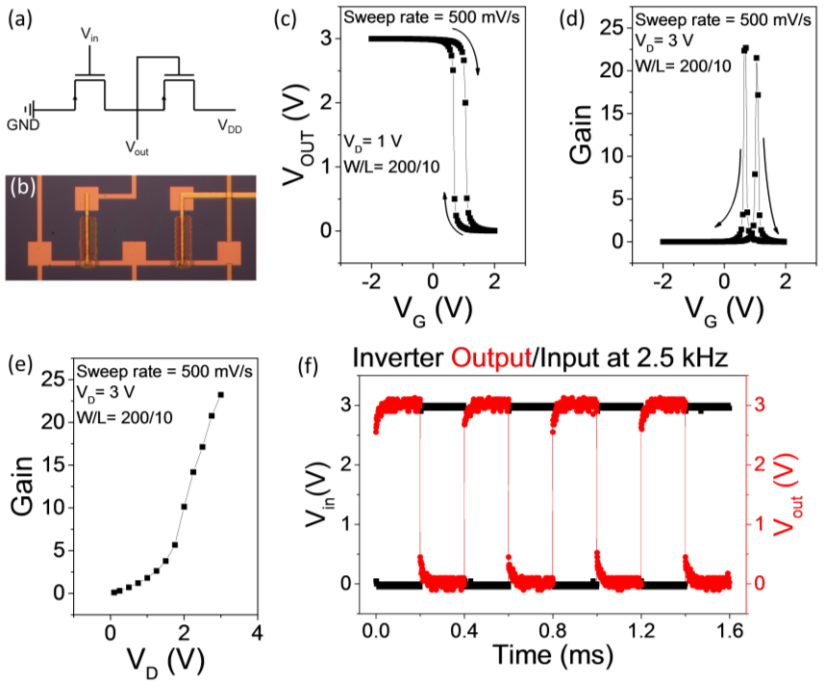


Figure 7.4. Inverter performance with internal loop feedback. a) Scheme of the inverter and b) the optical microscope image. The inverter c) quasi-static output vs. input and d) gain measurement at 500 mV/s sweep rate and V_D = *3 V*. e) The inverter gain dependence on applied bias voltage (V_D). f) The dynamic performance of the inverter with *W/L* = 200 µm/10 µm at 2.5 kHz and V_D = 3 V.

A better assessment of dynamic performance is obtained by examining ring oscillators based on the smallest ZnO EGT inverters with *W/L* = 200µm/10µm. Figures 7.5a and 5b display an optical micrograph and scheme of a 5-stage ring oscillator with an inverter buffer. The responses at different V_D and V_{Bias} values are plotted in Figures 5c and 5d. The maximum observed oscillation frequency, f_{osc}, is 1.9 kHz with V_D = 3 V and V_{Bias} = 2.75 V.[105,124,186,193,195–199] Considering the 5-stage ring oscillator rule, the stage delay is 50 µs, which is consistent with the data obtained from the discrete inverter dynamic response.

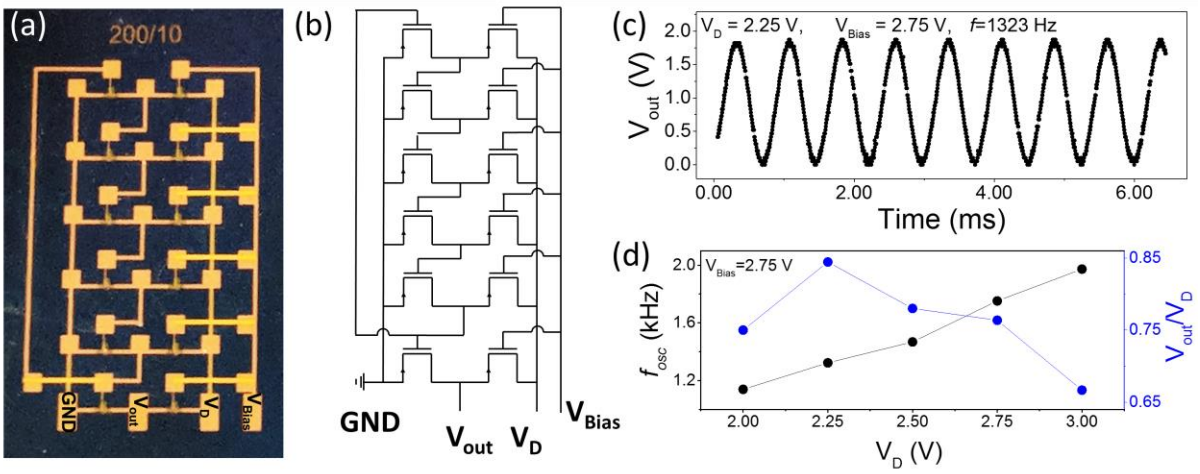


Figure 7.5. Low-voltage, five-stage ring oscillator. a) Optical image of EGT layout on SiO_2/Si. b) Circuit diagram. c) Output characteristics of a typical ring oscillator with oscillation frequency as high as 1,300 Hz. d) Frequency and output range of the ring oscillator as a function of drain voltage, V_D. Transistor dimensions: W/L = 200 µm /10 µm.

For an ideal device, the theoretical cut-off frequency, $f_{cut\text{-}off}$, can be calculated according to Equation 7.2:[110,157]

$$f_{cut-off} \approx \frac{\mu V_D}{2\pi L^2} \tag{7.2}$$

yielding an estimate of ~1 MHz for L = 10 µm and μ ~5 cm^2/Vs, which is clearly far higher than the ~20 kHz (50 µs) dynamic behavior we observe. We have shown previously that parasitic gate-source capacitance can dramatically increase delay times in EGTs,[138,179] and consequently we undertook AC impedance measurements on a typical ZnO EGT with W/L = 400 µm/20 µm, Figure 7.6, to assess dynamic capacitance. Figure 7.6a shows the C_G-V_G relationship at frequencies ranging from 10-50 kHz, and the inset indicates the measurement scheme in which the two terminals for the measurement are the gate contact and the source/drain electrode pair. As V_G sweeps positively the channel opens and C_G increases from ~25 pF to 60 pF at 10 kHz (25 pF is the capacitance floor associated with residual parasitic or 'overlap' capacitance in the device). An increase in C_G is expected as the ZnO channel becomes conductive above the threshold voltage, which increases the

effective capacitor area. The smaller C_G values at higher frequencies are a reflection of the inherent capacitance dispersion of electrolytes. That is, there is not a single number for capacitance for electrolytes in contact with semiconductors; the capacitance is a function of both time and voltage.

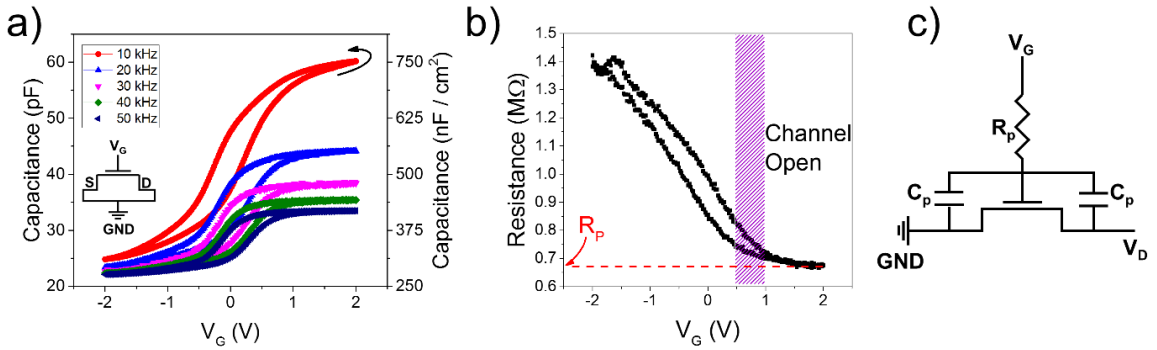


Figure 7.6. ZnO EGT impedance measurements. a) Dynamic capacitance vs. V_G relationship at different frequencies for a device with W/L = 400 µm/20 µm. For these measurements, the source and drain electrodes were shorted together; the second contact was the gate electrode. b) The device resistance vs V_G at 1 kHz measured simultaneously with the C-V_G relationship in a). The plateau value positive V_G is taken to be the parasitic series resistance R_p associated with the ion gel. c) The proposed equivalent circuit for a ZnO EGT indicating parasitic resistance and capacitance.

Critically, in addition to providing C_G, the impedance spectroscopy measurements also provide a measurement of the ion gel (ionic) resistance. [200,201] The gel has resistance because ions in the electrolyte have to move to charge/discharge the double layers when V_G changes. We term the gel resistance a series parasitic resistance R_P. Figure 7.6b displays total gate resistance R_G vs V_G. As V_G sweeps positive, the resistance decreases because R_G includes the sheet resistance of the ZnO channel. However, upon crossing the threshold voltage, R_G plateaus; we take the plateau value to be R_P, the parasitic resistance of the ion gel film. The key point is that R_P is enormous, on the order of 0.6-0.7 MΩ.

These impedance measurements thus provide a clear explanation for the discrepancy between delay times we measure (~50 µs) and what we might expect for an ideal device (~ 1 µs) based on Equation 2. The ion gel resistance R_P between the gate

contact and the channel, Figure 7.6b, is large. That is, polarization of the gate involves sluggish ion motion which dominates the dynamic performance of the device. The product R_pC_G can provide a rough estimate of the stage delay time. Taking R_P = 0.7 MΩ and C_G = 50 pF, we obtain R_pC_G = 35 μs, very close to the 50 μs delay time we measure. This R_pC_G calculation yields an expected delay 35 times greater than the ideal Equation 2 calculation. The implication is clear: our EGT inverters and ring oscillators are largely limited by the parasitic series (ionic) resistance of the cross-linked ion gel and not by the ZnO channel resistance. In order to shorten delay times, the ionic conductance of the photo-crosslinked ion gel films must be dramatically improved. We note in this respect that the photo-crosslinked ion gel we employed here offers processing advantages because it can be photopatterned and it is stiff enough to enable subsequent vapor deposition of a metallic gate, but its ionic resistance is far higher (>80x) than other formulations of the ion gel that we have reported previously.[3] Thus, there are significant prospects for further increases in EGT switching speeds with further optimization of the ion gel.

We also note that in our prior work we have emphasized the important role of parasitic parallel capacitance in EGTs due to electrolyte overlap with the source and drain electrodes, Figure 6c.[33,34] Parasitic capacitance continues to be an important speed limiting factor for EGTs (though we have taken steps to minimize it here), but our current work now highlights the critical role of an additional factor, namely parasitic series resistance. Despite these limitations, we have achieved state-of-the-art switching times for EGTs using a clean-room compatible fabrication process. Future work will focus on developing new ion gel materials and patterning methods to minimize all parasitic effects that limit EGT performance.

7.3 Conclusion

Photopatterned ion gel-based transistors have been successfully fabricated using a photo-crosslinkable ion gel. Advantages of the ion gel formulation are that it permits fine feature sizes fabricated using clean-room compatible techniques, and that it is compatible with thermal evaporation of metal gate electrodes; a disadvantage is the relatively high ionic resistance. ZnO-based EGTs and inverters fabricated with the gel operate at supply voltages < 3V and exhibit high gain (>20), channel-width-normalized maximum transconductances (20 S m^{-1}), and short 50 μs delay times, respectively, which pave the way toward new applications of EGTs. We have also shown that ion gel resistivity (parasitic resistance) along with parasitic capacitance are important to EGT dynamic performance. These considerations are central to ongoing efforts to improve the dynamic performance of low voltage EGTs for a variety of applications. [174,202]

7.4 Experimental Section

Photo-Patternable Ion Gel, Synthesis and Preparation: Poly[(styrene-*r*-vinylbenzyl azide)-*b*-poly(ethyl acrylate)-*b*-poly(styrene-*r*-vinylbenzyl azide)] (SEAS-N3) was synthesized via reversible addition−fragmentation chain transfer (RAFT) polymerization and a post polymerization reaction.[203] The detailed synthetic procedures have been described in a previous report.[180] The ionic liquid, 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide [EMI][TFSI], was purchased from Sigma Aldrich. The SEAS-N3 ion gel films were prepared using screen-printing from an ink solution prepared by co-dissolving SEAS-N3 and [EMI][TFSI] in ethyl acetate at a 1:9:10 ratio (w/w/w). The ion gel ink was kept in a –20 ºC freezer before printing. More details about this process are available in Supporting Information.

Si Stencil Fabrication: A 4-in. silicon wafer with a thickness of 525 (±25) µm was submerged in a potassium hydroxide (KOH) bath (30 wt% KOH in deionized water) at 90 °C for 105 min to reduce the thickness to ~100 µm, rinsed with deionized water, and dried. The wafer was prebaked at 200 °C for 5 min, vapor-coated with hexamethyldisilazane for 15 min, and spin-coated with photoresist (AZ9260) at 300 rpm for 10 s and at 3500 rpm for 60 s, sequentially. After soft-baking at 110 °C for 165 s, the photoresist was exposed to UV light through the photomask using a standard mask aligner (MA6, Karl Suss). Subsequently, the wafer was immersed for 1 min in a developer solution AZ400K and deionized water (1:3.5 v/v) and then rinsed with deionized water. This process was repeated 3 times and then the wafer was dried. The thinned wafer was bonded to a dummy wafer of standard thickness for support. First, the dummy wafer was spin-coated with Shipley S1813 photoresist at 3000 rpm, and then the thinned silicon wafer was bonded to it by heating the assembly to 105 ºC for 1 min. The dual wafer assembly was then etched by reactive ion etching (SLR-770, Plasma-Therm) for 200 Bosch cycles (~45 min). This process opened up the desired windows in the thinned wafer. After etching, the assembly was rinsed with acetone, ethanol, isopropanol, and deionized water to remove the photoresist. The dummy wafer was detached simultaneously with photoresist removal by gentle leveraging at the edges with a razor blade.

Device Fabrication: The detailed fabrication process is discussed in Supporting Information and Figure SI7. Briefly, ZnO was deposited using an ALD system (Savannah Series, Cambridge Nano Tech) with diethylzinc (DEZ) and water vapor as precursors. The ZnO film was annealed in a rapid thermal annealer (RTP-600S, Modular Process Technology): the first anneal at 300 ºC in N_2 lasted 15 min. The second anneal followed at

400 ºC in O_2 for another 15 min. The ZnO was then patterned with standard photolithographic procedures. HCl was used to wet etch ZnO. Standard lithography processes using Shipley S1813 resist were used to make the source and drain electrodes. An e-beam thermal evaporator (Temescal) was used for metal deposition. SiO_2 over the electrodes was e-beam deposited (Varian 3118). Acetone and isopropanol (50:50 v/v) were used for the overnight lift-off process. The same aligner used for photolithography (Karl Suss MA6) was used to align the silicon stencil. UV cross-linking of the ion gel on a selected area was conducted using a FBUVL-80 hand-held UV lamp (Spectroline™, intensity = 470-500μW/cm^2 at 254 nm).

Materials and Film Characterization: The thicknesses of ZnO and ion gel films were measured by a Gaertner Ellipsometer and KLA-Tencor P-16 surface profiler, respectively.

Electrical Characterization: Current−voltage (I−V) and capacitance-voltage (C−V) characteristics of transistors were collected using Keithley 237 and 2612B sourcemeters and an Agilent B1500A semiconductor parameter analyzer (C_s-R_s configuration) in combination with a motorized probe station in a N_2-filled glovebox and a Desert Cryogenics (Lakeshore CPX-VF) vacuum probe station, respectively. A Keithley 6517 electrometer was used to measure the inverter static output voltage. An Agilent 33500B waveform generator generated the input signal for inverters and a Tektronix TDS1002B digital oscilloscope was used to measure dynamic output voltage. All measurements were performed in inert atmosphere. The ZnO EGTs are electrochemically stable up to 3V.

Supporting Information. Supporting Information is available on Appendix 4 and from the Wiley Online Library or from the author.

Chapter 8 Ongoing Research and Future Work

8.1. 10 MHz class printed ion gel-base thin film transistors: Sub-3 V ZnO Electrolyte-Gated Transistors and Circuits with Improved Performance

A combination of best available structure and materials for electrolyte-gated transistor is shown. The ALD-grown ZnO film with thermally evaporated Au electrodes and SiO_2 passivation layer in combination with sequentially aerosol-jet printed ion gel and PEDOT:PSS leads to fast, high performance electrolyte-gated transistors. The resulting n-type ZnO EGTs display high electron mobility (9 cm^2/Vs) and ON/OFF current ratios (10^6). Further, EGT-based inverters exhibit static gains > 70 at supply voltages below 3 V, and five-stage EGT ring oscillator circuits display dynamic propagation delays of 0.12 μs/stage. In general, the aerosol-jet printing of ion gel and high quality ZnO semiconductor enabled circuits with improved sensitivity (gain) and computational power (gain × oscillating frequency).

8.1.1 Introduction:

Electrolyte-gated transistors (EGTs), including electric double layer transistors (EDLTs) and organic electrochemical transistors (OECTs), are being developed by a number of research groups for applications in bio- and printed electronics.[1,79,80,99,107,162–170,204,205] Attractive features of EGTs are their very high transconductances and low voltage characteristics, both of which derive from the huge specific capacitance of the electrolyte gate dielectrics that they employ, which varies from ~10 $\mu F/cm^2$ in the double layer operating regime to over 100 $\mu F/cm^2$ in the electrochemical regime.[1,12,127,171–177]

Applications of EGTs, require that these devices be integrated into circuits and thus they must have high speed response as well high transconductance.[202] Previously, it has been shown that the quasi-static qualities of EGTs can be improved by replacing organic semiconductor to high quality inorganic semiconductor. It has been shown that for the EGTs with high mobility the signal can path the micron size channel length in the order of μs. It has been also shown that the electrolyte can have the switching time (*RC*) in the order of tens of μs. We have showed previously that parasitic effects including series resistance and parallel capacitance can limit the device performance. The combination of highly ionic conductive and high mobility semiconductor in an optimized device architecture has not been reported, yet.

In this work our goal was to create discrete EGT devices and circuits by hybrid fabrication in order to have the best operating EGTs. In parallel, we aimed to improve EGT switching times by minimizing parasitic effects,[148–151] and by employing high electron mobility ZnO semiconductor films grown by atomic layer deposition (ALD) in combination with short (10 μm) source-drain channel lengths. In this work, we applied the previously optimized ion gel with high ionic conductivity.[3,73] We show here that these collective strategies have allowed us to fabricate high performance EGT circuits operating with sub-3V supplies and inverter stage delays of close to 0.1 μs. Importantly, we were able to MHz operation of 5-sage ring oscillators and show how the device performance scales with device geometry.

8.1.2 Results and Discussion:

Figure 8.1 shows hybrid fabrication of the ZnO EGTs. The ZnO film was grown by ALD and patterned by photolithography and wet etching. The electrodes and passivation

layers were deposited and patterned by e-beam evaporation and lift-off. The ion gel and gel layer were aerosol-jet printed.The ion gel ink was composed of a 1:9:90 weight ratio mixture of poly(styrene)-poly(ethylacrylate)-poly(styrene) triblock copolymer (SEAS) and the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMI TFSI) in ethyl acetate solvent.[70] Figures 8.1.2 d and e display the chemical structures of the ion gel components. The capacitance of the ion gel was measured by shorting the source and drain through both displacement current and impedance measurements.

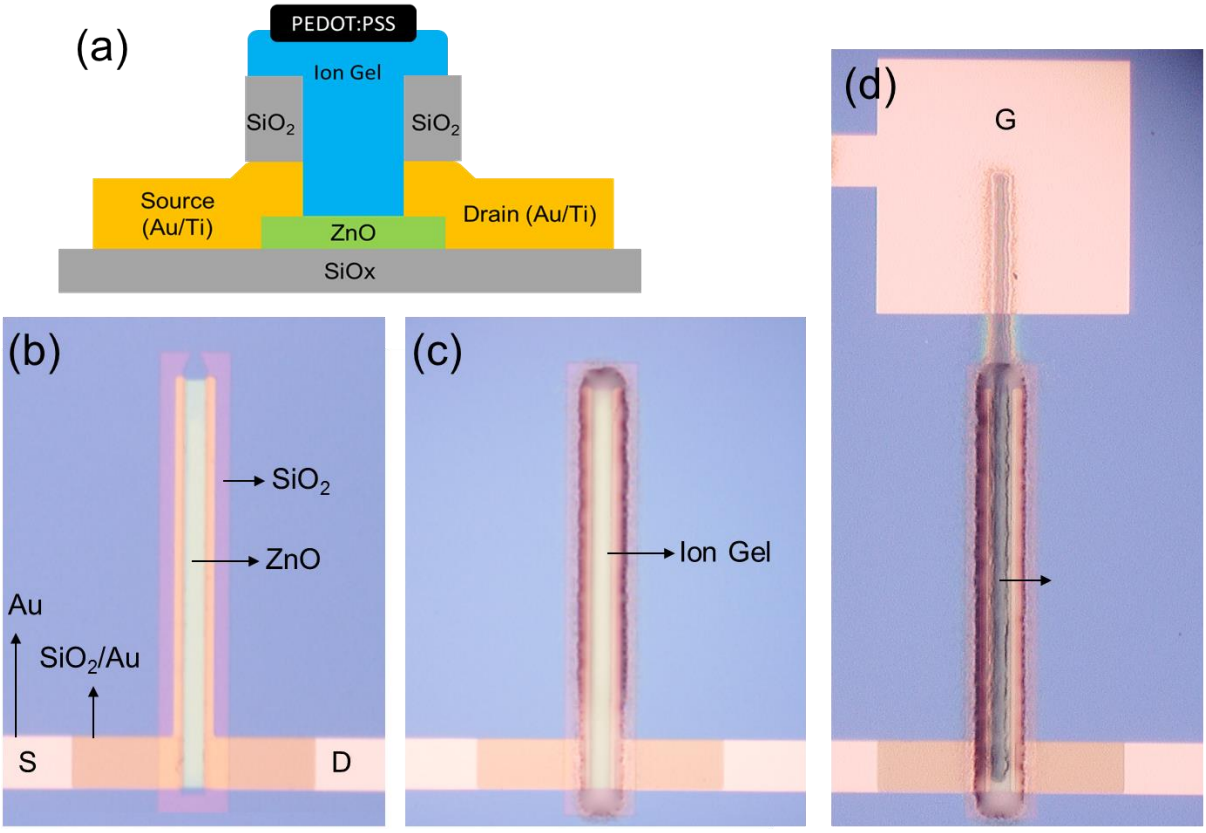


Figure 8.1.1. The hybrid fabrication of ZnO EGTs. a) the scheme of ZnO EGT cross-section. b) The ALD-grown ZnO, followed by e-beam thermally deposited electrodes which are passivated by SiO_2. There is additional layer of SiO_2 as a support to ion gel. All of these layers are deposited and patterned through conventional microfabrication methods in cleanroom. c) Ion gel and d) PEDOT:PSS are deposited by AJP to complete the device.

Figure 8.1.1a depicts a scheme of the top-gate EGT structure that we employed. Briefly, the ZnO semiconductor film was first deposited on the SiO_2 substrate by atomic

layer deposition (ALD) and patterned by photolithography and HCl etching. The Au source and drain electrodes with Ti adhesion layers and SiO_2 passivation overlayers were patterned by photolithography and lift-off. Importantly, the SiO_2 passivation layer reduces the contact area of the ion gel with the source and drain electrodes, thereby reducing parasitic, or so-called overlap capacitance, which can increase switching times.[11,179] The ion gel and PEDOT:PSS films were deposited with 10 µm resolution with aerosol-jet printer.

Figure 8.1.1d displays an optical image of a completed ZnO EGT with channel aspect ratio width (W)/length (L) = 600 µm/30 µm. Figure 8.2a and b reveal the quasi-static drain current (I_D) vs. gate voltage (V_G) characteristics at two different drain voltage values (V_D = 1 and 0.1 V, respectively) for a ZnO EGT with W/L = 200 µm/10 µm. Figure 2d further explores the robustness and sweep rate independence of ZnO EGTs over the time. ON/OFF current ratios of ~10^6 were achieved with positive threshold voltages,[155] V_{th} ~ 0.75 V. The estimated average electron mobility μ is 10 cm^2/Vs,[206] according to the standard linear regime relation for the transconductance g, Equation 9.1:[82,185]

$$g = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}\mu\, C_G V_D \tag{8.1.1}$$

This extracted high μ is due to the high quality of ALD-deposited and annealed ZnO.[207]

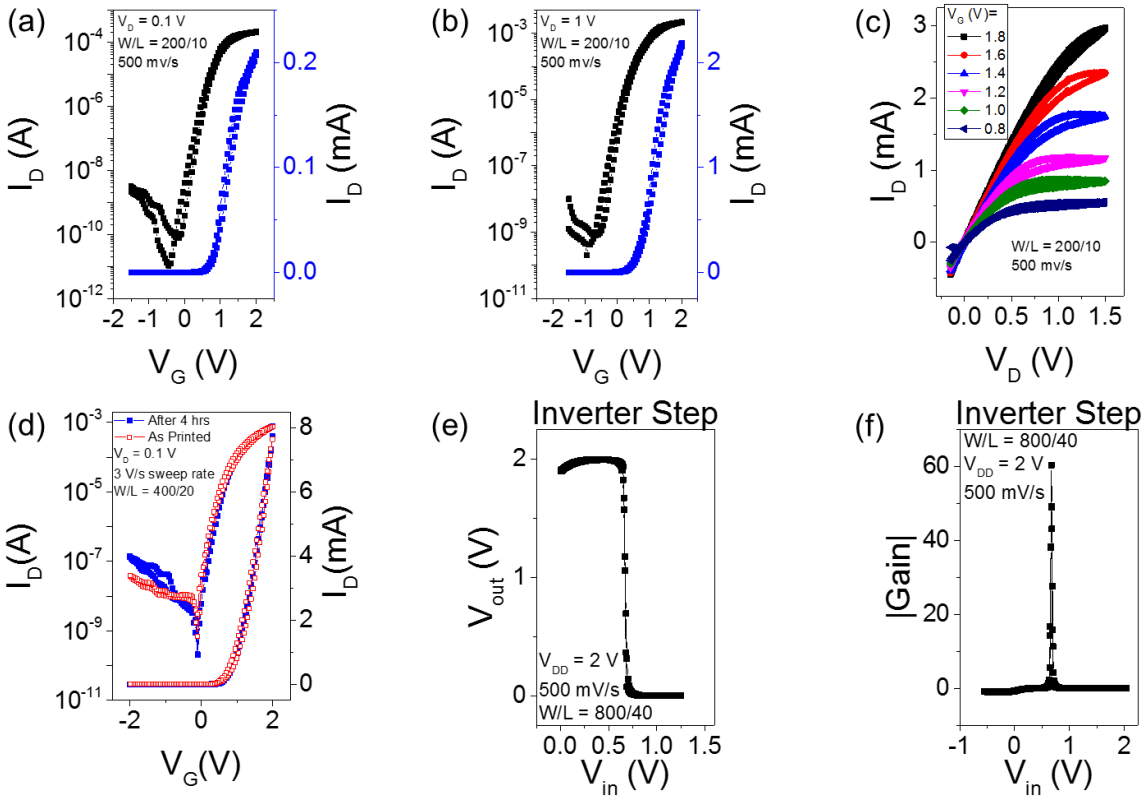


Figure 8.1.2. Quasi-static performance of ZnO EGT and Inverter. Transfer curves at V_D = a) 0.1 V and b) 1.0 V and c) the output characteristic for W/L = 200 µm/10 µm. d) the stability of ZnO EGT for W/L = 400 µm/20 µm after 4 hrs of 2V square-wave input at V_G. e) Inverter step and f) inverter gain for the configuration of inverter used in chapter 7 with internal feedback loop.

Figure 8.1.2c displays the output characteristics (I_D-V_D) of the ZnO EGT which follow the expected square law dependence on V_G. The linearity of the I_D-V_D traces near V_D=0 suggest that contact effects are minimal.[85,110,189]

Figures 8.2e and f display a ZnO EGT-based inverter performance. The load transistor is biased with an internal feedback loop as depicted in Figure 7.4a, in which the output voltage (V_{out}) is connected to the load transistor gate terminal. The quasi-static performance of the 200 µm/10 µm EGT inverter (V_{out} vs V_{in}) is shown in Figure 8.2 e at V_{DD} = 2V and a sweep rate of 500 mV/s. The inverter curve has a sharp step with corresponding gain, dV_{out}/dV_{in} > 60 as shown in Figure 8.1.2f.[103,190,191] The high gain of

these ZnO EGT-based inverters underscores their potential for further applications in low voltage bio-sensing, for example, where sensitivity is determined by inverter gain.[83,192,194]

The dynamic performance of the inverter was initially investigated using a square wave input. A typical device with *W/L* = 200/10 reveal an ideal dynamic response up to 300 kHz, as depicted in Figure 8.1.3. [10,86,124,195,196]

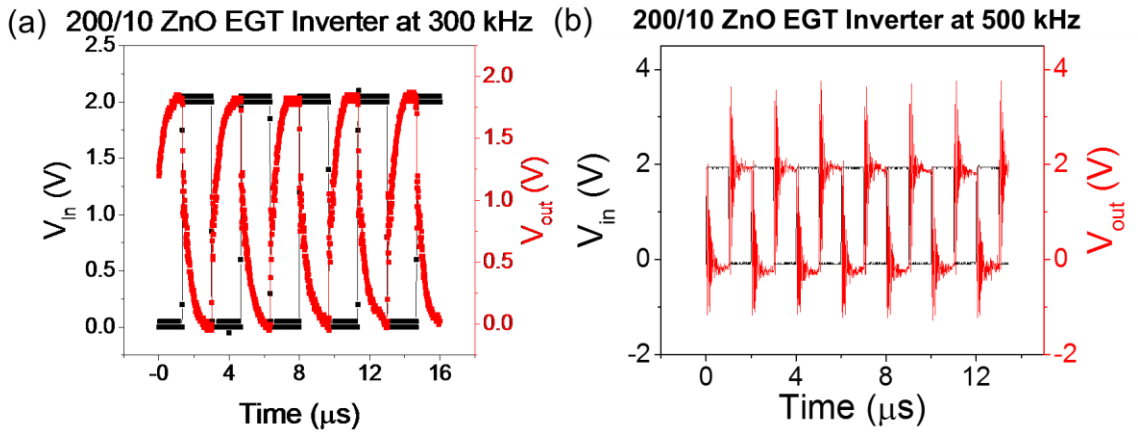


Figure 8.1.3. Inverter dynamic performance. a) 300 kHz and b) 500 kHz square-wave input for *W/L* = 200 μm/10 μm ZnO EGTs. For b) the different oscillation time constants are observed. A potential reason for these oscillations is ion gel *RC* time constant.

A better assessment of dynamic performance is obtained by examining ring oscillators based on the smallest ZnO EGT inverters with *W/L* = 200 μm/2.5 μm. Figure 8.4a display an optical micrograph a 5-stage ring oscillator with an inverter buffer. The maximum observed oscillation frequency, f_{osc}, is 1.72 MHz with V_D = 3 V and V_{Bias} = 1.5 V.[10,86,105,124,195,198,199,208] Considering the 5-stage ring oscillator rule, the stage delay is 0.12 μs, which is consistent with the data obtained from the discrete inverter dynamic response.

For an ideal device, the theoretical cut-off frequency, $f_{cut\text{-}off}$, can be calculated according to Equation 2:[85,110]

$$f_{cut-off} \approx \frac{\mu V_D}{2\pi L^2} \qquad (8.1.2)$$

yielding an estimate of ~15 MHz for L = 2.5 μm, which is close to 8 MHz (0.125 μs) dynamic behavior we observe. We have shown previously that parasitic gate-source capacitance and series resistance can be the problems in EGTs that can dramatically increase delay times,[11,179] and consequently we minimized the parasitic effects in the EGT design in this chapter.

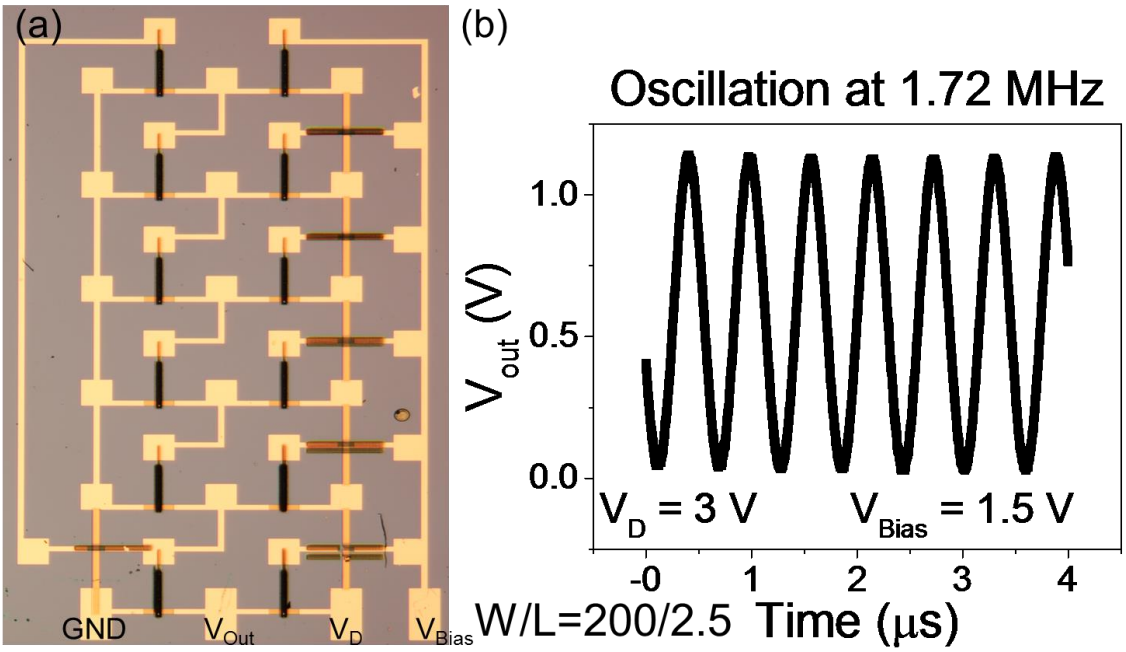


Figure 8.1.4. Ring oscillator performance. a) The optical image of the 5 stage ring oscillator with an inverter buffer. b) The inverter output for W/L = 200 μm/2.5 μm ZnO EGTs at V_D = 3V and V_{Bias} = 1.5 V.

8.1.3 Conclusion:

In conclusion, maximized ionic conductivity ion gel with minimized parasitic effects enabled us fabrication of 10 MHz class ZnO EGTs. These considerations are central to ongoing efforts on low voltage EGTs for a variety of applications.

8.1.4 Experimental Section:

Device Fabrication: ZnO was deposited using an ALD system (Savannah Series, Cambridge Nano Tech) with diethylzinc (DEZ) and water vapor as precursors. The ZnO film was annealed in a rapid thermal annealer (RTP-600S, Modular Process Technology): the first anneal at 300 ˚C in N_2 lasted 15 min. The second anneal followed at 400 ˚C in O_2 for another 15 min. The ZnO was then patterned with standard photolithographic procedures. HCl was used to wet etch ZnO. Standard lithography processes using Shipley S1813 resist were used to make the source and drain electordes. An e-beam thermal evaporator (Temescal) was used for metal deposition. SiO_2 over the electrodes was e-beam deposited (Varian 3118). Acetone and isopropanol (50:50 V/V) were used for the overnight lift-off process. The ion gel and PEDOT:PSS were aerosol-jet printed (AJ 100, Optomec Inc.) with sheath/carrier flow rates of 25 sccm/8 sccm and 18 sccm/12 sccm with 100 μm nozzle and 0.25 and 0.36 power, respectively.

Materials and Film Characterization: The thickness of ZnO was measured by a Gaertner Ellipsometer.

Electrical Characterization: Current−voltage (I−V) and capacitance-voltage (C−V) characteristics of transistors were collected using Keithley 237 and 2612B sourcemeters in combination with a motorized probe station in a N_2-filled glovebox. A Keithley 6517 electrometer was used to measure the inverter static output voltage. An Agilent 33500B waveform generator generated the input signal for inverters and a Tektronix TDS1002B digital oscilloscope was used to measure dynamic output voltage. All measurements were performed in inert atmosphere.

8.2 Electrolyte-gating mechanism study on 2*D*-MoS_2 EGTs[1]

2D materials such as MoS_2 and graphene have drawn attention due to their great electrical properties including high charge carrier mobility. We fabricated and characterized single-layer and multi-layer MoS_2 EGTs to further study EGT performance including the dynamic performance and its effect on the semiconductor channel stabilities.

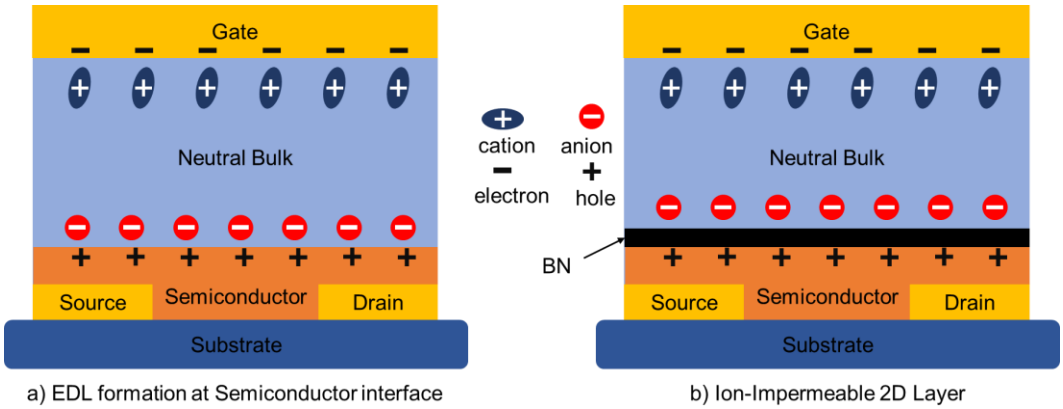


Figure 8.2.1. The experimental plan for investigating the effect of ions bombardment the semiconductor surface. a) MoS_2 EGT and b) MoS_2 EGT with BN barrier as an ion-impermeable layer between semiconductor and ion gel are displayed.

We have observed that single-layer MoS_2 is not very stable and is especially vulnerable to a square-wave input. One possible reason is ion bombardment or heating of the MoS_2 single layer. To investigate this hypothesis, one solution is to put an ion-impermeable layer such *BN* on the channel and study the EDL formation effect on the semiconductor channel. Figure 8.2. shows the suggested device architecture for this experiment.

[1] In collaboration with Yan Wang.

8.3 Stencil-assisted, spray-coated fast EGTs

In chapter 8.1, fastest EGTs were fabricated by aerosol-jet printing (AJP) of ion gel and PEDOT:PSS. It was shown that the gel *RC* time constant and semiconductor quality (mobility) constant limit the dynamic performance of the EGTs. Achieving a better semiconductor mobility requires smaller gel *RC* time constants to further improve the EGTs' dynamic performance. Therefore, the ion gel capacitance and ionic resistance must be reduced. Further improvements are achieved by having a more conductive gate, Equation 8.3.1.

$$R_{GeI}\, C_{GeI} = \rho L C_{specific} \tag{8.2.1}$$

Where ρ is the gel ionic conductivity, L is the ion gel thickness, and $C_{specific}$ is the gel specific capacitance. Considering ρ and $C_{specific}$ are already optimized [boxin paper], L is the only fabrication parameter left to be optimized.

Figure 2.6. displays the nozzle for the AJP. The carrier gas delivers the aerosol to the nozzle and the aerosol is then focused on the substrate by the sheath gas flow. These flows and their effects on the aerosol particle impacts upon the deposition on the substrate were studied by Ethan B. Secor.

Figure 8.3.1 shows ion gel confocal microscopy before and after PEDOT:PSS was printed on top of it. Since the aerosols have momentum when hitting the substrate, they deform the ion gel, especially on the heated aerosol-jet printer stage.[ethan secor papers] While the deformation of the ion gel helps achieve the final thin ion gel layer on the device, it limits the reproducible final ion gel thickness to ~3 μm.

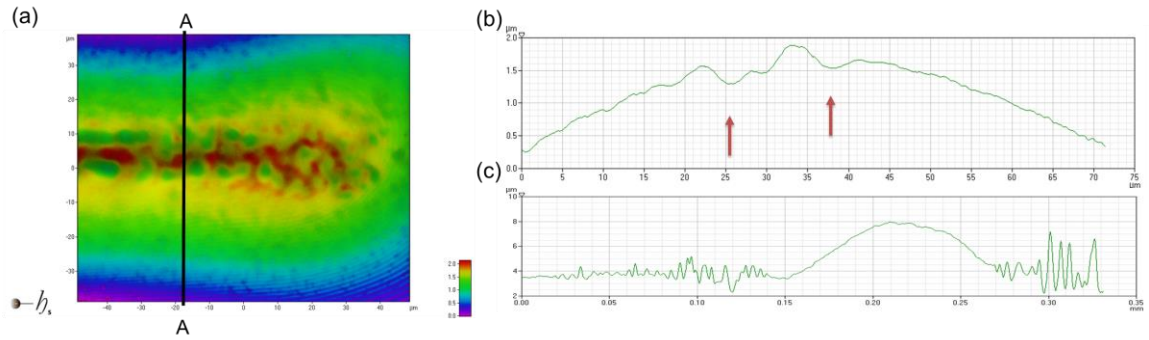


Figure 8.3.1. The confocal microscopy of the ion gel deformation. a) confocal image of ion gel with AJP printed PEDOT:PSS on top. The height analysis along the line A-A is give in b). The red arrows in b) represents the edges of the printed PEDOT:PSS. c) Ion gel as printed by AJP.

In order to have faster EGTs, a thinner ion gel is needed. One potential fabrication method is the combination of the aligned stencil used in chapter 8 and spray coating for the gel and PEDOT:PSS deposition. A second stencil is used for the Au deposition as a second piece of the gate electrode and interconnect. Figure 8.3.2 shows the stencil assisted delivery of ion gel, PEDOT:PSS, and Au. The previous layers are prepared as chapter 7.

The benefits of this fabrication method are better alignment than AJP, less particle impact, thinner ion gel layer, higher resolution, and having a 2-component gate with better conductivity in comparison to PEDOT:PSS and higher gating power in comparison to Au. The first gate layer is PEDOT:PSS at the interface of the ion gel with electrochemical doping capacitance of 100 $\mu F/cm^2$ whereas the second layer is Au with higher conductance. The goal of this fabrication is to minimize gate resistance. If a 500 nm-thick layer of ion gel is accessible, a 5-fold increase in the EGT dynamic performance is achievable.

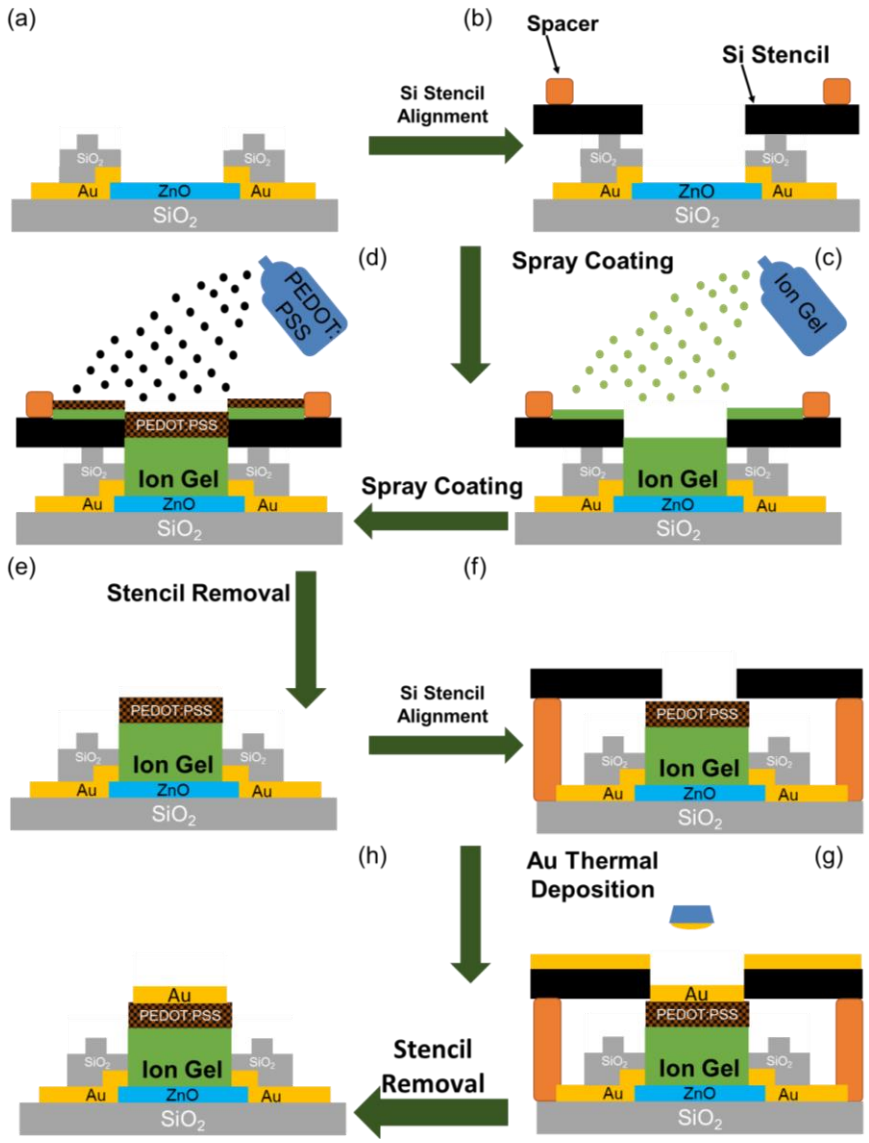


Figure 8.3.2. Hybrid gate fabrication with minimized ion gel thickness. a) the substrate is fabricated as the procedure mentioned in Chapter 7. b) a silicon-stencil is aligned with the aligner as described in Chapter 7. c) ion gel and d) PEDOT:PSS are sprayed on top of the stencil and substrate assembly. e) the stencil is removed. f) second silicon-stencil with the interconnect pattern is aligned and attached to the substrate. g) the whole assembly of stencil and substrate is put in the e-beam thermal Au evaporator. h) the stencil is removed, and the final structure is shown.

8.4 New designs for SCALE-processed EGTs[2]

As was discussed in section 8.3, AJP limits the thickness of the ion gel. Moving from AJP to another nozzle-based and more commonly used printing method (inkjet printing) is another option. The ink drops deposited by an inkjet printer are softer and have less impact which helps create thinner layers of printed ion gel film. In other to improve the resolution and alignment, a patented technique has been developed in Frisbie and Francis groups which is known as SCALE (Self-aligned, Capillarity- Assisted, Lithography for Electronics).[18,19,51,65,146,209–213] SCALE is discussed in Chapter 6. Briefly, SCALE is inkjet printing on a prepatterned substrate where the ink droplets are delivered to reservoirs and are confined by capillary channels connected to them. Despite all the improvements in SCALE, especially in quasi-static performance, fabrication of a fast SCALE EGT is a question. Here, two different strategies for having top-gated SCALE EGTs are provided. The current main challenge that needs to be addressed is capillarity flow of ion gel on the semiconductor and gate on the ion gel.

8.4.1 Hydrophilic ion gel and ZnO semiconductor

All the SCALE EGTs reported are based on the P3HT which makes a very hydrophobic surface. Having ion gel flowing on top of the P3HT requires tall walls of ~10 µm. Changing the P3HT to a semiconductor such as ZnO can help with the flow of ion gel which results in shorter ion gel walls and reduced final thickness. In order to use a ZnO layer in SCALE, a through study of electrode and substrate thermal stability is required as the ZnO annealing temperature is 300 °C.

[2] In collaboration with Motao Cao and Venkatesh Paidi.

To further assist with capillarity flow, the ionic liquid can be changed to a more hydrophilic one.[214] The hydrophilic ion gel not only can help with flow on top of ZnO but also can help with PEDOT:PSS flow on top of the ion gel.

If all the above-mentioned experiments are successful, the SCALE EGT design used in reference [[210]] is able to deliver kHz performance.[210]

8.3.2 Co-center reservoir design for semiconductor/ion gel/gate

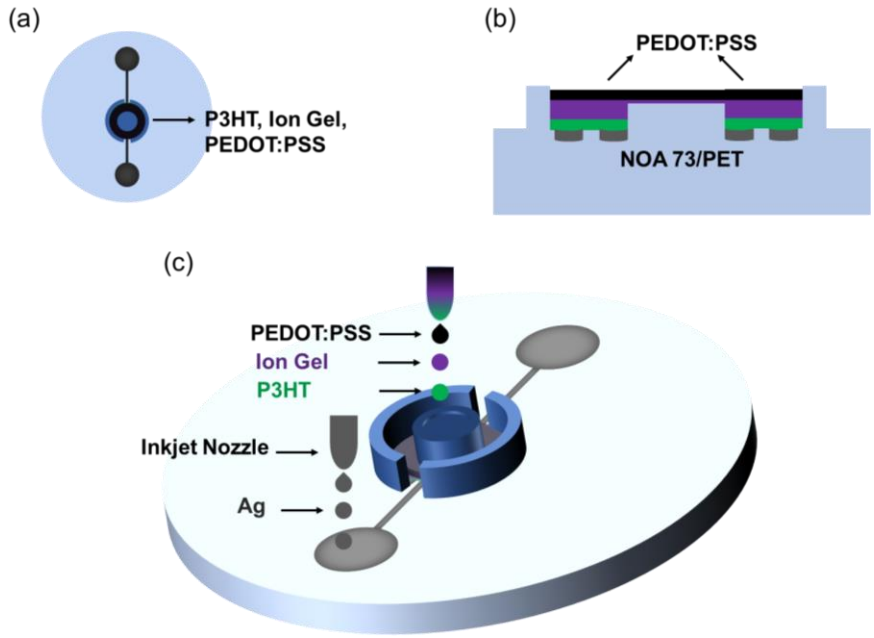


Figure 8.4.1. Top-gated SCALE EGT. a) The top view, b) the cross-section, and c) 3D scheme of printing of top-gated SCALE EGT. The same reservoir is used for P3HT, ion gel, and PEDOT:PSS.

In the previous chapter, the difficulty of having all the ink layers flowing on top of each other was mentioned. Another possible solution is to minimize the traveled length for the semiconductor, ion gel, and gate layers. Using a co-center design as shown in Figure 8.3.4 can help minimize the travel length and parasitic capacitance simultaneously. If an ion-impermeable semiconductor is used for this design, even a lower parasitic is expected.

Since the electrodes' widths in the functional area can be as small as 500 nm [Woo Jin and Fazel Scale], the limiting factor is the length of the electrode in the functional area. The functional area is determined by the minimum size of the droplets and delivery accuracy of the inkjet which is currently a diameter of ~200 μm. A more precise inkjet printer or ink delivery method is required for frequencies higher than 20 kHz.

8.5 CMOS EGTs[3]

Complementary metal oxide semiconductors (CMOS) based circuits have less power consumption and higher gain in theory. In order to have the CMOS EGT library complete, a p-type metal oxide semiconductor (PMOS) working with ion gel is required. However, PMOS options are very limited and their electrical properties are not as good as n-type metal oxide semiconductors. The most common PMOS is based on Cu_2O. Commercial inks for CuO are available through NovaCentrix with reported TFT mobility of 0.4 cm^2/Vs.[215]

[3] In collaboration with Jacob Dalhoff

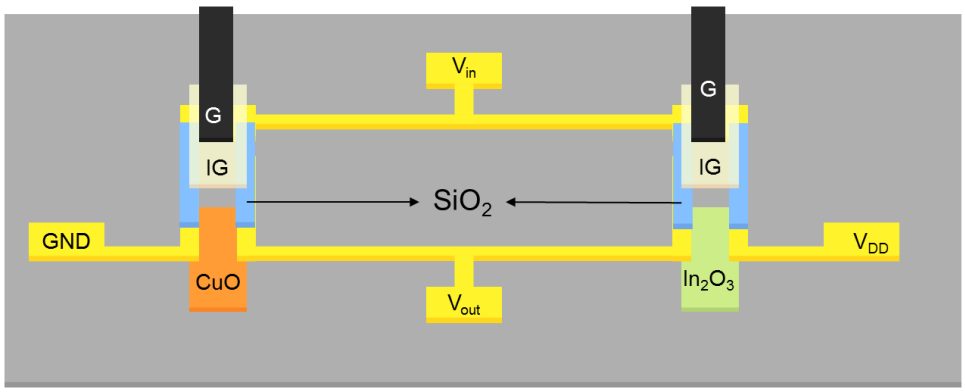


Figure 8.5.1. The CMOS EGTs. The metal oxide films where printed and annealed prior to electrode deposition. The ion gel and PEDOT:PSS gate are deposited by AJP.

Figure 8.5.1 suggests a device fabrication strategy for CMOS EGTs where the parasitic capacitance is reduced dramatically. The NMOS EGTs such as ZnO and In_2O_3 with mobilities of ~ 2-10 cm^2/Vs were reported, previously.

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Appendix

A1. Robust Cut-and-Stick poly(lactide) Ion Gels via Facile One-Pot Room Temperature Curing: Ion Gel as an Iono-elastomer for Strain Sensing Application.[4]

A1.1 Introduction

An ion gel is commonly defined as a polymer network swollen with a large amount of an ionic liquid (IL).[216] Since its introduction, a great amount of research effort has been devoted concerning both fundamental[3,72,217–220] and applied[2,77,137,221–226] aspects of the class of materials due to their convenient integration into solid state electronic devices arising from the mechanical integrity of the polymer network in combination with the excellent electrochemical properties from the IL. In terms of mechanical property, it is desirable for those highly plasticized ion gels to have a high toughness[73] to allow for the easy-handling of the materials at a thin-film scale for device fabrication[181,227] as well as applications in stretchable electronics[76,228,229] or electromechanical actuators.[230,231] The high toughness ion gels have been demonstrated previously through either chemical or physical crosslinking. Chemically crosslinked network ion gels can be achieved by the approach of crosslinking homopolymers or block polymers (BCPs). Chemically-crosslinked homopolymer ion gels have been synthesized via in-situ polymerization of monomers,[70,232] and crosslinking of the two star-shaped macromers with reactive chain ends.[233–235] Chemically-crosslinked

[4] This work was conducted in collaboration with Boxin Tang and Jacob P. Brutman. Boxin Tang did all the synthesis, ion gel formulation, and physical properties characterization. Fazel Zare Bidoky did the device fabrication, iono-elastomer and TFT characterization.

BCP ion gels can be achieved by chemical crosslinking within the micelle cores of the block polymer based ion gels.[73] In the case of physically-crosslinked ion gels, poly(vinylidene fluoride-*r*-hexafluoropropylene) (PVDFHFP)[227] and poly(vinylidene fluoride) (PVDF)[181] have been utilized to form mechanically robust ion gels. The microphase-separated crystalline domains provide high toughness to the resulting ion gels with ~200% of strain-at-break.

In the case of chemically-crosslinked homopolymer-based ion gels, the gel ionic conductivity is close to that of the neat IL, because the vast majority of the gel is the IL-polymer mixture, i.e., the ionically-conducting phase.[234] In the meantime, the chemical crosslinking ensures the high toughness of the ion gel with a strain-at-break well above 200% at 10-20 wt.% polymer.[235,236] In the previous reports, the hydrophilic poly(ethylene glycol) (PEG)-based star-shaped macromers were explored. The tetra-arm PEG polymers were first end-functionalized into two types of macromers that can react with each other. Subsequently, the macromers were allowed to crosslink with the presence of IL. While PEG has a low T_g that promotes fast ion conduction, water absorption can negatively impact the electrochemical stability of ILs[237] as well as organic semiconductors.[238] In previous work, poly(ethylene oxide) (PEO)-based electrolyte-gated transistors showed more significant degradation under humidity than that of the hydrophobic poly(ethyl acrylate) (PEA)-based electrolyte-gated transistors.[3]

Poly(lactide) (PLA) is a hydrophobic and degradable polymer that can be synthesized from renewable feedstock.[239–241] With two decades of development on the industrial production of PLA, the polymer can be produced with only 15−25% of extra cost from poly(ethylene terephthalate) (PET), a price range that makes PLA competitive for replacing

petroleum-based polymers in our daily use.[242] The initiator for the ring-opening transesterification polymerization (ROTEP) of PLA is commonly an alcohol, which makes PLA into star-shaped polyol macromer a convenient synthesis.[243] Hillmyer *et al.* have reported a straightforward synthesis of a star-shaped amorphous PLA vitrimer by reacting star-shaped hydroxyl-end functionalized PLA with methylenediphenyl diisocyanate (MDI) using Tin(II) 2-ethylhexanoate ($Sn(OCT)_2$) as both crosslinking and ROTEP catalyst.[244] Interestingly, PLA has also shown good compatibility with ILs.[74,245] A PLA-based ABA triblock polymer has recently been shown to form self-assembled micellar crosslinks in a low toxicity IL, 1-butyl-4-methylpyrrolidinium bis(trifluoromethanesulfonyl)imide ($[P_{14}][TFSI]$).[74]

Here, we adopt the facile approach of crosslinking tetra-arm hydroxy-terminated PLA and the MDI with the presence of two commonly used ILs, i.e., 1-ethyl-3-methylimidazolium bis(trifluoromethanesulfonyl)imide ([EMI][TFSI]) and $[P_{14}][TFSI]$. In this way, mechanically robust ion gels can be achieved under room temperature through a one-pot reaction with dichloromethane as the co-solvent. Because of the chemical crosslinks, the resulting ion gel at as low as 20 wt.% polymer is mechanically robust with a strain-at-break of over 200% and a stress-at-break of 0.5 MPa. Thin film ion gels at 20 wt.% polymer can be conveniently laminated onto transistor devices via a cut-and-stick approach and the ionic conductivity of the ion gels achieved a three-time increase than that of the PVDFHFP ion gels because of the lack of ion-insulating crystalline domains. In addition, the bulk ion gels have demonstrated excellent electromechanical response with a high sensitivity in resistance change with respect to a change in strain (e.g., five times change in resistance at 140% strain) and a low hysteresis (less than 0.03%).

A1.2 Experimental Procedures

Materials. Pentaerythritol (PERYT), methylenediphenyl diisocyanate (MDI) and tin(II) 2-ethylhexanoate ($Sn(OCT)_2$) were purchased from Sigma-Aldrich, stored in a glovebox under N_2 atmosphere and used as received. D,L-Lactide was provided by Altasorb stored in a glovebox under N_2 atmosphere and used as received. 1-ethyl-3-methylimidazolium bistrifluoromethanesulfonylimide ([EMI][TFSI]) was synthesized following a reported literature.[246] 1-butyl-1-methylpyrrolidinium bistrifluoromethanesulfonylimide ($[P_{14}]$[TFSI]) was purchased from Sigma-Aldrich. Poly(styrene sulfonate) (PEDOT:PSS) was purchased from H. C. Starck. Poly(3-hexylthiophene) (P3HT) was purchased from Rieke Metals. Anhydrous In_2O_3 was purchased from Sigma-Aldrich.

Synthesis of hydroxyl-terminated star-shaped poly(D, L-lactide) (tetra-arm PLA). $Sn(OCT)_2$ (0.005 eq., 0.014 g, 0.35 mmol) was dissolved in a minimal amount of toluene (*ca.* 0.5 mL) and charged in a pressure vessel, along with D, L-lactide (25 eq., 25 g, 175 mmol) and PERYT (1 eq., 0.8 g, 7 mmol) (Figure A1.2). The reaction mixture was heated to 160 °C for 3 h, then allowed to cool to room temperature and dissolved in an approximately equal volume of dichloromethane (DCM). The subsequent solution was precipitated in ethanol (*ca.* 10 times volume of product solution), redissolved in an approximately equal volume of DCM and reprecipitated in hexanes (10 times volume of DCM solution). The resulting polymer was then dissolved in DCM, transferred to a polypropylene container and dried with N_2 flow for approximately 24 h. The polypropylene container was then put in a vacuum oven at approximately 60 °C and 20 mTorr for 72 h,

and subsequently cooled to room temperature. The resulting polymer was obtained in an 80% isolated yield.

Molecular Characterization. The dispersity and molecular weight was obtained using MALLS-SEC (Agilent 1260 Infinity series SEC system with a Wyatt Technology Dawn Heleos-II MALLS detector and a Wyatt Optilab TrEX refractive index detector) with tetrahydrofuran (THF) as eluent at 1 mL/min flow rate at 25 ^{o}C and ^{1}H NMR spectroscopy (Bruker Avance III HD 500) at 25 ^{o}C in $CDCl_3$.

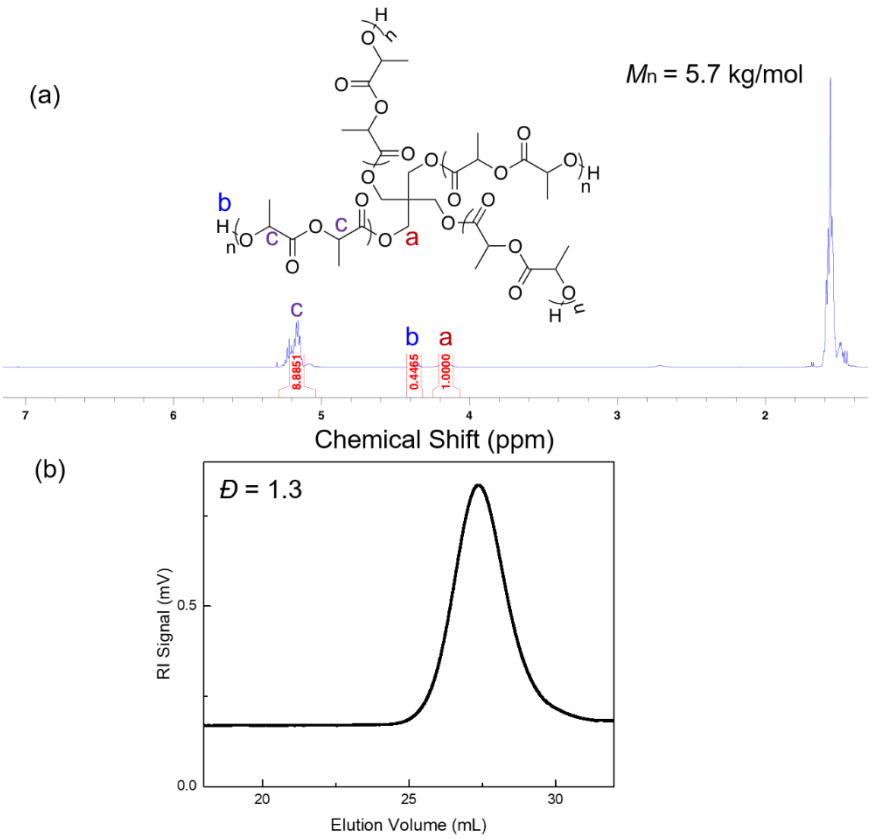

Figure A1. 1. (a) NMR of the tetra-arm PLA. (b) SEC trace of the tetra-arm PLA.

Ion Gel Preparation. For bulk ion gel samples, tetra-arm PLA (1 eq., 0.5g-scale), MDI (1.1 eq.) and IL (50-80 wt%) were dissolved in 3 ml of DCM. A stock solution of $Sn(OCT)_2$ in DCM was prepared (100 mg catalyst in 10 ml of DCM) and 0.005 mol ratio of $Sn(OCT)_2$:OH, was added to the fully dissolved HTSPLA, MDI and IL solution. After complete mixing, the resulting solution was poured into a polypropylene jar (125ml). The jar was covered with aluminum foil and left under N_2 purge at room temperature overnight. Then, the sample was further dried in a vacuum oven (~100 mTorr) at room temperature for 48 h. Poly(styrene-*b*-ethyl acrylate-*b*-styrene) (SEAS)-[EMI][TFSI] ion gel samples for extensional rheometry measurements were prepared by dissolving SEAS polymer (20-50 wt.% relative to the IL) and the IL in DCM and dried under N_2 purge in 5 ml glass Petri dishes and subsequently dried under vacuum (~100 mTorr) for 24 h at 80 ºC. The resulting ion gel film was then delaminated from the jar and rectangular shaped samples for extensional rheology were then cut at the dimension of *ca*. 0.7 mm (thickness) × 3 mm (width) × 20 mm (length). Samples for impedance spectroscopy were cut in circular shape at the dimension of *ca*. 4 mm of diameter. Thin ion gel samples that were cut-and-stick onto electronic devices were prepared in a similar manner using a reduced amount of chemicals (~ 0.1g of PLA scale). After drying, the resulting films were cut at a dimension of *ca*.1 cm diameter and 86 μm of thickness.

Determination of T_g. Differential scanning calorimetry (DSC) measurements of ion gels were carried out using a TA Instruments Q1000 DSC with liquid N_2 cooling capability. A sample of 5−10 mg was contained in a hermetically sealed aluminum pan. The samples were initially heated up to 60 ºC and annealed for 5 min to erase prior thermal history, and

then cooled rapidly to −150 ºC. Subsequently, they were heated to 160 ºC at 10 ºC/min. Glass transition temperatures were acquired from the second heating curves.

*Extensional Rheology of Ion Gels.*Extensional rheological measurements were performed on an ARES-G2 rheometer (TA Instruments) using an extensional viscosity fixture. Ion gel samples were cut at the dimensions described in the previous section and carefully lifted out of the petri dish. They were then loaded onto the fixture in between the drums (length = 13 mm). The thickness and the width of the samples were measured by the caliper. Tests were conducted at 30 °C, and the temperature was controlled using an environmental temperature controller under a nitrogen atmosphere. The sample was stretched at a constant Hencky strain rate = 1 sec^{-1}, and the instrument measured the resulting extensional stress until the sample broke.

Impedance Spectroscopy of Ion Gels. For ion gels, impedance spectroscopy was conducted using a two-point probe on a Solartron 1255B frequency response analyzer connected to a Solartron SI 1287 electrochemical interface. Samples were initially cut as described in the previous section, and sandwiched in a Teflon spacer of 4 mm diameter and 2 mm thickness between two stainless steel electrodes. During a measurement, the sample was kept at 30 ºC for 1 h before measurement and the sample temperature was controlled by a custom-built heating stage with a temperature feedback loop monitored by an independent thermocouple placed next to the sample. The ionic conductivity, σ, was calculated as $\sigma = l/Ra$, where l is the sample thickness, a is the superficial area of the sample, and R is the bulk resistance determined from the real part of the impedance, Z', in the high-frequency plateau.

Gel Fraction Determination of Ion Gels. The gel fraction of ion gels was determined by placing a small amount of the crosslinked ion gel sample (~ 50 mg) in a scintillation vial filled with DCM. The vial was close-capped and placed in a reaction hood with good ventilation for 24 h of swelling and the DCM was poured out and refilled once and the sample was allowed for swelling for another 24 h. The majority of the DCM was then poured out and the vial was then further-dried under vacuum (~ 100 mTorr) at 60 ºC for 24 h. The dried solid sample was then weighed. The gel fraction was then calculated as the ratio between the amount of solid after solvent extraction and the amount of solid initially added to make the ion gel sample.

P-Type and N-Type EGT Devices Fabrication and Testing. Source, drain and gate electrode contacts were patterned on a silicon wafer by photolithography with 5 nm of chromium and 30 nm of gold. The semiconductor channel width to length ratio was 100. The p-type semiconductor, P3HT (Rieke Metals Inc.), was dissolved in chloroform/terpineol (9:1 weight ratio) at a concentration of *ca.* 1 mg/mL. The n-type semiconductor, In_2O_3, was dissolved in acetonitrile at 0.02 M concentration and was subsequently sonicated for 15 min. The ion gel was prepared as mentioned in the previous section. The gate electrode, poly(3,4-ethylenedioxythiophene) poly(styrene sulfonate) (PEDOT:PSS) (H.C. Starck) in a 1.5 wt.% aqueous solution, was dissolved in ethylene glycol at 6 wt%. The silicon wafer with patterned contacts was first treated with O_2 plasma for 15 min to increase printed inks' wettability. The In_2O_3 was first printed using a commercially available aerosol ink jet printer (Optomec, Inc.). The substrate was then annealed at 400 ºC for 1h. After annealing, the P3HT was printed on the substrate. Then, the ion gel (~100 μm thickness) was cut into 1 cm diameter circular and laminated onto the

substrate, covering the semiconductor. PEDOT:PSS top gates were printed on top of the ion gel layers. The substrate was placed in a vacuum oven and dried (~100 mTorr) at room temperature for 24 h. Transistor measurements were conducted in a glovebox using Keithley 2400 and Keithley 2611B electrometers.

Electro-Mechanical Response Characterization of Ion Gels. To characterize the electromechanical response of an ion gel sample, the sample was first cut into a rectangular shape as described in the previous section. Then, the sample's thickness and width were measured by a caliper. After the cross-sectional area of the sample was measured, the two ends of the ion gel sample were taped by conductive tapes onto aluminum sample holders. Subsequently, the sample holders were fixed onto the two pressure clamps of the tensile tester and were insulated by placing PLA spacers between the clamp grips and the sample holders. Before a tensile measurement, the tensile tester was properly zeroed and the initial gauge length was measured. The two ends of the sample were connected at the conductive tape area to a Keithley 2612 electrometer. During a measurement, at a certain strain, an oscillating voltage from 0 to 1 V was passing through the sample at various sweep rates and the current was recorded.

A1.3 Discussion

A1.3.1 Synthesis of Ion Gels

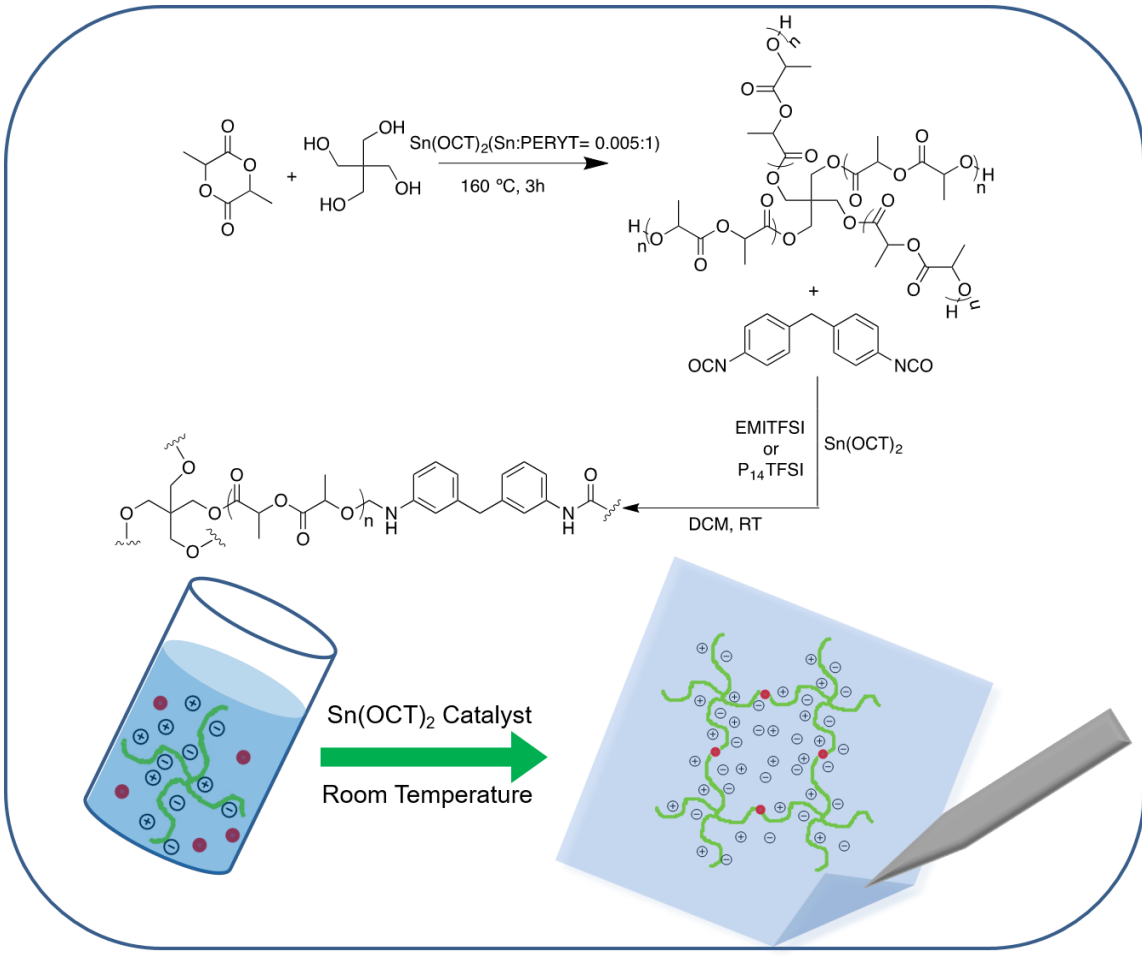

Figure A1.2. Synthetic route of the tetra-arm PLA-based ion gels with a cartoon illustration of the ion gel curing process.

For the synthesis of the ion gels, the tetra-arm PLA was first synthesized by ROTEP following a previous literature[244] with commercially available chemicals that were used as received. To make ion gels, the IL, tetra-arm PLA, MDI were initially dissolved with minimum amount of DCM as the co-solvent (0.5 g of polymer in 2.5 ml of co-solvent). The stock solution of $Sn(OCT)_2$ was then micropipetted into the well-dissolved curing solution. The solution was subsequently cured in air for 12 h and further dried under vacuum for 24 h, which was under room temperature throughout.

The DSC traces of the tetra-arm PLA-[EMI][TFSI] ion gels are shown in Figure A1.3. As PDLLA is miscible with the IL, the ion gel traces show a single glass transition temperature in between the glass transition temperatures of the pure IL (~ 92 ºC) and polymer (~ 40 ºC). The glass transition temperature increase with polymer concentration because of the increase in the content of the high T_g polymer.

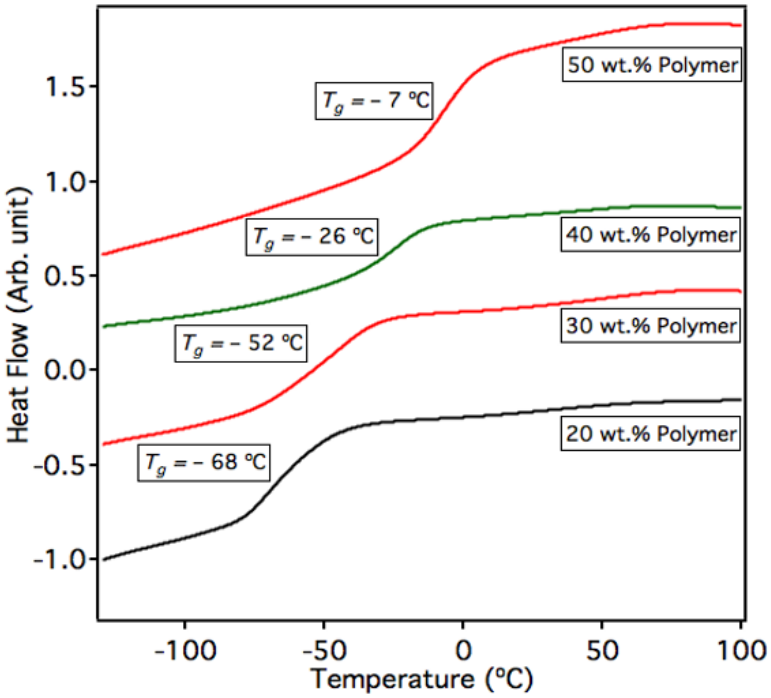

Figure A1.3. DSC traces of tetra-arm PLA-[EMI][TFSI] ion gels.

The gel fraction was determined for the resulting ion gels of various polymer loading. As shown in Figure A1.4, the gel fractions of ion gels from 20−50 wt.% polymer concentration are above 95 %, indicating that majority of the polymer participates in the network. The chemical crosslinking reaction is highly efficient even with the presence of IL and room temperature processing temperature, reaching above 98% for a highly swollen network of only 20 wt.% polymer.

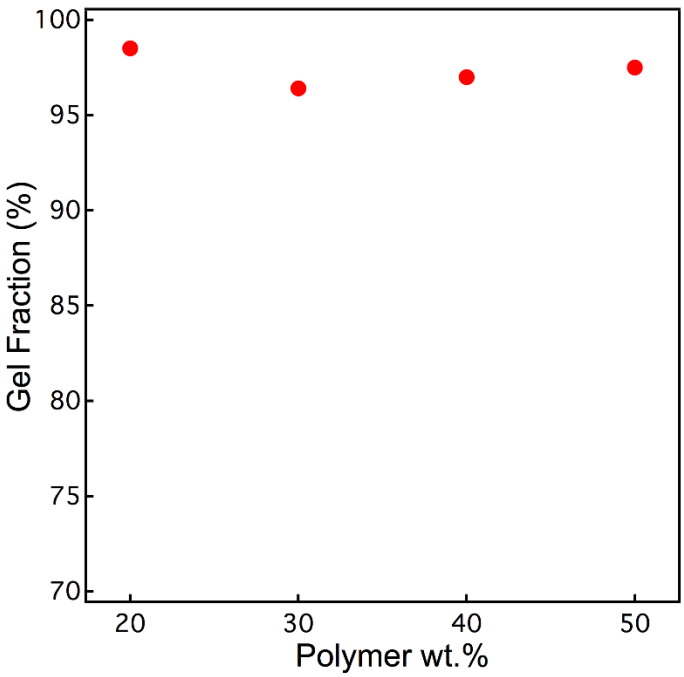

Figure A1.4. Gel fraction of tetra-arm PLA ion gels of various polymer concentrations.

A1.3.2 Mechanical Property of the Ion Gels.

The tensile properties of the ion gels are characterized on an ARES G2 (TA Instruments) using an extensional rheometry following procedures from a previous literature on similar systems.[73] The experimental setup is shown in Figure A1.5a. Since the ion gels are formed with two ionic liquids that are soluble in PDLLA, the stress-strain relationships of 20 wt.% tetra-arm PLA ion gels in $[P_{14}]$[TFSI] and [EMI][TFSI] were shown in Figure A1.5b. The stress-strain relationships of the two kinds of ion gels are similar, indicating the network formation is not affected by the choice of IL. The stress-strain relationships of the tetra-arm PLA-based ion gels and the poly(styrene-*b*-ethyl acrylate-*b*-styrene) (SEAS) triblock polymer-based ion gels. For the SEAS ion gels, the samples with lower midblock size demonstrate a steeper increase in stress with increasing

strain. From the previous report, the modulus of the ion gel at the same polymer loading increases with decreasing midblock molecular weight.[3] Thus, it is reasonable to expect a "stiffer" response in stress with respect to increasing strain. On the other hand, the stress-strain response of the tetra-arm PLA ion gel shows a drastic difference with a significantly higher stress-at-break compared to those of the SEAS ion gels. The difference likely arises from the chemical crosslinks in the tetra-am PLA ion gel as the failure mechanism changes from the physical chain-pullouts in the SEAS ion gels to the breaking of chemical linkages in the tetra-arm PLA ion gel. The toughness of the ion gels is compared in Figure A1.5d. The toughness of the chemically crosslinked ion gels reaches ~ 7-fold increase compared to that of the SEAS ion gel at 20 wt.% polymer concentration. Compared to the other method of increasing the mechanical toughness of the ABA triblock ion gel systems, this method uses less than 10 wt.% (based on the mass of polymer) of crosslinker, which is less than half of the fraction of polystyrene in the chemically-crosslinkable poly(styrene(azide)-*b*-ethylene oxide-*b*-styrene(azide)) (SOS-N_3) polymer.[73] As a result, the fraction of the ion-conducting phase in the tetra-arm PLA ion gel is larger compared with that of the SOS-N_3, which promotes high ionic conductivity.

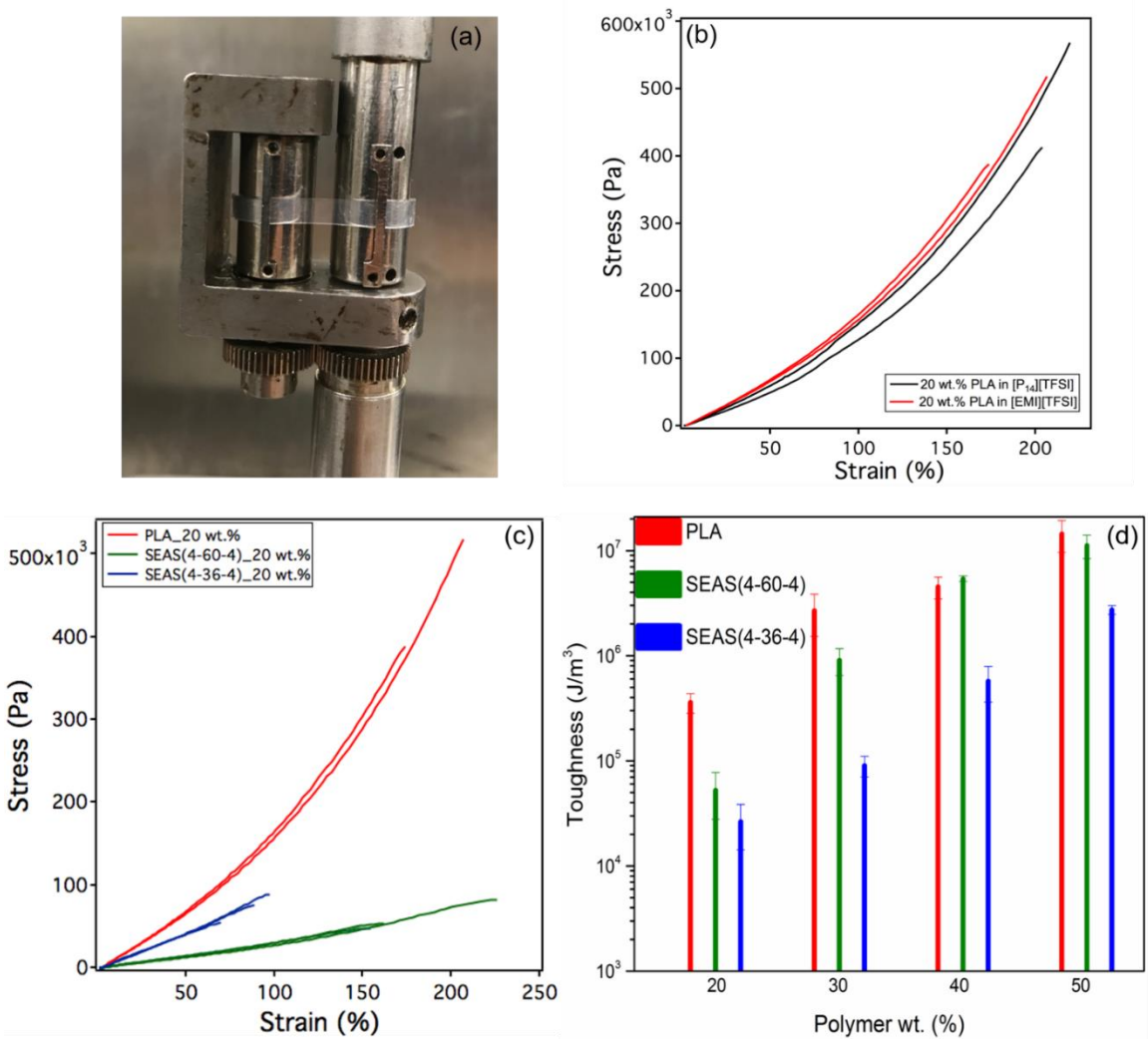

Figure A1.5. (a) A photo of a sample ion gel loaded onto the extensional fixture. (b) Stress-strain relationship comparison of 20 wt.% polymer tetra-arm PLA ion gels with $[P_{14}][TFSI]$ and [EMI][TFSI]. (c) Stress-strain relationship comparison of 20 wt.% polymer tetra-arm PLA, SEAS(4-60-4), and SEAS(4-36-4)-based ion gels. (d) Toughness comparison of the tetra-arm PLA, SEAS(4-60-4), and SEAS(4-36-4)-based ion gels at various polymer concentrations.

A1.3.3 Ionic Conductivity of the Ion Gels

The ionic conductivity at 30 ºC of the tetra-arm PLA ion gels, ABA triblock polymer ion gels and the PVDFHFP ion gels are shown in Figure A1.6 and the IL is [EMI][TFSI]. The tetra-arm PLA showed improved conductivities at polymer concentrations from 20−50 wt.% compared to those of the previously reported poly(styrene-*b*-methyl methacrylate-*b*-

styrene) (SMS) triblock polymer ion gels.[72] From the VFT equation shown in previous chapters, the lower the T_g of the IL-polymer mixture, the higher the ionic conductivity of the mixture. Because the T_g of the IL-soluble polymer is often higher than that of the IL, the T_g of the polymer needs to be low to ensure a low T_g of the IL-polymer mixture. Since the T_g of PLA is ~50 ºC lower than that of the poly(methyl methacrylate) (PMMA), the ion motion is less hindered in the tetra-arm PLA ion gels, and thus it is reasonable that the tetra-arm PLA ion gels show higher conductivities. In addition, since the conducting phase of the PLA ion gels is crosslinked by molecular crosslinks that take up about half of the fraction of the polystyrene physical crosslinks in the ABA triblock polymer, the ion-conducting phase fraction is significantly larger in the tetra-arm PLA ion gels, which contributes to a high ion conductivity. As a result, at polymer concentration of as low as 20 wt.%, the tetra-arm PLA ion gels show similar ionic conductivity as that of the SEAS and SOS ion gels. Even though the IL-soluble polymer blocks, PEA and PEO, of the two triblock polymers have a significantly lower T_g compared to PLA, the smaller fraction of the ion-insulating phase in the tetra-arm PLA ion gel ensures the similar conductivity between PLA and SEAS/SOS ion gels at lower polymer concentrations where the T_g of the ion-conducting phase is less influenced by the added polymer. On the other hand, the ionic conductivity of the tetra-arm PLA ion gels is also significantly higher than that of the PVDFHFP ion gels, another type of the cut-and-stick ion gel. At 20 wt.% polymer, a concentration relevant to the application of EGTs, the conductivity of the tetra-arm PLA ion gels is a factor of two higher than PVDFHFP ion gels of the same polymer concentration. The difference in conductivity may result from the tortuous ion pathways formed by the PVDF crystalline domains in the PVDFHFP ion gels.[247,248]

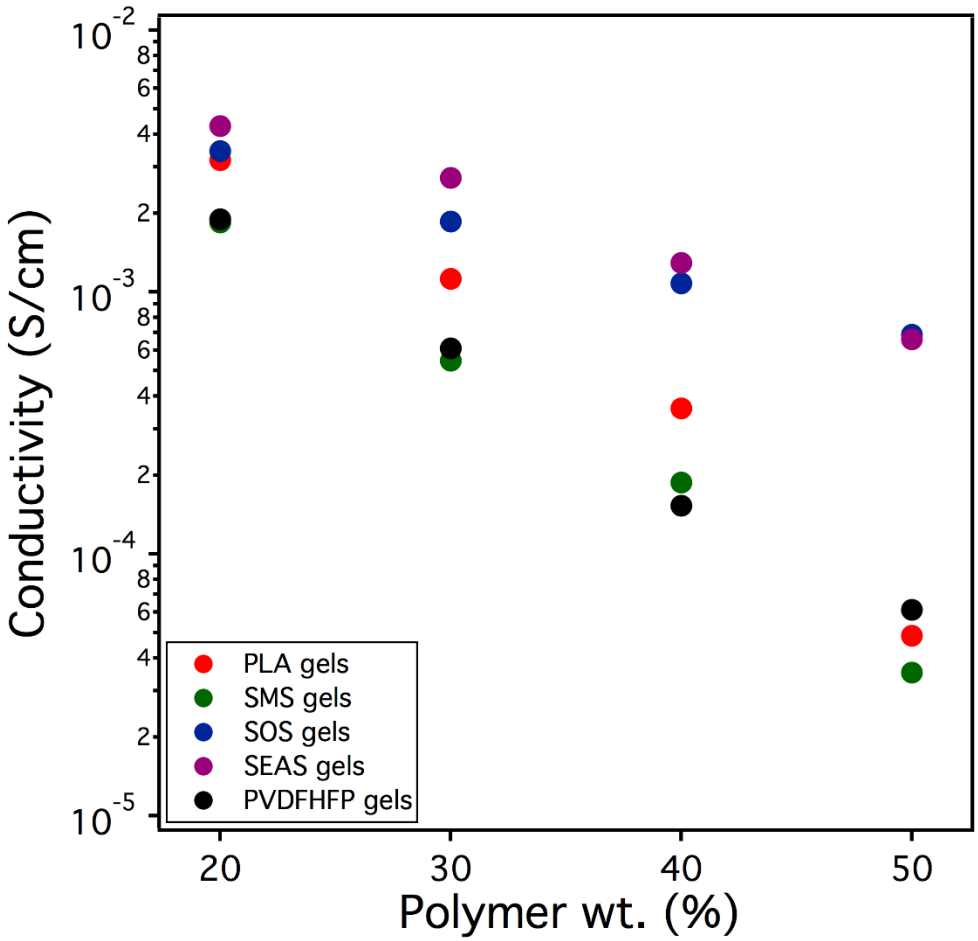

Figure A1.6. Ionic conductivity comparisons of tetra-arm PLA ion gels, ABA triblock polymer ion gels and PVDFHFP ion gels at various polymer loading with [EMI][TFSI] as the IL . (Refs. [72] and [3])

A1.3.4 P-Type and N-type EGTs by Ion Gels via a Cut-and-Stick Method.

Since all the reactants have negligible vapor pressure compared to the method of in-situ polymerization and the chemical crosslinking reaction can readily happen at room temperature, the tetra-arm PLA based ion gels can be conveniently made into thin films by changing the amount of materials and subsequently be laminated onto EGT devices owing to the excellent mechanical properties. As a result, both P- and N-type EGTs have been fabricated with the tetra-arm PLA-[P_{14}][TFSI] ion gel. The cross-section illustration of a

P3HT device example is shown in Figure A1.7a. Both the P- and N-type semiconductors were aerosol-jet printed on the patterned substrate. The width of the semiconductor channel (W) is 2000 μm and the length of the semiconductor channel (L) is 25 μm After annealing, the 20 wt.% polymer ion gel of ~86 μm thickness was conveniently laminated on top of the semiconductor layer. Then, the PEDOT:PSS top gate was printed on top of the ion gel layer. The transfer curves of the two kinds of EGT devices are shown in Figure A1.7c and d. Because of the high capacitance of the ion gel (~ μF/cm^2), both types of EGTs show low voltage operation (~1V) and a high ON/OFF current ratio of ~10^5.

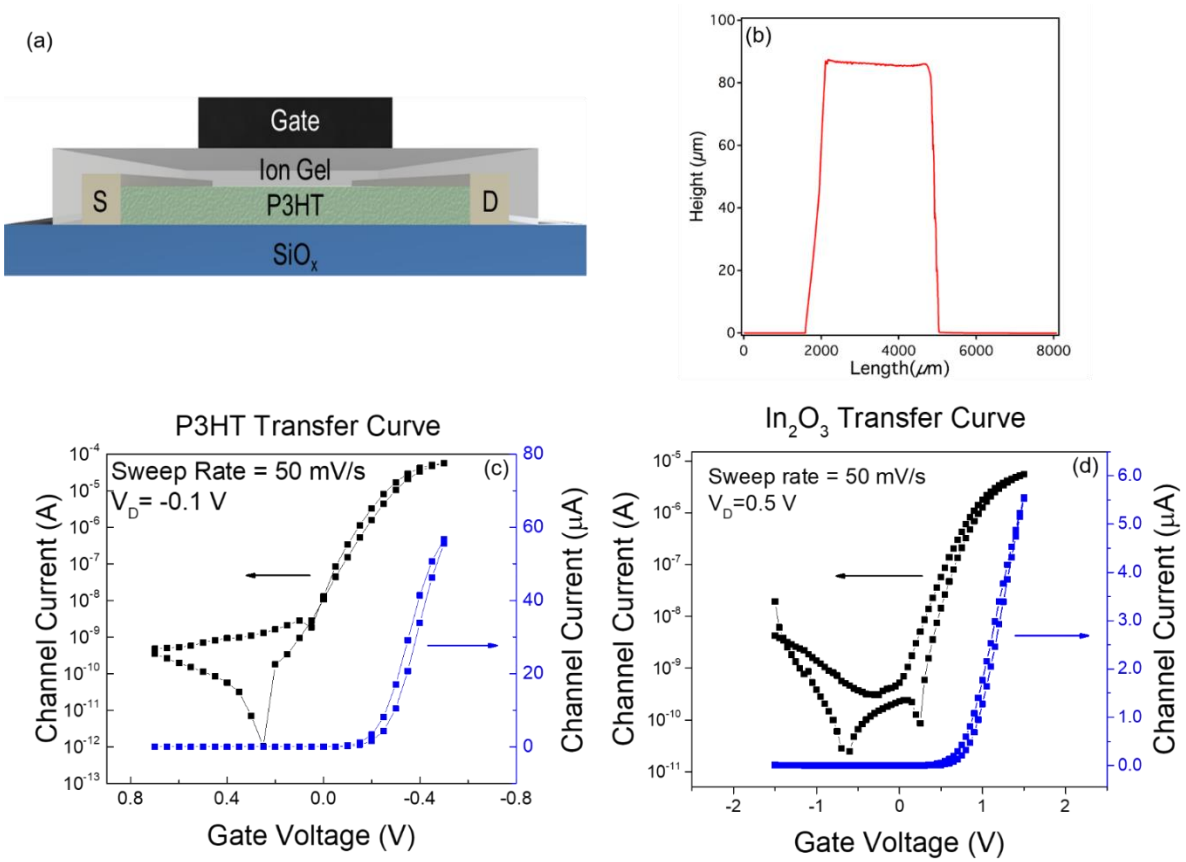

Figure A1.7. (a) Cross-sectional illustration of an example P3HT cut-and-stick EGT device structure. (b) The height profile of a typical cut-and-stick ion gel (~86 µm thickness). (c) The transfer curve of a P3HT EGT with the cut-and-stick ion gel. (d) The transfer charcteristics of an In_2O_3 EGT with the cut-and-stick ion gel.

A.1.3.5 Electro-mechanical Response of the Ion Gels

Because of the good electrical property of the IL, various efforts have been devoted to utilizing the electro-mechanical responses of the class of material in strain sensing applications for biological applications.[76,228,229] Chemically crosslinked networks were often used to provide the stretchability of the resulting IL-polymer composites.[76,228,229] Because of the demonstrated good mechanical properties of the tetra-arm PLA ion gels, the electro-mechanical response of the ion gels were investigated. For the choice of IL, $[P_{14}][TFSI]$ was used as the electrolyte because of its low toxicity nature. Many of the previous reports studied the change of resistance with respect to strain of such materials by measuring the ohmic resistance.[76,228,229] Because of the high electrical double layer capacitance of the ion gels, the ohmic response of this class of materials is affected by the charging of the electrical double layer. Consequently, the displacement current method was used to characterize the resistance of the ion gel. In this method, the voltage was swept from 0V to 1V and back to 0V for one cycle and each cycle was swept at a different sweeping rate, the recurrent *I* can be expressed as

$$I = c\frac{dV}{dt} + \frac{V}{R} \tag{A1.1}$$

where *V* is the applied voltage, $\frac{dV}{dt}$ is the voltage sweep rate and *R* is the ohmic resistance between two measuring electrodes. From the Equation A1.1, the current at a certain applied voltage is linearly dependent upon the voltage sweeping rate and the resistance can be calculated from the y-intercept of current versus sweep rate. A typical current versus sweep rate relationship for the tetra-arm PLA is shown in Figure A1.8a and the voltage change with respect to time is shown in Figure A1.8b. The fastest sweep rate translates to a

sweeping frequency of as low as ~ 0.2 Hz, and thus the electrical double layer capacitance can be regarded constant at such a low frequency. Consequently, the slope of the linear relationship shown in Figure A1.8a is the electrical double layer capacitance of the ion gel and the resistivity of the ion gel can be calculated from the y-intercept as illustrated in Equation A1.1. The resistivity change of the tetra-arm PLA ion gel versus strain is shown in Figure A1.9b. Since the ion gel consists of homogeneous IL-PLA mixture with negligible-size chemical crosslinks, the resistivity change with strain shows a continuous changing trend with a 4-fold resistivity change at strain of 140%. As the ion gel was unloaded to original state, the resistivity was also measured that showed excellent overlap with the resistivity change of the ion gel upon stretching, showing a difference of as low as 0.03%. The low hysteresis of resistivity change between stretching and un-stretching is particularly beneficial to the application of the ion gel in strain sensing as the ion gel can actively capture the strain change without influence by strain history.

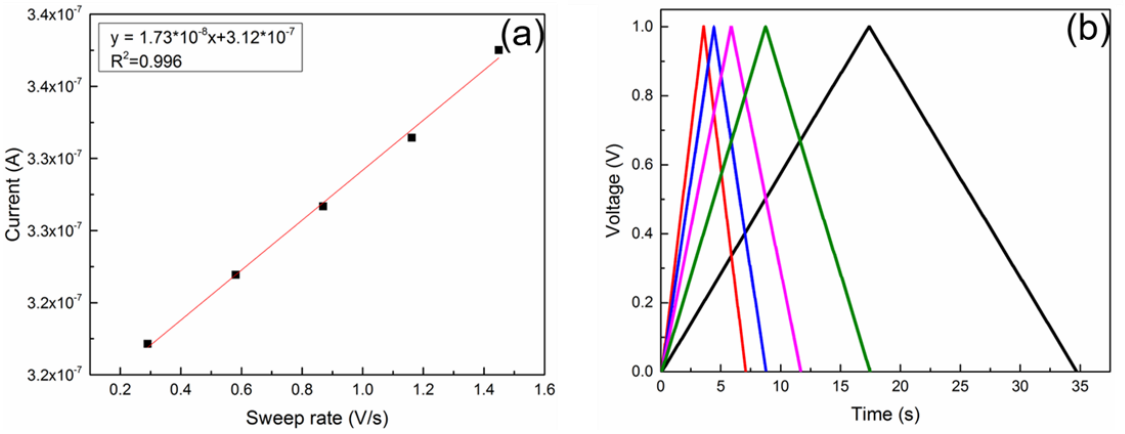

Figure A1.8. (a) A representative plot of current at the chosen voltage versus voltage sweep rate with linear fit, the slope as capacitance and the y-intercept as gel resistance. (b) Voltage change at each sweep rate versus time.

A1.4 Conclusions

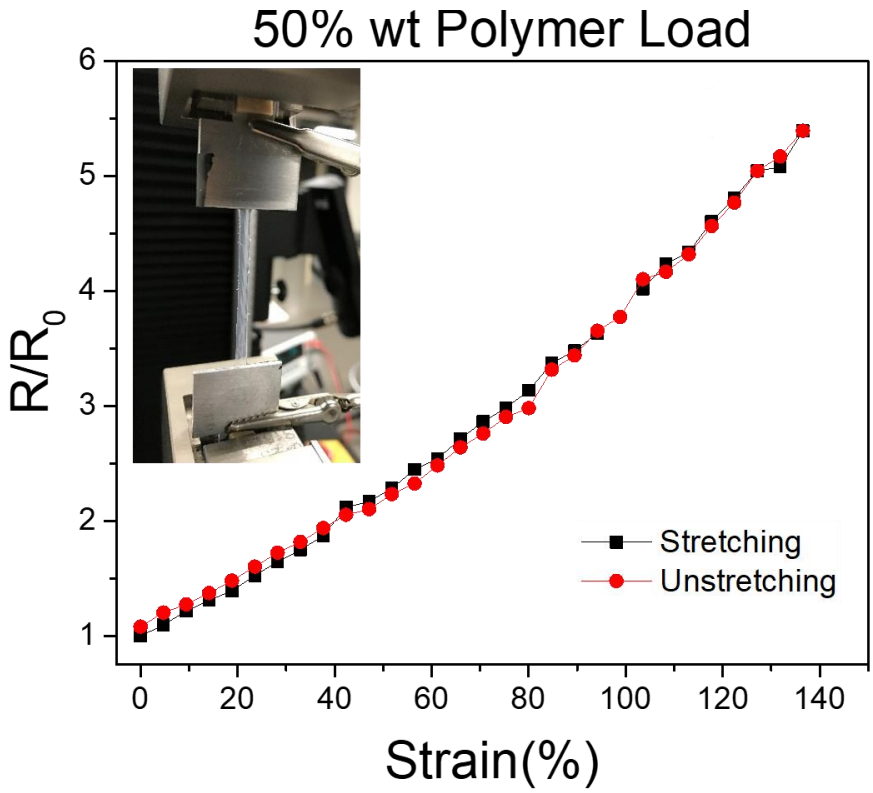

Figure A1.9. Change of resistance of 50 wt.% of tetra-arm PLA-[P_{14}][TFSI] ion gel normalized with initial resistance versus strain during stretching and un-stretching. The inset photo shows an ion gel sample during the test.

In conclusion, we demonstrate a facile method of crosslinking tetra-arm hydroxy-terminated PLA and the MDI with the presence of [EMI][TFSI] and [P_{14}][TFSI] to form chemically crosslinked ion gels in an one-pot approach. The resulting ion gel at as low as 20 wt.% polymer is mechanically robust with a strain-at-break of over 200% and a stress-at-break of 0.5 MPa. Because of the stretchability of this kind of material, thin film ion gels can be conveniently laminated onto transistor devices via a cut-and-stick approach and the ionic conductivity of the ion gels achieved a two-fold increase than that of the PVDFHFP ion gels because of the lack of ion-insulating crystalline domains. The bulk ion gels have also demonstrated excellent electromechanical response with a high sensitivity in

resistance change with respect to a change in strain (e.g., five times change in resistance at 140% strain) and a low hysteresis (less than 0.03%).

A2 Supporting information for Chapter 5

Cut-off frequency terminology. There are different ways to quantify dynamic performance by defining different types of working frequencies. The cut-off-frequency defined here can be also approached by investigating the maximum output voltage versus frequency on a semi-log plot. The cut-off frequency ($f_{cut-off}$) is then defined as the point where the maximum voltage output (V_{out}/V_D) drops linearly with input frequency increase on a log scale, Figure S1a.[249]

In some literature, the term transfer frequency ($f_T = 1/(t_{spike-on} + t_{spike-off})$) is used instead of cut-off-frequency and it is roughly two times of $f_{cut-off}$.[110,249,250]

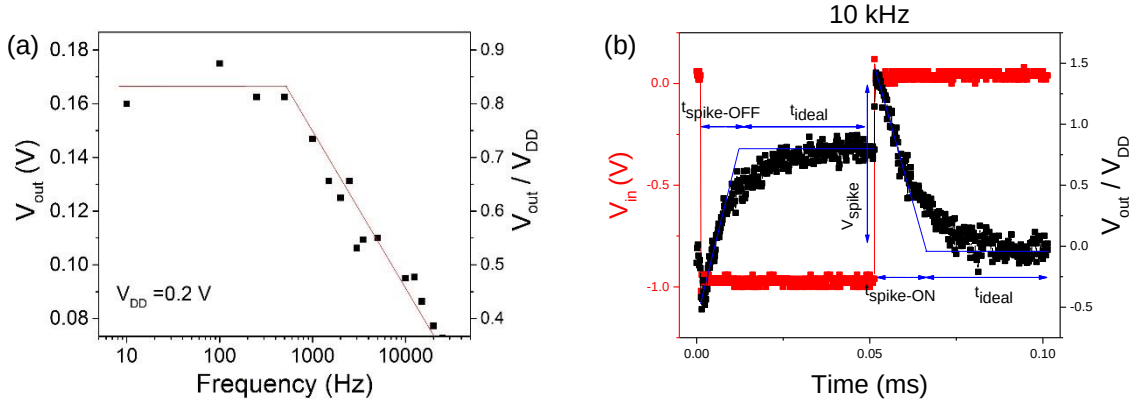

Figure A2.1. Different working frequency terminology. a) Cut-off frequency defined as the frequency where the linear drop starts (W=400 µm, L=20 µm, and a=5 µm). b) The transfer frequency defined at the point the response period is equal to summation of both non-ideality times (times to transfer from non-ideal to ideal response).

Aspect ratio (W/L) effect on dynamic performance. Figure A2.2 shows the results of a scaling experiment in which both channel width (W) and length (L) were varied, keeping the aspect ratio constant ($W/L = 20$). It is clear from Figure A2.2 that $f_{cut-off}$ is higher for the smaller channel width (W) and smaller overall footprint and W/L does not affect $f_{cut-off}$.

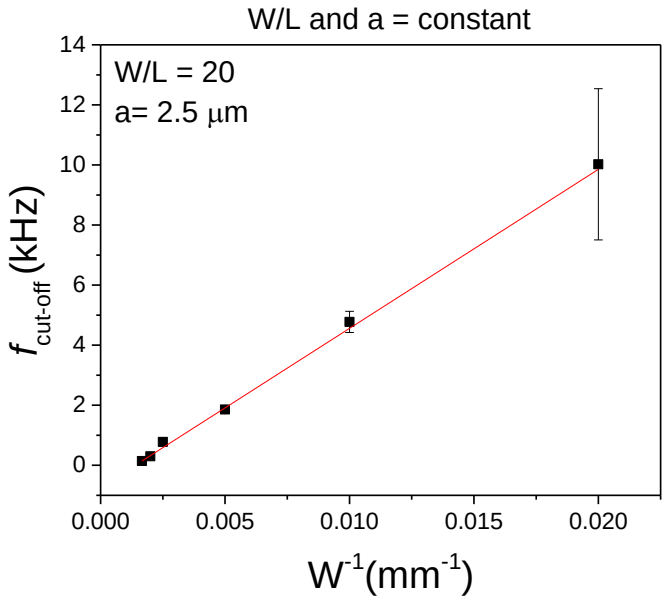

Figure A2.2. Geometrical scaling effect on $f_{cut\text{-}off}$ at fixed *W/L*.

Resistor-loaded P3HT EGT Equivalent Circuit Analysis. A resistor-loaded EGT inverter is shown in Figure S3a. The ion gel between gate and source/channel/drain is modeled by 3 capacitors[251]. The channel can be modeled by two variable resistors. The output potential (V_{out}) is the product of the resistance load (R_L) and the output current ($I_{D\text{-}out}$), Equation A2.1.

$$V_{out} = I_{D-out} \times R_L \quad \text{(A2.1)}$$

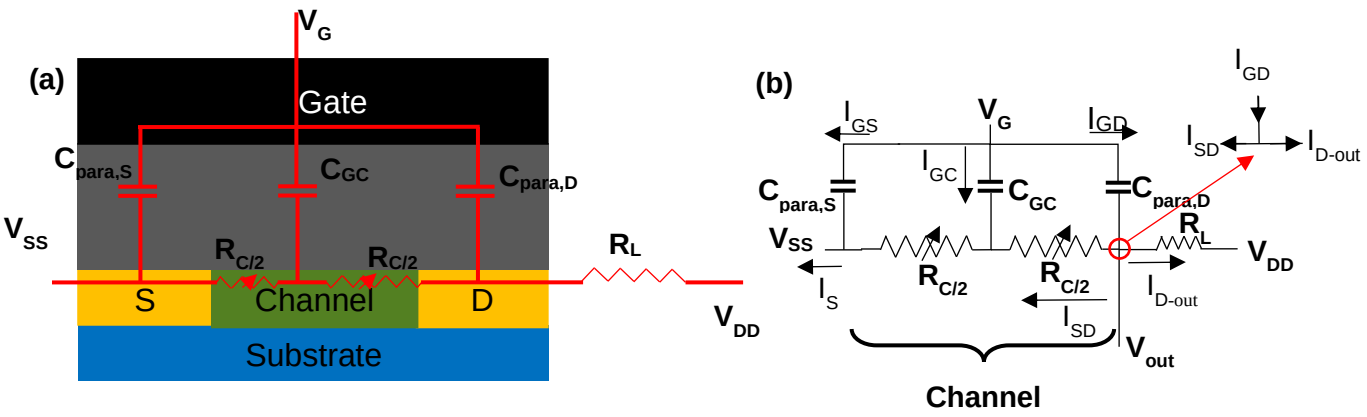

Figure A2.3. A resistor loaded P3HT EGT inverter equivalent circuit. a) The ion-gel film dielectric between gate and source/channel/drain is modeled by three capacitors, $C_{para,S}$/C_{GC}/$C_{para,D}$. The channel is modeled by two equal varying resistors, $R_{C/2}$. The printed PEDOT:PSS as load, is modeled by load resistor. b) The equivalent circuit with the output current node is shown.

Based on the simplified model, Figure S2b, the Kirchhoff current law is derived for the node at the output (V_{out}), Equation A2.2.

$$I_{D-out} = I_{GD} + I_{SD} \tag{A2.2}$$

$I_{D\text{-}out}$ is the output current and I_{GD} is the gate-to-drain current. I_{GD} consists of capacitive current and ohmic current, Equation A2.3.

$$I_{GD} = C_{para,D}\frac{dV_{GD}}{dt} + \frac{V_{GD}}{R_{Ion\ Gel}} \tag{A2.3}$$

$R_{Ion\ Gel}$ is the ion gel bulk resistance. The ohmic current is negligible based on the quasi-static measurements (~10^{-9} A)[94]. Therefore, the capacitive current is the major component of gate-to-drain current in dynamic performance. For the square-wave input, the capacitive current happens at the sharp polarity changes, when V_{in} and V_{out} switch rapidly. The capacitive current is approximately equal to product of parasitic capacitance ($C_{para,D}$) and the abruptness of the voltage step over the gate and the drain electrodes ($\Delta V_{GD}/\tau$), Equation A2.4.

$$I_{GD} \approx C_{para,D} \frac{\Delta V_{GD}}{\tau} \quad \text{(A2.4)}$$

The other term in Equation A2.2, I_{SD}, consists of four currents, the ideal current between source and drain through the channel ($I_{SD\text{-}ideal}$), capacitive gate-to-source current (I_{GS}), capacitive gate-to-channel (semiconductor) current (I_{GC}), and current to source (I_S), Equation A2.5.

$$I_{SD} = I_{SD-ideal} + I_{GS} + I_{GC} - I_S \quad \text{(A2.5)}$$

$I_{SD\text{-}ideal}$ is equal to current measured in quasi-static device performance, Figure 5.2a. When transistor is in OFF state, R_{EGT} is high, and I_{SD} is negligible in comparison to I_{GD}. Even, in ON state, although R_{EGT} is less than R_L (R_{EGT}<0.1R_L), the channel impedance is much larger than the load resistance. Thus, the dominant current in both ON-to-OFF and OFF-to-ON transitions is the capacitive gate-to-drain current, I_{GD}. As a result, I_{GD} is hypothesized to be the most limiting factor in the quasi-dynamic performance, Equation A2.6, which is consistent with Figure 5.

$$V_{spike} = I_{GD} \times R_L \quad \text{(A2.6)}$$

Referring to Equation A2.4, to calculate I_{GD} (and thus V_{spike}), we need $C_{para,D}$. Equation A2.7 outlines the $C_{para,D}$ calculation where the ion gel specific capacitance is $C_{Ion\ Gel}$.

$$C_{Para,D} = C_{Ion\ Gel} A_D \quad \text{(A2.7)}$$

By plugging Equations A2.7 and A2.S4 into Equation A2.6 we obtain Equation A2.8 for V_{spike}:

$$V_{spike} \approx C_{Ion\ Gel} A_D \frac{\Delta V_{GD}}{\tau} R_L \approx R_L C_{para,D} \frac{\Delta V_{GD}}{\tau} \quad \text{(A2.8)}$$

An exponential decay for the spike is assumed. Therefore, spike time, t_{spike} is the relaxation time for the spike. There are two different spike (relaxation) times for ON-to-OFF and OFF-to-ON transitions, $t_{spike\text{-}ON}$ and $t_{spike\text{-}OFF}$, respectively Figure S1b. In the ON-to-OFF transition, $R_{EGT} \gg R_L$ and the only relaxation path is through R_L. In the OFF-to-ON transition, R_{EGT} is small and relaxation time is smaller. However, Figure A2.4 suggests that there is not a significant difference between $t_{spike\text{-}OFF}$ and $t_{spike\text{-}ON}$. Therefore, the t_{spike} is considered equal to larger one, $t_{spike\text{-}OFF}$. To have 95% of the spike vanished, 3 $R_L C_{para,D}$ is required.

$$t_{spike} = 3\, R_L C_{para,D} \tag{A2.9}$$

Therefore, from Equations A2.8 and A2.9 neither V_{spike} nor t_{spike} is frequency dependent which is supported by Figure A2.3. In Figure A2.4, t_{spike} and V_{spike} remain constant for a $\frac{100\mu m}{5\mu m}$ aspect ratio device at 1 and 3 kHz square-wave inputs which shows the spike is independent of input frequency.

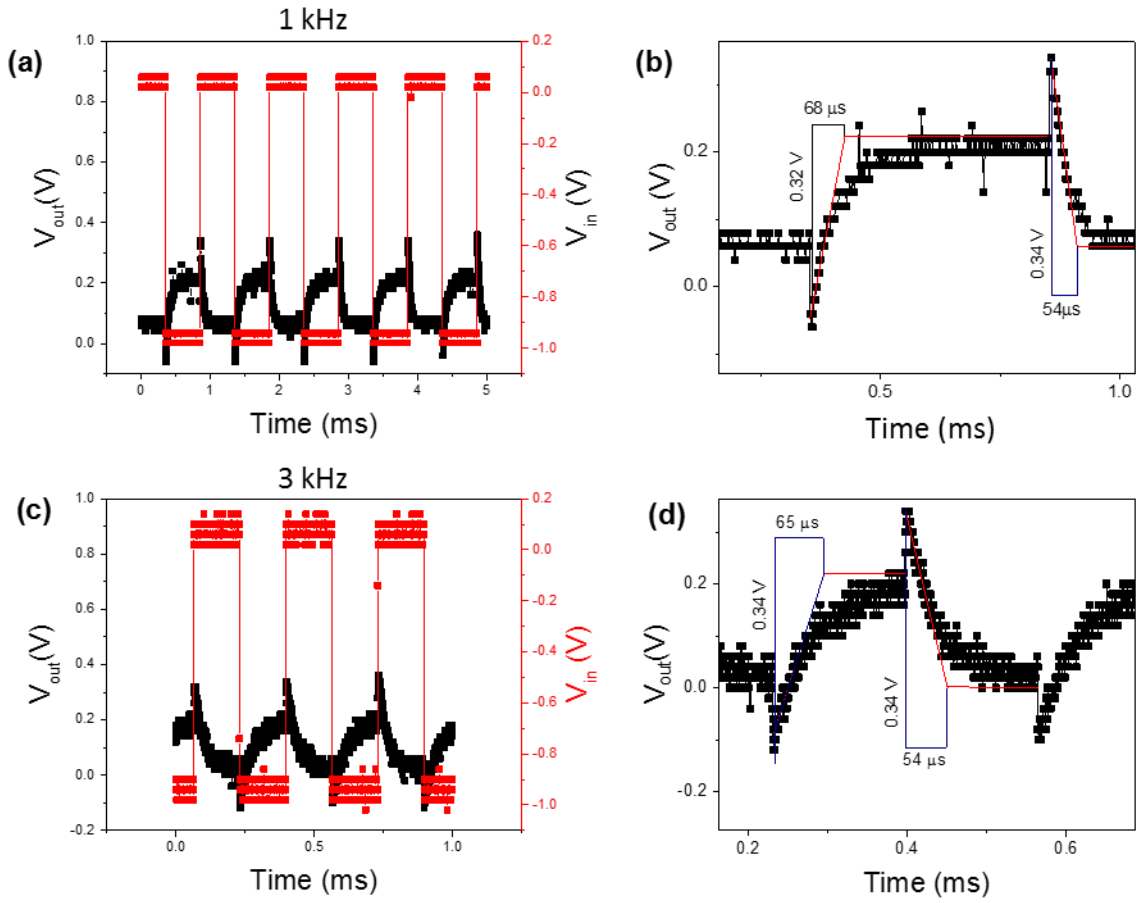

Figure A2.4. Spike times and heights. The W, L, and a are 100 µm, 5 µm, 5 µm, respectively. a) 1 kHz square-wave input, b) the magnified output for 1 kHz input, c) 3kHz input, d) magnified output for 3 kHz input. The spike times show no significant change by applying 3 times faster input.

Based on $f_{cut\text{-}off}$ definition, at $f_{cut\text{-}off}$, $t_{spike}=t_{ideal}$ and $1/f_{cut\text{-}off}=4t_{spike}$, and thus,

$$f_{cut-off} \approx \frac{1}{4t_{spike}} \tag{A2.10}$$

Inserting Equation A2.9 in Equation A2.10, $f_{cut\text{-}off}$ is derived as function of $C_{para,D}$, Equation A2.11. It is noteworthy that there is no L dependence in $f_{cut\text{-}off}$.

$$f_{cut-off} \approx \frac{1}{12R_L C_{para,D}} \tag{A2.11}$$

***V_{spike}, t_{spike}* and *$f_{cut\text{-}off}$* Calculation.** In the calculation of spike time and height it should be noted that a previous study shows that ion gel specific capacitance is dependent on the working frequency.[113] For the spike change, the time constant (τ) is very small which results in a smaller ion gel capacitance value, in order of 10 µF/cm^2. However, during the relaxation, the ion gel has enough time to form the double layer and electrochemically dope the P3HT, so the specific capacitance rises to around 100 µF/cm^2. With this in mind, the specific ion gel capacitance for the V_{spike} calculation is closer to 10 µF/cm^2, whereas, for the relaxation time calculation, the specific capacitance is closer to 100 µF/cm^2. Therefore, the calculated V_{spike} is closer to 1.25 V and the calculated $f_{cut\text{-}off}$ is closer to 6.67 kHz.

Best optimized device. The best optimized device response is displayed in Figure A2.5.

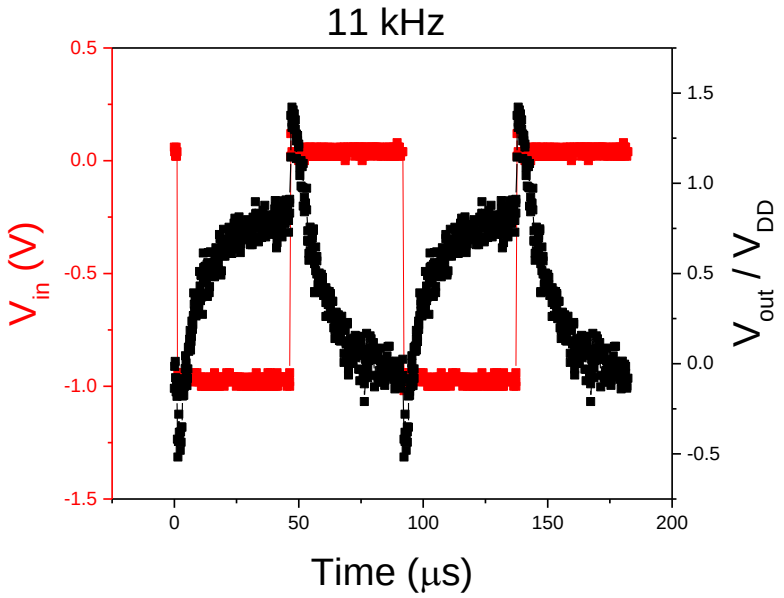

Figure A2.5. Optimized EGT with W=50 µm, L=2.5 µm, and a=2.5 µm. Cut-off frequency of 11 kHz.

A3. Supporting information for Chapter 6

Substrate Preparation. The 100 µm thick polyethylene terephthalate (PET) sheets were purchased from Tekra (New Berlin, WI, USA). The PET sheet was treated with O_2 plasma and hexamethyldisilazane (HMDS) for 15 min and 5 min, respectively. The AZ9260 photoresist and the AZ400 developer were purchased from Clariant Corporation (Somerville, NJ, USA). The photoresist was spin-coated on PET at 5000 rpm for 1 min and dried on a hotplate for 15 min at 120 °C. A Karl Suss contact mask aligner was employed to expose the photoresist through a photomask 4 times for 15 s with 10 s pauses between exposures. The AZ400 developer was diluted with 4 equivalent volumes of deionized water. The exposed substrate was soaked in the developer with gentle agitation for 3.5 min. The substrate was washed with water for 1 min and further HMDS treated for 15 min.

Fabrication of Top-Coated Electrodes. The reactive Ag ink was synthesized in-house using a previously reported procedure and inkjet-printed on the source, drain, and gate reservoirs.[17] The inkjet printing was performed using a custom-built drop-on-demand inkjet printer with an 80 µm diameter nozzle (MJ-AT-01, MicroFab (Plano, TX, USA)) in air at room temperature. A unipolar waveform was employed consisting of rise, dwell, and fall times of 5, 30, 5 µs, respectively, at a drive voltage and a frequency of 120 V and 1 kHz. After annealing at 85 °C for 15 min in the dark, the sample was immersed in a Cu electroless plating bath for 2 min, taken out, rinsed with deionized water, and dried using an air gun. The bath contained 2.7 g of $CuSO_4 \cdot 5H_2O$ (J.T. Baker (Phillipsburg, NJ, USA)), 10.2 g of ethylenediaminetetraacetic acid disodium salt (Fisher Scientific (Hampton, NH, USA)), 4.8 g of NaOH (Mallinckrodt (St. Louis, MO, USA)), 100 mL of deionized water, and 2 mL of formaldehyde (37% solution, VWR (Radnor, PA, USA)). The bath was heated

on a hot plate at 65 °C during Cu plating. The susbsterate was gently washed with deionized water and dried with N_2 gas in ambient condition. The prepared electrodes were covered with the AZ9260 photoresist with same conditions used for the substrate fabrication.

Device Fabrication. P3HT was purchased from Sigma-Aldrich (St. Louis, MO, USA), and a 1 mg mL^{-1} solution of P3HT in chloroform was made with stirring overnight on a hot plate at 55 °C. To produce stable aerosols, terpineol was added to the P3HT solution prior to printing (10% by volume). In order to make the ion gel, a solution with the mass ratio of 1:9:90 for (SEAS): ([EMI][TFSI]):ethyl acetate was made. The SEAS polymer was synthesized in-house using a previously reported procedure.[3] [EMI][TFSI] ionic liquid was purchased from EMD Chemicals (Gibbstown, NJ, USA) and stored in an inert atmosphere. For the PEDOT:PSS ink, PH1000 was purchased from Heraeus (Hanau, Germany), and 6 vol% ethylene glycol was added to the ink to enhance the conductivity. The organic semiconductor (P3HT), gate dielectric (ion gel), and gate contact (PEDOT:PSS) were sequentially printed with an aerosol jet printer (AJ 100, Optomec Inc. (Albuquerque, NM ,USA)). A 150 μm diameter nozzle was used to print. The sheath:feed gas flow rates (measured in standard cubic centimeter per min) for a 100 nm thick P3HT, 4 μm thick ion gel, and 0.5 μm thick PEDOT:PSS were 32:12, 28:8, and 45:25, respectively. A 1 cm long line of diluted 1:1 PEDOT:PSS : deionized water, without ethylene glycol, was also printed to form the 130 kΩ resistor.

Characterization. To avoid humidity effects on the devices, all the measurements were performed in a glovebox with a N_2 atmosphere. For the quasi-static electrical characterization of EGTs and inverters, two sourcemeters (Keithley 237 and 2612B) were connected to the source/drain/gate electrodes, and an electrometer (Keithley 6517A) to the

output electrode. An Agilent 33220 waveform generator was used to generate the input signal for inverters in the quasi-dynamic measurements and the responses were acquired with a Tektronix TDS1002B digital oscilloscope. The printed electrode lines were characterized with an optical microscope (KH-7700, HIROX), and SEM (JSL-6500, JEOL). FIB cutting was accomplished with a FEI Helios NanoLab G4 dual-beaminstrument.

Gating Mechanism. The electrochemical doping of polymeric materials with ions in the ionic liquid of ion gel.

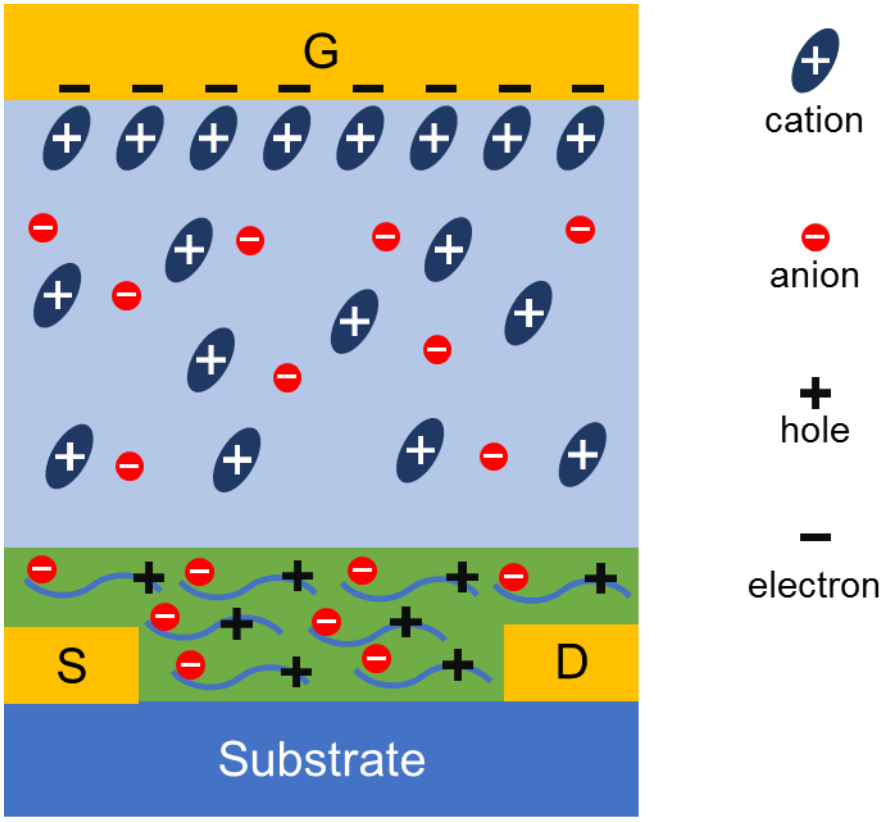

Figure A3. 1. Electrochemical gating mechanism of an EGT with a permeable polymeric semiconductor. The P3HT is doped under negative gate voltage and the channel is ON.

Capacitance Comparison. Figure A3.2(a) is the capacitance-frequency (C-f) measurement for a P3HT EGT without low-κ insulator coatings on the source and drain electrodes, acquired at different gate voltages. For the C-f measurements the source and drain of the EGT were shorted together and the impedance between the gate and the paired source and drain was measured with an AC amplitude of 100 mV around a DC offset (1, 0 or -1 V, as shown). Minimum capacitance detectable with the measurement setup is 1 nF. Figure A3.2(b) shows the gate voltage dependence of the quasi-static capacitance measured via the displacement current method.

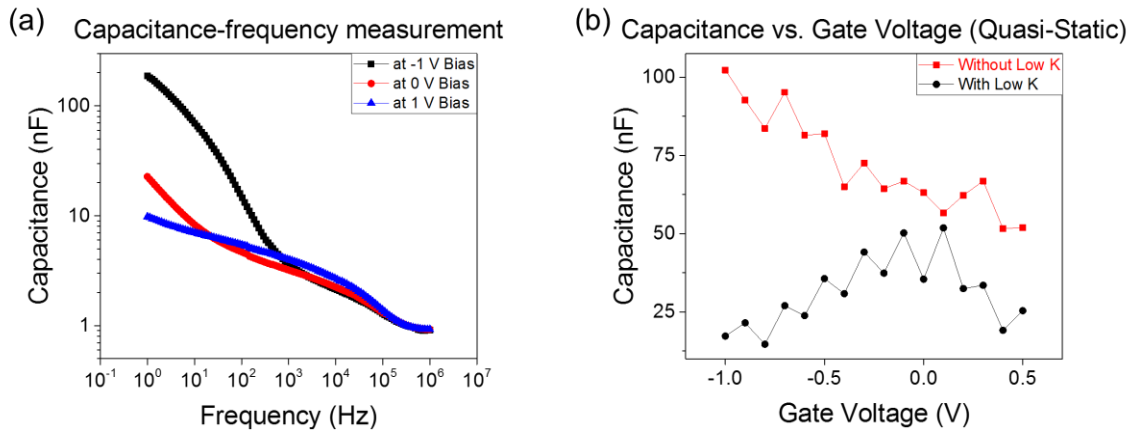

Figure A3.*2.* Capacitance dependencies on gate voltage and frequency. (a) The capacitance values of a P3HT EGT without low-κ electrode coatings were obtained at gate voltages of 1 V (blue curve), 0 V (red curve), and -1 V (black curve). (b) The voltage dependence of the quasi-static capacitance of P3HT EGTs with low-κ (black curve) and without low-κ (red curve) coatings were measured by displacement current.

Fabrication Scheme. The whole device fabrication is on PET and compatible with roll-to-roll process.

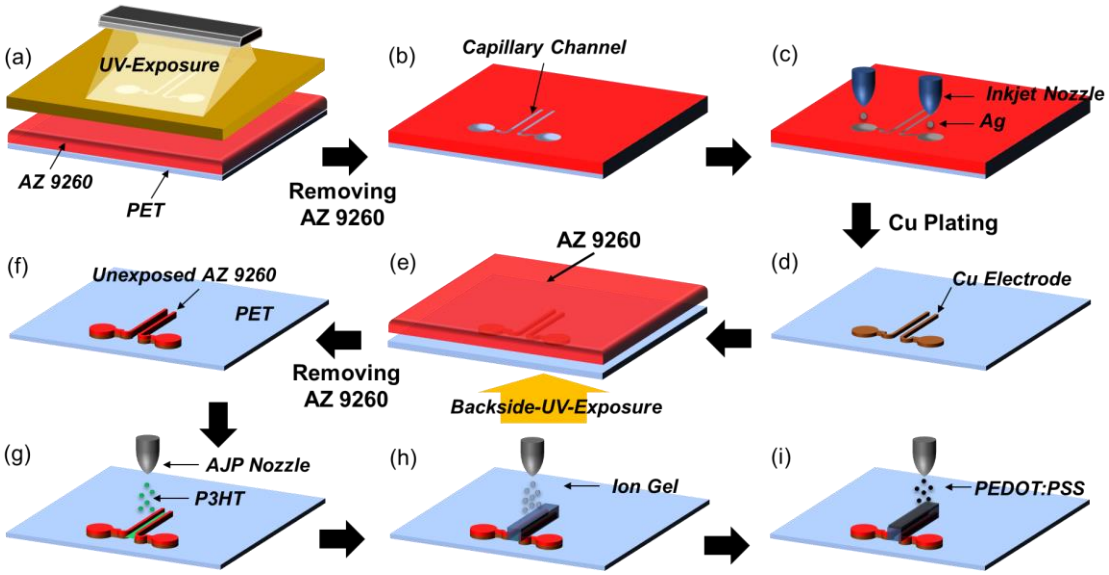

Figure A3.3. Fabrication process on plastic (PET) substrate. (a) AZ9260 photoresist spin coating on the transparent substrate and subsequent photo patterning, (b) photoresist development to produce capillary channels and reservoirs, (c) reactive Ag ink delivery to the reservoirs by drop-on-demand inkjet printer, (d) electroless Cu-plating of printed Ag and photoresist removal leaving raised metal electrodes ($W \times a$ = 500 µm×15 µm), (e) photoresist coating on raised metal electrodes and backside UV-illumination in order to expose all the photoresist except on the electrodes, and (f) photoresist left only on the electrodes in order to cover the top-side of the electrodes. (g), (h), and (i) Aerosol-jet nozzle delivers P3HT, ion gel, and PEDOT:PSS aerosols to the channel area on the PET substrate.

Fabrication Steps Microscopy. Different steps are characterized to ensure high quality of final electrodes. The fabrication process also enables printing of more complex features for other applications. The 5 μm resolution features are shown in the Figure A3.4 (d).

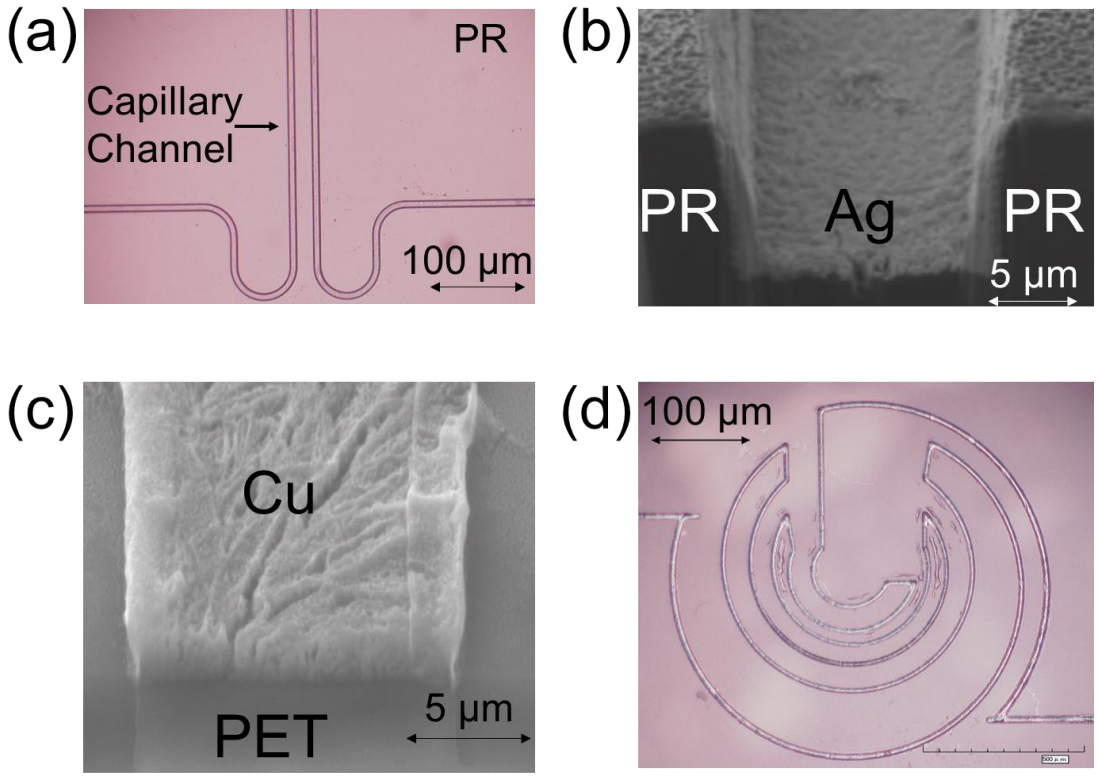

Figure A3.4. Microscopy and characterization of the covered, raised electrodes on PET substrate. (a) Optical microscopy of photoresist channel. (b) SEM cross section image of Ag coated photoresist capillary channel cut by FIB. (c) SEM cross section image of raised metal electrodes on PET cut by FIB. (d) Standalone printed raised conductive metal pattern with higher level of complexity.

SEM and Backscattered Electron Microscopy Image. Figure A3.5(a) is the SEM image of a top-coated electrode after a FIB cut. The backscattered electron microscopy image has higher contrast based on material atomic numbers. Figure A3.5(b) further demonstrates the composition of the printed layers and the interface between layers on the same cross-section as Figure A3.5(a).

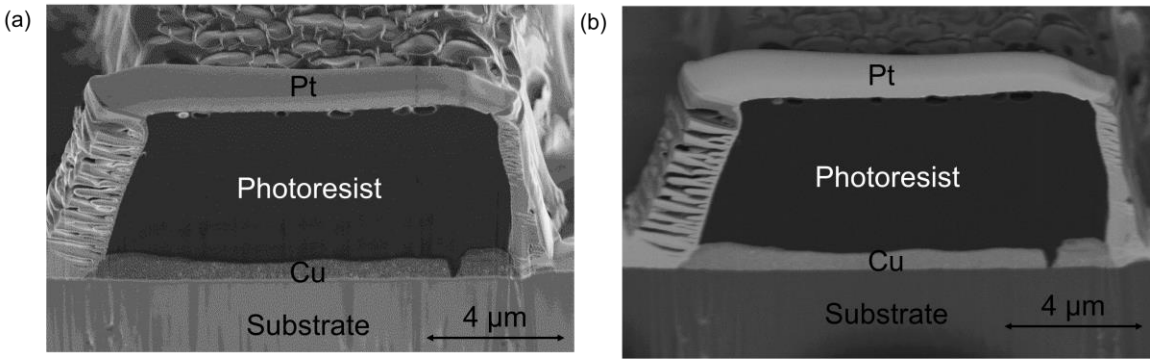

Figure A3.5. (a) SEM and (b) backscattered electron microscopy image of the focused ion beam cut electrode with insulator coating. The brightest to darkest contrasts are Pt, Cu, substrate, and photoresist. Before the FIB cut, a μm-thick layer of Pt was deposited at the cut position. The Pt layer protects the organic layers underneath, such as the photoresist, from ion beam damage. Pt also helps with thermal heat dissipation from the cut position to prevent the photoresist from melting and consequently losing the contrast at the cut interfaces. The Ag film is too thin to be seen in this image.

Profilometry of the covered electrodes. Figure A3.6 shows the surface profilometry of the covered electrode. The width of the electrode is measured as 7.8 µm at mean height and 8.5 µm at the bottom. The total height of the covered electrode is 5.4 µm consistent with the expected height of 6 µm from the spin coating conditions.

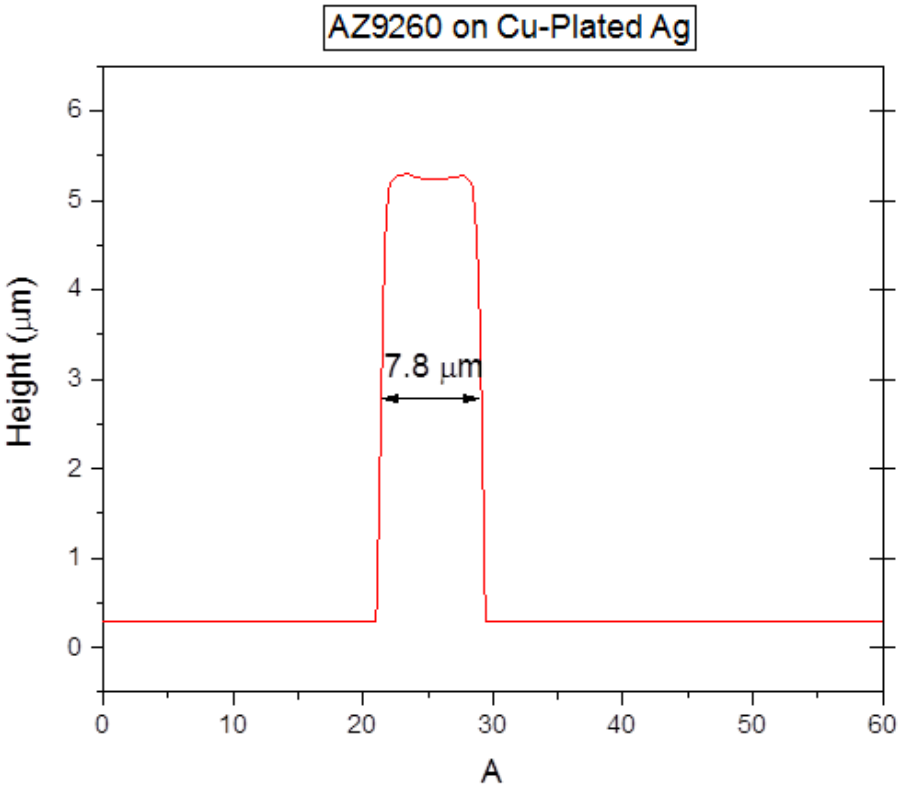

Figure A3.6. Profilometry of the final hybrid walls.

Displacement Current Measurement. Figure A3.7 shows the displacement current measurement for the device at different gate voltage sweep rates.

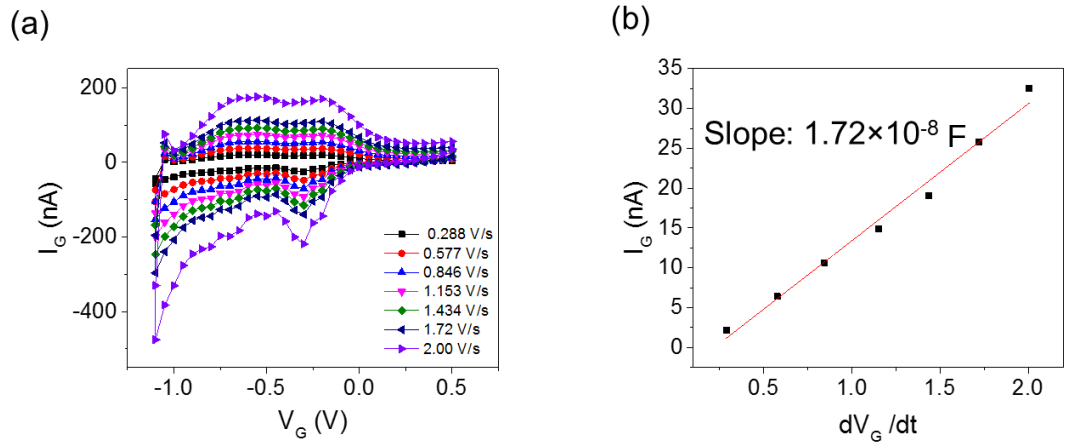

Figure A3.7. (a) Gate current I_G–V_G characteristics obtained at different gate sweep rates (dV_G / dt) for 100 nm-thick P3HT EGT (V_D = 0 V). (b) A plot of I_G versus dV_G / dt at V_G= -1 V. The C_{iongel} value of ion gel gate insulator was obtained from the slope of the plot divided by the total device area.

Log I_{ON}/I_{OFF} Calculation. The I_{OFF} current is calculated based on Eq. S1 as the average minimum log value of drain currents in forward, $I_{D\text{-}forward}$ and backward, $I_{D\text{-}backward}$ sweeps.

$$\log I_{OFF} \approx \frac{\log(\min I_{D-forward}) + \log(\min I_{D-backward})}{2} \quad \text{(A3.1)}$$

A4 Supporting information for Chapter 7

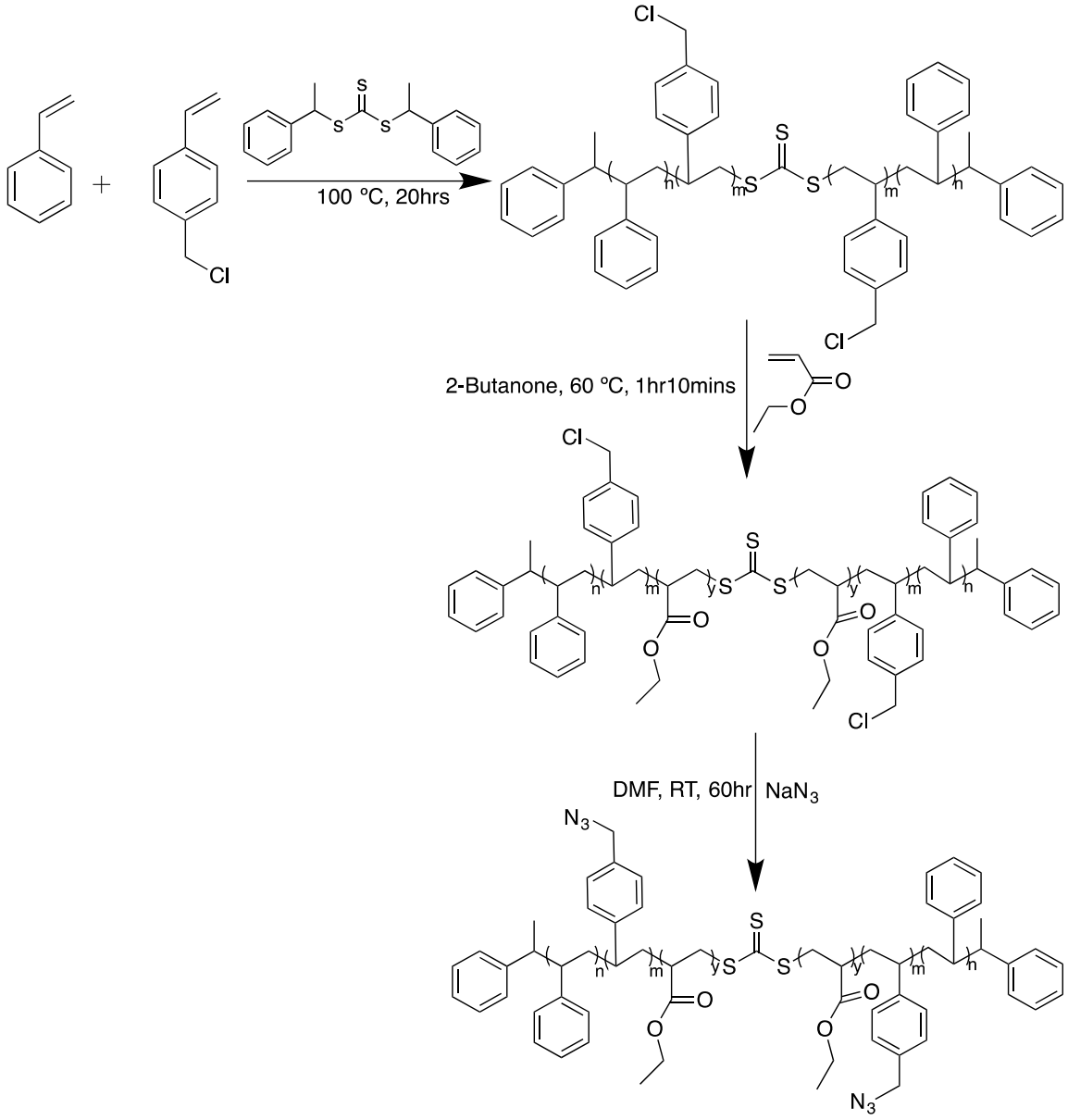

Figure A4. 1. Synthetic Route to SEAS-N3 Triblock Copolymer

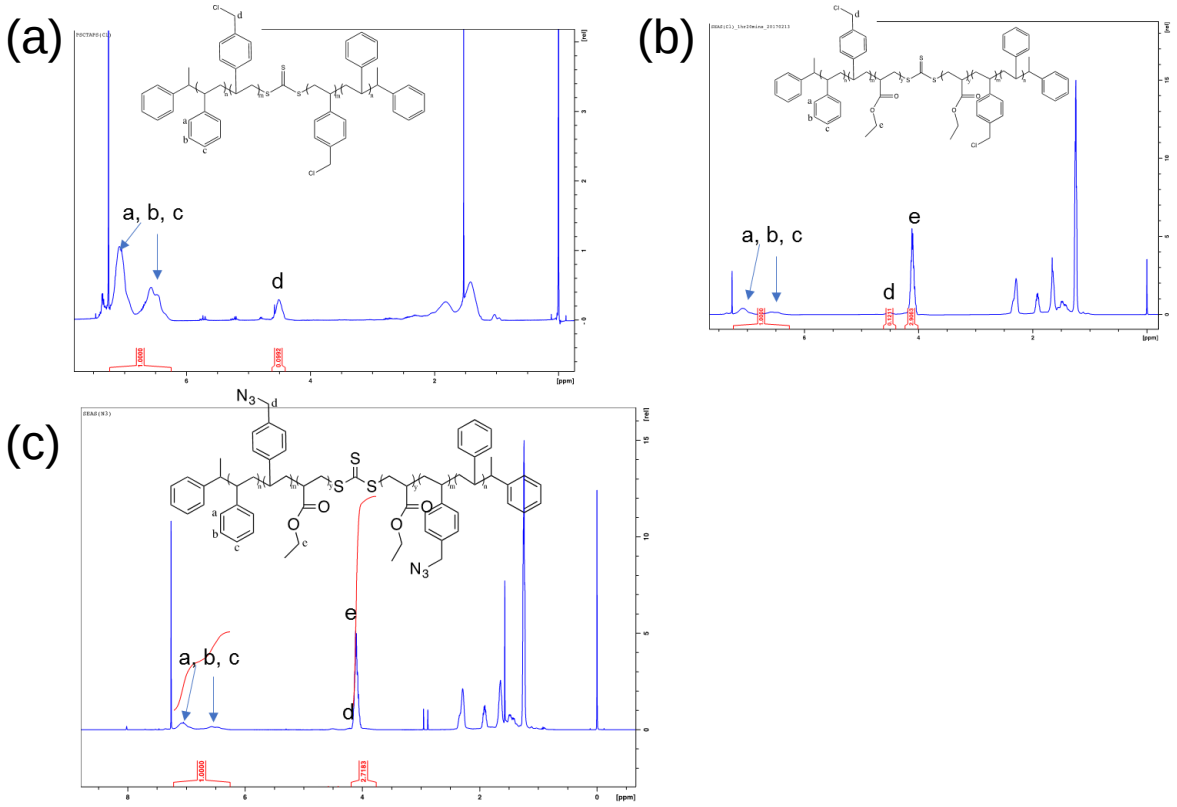

Figure A4.2. ^{1}H NMR spectra (500 MHz, in $CDCl_3$) of (a) poly[(styrene-r-vinylbenzyl azide) -CTA-poly[(styrene-r-vinylbenzyl azide), (b) SEAS-Cl, and (c) SEAS-N_3

Device Fabrication:

Semiconductor Layer. A 4 in. 500 µm-thick (±25 µm) p++ silicon wafer with 300 nm thermally grown SiO_2 was placed in a Savannah Series ALD system, Figure S3a. The ZnO was deposited with diethylzinc (DEZ) and water vapor as precursors at 235 ºC which showed minimum residual stress in the deposited ZnO film on SiO_2, Figure S3b. The deposition rate was ~1.32 Å per cycles measured by ellipsometry and fitted to the Cauchy model. The 50 nm-thick ZnO was achieved by 336 deposition cycles. The ZnO film was then annealed in a rapid thermal annealing chamber system, RTP-600S, Modular Process Technology. The film was annealed in N_2 and O_2 atmosphere at 300º C and 400º C, respectively for 30 min. The Shipley *(+)* tone photoresist, S1813 was spin-coated at 3000 rpm for 1 min on the wafer and baked at 105 for 1 min. A Karl Suss MA6 mask aligner was used to pattern the photoresist in hard contact mode, gap of 30 µm, and exposure time of 4 s. The pattern was developed in 351 developer solution (1:4 v/v water) for 15 s, Figure S3c. The wafer was rinsed for 1 min and dried with N_2. The wafer was immersed in a 3% (v/v) solution of HCl for 5 s and was rinsed for 1 min, Figure S3d. The photoresist was washed off with acetone, Figure S7e. It is noteworthy all the glassware should be washed with basic solution and water in advance as any acid contaminant dissolves the ZnO layer.

Electrodes, Passivation, and Support Layer. All the layers were patterned using the same photolithography procedure used for ZnO. The hard-baking steps were removed to ensure a clean lift-off process. The contact pads were patterned first, Figure S3f, followed by O_2 plasma cleaning in an STS etcher for 2 min. A 5-nm-thick Cr layer was deposited by ebeam evaporation first as an adhesive layer, followed by 25-nm-thick Au as the conductive pads and interconnects, Figure S3g. An overnight soaking followed by acetone and isopropanol

wash were performed in a lift-off process, Figure S3h. The electrodes were patterned, Figure SI3i, and 10-nm-thick Ti/60-nm-thick Au/10-nm-thick Ti were deposited by ebeam evaporation followed by 100 nm SiO_2 deposition, Figure S3j. An overnight lift-off process was performed, S3k. Another photolithography step was done for SiO_2 supports followed by 250 nm SiO_2 deposition and lift-off (not shown in Figure S3).

Silicon Stencil-Based Ion Gel Screen-Printing: The Si stencil was attached to a Kapton film with an opening corresponding to the stencil printing area. The Kapton film was attached to an acrylic plate with an opening inside it. The acrylic palate had the same dimension of the 5 in. photomask and was laser cut in a machine shop. The acrylic stencil holder was attached in the Karl Suss MA6 aligner and aligned on the substrate with the finished surface face down toward the wafer, Figure S3l. The hard contact mode was selected. Then 1 ml of ion gel ink was delivered on the stencil. After solvent evaporation, the remaining gel was squeezed with a razor blade on the stencil at a 45º degree angle, Figure S3m. The whole gel was squeezed back and forth 3 times. Then, 1 ml of -20 ºC ion gel ink was added and before evaporation of the solvent, it was squeezed till all the solvent is evaporated. Then the UV lamp was fixed on the stencil. The 254-nm UV light was exposed to the substrate for 3 min, Figure S3n. The UV lamp and stencil were removed, and features were checked by optical microscope, Figure S3o. If uncured ion gel was evident, it was removed by 5 s wash with saturated chloroform ionic liquid solution.

Top-gate Au Electrode deposition: Another Si stencil adhered to Kapton with an opening (as above) was attached to the acrylic plate and was aligned on top of the substrate, Figure S3p, in a mask aligner. Before hard contact, the substrate holder was slipped out and double-sided tape was attached to the substrate. The substrate holder was reinserted into

the aligner in very close proximity (~ 200 μm) to the stencil. Then the substrate was precisely aligned and brought into hard contact with the stencil. Substrate and stencil were thus adhered in precise registry by means of the tape. The acrylic plate was removed from the aligned stencil and substrate pair by cutting the Kapton around the circumference of the stencil. The stencil and substrate sandwich was then loaded into an e-beam evaporator for deposition of 25 nm-thick Au on the ion gel through the stencil openings, Figure S3q. This formed the gate electrodes. To access the devices, the stencil was broken, Figure S3r.

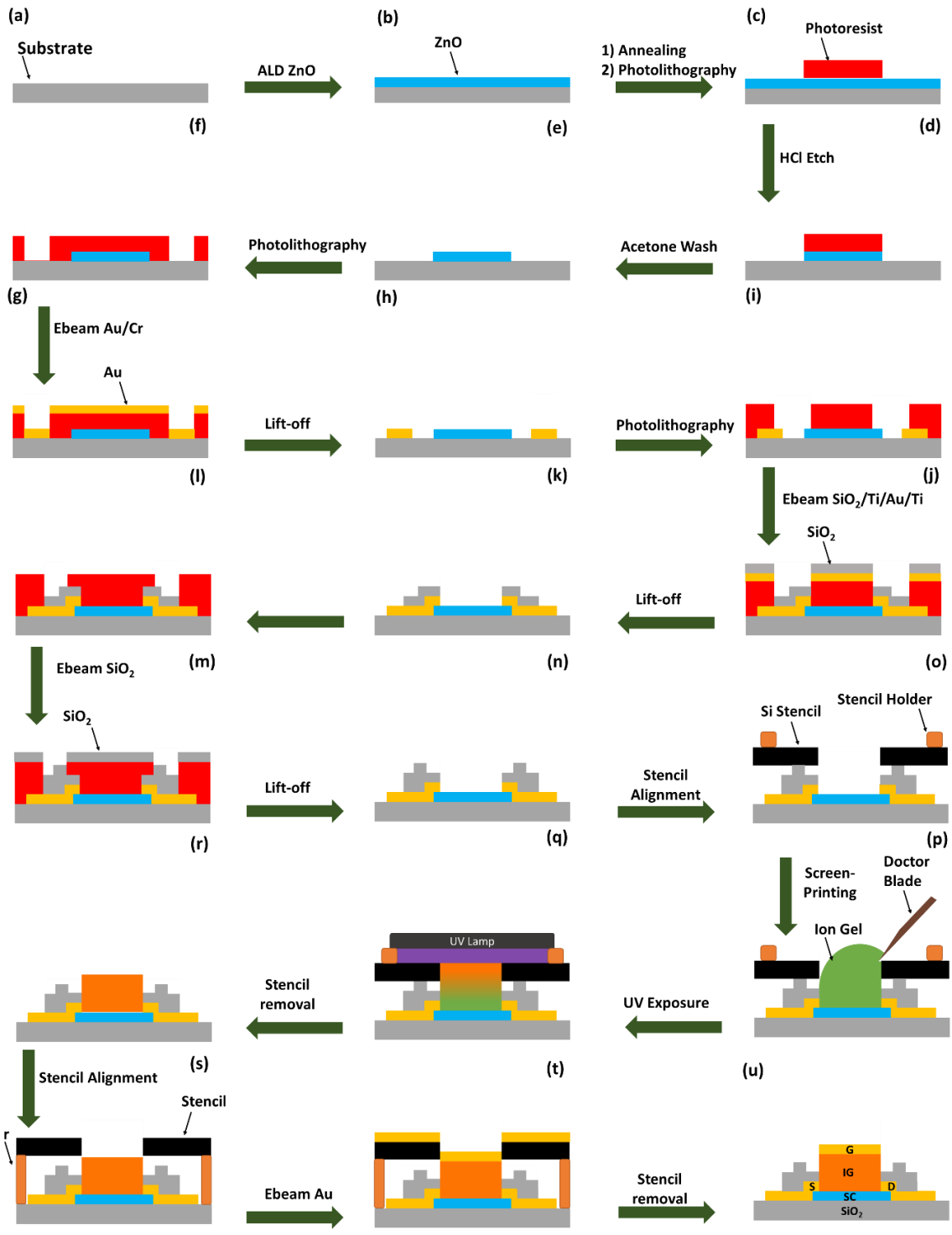

Figure A4.3. Full EGT fabrication sequence. a) Silicon substrate. b) A ZnO 50 nm-thick layer is deposited at 235 ºC by ALD, followed by annealing at 300ºC and 400ºC in N_2 and O_2 atmosphere respectively. c) The first layer is photolithography patterned followed by d) chemical wet etching with HCl. e) The photoresist is removed in acetone batch followed by f) photolithography for contact pads deposited by g) e-beam thermal evaporation of 5 nm-thick Cr (adhesive layer) and 25 nm-thick Au (conductive interconnects). (h) Overnight

acetone lift-off followed by i) source/drain electrode definition by photolithography. j) The same evaporation as the previous one with additional SiO_2/Ti applied to passivate the electrodes followed by k) lift-off. l), m), n) photolithography, e-beam evaporation, and lift-off of the 250 nm-thick SiO_2 layer. o) Stencil is aligned by aligner and p) ion gel is screen-printed and q) photo-crosslinked by 254 nm UV exposure for 3 min. r) The ion gel stencil is removed. s) Gate stencil is aligned and t) the 25 nm-thick Au is deposited on top followed by u) removal of gate stencil.

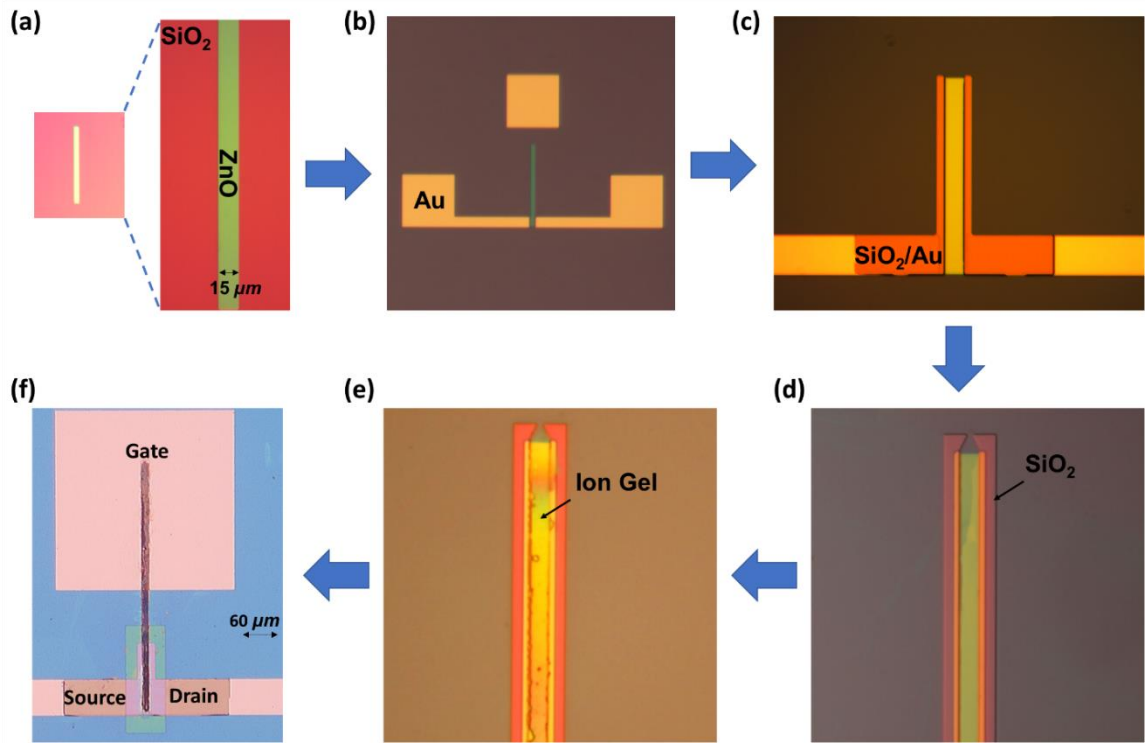

Figure A4.4. Optical images of a ZnO EGT at different fabrication steps. a) Silicon substrate with a 50 nm-thick ALD grown ZnO layer, thermally annealed at 300 ºC and 400 ºC and patterned by photolithography and HCl wet etching. b) photolithography patterned and thermally deposited Au contact pads (5 nm-thick Cr as adhesive layer and a layer of 25 nm-thick Au as conductive interconnects). c) and d) source/drain electrodes are deposited with additional SiO_2/Ti (250 nm/5 nm) applied to passivate the electrodes and support the ion gel. e) screen-printed and UV cured ion gel on the ZnO channel. f) final device after Au gate electrode deposition.

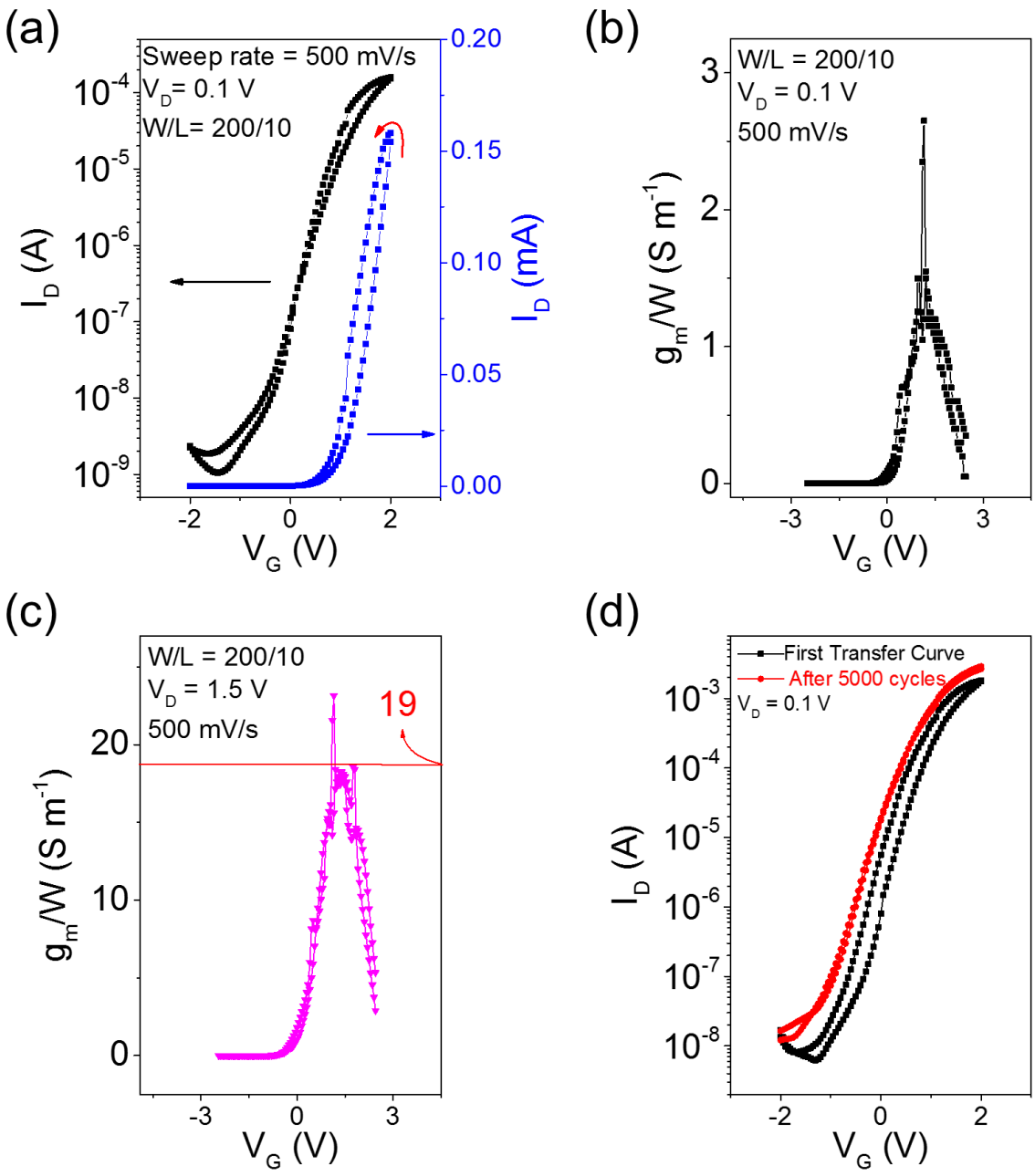

Figure A4.5. EGT characterization. a) Transfer and b) transconductance curves for a *W/L* = 200 µm/10 µm ZnO EGT at V_D = 0.1 V and sweep rate of 500 mv/s. c) The transconductance in the saturated regime at V_D = 1.5 V. d) Stability data for ZnO EGTs after 5000 I_D-V_G cycles (~22 hrs). The ON/OFF current ratio is constant but there is a small threshold voltage shift.

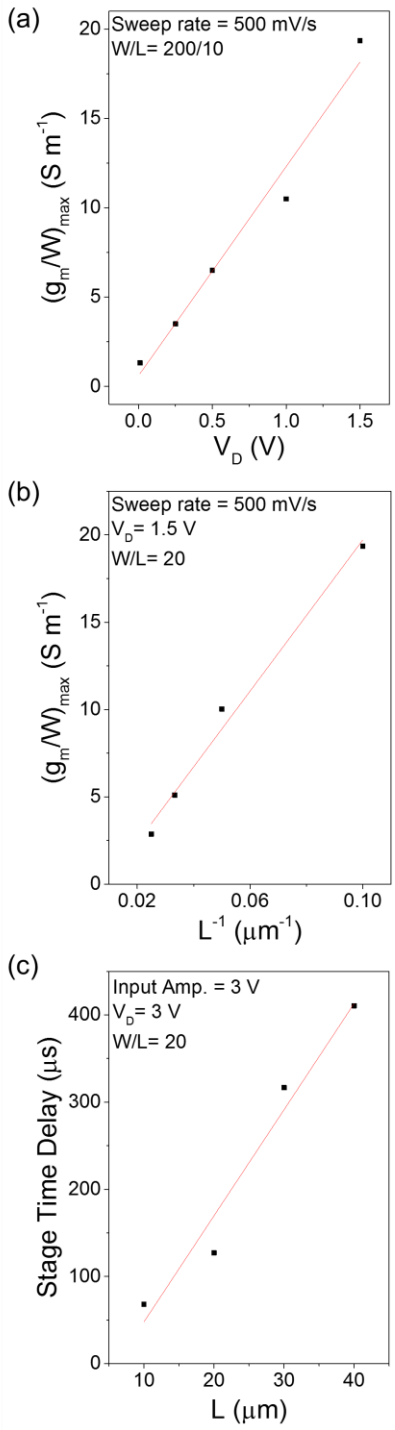

Figure A4. 6. ZnO EGT scaling characterization. a) The channel-width-normalized transconductance vs. V_D for a device with W/L = 200 μm/10 and b) Width normalized transconductance vs. L^{-1} with the 500 mV/s sweep rate at V_D = 1.5 V. c) The stage delay time for an EGT inverter with internal feedback vs. the device channel width. The W/L aspect ratio is constant overall devices and is 20.

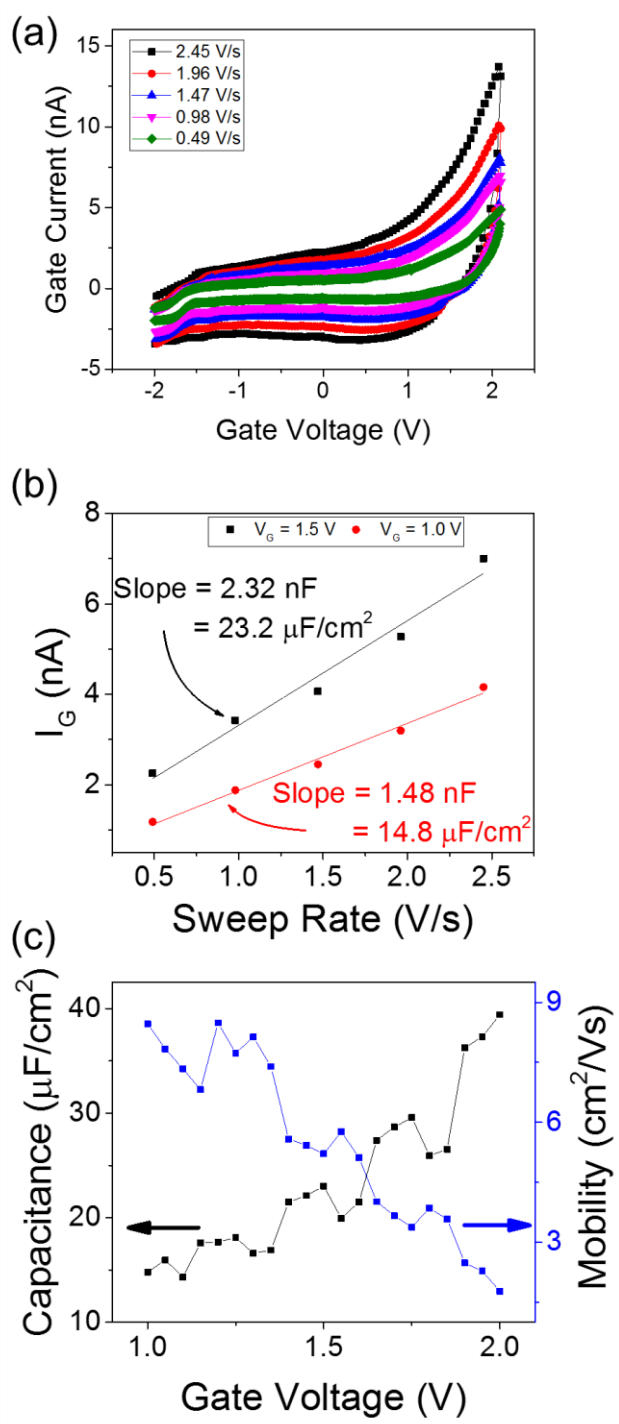

Figure A4. 7. a) and b) Gate displacement current vs. sweep rate. The slope gives EGT gate capacitance at V_G= 1.5 V and 1.0 V for W/L = 100 µm/100 µm c) The capacitance and mobility dependence vs. V_G are shown. The capacitance is measured as described in Figure S6 from displacement current measurement. The mobility is measured from Figure S7b at V_D = 0.1 V in the linear regime using Equation 1.