DESIGN AND REALIZATION OF A UHF RFID INTERROGATOR

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Abstract- RFID is a generic item which uses radio waves to automatically identify objects and people. This paper presents a flexible RFID interrogator system architecture which could support various kinds of RFID standards and realizes a UHF RFID interrogator based on the EPC global C1G2 standard in details. The proposed interrogator system consists of RF analog front end, digital baseband and MAC layer. The system circuit contains a FPGA chip and peripheral circuits. NiosII core as a controller is inserted in FPGA. The proposed FPGA based baseband platform could implement various kinds of RFID standards, and efficiently reduce the design time and development cost.

Index terms: RFID, interrogator, reader, UHF, EPC C1G2 , baseband, transceiver

I. INTRODUCTION

Radio Frequency Identification (RFID) is a kind of technology that allows identification via the use of radio waves. The basic RFID systems are consisted of tags and interrogators. Interrogators are also known as readers. A tag usually has an antenna for transmitting signals to RFID reader and a microchip for storing basic information such as ID and information of manufacture [1]. Auto-ID technologies use barcodes, which is optical character recognition technology to identify the product information. Passive UHF RFID is considered as barcode replacement due to its low cost. Barcodes have some disadvantages. They can be read only in the sight of reader. If the barcode can not be seen, it can not be read. The information stored in barcodes is fairly limited. The information is fixed and the user can not change it. By contrast, RFID system uses radio frequency waves to recognize a tag without the need of the line of sight. The tag has an integrated circuit with memory, so the information can be stored and easy to be written. However, RFID tags are still expensive than barcodes. As the cost of tags continues to drop, radio frequency identification has been used in many applications such as automated toll systems, asset management systems and payment systems. RFID reader can track, sense, and identify various targets in wide areas such as supply chain, medical science industry, transportation, access control, airline baggage handling, and homeland security fields.

a. Energy

RFID technology can be classified based on the energy source of the tags. There are passive, semi-passive, and active tags [2, 24]. Passive tags derive the energy from the radio frequency waves that the reader have provide, it means that tag can work without any energy source. Due to the low cost, there are only less than 5000 gates on a tag so that the tag has only limited computational ability and storage. By contrast, active tags need batteries, when they communicate to the reader, active tags can be read in a wider range than passive tags. However, battery will limit the lifetime of the tag and expand the size of the tag. Semi-passive tags are between passive and active tags. Semi-passive tags have much smaller batteries, longer lifetimes than active tags, and longer communication ranges compared to passive tags.

b. Frequency

According to different working frequency, RFID system can be segmented in another way. Each frequency has different characteristics. High frequency (HF) and ultra high frequency (UHF) are most popular bands. HF RFID working at around 13.56 MHz. Near Field Communication is a popular RFID technology in the HF range. The range is up to tens of centimeters and transfers power to the tag via inductive coupling to passive tags. UHF RFID work frequency is from 860MHz to 960MHz.The work frequency is higher and the read range of a tag is farther, passive tags are powered through electric coupling at the range of UHF RFID. Typically, HF can be interrogated up to 1m. Due to the propagation at 915MHz frequency, the range is up to about 10 meters for passive tags.

c. Protocol

In this paper we focus on passive UHF RFID operating at the 915 MHz band. In 2005,EPC Global published the Class 1 Generation 2 UHF RFID Protocol for Communications[3],which commonly known as EPC C1G2. With the standard's publication and modification by Walmart, their tags compliant with this standard, the cost of tags reached the levels that made it appropriate for use in the retail market. The specification describes a reader talk first communication. A reader initials an inventory round by sending an un-modulated signal to tags. Continues carriers (CW) are sent through the inventory round to keep the energy of tags. Once the tags are powered up, the reader initiates the communication by sending commands. Afterwards, tags response the command by backscattering the CW from the reader.

There are several systems about the design of UHF RFID reader [4-11, 18-23]. Some designs use microcontroller unit or DSP chip as main controller. Some designs use ARM as main controller and FPGA as encoder and decoder. Baseband processor decides the performance of the UHF RFID reader system. In this paper, a UHF RFID reader based on FPGA has been designed and it is compatible with EPC C1G2 Standard. FPGA could meet the complex requirement and flexible apply to different standards. The paper is organized as follows. First, Reader's generic architecture is briefly reviewed in Section II. The proposed reader RF architecture, digital baseband, MAC layer and circuit implementation are described in Section III. Finally, experimental results are discussed in Section IV and conclusions are summarized in Section V.

II. GENERIC ARCHITECTURE

Generally, the reader platform is divided into RF, baseband and MAC layer sections. The system architecture is shown in figure 1. The RF section is essentially a UHF transceiver, which converts baseband signal to radio frequency (915 MHz), or inverse. The digital baseband is the upper level of the physical layer (PHY).The digital baseband executes symbol-bit conversion, digital modulation, demodulation, encoding and decoding. The RF and baseband sections are unity of PHY layer. The Media Access Control (MAC) layer is executed by the MAC processor which provides interface to the host PC and networking devices. The whole system architecture can be divided into signal transmitter part and receiver part. The communication starts from the transmitter part. Firstly, the MAC processor selects command according to reader state and the previous received signal. According to the format defined in the standard, the selected command is encoded in the baseband part, and then is converted to analog signals by the digital-to-analog converter (DAC) and is sent to the RF part. In RF part, the analog signals will be modulated from baseband signals to RF signals. Finally the RF signals will be moved to the antenna and sent to the RFID tag through air interface. The tags receive the reader command and send response signals to the reader. In receiver part of the reader, the received signals from the tag are filtered by the band pass filters, down-converted by the mixer and processed by the low-pass filters. Then the baseband signals are converted to digital signals by the analog-to-digital (ADC) converter. The digital signals will be decoded to a standard format. The decode results will detect the status like collision or no data. The status is sent to the control part, and the next reader command will be sent to the tag. Followed by the Rx operations, a new round of transmitter operation such as command generation, encoding and modulation will be performed.

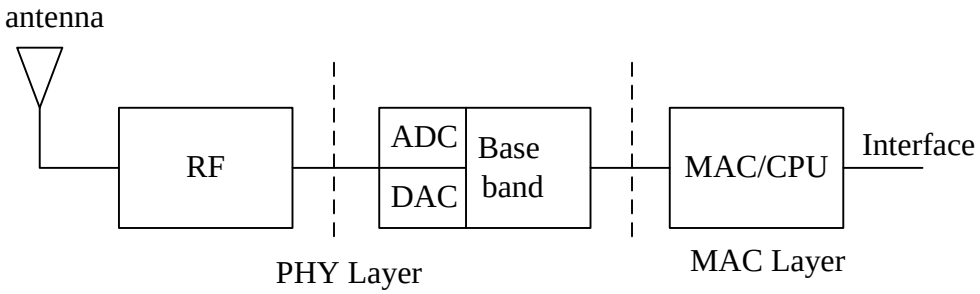

Figure 1. System architecture

When the reader interrogates a tag, the passive tag obtains energy from the continuous wave (CW) signal transmitted by a reader. In addition, the passive tag responds to reader though backscattering the CW signal [12]. Therefore, an RFID link is half duplex: reader to tag is forward channel and then tag to reader is backward channel. This shows that RFID links are not balanced. Moreover, the backward channel link is highly correlated with the forward channel link. because the tag's backscatter power is limited by the reader's transmit power. These link characteristics can use the link budget concept to calculate.

The range of a reader can interrogate a tag is highly influenced by the environment. We consider a number of different propagation models that may be applicable in different scenarios. As a baseline, we consider a free-space model[17].

$$P_{RX}(r) = (\frac{\lambda}{4\pi r})^2 P_{TX} G_T G_R \quad (1)$$

where

λ: the wavelength in free space

r : the operational distance between an RFID tag and the reader

P_{TX} : the signal power feeding into the reader antenna by the transmitter

G_R : the gain of the reader antenna

G_T : the gain of the tag antenna.

The RFID link is not defined as a noise limited RF communications link. In forward link, the tag is gaining enough carrier power from the reader. In reverse link, the tag's backscatter signals are not the noise power at the reader receiver. The limitation in a typical passive RFID link described in [13] and [14] .For example, RFID tag should have a turn on power of -17.4 dBm in EPC C1G2 compliant commercially requirement. Assuming a reader transmit power is 30 dBm, reader antenna gain is 6 dBi and tag antenna gain is 2 dBi. At 915 MHz carrier frequency, the maximum path loss between the reader and the tag in free space is 55 dB. Tags must absorb energy to maintain operation in the backscatter modulation, the amount of power backscatter is less than the received power. This modulation loss factor is described in [15] is about -6dB lower than tag receive powers. Since the channels are interfered with each other, the path loss is also 55 dB when the tag signals are back to the reader. Therefore, the reader receives the tag's backscatter signal with a minimum power of -78 dBm limitation. Additionally, the typical reader receiver is not consider about thermal noise limit. The thermal noise of a receiver has a noise floor of -120

dBm with 250 kHz wide bandwidth. By contrast, the tag's weakest backscatter signals require a theoretical SNR of about 42 dB. In reality, the RF components such as mixers will increase to the noise figure of the system and raise the noise floor. The lowest SNR would be 17 dB to meet the design requirement for noise figure of 25dB.

III. DESIGN IMPLEMENTATION

a. RF architecture

The block diagram of RF circuit is shown in Figure 2.In the part of the receiver, the RF signals pass through appropriate band pass filter and amplifier, and then pass through orthogonal decomposition to get I/Q signals. The signals are processed by down-conversion and DC offset module. Finally, they are amplified and sent to digital part. In the transmitter part, the baseband signals pass through ascending cosine filter and Hartley transform, and then they enter digital-to-analog converters. DACs convert the signals to analog signals, the two analog signals pass through mixer respectively, then they are modulated to sideband or double sideband signals .Finally the signals are amplified and send to antenna. Antenna transmits electromagnetic energy and signals to the tag.

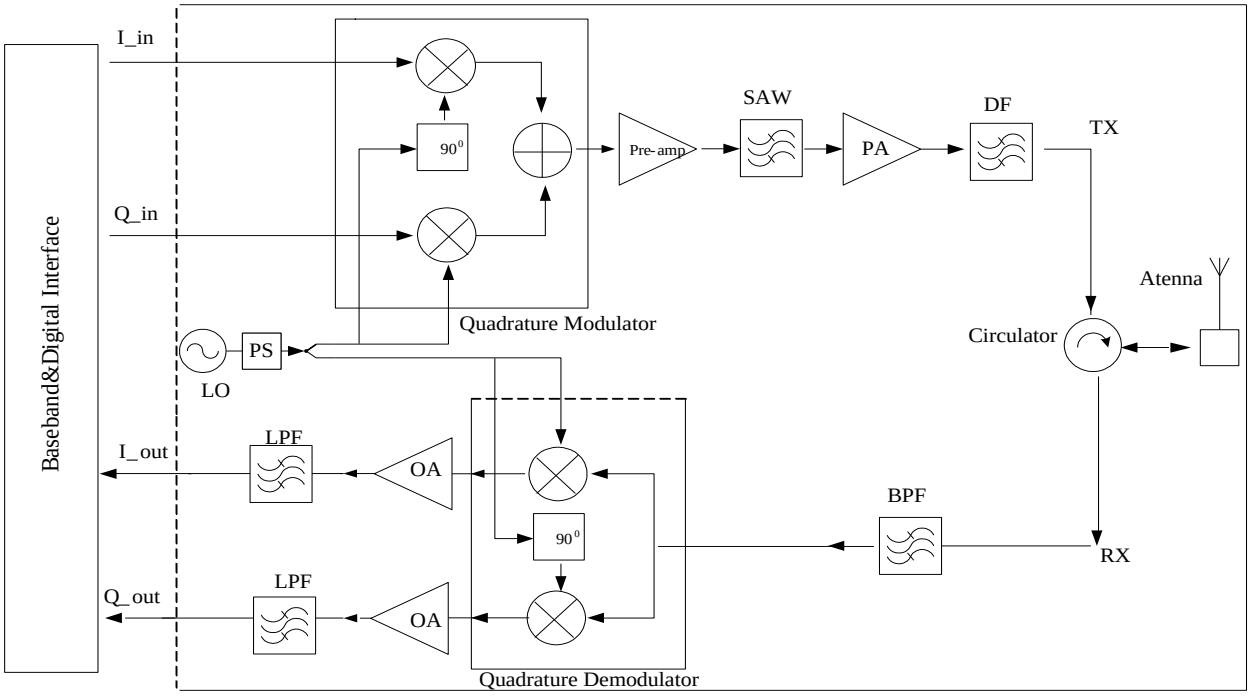

Figure 2. Block diagram of RF circuit

According to EPC C1G2 protocol [3], RFID reader system uses three modulations: DSB-ASK, SSB-ASK or PR-ASK. In order to meet the more flexible protocol requirements, the transmitter circuit uses orthogonal I/Q modulation to suppress one useless sideband in the double sideband signal [16]. When the two baseband signals go through I/Q two-way conversion respectively, add or subtract, modulators send out SSB modulation signals. In order to reduce hardware costs, the signals accomplish modulation and up-conversion at the same grade.

Zero-IF receiver architecture is applied in the circuit. The zero-IF receiver local oscillator (LO) and the received backscatter signals have the same frequency, therefore, the receiver LO and transmitter LO could use the same local oscillator to reduce hardware cost, circuit complexity and power consumption. When the received signals are at zero frequency, they have not power distribution. After appropriate filter, Direct current (DC) offset has little effect on the received signals. In order to avoid the zero-effect in the receiver, the orthogonal I/Q receiver structure has been designed. When the multi-channel or phase offset causes one channel can not receive a valid signal, another channel (phase-shifted 90 degrees) could receive a strong signal, and vice versa. The analog front-end architecture based on direct conversion is shown in Figure 2, which includes a local oscillator (LO), Power splitter(PS),Quadrature modulator, Pre-amplifier (Preamp), Power amplifier (PA) , Dielectric filter (DF),Circulator, Operation amplifier(OA),some filters and the antenna. In the proposed design, RF front end is built from discrete components. LO signals are created by the frequency synthesizer. The frequency synthesizer chip is Si4133. The Si4133 is a monolithic integrated circuit which performs IF and dual-band low noise RF frequency synthesis for RFID applications. Power splitter is MAPDCC0001, it provides receiver and transmitter LO signals. Quadrature modulator acts as a mixer, which mixes the base band signals and the orthogonal LO signals to get up-conversion. Linear company’s modulator LT5568 could meet the requirements. Pre-amplifier is Mini-circuits company's ERA-5+, and MURATA provided SAW Filter, Dielectric Filter. Power amplifier is M/A Company's MAPPSS0095.After through amplifiers and filters, the modulated carrier is sent to antenna. Circulator is MAFRIN0461, which make the received and sent signals isolated. The received signals go through LT5516 demodulator, are amplified by the dual power amplifier LT6231 and filtered by Low pass filter LT1568.

b. Digital baseband architecture

The digital baseband hardware consists of a FPGA, two high-speed 12 bit DACs, two high-speed 12 bit ADCs, low speed ADC and DAC, SDRAM, FLASH and some common interfaces. A block diagram of the components of the digital baseband is shown in Figure 3.

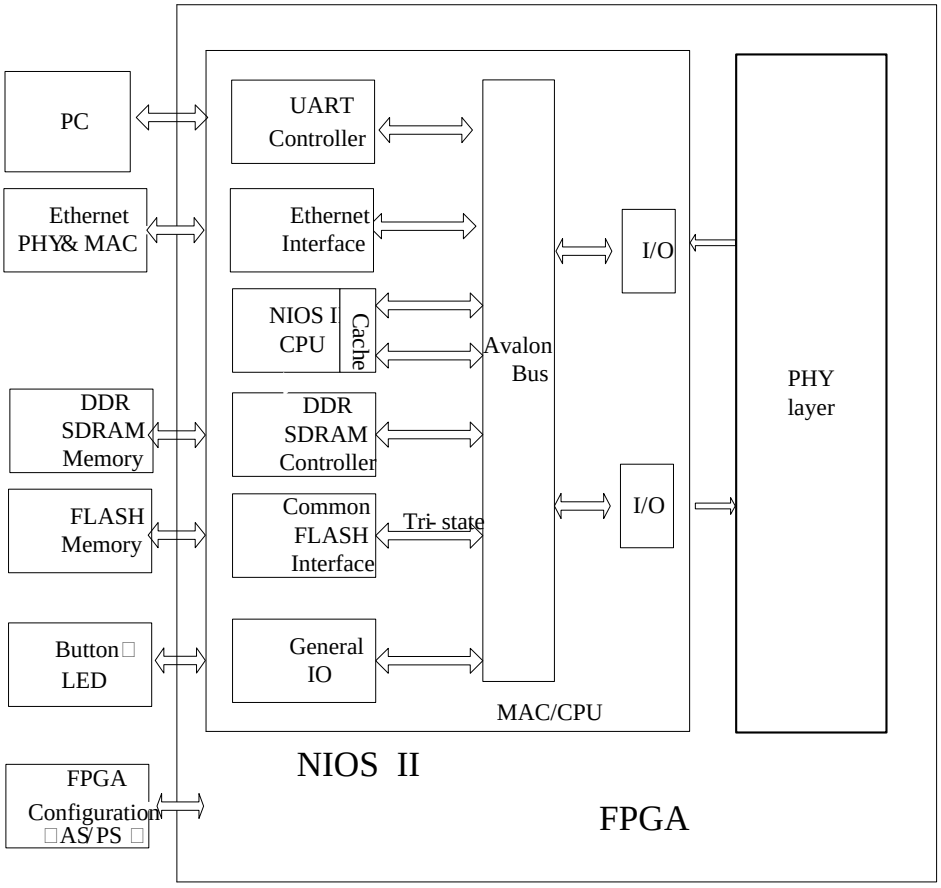

Figure 3. Block diagram of digital baseband circuit

The high-speed ADC is LTC2291. The LTC2291 is used to sample and hold differential input analog signal. The high-speed DAC is DAC902, which highest sampling rate is up to 165 MSPS. LTC1096/LTC2630 is low speed ADC/DAC,which is used for configuring the RF synthesizer. Altera EP3C16Q240 FPGA as the system controller and baseband processor, which is used for controlling ADC, DAC, encoding, decoding, modulating, demodulating. It can support complex digital system on a single chip at a low cost than ASIC. We use a 64Mbits MT48LC8M8A2 SDRAM and 128Mbytes Intel28F128 FLASH to extend data and program spaces. Besides, Ethernet, RS232 and JTAG interfaces are implemented in the digital baseband circuit.

c. Physical layer

FPGA implements the functions of CPU, transmitter and receiver. Transmitter and receiver function are belong to physical layer. The physical layer is described in verilog HDL language and implemented in FPGA. As shown in figure 4, the transmitter of the digital baseband consists of TMPI (Transmitter Message Passing Interface),buffer memory, CRC encoder, PIE encoder, preamble, frame-sync encoder and ASK modulator. When a command is transmitted, it is first padded with a CRC5 or CRC16 pattern and then encoded by PIE, using one of the three Tari values: 6.25 s, 12.5 s or 25 s. Tari depends on configuration parameters which received from the CPU. A preamble or frame-sync pattern is added at the beginning of the encoded packet. Finally, the digital baseband processor is responsible for detecting the bit boundary (timing synchronization) and the start of the packet (frame synchronization), the backscatter signals reply from the tag are FM0 or Miller-subcarrier encoded bits. The modulator converts the baseband signals to double sideband amplitude shift keying (DSB-ASK), single sideband amplitude shift keying (SSB-ASK) or phase reversal amplitude shift keying(PR-ASK) modulation. To satisfy the RF envelope of the EPC C1G2 protocol, the output signals of encoder pass through the pulse shaping filter before DAC. The transmitter procedure is controlled by transmitter control module. The two synchronizations use running windows to calculate the correlated value in the preamble frame. If the correlated value is bigger than a certain threshold, the bit boundary is found.

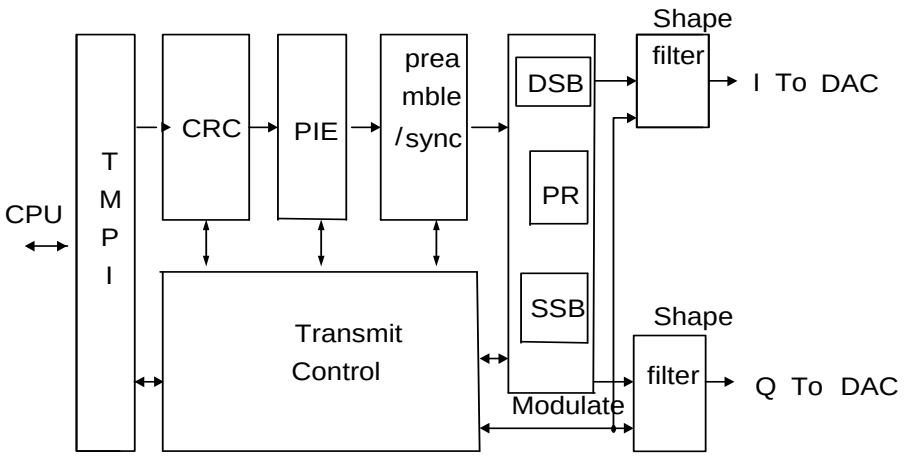

Figure 4. Block diagram of transmitter in baseband

For bit decoding, the correlated value compared with the threshold value is used to determine if a bit-0 or a bit-1 is received. The algorithm employed can be achieved with signal-to-noise ratio (SNR) of about 11 dB for FM0 and SNR at least 2 dB lower for Miller-subcarrier.

As shown in Figure 5, the Receiver of the digital baseband consists of RMPI(Receiver Message Passing Interface) and buffer memory ,FIR filter ,demodulator ,decoder ,CRC check and receive control block.

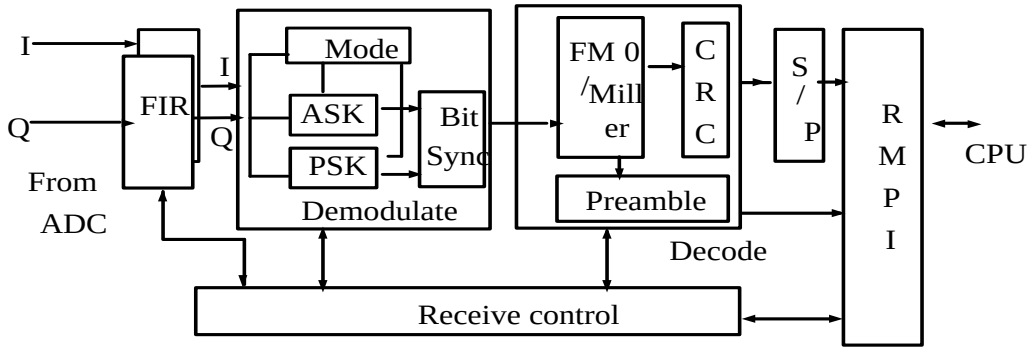

Figure 5. Block diagram of receiver in baseband

Receive control block is targeted for outputting control signal to each block. According to configuration register, receiver control block outputs the signals which include demodulation mode select,FM0 or Miller mode select, whether CRC check or not. After RF demodulating the tags' backscatter signals and ADC converting, the tag signals pass through FIR filter first, then they are demodulated. Demodulation mode is ASK or PSK, which could be decided by tag type. After that, bit synchronization circuit extracts clock information to synchronize the data and sends the data to decoder. The baseband receiver decoder is composed of a preamble detector and a decoder which is designed to decode FM0 and Miller codes. Except the general decoding procedure, the baseband decoder also detects collision occurrences and verifies whether there is a bit error or not. If CRC check is success without an error, the serial format data will be shifted to parallel format and be sent to RMPI (Receiver Message Passing Interface). At the same time, receiver produces RX buffer write, write address, write enable signal and the counts number of the data, puts the result to the certain registers to CPU.

d. MAC layer

The MAC layer is described in C language and implemented in NiosII core which embedded in FPGA. NiosII performs all commands and controls. This architecture is an advantage for implementing various kinds of RFID standards by changing the software of NiosII core. It

efficiently reduces the design and development time and cost, and achieves flexible and efficient way.

The MAC layer processes communication commands. A reader communicates to tag populations using three basic operations: Select, Inventory, Access. There are 14 commands to communicate with tag, including Select, Query, Query_adjust, Query_rep, Ack, Nak, Req_rn, Read, Write, Kill, Lock, Access, Block_write and Block_erase.

According to select command, the particular tag population based on user defined criteria will be selected. Query command initiates an inventory round and decides which tags will participate in the round query .Query command contains a slot-count parameter Q ,which make the tags to produce a random time slot. Query_adjust command repeats a previous query and may increment or decrement Q, but does not introduce new tags into the round. Query_rep command repeats a previous query without changing any parameters and introducing new tags into the round. Ack command is to acknowledge the tag. Nak command causes all tags in the inventory round to return to arbitrate without changing their inventoried flag. Rq_rn command is to obtain a new RN16. Read, Write, Kill, Lock,Block_write and Block_erase commands are to write or erase tags memory.

Figure 6 shows the implementation of the inventory procedure. First, the baseband CPU configures reader's mode, which including modulator and encoder configuration. The reader sends 5ms continues carrier wave to wake up the tags, then it sends Select command to select particular tag populations. After waiting for 300us carrier wave, the reader sends Query command. Query command initiates an inventory round, and the reader waits for the 16bit random number response. Reader sends Select command repeatedly when it is timeout. After getting RN16 from the tag, the reader sends ACK command to request tag's EPC. If reader could receive the EPC from the tag, then it will get the EPC from the buffer memory. Otherwise it sends Select command again.

As RFID tag is stored with a unique Electronic Product Code (EPC) and related product information, which raises important security and privacy issues. RFID tag and reader use wireless communication and the channel is considered not secure. In most standards, authentication feature are based on a simple password system or access control password, where security can be easily cracked by eavesdropping a password. In EPC global C1G2, the standard specifies that a tag has four memory banks: Reserved, EPC, TID, and User. 32-bit Access Password (APwd) and

32-bit Kill Password (KPwd) are stored in Reserved memory bank, and EPC number is stored in EPC memory.

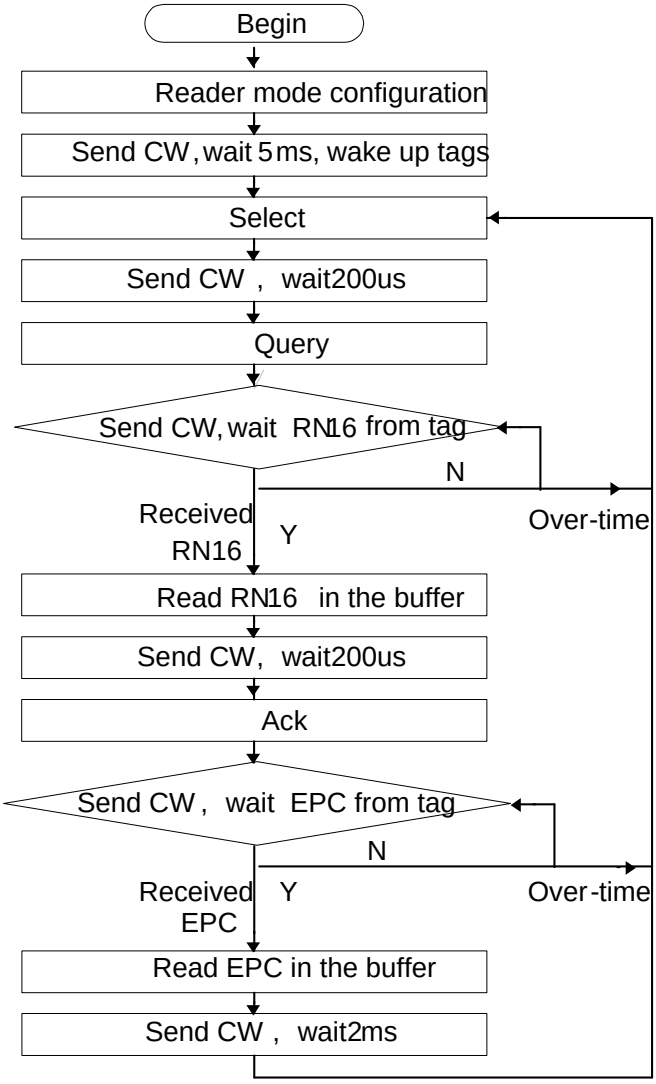

Figure 6. Inventory procedure

APwd and KPwd are protected because the reserved memory bank is not allowed to be read or written by any reader. APwd is used when data are needed to be exchanged between a reader and a tag. A compliant RFID reader can use KPwd to permanently disable the tag.

It is very easy to understand the multi-step procedure shown in Figure 7. RT1 and RT2 are random number, they use XOR operation to obscure APwd, which is known as Cover-Coding APwd (CCPwd). XOR operation shall be performed on APwd's 16-bit Most Significant Bits

(MSB) APwdM firstly, then be performed by 16-bit Least Significant Bits (LSB) APwdL. The cover-coding make the reader-to-tag communications more safety, as a reader performs an XOR operation for data encryption. Then, a tag can recover the received messages by doing another XOR operation. Assuming that the signals from a tag to a reader are too weak to be eavesdropped by the attacker, this cover coding scheme is an effective encryption scheme. However, an enhanced receiver or an implanted receiver near to a tag can make the cover-coding scheme useless.

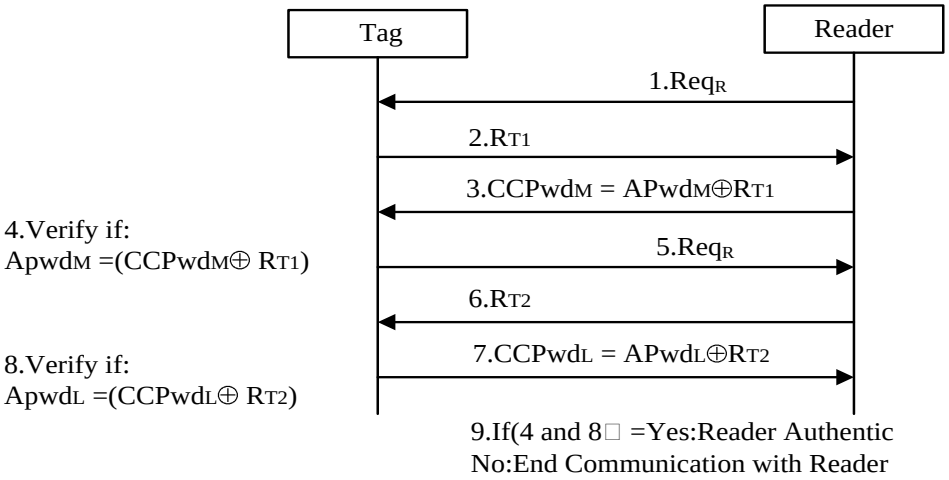

Figure 7. Authentication scheme between a reader and a tag

IV. EXPERIMENTAL RESULTS

The development platform Quartus II is embedded in Signaltap II Logic Analyzer. We could use Signaltap II Logic Analyzer to observe the function of FPGA internal circuits and capture the signals of the baseband circuit. Some verification results of baseband modules are shown below. The verification results of ASK demodulator are shown in Figure 8, When I signal is stronger than Q signal, I signal can be demodulated successfully. The verification results of FM0 decoder are shown in Figure 9 and the results of Miller decoder are shown in Figure 10. The verification results of bit synchronization module are shown in Figure 11. Synchronous data can be successfully extracted from the input data and clock signal.

In RF transmitter, the signal generator generates RFID baseband PIE coded signals, such as Read command 1100001011100111110000001. Zero symbol length of time of Tari is set to 25us and

transmission rate is 40Kbps. When the signals is encoded and input to RF system, the rate is 80Kbps. Access by the differential I/Q quadrature signals to the up-conversion, after a pre-amplifier and power amplifier, the output RF signals go through a 30dB attenuator and enter into the spectrum analyzer. The spectrogram of RF signal is shown in figure 12. The spectrum Span is set to 1MHz and channel width is 500KHz. Channel power is about 24dBm. Power spectral density is 65.24dBm/Hz and the coaxial cable loss is about 2dB. The power of the RF output signal is less than the expected power approximately 3dB, but it is still in the adjustable range of the output power.

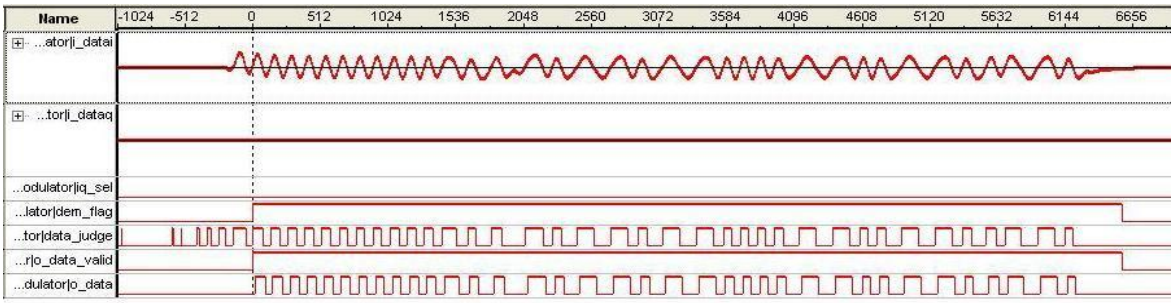

Figure 8. The verification results of ASK demodulator

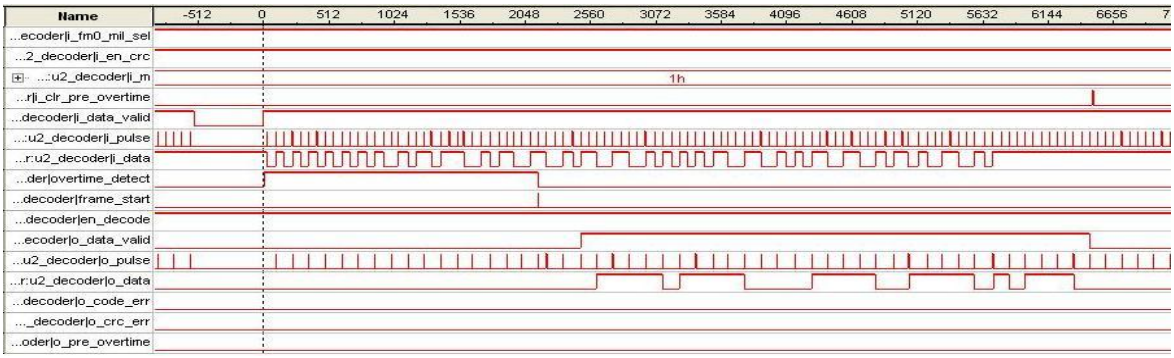

Figure 9. The verification results of FM0 decoder

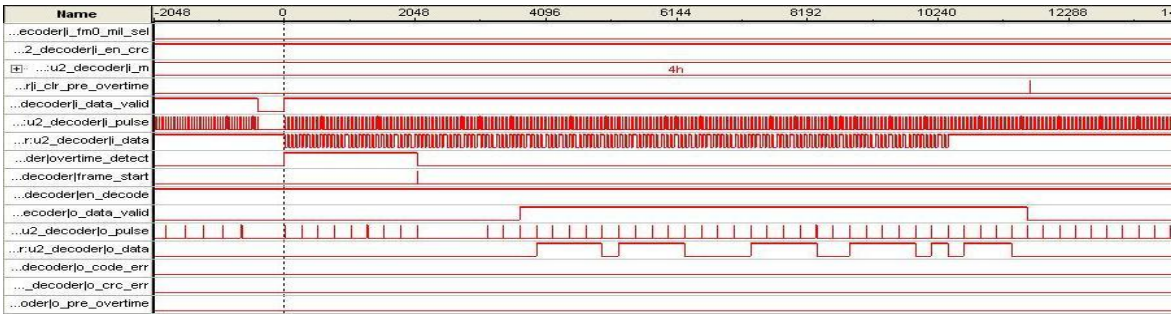

Figure 10. The verification results of Miller decoder

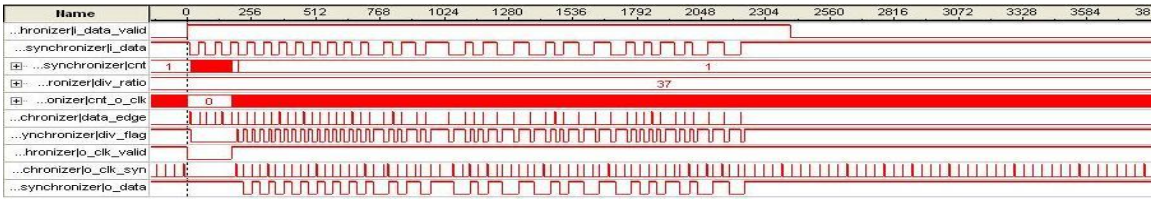

Figure 11. The verification results of bit synchronization

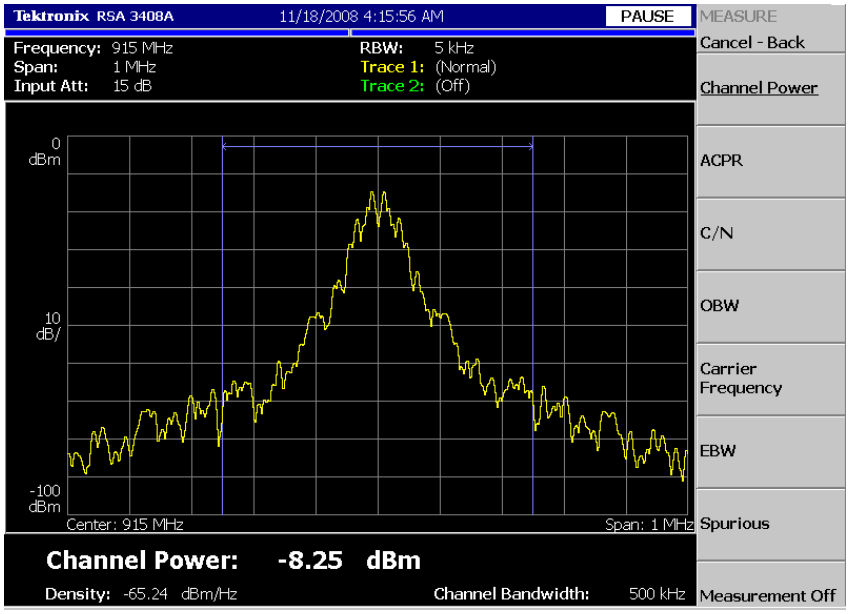

Figure 12. The spectrogram of RF transmission signal

In the RF receiver, the reader receives the backscatter signals of the tag. The signals are encoded in FM0 with a rate of 80kbps.After frequency conversion by the 915MHz signal generator ,the power of received signal is -70dBm,as shown in figure 13.

The received RF signals are down converted to the baseband frequency by the quadrature demodulator, and then amplified by an operational amplifier and filtered by the low pass filter. After FM0 decoding, the received data are 000000000000(12 preamble codes) 1010V1 (synchronous preamble codes) 0100010000000101 (the RN16 returned by tag). The final baseband waveforms of received signals are shown in figure 14. The demodulated signals are completely match with original command and the signals' amplitude is satisfied with the sampling requirements of the ADC.

The waveform of transmitting signal from reader and the waveform of backscatter signal from tag could be captured by the spectrum analyzer. The communication process between the reader

and tag is shown in Figure 15. Select and Query commands are sent by reader, then the tag responses with RN16.When the reader sends ACK, it will get EPC from the tag.

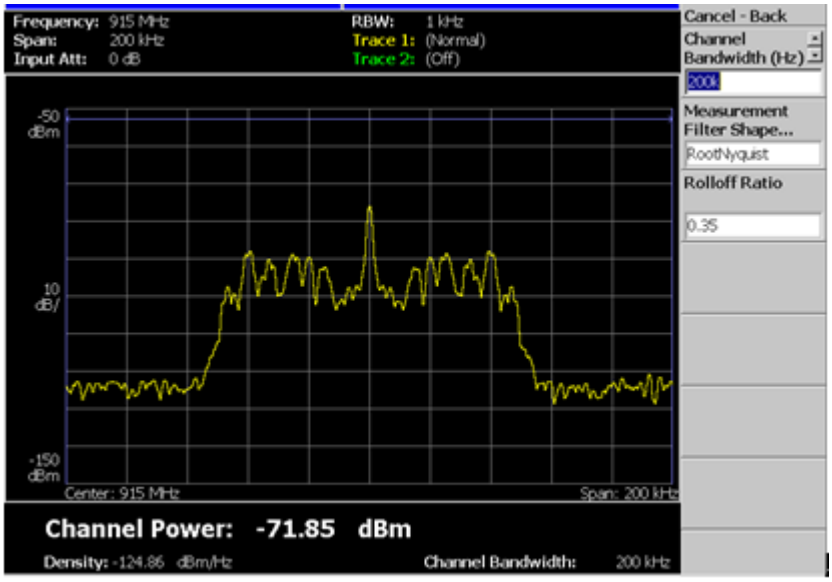

Figure 13. The spectrogram of RF received signal

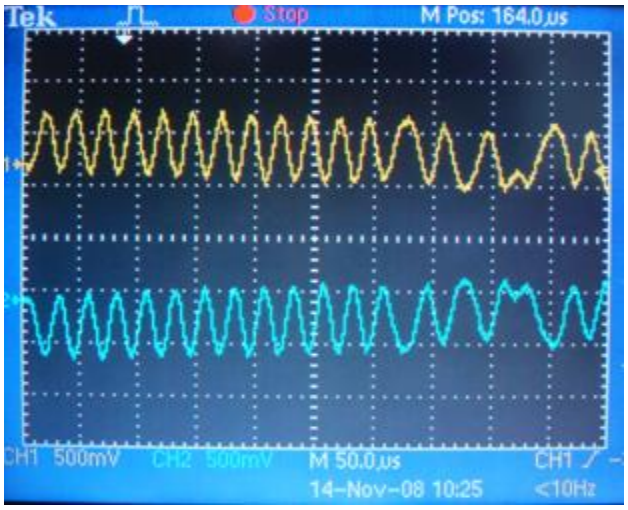

Figure 14. The baseband waveforms of received signals

Software in NIOS II continuous read the tag's EPC information and sends the tag's EPC to the host computer via an RS232 interface. Computer uses UART software to responsible for receiving from the NIOS II information. If the reader correctly reads the tag's EPC Information, then it displays the EPC data and length. If the reader can not correctly read the tag EPC information, it displays an error. For example, when waiting timeout, violations of FM0/Miller coding rules error or CRC checksum error happened, it displays an error. During the debug

process, adjusting the distance between the reader and the tag, the reader can correctly read the tag's EPC information within 3 meters .The results verify the reader could meet the design requirements.

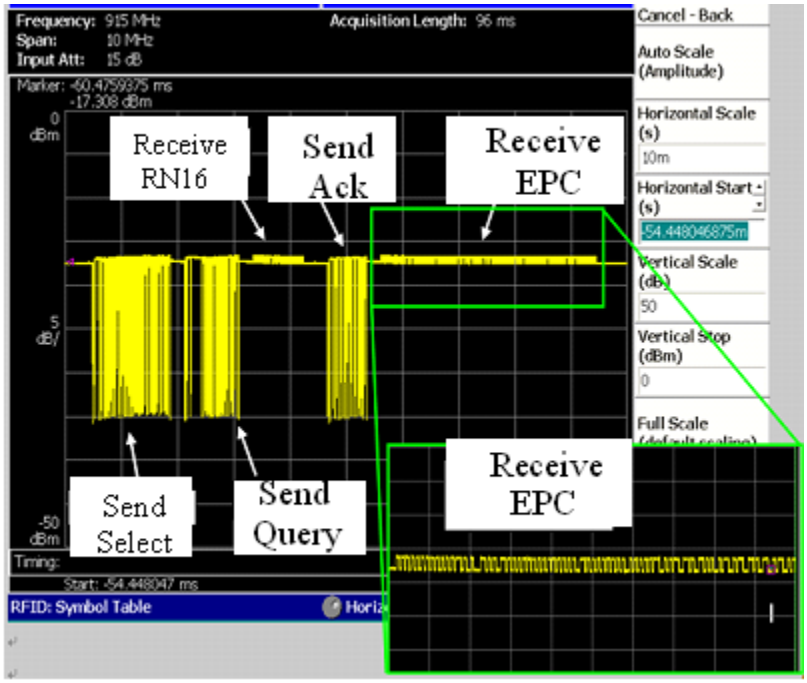

Figure 15. Communication between the reader and tag

V. CONCLUSIONS

This paper presents design and realization of a UHF RFID reader, which is compatible with EPC C1G2 Standard. The experimental results demonstrated that the reader could send commands and receive data from the tag correctly. The designed reader's architecture is not only applicable for EPC C1G2 protocol, but also applicable for other RFID standards. The ISO18000 6A/6B/6C protocols share the same uplink configuration, which is similar with EPC C1G2, but they differ in the downlink modulation and anti collision approach, however they could also be realized in this platform. The FPGA is a system controller and baseband processor .It could be flexible adjusted to implement physical layer of different protocol. The NiosII core in FPGA performs all commands and controls and could achieves rapid, flexible and efficient development. Since all standard dependent properties could be mapped into reconfigurable hardware components in FPGA. We use verilog HDL language to implement the MAC layer of EPC C1G2 protocol with all the states, commands and functions. We will focus on the development of a framework

supporting multiple receive and transmit antennas to enable MIMO RFID systems in future work. By this means it is expected to greatly improve the detection range and the data rate. We observe that EPC C1G2 protocol lacks the security features to make the EPC-ID secure or to have a mutual authentication between the tags and reader. Hence there is a need to integrate security protocol with the EPC C1G2 to have a secure communication.

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