



## DESIGN OF SRAM ARCHITECTURE WITH LOW POWER WITHOUT AFFECTING SPEED USING FINFET

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*Abstract- In average 8T SRAM Architecture, it requires maximum number of transistor counts and does not need any write back scheme. To achieve the higher word line (WL) Voltage, the bit line (BL) is connected to the gate of the read buffer SRAM Architecture. That boosted voltage is not used when the threshold voltage is high. Its leads to the reduction of read stability of the SRAM Design. In that case, the gate terminal of the SRAM Architecture is not connected to the buffer results a large delay. To overcome the disadvantage of the average 8T SRAM architecture, the 6T SRAM Design is proposed. In proposed 6T SRAM Design, the number of transistor counts and Power is reduced than the existing design. Various factors of the proposed SRAM Architecture, which stores multiple bits in terms of power and transistor counts. The simulation of 6T SRAM design is carried out in S-Edit and the synthesized in T-Spice.*

**Index terms:** Static random access memory (SRAM), Low voltage operation, Low power consumption,

## I. INTRODUCTION

In this work we examine methods to incorporate flexibility into the circuits and architecture of low power systems. SRAMs are widely used as cache memories for storage in microprocessors because of their high speed operation and low power dissipation circuits. The standard architecture of 6T (6 Transistor) SRAM based cell continues to play a major role in all VLSI systems due to its short access times and full compatibility with FinFET technology. The rapid shrinking of transistor sizes according to Moore's Law [1] has propelled integrated circuits (ICs) into a power-limited era [1]. Figure 1. Shows the SRAM function.

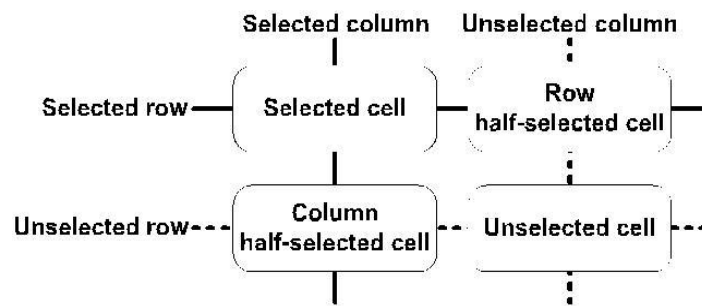


Figure 1. SRAM Function

In recent years, with the widespread usage of battery powered application, low power operation has become a critical issue associated with system-on-chip (SoC) design. The amount of embedded SRAM in modern Systems on-Chips (SoC) increases the performance requirements in each technology. A low-power SoC can be effectively realized with a low-power static random access memory (SRAM) because the SRAM critically affects the total power of the SoC. Further, power reduction can be effectively achieved by decreasing the operating voltage because of the quadratic dependence of power on the operating voltage in FinFET technology [2]. The amount of embedded SRAM in modern Systems on-Chips (SoC) increases to meet the performance requirements in each technology generation [3].

Low power design is a buzzword that days and designing with low power requirements has been always an important aspect of video applications. The overarching reason why the low power design is becoming very important today for increasing of leakage current with the shrinkage of device dimension. Low power design is indispensable to realize battery operated systems. Due to the limited size of handheld devices, it is not possible to use larger batteries on it and short battery life time of a smaller battery limits then use of them [4]. Therefore low power

design is very essential for extending the battery life time. Most of the digital devices consists of memories and hence reducing power consumption of memories as well as area reduction is paramount important as for today to improve speed and performance, efficiency and reliability. One of the effective ways to reduce the dynamic power consumption is lowering the operating voltage due to its quadratic relationship [5]. This trend is continuing also for real time video System on Chip (SoC). Two aspects are important for SRAM cell design: (i) the cell area and (ii) stability of cell. Nowadays this technology power dissipation in the memory circuits has become an important design consideration. As technology scaling, more devices are integrated into the system, as a result the corresponding leakage power also increases. Lower power voltages and smaller device dimensions have a significant effect on data stability, dynamic power consumption and leakage power in SRAM cell [6].

The remainder of this paper is organized as Section 2 describes and analyzes the average-8T SRAM Architecture. Section 3 describes the structure and operation of the proposed 6T SRAM architecture. In this section 4, the proposed 6T SRAM architecture is simulated and compared with the average-8T SRAM architecture, based on the 45-nm FinFET technology. Section 5 summarizes the conclusion of this paper.

## II. AVERAGE-8T SRAM ARCHITECTURE

In the average-8T static random-access memory (SRAM) has a competitive area and does not require a write-back scheme. In the average-8T SRAM architecture, a full-swing local bitline (BL) is connected to the gate of the read buffer that can be achieved with wordline (WL) voltage. However, in the case of an average-8T SRAM based on an advanced technology, such as a 45-nm FinFET technology, the variation in threshold voltage is large and the boosted WL voltage cannot be used, because it degrades the read stability of the SRAM. Thus, a full-swing local BL cannot be achieved by the full supply voltage ( $V_{DD}$ ), resulting in a considerably large read delay.

An advantage of the average-8T SRAM architecture is that it does not require a write-back scheme for bit-interleaving, and it exhibits a competitive area. However, in the case of an average-8T SRAM architecture based on an advanced technology such as a 45-nm FinFET technology, full-swing LBL cannot be achieved owing to the tradeoff between the read stability and the read delay. Thus, the gate of the read buffer cannot be driven by a full  $V_{DD}$ , resulting in a considerably large read delay in a low-voltage region. Further, the RBLs in the unselected

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### III. PROPOSED MODEL

#### 3.1 6T SRAM CELL DESIGN

The proposed 6T SRAM stores multiple bits in one block, as in the case of an average-8T SRAM. Figure 3.1. Shows the architecture of the proposed 6T SRAM that stores  $i$  bits in one block. The minimum operating voltage and area per bit of the proposed 6T SRAM depend on the number of bits in a block. A configuration that stores four bits in one Block is selected as the basic configuration by considering the balance between the minimum operating voltage and the area per bit, which will be described in Section 4.

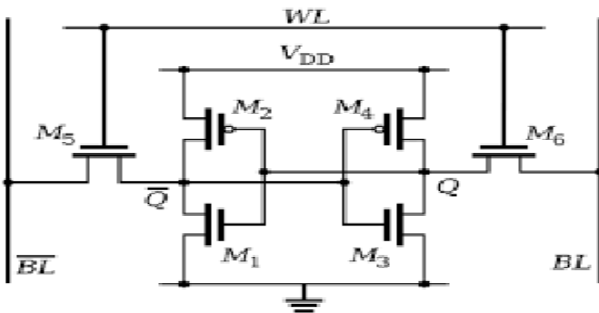


Figure 3.1. Proposed 6T SRAM Architecture

The basic configuration of the 6T SRAM cell design uses bi-stable latching circuitry to store a bit (M1, M2, and M3 & M4) and two access transistors (M5 & M6). Word Line (WL) is connected to the access transistors at their consecutive gate terminals. WL is used to select the cell. Source/Drain terminals are connected to the Bit Lines (BL & BLB), which are used to perform the read and write operations on the cell [7]. The problem produced with bulk MOSFET based 6T SRAM cell during read operation is, when the WL is turned ON, it raises the output voltage at node that stores 0, which turn ON the opposite inverter pull down transistor, when this happens the voltage at node which stores "1" will be reduced. This voltage may drop little, but it should not fall below the threshold voltage. If it drops below the threshold voltage of MOSFET, it leads to read destructive operation. Due to this stability of the 6T SRAM cell will be degraded. The operation of writing is delivered by forcing one bit line low while other bit line remains at about

,which could leads to enhancement in dynamic power consumption. While technology scaling, in the latently coming manufacturing process the operating voltage and threshold voltage decrease and it demolishes the stability of the SRAM cell. Due to the direct paths between bit lines to the store the various nodes, the data stored in conventional SRAM cell easily deteriorated by the external noise variously. Based on the above reasons bulk MOSFET based 6T SRAM cell is not applicable for real time video applications [8]. Hence we require a new design for high stability, low dynamic and leakage power.

The head switch and cross-coupled pMOSs of the proposed 6T SRAM are notable differences from the average-8T SRAM. WLS (WL1~4), the block select signal (BLK), and the read WL (RWLB) are row-based signals, whereas the write WL (WWL), write BLs (WBL and WBLB), and read BLs (RBL and RBLB) are column-based signals. During the hold state, WLS, WWL, and WBLs are held at 0 V. BLK is held at VDD to connect the WBLs and the LBLs, so that the LBLs are discharged to 0 V and the read buffers are turned OFF. Further, the RWLB is also held at VDD to turn OFF the head switch and to eliminate the RBL leakage current.

### **3.2. Read Operation**

The read operation of the proposed 6T SRAM architecture is shown in Figure 3.2. This operation is performed in two phases. During the first phase, BLK of the selected block is forced to remain at 0V, and the selected WL is enabled. On the basis of the stored data, although the voltage of the LBL that is connected to the 1 storage node becomes high, its value cannot be as high as that of the full VDD because of the  $V_{th}$  drop through the pass gate transistor, and the voltage of the other LBL remains low. The read operation in the first phase is similar to that of the average-8T SRAM, except that the RBL is not discharged because the RWLB is high in the first phase. With the assertion of WL, although the 1 storage nodes is disturbed, the read disturbance is small because of the small capacitance at the LBL. This smaller read disturbance makes the proposed 6T SRAM be able to operate in significantly lower operating voltage compared with average-8T SRAM architecture. The second phase starts with the falling of the RWLB. The assertion of the RWLB enables not only the discharge of the RBL but also the feedback of cross-coupled pMOSs. Positive feedback of the cross-coupled pMOSs increases the LBL to the value of the full VDD, owing to which the LBL can achieve a full swing, and the gate of the read buffer is driven by the full VDD, without the need for a boosted WL voltage. Thus, in the case of the proposed 6T

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SRAM based on an advanced technology, the suppressed WL voltage can be used to enhance the read stability, without degrading the read delay. In other words, the advantage of the proposed SRAM architecture is that it eliminates the tradeoff between the read stability and the read delay. The suppressed WL voltage is used to enhance the read stability, and the full-swing LBL minimizes the read delay. In the case of the average-8T SRAM architecture, the read buffer consists of two stacked nMOSs that reduce the RBL leakage. On the other hand, in the proposed 6T SRAM architecture, a single nMOS is used as the read buffer to increase the read current, and the buffer foot is attached to reduce the RBL leakage. The column half-selected block is in the hold state in which the read buffers are turned OFF, so that the RBL discharge is not affected by the column half-selected block. When both the BLK and the WL are simultaneously high, the 1 storage node and the WBL that is held at 0 V are connected, causing the data to flip. Thus, the WL should increase after the fall in the BLK is completed. For the robustness of the positive feedback of the cross-coupled pMOSs despite of the variation in  $V_{th}$ , a sufficient LBL development is needed. Thus, the RWLB should be asserted with a sufficiently large timing margin after the WL is asserted; this requires an additional timing overhead, which does not exist in the average-8T SRAM.

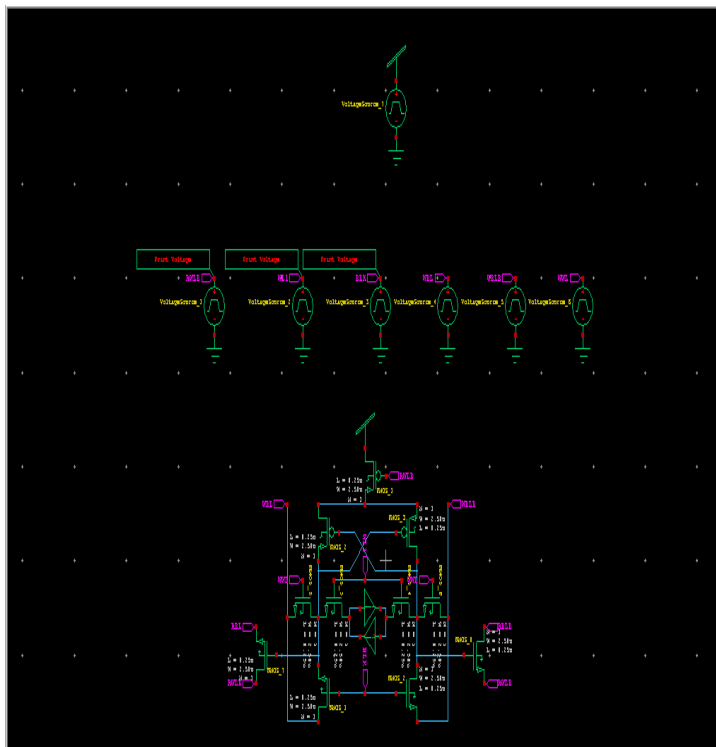


Figure 3.2. Read Operation of 6T SRAM Architecture

As in the case of the average-8T SRAM architecture, in the proposed 6T SRAM architecture, it is essential to carefully control the signal timing to avoid the data from flipping, as shown in Fig. 3. When both the BLK and the WL are simultaneously high, the 1 storage nodes and the WBL that is held at 0V are connected, causing the data to flip. Thus, the WL should increase after the fall in the BLK is completed. For the robustness of the positive feedback of the cross coupled pMOSs in spite of the variation in  $V_{th}$ , a sufficient LBL development is required. Thus, the RWLB should be asserted with a sufficiently large timing margin after the WL is asserted; this requires an additional timing overhead, which does not exist in the average-8T SRAM. An important point to note here is that the total read delay of the proposed SRAM based on an advanced technology such as the 45-nm FinFET technology is considerably lesser than that of the average-8T SRAM because the LBL of the average-8T SRAM architecture cannot achieve full swing, and its read buffer consists of two stacked nMOSs.

### **3.3. Write Operation**

The write operation of the proposed 6T SRAM architecture is shown in Figure 3.3. As shown in this figure, BLK of the selected block is forced to remain at 0V, and the selected WL is enabled. Develop, the WWL is forced to remain at VDD so that the write access transistors are turned ON, and the WBLs are forced to remain at a certain voltage level on the basis of the write data. Both the storage nodes are connected to the WBLs through pass gate transistors and write access transistors. Thus, the write operation is differential, and the write ability of the proposed SRAM is better than that of the average-8T SRAM, whose write operation is single-ended.

The row half-selected block shown in Figure 3.3 is in the same condition as it was in the read operation, except that the RWLB is high. Although the storage nodes of the row half-selected blocks are disturbed during the write operation, the disturbance is small because of the small capacitance at the LBL. Thus, the stability of the row half-selected block is ensured without the need for a write-back scheme. Further, in the case of the average-8T SRAM architecture, during the write operation, the RBLs in the unselected columns are unnecessarily discharged because the row half-selected block is in the same condition as it was in the read operation, resulting in the consumption of a large amount of dynamic power. In this regard, the advantage of the proposed 6T SRAM is that it eliminates the unnecessary RBL discharge by using a buffer foot that is forced to high during the write operation.

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Unlike in the case of the average-8T SRAM architecture, in the proposed 6T SRAM architecture, the sources of the block mask transistors are connected to the WBLs, not to VSS, to eliminate a dc current path in the column half-selected block. When the sources of the block mask transistors are connected to VSS, the dc current flows from a high WBL to VSS through the write access and block mask transistors in all the column half-selected blocks where BLK and WWL are high, resulting in the consumption of a large amount of static power during the write operation. The dc current path in the column half-selected block is eliminated by connecting the sources of the block mask transistors to the WBLs.

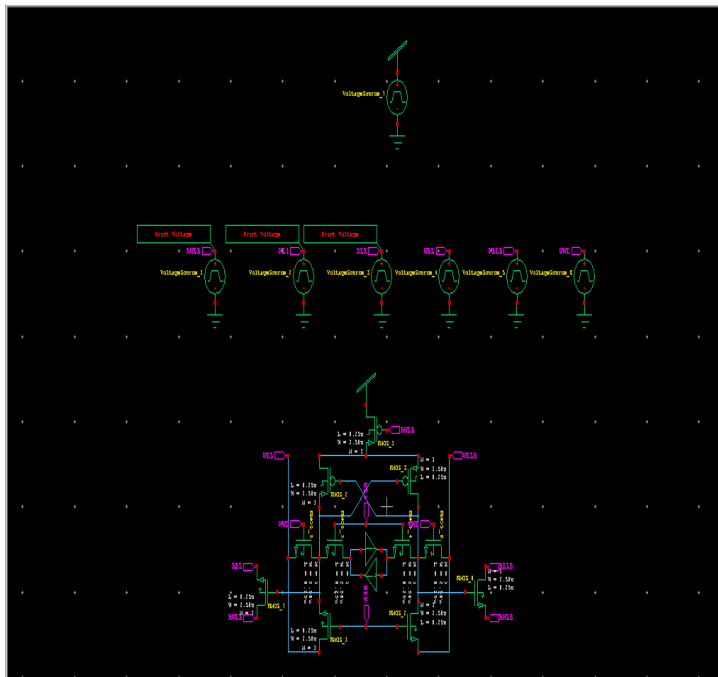


Figure 3.3. Write Operation of 6T SRAM Architecture

### 3.4 Layout and area

In the layout of the 6T SRAM architecture, the four cells are located at each corner of the layout, and not in one line, and the additional transistors are placed at the center of the layout. This folded column layout configuration and contributes toward a decrease in the



RBL capacitance of the average-6T SRAM architecture. The schematic design of the proposed 6T SRAM architecture is shown in figure 3.4.

However, this folded column then configuration is not applied to the proposed SRAM architecture to reduce its area even though the RBL capacitance increases. In the layout of the basic configuration of the proposed SRAM architecture based on the 45-nm FinFET technology, designed with the smallest transistors. The local interconnect in the middle of line is employed to reduce the number of metal layers. VDD and VSS are routed in metal 1; the LBLs are routed in metal 2; the BLK and RWLB are routed in metal 3; the RBLs, WBLs, and WWL are routed in metal 4; and the WLs are routed in metal 5.

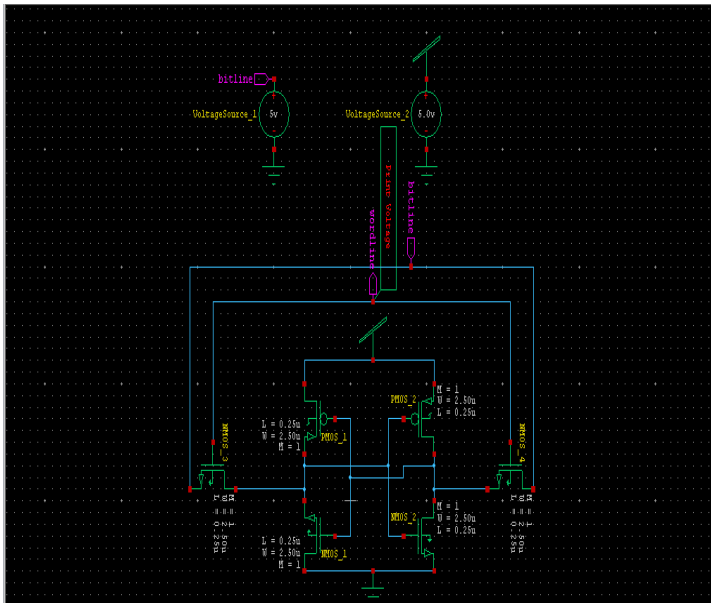


Fig 3.4: Schematic design of Proposed 6T SRAM Architecture

The area of the proposed SRAM that stores two bits in one block is greater than that of the 8T SRAM cell. However, the area per bit of the proposed SRAM that stores four bits in one block is 27% lesser than that of the 6T SRAM cell and slightly lesser than that of the average-8T SRAM, despite the fact that a greater number of transistors are attributed to the use of the head switch and crossed coupled pMOSs.

#### IV. EXPERIMENTAL RESULTS AND ANALYSIS

The architecture of the proposed SRAM is verified by the HSPICE Monte Carlo simulation using a BSIM-CMG FinFET model. The characteristics of this model are fitted to those of a commercial low-power device based on the 45-nm FinFET technology [9].

##### **4.1 Minimum Operating Voltage**

The Synthesis transistor counts result for proposed 6T SRAM architecture is shown in figure 4.1.1. An assist circuit contributes toward a decrease in the minimum operating voltage of an SRAM. In this regard, several types of assist circuits exist. For example, boosted cell supply voltage (VCELL), negative VSS, suppressed WL, and suppressed BL read assist circuits improve the read stability of an SRAM. On the other hand, suppressed VCELL, boosted VSS, boosted WL, and negative WBL write assist circuits enhance the write ability of an SRAM. The boosted VCELL, negative VSS, and suppressed BL read assist circuits are column-based, while the suppressed WL read assist circuit is row-based. If the boosted VCELL or negative VSS read assist circuit is used in the proposed SRAM architecture, during the write operation, read assist will be applied to all the unselected columns because the row half-selected blocks are in the same condition as they were in the read operation, resulting in the consumption of a large amount of power. The suppressed BL read assist circuit cannot be applied to the proposed SRAM architecture, because it is essential for the LBLs of the proposed SRAM to be precharged to 0 V to turn OFF the read buffer in the column half-selected block. Thus, the suppressed WL read assist circuit is applied to the proposed SRAM architecture. The Synthesis power result for proposed 6T SRAM architecture is shown in figure 4.1.2.

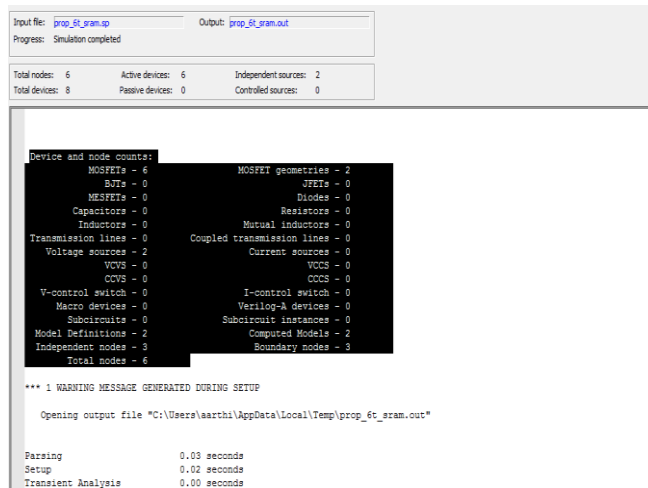


Figure 4.1.1. Synthesis transistor counts  
 Results for proposed 6T SRAM Architecture

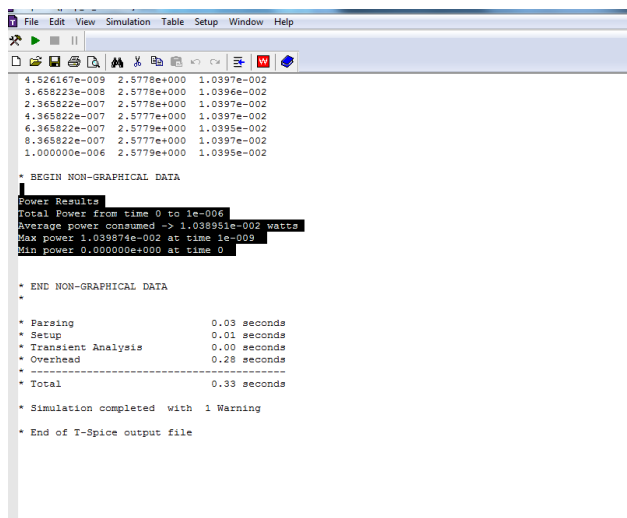


Figure 4.1.2: Synthesis power  
 Results for proposed 6T SRAM Architecture

Likewise, the suppressed VCELL, boosted VSS, and negative WBL write assist circuits are column-based, and the boosted WL write assist circuit is row-based. If the suppressed VCELL or boosted VSS write assist circuit is applied, not only the wire capacitance but also the storage node

Design of sram architecture with low power without affecting speed using finfet capacitances in all the column half-selected cells will be charged and discharged, resulting in the consumption of a large amount of dynamic power. The boosted WL write assist circuit cannot be applied to the proposed SRAM because the WL is already used as the suppressed WL read assist circuit. Thus, the negative WBL write assist circuit is considered to be the most suitable write assist circuit for the proposed SRAM architecture.

#### 4.2 Energy and Power consumption

The average energy consumption per operation is measured in a 256 rows  $\times$  128 columns SRAM array with 3-to-1 bit interleaving at a minimum operating voltage of 0.4 V. Despite the fact that the proposed SRAM exhibits a higher RBL capacitance than the average-8T SRAM, as mentioned in Section 3, the proposed 6T SRAM consumes a considerably smaller amount of read energy than that consumed by the average-8T SRAM because the exceedingly long read delay of the average-8T SRAM causes a large active leakage. Further, the write energy of the proposed 6T SRAM is considerably lesser than that of the average-8T SRAM because the unnecessary RBL discharges in the unselected columns are eliminated in the proposed SRAM. Figure 4.2.1. Tabulation for Existing and Proposed Results

DESIGN	FACTO R	EXISTIN G DESIGN	PROPOSE D DESIGN
AVERAGE 8T SRAM DESIGN	Transist or Counts	32	6
PROPOSE D 6T SRAM DESIGN	Power	6.09e-002 Watts	1.03e-002 watts

Figure 4.2.1. Tabulation for Existing and Proposed Results

The standby power is measured at a minimum data retention voltage, which ensures the  $5\sigma$  hold stability yield. The minimum data retention voltages of the average-8T and the proposed 6T SRAMs are identical at 0.24 V. In the standby mode of the average-8T SRAM architecture, the BLK, WLs, and WBLs are held at 0 V, whereas the RBLs are set to a high-impedance mode. Figure 8.shows the tabulation of the existing and proposed results, where the BLK, WLs, and WWL are held at 0V, and the RBLs and RWLB are held at VDD, whereas the WBLs are set to a high-impedance mode. Unlike in the case of the average-8T SRAM architecture, in the proposed 6T SRAM architecture, although thecross coupled pMOSs form additional leakage paths, the leakage paths through the write access transistors are eliminated. Consequently, from the result of the simulation, the average standby power of a 256 rows  $\times$  128 columns SRAM array is approximately identical at  $1.03 \mu\text{W}$  for both the SRAM architectures. Figure 4.2.2. Shows the Graphical representations for Existing and Proposed Design

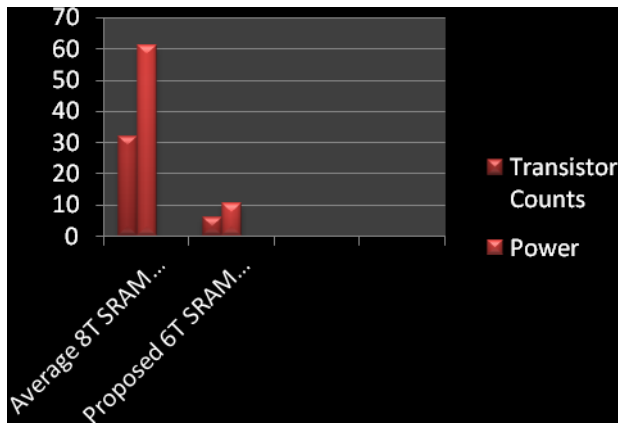


Figure 4.2.2. Graphical representations for Existing and Proposed Design

## V. CONCLUSION

In our proposed 6T SRAM architecture is that it does not require a write-back scheme for bit-interleaving, and it exhibits a competitive area. However, in the case of an average-8T SRAM architecture based on an advanced technology such as a 45-nm FinFET technology, full-swing LBL cannot be achieved due to the tradeoff between the read stability and read delay on it. Concurrently in addition, the unwanted RBL discharge during the write operation is eliminated by using the read buffer with a buffer foot, resulting in the saving of power during the write operation. Consequently, it can be concluded that the proposed 6T SRAM based on the 45-nm FinFET technology exhibits a considerably smaller read delay and consumes less energy with a slightly smaller area than the average-8T SRAM. The power has been consumed only because of the reduction in the transistor counts.

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