
# DESIGN OF LOW COMPLEXITY ACCUMULATOR USING FINFET FOR VARIOUS TECHNOLOGIES

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***Abstract- FINFET terminological in exactitude process reuses a massive part of well accustomed conventional CMOS process. FINFET is a likely-look alternative to conventional MOSFET which has reached its limit and has too much leakage for too little performance gain. FINFET is being suggested as basics for future IC processes because its power or performance benefits, scalability, superior controls over short channel effort etc., In this paper we propose a outlook for scheming accumulator using FINFET for purpose of minimize number of transistor differentiate to CMOS logic. In circuit level, widely used D flip-flop and at constructional level the full adder cells of FINFET (dual gate transistor) 10T can be used. FINFET is the most propitious double gate transistor, forecast as one of the candidate to restore the epic MOSFET. FINFET technology power consumption is compare with CMOS technology to analyze how the area, delay and power can be reduced.***

**Index terms: FINFET (FIN field effect transistor), CMOS (Complementary Metal oxide semiconductor), accumulator, low power consumption, reduce delay.**

## I. INTRODUCTION

Conventional MOSFETs have an indelible problem for large leakage current for gate to channel increasingly unconvincing transistor characteristics. The integrated circuit technology is flourishing at a serious stride since the origination of first MOS microprocessor in 1970. The prime driving force beyond this development is the technique of scaling. The scaling of MOS transistor has evolve in high density, high performance chips. But this miniaturization is obstructed by much awful case that emerges in MOS device as the device size goes on shrinking. Out of this concern, power dissipation is an extensive complication. CMOS has been used widely in current technologies, but it cause the short channel effect such as DIBL, GIDL, channel length Modulation, mobility degradation etc., In view of the barrier in planar CMOS transistor scaling to preserve tolerable gate to a channel control FINFET based accumulator has been proposed as technology option for restore the existing CMOS technology. The enchantment of FINFET consists in the realization of self-aligned double gate devices with a conventional CMOS process shown in figure-1. This entitle extending the gate scaling following the planar transistor restriction, maintaining a better accomplishment due to low doping concentration in the channel. In this work the area, delay and power consumption of FINFET accumulator are examined. This result of FINFET accumulator is compared against CMOS based accumulator.

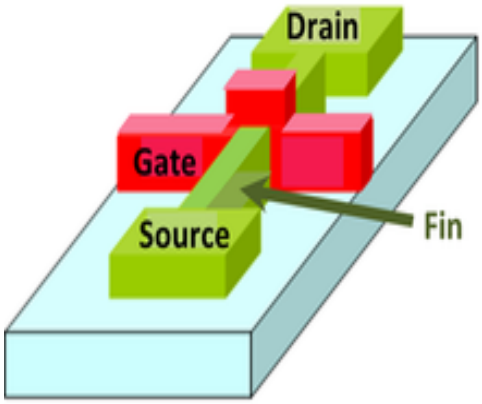



Figure.1 FINFET dual gate transistor

In second section discuss about the proposed model of FINFET. The third section describe about explanation of D Flip-flop, full adder and accumulator using FINFET. The fourth section gives the output of accumulator and at last conclusion of the result analyses will be declared.

## II. Proposed model

FINFET is a most advanced technology in VLSI (very large scale integration) which replaces bulk CMOS technology. In this proposed model, CMOS accumulator is replaced by a FINFET accumulator to show the reduction in power consumption, area, delay and improvement in the performance of the accumulator. The term accumulator is used in a widely variety of non-computing application and activities, such as electrical engineering (an energy storage device such as rechargeable battery or ultra-capacitor) hydraulics (mechanical energy storage devices), in stack trading (a contract or agreement) and even in gambling (parlay bet). Accumulator is a register for short term, intermediate storage of arithmetic and logic data in a computer's CPU (central processing unit). The most elementary use for an accumulator is adding a sequence of numbers. The numerical value in the accumulator increase as each number is added, exactly as it happens in simple desktop calculators. Once the sum has been determined, it is written to the main memory or another register.

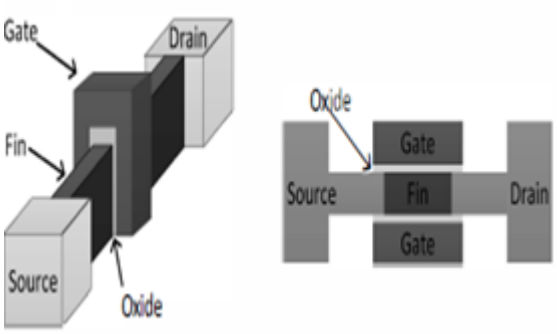



Figure.2

a) Three dimension structure b) Cross section top view

Here in this proposed paper accumulator is designed with FINFET D flip-flop and FINFET full adder and hence the result is showed in MODEM SIM software in percentage compared with CMOS accumulator. Intension of this paper is to reduce the power consumption, delay, numbers of transistor and area.

**2.1 FINFET Technology**

FINFET is mostly used in a current technology. It is a quasi-planar effect transistor and the working principle is similar to the planar MOSFET. The effective width of the FINFET is 2nHfin.FINFET gate consist of double gate transistor and it optimize the power and performance. Here the double or multiple gates can be used to enhance the electrostatic control. In the conventional planar transistor current flows through the circuits depends only the width of the device (W).Width is the half of the channel length. If the channel scale is down, it necessary to

decrease channel length and transistors which improves the performance of the transistor. In Figure.2 shows that three dimensional structure of FINFET which consists of source, drain, gate and cross section top view shows that dual gate transistor. FINFET has advantage of reduction in leakage power, operating power, leakage current, transistor gate delay, reduced threshold gate level.

**2.2 Full adder**

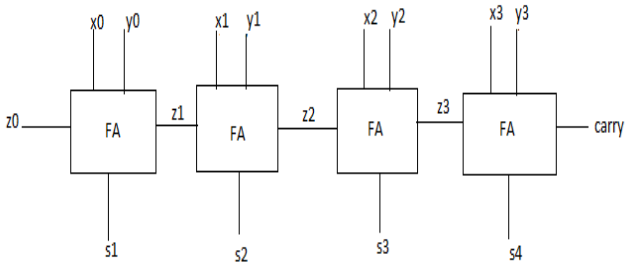
Adders have become an important part in this world; there is no design without adder. In VLSI adders used a basics component. Full adder is a combinational circuit that performs the addition operation of inputs bits. Full adder is a core of much digital and analog circuit. It is used as major furbearing circuits for many digital designs. Full adder circuits are analysed for low power consumption, reduced delay and low power products. Design of full adder speed is restricted by size of the transistor, parasitic capacitance and delay in the critical path. The truth table for full adder is given in table1.

Table 1. Truth table of full adder

| X | Y | Z | Sum | Carry |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**2.3 Full adder using FINFET**

Dual gate FINFET has two electrically independent gates, which gives circuit design more flexibility in design low power and reduced the number of transistor. Field effect transistor full adder have indicated as alternatives to reduced the short channel effect(SLE) of scaled devices due to their better electrostatic control of



channel charges. In this paper propose a low power and area efficient full adder. FINFET full adder design confirms that there is reduction of 25 to 30 percent in the value of power dissipation when compared to CMOS full adder technique.

Figure.3 4-bit full adder

In the figure.3 four bit full adder is used for 4 bit addition purpose which includes 4 bit inputs (x0, y0), (x1, y1), (x2, y2), (x3, y3) and four sum outputs s1,s2,s3,s4. A carry input z0 is given to the first full adder FA1; the inputs such as z1, z2, z3 are given to the forthcoming full adder FA2, FA3, FA4 respectively. The full adder block FA1 is schematically represented by using FINFET logic. [8]

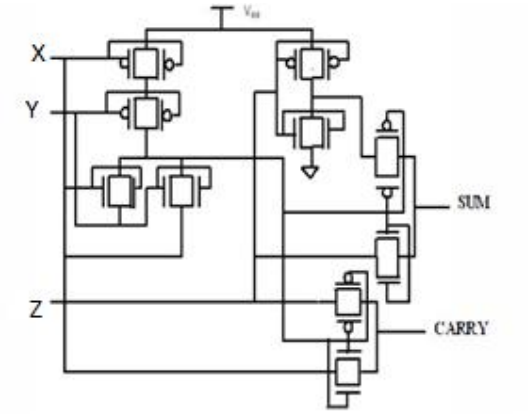



Figure.4 1-bit FINFET full adder

In static CMOS Full adder with pull up and pull down networks used 28 transistors but FINFET full adder required only 10 transistors. In this proposed paper FINFET full adder is designed in that accumulator to reduced power consumption, area and delay.

**2.4 D flip- flop**

D flip-flop is considered to be the most essential memory cell in the vast majority of digital circuit, which brings it extensive utilization especially under low power consumption. In recent research focus, numerous different types of D flip-flop have been invented and investigated and the continuous research trend has turned to high speed low power consumption performance. To implement high performance VLSI, obviously D flip-flop is chosen for extremely significant part in design flow. There two aspects for choosing D flip-flop, one is direct effect on clock frequency of digital circuit system and another which tends to consume 30% to 50% of power dissipation. Table 2 shows that D flip-flop stores a bit of data. i.e. input data applied at input D, its change the

output state according to the inputs and remain in the same state until the inputs changes. It is also used to introduce the delay in the circuit, and it is used as a buffer to store the intermediate data.

Table 2.Truth table of D-Flip-flop

| **Q** | **D** | **output** |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

### 2.5 D flip-flop using FINFET

FINFET has two electrical gates for the more flexibility design to reduce the low power consumption. Here D flip-flop is specifying used in the accumulator for reducing the numbers of transistor. It is delay flip flop used to reduced delay, power and area. In figure.5 shows that FINFET D flip-flop used a clock, reset, and a FINFET transistor is designed in the accumulator to show the reduced in the design when compared to the CMOS transistor. Here accumulator is effective by using the D flip-flop instead of another flip-flop. Hence the performance can be improved. [6]

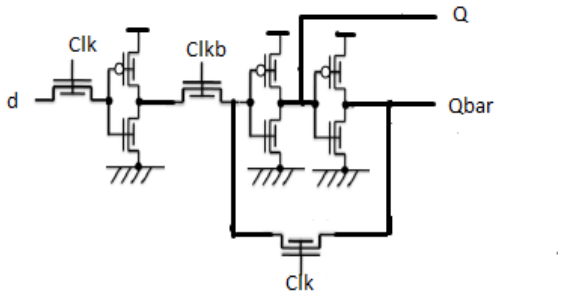



Figure.5 FINFET D FLIPFLOP

### 2.6 Accumulator

Accumulator is a 8-bit register used as a temporary storage device and to perform a arithmetic operation such as Addition, Subtraction, multiplication, division logic operation like

AND,OR,XOR etc., It is a part of ALU that stores a result in memory. The most elementary use for an accumulator is adding a sequence of numbers.

The term accumulator is used in a widely variety of non-computing application and activities, such as electrical engineering (an energy storage device such as rechargeable battery or ultra-capacitor) hydraulics (mechanical energy storage devices), in stack trading (a contract or agreement) and even in gambling (parlay bet). Accumulator dramatically improved the performances in the system like this providing a scratchpad area where the result of one operation can be fed in the next one for little or no performance partly. Accumulator size which is depends on the processor type; it can store the final value of the process already perform the task. FINFET accumulator used 5% of transistor when compared with CMOS technology and also the delay and area are minimized.

## III. Analytical result

CMOS accumulator has 6% of power consumption, 5% of area and numbers of transistor used is 13% shown in figure-6 and table-3 these output waveform is shown in XILINX.

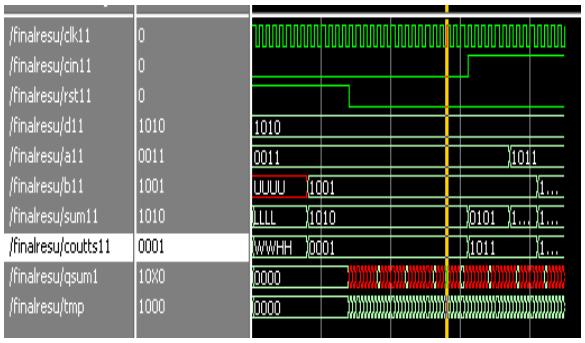



Figure.6 CMOS accumulator output waveform

Model Sim realization of accumulator using CMOS logic

Table 3. CMOS accumulator performance

| **Macro cells Used** | **P terms used** | **Registers Used** | **Pins Used** | **Function block inputs used** |
|---|---|---|---|---|
| 4/72 | 8/360 | 3/72 | 9/72 | 9/216 |

| | | | | |
|---|---|---|---|---|
| (6%) | (3%) | (5%) | 13% | (5%) |

In FINFET accumulator designed by 12%of power consumption, 1% of area and 5% of transistor is used and the output is shown in figure6 and the table4 model sim.

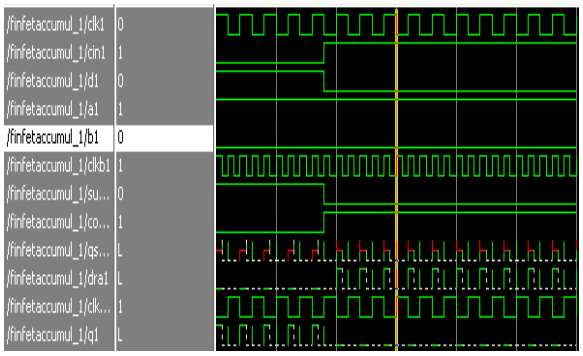



Figure.7 FINFET accumulator output waveform

The above figure represents the output of full adder designed using FINFET accumulator. The major disadvantage in towards circuit is delay. The main motive of every designer is to reduce the delay and power. This is achieved in our design of accumulator using FINFET. In existing model the design of accumulator using CMOS logic yields more delay and increases power consumption due to the usage of increased number of transistors. When the transistor count reduces the power consumption also gradually increases because the leakage power of any circuit designed using CMOS logic uses increased transistor count. This major drawback observed in the CMOS logic design is overcome by our proposed model. The proposed model includes accumulator design using FINFET, the major advantage of using FINFET is reduced transistor and registers, reduced power consumption and delay. Thus our proposed model acts as a good solution to solve all these problems. Hence this proposed model can be easily applied in real time such as smart phones.

Table 4. FINFET accumulator performance

| **Macro cells** | **P terms used** | **Registers Used** | **Pins Used** | **Function block inputs** |
|---|---|---|---|---|

| **Used** | | | | **used** |
|---|---|---|---|---|
| 1/72 (2%) | 1/360 (1%) | 0/72 (0%) | 3/72 5% | 1/216 (1%) |

## IV. Comparison of CMOS and FINFET accumulator

When CMOS is compared with FINFET technology it proved that the area, power consumption and delay have been reduced. In FINFET consumed 4% of power, 7% of the transistor and 4% of area less than the CMOS accumulator. Hence FINFET is most advanced technique and it is used in the current technology.

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