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Matthew Jon Curry

Candidate

Physics and Astronomy

Department

This dissertation is approved, and it is acceptable in quality and form for publication:

Approved by the Dissertation Committee:

Ivan H. Deutsch

Chairperson

Stephen M. Carr

Malcolm S. Carroll

Jason R. Petta

Improving the Readout of Semiconducting Qubits

by

Matthew Jon Curry

B.S., Physics, California Polytechnic State University, 2011
M.S., Physics, University of New Mexico, 2013

DISSERTATION

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
Physics

The University of New Mexico

Albuquerque, New Mexico

May, 2019

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Dedication

To my family and friends.

Acknowledgments

This dissertation is a map I wish I had at the beginning of graduate school. Everything here would not have been possible without guidance from my advisers as well as support from my friends and family. I would now like to take the time to thank everyone.

I owe a great deal to my two research advisers at Sandia National Laboratories: Steve Carr, and Malcolm Carroll. I first began research with Steve at Sandia in the summer of 2012. Steve showed me the basics of experimental research in a nicely detailed manner. I learned how to use a lock-in amplifier and electrically characterize devices at cryogenic temperatures. Steve's careful nature with handling devices and instruments is a skill that I practice to this day. I am grateful for Steve's patience with me as I grew to be the experimentalist I am now. Further along in graduate school, I adiabatically began working with Malcolm as my primary research adviser. Malcolm had a fundamentally different way of advising which I grew to appreciate. As we moved from device to device and anticrossing to anticrossing, I learned a great deal about quantum dots and singlet-triplet qubits. I watched new types of readout and qubits develop during our long group meetings. The scientific method style of presentation is something I always try to do moving forward. Planning measurements out well in advance is a skill that I appreciated learning and continue working on. Again, I couldn't be more thankful for both my advisers' patience and guidance.

At Sandia, there are many other people I would like to thank. Mike Lilly helped me get started in a lab at CINT and attended the early HBT meetings. I am very grateful for all the assistance with dilution refrigerators Mike as provided over the years. Troy England arrived later in the HBT project and his expertise in HBTs was invaluable for the entirety of the project. I could not be more fortunate that such an expert joined Sandia during my graduate studies. Martin Rudolph was also incredibly helpful with the HBT project and publications. I will miss working with him moving forward. Ryan Jock is a great colleague I always look forward to chatting with. It will be nice working together in the future. My previous manager, Clark Highstrete, was an interesting person to talk to. He flew the F-16 in the US Air Force and graduated from the same physics Ph.D. program at UNM, which was rather encouraging. Similarly, my current manager, Steve Rinaldi, was in the US Air Force and has a Ph.D. I've been hired as a member of the staff at Sandia through Steve, so I am very thankful, to say the least. I would not have been able to make it through the long days of research without my fellow graduate students at Sandia: Patrick Harvey-Collard, Chloe Bureau-Oxton, and Amir Shirkhorshidian. Patrick provided incredible amounts of advice and knowledge, and Chloe left hidden bags of M&Ms that I'm still finding to this day. I look forward to working with Dwight Luhman as the new principal investigator for many years to come. In no particular order, I would also like to thank: Tzu-Ming Lu, Meenakshi Singh, Ezra Bussmann, Wayne Witzel, Toby Jacobson, Dan Ward, Shashank Misra, Andrew Baczewski, Andrew Landahl, Kenny Rudinger, Andy Mounce, Lisa Tracy, Rick Muller, Tom Harris, Ed Bielejec,

Vanita Srinivasa, Erik Nielsen, Peter Sharma, Mike Wanke, Jonathan Rivera, Rohith Vudatha, Nick Brechtel, Albert Grine, Victor Chavez, and Chuck Fuller.

At UNM, I had many great professors and fellow graduate students who I would like to thank. Ivan Deutsch was my research advisor throughout my time at UNM. Ivan was extremely helpful with any questions I had about graduate school and the classes I took with him. Long ago, Ivan encouraged me to accept the offer from the UNM physics Ph.D. program, which has opened many doors for me now. When I was deciding what research to begin with, Ivan recommended chatting to Steve Carr which eventually lead to my career at Sandia. I've greatly enjoyed Ivan being on my dissertation committee and all the advice he has given helping me graduate. Carl Caves is a great character that UNM will surely miss as he retires. Carl was also a large part of why I eventually attended the UNM physics Ph.D. program. I enjoyed Carl's quantum mechanics and quantum information classes as well as his dry sense of humor. Dave Dunlap, Kevin Cahill, and Vasudev Kenkre were also professors I enjoyed taking courses from. I have many friends to thank and not nearly enough time! Andy Ferdinand came from Cal Poly with me and was my first roommate in graduate school. I went on many outdoor adventures that I otherwise may not have gone on with Andy, and it made the early years much nicer. Andy is a great friend and someone I enjoy sharing liter glasses of beer with! Adrian Chapman was an amazing running and gaming buddy for almost all of graduate school. I could not have wished for a better friend. I miss all the good times and hopefully we'll end up working closer together someday! I would like to thank Evelyn Dohme for doing an excellent grammar run-through of this dissertation! Rest in peace, Kornelius Jakobsen, you are not forgotten. In no particular order, I would also like to thank: Josh Combes, Chris Ferrie, Jason Petta, James Hendrie, Jonathan Bainbridge, Karishma Bansal, Mitchell Brickson, Austin Daniel, Kathy DeBlasio, Chris DiLullo, Akram Amin, Matt DiMario, Rachel James, Aidan Grummer, Luke Horstman, Rachel, Horstman, Ning Hsu, Forrest Hubert, Matt Koppa, Megan, Lewis, Neil McFadden, Chelsea McFadden, Kevin Meaney, Anupam Mitra, Ben Morrison, Gopi Muraleedharan, Manuel Arias, Jaksa Osinski, Nate Ristoff, Rockie Curdes, Maziar Ziabari, Keith Sanders, Ezad Shojaee, Sam Slezak, Changhao Yi, Zhixian Yu, Ninnat Dangniam, Jonathan Gross, Anastasia Ierides, Linh Le, Xiaodong Qi, Ciaran Ryan-Anderson, Jacob Miller, Peter Relich, Mark Gorski, Tzu Cheng Wu, Charlie Baldwin, Matt Chase, Bob Keating, Brad Knockel, Ken Obenberger, Satomi Sugaya, Matthias Lang, Akash Rakholia, Ben Baragiola, Chris Cesare, Zhang Jiang, Leigh Norris, Rob Cook, Ben Johnson, Bibek Pokharel, Caleb Grimes, Eric Bahr, Kari Jacobs, Phil Casady, Dillon Thomas, Gena Robertson, Iman Chudnoff, Justin Peinado, Rachel Hellmer, Michael Treiman, Peter Sinclair, Vikas Buchemmavari, Dante Archuleta, and Joe Landers. I probably forgot a few people, so I apologize ahead of time.

At Cal Poly, there were several professors responsible for encouraging me to attend graduate school. Brian Granger gave me my first research opportunity ever with Google Summer of Code 2010. This experience and the research afterward

were seminal in my understanding of object-oriented programming and quantum mechanics. I've since used Python and Lyx throughout graduate school, and I've benefited tremendously as a result. I've even written this dissertation using Lyx! I'm very thankful to have worked with Brian so early in my studies and experienced the basics of quantum computing. Kat Gillen provided the first experimental research experience for me in her laser lab. Although I did not end up working with lasers, I still gained an appreciation for the research. Ron Zammit was an excellent electronics teacher and an entertaining friend outside of class. Through Ron's classes, I became motivated to learn about old electronics such as vacuum tubes and analog computers. He even let us keep some old tubes, which I still have today! Dane Iracleous is my comedic partner. Our thoughts resonate on a level I've never since experienced. I don't know how many times I've thought back on some of the silly things we thought up during college and immediately started uncontrollably cracking up. If nothing else works out for me, let's be a comedy duo! Galen Cauble was a great friend throughout my undergraduate experience. I miss all the wonderful adventures we had around San Luis Obispo. I enjoyed working with Addison Cugini on the Python projects, and I'm thankful for his patience with me as I learned how to program. Langston Johnson was an excellent roommate to have during my last year at Cal Poly. Langston is one of the kindest people I know. In no particular order, I would also like to thank: Austin Mello, Tom Gutierrez, Jeremy Kruger, Ben Knudson, Michelle Carey, Matt Sawyer, Leila Jewell, Dani May, Casey Allard, Nate Padilla, Rebecca Rosen, Keith Gresiak, Rebecca Peters, Anna Kopcrak, Bethany Biscaglio, Jonathan Ward, Mitch Sanders, Grant Olson, and Mark Fagundes.

Back home in Santa Cruz, California, there are several friends and teachers I must acknowledge. Dean Mimmack properly introduced me to physics via the "shut up and calculate" school of thought. I had the honor of attending a class from a high school teacher who had taught physics for around 40 years! We programmed BASIC on Apple II computers and made our own double-slit experiments by depositing soot on a glass slide and using a razor blade to scrape two lines close together. By the end of the two years with Dean, we made it to Feynman diagrams! I've never heard of any other high school students in all my career making it as far as we did. There is a nontrivial amount of physics background I received through Dean, and I'm extremely grateful for it. Robyn Miranda was an excellent English teacher, and I learned how to write well from her. Kevin Chapman has been a great friend for many years. We were always on a similar level when it came to running cross country and gaming. We have had so many great discussions over the years, and it's always effortless to resume where we left off. Georgi Dinolov is another great friend who I enjoyed my high school times with. I definitely do not have enough time to cover all the ridiculous adventures I've been on with Georgi, but I look forward to meeting up in the future. Casidhe Lee was my most hard-working friend in high school. I'm still impressed to this day with the progress he's made in his career. I'm sorry about all the horrible pranks we did to you, Casidhe. Try to forget them as you get older! Erin Warren is a fantastic friend and amusing character who always inadvertently encouraged me to be as honest as possible. Erik Lowe has always been a great friend to share an

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Lastly, I would like to thank Jaimie Stephens for all the support, discussions, and love during my time in graduate school.

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Abstract

Semiconducting qubits are a promising platform for quantum computers. In particular, silicon spin qubits have made a number of advancements recently including long coherence times [1, 2], high-fidelity single-qubit gates [2, 3], two-qubit gates [4], and high-fidelity readout [5]. However, all operations likely require improvement in fidelity and speed, if possible, to realize a quantum computer.

Readout fidelity and speed, in general, are limited by circuit challenges centered on extracting low signal from a device in a dilution refrigerator connected to room temperature amplifiers by long coaxial cables with relatively high capacitance. Readout fidelity specifically is limited by the time it takes to reliably distinguish qubit states relative to the characteristic decay time of the excited state, T_1. This dissertation explores the use of heterojunction bipolar transistor (HBT) circuits to amplify the readout signal of silicon spin qubits at cryogenic temperatures. The cryogenic

amplification approach has numerous advantages including low implementation overhead, low power relative to the available cooling power, and high signal gain at the mixing chamber stage leading to around a factor of ten speedup in readout time for a similar signal-to-noise ratio. The faster readout time generally increases fidelity, since it is much faster than the T_1 time.

Two HBT amplification circuits have been designed and characterized. One design is a low-power, base-current biased configuration with non-linear gain (CB-HBT), and the second is a linear-gain, AC-coupled configuration (AC-HBT). They can operate at powers of 1 and 10 μW, respectfully, and not significantly heat electrons. The noise spectral density referred to the input for both circuits is around 15 to 30 fA/$\sqrt{\text{Hz}}$, which is low compared to previous cases such as the dual-stage, AC-coupled HEMT circuit at $\sim$ 70 fA/$\sqrt{\text{Hz}}$ [6]. Both circuits achieve charge sensitivity between 300 and 400 μe/$\sqrt{\text{Hz}}$, which approaches the best alternatives (e.g., RF-SET at $\sim$ 140 μe/$\sqrt{\text{Hz}}$) but with much less implementation overhead. For the single-shot latched charge readout performed, both circuits achieve high-fidelity readout in times < 10 μs with bit error rates $< 10^{-3}$, which is a great improvement over previous work at > 70 μs [5]. The readout speed-up in principle also reduces the production of errors due to excited state relaxation by a factor of ~ 10. All of these results are possible with relatively simple, low-power transistor circuits which can be mounted close to the qubit device at the mixing chamber stage of the dilution refrigerator.

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Glossary

^{28}Si	Silicon Isotope (Mass Number = 28)
^{29}Si	Silicon Isotope (Mass Number = 29)
2DEG	Two-Dimensional Electron Gas
^{31}P	Phosphorus Isotope (Mass Number = 31)
AC	Alternating Current
AC-HBT	AC-Coupled Heterojunction Bipolar Transistor Circuit
Al	Aluminum
AlGaAs	Aluminum Gallium Arsenide
As	Arsenic
BASIC	Beginner's All-Purpose Symbolic Instruction Code
BER	Bit Error Rate
Bit	Binary Digit
BJT	Bipolar Junction Transistor
BW	Bandwidth

CB-HBT	Current-Biased Heterojunction Bipolar Transistor Circuit
CdS	Cadmium Sulfide
CF_4	Tetrafluoromethane
CINT	Center For Integrated Nanotechnologies
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
DC	Direct Current
DCE	Dichloroethene
DR	Dilution Refrigerator
e	Electron Charge ($1.602 \cdot 10^{-19}$ C)
EBL	Electron-Beam Lithography
ENIAC	Electronic Numerical Integrator and Computer
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
h	Planck Constant ($4.14 \cdot 10^{-9}$ μeV·s)
HBr	Hydrogen Bromide
HBT	Heterojunction Bipolar Transistor
HBT-SET	Antiquated Name For CB-HBT

HEMT	High-Electron-Mobility Transistor
IBM	International Business Machines
IC	Integrated Circuit
JPA	Josephson Parametric Amplifier
k_B	Boltzmann Constant (86.17 μeV/K)
LC	Inductor Capacitor
LHe	Liquid Helium
MC	Mixing Chamber
m_e	Electron Rest Mass ($9.11 \cdot 10^{-31}$ kg)
MITS	Micro Instrumentation and Telemetry Systems
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
N_2	Nitrogen Gas
NV	Nitrogen-Vacancy
O_2	Oxygen Gas
OFIG	Only Found In Glossary
PCB	Printed Circuit Board
Poly-Si	Polycrystalline silicon
PTR	Pulse Tube Refrigerator

QD	Quantum Dot
QPC	Quantum Point Contact
Qubit	Quantum Bit
RF	Radio Frequency
RMS	Root Mean Square
RT	Room Temperature
RTS	Random Telegraph Signal
SEM	Scanning Electron Microscope
SET	Single-Electron Transistor
Si	Silicon
Si-MOS	Silicon Metal-Oxide-Semiconductor
Si_3N_4	Silicon Nitride
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
SNL	Sandia National Laboratories
SNR	Signal-To-Noise Ratio
SoC	System On Chip
STM	Scanning Tunneling Microscope
T_1	Excited State Relaxation Time

Glossary

T_2	Dephasing Time Measured Using Spin Echo
$T_2{}^*$	Dephasing Time Measured Using Ramsey Interferometry
TEM	Transmission Electron Microscopy
TEOS	Tetraethoxysilane
Ti	Titanium
TIA	Transimpedance Amplifier
TiN	Titanium Nitride
TLA	Three-Letter Acronym
Transmon	Transmission Line Shunted Plasma Oscillation Qubit
UNM	University of New Mexico
W	Tungsten

Chapter 1

Introduction

1.1 Motivation

Humans have been generating, processing, and storing information for thousands of years. The rate at which this occurs is increasing exponentially over time with different eras marked by major technological advances. Beginning with the Sumerian abacus around 2500 BC, humans began encoding and processing numbers as large as 10 billion on a device which used sliding beads. In the 1620s, the slide rule was invented, which allowed calculations to be performed much faster than on an abacus. Shortly after the invention of the slide rule, mechanical calculators were created by several individuals including the mathematician, Gottfried Leibniz. Mechanical calculators were eventually made portable and were not directly replaced until the 20th century. In 1804, Joseph-Marie Jacquard invented a loom which used punch cards to store the pattern intended to be woven. This invention laid the foundation for computers storing and processing information via punch cards, which were used well into the 20th century. An example of an IBM punch card used at the University of New Mexico in the 1970s can be seen in Figure 1.1. The first programmable com-

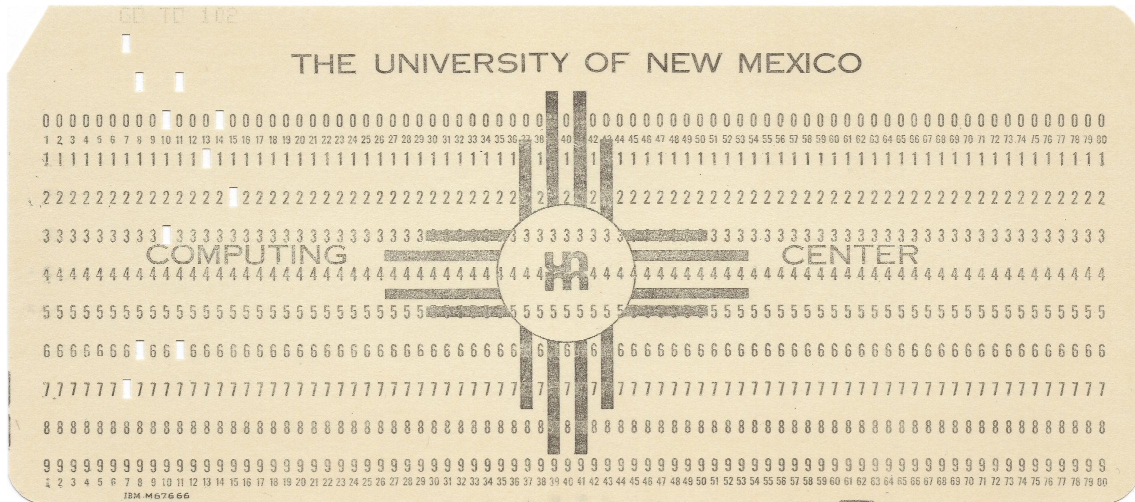

Figure 1.1: UNM Punch Card
Punch card from The University of New Mexico Computing Center circa 1970. This storage medium is capable of encoding up to 960 bits per punch card. The pictured punch card represents one line of code instructing the computer to "GO TO 102" and execute the code found at line 102, which is the 102nd punch card in the program. The code is printed at the top left region of the punch card, albeit slightly faded.

puter was proposed in 1837 by Charles Babbage. This computer was known as the "analytical engine" and was designed to be completely mechanical and hand cranked, however, it was never constructed. The first analog computers were developed and used in the late 19th century to solve specific problems by using a continuously changing physical property. For example, a type of mechanical analog computer known as a "differential analyzer" could use integration to solve differential equations via rotating disks.

The development of the first digital, electronic computers occurred around the time of World War II, with the general idea formulated by Alan Turing in 1937 [7]. These early digital computers were first created using electromechanical relays. Eventually, the electromechanical relay computers were replaced by vacuum tube computers, which were purely electronic in operation. An example of an early vacuum tube computer is the Electronic Numerical Integrator and Computer (ENIAC), which

was built in 1945 at the University of Pennsylvania and contained over 20,000 vacuum tubes and around 5,000,000 connections soldered by hand. The ENIAC used punch cards to store information and it was originally designed to compute artillery firing tables, but it actually first computed the feasibility of thermonuclear weapons.

The development of the transistor in 1947 resulted in a highly disruptive advancement for computers. Instead of macroscopic, power-inefficient, and relatively unreliable glass tubes, there were now solid, microscopic, power-efficient, reliable components. Previously taking up the area of a large room, computers could now fit in a much smaller area the size of an office. Eventually, the integrated circuit (IC) was developed in the late 1950s and many transistors could now be fabricated on the same piece of semiconducting material. Using the integrated circuit concept, Intel created the first microprocessor, the Intel 4004, in 1971. The microprocessor contained most of the hardware necessary to build a computer in a component smaller than a single vacuum tube. Computers became far more affordable for individuals to purchase leading to the first commercially successful personal computer, the MITS Altair 8800, being created in Albuquerque, New Mexico in 1975. The success of the Altair 8800 attracted Bill Gates and Paul Allen to found Microsoft in Albuquerque and develop a BASIC programming language interpreter for the Altair 8800. Over the next few decades, computers became smaller, more powerful, and more affordable. Recently developed system on chip (SoC) integrated circuits contain all components required for a computer and enable highly-portable, power-efficient computers such as smartphones. Through more precise fabrication, the number of transistors on an integrated circuit has been roughly doubling every two years [8], however, the transistors will eventually reach hard, physical limits when shrunk to near the atomic scale. Increasing the performance of computers by shrinking the transistors will eventually no longer be viable. Fortunately, another paradigm for computing exists.

The technological advancements covered so far have focused on a form of computation now known as "classical computing." For classical computers, the basic unit of information is a bit, which can encode one of two values (e.g., 1 or 0, true or false, on or off, punched or unpunched). This dissertation focuses on a new form of computation: quantum computation. Quantum computation differs from classical computation by taking advantage of the effects of quantum mechanics such as entanglement and superposition. Instead of bits, quantum computers use quantum bits or "qubits," which are quantum-mechanical two-level systems (e.g., an electron spin state in a magnetic field). Qubits can encode two values similarly to a bit, however, they can also be in a coherent superposition of both values (e.g., $\frac{1}{\sqrt{2}}[|0\rangle + |1\rangle]$). The idea for quantum computing began in the early 1980s from physicists such as Paul Benioff and Richard Feynman [9–11]. One of the early motivations for quantum computing was the apparent difficulty in simulating quantum systems efficiently with classical computers, therefore direct control of a quantum system would be advantageous for simulation. In 1994, Peter Shor proved that a quantum computer could factorize integers in polynomial time, where the number of steps required to factorize an integer, N, grows at a rate roughly proportional to $\log(N)$ [12]. This result was highly disruptive to the field of cryptography, where many techniques for protecting sensitive information rely on the notion that classical computers are only known to be able to factor integers in exponential time, where the number of steps for factorization grows at a rate roughly proportional to e^N. If N is large enough (e.g., $N = 2^{4096}$), then the number of steps required ($e^{2^{4096}}$) will be on an enormous scale where the factorization effectively becomes impossible. Another advantage of quantum computers is secure communication using quantum entanglement, which is of particular importance for preventing interception of sensitive information [13]. Efficient simulation of chemical reactions is an application of quantum computing which may lead to major chemical breakthroughs. For example, around 2% of the world's energy is used on the Haber-Bosch process, the current method for producing

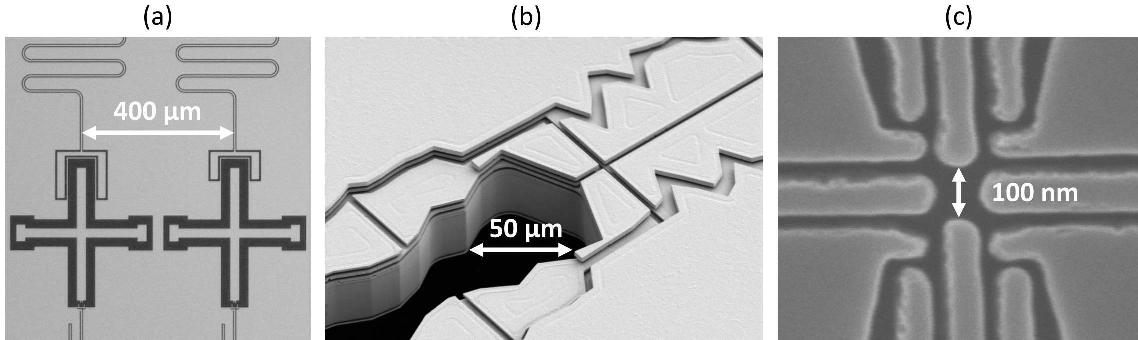

Figure 1.2: Prevailing Quantum Computing Architectures (2018)
Example images of the currently prevailing quantum computing architectures as of 2018. (a) Optical image of two superconducting transmon qubits (image credit [15]). The "+" pattern is the relatively large shunting capacitor used to suppress charge noise. (b) SEM image of part of the second-generation Sandia high optical access trap for trapped-ion qubits (image credit [16]). The ions are typically trapped several micrometers apart in these systems. (c) SEM image of Sandia Si-MOS quantum-dot and donor atom qubit device. This dissertation will focus on this type of device.

nitrogen fertilizer. This process requires relatively high temperatures and pressures ($\sim$ 20 MPa and $\sim$ 500 °C), whereas plants extract fertilizer out of atmospheric pressure air at room temperature. The mechanism plants use to do this is not currently understood, however, quantum simulation of the chemicals involved could reveal the underlying mechanism and enable enormous amounts of energy saving [14].

As of 2018, fruitful quantum computers remain a challenge to realize. Just as classical computers had many different early forms (e.g., vacuum tubes and electromechanical switches), quantum computers have several prevailing physical architectures. These qubit architectures include: semiconducting, superconducting, trapped ion, and nitrogen-vacancy (NV) centers. Semiconducting qubits generally use quantum dots or donor atoms to encode qubits on the spin states of the occupying electrons [4, 17–22]. Superconducting qubits are typically made out of aluminum with one or two Josephson junctions connected in parallel to a large shunting capacitor ("+" pattern in Figure 1.2(a)) [15, 23–25]. This type of qubit is known as

Architecture	T_1	T_2
Semiconducting	$>$ 10,000 s [1]	$>$ 10,000 s [1]
Trapped Ion	$>$ 4000 s [35]	$>$ 50 s [35]
NV Center	15 s [34]	$>$ 1 s [32]
Superconducting	0.0001 s [25]	0.0001 s [25]

Table 1.1: Qubit Coherence Times (2018)
Longest observed qubit coherence times for currently prevailing quantum computing architectures as of 2018. The effective T_1 time for trapped ion qubits is limited by the trap lifetime (the intrinsic T_1 time for the trapped ion hyperfine qubits is actually greater than 1,000,000 years). Most numbers shown are approximate values.

a "transmon," and it is analogous to a resonant LC circuit where the linear inductor is replaced with a Josephson junction to create an anharmonic oscillator. While semiconducting and superconducting qubits generally require cryogenic operation ($\lesssim$ 100 mK), the trapped-ion and NV center qubits can be operated at room temperature. Trapped ion qubits are created by using a combination of static and oscillating electric fields to form a rotating saddle potential that a single ion cannot escape from [26]. Figure 1.2(b) shows part of an ion trap made on a surface where the ions are shuttled around with electrodes and interact through collective quantized motion [16, 27–30]. NV center qubits are made out of point defects in a diamond lattice, where a neighboring nitrogen atom and a lattice vacancy form a multi-electron system that is controlled optically [31–34].

All quantum computer architectures must satisfy general criteria in order to be a viable candidate for quantum computing. The criteria were originally outlined by David DiVincenzo in 2000 [36] and consist of five main categories:

1. *Initialization*: Reliable initialization of the qubits to the ground state in a quantum computer is critical to achieve. Each of the current, prevailing quantum computer architectures has a different way to initialize the qubit into the ground state, $|0\rangle$. For example, trapped ion quantum computers use a laser

that is focused on the ion at an energy which couples the excited state, $|1\rangle$, to higher energy excited states which then decay to the ground state or back to the excited state. When the higher energy states decay, visible light is emitted. The laser only couples the excited state to higher energy excited states, so when the ion is in the ground state, it remains in the ground state and no more light is emitted [30]. For superconducting qubits such as the transmon, the excited state decay is relatively fast ($\sim 100\ \mu$s). The protocol is to simply wait for a period of time which is long relative to the decay time and verify that the qubit is in the ground state before performing computations. For semiconducting qubits, the rate at which electrons tunnel back and forth from an electron reservoir to a quantum dot is important for reliable initialization and is covered in Section 3.2.

2. *Control*: The ability to perform rotations of the qubit state about the Bloch sphere and conditional rotations which depend on the state of a second qubit is critical for achieving a universal digital quantum computer. The control of the type of semiconducting qubit covered in this dissertation is outlined in Section 2.3.

3. *Coherence*: The lifetime of the excited state, T_1, and the dephasing time, T_2, are two timescales that must be long relative to the amount of time the qubit state rotations require. Table 1.1 shows the difference in the longest absolute coherence times for each prevailing quantum computer architecture. Semiconducting qubits can in principle take advantage of the nuclear spins of ionized donor atoms in ^{28}Si to achieve long absolute coherence times.

4. *Readout*: Different quantum computing architectures use different methods to measure the state of the qubit. For example, in trapped ion quantum computers, the ion will have laser light directed at it such that the excited state will fluoresce and the ground state will not [30]. Superconducting transmon qubits

use a capacitively coupled microwave resonator which changes the phase of the readout signal depending on the state of the qubit [23]. For semiconducting qubits, the readout is usually performed using a charge sensor, and the readout is covered in Sections 2.3 and 3.6. Table 1.2 shows the lowest readout error rates achieved for each of the prevailing quantum computing architectures.

5. *Scalability*: Since fruitful quantum computers will require many qubits, system-wide operation must remain possible as the number of qubits is increased. In general, the control and readout apparatuses must be able to address multiple qubits, otherwise, the number of apparatuses will increase directly with the number of qubits. The qubits must also be able to remain coupled together quantum mechanically to some degree as qubit number increases. The physical size of the qubits is another factor that is a concern for scalability. For example, Figure 1.2 shows three different quantum computing architecture candidates with dramatically different length scales. The superconducting qubits are relatively large at the hundreds of micrometer scale. The trapped ion and NV center qubits are spaced several micrometers apart on average, and the control electrodes for trapped ions are at the tens of micrometer scale. Semiconducting qubits are relatively small and can be spaced tens of nanometers apart.

1.2 Improving Qubit Readout

This dissertation is about improving the readout fidelity of semiconducting qubits. The readout fidelity typically depends on the time it takes to measure the qubit's quantum state. Once the quantum state is projected on to the basis intended for measurement, the probability that the excited state will decay to the ground state is,

$$P_{\text{decay}} = e^{(-t_{\text{meas}}/T_1)}, \tag{1.1}$$

Architecture	Readout Error Rate	Measurement Time
Semiconducting	$1.4 \cdot 10^{-3}$ [5]	70 μs [5]
Trapped Ion	$1 \cdot 10^{-3}$ [38]	400 μs [38]
NV Center	$4.5 \cdot 10^{-2}$ [34]	200 ms [34]
Superconducting	$8 \cdot 10^{-3}$ [24]	90 ns [24]

Table 1.2: Qubit Readout Error Rates (2018)
Lowest readout error rates for currently prevailing quantum computing architectures as of 2018. Measurement times to achieve the error rates are listed in addition. Most numbers shown are approximate values.

where T_1 is the characteristic decay time of the excited state, and t_{meas} is the time starting at the beginning of the readout process. This probability is proportional to the fidelity of the readout, therefore, the readout error rate is given by,

$$\Gamma_{\text{error}} = 1 - e^{(-t_{\text{meas}}/T_1)} \approx \frac{t_{\text{meas}}}{T_1}, \tag{1.2}$$

where decreases in t_{meas} will directly decrease the readout error rate relative to T_1. Using a readout technique known as "latched readout" and the right balance of tunnel rates (Sections 2.3 and 3.6), the T_1 time during readout can effectively become ~ 10 ms [5]. An important threshold to reach for fault-tolerant quantum computation is error rates less than $1 \cdot 10^{-3}$ [37]. In order for the readout error rate to be reduced to $< 1 \cdot 10^{-3}$, the measurement time must take no longer than ~ 10 μs. In previous work, the readout time was limited to > 70 μs (see "Semiconducting" section of Table 1.2). Therefore, it is necessary to improve the readout time (i.e., same SNR for faster integration time) to reach fault tolerant operation.

Typical approaches for improving readout include using amplification to increase the signal-to-noise ratio (SNR) and therefore decrease the integration time it takes to achieve a certain SNR. Since semiconducting qubits are operated at cryogenic temperatures in dilution refrigerators, there are nontrivial constraints placed on the amplification possibilities. Common amplifiers such as a transimpedance amplifier (TIA) do not necessarily work at cryogenic temperatures and will dissipate more

energy than the dilution refrigerator can remove while maintaining low temperatures. Certain transistors have been shown to operate at the cryogenic temperatures required for qubit operation (Section 2.4 and Chapter 5). One such transistor is known as a "heterojunction bipolar transistor" (HBT) and can provide signal gain as high as $\sim$ 1,000 at powers as low as $\sim 1\ \mu$w, which allows the dilution refrigerator to maintain cryogenic temperatures.

Two HBT amplification circuits have been designed and used to decrease the measurement time for semiconducting qubit readout. These circuits and the results are covered in Chapter 6. The key result is that for both amplification circuits, the measurement time has been reduced to less than 10 μs.

1.3 Outline

This dissertation is organized into five main chapters. In Chapter 2, background material is covered for the specific semiconducting qubits used in this work. The chapter begins with a discussion on semiconducting devices in general, starting with the MOSFET device. Then quantum dots are defined and their formation is covered. Measurements specific to quantum dots are shown with example data. Next, the specific semiconducting qubit used in this work, the "singlet-triplet qubit," is described along with its operation and measurement. Finally, a review of the current semiconducting readout techniques is done with the focus on cryogenic amplification and its benefits. Chapter 3 covers the experimental methods used to tune and operate the singlet-triplet qubits. This includes tuning the tunnel rate for reliable qubit initialization, minimizing electron temperature, verifying the energy scales via magnetospectroscopy, tuning the tunnel coupling, and performing readout to characterize cryogenic amplification benefits. Chapter 4 focuses on the Si-MOS devices fabricated at Sandia National Laboratories for improving the single-electron regime

achievability and tunability. Simulations of the devices were a contribution of this dissertation work to the resulting paper described in Chapter 4. The simulations helped verify the tuning orthogonality between the quantum dot occupancy and the tunnel rate. Chapter 5 shows the initial results from characterizing the CB-HBT connected to a charge sensor at 4 K. The amplifier was characterized by increasing the frequency of the input signals as well as monitoring random telegraph signal as the bandwidth of the room temperature amplifier was increased. Finally, in Chapter 6, the two HBT amplification circuits are characterized by performing single-shot latched charge readout. The chapter starts by describing the differences between the two circuits, with the AC-HBT being designed and measured by coworkers at SNL. Then, a comparison of noise, bandwidth, power, and electron temperature is done to highlight the performance differences between the two circuits. Finally, a double quantum dot is tuned to few electrons and single-shot latched charge readout results from the CB-HBT are compared to the AC-HBT case. Both circuits are able to perform high-fidelity readout with measurement times less than 10 μs, however, the CB-HBT operates at lower power.

Chapter 2

Background

2.1 Semiconducting Devices

Semiconducting devices are ubiquitous in the developed world. Whether used as a simple switch, amplifier, or even in a microprocessor, semiconducting transistors form much of the foundation of the information age. A transistor can be described simply as a device which has one input terminal to control the conductance between two other input/output terminals completely electronically. Originally, vacuum tube technology was used to amplify "feeble" electric signals beginning with Lee De Forest's 1907 triode tube invention, but there were several limitations including size, cost, and lifetime. Vacuum tube amplifiers were eventually replaced by semiconducting transistors in the middle of the 20$^{\text{th}}$century. The semiconducting transistor was first patented by Julius Lilienfeld in 1925 and then later fully theorized and developed by William Shockley, Walter Brattain, and John Bardeen at Bell Labs in 1947 [39]. Since its creation, the semiconductor industry has expanded exponentially, with sales totaling $412,000,000,000 in 2017 [40].

The first transistor invented at Bell Labs was essentially a bipolar-junction tran-

sistor (BJT) (see Appendix A). Since the first transistor, many other transistor architectures have been created including: heterojunction-bipolar transistors (HBTs), insulated-gate-bipolar transistors (IGBTs), avalanche transistors, Schottky transistors, field-effect transistors (FETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), junction gate field-effect transistors (JFETs), metal-semiconductor field-effect transistors (MESFETs), fin field-effect transistors (FinFETs), organic field-effect transistors (OFETs), floating-gate transistors, deoxyribonucleic acid field-effect transistors (DNAFETs), carbon nanotube field-effect transistors (CNFETs), high-electron-mobility transistors (HEMTs), and numerous others. In this section, the focus is on how metal-oxide-semiconductor field-effect transistors (MOSFETs) operate and are fabricated.

MOSFET devices are typically made up of three material layers and have three input/output terminals. Figure 2.1(a) shows a schematic cross-section of a conventional MOSFET, where the gate is an electrically conductive input which generates an electric field below it in the p-type silicon substrate. By adjusting the voltage on the gate, the electric field will change the energy of the conduction band and valence band edges in the silicon substrate. In an enhancement mode device, a positive voltage on the gate will decrease the energy of the conduction band edge until it is at or below the Fermi level (average energy to add an electron to the silicon substrate). In Figure 2.1(b), when the Fermi level of the electrons is above the conduction band edge in the region below the gate, the silicon substrate becomes conducting. Therefore, current will flow if a voltage bias is placed across the source and drain ohmic contacts. When the gate voltage is sufficiently high and the MOSFET is in saturation mode, the amount of current for a given gate voltage is,

$$I_{\mathrm{SD}}(V_G) \approx \frac{\mu_n C_{\mathrm{oxide}}}{2} \frac{W_{\mathrm{G}}}{L_{\mathrm{G}}} \left(V_{\mathrm{G}} - V_{\mathrm{th}}\right)^2 , \tag{2.1}$$

where $\mathrm{I_{SD}}$ is the source-drain current, μ_n is the charge-carrier mobility, $\mathrm{C_{oxide}}$ is the gate oxide capacitance per area, $\mathrm{W_G}$ is the width of the gate, $\mathrm{L_G}$ is the length of the

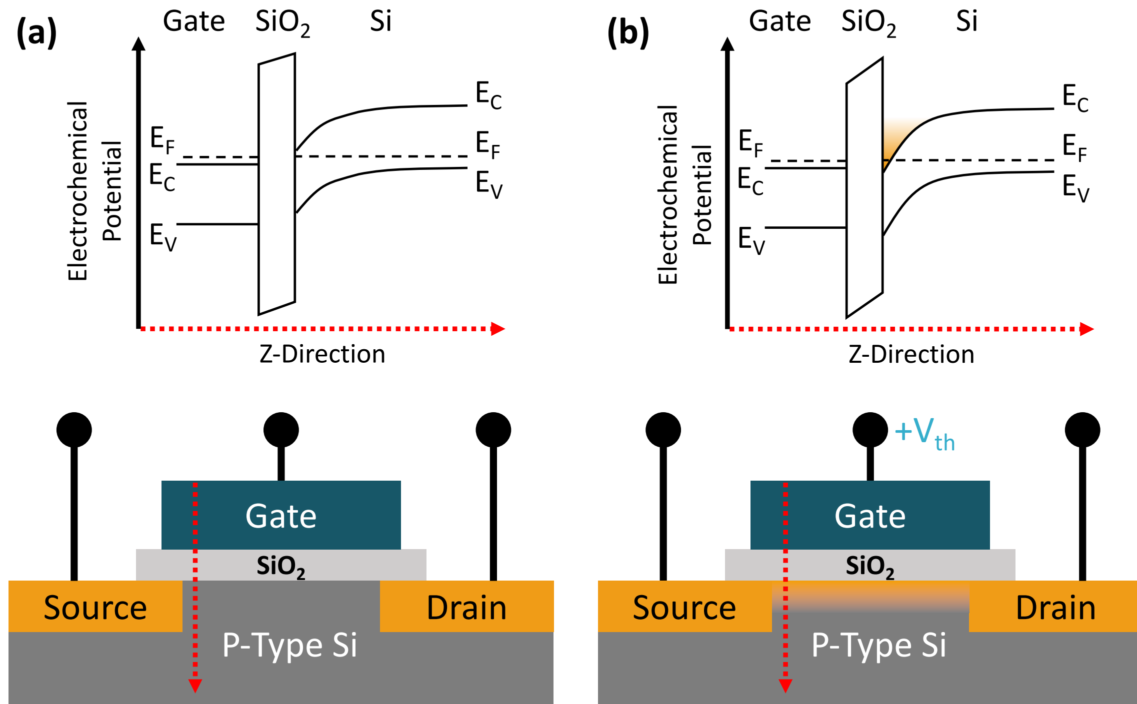

Figure 2.1: MOSFET Schematic and Band Diagrams
(a) Metal-oxide-semiconductor field-effect-transistor (MOSFET) basic schematic and band diagram pertaining to zero voltage bias on the gate. The band diagram direction corresponds to the red dashed line going from the top of the gate into the p-type silicon substrate. Electrons with energy in the conduction band are represented by orange coloration. Connections to the MOSFET are shown as black lines with black circles on the ends (connection leads). (b) MOSFET basic schematic and band diagram pertaining to large enough voltage bias on the gate to enhance a conducting channel between the source and drain.

gate, V_G is the gate voltage, and V_{th} is the threshold voltage.

MOSFETs are fabricated using several different methods. One method is to start with bulk silicon and grow a silicon dioxide (SiO_2) layer on top (around 5–100 nm thick) by subjecting the silicon to high temperatures. Next, heavily-doped, n-type polycrystalline silicon (polysilicon) is deposited on top of the silicon dioxide and etched into the shape of the gate. Regions of the oxide on either side of the gate are etched away and the silicon substrate underneath is doped with donors to create n-type regions (the source and drain regions). Finally, metal is deposited on to the surface and etched away such that only the source and drain regions have metal channels leading to them to form ohmic contacts.

The MOSFET architecture is what forms the basis for the silicon spin qubit platform covered in this dissertation. While this section has focused on the "classical" transistor mode of MOSFETs, most of the dissertation focuses on the MOSFET architecture being used in a far different capacity. Instead of using a relatively large gate to form a well-understood conductive channel, the gate is effectively shrunk down to a size where quantum mechanical tunneling governs the transport of electrons. The gate is also used to form and control quantum dots and qubits, which is covered in Section 2.2. The device used to generate most of the results in this dissertation has many separate polysilicon gates patterned out laterally on top of the oxide layer and is imaged in Figure 2.2. Figure 2.3 shows a three-dimensional model of the region of interest of the silicon MOS (Si-MOS) device used. The images are of the device being gradually rotated from a top view (Figure 2.3(a)) to a side view (Figure 2.3(f)). The narrower gates are generally used to form and control where the quantum dot will be located. The larger gates are used to form electron reservoirs (essentially sources and drains) that provide electrons for the quantum dot.

Si-MOS lateral quantum dot devices are fabricated at Sandia National Laborato-

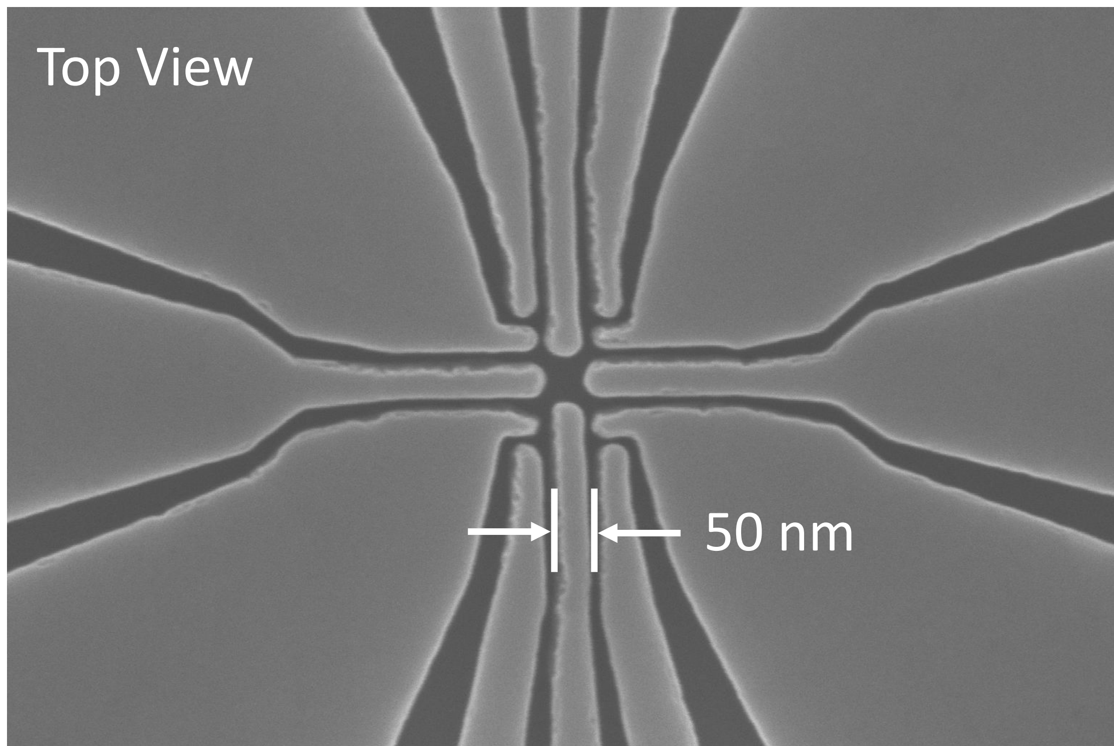

Figure 2.2: Si-MOS Nanostructure SEM Image
Scanning electron microscope (SEM) image of the Si-MOS nanostructure (top view). Lighter grey regions are the polysilicon gates which lie on top of the silicon dioxide and silicon substrate below. Feature sizes are as small as 50 nm by using electron beam lithography to pattern the polysilicon gates.

ries using a silicon foundry. A p-type silicon substrate with a ^{28}Si enriched epitaxy layer (500 ppm ^{29}Si) is used because it has far fewer ^{29}Si nuclear spin moments coupling to spin qubits, which results in longer spin coherence times [41]. A 35 nm thermal silicon oxide (SiO_2) is then grown on the substrate at 900 °C. Next, an amorphous silicon layer is formed on top of the oxide and n-type doped with arsenic. The amorphous layer is then crystallized into degenerately doped polysilicon (poly-Si). The poly-Si is patterned using electron beam lithography (EBL) and ZEP resist with feature sizes down to 50 nm. After the resist is stripped away, the remaining poly-Si forms the nanostructure shown in Figure 2.2 (light gray regions).

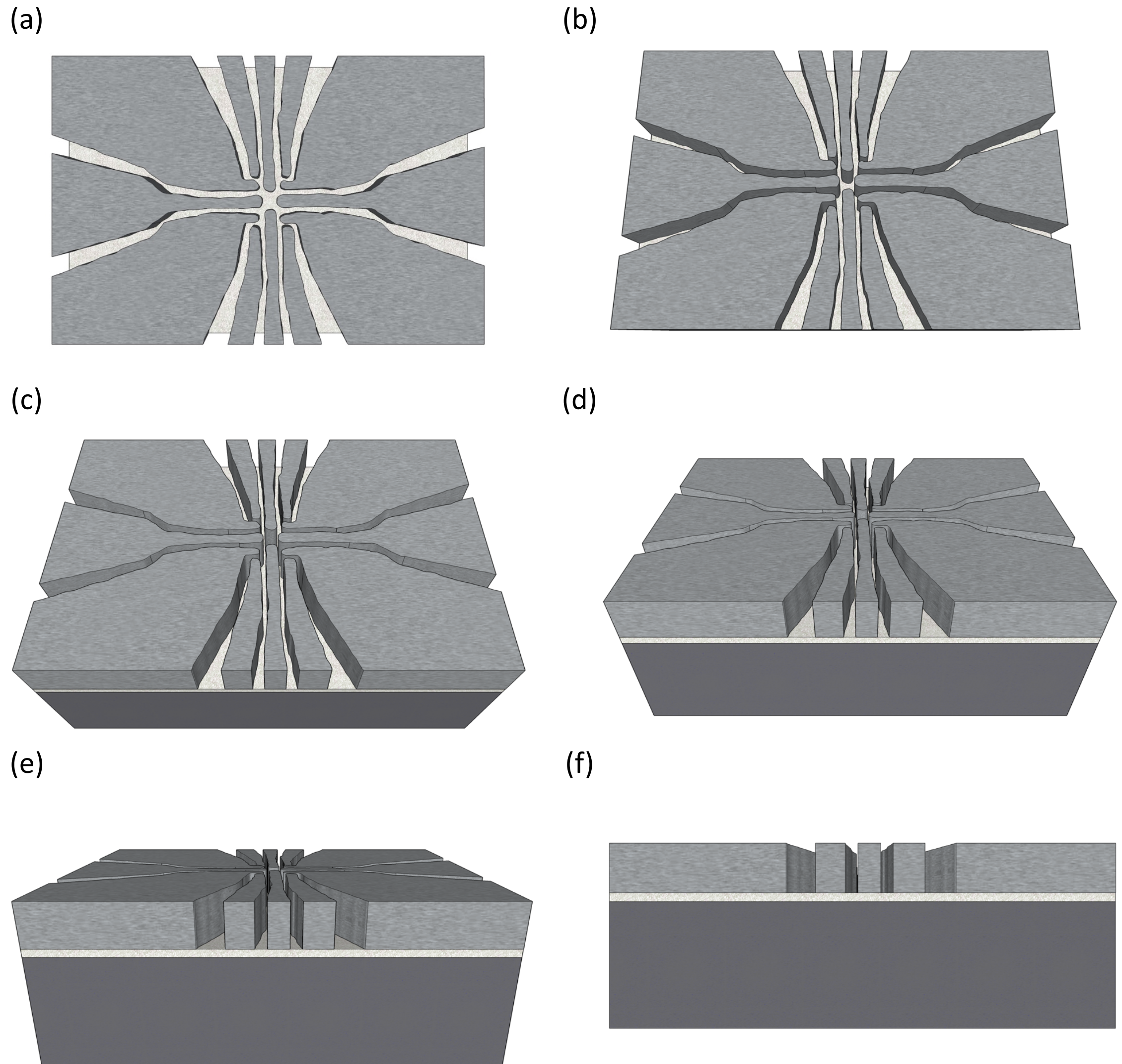

Figure 2.3: Si-MOS 3D Model Complete Device
Three-dimensional model images of Si-MOS qubit device. All electrostatic gates are drawn to scale. (a) Top view. (b)–(e) Several orientations are shown between top and side view of the device. (f) Side view. The polysilicon and oxide layer thicknesses are drawn to scale, however, only a fraction of the ^{28}Si epitaxial layer is shown (dark gray bottom layer). The oxide layer is 35 nm thick (light-colored middle layer) and the polysilicon layer is 200 nm thick (top layer). For full fabrication details, see Section 4.5.

2.2 Quantum Dots and Donor Atoms

A quantum dot is a nanoscale potential which tightly confines charge into discrete bound states much like the classic "particle in a box" problem found in elementary quantum mechanics classes [42]. A notable early demonstration of a quantum dot was performed by Louis Brus in 1983 via colloidal suspension of semiconducting cadmium sulfide (CdS) crystallites [43, 44]. Using transmission electron microscopy, the CdS crystallites were measured to be 30–50 Å in diameter, and through resonance Raman spectroscopy, they were found to have atom-like electronic bound states. A later experiment using molecular beam epitaxy (MBE) growth found similar behavior with gallium-arsenide (GaAs) aluminum-gallium-arsenide (AlGaAs) quantum well crystalline structures grown on a GaAs substrate [45]. Marc Kastner measured the first gate-voltage-dependent conductance oscillations through a small MOSFET transistor, which was dubbed the "single-electron transistor" (SET), a relatively large quantum dot that will be covered later in this section [46, 47]. Unlike the MBE grown quantum dots, the SET is partially electrostatically formed, meaning that part of the confining potential is defined by electric fields originating from a conducting gate. Similar designs using lateral gate geometry were later shown to form quantum dots with as few as one or two electrons [48, 49]. This dissertation will focus on the electrically measured, electrostatically defined quantum dots in Si-MOS [50–52].

Quantum dots in Si-MOS are created by confining electrons electrostatically in a manner similar to how the conducting channel is formed in a MOSFET. Figure 2.4 shows a model of the Si-MOS device used in this dissertation which has been cut across the gate where the quantum dot is intended to be formed underneath. After rotating the device from a top view (Figure 2.4(a)) to a side view (Figure 2.4(f)), the region where the quantum dot is formed is visible underneath the narrower polysilicon gate in the center. Figure 2.5 shows a schematic representation of the Si-MOS quantum dot and donor atom system. Since this is an enhancement

mode device, a positive voltage is placed across gates where electrons are intended to be accumulated against the Si-SiO_2 interface. Underneath the larger "Source/Drain Gates," two-dimensional electron gases (2DEGs) are formed which act as electron reservoirs. The electrons in the reservoirs are schematically shown relatively large and countable, but the actual number of electrons in the reservoirs is much larger with surface density around 10^{12} electrons/cm^2. Below the "Dot Gate," as few as one electron is confined vertically against the Si-SiO_2 interface and laterally by electrostatically defined tunnel barriers. Phosphorous donor atoms with mass number 31 are implanted next to the quantum dot via stochastic ion implantation. The ^{31}P donors are directed into the substrate with 45 keV of energy. A single ^{31}P donor is intended to be tunnel coupled to the quantum dot to form a singlet-triplet qubit, which is covered in Section 2.3.

Figure 2.6 shows the electrochemical potential of the conduction band edge for both the quantum dot and donor atom along relevant directions. The quantum dot possesses an anisotropic potential due to two different confinement modes. In the vertical direction, the quantum dot is confined against the Si-SiO_2 interface in a triangle potential. The vertical wall of the triangle potential is due to the large band gap of the insulating SiO_2 (8.9 eV). The slanted wall of the triangle potential is due to the dependence of the conduction band edge on the electric field originating from the conducting gate above. This electric field linearly changes the edge of the conduction band relative to the Fermi level as a function of distance. Confinement in the vertical direction is exactly the same as how a conducting channel is formed in a MOSFET (Section 2.1). Confinement in the lateral direction is the main difference in this type of device. In the lateral direction, tunnel barriers are formed when there is an insufficient electric field to bend the conduction band edge below the Fermi level. This is accomplished by having gaps on the sides of the "Dot Gate" which are visible in Figure 2.5 as well as using other nearby poly-Si gates with negative voltage bias placed on them (Figure 2.2 narrow poly-Si gates on either side of "Dot Gate"). In the

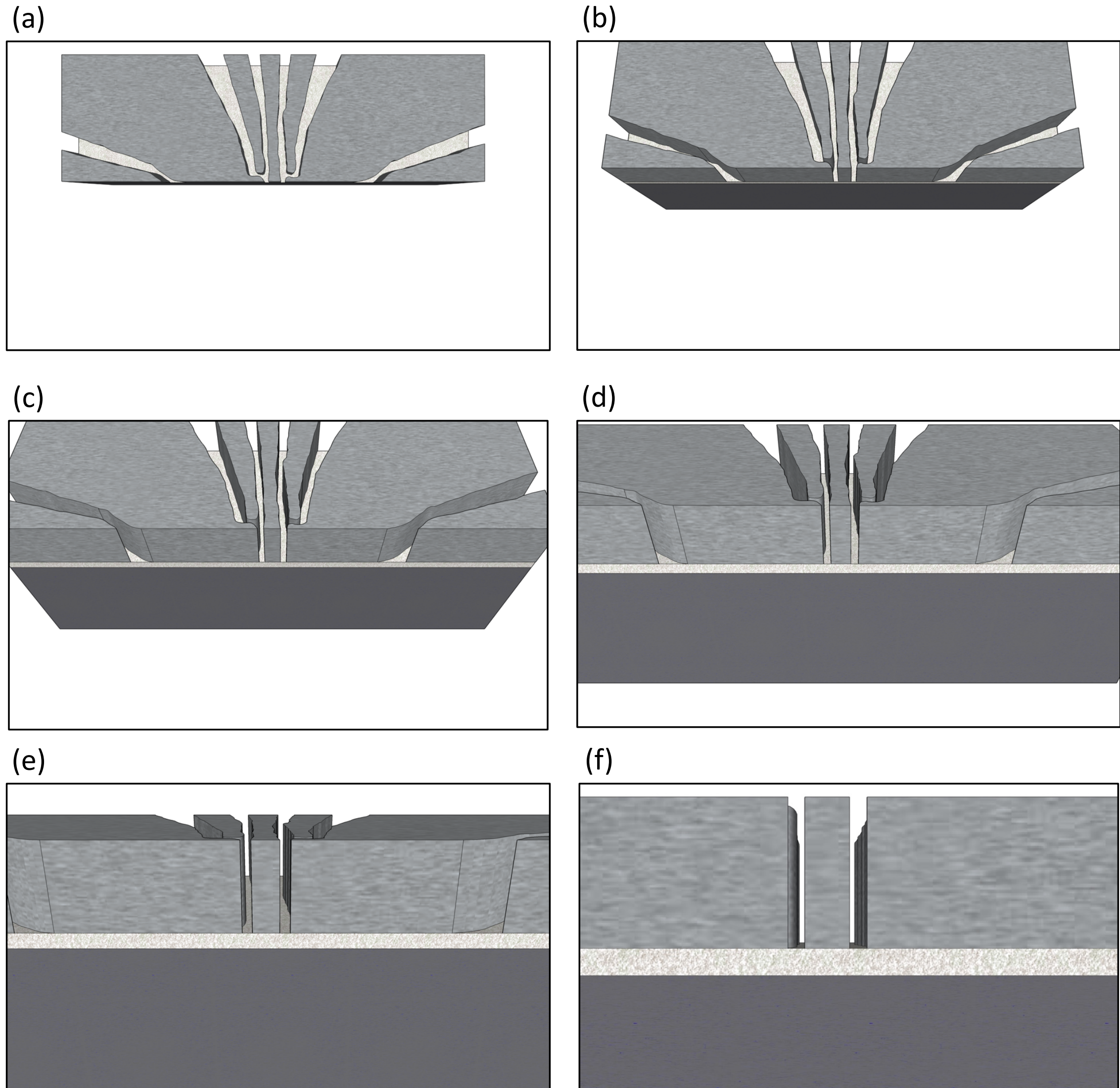

Figure 2.4: Si-MOS 3D Model Sliced Device
Three-dimensional model images of sliced Si-MOS device. The cut has been made through a region of interest where the quantum dot is intended to be formed. (a) Top view. (b)–(e) Multiple orientations of the cut device between top and side view. (f) Side view. The polysilicon and oxide layers are drawn to scale, however not all of the ^{28}Si epilayer is shown.

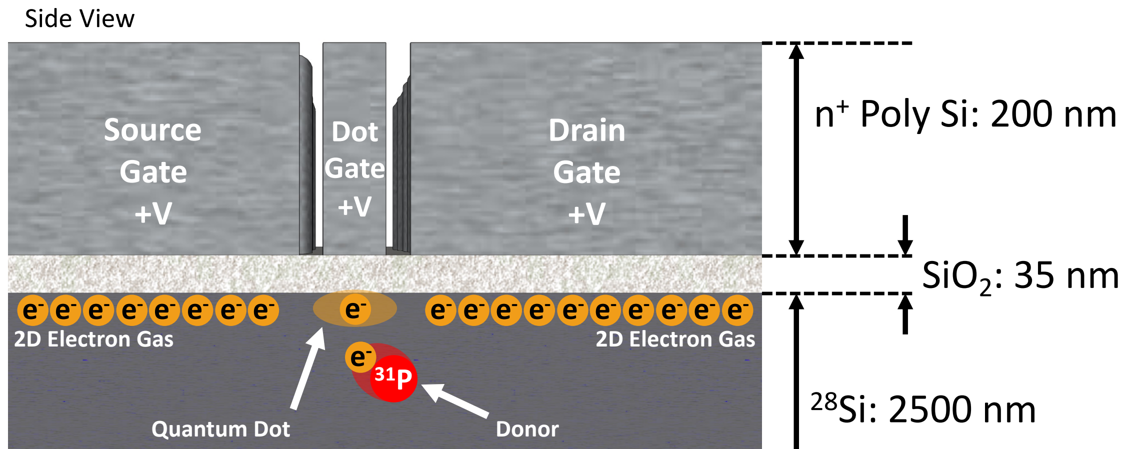

Figure 2.5: MOS Quantum Dot and Donor Atom System
Schematic drawing of a Si-MOS quantum dot and donor atom system. The upper, conductive polysilicon gates generate electric fields which bend the conduction band in the silicon substrate below the Fermi level of the electrons. Larger-area gates such as the "Source Gate" and "Drain Gate" form two-dimensional electron gases (2DEGs) below which act as reservoirs of electrons for the quantum dot. Electrons in the reservoirs are drawn relatively large (the actual surface density of the electrons is around 10^{12} electrons/cm^2). Below the smaller "Dot Gate," the quantum dot is formed by the triangular confining potential against the silicon dioxide and the quadratic potential along the lateral direction. ^{31}P donors are implanted stochastically between the polysilicon gates near the quantum dot.

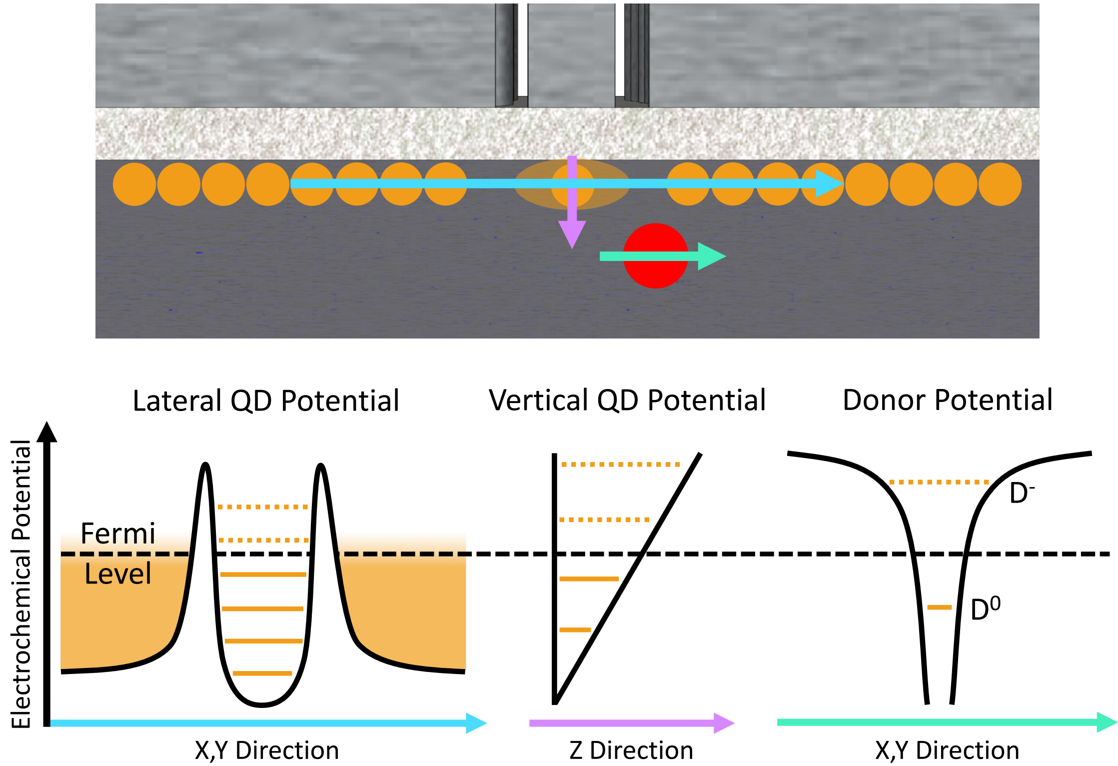

Figure 2.6: Si-MOS QD and Donor Potentials
Electrochemical potential of the conduction band edge for the Si-MOS quantum dot and donor drawn schematically for different directions in the silicon substrate. The uppermost schematic shows the Si-MOS device with color-coded directions for the potential plots below. Orange represents electrons and electron energy levels. In the quantum dot and donor, filled energy levels are drawn as solid, orange lines, and unoccupied energy levels are drawn as dashed, orange lines. The Fermi level is the average value of the electrochemical potential to add an additional electron to the silicon substrate. In the reservoir regions (left and right of the quantum dot), the energy levels are much closer together than in the quantum dot or donor region. The energy levels of the reservoir near the Fermi level are distributed according to a Fermi-Dirac distribution which depends on temperature.

reservoir regions, the energy levels are much closer together than in the quantum dot or donor region, therefore they are drawn as an orange continuum. The energy levels of the reservoir near the Fermi level become faded due to the occupancy probability following a Fermi-Dirac distribution which depends on temperature,

$$n(E) = \frac{1}{e^{(E-E_F)/k_B T} + 1}, \tag{2.2}$$

where n is the occupancy probability, E is the electrochemical potential, $\mathrm{E_F}$ is the Fermi level, k_B is the Boltzmann constant (86.17 μeV/K), and T is the temperature. Figure 2.7 shows a plot of Equation 2.2.

Electrons in a quantum dot have energy from two different phenomena:

1. *Electrostatics*, where the energy stored by adding charge to a capacitor is, $\frac{Q^2}{2C}$, where Q is the total charge and C is the capacitance.

2. *Quantum mechanics*, where the energy levels are dictated by the behavior of the confinement potential. For example, consider an electron in a confinement potential that has vertical walls separated by distance, w, with zero potential inside the walls and infinite potential outside the walls. This is the classic "particle in a box" problem from elementary quantum mechanics classes where the energy levels are given by, $E_n = \frac{n^2 h^2}{2 m_e w^2}$, where n is the level number, h is the Planck constant ($4.136 \cdot 10^{-15}$ eV$\cdot$ s), and m_e is the electron rest mass ($9.11 \cdot 10^{-31}$ kg).

Estimating the energy of electrons in the quantum dot will involve both electrostatics and quantum mechanics. The source and drain reservoirs and electrostatic gate all have a capacitance to the quantum dot (C_S, C_D, C_G) and have voltages applied (V_S, V_D, V_G). The energy of a quantum dot with N electrons is estimated by,

$$U(N) = \frac{(-eN + C_S V_S + C_D V_D + C_G V_G)^2}{2(C_S + C_D + C_G)} + \sum_{n=1}^{N} E_n, \tag{2.3}$$

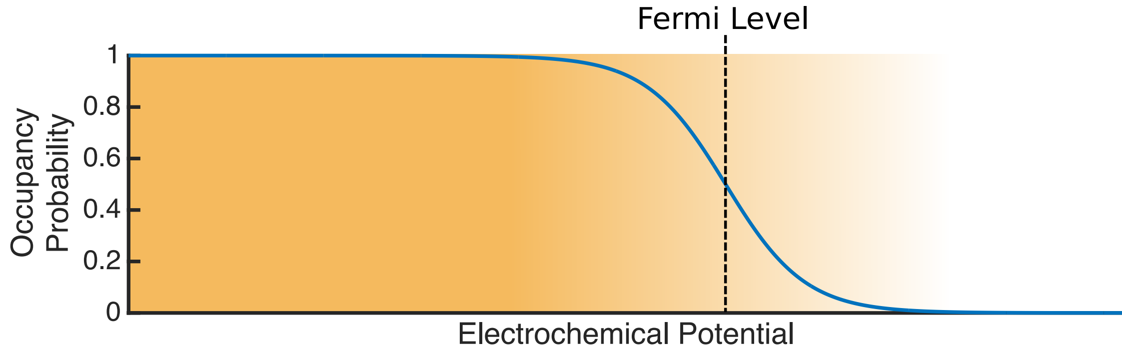

Figure 2.7: Occupancy Probability

The probability that the energy state at a given electrochemical potential will be occupied. This is a plot of Equation 2.2 with the average value of the electrochemical potential to add an electron to the reservoir labeled (which is E_F, the Fermi level). The orange color overlaid represents effectively a continuum of occupied states with white meaning unoccupied. The color changes from orange to white as the occupancy decreases following the Fermi-Dirac distribution. The width of the Fermi-Dirac function depends on temperature, where greater width means higher temperature.

where U is the energy, e is the electron charge ($1.602 \cdot 10^{-19}$ C), and E_n is an electron energy level given by quantum mechanics. Since the energy depends quadratically on the gate voltage, V_G, it is more convenient to work with an energy scale which depends linearly on the gate voltage. The electrochemical potential is such an energy scale, and it is defined as,

$$\mu(N) \equiv U(N) - U(N-1) = \frac{Ne^2}{C} - \frac{e^2}{2C} - \frac{e}{C}(C_S V_S + C_D V_D + C_G V_G) + E_N, \quad (2.4)$$

where μ is the electrochemical potential, C is the total capacitance to the quantum dot ($C_S + C_D + C_G$), and E_N the quantum mechanical energy level of the Nth electron. The electrochemical potential forms a “ladder” of energy levels as each electron is added to the quantum dot. The energy difference between two electrochemical potential levels is,

$$E_{\text{add}}(N) = \mu(N+1) - \mu(N) = \frac{e^2}{C} + E_{N+1} - E_N \equiv E_C + \Delta E, \quad (2.5)$$

where E_{add} is known as the addition energy, E_C is defined as the charging energy

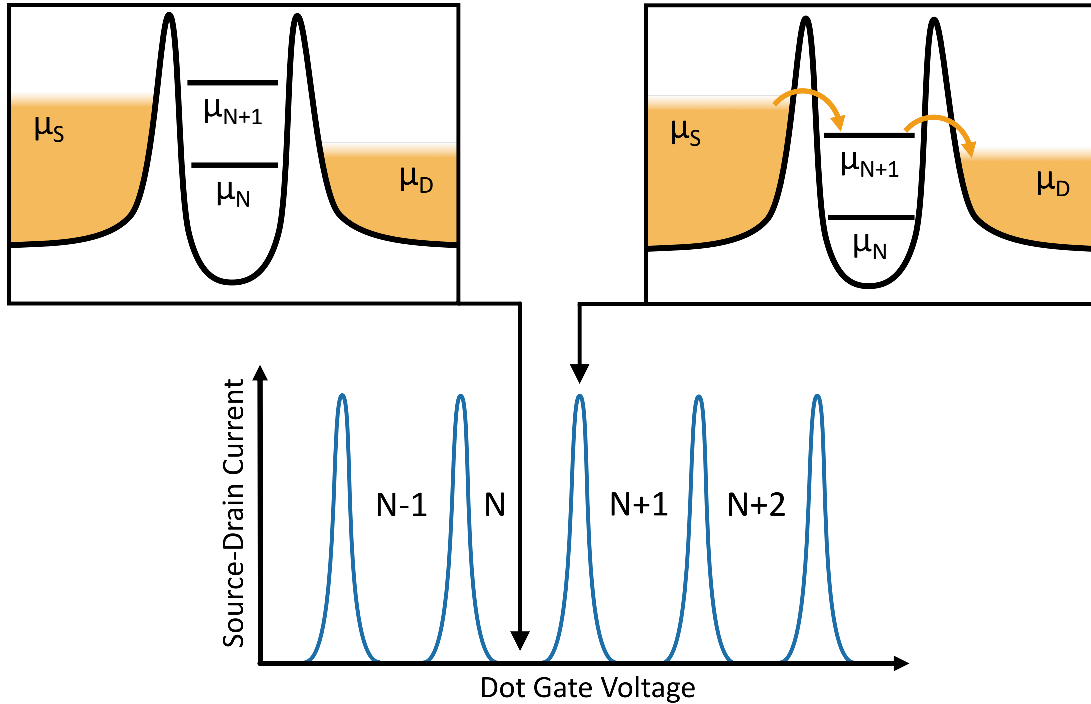

Figure 2.8: Coulomb Blockade
Electrochemical energy of source, drain, and quantum dot showing the phenomenon known as "Coulomb blockade." On the right, there is an available electrochemical potential energy level of the quantum dot between the source and drain bias window, therefore current flows. On the left, there is no available energy level between the bias window and no current flows (Coulomb blockade). As gate voltage is changed, resonances in current show up each time the occupancy of the quantum dot is changed. The width of the resonances depends on temperature.

($E_C = \frac{e^2}{C}$), and ΔE is the difference between two quantum mechanical energy levels of an electron. As expected, the addition energy consists of an electrostatic component (E_C) and a quantum mechanical component (ΔE). For a quantum dot with many electrons, it is typically true that $E_C > \Delta E$.

When a voltage bias is placed across the source and drain reservoirs, the electrochemical potential difference between the two reservoirs is given by, $-e(V_S - V_D) \equiv -eV_{SD} = (\mu_S - \mu_D)$. Current will flow into the source and out of the drain only when

electrons can tunnel into and out of the quantum dot. Electrons will tunnel from the source to the quantum dot and then to the drain only when there is an available electrochemical energy level of the quantum dot in between the source and drain electrochemical potentials. If $|-eV_{SD}| < E_{\text{add}}$, the current through the quantum dot will resonantly change from zero to a peak value as the gate voltage is changed. The phenomenon where electron tunneling is prevented is known as "Coulomb blockade" and is portrayed in Figure 2.8. The upper left plot of Figure 2.8 shows a blockaded, zero-current condition, where there is no quantum dot electrochemical energy level between the source and drain bias window. The upper right plot of Figure 2.8 demonstrates the case where current does flow at the peak of a resonance. As quantum dot gate voltage is decreased (right to left on the plot), electrons are emptied out of the quantum dot with the resonances marking each time the electron occupancy changes by one. The opposite is true if the quantum dot gate voltage is increased. The source-drain current for a given resonance centered around the peak at a gate voltage, V_{center}, is given by,

$$I_{SD}(V_G) = \frac{e^2}{4k_BT}\frac{\Gamma_S\Gamma_D}{\Gamma_S + \Gamma_D}\cosh\left(\frac{\alpha_G(V_G - V_{\text{center}})}{2k_BT}\right)^{-2}, \tag{2.6}$$

where Γ_S is the tunnel rate from the source reservoir to the quantum dot, Γ_D is the tunnel rate from the quantum dot to the drain reservoir, k_B is the Boltzmann constant (86.17 μeV/K), T is the temperature, and α_G is known as the lever arm of the dot gate. The tunnel rate terms and electron charge may be treated as a free parameter for the purposes of fitting the equation to data. The lever arm is a quantity which relates a change in gate voltage to a change in the electrochemical potential of the quantum dot,

$$\Delta\mu_{QD} = \alpha_G \Delta V_G, \tag{2.7}$$

which can be extracted in several ways outlined in Chapter 3 and from a measurement described next.

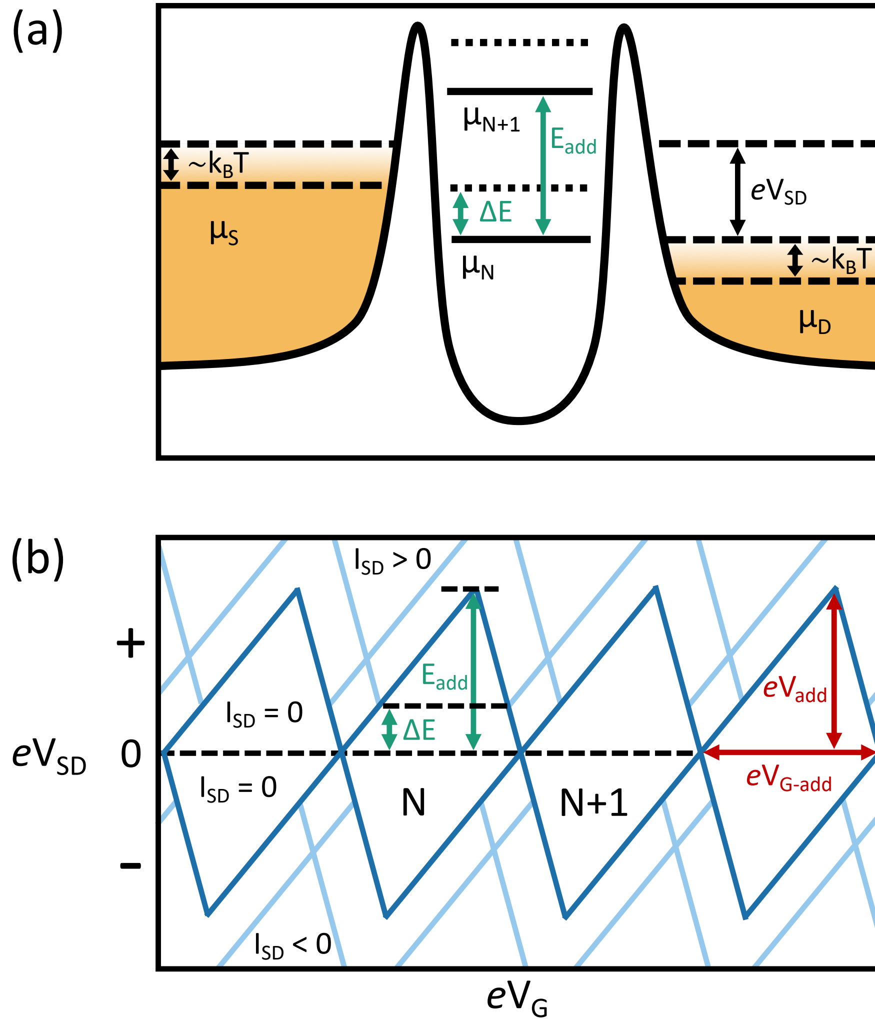

Figure 2.9: Coulomb Diamonds
(a) Electrochemical potential of source and drain reservoirs and the quantum dot. Excited state energy levels in the quantum dot are represented as black dashed lines. The Fermi-Dirac width for the source and drain reservoirs is shown between two dashed lines. The bias between the source and drain is depicted above the electrochemical potential of the drain. (b) Coulomb diamond measurement diagram where the derivative of the source-drain current with respect to the source-drain bias is plotted. The dark blue lines represent changes from zero current to some current. In the "diamond" regions, there is no current flowing. Only the first excited states are shown for simplicity, which are depicted as light blue lines. The addition energy and ΔE are both shown in green. The voltages used to extract the quantum dot gate lever arm are shown in red.

When the source-drain bias is changed against the dot gate voltage and the source-drain current is plotted, a diamond pattern appears. This pattern and measurement are known as "Coulomb diamonds." Figure 2.9(b) shows this effect when the derivative of the source-drain current with respect to source-drain bias is plotted. Dark blue lines represent changes from zero source-drain current to some current. When $|eV_{SD}| < \Delta E$, tunneling of electrons only occurs through the ground state energy as V_G is changed and Coulomb blockade is observed, which is shown in the lower plot in Figure 2.8. When $|eV_{SD}| > \Delta E$, excited state energies will now enter the source-drain bias window in addition to ground state energies as V_G is changed. These excited state energies show up as changes in the current, which are depicted as light blue lines. More excited state energies exist than are shown in Figure 2.9(b), however, only the lowest excited state energies are shown for simplicity. Figure 4.3(d) shows actual data for a Coulomb diamond measurement.

The lever arm may be extracted from a Coulomb diamond measurement by using the following relationship,

$$eV_{\text{add}} = E_{\text{add}} = \alpha_G(eV_{G\text{-add}}), \tag{2.8}$$

where V_{add} is the source-drain bias at the "top" of a diamond, and $V_{G\text{-add}}$ is the gate voltage bias difference across a diamond at zero source-drain bias. Both of these quantities are shown in red on Figure 2.9(b).

Coulomb blockade is a useful phenomenon for measuring more than just the properties of a quantum dot. Coulomb blockade can also be used to sense the movement and number of charges near the quantum dot. When used for this purpose, the quantum dot is referred to as a single-electron transistor (SET) or charge sensor. The Si-MOS nanostructure geometry used in this dissertation has symmetry about the horizontal axis (Figure 2.2). Figure 2.10 shows a top view of the Si-MOS device with regions of electron enhancement colored brownish-orange. The upper quantum dot is intended to be used as a charge sensor and is relatively large with ten or more

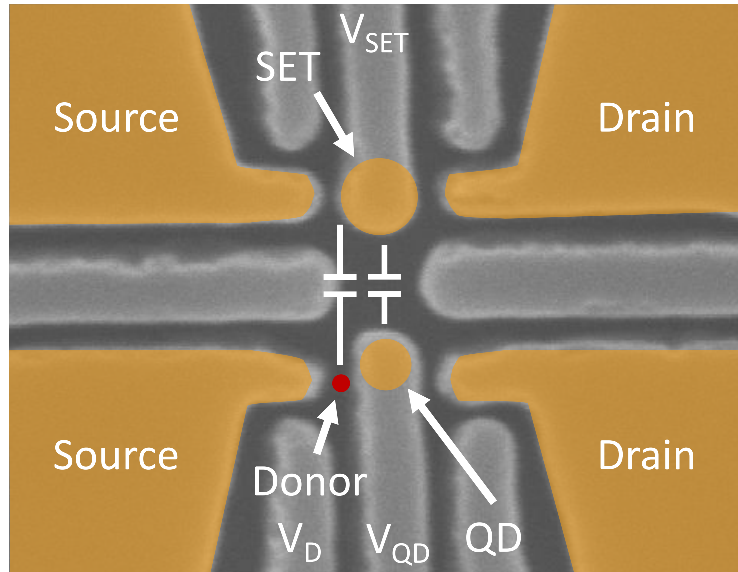

Figure 2.10: Charge Sensor Top View
Top view of Si-MOS device with regions of electron enhancement colorized brownish-orange. Visible on the upper part of the device, the single-electron transistor (SET) is a large quantum dot which acts as a charge sensor. The quantum dot and donor system are visible on the lower portion of the device. The capacitor symbols represent mutual capacitance between the SET and nearby objects with charge.

electrons in it. The intention for making the quantum dot large is to increase the mutual capacitance, C_{mutual}, between it and any other nearby objects with charge. A basic example of detecting the change in charge occupancy of the implanted ^{31}P donor atom is shown in Figure 2.11. When the donor is neutralized (D^0 state occupied), the Coulomb blockade peak in the charge sensor follows the behavior shown in red. When the donor is ionized, the Coulomb blockade peak shifts down in energy and follows the behavior shown in blue. In either of these cases, the voltage, V_{SET}, of the electrostatic gate above the SET is being changed. This is done to illustrate the point that the Coulomb blockade peak shifts location depending on the charge state of the donor. When the voltage, V_D, of the electrostatic gate near the donor is changed, the signal of the Coulomb blockade peak behaves differently.

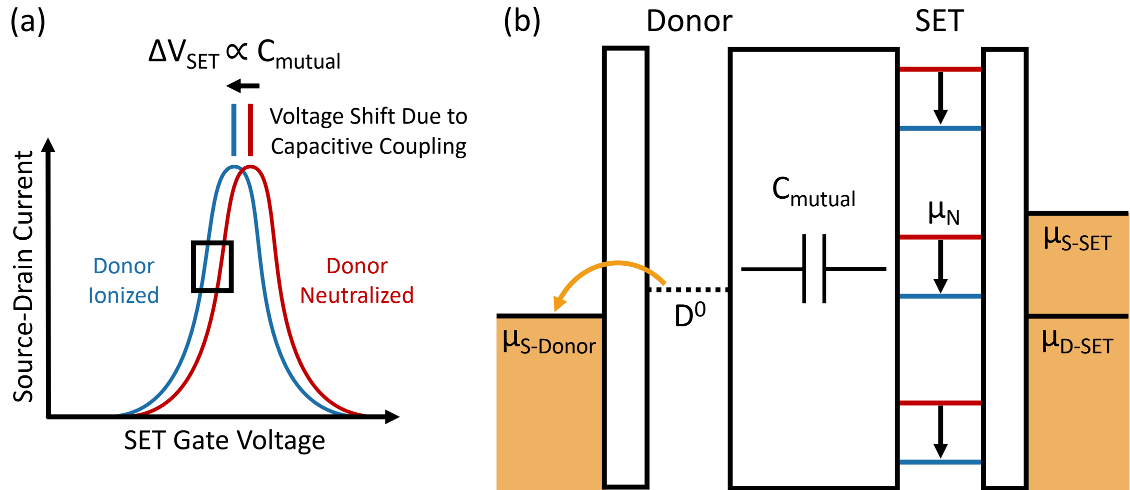

Figure 2.11: Charge Sensing Schematic
(a) Source-drain current vs. electrostatic gate voltage of the single-electron transistor (SET) for two donor charge states. When the donor is neutralized (red), the Coulomb blockade peak is higher in energy. When the donor is ionized (blue), the Coulomb blockade peak shifts lower in energy to the left. The voltage shift is proportional to the mutual capacitance between the SET and donor atom. (b) Electrochemical schematic of the charge-sensing system. The donor atom's D^0 state is shown ionizing into the source reservoir near the donor. The mutual capacitance between the donor and SET is shown in the large tunnel barrier between the two objects. The electrochemical ground states of the SET shift down in energy from the red condition to the blue condition when the donor is ionized.

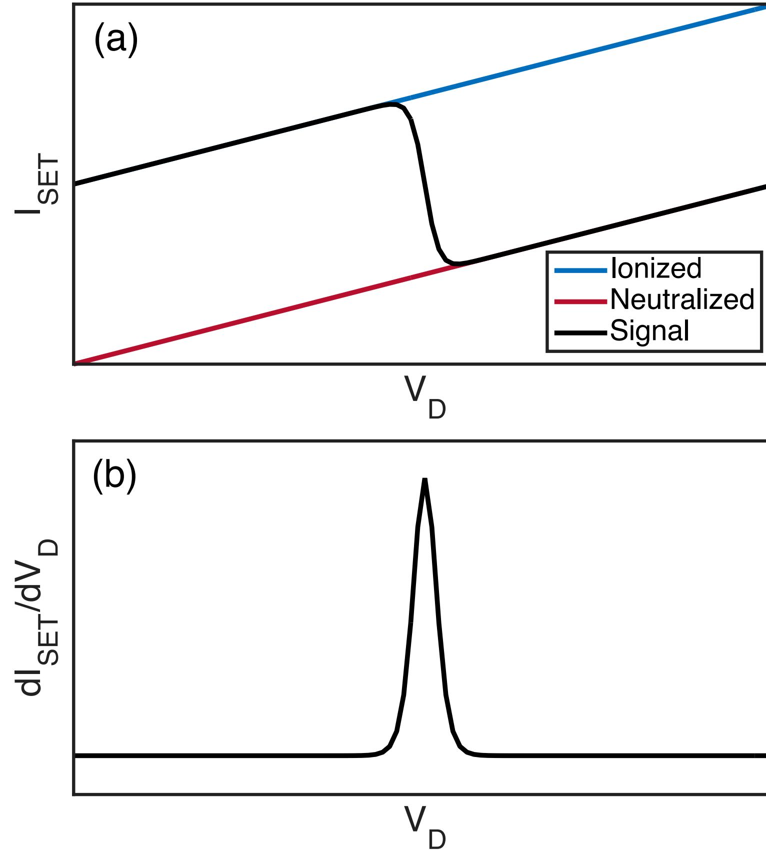

Figure 2.12: Charge Sensing Signal
(a) Equation 2.12 plotted as a function of donor gate voltage. The ionized and neutralized donor charge state currents are plotted as well. An example of data similar to this behavior is plotted in Figure 3.4. (b) The derivative of the charge-sensor signal with respect to the donor gate voltage. The signal forms a peak which is aids in visualizing charge transitions.

If the donor is ionized, the current of the charge sensor will follow an approximately linear behavior for a range of gate voltage biases (shown in the black box of Figure 2.11(a)),

$$I_{\text{ionized}}(V_D) \approx m_{\text{SET}} V_D + I_0, \tag{2.9}$$

where m_{SET} is the sensitivity of the charge sensor, V_D is the gate voltage of the gate near the donor, and I_0 is the current offset. If the donor is neutralized, the current of the charge sensor will follow a similar behavior with a voltage shift due to the mutual capacitance between the donor and charge sensor,

$$I_{\text{neutralized}}(V_D) \approx m_{\text{SET}}(V_D - \Delta V_D) + I_0. \tag{2.10}$$

The voltage shift is,

$$\Delta V_D = \frac{1}{C_{D\text{-SET}}} \frac{\Delta e\, C_{\text{mutual}}}{C_{\text{SET}}}, \tag{2.11}$$

where Δe is the change in charge, $C_{\text{D-SET}}$ is the capacitance between the SET and electrostatic gate near the donor, C_{mutual} is the mutual capacitance between donor and charge sensor, and C_{SET} is the total capacitance experienced by the SET [51]. Note, Equation 2.11 is true if $C_{\text{SET}} \gg C_{\text{mutual}}$ [51]. The change in charge does not occur at a single point in donor gate voltage since the source reservoir's energy occupancy is described by a Fermi-Dirac function (Equation 2.2). Therefore, the charge sensor current can be described by a single equation,

$$I_{SET}(V_D) \approx m_{\text{SET}} \left[V_D + \Delta V_D \left(\frac{1}{e^{(V_D - V_0)/(k_B T/\alpha_D)} + 1} - 1 \right) \right] + I_0, \tag{2.12}$$

where V_0 is the mean donor gate voltage value at which the donor is ionized, k_B is the Boltzmann constant (86.17 μeV/K), T is the temperature, and α_D is the lever arm of the electrostatic gate (typically specified in μeV/mV). Equation 2.12 is plotted in Figure 2.12(a) with the ionized and neutralized donor state currents plotted as well. Data with behavior similar to this is plotted in Figure 3.4. The derivative of

the charge-sensor signal with respect to gate voltage creates a peak that is plotted in Figure 2.12(b). Plotting the derivative of the charge-sensor signal is a method to clearly visualize charge transition resonances. Instead of subtle changes in current on the edge of a Coulomb blockade peak in the charge sensor, there is now a small background with relatively large peaks which represent charge transitions.

So far, one electrostatic gate has been considered for the donor atom ionizing. There are many other gates defined on the Si-MOS nanostructure (see Figure 2.2) and the nearby quantum dot can change occupancy similarly to how the donor atom does, which can then be sensed by the SET. Figure 2.13 shows plots of two gate voltages with the derivative of the charge-sensor current plotted as different colors. These plots are two-dimensional analogs of the example in Figure 2.12(b) with many more charge state transitions. Such a plot is known as a "stability diagram," because resonant lines indicate boundaries of charge stability in the system. For example, in Figure 2.13(a), the system has one electron in the quantum dot between the two charge transition lines which surround the "1" region. The quantum dot was verified to have one electron, in this case, using methods outlined in Chapter 3. The slope of a given charge transition line is equal to the ratio of capacitances from the respective electrostatic gates to the quantum dot,

$$\text{slope} = \frac{C_{QD}}{C_D}. \tag{2.13}$$

Different electrostatic gates will have different capacitance ratios for different objects. Figure 2.13(b) shows the behavior of the stability diagram when the quantum dot is tunnel coupled to a donor atom. The convention used throughout this dissertation to show charge occupancy in both the quantum dot and donor atom is ($N_{\text{e-QD}}$, $N_{\text{e-D}}$), where $N_{\text{e-QD}}$ is the number of electrons in the quantum dot, and $N_{\text{e-D}}$ is the number of electrons in the donor atom. The slope of the charge transition line between the (1,0) and (1,1) regions is different than the slope between the (1,0) and (2,0) regions because the capacitive coupling ratio is different for the gates to the

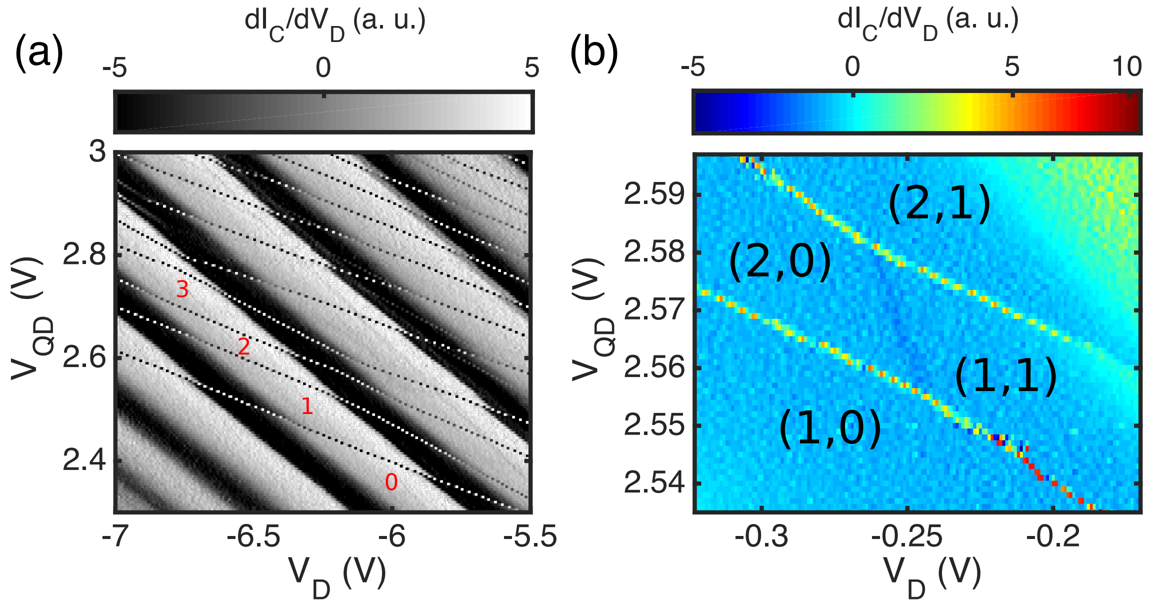

Figure 2.13: Stability Diagrams
(a) Stability diagram showing many charge-sensed quantum dot occupancy resonant lines. The derivative of the charge sensor current with respect to donor gate voltage is plotted. The seven larger "background" oscillations are Coulomb blockade resonances in the charge sensor. The red numbers indicate regions of stable charge occupancy for the quantum dot. (b) Stability diagram showing the (2,0)-(1,1) anticrossing of the quantum dot and donor atom. The faint line in the middle of the plot is the charge state transition line between (2,0) and (1,1).

donor than to the quantum dot, respectively. This stability diagram is an important map for operating the system as a qubit, which is covered in Section 2.3.

2.3 Singlet-Triplet Qubit

The particular type of semiconducting qubit primarily used and referenced in this dissertation is known as a "singlet-triplet" qubit, which was originally demonstrated in 2005 by Jason Petta in a GaAs system [20, 53, 54]. This type of qubit uses two electrons and two confinement potentials where one of the electrons can be

controllably moved from one potential to the other. The quantum dot and donor atom make up the two confinement potentials covered in this work. The occupancy of the system changes according to ϵ (detuning), which is the electrochemical potential of the quantum dot relative to the donor atom. Since there are two electrons in this system, the available spin states are the singlet state and the three triplet states,

$$|\boldsymbol{T_+}, s=1, m_s=1\rangle = |\uparrow\uparrow\rangle, \tag{2.14}$$

$$|\boldsymbol{T_0}, s=1, m_s=0\rangle = \frac{1}{\sqrt{2}}\left(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle\right), \tag{2.15}$$

$$|\boldsymbol{T_-}, s=1, m_s=-1\rangle = |\downarrow\downarrow\rangle, \tag{2.16}$$

$$|\mathbf{S}, s=0, m_s=0\rangle = \frac{1}{\sqrt{2}}\left(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle\right), \tag{2.17}$$

where s is the spin quantum number, m_s is the secondary spin quantum number, $\uparrow$ is an $m_s = +\frac{1}{2}$ electron spin state, and $\downarrow$ is an $m_s = -\frac{1}{2}$ electron spin state. The three triplet states are degenerate until a magnetic field parallel to the plane of the Si-MOS device is applied with a magnitude of around 300 mT. This magnetic field splits the two polarized triplet states, $|T_\pm\rangle$, relatively far away from the unpolarized triplet state, $|T_0\rangle$. Once the polarized triplet states are split away, the qubit is encoded in the $|S\rangle$ and $|T_0\rangle$ subspace, with energy scales dictated by the valley splitting in silicon. Bulk silicon has six conduction band minima which depend on crystallographic direction. These minima cause six-fold degeneracy in energy levels in the conduction band. This degeneracy is partially lifted at the Si-SiO_2 interface where conduction band minima aligned along the x- and y-directions are split off from the minima aligned along the z-direction. The remaining two conduction band minima are split by the relatively strong electric field perpendicular to the Si-SiO_2 interface, where this energy splitting is known as "valley splitting."

When the electrons are in the (2,0) charge configuration ($N_{\text{e-QD}}$, $N_{\text{e-D}}$), the spin states load into the available valley states such that the singlet state, (2,0)S, is the ground state and the triplet state, (2,0)T_0, is the excited state. The energy separation

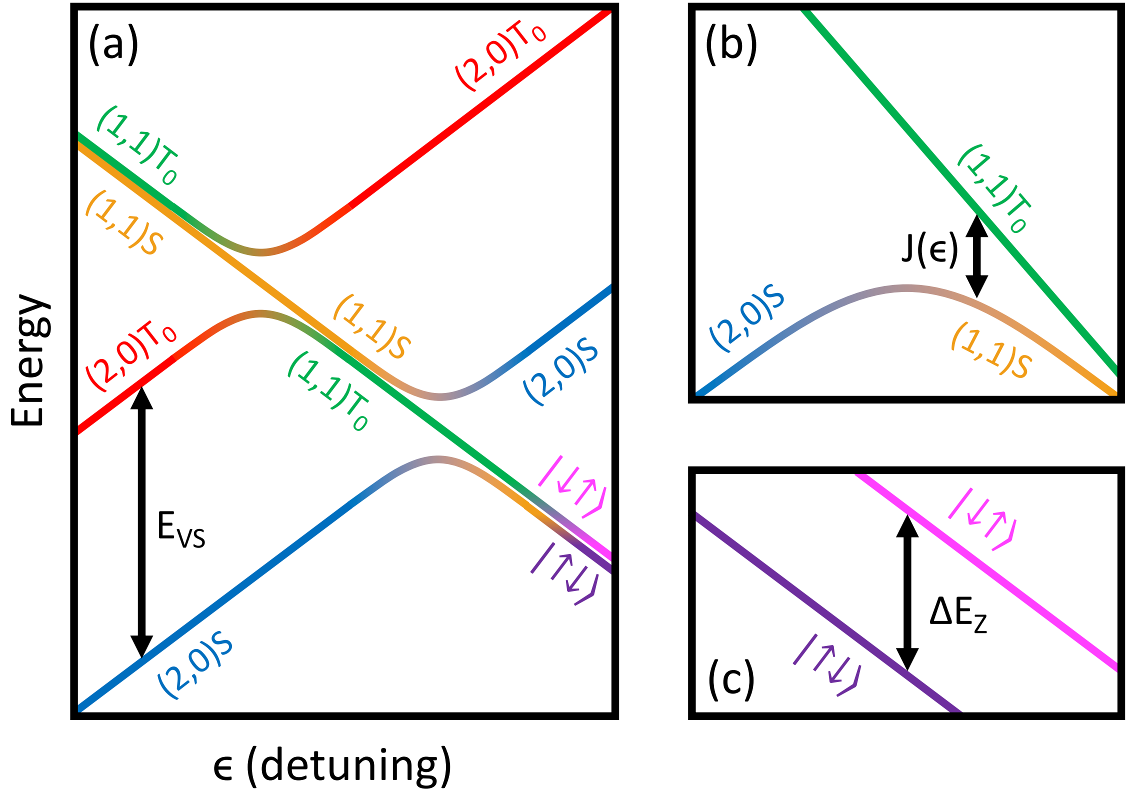

Figure 2.14: Singlet-Triplet Qubit Energy Diagram
Energy levels in the singlet-triplet qubit plotted as a function of detuning. (a) Singlet and triplet (2,0)-(1,1) anti-crossing full diagram. The valley splitting energy, E_{VS}, separates the singlet and triplet (2,0) states. (b) Closer view of the singlet (2,0)-(1,1) anti-crossing showing the exchange energy, $J(\epsilon)$, which strongly depends on detuning. (c) Closer view of the $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ basis relatively far in positive detuning. The effective magnetic field gradient due to the contact hyperfine interaction of the electron localized to the donor atom is what separates the energy of the two states.

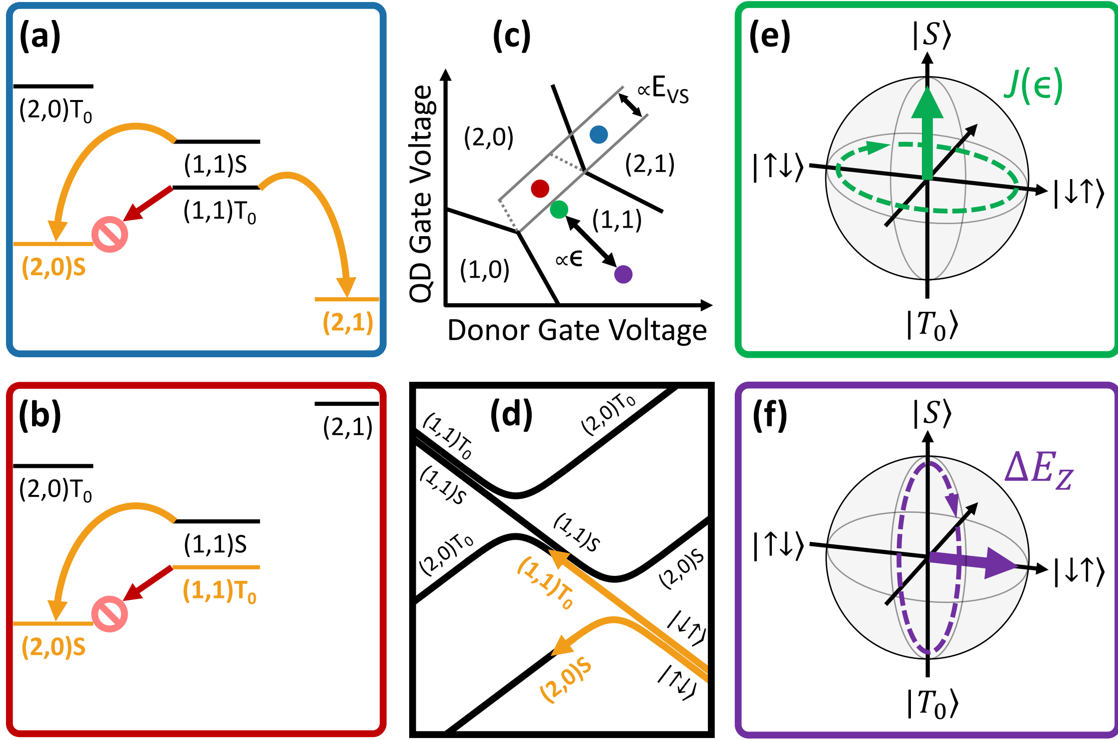

Figure 2.15: Singlet-Triplet Qubit Operation and Readout
Singlet-triplet qubit operation and readout schematic diagram. (a) Latched readout where the (1,1)T_0 state is transferred to the (2,1) state, which increases the readout signal by one electron. (b) Pauli spin blockade readout where the signal is limited by the electric dipole coupling between the qubit and charge sensor. (c) Schematic drawing of the (2,0)-(1,1) stability diagram showing various detuning points and readout points. (d) Energy vs. detuning diagram for the singlet-triplet qubit. Readout paths are shown in orange for the (1,1)T_0 and (2,0)S states. (e) Zero detuning point where the exchange interaction dominates. (f) Positive detuning point where the contact hyperfine interaction dominates.

between (2,0)S and (2,0)T_0 is the valley splitting energy, E_{VS}, which is depicted in Figure 2.14(a) on the lower lefthand side. Since there is tunnel coupling between the quantum dot and donor atom, the (2,0) and (1,1) charge states hybridize for both the singlet and triplet spin states. Figure 2.14(b) shows a closer view of the singlet (2,0)-(1,1) anti-crossing, where the energy of (1,1)S changes relative to the energy of (1,1)T_0. This energy difference is referred to as the exchange interaction, $J(\epsilon)$, which strongly depends on the detuning. The eigenstates of the exchange interaction are (1,1)S and (1,1)T_0.

The electrons experience an effective magnetic field gradient if they are in (1,1) due to the contact hyperfine interaction between the spin of the electron localized to the donor atom and the nuclear spin of the donor atom,

$$\Delta E_Z = A\hat{S} \cdot \hat{I}, \tag{2.18}$$

where A is the contact hyperfine term, $\hat{S}$ is the electron spin operator, and $\hat{I}$ is the nuclear spin operator. The eigenstates of the contact hyperfine term are $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$. Since (1,1)S and (1,1)$T_0$ are no longer eigenstates when the contact hyperfine term dominates, rotations between (1,1)S and (1,1)T_0 occur. The simplified Hamiltonian of the system is,

$$\hat{H}_{ST} = \frac{-J(\epsilon)}{2}\hat{\sigma}_z \pm \frac{A(\epsilon)}{4}\hat{\sigma}_x, \tag{2.19}$$

where $\hat{\sigma}_z$ and $\hat{\sigma}_x$ are the Z and X Pauli spin matrices respectively. Factors of 1/2 in the Hamiltonian come from the spin operators, and the sign in front of the contact hyperfine term changes depending on the spin state of the donor nuclear spin [22]. In Figure 2.15(c), the green detuning point is where Z rotations of the qubit are performed due to the exchange interaction. X rotations are performed at the purple detuning point where the contact hyperfine term of the Hamiltonian dominates. Z and X rotations about the singlet-triplet qubit Bloch sphere are shown in Figures 2.15(e) and 2.15(f), respectively.

Readout of the singlet-triplet qubit can be performed in several different ways. The simplest form of readout is known as "Pauli spin blockade" [55]. After qubit rotations are performed, the system is adiabatically biased to the red detuning point shown in Figure 2.15(c) with the state of the system following one of the orange paths shown in Figure 2.15(d). Figure 2.15(c) shows the energy levels of the system at the red detuning point. The (1,1)S state transfers to the (2,0)S state, however, the (1,1)T_0 state cannot transfer to (2,0)S due to the conservation of spin angular momentum. When the charge sensor detects movement of charge, the qubit is measured to have been in a singlet state. Similarly, if there is no movement of charge, the qubit is measured to have been in a triplet state. This form of readout is limited by the electric dipole coupling of the quantum dot and donor atom system to the charge sensor. If the electron does not move toward or away from the charge sensor, the signal is severely reduced and can cause readout to be slow with low fidelity.

A form of readout which increases the signal by one electron is known as "latched readout" [5]. This form of readout begins exactly the same as with the Pauli spin blockade readout. After the system is biased to the red detuning point in Figure 2.15(c), the system is then rapidly biased to the blue detuning point. The (2,1) charge state is lowered below the energy level of (1,1)T_0, which results in an electron loading into the quantum dot. Now, (1,1)T_0 is mapped to (2,1) resulting in a signal difference of one electron rather than a movement of charge. The latched readout can also be performed with the system biased to a point in the opposite direction relative to going from the red point to the blue point. In this case, the (1,0) level is lowered below other energies and the (2,0)S state is transferred to (1,0) leading to the same signal difference of one electron. The latched readout is limited by the metastable lifetime of the (2,0)S state as well as other relaxation and transfer rates outlined in Section 3.6.

2.4 Cryogenic Amplification

Sections 2.2 and 2.3 have outlined how singlet-triplet qubits are created, operated, and measured. The measurement of the singlet-triplet qubit or any other spin qubit in semiconductors involves mapping the spin states to charge states. The charge states are usually detected by a charge sensor which will change conductance proportional to the mutual capacitance between itself and the qubit. Various techniques exist to determine the conductance of the charge sensor rapidly while minimizing noise, with the exception of techniques that effectively use the electrostatic gates as sensors. The techniques include embedding the charge sensor into an RF resonant circuit [56, 57], coupling the charge sensor to a superconducting resonator [58], dispersive RF gate sensing [59], and cryogenic amplifiers [6, 60–63]. A summary of the single-shot performance of these techniques is shown in Table 2.1. In general, RF techniques provide the lowest charge sensitivity, while transistor techniques provide reasonably low charge sensitivity with considerably lower implementation overhead.

This dissertation focuses on the cryogenic amplifier approach for improving the readout of silicon spin qubits. Due to the relatively small energy scales found in semiconducting qubits, the temperature at which the qubits are operated at must be around 100 mK or lower (see Section 3.3). Therefore, the qubit is operated at the mixing chamber stage of a dilution refrigerator, which is shown in Figure 2.16. The upper two stages are cooled by a pulse tube refrigerator, where a closed-loop helium expansion cycle removes heat from the system. The mixing chamber stage uses the enthalpy of mixing of ^{3}He and ^{4}He to cool the system to temperatures as low as 20 mK [64, 65].

Conventional approaches for improving the signal-to-noise ratio (SNR) of a readout signal do not necessarily work at the low temperatures required for qubit operation. For example, a transimpedance amplifier (TIA) can be used to amplify current,

Technique	Carrier Frequency	Bandwidth	SNR	Charge Sensitivity $\left(\mu e/\sqrt{\text{Hz}}\right)$	Input Referred Noise $\left(\text{fA}/\sqrt{\text{Hz}}\right)$	Citation
HBT (Single Stage)	None	20 kHz	7.5	330	20	Ch. 6 & [63]
HBT (Dual Stage)	275 kHz	100 kHz	7.5	400	25	Ch. 6
HEMT (Single Stage)	None	800 kHz	3	400	133	[62]
HEMT (Dual Stage)	300 kHz	100 kHz	10	350	70	[6]
RF-QPC	763 MHz	1 MHz	7	146	—	[57]
RF-SET	220 MHz	10 MHz	4	140	—	[56]
RF Gate Sensing	700 MHz	30 kHz	1	6000	—	[59]
Super-conducting Cavity and JPA	7.88 GHz	2.6 MHz	9	80	—	[58]

Table 2.1: Single-Shot Readout Techniques (2018)
Summary of the state of the art of various single-shot readout techniques used on semiconducting qubits as of 2018. Charge sensitivity is calculated using, $\sqrt{\tau_{int}}/\text{SNR}$, where τ_{int} is the integration time necessary to achieve the given SNR. Most numbers shown are approximate values.

but the electronics used in the TIA will experience carrier freeze-out and not function at cryogenic temperatures. Moreover, even if conventional TIAs did operate at cryogenic temperatures, the power dissipated by their circuitry would be orders of magnitude greater than the cooling power of the dilution refrigerator, which is around 100 μW. This limits TIA operation to be at room temperature. The typical setup for measuring the conductance of a charge sensor is depicted in Figure 2.17(a). An AC or DC voltage source is connected to an ohmic contact of the charge sensor. Depending on the conductance of the charge sensor, certain currents will flow out of the charge sensor and up into a room temperature TIA. Typically, the current

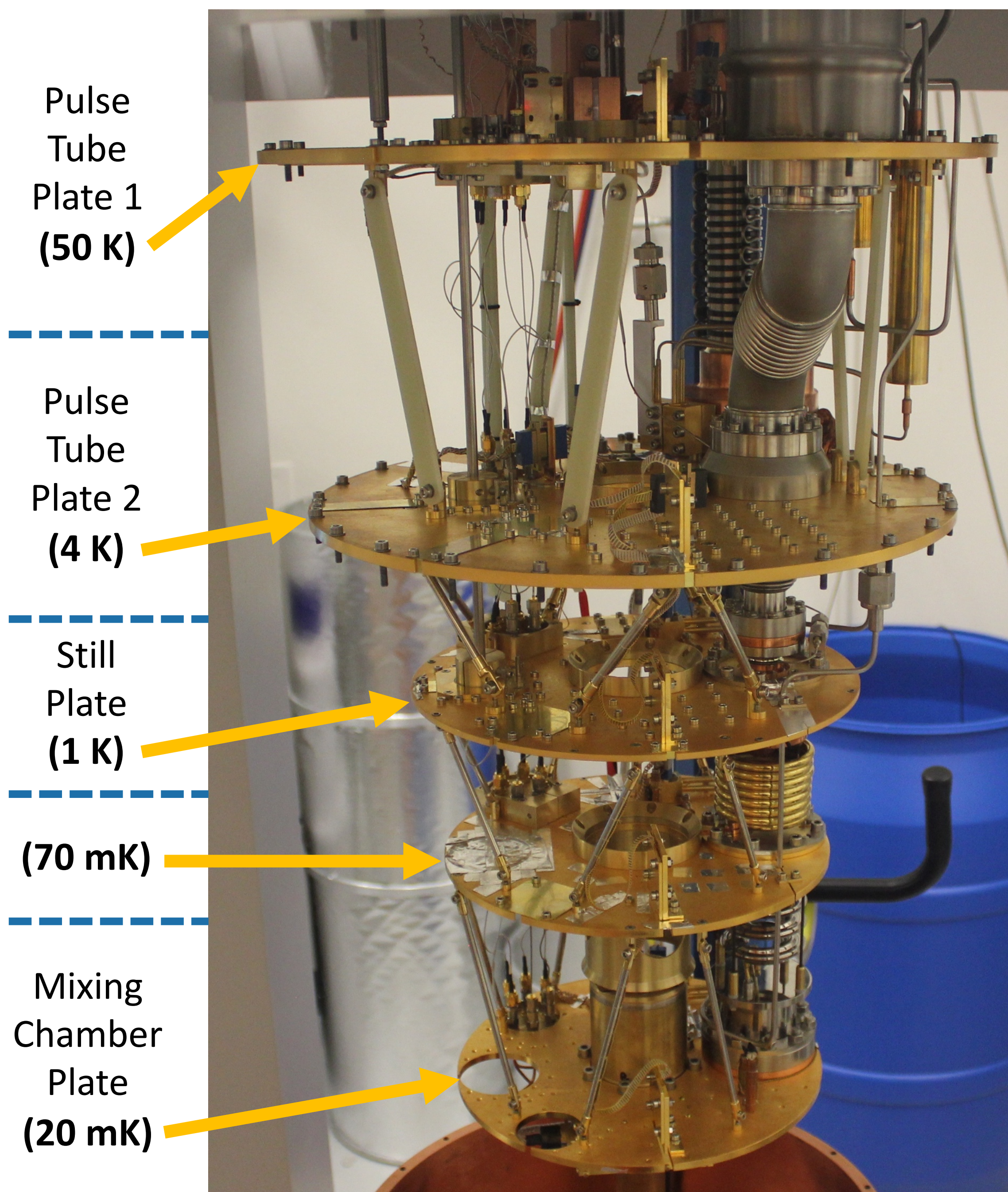

Figure 2.16: Inside of Dilution Refrigerator

signal will be around 100 pA, which is relatively small considering what the TIA is designed to amplify. This basic measurement setup has two limitations. Firstly, due to the relatively small readout signal, the gain of the TIA will need to be increased to a value which is relatively high (e.g., 10^8 V/A). As a result, the bandwidth of the TIA will be lower than desired (e.g. 1 kHz). Since the TIA is located about 1 meter away from the charge sensor, the coaxial cables used to electrically connect the two devices will introduce a parasitic capacitance of around 200 pF. This parasitic capacitance will further limit the bandwidth of the TIA. Secondly, vibrations from the various pumps used in the dilution refrigerator cause triboelectric noise on the same line which carries the readout signal [66].

Cryogenic amplification is one way to lift the limitations of the basic measurement setup. Transistors which work at cryogenic temperatures and dissipate low amounts of power are required for cryogenic amplification. Fortunately, several commercially available models have been identified which satisfy these criteria (Chapter 5). Currently, either a heterojunction bipolar transistor (HBT) [63] or a high-electron-mobility transistor (HEMT) [6, 62] are known to work as a cryogenic amplifier. These transistors can be used to design amplification circuits which dissipate power between 100 nW to 10 μW. Figure 2.17(b) shows the basic measurement setup enhanced with a cryogenic amplifier on the mixing chamber stage of the dilution refrigerator. The cryogenic amplifier provides signal gain between 10 and 1000 with only centimeters of wire between itself and the charge sensor. The increase in the signal before system noise is introduced results in greater SNR. The evidence for this benefit is shown in Figure 2.18, where several noise spectral density traces are plotted for different cryogenic amplifier gains. For these traces, the noise is referred to the output of the cryogenic amplifier, which is a current-biased HBT circuit (see Chapter 5 and Section 6.3). As the gain is increased, many of the noise peaks are gradually decreased relative to the average value of a given noise trace. For example, when the HBT gain is in the thousands (green data), almost none of the noise peaks

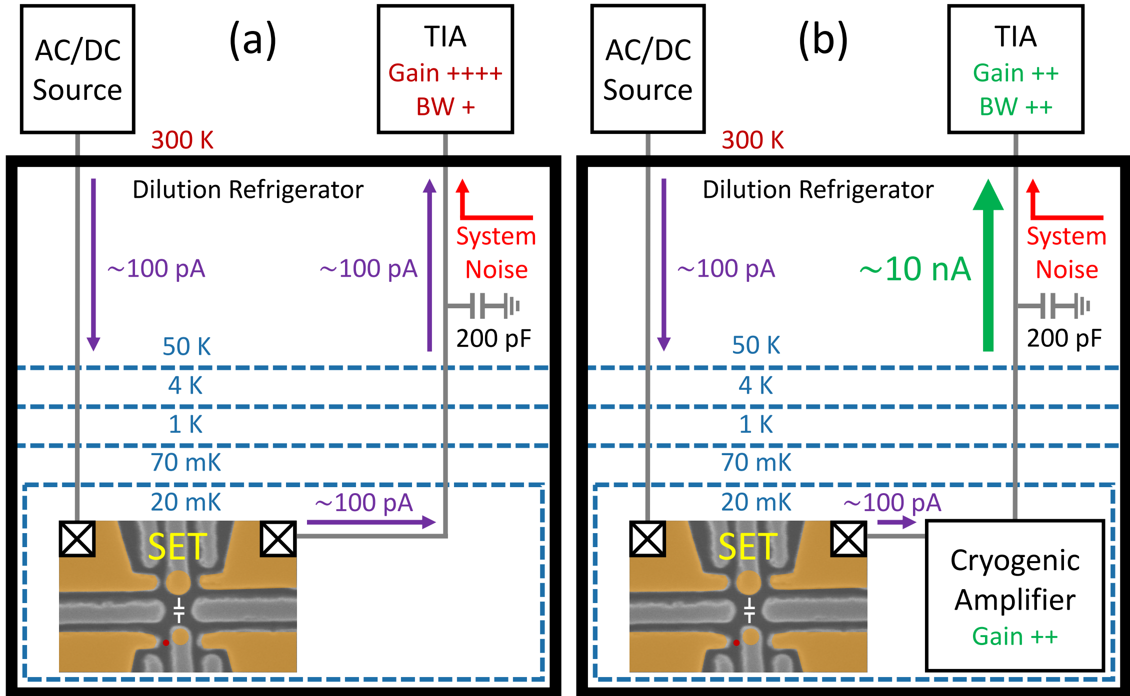

Figure 2.17: Cryogenic Amplification

Schematic diagram of two charge-sensor measurement setups (not drawn to scale). (a) The basic setup used to measure semiconducting spin qubits. The AC or DC source supplies a voltage bias and causes current to flow through the SET. Depending on the conductance of the SET, different currents will enter the transimpedance amplifier. As the current travels up the wire to the TIA, the system introduces noise and a parasitic capacitance around 200 pF is added from the coaxial cable. The signal entering the TIA is relatively small, therefore, the gain of the TIA must be increased to a relatively high value and bandwidth is lowered as a result. (b) A cryogenic amplifier is added to the basic measurement setup. The cryogenic amplifier increases the signal before the system noise and parasitic capacitance are introduced. As a result, the gain of the TIA may be lowered and the bandwidth of the TIA increases.

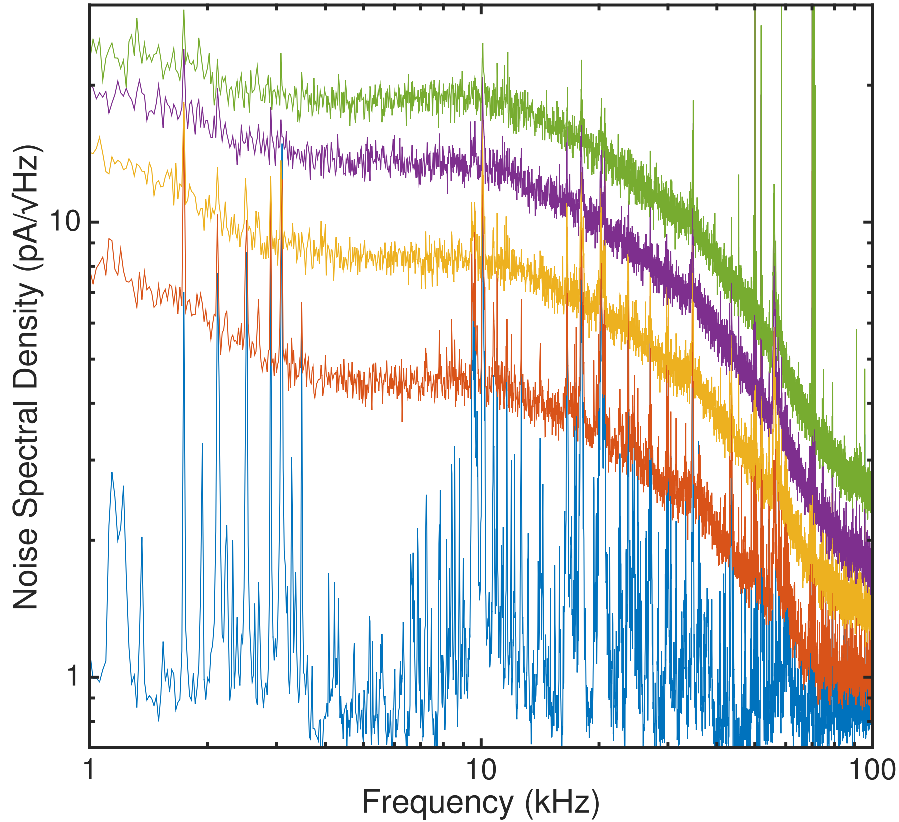

Figure 2.18: Noise Dependence on Gain
Noise spectral densities referred to the HBT collector for the CB-HBT. The blue curve on the bottom of the plot corresponds to low HBT gain. The gain is gradually increased for the next few noise spectral densities above. Many noise peaks relative to the average value of a given noise trace are minimized as the gain is increased.

found at tens of kHz or lower are visible anymore. The noise originating near the charge sensor, which was not observable at low HBT gain values, is visible above the system noise at higher HBT gains. When the gain of the HBT is divided out from the noise referred to the output, the value for the noise at the input is between 10 and 20 fA/$\sqrt{\text{Hz}}$ on average (Figure 6.3(b)), which is around 100 times lower than the minimum observed system noise (1 pA$\sqrt{\text{Hz}}$) in the basic measurement setup.

Chapter 3

Experimental Methods

3.1 Introduction

Fabricating a silicon spin qubit is the first step in getting the qubit operational. Many additional steps are required after the qubit is inserted into a dilution refrigerator and connected to control instruments. In this chapter, the process of electrostatically "tuning" the quantum dot and donor atom system into a qubit is described in several sections. The first section covers the tuning of the rate of electrons tunneling from the quantum dot to the nearby electron reservoir. This tunnel rate is necessary to tune appropriately for reliable qubit initialization. Next, a discussion on measuring and minimizing electron temperature is made. Electron temperature is a parameter which will reduce the fidelity of the qubit if it is too great relative to the qubit's excited state energy. Magnetospectroscopy, the process of measuring the qubit's excited state energy, is then discussed in the context of verifying the few-electron regime. Then, the measurement of the tunnel coupling between the quantum dot and donor atom is described, which is crucial for qubit operation considering instrumentation and coherence limitations. Finally, this chapter concludes on single-shot readout

performed after all the previous qubit tuning is correctly implemented.

3.2 Tunnel Rate Spectroscopy

Reliable initialization of a qubit is crucial for building a digital quantum computer [36]. For singlet-triplet spin qubits covered in this section, the system is initialized with one electron (see Section 2.2) and then a second electron is loaded into the system via a nearby electron reservoir. The rate at which the second electron is loaded is important for determining whether or not the qubit will be in a singlet state (ground state) or a triplet state (excited state).

Tunnel rate spectroscopy is the process where the electrochemical potential of the quantum dot is pulsed at different frequencies and its average value is moved into resonance with an electron reservoir. The goal of tunnel rate spectroscopy is to measure the singlet loading rate of the quantum dot, f_{singlet}. The nearby charge sensor is biased to the (approximately linear) edge of a Coulomb blockade peak as outlined in Section 2.2. When there is one electron in the quantum dot, the current of the charge sensor will follow a linear behavior for a range of gate voltage biases,

$$I_{1e}(V_G) \approx m_{CS} V_G + I_0, \tag{3.1}$$

where m_{CS} is the sensitivity of the charge sensor, V_G is the gate voltage of the pulsing gate, and I_0 is the current offset. When there are two electrons in the quantum dot, the current of the charge sensor will follow a similar behavior with a voltage shift due to the mutual capacitance between the quantum dot and charge sensor,

$$I_{2e}(V_G) \approx m_{CS}(V_G - \Delta V_G) + I_0. \tag{3.2}$$

The voltage shift is, ΔV_G, which is proportional to the mutual capacitance between the quantum dot and charge sensor (Equation 2.11). The change in charge does not

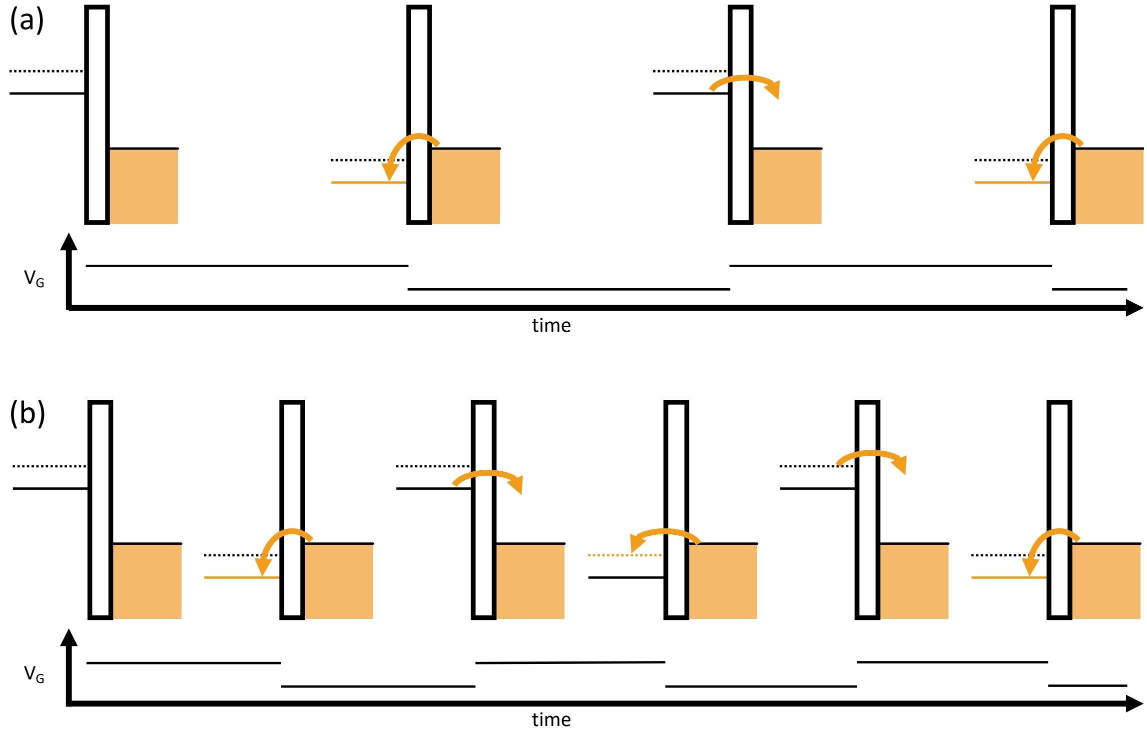

Figure 3.1: Tunnel Rate Spectroscopy Example
(a) Lower-frequency tunnel rate spectroscopy. In this case, $f_{\text{pulse}} < f_{\text{singlet}}$, so only the ground state is loaded when the ground and excited state electrochemical potentials are pulsed below the average value of the electrochemical potential of the electron reservoir. (b) Higher-frequency tunnel rate spectroscopy. Here, $f_{\text{pulse}} \approx f_{\text{singlet}}$, therefore the excited state will be loaded occasionally during a pulse cycle.

occur at a single point in gate voltage since the electron reservoir's energy occupancy is described by a Fermi-Dirac function (Equation 2.2). Therefore, the charge sensor current can be described by a single equation,

$$I_{CS}(V_G) \approx m_{CS}\left[V_G + \Delta V_G\left(\frac{1}{e^{(V_G - V_0)/(k_B T/\alpha_G)} + 1} - 1\right)\right] + I_0, \tag{3.3}$$

where V_0 is the mean gate voltage value at which the second electron is loaded, k_B is the Boltzmann constant (86.17 μeV/K), T is the temperature, and α_G is the lever arm of the electrostatic gate (typically specified in μeV/mV). Subtracting out the linear term ($m_{CS}V_G$) in the charge sensor current leaves two distinct occupancy

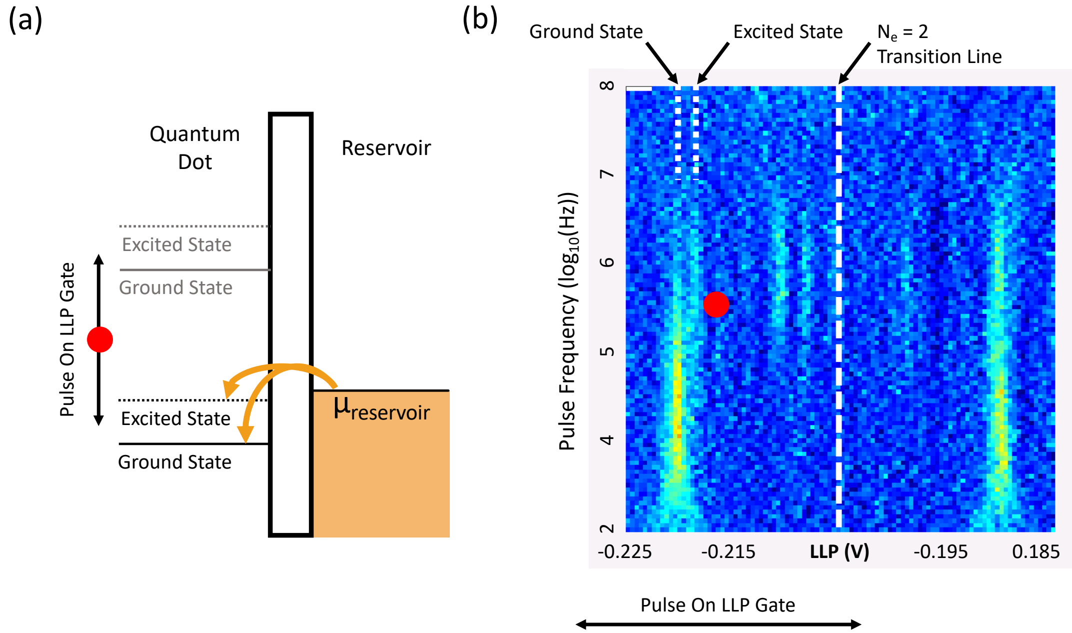

Figure 3.2: Tunnel Rate Spectroscopy: Higher Frequency
(a) Energy level schematic corresponding to loading at a rate, $f_{\text{pulse}} \approx f_{\text{singlet}}$. Either the ground or excited state can be loaded in this case (as indicated by orange arrows). (b) Data of tunnel rate spectroscopy. The second resonant line appears next to the first, indicating that the excited state is now being loaded during a pulse cycle.

cases,

$$I_{CS}(V_G) - m_{CS}V_G = \begin{cases} I_0 & (V_G < V_0) \\ I_1 \equiv I_0 - m_{CS}\Delta V_G & (V_G > V_0). \end{cases} \tag{3.4}$$

The pulse used in tunnel rate spectroscopy is typically a square pulse with amplitude, V_{amp}, voltage offset, V_G, and frequency, f_{pulse}. When pulsing such that $V_G < (V_0 - V_{\text{amp}}/2)$, the average charge sensor offset signal will be I_0, since the ground and excited state electrochemical potentials always remain unloaded above the electrochemical potential of the reservoir. When pulsing such that $V_G > (V_0 + V_{\text{amp}}/2)$, the average offset signal will be I_1, since the ground and excited states always remain loaded below the electrochemical potential of the reservoir. If $(V_0 - V_{\text{amp}}/2) < V_G <$

$(V_0 + V_{\text{amp}}/2)$ and $f_{\text{pulse}} < f_{\text{singlet}}$, the average offset signal will be $(I_0 + I_1)/2$, since the qubit spends an equal amount of time loaded and unloaded. This relatively low-frequency condition is shown as a conceptual diagram in Figure 3.1(a), where only the ground state is loaded and the quantum dot is occupied by a second electron only half the time (charge sensor signal offset is in-between both cases in Equation 3.4). The data for this condition is shown in Figure 3.2(b) for pulsing frequencies around 10 kHz (4 on the log scale). The data plotted is the derivative of the charge sensor current, therefore only resonant features show up. The resonances are the lighter colored lines representing a change from one charge sensor offset current to another. The resonant line to the left of the $N_e = 2$ occupancy line (separated by half the pulse amplitude) is where the loading of the ground state begins as the voltage offset of the pulse is increased. The other resonant line to the right of the $N_e = 2$ occupancy line is where the unloading begins as the voltage offset of the pulse is increased.

When $f_{\text{pulse}} \approx f_{\text{singlet}}$, a second resonant line will appear in the data corresponding to the loading of the excited state (Figure 3.2(b) to the left of the red dot). This resonant line appears because the ground state is not loading each pulse cycle due to the pulse frequency being relatively fast. Instead, the excited state is occasionally loaded, which is shown as a conceptual diagram in Figure 3.1(b). The red dot in Figure 3.2 is the pulsing gate offset voltage where both the ground and excited states can load. Therefore, the red dot would not be an ideal voltage offset and frequency to load only the ground state of the qubit. If the pulsing gate offset voltage is adjusted such that it is in between the ground and excited state loading lines, the singlet state will be the only state loaded because the electrochemical potential of the excited state never gets below the average value of the electrochemical potential of the electron reservoir. Therefore, tunnel rate spectroscopy can be used to extract the appropriate loading bias voltage for qubit initialization. The frequency where the excited state loading line appears is approximately f_{singlet}, and singlet states can be

reliably loaded at frequencies less than that value and at voltage offsets in between the two loading lines.

It is important to observe the excited state loading line appearing at frequencies which allow rapid loading of the qubit to perform computations quickly and repeatedly. If the excited state loading line appeared much lower (e.g., 10 kHz), the number of computations able to be performed in a given time period would be significantly reduced. For this experimental setup, in particular, a bias tee was used on the pulsing gate to enable lower electron temperature (see Figure 3.3). This bias tee acts as a high pass filter on pulses sent to the gate, therefore if the singlet loading rate was less than the cutoff frequency of the high pass filter (1 kHz), singlet states would not be able to be loaded reliably.

Once tunnel rate spectroscopy is initially performed on the qubit and the singlet loading rate is extracted, the loading rate is tuned to be practical and compatible with the experimental parameters outlined above. The tuning is done by increasing or decreasing the tunnel barrier dimensions in between the quantum dot and electron reservoir. Manipulating the tunnel barrier dimensions is accomplished by using nearby electrostatic gates with relatively large amounts of capacitive coupling to the tunnel barrier. This tuning will manifest itself as the shifting of the excited state loading line in frequency in tunnel rate spectroscopy. After careful tuning, the qubit will be reliably initializing and ready for different parameters to be tuned or computations to be performed.

3.3 Electron Temperature

The temperature of the electrons is critical to measure and necessary to minimize in silicon spin qubits. If electron temperature is large relative to the valley splitting of the qubit, the ground state may suffer random excitations into the excited state.

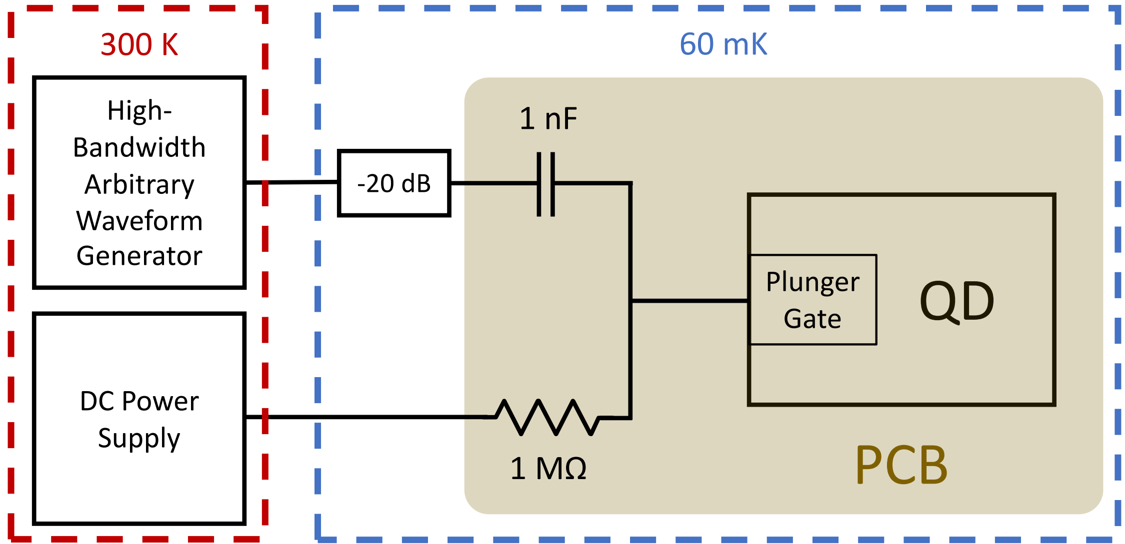

Figure 3.3: Electrostatic Gate Bias Tee Schematic
Schematic of the bias tee used on an electrostatic gate to rapidly control the quantum dot and prevent electron heating. Room temperature voltage supplies are connected to the device either resistively (DC) or capacitively (AC). The higher-bandwidth line leading to the device is attenuated by -20 dB (factor of ten in voltage) to reduce room temperature Johnson-Nyquist noise. The bias tee consists of two discrete components on the PCB where the quantum dot silicon die is mounted. In this case, the resistor was 1 MΩ and the capacitor was 1 nF. Signals sent to the higher-bandwidth line will need to dissipate powers less than 100 μW into the attenuator so that they do not heat the mixing chamber stage of the dilution refrigerator.

Typically, the valley splitting is around 100–300 μeV in the Si-MOS devices fabricated at Sandia National Laboratories (Section 4.8). The energy associated with the electron temperature will need to be at least a factor of ten less than the valley splitting in order to achieve high fidelity operation. Therefore, the electron temperature should be around 10–30 μeV or 116–348 mK. Dilution refrigerators using a mixture of ^{3}He and ^{4}He can run at temperatures as low as 5 mK [64, 65]. This temperature is the nominal temperature of the silicon device mounted at the mixing chamber stage of the dilution refrigerator, however, the temperature of the electrons is usually measured to be higher.

Several reasons for the temperature discrepancy exist: first, silicon has much lower piezoelectric phonon coupling to electrons than gallium-arsenide [67, 68]; second, there are electrically conductive lines leading down to the device from room temperature to control the occupancy of the quantum dot and operate the qubit. Many of these lines are filtered using a low-pass filter with a cutoff at lower frequencies (100 Hz) or higher frequencies (10 kHz). For the electrostatic gates nearest the quantum dot and donor atoms, the lines must respond at a much higher frequency in order to operate the qubit rapidly relative to the tunnel coupling (100 MHz to GHz). If lines with GHz bandwidth are connected directly to the gates, then GHz (or as great as THz) Johnson-Nyquist noise will enter the quantum dot via the capacitive coupling of the gates to the quantum dot. If nothing is done to prevent Johnson-Nyquist noise from entering the quantum dot, it will heat the quantum dot to temperature equivalent energies equal to or greater than the valley splitting and the qubit fidelity will be severely impacted. One approach to prevent this from happening is to use a bias tee connected to the electrostatic gate. Figure 3.3 shows a schematic of the bias tee used for one of the gates coupled to the quantum dot (there are two total gates with bias tees). The RC cutoff of this bias tee is 1 kHz, therefore signals with higher frequency than this value entering the resistive (DC) line will not be incident on the quantum dot. Signals with higher frequency than 1 kHz on the capacitive (AC) line will be incident on the quantum dot. The higher frequency signals and noise from room temperature are attenuated at the mixing chamber stage via a -20 dB attenuator (a factor of ten attenuation in voltage). This attenuator reduces noise generated at room temperature by a factor of ten and signal inputs from the arbitrary waveform generator can easily be increased by a factor of ten to allow the same magnitude to be incident on the quantum dot. The power dissipated at the attenuator sets the upper bound on the magnitude of the waveforms that can be used (less than 100 μW in this case). This power limit is also the reason a separate DC line exists to input biases of several volts, which, if attenuated at the mixing

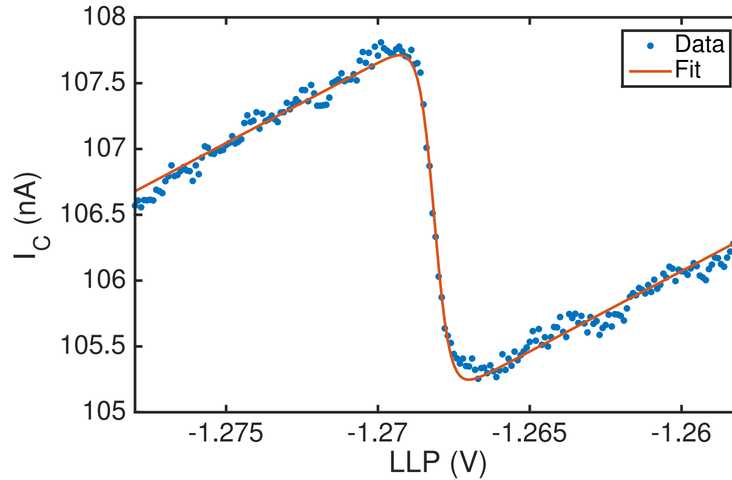

Figure 3.4: Electron Temperature Extraction
Charge-sensed quantum dot occupancy resonant transition is measured with 100 μV resolution. The fit function is also plotted, which fits well with the resulting coefficient of determination, $R^2 = 0.992$. The electron temperature extracted in this case was 163 ± 5 mK.

chamber stage, would significantly heat the dilution refrigerator.

The simplest way the electron temperature is extracted is by effectively sampling the Fermi-Dirac distribution of the electron energy occupancy at the reservoir. This is done by biasing the charge-sensor to the edge of a Coulomb blockade peak, where the current changes the most during changes in occupancy of the charge-sensed quantum dot (see Section 2.2). The quantum dot electrochemical potential is brought into resonance with the average energy of the electron reservoir. The signature of the change in quantum dot occupancy appears as a shift in the charge-sensor current, where the current changes according to a Fermi-Dirac distribution. Figure 3.4 shows data for a $\mathrm{N_e} = 1$ to $\mathrm{N_e} = 2$ transition resonance. Equation 3.3 is fit to this data with the resulting coefficient of determination, $R^2 = 0.992$. The extracted electron temperature is 163 ± 5 mK, which is consistent with other measurements of quantum dot devices performed in the same dilution refrigerator.

Another way to extract electron temperature is to perform the measurement outlined in the previous paragraph and monitor the width of the Fermi-Dirac function as a function of dilution fridge temperature as the fridge is heated. The equation used to fit this dependence is,

$$\text{width} = \frac{k_B}{\alpha_{\text{gate}}} \sqrt[N]{T_{MC}^N + T_e^N}, \tag{3.5}$$

where k_B is the Boltzmann constant (86.17 μeV/K), α_{gate} is the lever-arm of the electrostatic gate, T_{MC} is the measured temperature of the mixing chamber, T_e is the extracted temperature of the electrons, and N (> 2) is the exponent related to the mechanism of heating.

3.4 Magnetospectroscopy

Verifying that the quantum dot is in a regime with electron occupancy down to one electron is crucial for its operation as a qubit. Increased spacings between dot occupancy transition lines and a general trend of decreasing dot-lead tunnel rates are not sufficient evidence for the few-electron regime. One method to verify that the quantum dot is in the few-electron regime is to perform magnetospectroscopy. Magnetospectroscopy is a process where the global magnetic field magnitude is changed and the electrochemical potential to add the Nth electron is measured. The dependence of the electrochemical potential to add the Nth electron is given by,

$$\mu_N(B) = -g\mu_B B \Delta S_{\text{dot}}(N), \tag{3.6}$$

where g is the electron spin g-factor (constant which relates the magnetic moment to the spin angular momentum of the electron), μ_B is the Bohr magneton (58 μeV/T), B is the magnetic field magnitude, and $\Delta S_{\text{dot}}(N)$ is the change in the total spin of the quantum dot when adding the Nth electron. The slope of $\mu_N(B)$ is $\pm\frac{1}{2}g\mu_B$ depending on if the electron added is spin-up (+) or spin-down (−).

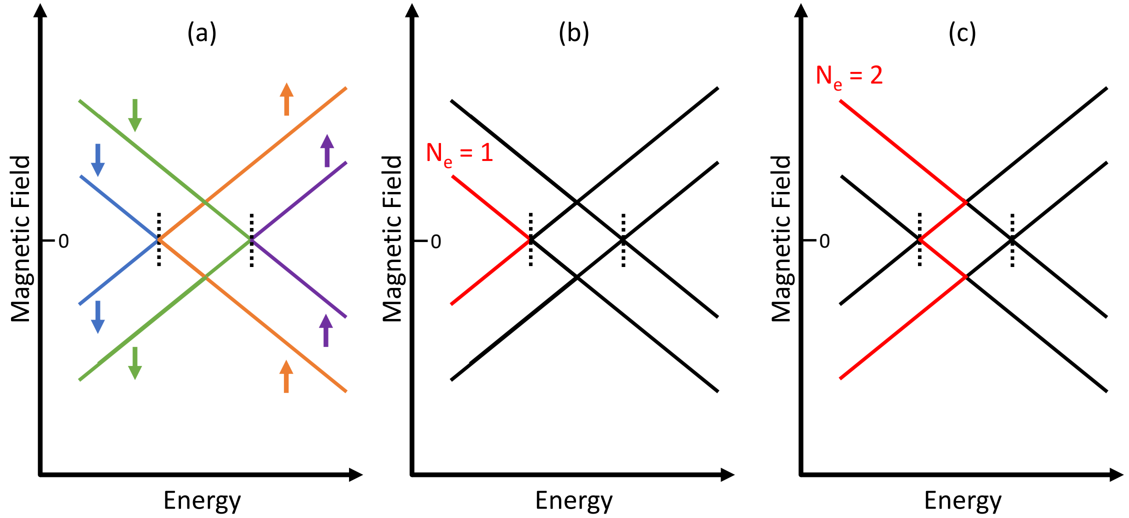

Figure 3.5: Magnetospectroscopy Model
(a) Magnetic field magnitude vs. energy for the first two valley states in silicon. All spin states are shown independently of spin filling. (b) Magnetic field magnitude vs. energy for the one-electron spin filling. (c) Magnetic field magnitude vs. energy for the two-electron spin filling.

When valley physics is added to the magnetospectroscopy model, specific signatures in the behavior of the electrochemical potential emerge. For the following details, the valley splitting energy is assumed to be much less than the orbital energy of the quantum dot. Figure 3.5(a) shows the dependence of the electrochemical potential for different spin states in the lowest two valley energy states in silicon (independent of spin filling). If a single electron is added to the quantum dot, the electrochemical potential (μ_1) will follow the behavior of a spin-down electron ($-\frac{1}{2}g\mu_B B$), which is shown in Figure 3.5(b) (red lines). When a second electron is added to the quantum dot, the electrochemical potential (μ_2) will first follow the behavior of a spin-up electron ($+\frac{1}{2}g\mu_B B$) until a degeneracy point is reached between the energy of a ground state spin-up electron (orange) and an excited state

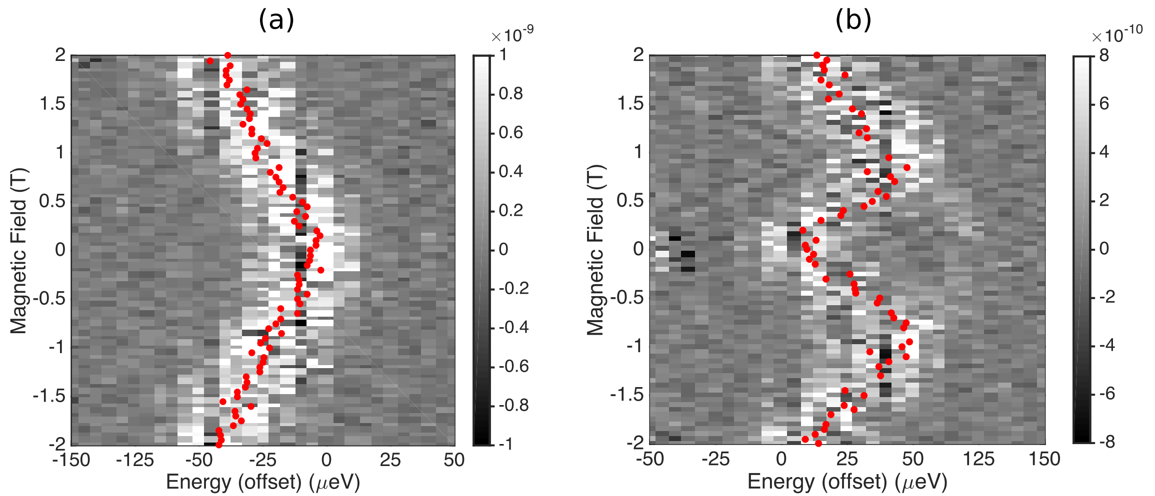

Figure 3.6: Magnetospectroscopy Data
(a) Magnetospectroscopy data for the single electron spin filling. A single slope is observed which matches the predicted behavior in Figure 3.5(b). (b) Magnetospectroscopy data for the two electron spin filling. A "kink" is observed in the data, which matches with the prediction in Figure 3.5(c).

spin-down electron (green), then μ_2 follows the behavior of a spin-down electron. It is assumed that the magnetic field magnitude and electrochemical potential will be changed slowly relative to the hybridization of the two spin states (orange and green) such that the system stays in the lowest energy.

Magnetospectroscopy measurements were performed on the quantum dot to verify the few-electron regime, confirm the magnetospectroscopy model, and assign electron occupancy values to the last two dot-lead resonant lines. Figure 3.6 shows 2D plots where the electrochemical potential of the dot is changed and the magnetic field magnitude is stepped for different electron occupancy lines. The measurements take place with the SET biased to the edge of a Coulomb blockade peak, where the SET is most sensitive to movement or changing of nearby charges. The change in electron occupancy of the quantum dot results in a shift in the electrochemical potential of the SET which manifests itself as a Fermi-Dirac function superimposed on the

edge of the SET Coulomb blockade peak (see Section 2.2 for the details of why this happens). Fitting functions to the Fermi-Dirac signature is performed exactly as outlined in Section 3.3. The centers of the fitted Fermi-Dirac functions are plotted as red dots in Figure 3.6.

The behavior of the electrochemical potential as the magnetic field magnitude is changed matches the predicted behavior shown in Figure 3.5. Particularly, for the two-electron case in Figure 3.6(b), a "kink" in the trend of the red dots is clearly visible. The kink corresponds to a point in energy halfway between the ground and excited state, therefore the energy at the kink is half the valley splitting energy. For the data shown in Figure 3.6, the valley splitting is estimated to be 105 $\pm$ 5 μeV. From the electron temperature measurement, the base temperature of the electrons in the reservoir was around 150 mK, which corresponds to an energy of around 13 μeV. Therefore, it holds that the valley splitting can be resolved energetically through the magnetospectroscopy measurements since the valley splitting energy was about eight times larger than the temperature equivalent energy. If the valley splitting energy was similar to the temperature equivalent energy, the kink would be much smaller relative to the linewidth of the Fermi-Dirac function and therefore much more difficult—or impossible—to resolve.

One important consideration for performing magnetospectroscopy measurements is the electrostatic landscape of the quantum dot. For example, if the dot-lead transition line being examined is close to a charge anti-crossing, the model outlined previously in this section may not hold. The quantum dot should be in a well-understood, single-dot regime in order for the model to be valid. Otherwise, the orbital energy may be similar to or smaller than the valley splitting energy, and the signatures may be misleading.

3.5 Tunnel Coupling Estimate

The tunnel coupling between the quantum dot and donor atom is an important parameter to measure and tune for qubit operation. Several methods for estimating the tunnel coupling exist, including fitting an equation to the zero-detuning transition line and extracting the tunnel coupling from the fit [69]. This method will not work if the energy associated with the electron temperature is greater than the energy associated with the tunnel coupling. This section covers the simplest way to estimate and tune the tunnel coupling via pulsing measurements.

For qubit operation, the tunnel coupling should be tuned to around 10 μeV. This value becomes more intuitive when converted to frequency using, $E = hf$, where E is the energy, f is the frequency, and h is the Planck constant ($4.136 \cdot 10^{-15}$ eV$\cdot$s). Using this equation, the ideal tunnel coupling value in frequency is around 2.42 GHz (414 ps). If the tunnel coupling is significantly less than 10 μeV, the qubit will not be able to perform Z rotations within the coherence time, T_2^*, which ranges from around 1 μs [22] to 120μs [41]. If the tunnel coupling is significantly greater than 10 μeV, the qubit will not be able to be reliably controlled due to instrumental limitations. The pulse generator used for the measurements has a time resolution of 1 ns. If the tunnel coupling equivalent time is on the order of 1 ns or much lower, then the pulse generator will not be able to produce pulses which rotate the qubit a reproducible number of times. Additionally, if the tunnel coupling is too great, the hybridization between the singlet (2,0) and singlet (1,1) states will cause measurement errors. This manifests itself as singlet (2,0) states becoming singlet (1,1) states, which are indistinguishable by the charge sensor from triplet (1,1) states.

A simple pulse sequence can be used to estimate the tunnel coupling. Figure 3.7 shows the energy levels of the qubit and electron reservoir for each step of the pulse sequence. First, the qubit is initialized into (1,0), where the electron occupancy

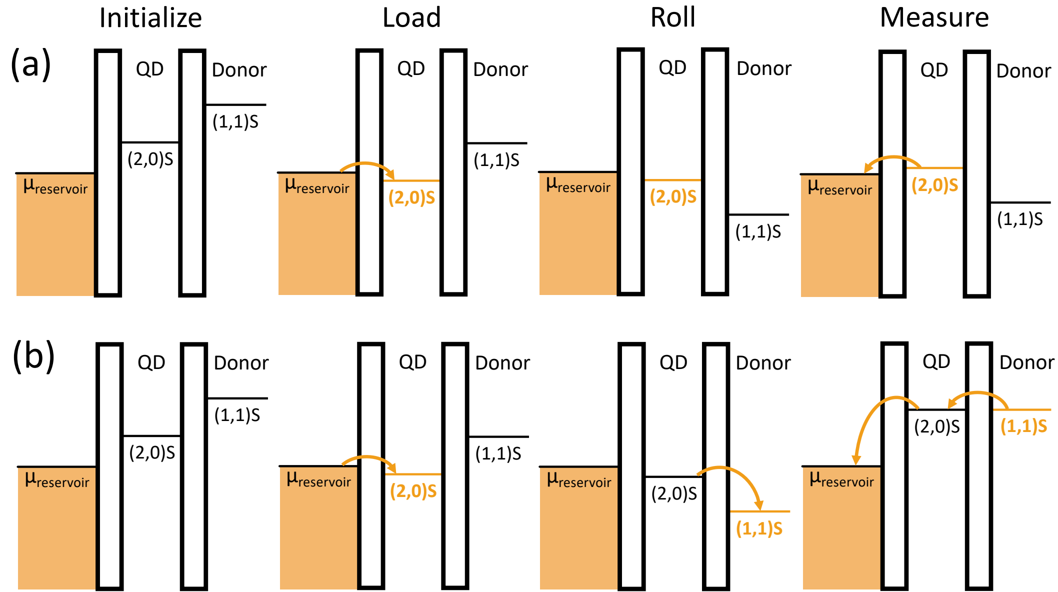

Figure 3.7: Tunnel Coupling Measurement Diagram
(a) Pulse sequence when the roll step ramp rate is fast relative to the tunnel coupling between the quantum dot and donor atom. In this case, the singlet (2,0) state does not transfer to the triplet (1,1) state. When the energy of the singlet (2,0) state is raised above the energy of the electron reservoir, an electron tunnels out of the quantum dot into the reservoir. (b) Pulse sequence for the case where the roll step ramp rate is slow relative to the tunnel coupling. Singlet (2,0) states transfer to singlet (1,1) states. Unlike the previous case, the singlet states must now be made resonant before an electron can tunnel off of the quantum dot. The roll step ramp time when this condition occurs is approximately equal to the tunnel coupling between the quantum dot and donor atom.

numbering convention is, (the number of electrons in the quantum dot, the number of electrons in the donor atom). The initialization step must have sufficient wait time in order to ensure the system is in (1,0). Next, a singlet (2,0) state is loaded during the load step, which is calibrated through the method outlined in Section 3.2. The crucial pulsing step for this measurement is the roll step. For the roll step, the time spent ramping to the roll point will determine if the singlet (2,0) state transfers to the singlet (1,1) state. This transfer rate is proportional to the tunnel coupling and will provide a reasonable estimate of the tunnel coupling. Finally, the measurement

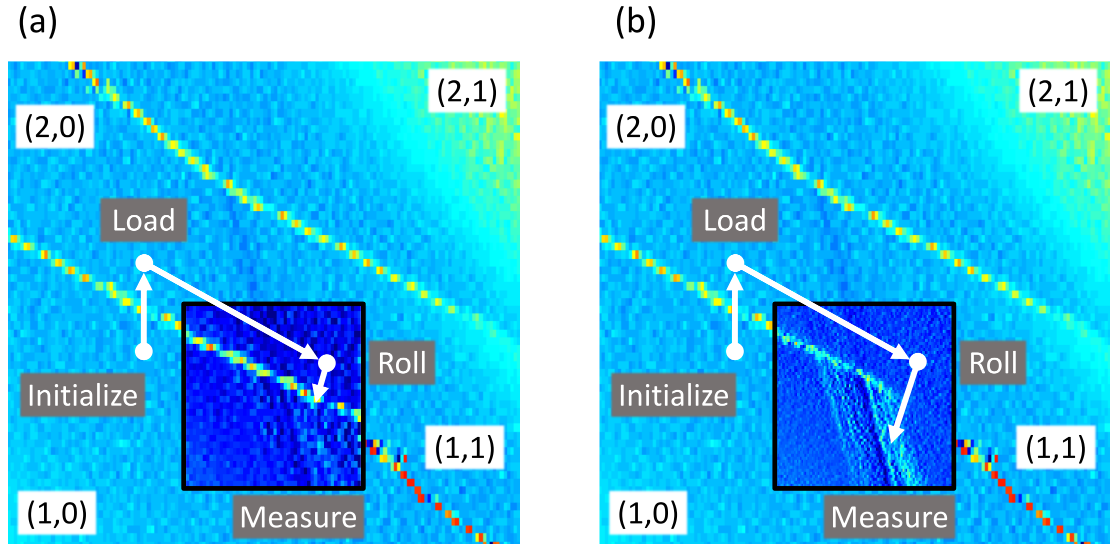

Figure 3.8: Tunnel Coupling Measurement Data
DC gate voltage values are the same as in Figure 2.13(b). (a) Fast roll ramp (200 ns). An extension of the $N_e = 2$ resonant line is visible, which corresponds to an electron transferring out of the quantum dot into the electron reservoir. In this case, the time spent moving to the roll step is much faster than the tunnel coupling between the quantum dot and donor atom. Therefore, slower times moving to the roll step are required to estimate the tunnel coupling. (b) Slow roll ramp (100 μs). An extension of the zero-detuning line is visible, which means that the singlet (1,1) state has transferred into the singlet (2,0) state and then an electron has transferred out to the electron reservoir. The time spent moving to the roll step corresponds to an approximate value for the tunnel coupling.

step is performed, which is necessary for determining if the singlet state transferred or not. The measurement point is changed according to a raster about two pulsing gate voltage ranges. Depending on whether the singlet state was transferred or not, the system will relax to (1,0) when the singlet (2,0) level is aligned with the energy of the electron reservoir (Figure 3.7(a), measure step) or when the singlet (2,0) level is aligned with the singlet (1,1) level (Figure 3.7(b), measure step).

Example data for the tunnel coupling estimate pulse sequence is shown in Figure 3.8. The background of either plot is the derivative of the DC current through

the charge sensor, which reveals the (2,0)-(1,1) anti-crossing. The darker blue inset in either plot is the derivative of the raster of the measurement step in the pulse sequence. This inset is superimposed on the DC data for the same gate voltages in either measurement. DC gate voltage values are the same as in Figure 2.13(b). The data in Figure 3.8(a) corresponds to the example in Figure 3.7(a), and the data in Figure 3.8(b) corresponds to the example in Figure 3.7(a). The difference between the two plots is that Figure 3.8(a) is using 200 ns to move to the roll step, and Figure 3.8(b) is using 100 μs to move to the roll step. In Figure 3.8(a), the extension of the $N_e = 2$ resonant line appears, which corresponds to an electron transferring out to the electron reservoir (instead of transferring to singlet (1,1)). In Figure 3.8(b), the extension of the zero-detuning line appears, which corresponds to singlet (1,1) states transferring to singlet (2,0) states and then an electron transferring out to the electron reservoir. This singlet transfer condition only occurs when the time spent moving to the roll point is 100 μs, which approximately corresponds to a tunnel coupling of 10 kHz or $4.183 \cdot 10^{-5}$ μeV.

The approximate tunnel coupling, in this case, was far off from the target tunnel coupling of 10 μeV. A nearby gate (LRP) was used to tune the tunnel coupling. Since the donor atom or defect is fixed wherever it is implanted, changing a voltage to more negative bias on the right side moves the quantum dot closer toward the donor/defect on the left side. The change in voltage, in this case, was around 100 mV. Tunnel coupling estimate pulsing measurements were performed again, and the tunnel coupling was extracted to be at least 0.021 μeV, which is much closer to the target value. Note that extracting the tunnel coupling using this method will yield an approximate value and will be limited by how rapidly the instrument can pulse from voltage to voltage. For example, if the fastest the instrument can pulse to the roll point is 4 ns, then the lower bound on the tunnel coupling will be 1.046 μeV. Therefore, this method is best used when the tunnel coupling is relatively low. If the tunnel coupling is relatively high, the method mentioned at the beginning of this

section will be a superior choice [69].

3.6 Latched Charge Readout

Performing readout is a critical final step for determining the quantum state of the qubit. The method outlined in this section uses elements from Pauli spin blockade readout [20] and latched charge readout [5].

Figure 3.9(b) shows the pulse sequence superimposed on top of DC and measurement pulsing data (DC gate voltage values are the same as in Figure 2.13(b)). The light blue data in the background is the derivative of the DC charge sensor current, and the smaller dark blue square is the derivative of the raster of the current in the measurement step. The system is initialized into (1,0) by waiting an appropriate amount of time (e.g., 40 μs in this case). Then a second electron is loaded into the quantum dot forming a singlet state, where the loading position and speed is calibrated via the method in Section 3.2. Finally, the system is pulsed into the (2,1) region and a raster of the measurement point is performed. In the dark blue measurement region in Figure 3.9(b), two distinct resonant lines appear, which correspond to the singlet/triplet (2,0) to (1,1) resonances. The typical pulse sequence for performing manipulations on the qubit and then reading out would consist of initializing and loading as before, however, pulses into the (1,1) region and then to the latched charge region would be performed. Note, in the case of the pulse sequence shown in Figure 3.9(b), the (1,1) region is avoided entirely for simplicity.

The appropriate measurement bias for latched readout is between the singlet and triplet resonant lines and above the (1,1)-(2,1) resonant line. Figure 3.9(a) shows the energy levels of the system when the measurement point is at the appropriate bias voltages. Singlet (1,1) states will transfer into singlet (2,0) states with rate, Γ_1. Triplet (1,1) states do not transfer into singlet (1,1) states due to the Pauli exclusion

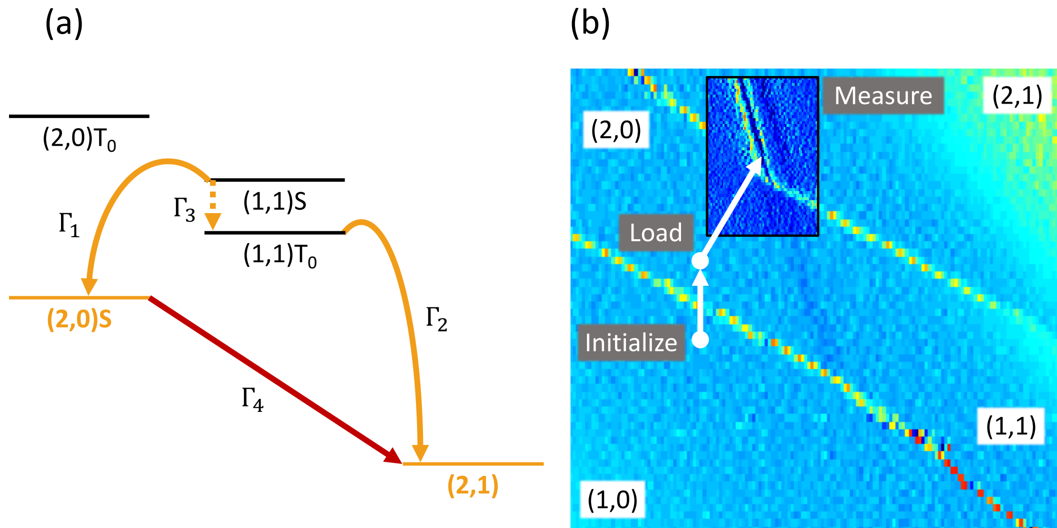

Figure 3.9: Latched Charge Readout
DC gate voltage values are the same as in Figure 2.13(b). (a) Energy level diagram during the measurement step of the pulse sequence. The energy levels correspond to the voltages at the tip of the white arrow in the measurement step in (b). Latched readout occurs in this region due to the (2,1) energy level being lowered below the other levels. The metastable lifetime of loading an electron onto the donor (Γ_4) must be relatively long for this readout scheme to work. (b) Data from readout pulsing measurements. The background of the plot is the derivative of the DC current of the charge sensor. The darker blue region is the derivative of the raster of the measurement step of the pulse sequence. White arrows depict the voltage values of the readout pulse sequence. The two resonant lines appearing in the measurement step raster are the singlet/triplet (2,0) and (1,1) resonant lines.

principle. Instead, if the system is in the triplet (1,1) state, an extra electron will be loaded into the dot moving the system into the (2,1) charge configuration with rate, Γ_2. The relaxation of singlet (1,1) states into triplet (1,1) states occurs with rate, Γ_3. In this readout scheme, singlet (2,0) states are not at the ground state energy and will decay to (2,1) with rate, Γ_4. In order for the latched charge readout to be performed with high fidelity, the state transfer rates must be much larger than the excited state decay rate,

$$\Gamma_1 \,\&\, \Gamma_2 \gg \Gamma_3, \tag{3.7}$$

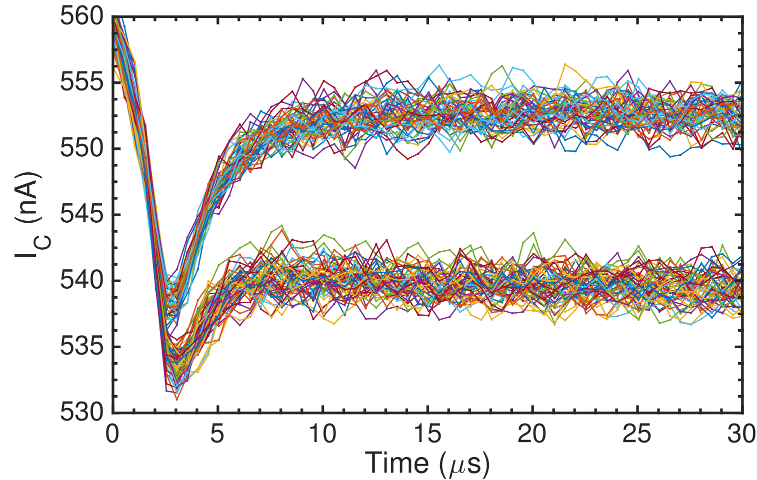

Figure 3.10: Latched Charge Readout Single-Shot
100 single-shot traces showing latched readout during the readout step of the pulse sequence. The outcomes with higher current at times greater than 10 μs correspond to singlet (2,0) states being read out. Outcomes with lower current at times greater than 10 μs correspond to (2,1) (triplet) states being read out. The metastable lifetime of the donor being loaded with an electron is greater than 10 ms in this case, therefore relaxation events are not seen in the much faster readout window.

and the total measurement time must be much shorter than the time for the singlet (2,0) states to decay to (2,1),

$$t_{meas} \ll \frac{1}{\Gamma_4}. \tag{3.8}$$

Γ_1 is proportional to the tunnel coupling of the quantum dot and donor, therefore it can be tuned according to Section 3.5 and will typically be of order 10 GHz. Γ_2 is the tunnel coupling between the quantum dot and electron reservoir when one electron occupies the donor. This rate can also be tuned similarly to how the tunnel rate is tuned in Section 3.2 and will typically be greater than 100 kHz. Γ_3 is set by properties of the system such as phonon coupling, and it is typically around 100 Hz [5]. Γ_4 is set by the hybridization between the singlet (2,0) and singlet (1,1) states, which is dependent on the tunnel coupling between the quantum dot and donor atom.

Figure 3.10 shows 100 single-shot traces from the latched charge readout performed. The time plotted begins at the readout step of the pulse sequence. The readout was performed using the CB-HBT amplification circuit, which is covered in Chapters 5 and 6. After about 3 μs, two distinct current levels are visible corresponding to singlet (2,0) states (higher current) and (2,1) (triplet) states (lower current).

Chapter 4

Single-Electron Si-MOS Devices

4.1 Preface

This chapter was originally published in Applied Physics Letters in 2019 as "Quantum dots with split enhancement gate tunnel barrier control" [70].

The contribution from this dissertation was Thomas-Fermi model simulations of the devices used in this chapter. Figure 4.1(c)&(d) and Table 4.2 show results and parameters from the Thomas-Fermi model simulations. These simulations verified the tuning orthogonality between the QD occupancy and the tunnel rate, which aids in achieving the single electron regime relatively simply.

4.2 Introduction

Silicon (Si) quantum dots (QDs) are strong contenders for the realization of spin qubits [18, 71]. Silicon germanium heterostructure (Si/SiGe) platforms with integrated micromagnets [72] have produced the highest performance qubits [73–75],

with fidelities over 99.9% [3], while metal-oxide-semiconductor (MOS) platforms have also achieved fault tolerant fidelities [41].

Most of the high-performance systems mentioned above are enhancement mode devices comprising at least two layers of control gates. The overlapping gates ensure strong confinement and the highest electrostatic control over regions surrounding the QDs. Those current multi-stack devices have therefore achieved excellent tunability, thanks in part to independent control of reservoirs, dots and tunnel barriers through respectively dedicated gates. On the other hand, single-layer enhancement mode devices are being explored for ease of fabrication and potentially higher yield, in both Si/SiGe and MOS systems [5, 22, 76–78]. In particular, all-silicon MOS single-layer devices are expected to avoid thermal mismatch and additional dielectric charge noise from overlayers [79, 80]. Those single-layer devices generally use a single gate to form a source-dot-drain channel, relying on constrictions and lateral depletion gates to shape the confinement potential [76, 81]. Reservoir filling, dot charge occupation, and tunnel rates are therefore controlled differently than in multi-gate stack architectures. Various architectures and methods of tunnel barrier control impact tunability differently, and understanding those differences will influence choices of multi-QDs initialization, manipulation and readout schemes, including automatic tuning procedures [82, 83], as well as reproducibility, versatility, and scalability of devices [84].

Here, a single gate stack structure featuring a split gate for dot and reservoir formation is explored. The tunnel barrier is simply formed by the gap between the dot and reservoir gates. In all-silicon MOS devices based on this elementary structure, an investigation is performed on how tunnel barrier control can be achieved by modulation of the reservoir gate voltage. The operation principle is studied in two variations of the layout, emphasizing some intrinsic effects brought by the use of a reservoir gate for tunnel control, in contrast with the more frequent method

of control using a dedicated barrier gate directly on top of the barrier. Then, a control orthogonality metric is defined with significance for tunability and versatility of quantum dot devices and it is used to compare a split gate QD device to a multi-stack device from the literature. Finally, this work concludes with an examination of single-electron regime characteristics and valley splitting tuning in the split gate devices.

4.3 Split Enhancement Gate Tunnel Barrier

The elementary single-gate stack structure explored consists of a quantum dot (QD) enhancement gate, AD, and a reservoir (R) enhancement gate, AR, separated by a gap, as shown in Figure 4.1(a). This base unit of design is referred to as the "split enhancement gate" structure. Devices are fabricated using the Sandia National Laboratories MOS quantum dot process [85, 86], which is described in Section 4.5. The gate stack consists of a 10,000 Ω-cm n-type silicon float zone substrate, a 35 nm SiO_2 gate oxide and a degenerately As-doped 100 nm thick polysilicon gate (shown in Figure 4.1(a)). The polysilicon nanostructure is defined by a single electron-beam lithography and dry etching step. The gate oxide properties have been characterized in Hall bars fabricated on the same starting gate stack as the nanostructures. Peak mobility, percolation density [85, 87], scattering charge density [85, 88], interface roughness and interface correlation length [89] were extracted for the wafers used for each of the devices and are indicated in Table 4.1 of Section 4.6.

In this study, there are two different layouts of split enhancement gate devices: 1), a single-lead layout (devices A1 and A2), where a single reservoir is connected to a dot; and 2), a double-lead layout (device B), where the dot is connected in series to reservoirs to enable transport measurements, in addition to charge sensing. Devices A1 and A2 present the same layout, with only differences in scale and spac-

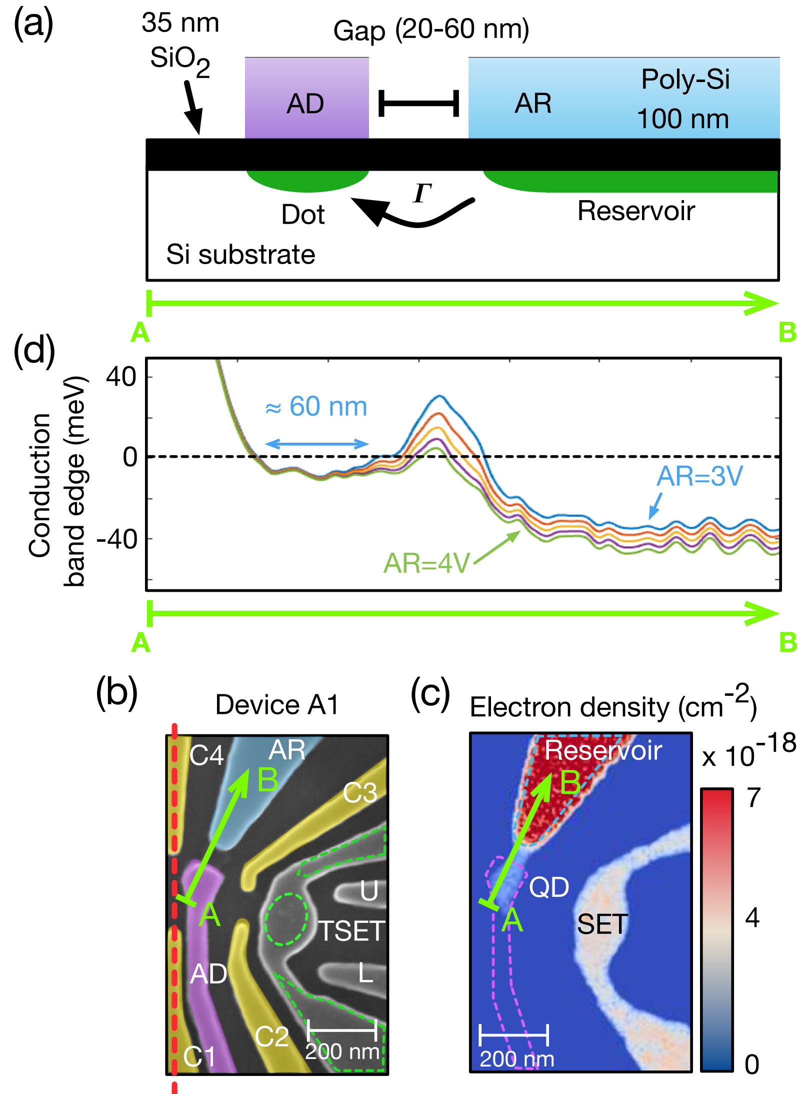

Figure 4.1: Single-Lead Device Schematic and Model
(a) A schematic transverse cut of the split enhancement gate tunnel barrier devices. AR is the reservoir enhancement gate, and AD is the dot enhancement gate. (b) False-color scanning electron micrograph (SEM) of single-lead split-enhancement gate device A1. C1, C2, C3, and C4 are confinement gates. The gate TSET forms the SET channel, and U and L help define its source and drain barriers. A mirror structure, on the left side of the dotted red line, not shown for clarity, includes gates AD′, AR′, C2′, C3′, TSET′, U′, and L′. (c) Simulated electron density, representing approximately 20 electrons in the dot. (d) Simulated conduction band edge profile (smoothed traces) along the green arrow A-B from (a), (b), (c) and (d), for V_{AR} varying from 3 to 4 V with 0.25 V increments, with other parameters kept constant.

ing. (see Table 4.1 in Section 4.6). For all devices, measurements are performed using a proximal SET as a charge sensor with standard lock-in or RF reflectometry techniques[90]. Details on the measurements and a list of all voltages employed are given in Section 4.6.

To illustrate the split enhancement gate tunnel barrier structure and its operation, Thomas-Fermi numerical simulations have been performed [91] of device A1, as shown in Figure 4.1(b), using the corresponding MOS structure and operating gate voltages as input parameters. Figure 4.1(c) shows the simulated electron density at the Si/SiO_2 interface when the device is experimentally set in a ~ 20 electrons regime. As expected, a reservoir is formed under AR gate, and a quantum dot under the tip of AD gate, separated by the tunnel barrier region. Some form of tunnel barrier control using the reservoir gate voltage, V_{AR}, is suggested by variations of the potential along the dot-reservoir axis (Figure 4.1(d)). Indeed, as a function of V_{AR}, the tunnel barrier potential height and width are modified, while the QD conduction band edge stays fairly constant relative to the Fermi level of the reservoir, indicating some form of tuning orthogonality between charge occupation of the QD and tunnel rate to the reservoir (similar quantities are evoked in [84]). Sufficient tuning orthogonality would allow simultaneously for a wide range of tunnel rate Γ and the ability to regularly tune these devices to the single electron regime. Therefore, this characteristic is investigated for a QD based on a split enhancement gate structure employing the reservoir gate as a knob [92].

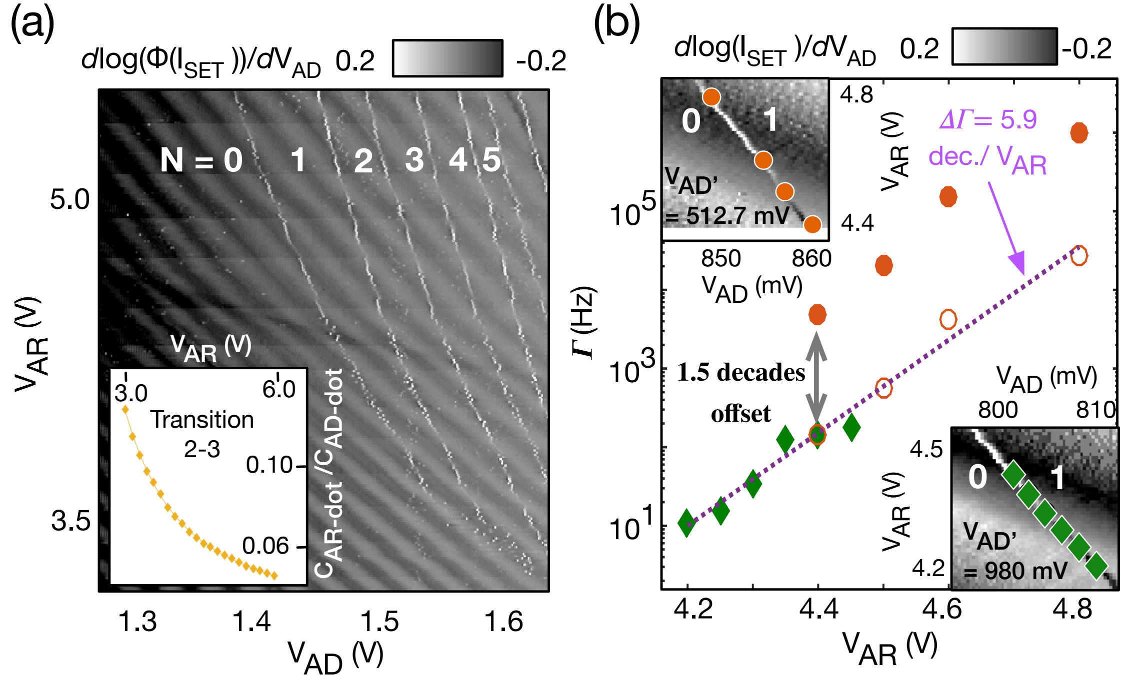

Figure 4.2: Single-Lead Device Stability Diagram and Tunnel Rates
(a) Stability diagram of AD vs AR in the few-electron regime for the single-lead device A2 (split enhancement gate device). The data was processed through a 5th order Butterworth digital filter and a Hilbert transform to extract the phase ϕ(SET) of the signal and minimize the appearance of the background's SET's Coulomb oscillations (darker, more horizontal features). Charge occupation N in the dot is indicated for each region between the transitions (thin white and more vertical features). Bottom left inset: capacitance ratio $C_{\text{AR-dot}}/C_{\text{AD-dot}}$ as a function of V_{AR} extracted from the $N = 2 \rightarrow 3$ charge transition's slope. (b) Reservoir-dot tunnel rate as a function of V_{AR} for the $N = 0 \rightarrow 1$ transition in device A1. The green (diamonds) data points are obtained via full counting statistics of single-shot traces [93] while the orange (circles) data points are extracted from pulse spectroscopy [19]. Hollow orange circles are the orange filled circle data points translated by ~ 1.5 decades. The dotted line is an exponential fit to green and hollow orange data points, yielding a slope $\Delta\Gamma$. Top left inset: zoom on the region of the stability diagram corresponding to the orange data points, with the left dot accumulation gate AD′ at 512.7 mV. Bottom right inset: Zoom on the region of the stability diagram corresponding to the green data points, with $V_{\text{AD}}{}' = 980$ mV.

4.4 Single-Electron Regime and Tuning Orthogonality

Figure 4.2(a) shows how the QD occupancy can be tuned down to the single electron regime in device A2 (Figure 4.2(b)). The single electron occupation was confirmed with spin filling from magnetospectroscopy and yields an 8 meV charging energy for the last electron. The effect of V_{AR} on the tunnel rate is qualitatively visible from the charge transitions, which go from a “smooth” appearance at high V_{AR}, when Γ is high compared to the measurement rate, to a speckled appearance at low V_{AR}, when Γ is of the order of the measurement rate or lower [94].

A gradual decrease of the AR gate capacitance to the dot, $C_{\text{AR-dot}}$, is observed as the reservoir fills up with electrons, as shown in the inset of Figure 4.2(a) (assuming $C_{\text{AD-dot}}$, the capacitance of the AD gate to the dot, stays constant). The capacitance ratio $C_{\text{AR-dot}}/C_{\text{AD-dot}} = -1/m$ is extracted from the slope m of the transition $N = 2 \rightarrow 3$ in the stability diagram [95]. A similar dependence of the capacitance ratio is also observed in numerical simulations, but the agreement is only qualitative, due in part to the limitations of the semi-classical simulation. This visible curvature in the dot transitions is attributed to a screening effect of the reservoir gate potential, induced by the accumulated charges in the reservoir. This specific effect, therefore, seems to be caused by the use as a tuning knob of an enhancement gate connected to an ohmic contact.

Device A1 also exhibits a comparable behavior as a function of AR and AD gates (see Section 4.6). The dot-reservoir tunnel rate is measured as a function of AR voltage for device A1, along the $N = 0 \rightarrow 1$ charge transition, as V_{AR} is compensated with V_{AD} to preserve the charge state, Figure 4.2(b). Two data sets (diamond and filled circles) were taken at different voltages on a surrounding gate, $V_{AD'}$. The 467 mV difference results in a 1.5 decade global offset in tunnel rates.

This offset (hollow circles) is subtracted to extract a single exponential dependence of Γ with V_{AR} [96, 97].

From the slope of the exponential fit, a gate response of $\Delta\Gamma = 5.9 \pm 0.7$ dec./V_{AR} is extracted. This response is defined as the variation in dot-reservoir tunnel rate induced by a change of 1 V on gate AR when compensated by gate AD to keep the dot chemical potential fixed. It is more useful for comparison between devices when the device geometry specific capacitance is removed by converting to change in chemical potential, $\Delta\mu_{dot}$. The following metric is defined:

$$\beta_{AR,AD} = \Delta\Gamma_{AR,AD}/\Delta\mu_{dot}, \tag{4.1}$$

where $\Delta\Gamma_{AR,AD}$ is the change in tunnel rate induced by the change in voltage on AR (and compensated by AD), $\Delta\mu_{dot}$ is the change in chemical potential caused by gate AR (equal to the chemical potential compensated by gate AD), and $\beta_{AR,AD}$ is defined as the "tuning orthogonality." For device A1, the above analysis leads to $\beta_{AR,AD} = 0.9 \pm 0.3$ decade/meV, using the gate lever arm $\alpha_{AR} \sim 0.007$ meV/mV (from $\alpha_{AD} \sim 0.22$ meV/mV). Note that the chemical potential of the QD does not actually shift for a given tunnel rate variation here since there is a second gate compensating the chemical potential shift from the first. Therefore, care must be taken in interpreting this ratio: it does not represent the effect of a single gate on the tunnel rate, but rather the interplay of two gates acting in opposite direction on the two quantities, with unequal contributions.

Taken individually, more positive voltages on gates AD and AR would both tend to decrease the barrier height and width, as one would expect and as shown in the conduction band edge simulations of Figure 4.1(d). But if one wants to keep the dot occupation fixed, and shift from high to low tunnel rates, gates AD and AR have to be swept in the opposite direction. The measurements indicate that in this case the lever of gate AR on the tunnel barrier still overcomes the opposite effect of gate AD. Furthermore, the screening effect from charges under AR is speculated to contribute

to this efficiency, as it reduces the lever of gate AR on the dot occupation, but on the tunnel barrier, such that less compensation on AD is necessary to maintain charge occupation than if no screening effect was present.

The quantity $\beta_{1,2}$ can be estimated for other designs in the literature, for any pair of gates 1 and 2 used to tune the tunnel rate and compensate for a change in the dot occupation, respectively. For comparison, it is estimated that $\beta_{BG,AD} = 1.4 \pm 0.5$ decades/meV for the case of a dedicated barrier gate BG compensated by the dot accumulation gate AD equivalent in a Si/SiGe device [98]. This indicates a tuning orthogonality that can reach the same order of magnitude as dedicated barrier gate devices in multi-stack architectures. Single-layer split enhancement gate layouts could, therefore, provide a wide operation range [48] for single-electron QD devices. Details on the calculations as well as assumptions leading to the metric β and its limitations are provided in Section 4.7.

The double-lead layout also supports transport down to the last electron and exhibits a typical split enhancement gate behavior. Figure 4.3(a) shows device B, where transport is through a QD under gate AD with source and drain reservoirs under gates AR_1 and AR_2. A mirrored structure can be operated as an SET charge sensor, correlating the transport transitions (Figure 4.3(b)) with charge sensed measurements (Figure 4.3(c)).

In Figure 4.3(b), the tunnel rate ranges from the lifetime broadened regime at high V_{AR}, corresponding to a $\sim$ 3 GHz tunnel rate [98, 100] to slower than can be detected by the charge sensor, $\sim$ 8 Hz. The slight curvature in the dot and SET transitions of Figure 4.3(d) is ascribed to a similar screening effect as in the single lead devices, although it is not as pronounced. This demonstrates that two neighboring barriers in series can be tuned relatively orthogonally (i.e., crosstalk is not a prohibitive issue), and that the split enhancement gate concept can be applied in several layouts.

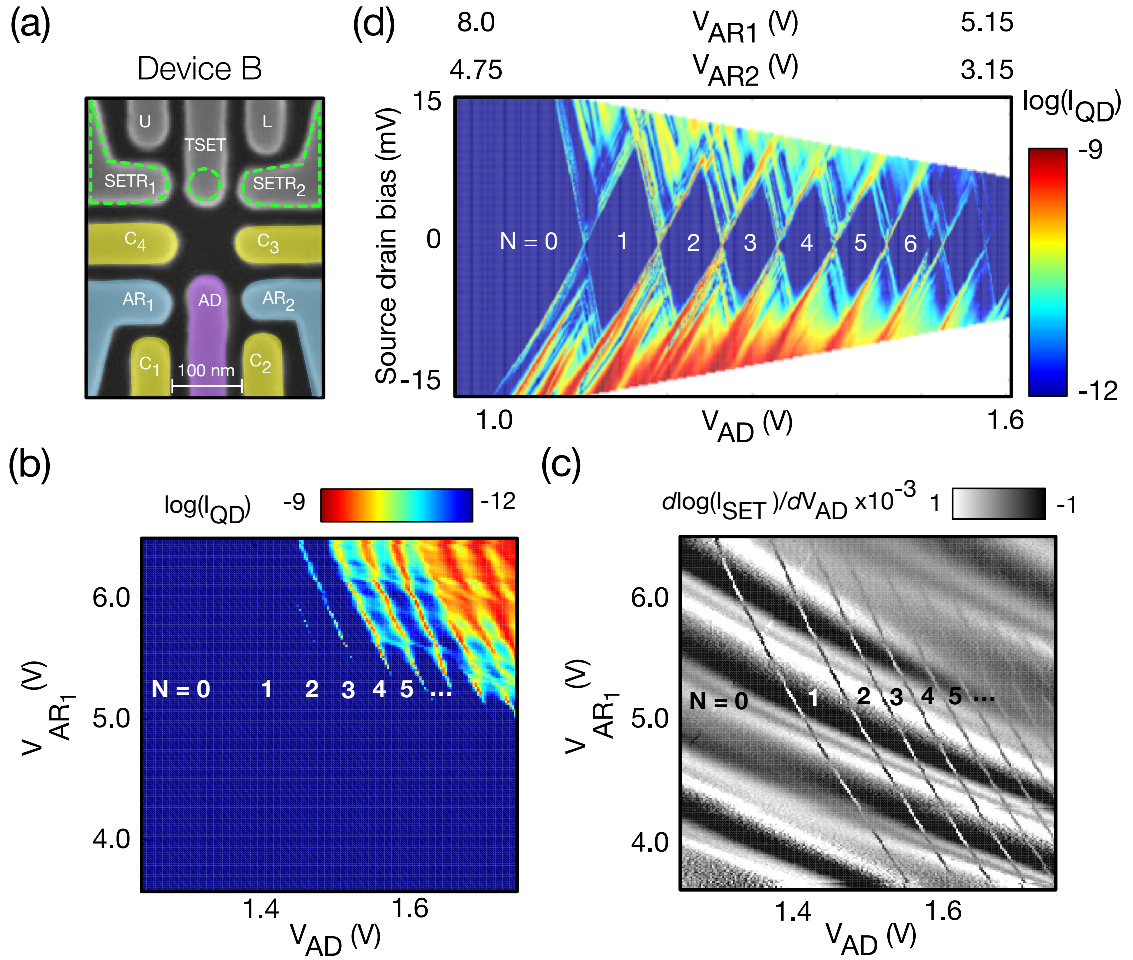

Figure 4.3: Double-Lead Device Schematic and Occupancy Measurements
(a) SEM of a double-lead single quantum dot device, device B. C1, C2, C3, and C4 are confinement gates, AD is the dot accumulation gate, and AR_1 and AR_2 are the source and drain reservoirs accumulation gates, respectively. A mirror structure above is operated as an SET for charge sensing. (b) Stability diagram of transport for AD vs AR_1. (c) Stability diagram of charge sensing corresponding to the transport diagram in (b). (d) Coulomb diamond measurement corresponding to a stability diagram of AD vs AR_1 and AR_2. The small diamond after electron #6 is due to a donor ionization [99] (see fabrication details in Section 4.5).

In Figure 4.3(d), V_{AR_1} and V_{AR_2} are adjusted simultaneously to symmetrize the tunnel barriers on the source and drain side of the QD, giving rise to Coulomb diamonds [101], with the last electron charging energy of 11 meV. The notable difference in voltage ranges applied on AR_1 and AR_2 is attributed mainly to asymmetry in the voltages applied on the neighboring gates on the left and right side of the device, although small variations in the width of the dot-reservoir gap could also contribute to the difference. The precise effect of the dot-reservoir gap width on the tuning orthogonality and general efficiency remains to be studied in detail.

The addition energy of the last electron and the first orbital energy are extracted from the Coulomb diamonds of Figure 4.3(d), yielding approximately $E_{add} = 11$ meV and $\Delta E = 3$ meV, respectively. A classical capacitance between the QD and the AD gate of 2.9 aF is estimated (e.g., $C_{AD} = e/\Delta V_{AD}$ with $\Delta V_{AD} = 56$ meV the voltage applied on gate AD to go from the $N = 0 \rightarrow 1$ charge transition to the $N = 1 \rightarrow 2$ transition in Figure 4.3(b)). The classical capacitance can be associated with a circular 2D QD below the gate and is used to estimate a QD radius of $\sim$ 30 nm, using $\epsilon_r = 3.9$ for the SiO_2 and neglecting small errors due to the electron offset from the SiO_2 interface and depletion of the polysilicon. The orbital energy also provides an estimate of QD size. Following Zajac et al. [98], an effective length of a confining 2D box ($\pi r^2 = L^2$) is extracted and using $\Delta E = \frac{3\hbar^2\pi^2}{2m^* L^2}$ =3 meV, a similar dot size, $r \sim 25$ nm, is obtained using $m^* = 0.19\ m_e$. Those estimated dot size and energies are similar to the ones obtained in multi-stack accumulation mode quantum dot devices [98, 102].

Finally, an investigation of the spin filling and singlet-triplet energy splitting in the silicon QDs using magnetospectroscopy [98, 103, 104] indicates that the valley splitting is linearly tunable with the vertical electric field (8.1 ± 0.6 μeVm/MV in the double-lead device) and is tunable over a range of $\sim$ 75-250 μeV (see Section 4.8 for details).

4.5 Sample Fabrication

The fabrication is composed of two phases. The first phase is run in a 0.35 micron CMOS silicon foundry, and the second phase is performed in another fabrication area that provides more flexibility in processing, particularly the e-beam lithography used for the nanofabrication. Three different devices are presented in this work. The process flow for devices A1 and A2 is described. Significant differences in the structure are noted for device B.

Phase 1 (silicon foundry): The initial material stack is fabricated using a 0.35 micron silicon foundry process at Sandia National Laboratories. The starting material is a 150 mm diameter float zone <100> n-type silicon wafer with a room temperature resistivity of 10,000 Ω-cm. Device B used a p-type float zone substrate with a 99.95% Si^{28} enriched epitaxy layer instead. A 35 nm thermal silicon oxide is grown at 900°C with dichloroethene (DCE) followed by a 30 min, 900°C N_2 anneal. The next layer deposited is a 100 nm amorphous silicon layer followed by a 5×10^{15}cm^{-2}, 10 keV arsenic implant at 0° tilt. Device B used a 200 nm layer and the implant energy was 35 keV with the same dose. The amorphous layers are crystallized later in the process flow to form a degenerately doped poly-silicon electrode. In the silicon foundry, the poly-Si is patterned and etched into large scale region, a "construction zone" around 100 μm × 100 μm in size, that will later be patterned using e-beam lithography to form the nanostructure.

After etching, ohmic implants are formed using optical lithography and implantation of As at 3×10^{15}cm^{-2} density at 100 keV. An oxidation anneal of 900°C for 13 min and an N_2 soak at 900°C for 30 min follows the implant step and serves the multiple purposes of crystallizing, activating and uniformly diffusing the dopants in the poly-Si while also forming a SiO_2 layer (10–25 nm) on the surface of the poly-Si. This SiO_2 layer forms the first part of the hard mask layer used for the nanostructure

etch in the construction zone. The second part of the hard mask is a 20 nm Si_3N_4 layer (35 nm for device B). An 800 nm thick field oxide is subsequently deposited using low-pressure chemical vapor deposition (CVD), tetraethoxysilane (TEOS) or high-density plasma CVD for device B. The field oxide is planarized using chemical mechanical polishing (CMP) leaving approximately 500 nm over the silicon and 300 nm over the poly-Si. Vias are etched to the conducting poly-Si and n^+ ohmics at the silicon surface. The vias are filled with Ti/TiN/W/TiN. The tungsten is a high contrast alignment marker for subsequent e-beam lithography steps. Large, approximately 100 μm $\times$ 100 μm windows aligned to the construction zones are then etched in the field oxide to expose the underlying hard mask and poly-Si construction zone for nanostructure patterning. The last processing step for the devices in the silicon foundry is a 450°C forming gas anneal for 90 min.

Phase 2 (separate nano-micro fabrication facility): The wafers are removed from the silicon foundry and subsequently diced into smaller parts, leading to 10 mm $\times$ 11 mm dies, containing each 4 complete QD devices. The nanostructure is patterned using electron beam lithography and a thinned ZEP resist. The pattern is transferred with a two-step etch process. First, the SiN and SiO_2 hard mask layers are etched with a CF_4 dry etch, and O_2 cleans then strips the resist *in-situ*. The second etch step is to form the poly-Si electrodes, which is done with an HBr dry etch in the same chamber. The poly-Si etch is monitored using end-point detection in a large scale etch feature away from the active regions of the device. Wet acetone and dry O_2 cleans are used to strip the residual resist after the poly-silicon nanostructure formation. After the wet strips off the tungsten vias, a lift-off process is used for aluminum formation of bond pads to contact the ohmics and poly-silicon electrodes.

The last step is a 400°C, 30 minute forming gas anneal. For device B, after the polysilicon etch, a second e-beam lithography and implant step was done to place donors near the QD region. The device was sent out for implantation, 4×10^{11}cm^{-2}

Phosphorus at 45 keV. After the implant step, the photoresist was stripped with acetone and then the metal and residual organics were stripped from the surface using peroxide and RCA cleans. The device was subsequently metalized using an Al lift-off process similar to devices A1 and A2.

4.6 Devices and Experimental Parameters

Experiments are performed in two distinct laboratories, Université de Sherbrooke (devices A1 and A2) and Sandia National Laboratories (device B), in dilution refrigerators sustaining an electronic temperature of 125 mK and 160 mK, respectively. In the limited testing of standard measurements, the samples are found to be robust to thermal cycles (i.e., little threshold shift) and no devices were visually altered by the long-distance shipping (e.g., damage from electrostatic discharge was not observed). The devices are also electrically stable, with the drift of the quantum dot chemical potential in device B characterized as approximately 5.3 $\pm$ 0.5 μeV standard deviation over a 150 hour period.

Table 4.1 compares the characteristic of devices A1, A2, and B. Table 4.2 exposes the experimental parameters for all measurements shown or mentioned in the main text for devices A1 and A2 (single-lead devices), while Table 4.3 does the same for device B.

A statement concerning device A1 is helpful for full comprehension. The full range AD vs AR stability diagram for device A1 is not shown in the main text for the sake of clarity. Indeed, features not related to the split enhancement gate operation principles, and attributed to an irregularly shaped confinement potential under gate AD, were presents in the full-range stability diagrams of device A1 (see Figure 4.4(b). This effect could be mitigated, but only up to a certain point, by applying more negative voltages on gates C1 and C2. The stability diagram of device A2, however,

Device	**A1**	**A2**	**B**
Reservoirs	Single Lead	Single Lead	Double Lead
Device Dimensions	AD-C2: 60 nm, AD-AR: 100 nm, AD width: 100 nm	AD-C2: 25 nm, AD-AR: 30 nm, AD width: 75 nm	AD-C2: 30 nm, AD-AR: 20 nm, AD width: 50 nm
Mobility	4560 $cm^2/V/s$	4560 $cm^2/V/s$	11600 $cm^2/V/s$
Interface Roughness	2.4 Å	2.4 Å	1.8 Å
Percolation Density	$6.0 \times 10^{11} cm^{-2}$	$6.0 \times 10^{11} cm^{-2}$	$1.6 \times 10^{11} cm^{-2}$
Scattering Charge Density	$7.6 \times 10^{10} cm^{-2}$	$7.6 \times 10^{10} cm^{-2}$	$5.2 \times 10^{10} cm^{-2}$
Interface Correlation Length	26 Å	26 Å	22 Å
Wafer Type	10 000 Ω-cm, n	10 000 Ω-cm, n	10 000 Ω-cm, p*
Polysilicon Gate Stack Thickness	100 nm	100 nm	200 nm
Silicon Gate Oxide Thickness	35 nm	35 nm	35 nm

Table 4.1: Measured Device Characteristics
Devices A1 and A2 present the same layout, differing only in the spacing between the gates and the width of the gates (A2 gates are more closely packed than A1 gates). For comparison, the devices are labeled by the distance between gates AD and C2, and the distance between AD and AR tips (see Figure 4.1(b)).
*Device B contains a 99.95% Si^{28} enriched epitaxy layer.

Data	**Figure 4.1d**	**Figure 4.2a**	**Figure 4.2b, Top Inset**	**Figure 4.2b, Bottom Inset**	**Figure 4.4b**
Device	A1	A2	A1	A1	A2
AD	1.75 V	1.25 to 1.65 V	0.840 to 0.870 V	0.790 to 0.820 V	1.25 to 1.40 V
AR	3.0 to 6.0 V	3.0 to 6.0 V	4.4 to 4.9 V	4.2 to 4.5 V	6.5 V
C1	-1.0 V	-3.0 V	-1.0 V	-1.0 V	-1.0 V
C2	-3.0 V	-1.4 V	-3.0 V	-3.0 V	-3.0 V
C3	-1.0 V	-1.4 V	-1.0 V	-1.0 V	-1.0 V
C4	-1.0 V	-1.0 V	-1.0 V	-1.0 V	-1.0 V
TSET	2.59 V	2.0 V	2.45V	2.59 V	2.0 V
U	-1.32V	-1.4 V	-3.19 V	-2.32V	-1.4 V
L	-2.06 V	-1.4 V	-1.75V	-2.06V	-1.4V
AD’	0.980V	0V	0.5127 V	0.980 V	0V
AR’	7.0 V	0 V	7.0 V	7.0 V	0V
C2’	-3.0 V	0 V	-1.0 V	-1.0 V	0 V
C3’	-1.0 V	0 V	-1.0 V	-1.0 V	0 V
TSET’	0 V	0 V	0 V	0 V	0 V
U’	0V	0 V	0 V	0 V	0 V
L’	0 V	0 V	0 V	0 V	0 V
Details	Thomas-Fermi numerical simulations.	Charge sensing, $f_{\mathrm{LI}} = 16.4$ Hz (lock-in frequency), $\mathrm{V_{SD}} = 100\ \mu$V (source-drain voltage).	Pulse spectroscopy, measured by charge sensing, $f_{\mathrm{LI}} = 19$ Hz, $\mathrm{V_{SD}} = 100\ \mu$V.	Single-shot measured by RF reflectometry, carrier wave $f = 180$ MHz, bandwidth of 326 kHz.	Charge sensing, $f_{\mathrm{LI}} = 16.4$ Hz, $\mathrm{V_{SD}} = 100\ \mu$V.

Table 4.2: Single-Lead Device Experimental Parameters
Experimental parameters for various data sets of the main text, for devices A1 and A2.

Data	**Figure 4.3b and 4.3c**	**Figure 4.3d**	**Figure 4.4a**	**Figure 4.4b**
Device	B	B	B	B
AD	1.2 to 1.8 V	0.9 to 1.6 V	1.8 V	1.21 to 1.8 V
AR1	3.0 to 7.0 V	5.15 to 8.0 V	5.0 V	5.0 V
AR2	3.5 V	3.15 to 4.75 V	3.0 V	3 to 3.1 V
C1	-2.7 V	-1.5 V	-6.7 to -5.3 V	-6.7 to -0.76 V
C2	-4.0 V	-3.0 V	-3.0 V	-3.0 V
C3	-0.26 V	0 V	-0.26 V	-0.26 V
C4	-4.2 V	-4.2 V	-4.2 V	-4.2 V
TSET	2.61 V	0 V	2.53 V	2.53 V
SETR1	2.5 V	0 V	2.5 V	2.5 V
SETR2	2.5 V	0 V	2.5 V	2.5 V
U	-1.5 V	0 V	-4.8 V	-4.8 V
L	-4.8V	0V	-0.92V	-0.92 to -1.26 V

Table 4.3: Double-Lead Device Experimental Parameters
Experimental parameters for various data sets of the main text, for device B. All measurements are made with a Lock-In frequency of 492.6 Hz and a source-drain bias of 50 μV_{RMS}.

is much cleaner owing to its smaller features compared to A1, but experimental setup constraints at that time prevented repeating the tunnel rate measurements on device A2, hence the reliance on qualitative analysis only for this device. It is emphasized that with the appropriate confinement, both devices qualitatively exhibit the same tunnel rate modulation and bending of the charge transitions, which, as stated in the main text, is believed to be intrinsic to the split enhancement gate tunnel barrier.

Figure 4.4(b) illustrates the effect of insufficient and irregular confinement of the dot in device A1. Figures 4.4(c)–(f) show how the smaller features of device A2, combined to an increasingly more negative voltage on gate C1, lead to more regular dot transitions, and the clean diagram shown in Figure 4.2 (a) of the main text. This observation is in agreement with the clean and regular transitions witnessed for device B (Figure 4.3(d)), which possesses even smaller features than device A2 (see Table 4.1).

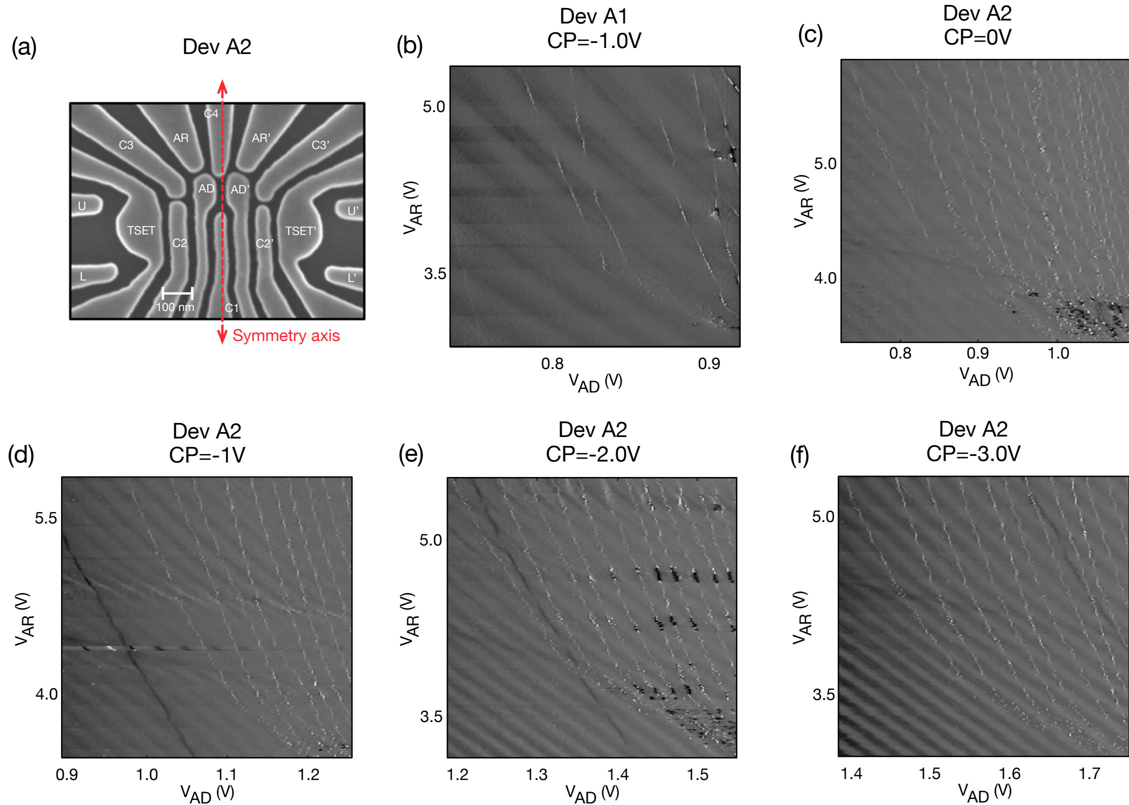

Figure 4.4: Single-Lead Device Single-Electron Stability Diagrams
(a) SEM of single-lead device A2. The device has a symmetry axis between the two quantum dots. Experiments on device A2 involved the formation of a single quantum dot, on the left side of the device only (under AD). (b) Wide range stability diagram for device A1 corresponding to the bottom right inset of Figure 4.2(a) in the main text. The pale charge transitions on the left-hand side are transitions in the left QD, which was activated for this measurement series. The large features of device A1 and the small negative voltage on C1 are responsible for the irregularities in the right dot transitions (right-hand side). (c), (d), (e), (f) Stability diagrams for device A2, with all parameters kept the same except for C1 gate voltage. A more negative voltage on C1 leads to more regular quantum dots, as expected.

4.7 Tuning Orthogonality

When designing a QD device, it is of interest to provide local control of important device properties, with the surface gate voltages often serving as the control knobs. One often used parameter is the gate lever arm α, which describes the efficacy of a gate voltage on the QD chemical potential level μ. The lever arm is defined as

$$\Delta\mu_i = \alpha_i \Delta V_i, \tag{4.2}$$

where there is a unique α_i for each gate i. In a similar spirit, a parameter describing the controllability of the QD-reservoir tunnel rate can be defined as

$$\Delta\Gamma_i = \beta_i' \Delta V_i. \tag{4.3}$$

While α is always positive by definition, β' can be positive or negative, depending on if gate i increases or decreases the reservoir-QD tunnel rate with a positive voltage change. For example, for a QD under gate AD, gate AR increases the tunnel rate with increasing voltage, while gate AD′ decreases the tunnel rate with increasing voltage (Figure 4.2(b)). Geometric arguments can typically be made to estimate the sign of β' by considering whether a positive voltage change on a gate is pulling the dot towards or away from the reservoir.

Of particular interest for designing QDs is the ability to tune the tunnel rates to the QD while only imparting a minimal change in the QD chemical potential, which denotes a high degree of tuning orthogonality between the two properties. Good orthogonality facilitates emptying the QD (fewer gate compensations are required to obtain $N = 1$) and tuning the reservoir coupling with minimal effect on the shift in the charge stability diagram (quicker optimization of relaxation and coherence times). For a single gate, the orthogonality between the tunnel rate and the chemical potential tunability is optimized by maximizing the ratio $\frac{\Delta\Gamma_i}{\Delta\mu_i} = \frac{\beta_i'}{\alpha_i} \equiv \beta_i$. This can be rewritten in an analogous form to the lever arm:

$$\Delta\Gamma_i = \beta_i \Delta\mu_i. \tag{4.4}$$

To obtain β_i, one must measure the change in both tunnel rate and chemical potential for a change on the gate voltage ΔV_i. In practice, this is impossible because a change in a single voltage moves the QD level out of resonance with the Fermi level, and a change in tunnel rate cannot be determined. Thus, one must consider the effect of two gate voltages changing and compensating each other such that the QD chemical potential is always in resonance with the Fermi level. Continuing the analogy with the lever arm, it is assumed that the total change in tunnel rate is simply the sum of the contributions of each gate that has changed. For two gates 1 and 2, this results in

$$\Delta\Gamma_{1,2} = \Delta\Gamma_1 + \Delta\Gamma_2 = \beta_1\alpha_1\Delta V_1 + \beta_2\alpha_2\Delta V_2. \tag{4.5}$$

As the chemical potential has not changed, there is an additional constraint

$$\Delta\mu_{1,2} = \Delta\mu_1 + \Delta\mu_2 = \alpha_1\Delta V_1 + \alpha_2\Delta V_2 = 0. \tag{4.6}$$

Combining Equation 4.5 and Equation 4.6, the two-gate tunnel rate orthogonality parameter is defined as

$$\beta_{1,2} \equiv \beta_1 - \beta_2 = \frac{\Delta\Gamma_{1,2}}{\Delta\mu_1}, \tag{4.7}$$

which is directly attainable from the measurements in Figure 4.2(b). From the data, a slope of $\frac{\Delta\Gamma_{AR,AD}}{\Delta V_{AR}} = 5.9 \pm 0.7$ decades/$\mathrm{V_{AR}}$ is extracted, which describes the change in tunnel rate induced by a change in both $\mathrm{V_{AR}}$ and $\mathrm{V_{AD}}$. With a lever arm $\alpha_{AR} \sim 0.007$ eV/V, it is determined that $\beta_{AR,AD} = 0.9 \pm 0.3$ decades/meV.

For comparison, $\beta_{1,2}$ is extracted for a multilayer enhancement mode Si/SiGe device which uses a dedicated barrier gate located directly on top of the tunnel barrier, sandwiched between the reservoir and QD gates (Zajac *et al.* [98]). Information on the tunnel rates is determined from the stability diagram of the tunnel barrier gate LB1 and the QD gate L1 (Figure 2a of Zajac *et al.* [98]). To more easily compare this data to the device in this work, the gates are relabelled LB1→BG and L1→AD. The

voltage ranges studied show transition rates ranging from the measurement sample rate (assumed to be at least 10 Hz) to the lifetime broadened regime ($\frac{k_B T_e}{h} = 800$ MHz for a reported electron temperature of $T_e = 40$ mK). This provides two coordinates $(\Gamma, \mathrm{V_{BG}})$ to estimate the tunnel rate orthogonality, where it is found that $\Delta\Gamma_{BG,AD} = \frac{7.9\text{decades}}{0.4\mathrm{V_{BG}}} = 19.8$ decades/$\mathrm{V_{BG}}$. From the reported lever arms and capacitance ratio for the QD and barrier gates, it is determined that $\alpha_{BG} = 0.022$ eV/V, and thus $\beta_{BG,AD} = 1.4 \pm 0.5$ decades/meV.

The definition of $\beta_{1,2}$ lends itself to compare other devices and geometries as well, as $\beta_{1,2}$ is independent of geometry specific information like capacitances. The concept of $\beta_{1,2}$ can also be extended to optimize QD devices for other characteristics which may be useful for qubit operation. For example, one can similarly define a parameter that describes the orthogonality between a double-QD coupling and the double-QD detuning, or a double-QD coupling and the valley splitting.

4.8 Valley Splitting Tuning

In this section, the spin filling and singlet-triplet energy splitting in the silicon QDs are examined using magnetospectroscopy [98, 103, 104].

The first 4 charge transitions from device B are shown as a function of the transverse magnetic field, at $\mathrm{V_{AD}}$=1.8 V, in Figure 4.5(a). The first transition shows a shift in chemical potential consistent with a lowering of energy due to increasing Zeeman splitting. The inflection point at $B = B_{ST}$ in the $N = 1 \rightarrow 2$ charge transition indicates the magnetic field at which the singlet-triplet (ST) transition occurs in the quantum dot [105, 106]. The magnetospectroscopy for the $N = 2 \rightarrow 3$ transition has an inflection at the same B-field as the $N = 1 \rightarrow 2$ transition. This is consistent with a simple model for which there are two valleys and the 2nd valley is loaded with a 3rd electron as spin-down. The inflection point again marks the crossing of the spin-up of

the lower valley with the spin-down of the upper valley. The 4th electron then loads always spin-up, also suggesting that the next orbital energy is well offset from this lower manifold, which is indeed consistent with the order of 3 meV estimate from the Coulomb diamonds. This spin filling also indicates a relatively small Coulomb repulsion relative to orbital energy spacing [107].

The magnetospectroscopy measurements are repeated for different V_{AD}, compensating with the confinement gate C1 to maintain charge occupation. The single particle valley splitting is estimated from $E_{VS} = g\mu_B B_{ST}$, assuming $g = 2$, for devices A2 and B (Figure 4.5(b)). For device B, a linear tunability of E_{VS} is extracted using the accumulation gate voltage of 231 ± 15 μeV/V, with the error range corresponding to a 95% confidence interval on the fit. Roughly approximating the vertical electric field as $\Delta F_Z = \Delta \text{V}_{\text{AD}}/t_{ox}$, where t_{ox} is the gate oxide thickness, 35 nm here, this tunability is converted to 8.1 ± 0.6 μeV m/MV. The linear trend is qualitatively consistent with theory and recent observations in MOS QDs [105, 109].

For device A2, although the measurements were too noisy to extract a convincing tunability fit, all data points are located into the confidence interval for device B's tunability. Note that differences in valley splittings between devices A2 and B would be expected from variations in electrostatic environments (e.g., gate layout and dimensions, distribution of voltages to reach single electron occupation and threshold voltages) and in interface roughness, approximately 20% different between the two samples [109].

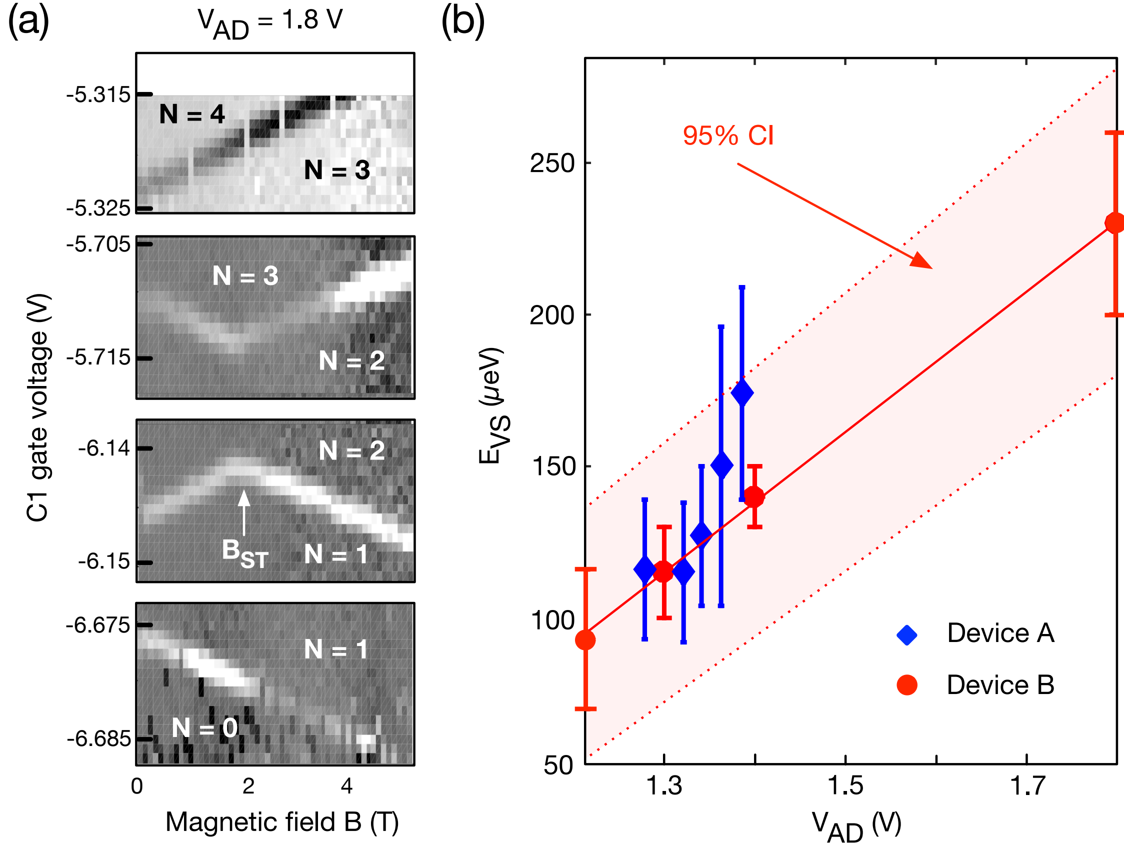

Figure 4.5: Double-Lead Device Magnetospectroscopy and Valley Splitting (a) In-plane magnetospectroscopy measurements for device B, for transitions $N = 0 \rightarrow 1$, $1 \rightarrow 2$, $2 \rightarrow 3$, and $3 \rightarrow 4$, from a stability diagram similar to Figure 4.3(c), at V_{AD}=1.8 V. A lever arm of 31 ± 4 μeV/mV is inferred assuming g=2, within 15% of the lever arm extracted from Coulomb peak width temperature dependence [108]. B_{ST} indicates the magnetic field at which the singlet-triplet transition occurs. (b) Extracted valley splitting E_{VS} as a function of the dot accumulation gate voltage V_{AD}. The diamonds (blue) data points are for device A2 (single-lead, Figure 4.4), and the circles (red) data points are for device B (double-lead, Figure 4.3(a)). Dashed red line indicates the fit for the valley splitting tunability of device B, and the 95% confidence range (CI) is indicated by the red filled region.

4.9 Conclusion

In conclusion, a split enhancement gate architecture implemented in single-lead and double-lead layouts of polysilicon MOS QD devices is explored. The single-electron regime was reliably achieved in three different devices. Using the reservoir enhancement gate to modulate the tunnel rate and compensating with the dot enhancement gate, a tuning orthogonality of $\beta_{AR,AD} \approx 0.9$ decade/meV was found in one of the single-lead devices. It is argued that the notable tuning orthogonality, which is comparable to what can be achieved in devices with a dedicated barrier gate in multi-stack architectures, is boosted by the screening effect arising from the use of an enhancement gate as a tuning knob. In addition, a strongly confined quantum dot with charging energies up to 11 meV and an orbital energy of 3 meV was observed in the device with smallest features, corresponding to a $\sim$ 30 nm radius, and a linearly tunable valley splitting up to 250 μeV.

Chapter 5

Characterization of the CB-HBT at 4 K

5.1 Preface

This chapter was originally published in Applied Physics Letters in 2015 as "Cryogenic preamplification of a single-electron-transistor using a silicon-germanium heterojunction bipolar transistor" [63].

5.2 Introduction

Donor spin qubits have recently received increased interest because of the demonstration of high fidelity coherent control of phosphorus donors using a local electron spin resonance technique [110, 111]. This approach is of interest both for quantum information [71, 112, 113] as well as representing a new experimental platform to investigate the behavior of single impurities in semiconductors using electron and

nuclear magnetic resonance. Single-shot readout [19, 114, 115] of the spin polarization is an important component of the measurement. It may be accomplished using a wide-band measurement of the single electron transistor [116] (SET) conductance, which is sensitive to the ionization condition of any nearby donors [21, 81]. The technique relies on the alignment of the neighboring SET chemical potential between discrete Zeeman energy levels. The donor spin-up electron ionizes into the SET, leading to a detectable transient change in the local electrostatic potential, while an SET electron waits to reload into the donor as a spin-down. The temporary ionization of the donor changes the conductance of the SET, which is measured as a current pulse corresponding to a spin-up electron or no pulse if the electron was spin-down.

Readout fidelity can be no better than what the signal-to-noise-ratio (SNR) provides for a particular bandwidth, although other factors can introduce errors that degrade the fidelity, such as rapid tunneling events that are faster than the bandwidth of the readout. The donor readout technique is performed at cryogenic temperatures less than 4 K, which are typically necessary to observe the spin readout of the donor state at reasonably low magnetic fields. The SET current is subsequently amplified at room-temperature (RT) using one or several amplification stages, typically including a transconductance amplifier. The line capacitance between the transconductance amplifier and the SET typically sets the limits of performance of the circuit. Increased readout bandwidth can improve fidelity, for example, by detecting faster tunnel events, however, the increased bandwidth reduces SNR. The SNR can be increased if amplification is introduced before the dominant noise source contributes to the signal.

Several approaches have been pursued to maximize SNR using cryogenic electronics for readout and amplification. One technique is to embed an SET in an RF resonant circuit, referred to as RF-SET [56, 117, 118], which has resulted in some of

the most competitive readout performance. However, the RF-SET technique requires a significant investment to implement, it introduces some challenges to integration [59, 119, 120], and for the purpose of donor spin readout it, can introduce an additional complication of directly modulating the chemical potential of the SET. An alternative technique, similar in some respects to the RF-SET approach, is to couple an SET or similar device to a superconducting resonator [121–123], which may be followed by additional superconducting quantum circuitry such as a Josephson Parametric Amplifier [58, 124, 125]. Current comparators have shown promise but their thresholds of sensitivity have been near the limits of the current output of SETs, making them difficult to implement without a preamplification stage [126, 127]. Cryogenic preamplification using discrete high-electron-mobility-transistors (HEMTs) has been investigated resulting in sufficient SNR for a particular bandwidth [62]. However, HEMTs may require a relatively high power dissipation, and the typical circuit configuration introduces a fixed load resistance in front of the gate that can limit the circuit bandwidth.

In this chapter, a discrete, commercial silicon-germanium (SiGe) heterojunction bipolar transistor [128–132] (HBT) is used for cryogenic [133, 134] amplification of a silicon SET's output current. This is a preamplification stage for a single electron spin readout circuit. The SiGe HBT can be operated at relatively low power, has low overhead for implementation, and in principle could be integrated with a silicon-based qubit process flow. It is found that the HBT provides a current gain of order of 100–2000. The current gain and the noise spectrum with the HBT result in an SNR that is a factor of 10–100 larger than without the HBT at lower frequencies. The transition frequency defined by SNR = 1 has been extended by as much as a factor of 10 compared to without the HBT amplification. The power dissipated by the HBT is estimated to be between 5 nW to 5 μW for the relevant operation range.

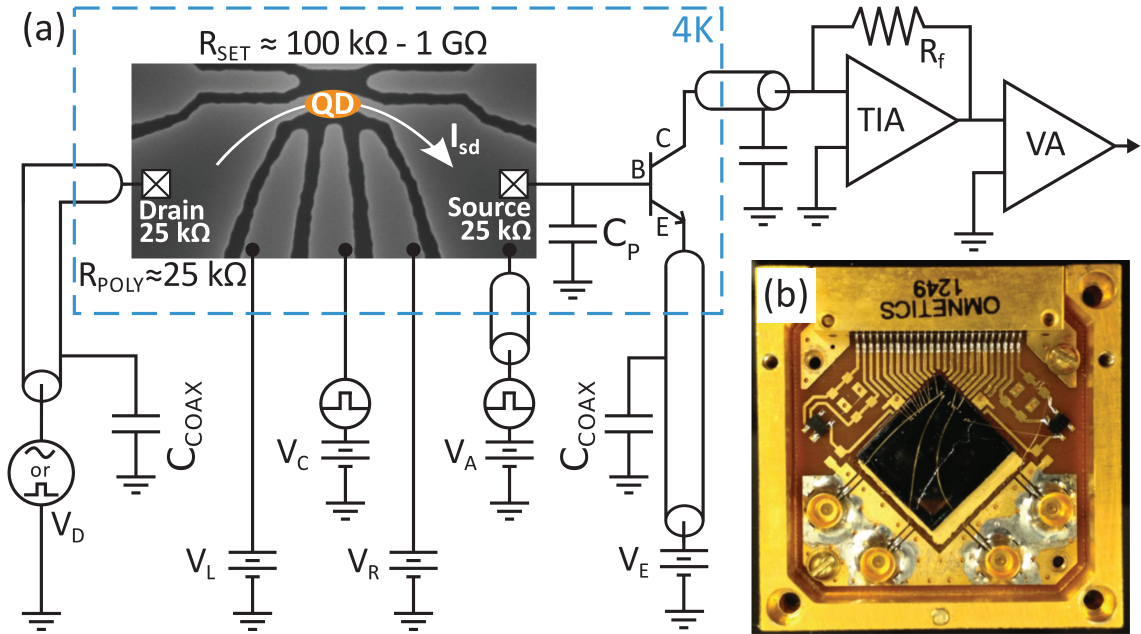

Figure 5.1: HBT-SET Circuit
The SEM image shows the silicon metal-oxide-semiconductor device geometry with polysilicon gates labeled V_L,V_C,V_R, and V_A. The quantum dot (QD) is formed beneath the narrow channel of the gate labeled V_A. The circuit is DC biased by V_E and AC biased by V_D (either sinusoidal or pulsing inputs). The parasitic capacitance, C_P, is due to the device and/or PCB. The parasitic capacitance, C_{COAX}, is due to the length of the wires leading to and from the device immersed in liquid helium at 4 K. Room-temperature transimpedance (TIA) and voltage (VA) amplifiers are used to amplify the signal before it is read out on a lock-in amplifier or oscilloscope.

5.3 HBT Characterization

The measurement circuit with both HBT and SET is shown in Figure 5.1. The base of the HBT is connected to the source of the SET using a bond wire between a surface mount HBT and the SET chip both of which are immersed in liquid helium during measurement. The HBT collector is connected to a one-meter long Lakeshore 304 stainless steel braided coaxial cable with a capacitance of approximately 174 pF/meter. The emitter is connected via an identical cable to either a Keithley 2400

or an Agilent 33500B for low- or high-frequency measurements, respectively. The gate labeled V_A is also connected to coaxial cables for pulsed measurements while all other leads were connected through twisted pair lines. The HBT collector is connected to a room-temperature Femto DLPCA-200 transimpedance preamplifier, unless otherwise noted. A subsequent SR560 voltage preamplifier is used as a variable bandwidth filter but otherwise is set to a gain of 1. Lock-in measurements were done with a Zurich HF2LI or SR830 using a 100:1 resistive voltage divider and typically an excitation voltage of 100 μV or 1 mV on the SET drain, without or with the HBT respectively unless otherwise noted. The DC bias was set by the DC source applied to the HBT emitter with no voltage division.

HBTs were first characterized in liquid helium with room-temperature load resistors without the SET to simulate different SET resistances and calibrate the transistor's collector current as a function of base current and load resistance, Figure 5.2. Multiple commercially available high bandwidth HBTs were measured at low temperature. Resistances between 100 kΩ and 1 GΩ were examined. The DC behavior of these HBTs at low temperature is exponential. As the input current, I_B, increases, the readout current, I_C, increases exponentially, Figure 5.2(a). The turn-on behavior of the HBT in the circuit depends solely on the forward-bias diode drop across the base-emitter (BE) junction, V_{BE}. V_{BE} is calculated by subtracting the voltage drop across the resistor from the bias applied to the emitter. For different resistances, input and readout current behave exactly the same as V_{BE} is increased, Figure 5.2(b),(c). Therefore, for a given readout current the input current is known and by using this curve as a calibration, the potential across an SET connected to the HBT, for a fixed emitter bias, can be estimated as $\triangle V_{SET}(I_C) = |V_E| - |V_{BE}(I_C)|$. Note that not all HBTs measured at 4 K showed greater than unity current gain ($I_C/I_B > 1$) combined with the correspondingly low voltage of $0.1 - 2$ mV across the test resistance. Typical operation of the silicon SETs for readout is done with a bias voltage of $80 - 300$ μV, well below the charging energy of the SET to avoid reduction

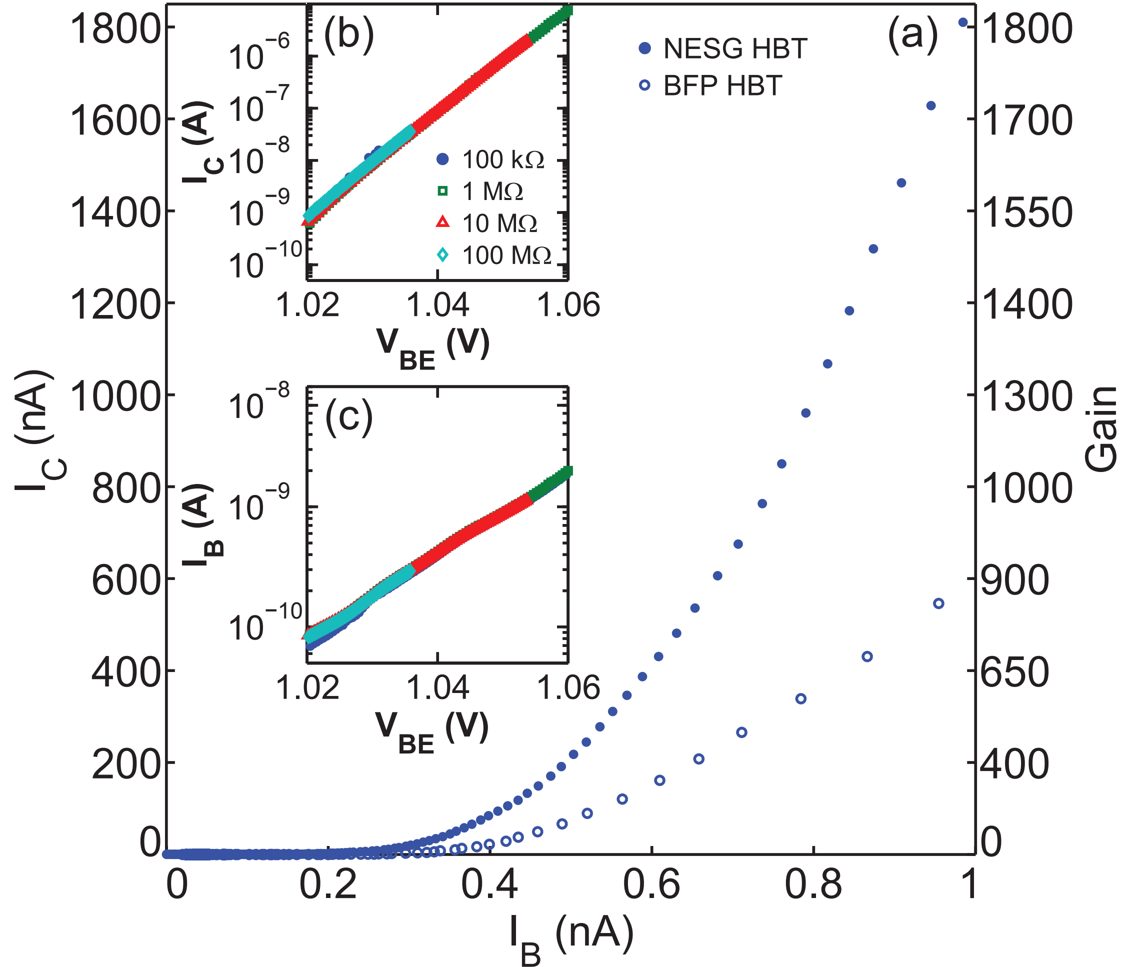

Figure 5.2: HBT Biasing Calibration Curves at 4 K
(a) Collector current and as a function of base current for the CEL NESG3031M05 HBT used and an Infineon BFP842ESD HBT. This curve enables mapping from readout current to device input current regardless of SET resistance. The gain shown is for the NESG HBT. (b) Collector current as a function of the HBT base-emitter voltage for different resistors in-line with an NESG HBT. Identical HBT turn-on behavior is observed regardless of the load resistance before the base-emitter junction of the HBT. (c) Base current as a function of the HBT base-emitter voltage for different resistors in-line with an NESG HBT. These current curves similarly overlap.

of sensitivity from broadening of the Coulomb blockade peaks. Out of 25 HBTs characterized at 4 K, the California Eastern Laboratories (CEL) NESG3031M05[1] HBT showed the highest current gain and lowest test resistance biasing, so it was selected for measurements with the SET.

5.4 Frequency Response

To examine the frequency response of the SET with and without the HBT, narrowband lock-in measurements were done by inputting a small voltage sinusoidal signal into the SET's drain resulting in a sinusoidal input current, i_b, and a sinusoidal readout current, i_c. To ensure the DC operating point was minimally perturbed, input signal magnitudes were constrained to $i_c \leq 0.2 \cdot I_C$, remaining within a linear signal regime. A set of charge stability plots show Coulomb blockade through the quantum dot, Figure 5.3(a),(b),(c). The stability plots are formed by sweeping the center plunger, V_C, and stepping the left and right plungers, $V_{L,R}$, as indicated in Figure 5.1. Qualitatively, the presence of Coulomb blockade confirms that a DC bias can be chosen that produces V_{SD} sufficiently below the charging energy of the QD. It is estimated that V_{SD} for $V_E = -1.051$ V is approximately 1 mV, extracted from the appropriate I_C vs V_{BE} curve.

The HBT-SET current does not go to zero in the blockaded regions. Verilog-A simulations of the circuit including a model for SET conductance and the calibrated 4 K HBT parameters [135] predict that the HBT-SET minimum conductance for the Coulomb blockade will be prevented from going to zero. This behavior is believed to be a consequence of having a floating source that increases V_{SD} to maintain some current through both the HBT and SET at all times. That is, relatively small changes

[1] At the time of publication (2015), the manufacturer's website states that the CEL NESG3031M05 HBT is no longer in production. However, the Infineon BFP842ESD HBT had a similar biasing calibration curve at 4 K as shown in Figure 5.2(a).

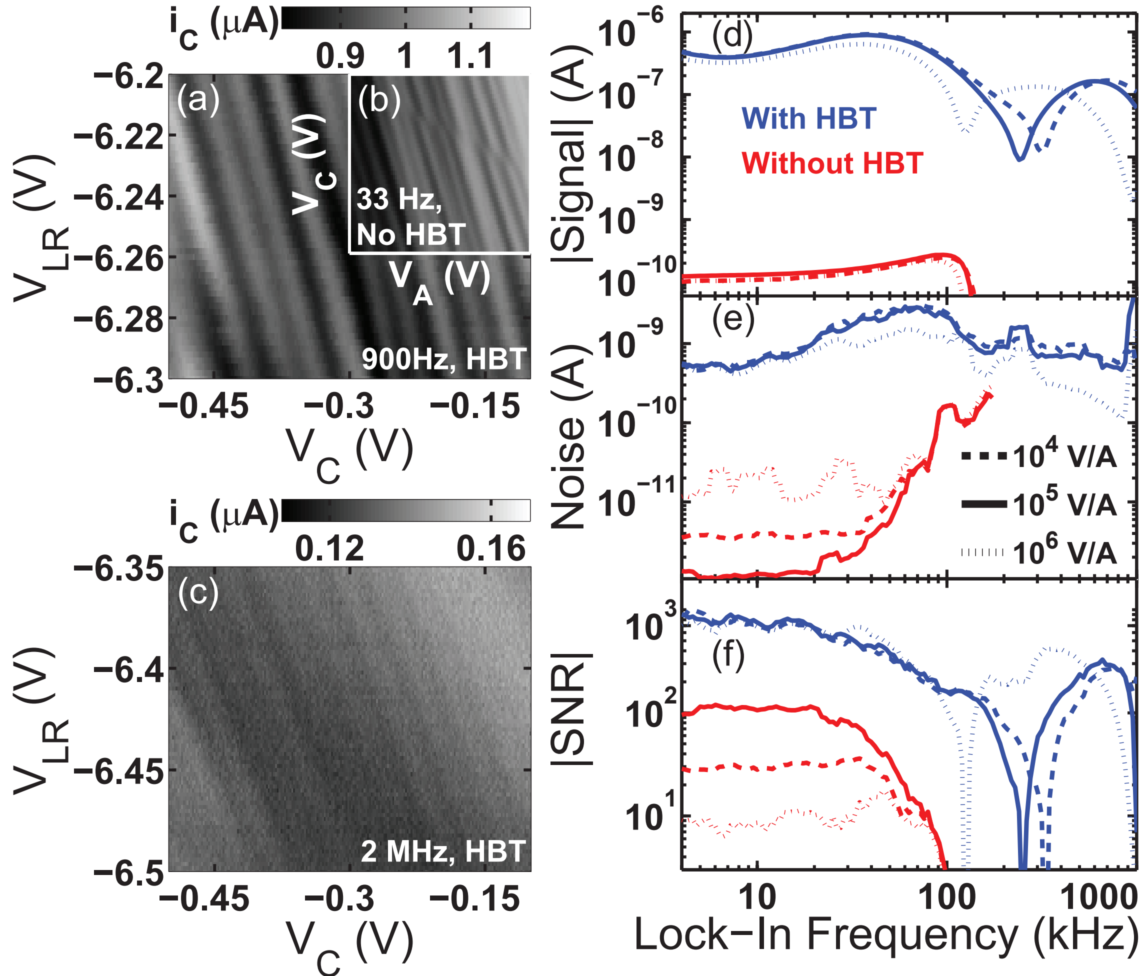

Figure 5.3: HBT-SET Stability Plots and Frequency Domain Data
All measurements were performed at a temperature of 4 K. (a) Stability plot showing the SET Coulomb blockade behavior of the HBT-SET circuit at 900 Hz. Well defined peaks and contrast are found when an HBT is added. (b) Stability plot of same SET and resulting Coulomb blockade with no HBT. Similar contrast to (a) is observed. (c) Stability plot showing the SET Coulomb blockade in a very similar voltage range as (a) but with an input frequency of 2 MHz. The SNR decreases at the higher frequencies in this narrowband measurement. (d),(e),(f) Narrowband measurements as a function of input frequency. All data is the lock-in output's in-phase quadrature. The signal and SNR are plotted as absolute values.

in the DC bias current through the HBT lead to relatively large voltage shifts from V_{BE} to V_{SD}. The current turn-off of the Coulomb blockade is consequently suppressed because the shift of voltage drop from V_{BE} to V_{SD} is always enough to maintain a small current through both the SET and the HBT. Quantum point contacts (QPC) are also frequently used as charge sensors and would likely minimize this complication of the amplification circuit. That is, the conductance of a QPC varies much less over similar bias ranges, and usually, very low conductance conditions can be avoided.

Quantitatively, the cases with and without HBT are compared for equal input signals, 100 μV, and similar SET resistance, 100 kΩ to 1 MΩ, Figure 5.3(d),(e),(f). The lock-in signal shown is the in-phase quadrature. The frequency dependence of the narrowband SNR is shown for several room-temperature transimpedance amplifier gain settings (Figure 5.3(f)). The current gain and the noise spectrum with the HBT result in a signal-to-noise-ratio (SNR) that is a factor of 10–100 larger than without the HBT at lower frequencies. For stability plots such as Figure 5.3(a), the lock-in time constant was able to be reduced by at least a factor of 10 due to the increased SNR, thereby reducing the total acquisition time by at least the same factor.

In Figure 5.3(f), the transition frequency, defined by SNR = 1, for the case without the HBT is observed to be $\sim$ 100 kHz, where $|\mathrm{SNR}| << 1$ for frequencies higher than 100 kHz. The transition frequency is extended with the addition of the HBT. The extended transition frequency with the HBT enabled acquisition of narrowband stability plots at 2 MHz, as shown in Figure 5.3(c). For frequencies near and beyond approximately 200 kHz in Figure 5.3(f), a significant shift in phase that approaches 180 degrees is observed in the lock-in detected signal. The absolute value of the signal and SNR is plotted in Figure 5.3(d) and 5.3(f) in order to show this phase shift. Circuit analysis of Figure 5.1(a) indicates that the HBT circuit has a pole due to the SET resistance and the parasitic capacitance, C_P, as well as an additional

pole due to the HBT base-collector resistance and the parasitic capacitance of the coaxial cables, C_{COAX}.

5.5 Time Domain Measurements

The response of the HBT-SET circuit was measured in the time domain by tuning the SET in resonance with a nearby charge center such that tunneling events on/off of the charge center are observed as changes in the conductance of the SET between two conductance states: charge center neutral or ionized, Figure 5.4(a),(b),(c). This is similar to a charge sensing or spin readout configuration. The magnitude of conductance change is not the largest possible but was chosen in this case because of a combination of factors including the average tunneling rate of the transition. These data were acquired using a room-temperature amplification chain consisting of a Femto DLPCA-200 transimpedance amplifier with sensitivity 10^5 V/A followed by an SR 560 voltage amplifier with a gain of 1 and variable low-pass filter -3 dB frequencies. Measurements of signal amplitude, noise (RMS deviation from the mean value of a voltage level), and SNR are summarized for voltage-amplifier low-pass filter settings up to 1 MHz. Other circuit parasitics introduce signal loss at frequencies less than 1 MHz as indicated by the narrowband measurements, however, SNR > 1 is still achieved at ~ 1 MHz with the HBT-SET circuit, as shown by the green (RTS) curve in Figure 5.4(f).

The circuit response to direct pulsing on the drain ohmic was investigated to more directly examine rise/fall time response. The pulses were generated by applying externally controllable square voltage pulses to the drain ohmic, with the voltage amplitude converted to a current amplitude by measuring and taking the difference of the current at both voltage levels with a current meter. Square pulses with amplitude 150 pA and width 2 ms were used for the uppermost (blue) curve in Figure

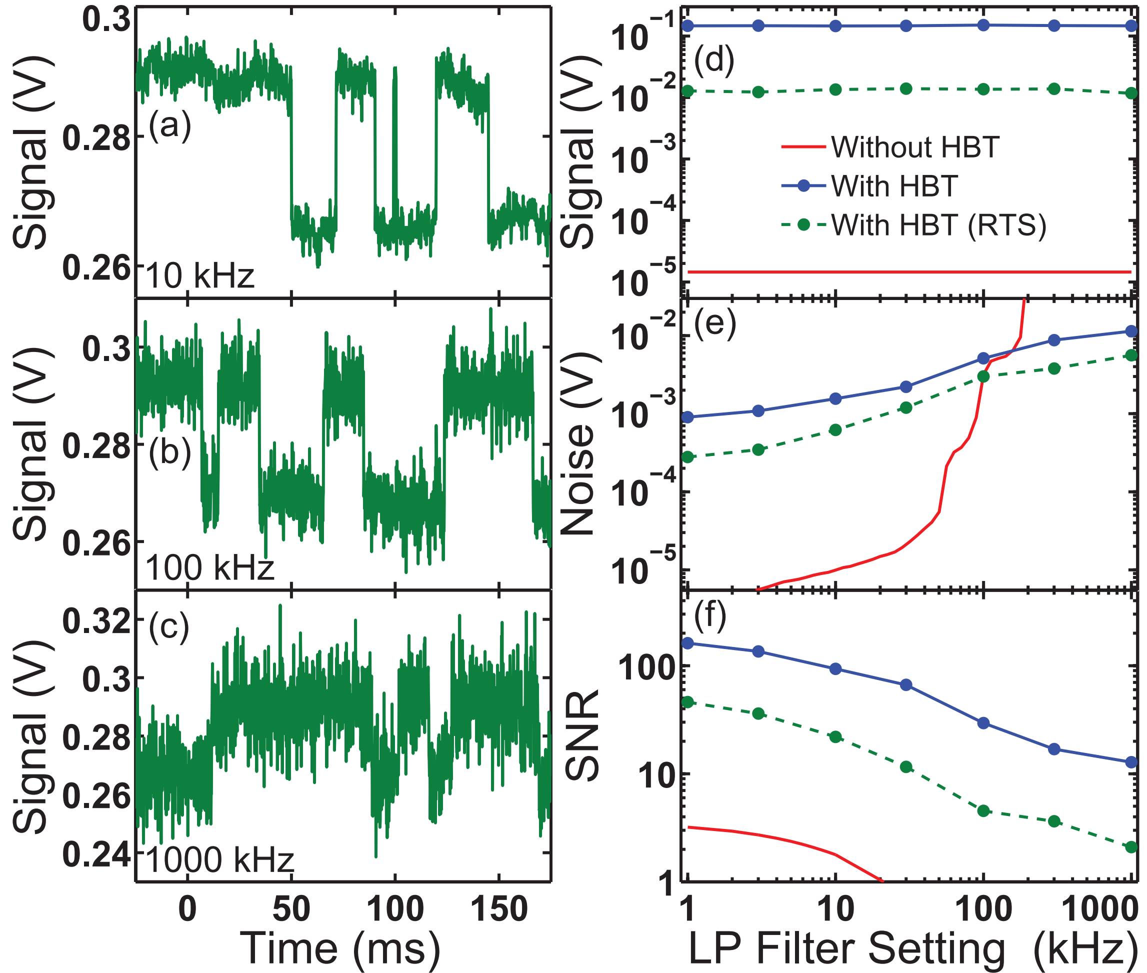

Figure 5.4: HBT-SET RTS Readout Traces with Signal, Noise, and SNR (a),(b),(c) Single-shot oscilloscope traces of random telegraph signal (RTS) due to proximal charge center tunneling. Room-temperature low pass filter settings of 10 kHz, 100 kHz, and 1000 kHz are used to monitor the RTS. (d),(e),(f) Measured wideband signal magnitude, noise magnitude, and SNR as a function of low-pass (LP) filter setting. The blue curves show calibrated input current (150 pA) pulse data for the HBT-SET circuit. The red curve is the same current input as the blue curve with noise calculated from the narrowband noise spectral density for the SET circuit without the HBT. The green curve shows the measured RTS data from Figure 5.4(a)–(c).

5.4(d). This data was acquired using an RT amplification chain consisting of a Femto DLPCA-200 transimpedance amplifier with sensitivity 10^5 V/A followed by an SR 560 voltage amplifier with a gain of 1 and variable low-pass filter -3 dB frequencies. It was found that the conductance of the SET modified the bandwidth of the circuit response and that for the minimum and maximum conductances examined, 0.313 μS and 0.183 μS, respectively, the response times were 14.5 μs and 0.612 μs, respectively. The SNR from the random telegraph signal (RTS) like behavior is overlaid as green curves. The blue curve in Figure 5.4(f) shows an improved SNR primarily because the current through the SET is being driven by an external pulse instead of being limited by the change in conductance in the SET from the RTS charge center at a fixed V_{SD} range. Through the calibration of voltage to current, a current amplitude of 13 pA for the RTS data in Figure 5.4(a)–(c) is observed.

For comparison between the device with and without the HBT, the wideband SNR is estimated from the narrowband measurements. That is, if it is assumed that the same current pulse amplitude of 150 pA is used for the uppermost (blue) curve in Figure 5.4(d), the total noise can be calculated by integrating the noise spectral density that was measured in the narrowband measurements without the HBT. Noise spectral density was calculated by dividing the solid red curve in Figure 5.3(e) by the square root of the noise-equivalent-power bandwidth of 1.25 Hz, calculated from the lock-in time constant and filter roll-off. The noise spectral density was integrated to an upper limit equal to the voltage amplifier low-pass filter -3 dB frequency, resulting in the red curve in Figure 5.4(e). It is found that the noise increases nonlinearly with the HBT and also for the calculated case without the HBT, while the signal stays constant throughout the low-pass filter setting range. With the HBT, there is an increase in SNR of about a factor of 10 for the RTS case (green), and about a factor of 60 for the direct pulsing case (blue) at lower frequencies. The greater SNR, particularly at lower frequencies, appears to be due to amplification in the signal before the dominant noise source is introduced, perhaps near the input of the

preamplifier at room-temperature. The SNR for the direct pulsing (blue) and the RTS (green) is reduced at higher filter settings because of the nonlinearly increasing noise. However, with the HBT the gain is sufficiently high such that pulsing events are detectable at the microsecond time scale.

An estimate of the DC power dissipation of the HBT can be made by taking the product of the current through and the voltage across the HBT. The peak conductance conditions observed in this work correspond to $I_B \approx 1$ nA and $I_C \approx 5$ μA maximum and $|V_E| \approx 1$ V, from which a power dissipation of $V \cdot I = 1(V) \times 5 \cdot 10^{-6}(A) = 5$ μW is estimated. Regions off of peak conductance, that is, most of the stability diagram, correspond to power dissipations as low as 10–100 nW. Even at the highest estimated power of 5 μW, the power dissipation is less than or about equal to the cooling power of the lowest temperature stage of a dilution refrigerator.

5.6 Conclusion

A discrete, commercial SiGe HBT was examined for low power cryogenic preamplification of an SET charge sensing circuit. The HBT-SET charge sensing circuit is shown to produce a substantial increase in SNR relative to the SET charge sensing circuit without an HBT. The gain is non-linear when using the SET readout configuration. readout behavior is simulated by using the circuit to detect random telegraph signal of a nearby charge center. The HBT-SET circuit was voltage biased to a point where the power dissipated was 0.01–5 μW; the gain was 100–2000; and the source-drain bias across SET was $\sim$ 0.1–1 mV. The current gain and the noise spectrum with the HBT result in an SNR that is a factor of 10–100 larger than without the HBT at lower frequencies. The transition frequency defined by SNR = 1 has been extended by as much as a factor of 10 compared to without the HBT amplification. The increased performance is believed to be due to signal gain near

the SET before a major noise source is introduced in front of the room-temperature transimpedance amplification stage.

Chapter 6

HBT Circuit Comparison

6.1 Introduction

Spin qubits in semiconductors are a promising platform for building quantum computers [4, 17, 19–21, 136–138]. Significant progress has been achieved in recent years, including demonstrations of extremely long coherence times [2], high-fidelity state readout [5, 139–141], high-fidelity single qubits gates [2, 74, 75, 142], and two-qubit gates [3, 4, 142, 143]. As the field advances to multiple qubit systems, improvements in single-shot state readout and measurement times will be necessary to achieve fault tolerance. Improving the signal-to-noise ratio (SNR) and bandwidth (BW) of the qubit state detection is critical for both tunnel rate selective readout [19] and energy selective readout [20]. With the same bit error rate, faster readout will reduce tunnel rate and metastable relaxation or relaxation related errors.

Cryogenic amplification is one way the readout SNR and BW can be improved. Challenges are that: 1) input signals remain relatively small [22, 144–147] and 2) significant noise and parasitic capacitance is introduced into the measurement circuit when routing the signal out of a dilution refrigerator [66]. Several approaches for cryo-

genic amplification include: radio-frequency (RF) resonant quantum point contact (QPC) and single electron transistor (SET) circuits [56, 57, 115, 117, 120, 148–150], gate dispersive RF circuits [59], Josephson parametric amplification circuits [58], and cryogenic transistors [6, 60–63]. For single-shot readout, qubit state distinguishability with sensitivity 140 $\mu e/\sqrt{\text{Hz}}$ has been demonstrated [56]. However, many of these circuits require elements to be mounted at multiple fridge stages and the use of custom on-chip components, adding to the complexity of their implementation. Simpler amplification circuits that use low power transistors mounted directly on the mixing chamber stage with the qubit device thus have significant appeal [6, 63]. For example, a proof of principle readout demonstration with a dual stage HEMT achieved Te = 240 mK, gain = 2700 A/A, power = 13 μW, noise referred to input $\leq$ 70 fA/$\sqrt{\text{Hz}}$, and 350 $\mu e/\sqrt{\text{Hz}}$ charge sensitivity [6].

Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have been demonstrated to operate at liquid helium temperatures [63, 132], as well as millikelvin temperatures in dilution refrigerators [131, 151–153]. The HBT is motivated by low 1/f noise, high R_{out}, and possible opportunities to achieve higher gain at the same power. Furthermore, there can be bipolar junction transistor (BJT) advantages compared to field effect transistors (FETs) for low input impedance amplifier circuits [154]. The approach here is to use a single SiGe HBT as a cryogenic amplifier at the mixing chamber stage of a dilution refrigerator to improve the SNR and BW of the signal from an SET used as a charge-sensor. Two different HBT circuits have been designed and characterized: 1) the current-biased HBT circuit (CB-HBT) (Figure 6.2(a)) and 2) the AC-coupled HBT circuit (AC-HBT) (Figure 6.1(a)). The CB-HBT simply has the drain of the SET connected to the base of the HBT, while the AC-HBT has the base of the HBT connected to the drain of the SET via a resistor-capacitor (RC) bias tee. Regardless of the coupling between the HBT and SET, the HBT must be DC biased in order to amplify. For either circuit, the silicon metal oxide semiconductor (Si-MOS) device and HBT are mounted on a printed circuit

board (PCB) only centimeters apart. The proximity of the HBT amplifier to the SET has the advantages of minimizing parasitic input capacitance and increasing signal before noise from the fridge is added. However, since the mixing chamber stage has a cooling power of around 100 μW at 100 mK, the HBT circuits must operate with powers similar or less in order to avoid heating.

In this chapter, the two amplification circuits are first introduced with discussions of gain, sensitivity, bias behavior, and noise. The basic performance and operation of the two amplifiers are then compared and the input-referred noise is extracted as well as signal response and heating of the quantum dot electrons. Finally, the performance for single-shot readout is compared and discussed, which somewhat depends on the specific layout of the SET and quantum dot to produce larger signals via increased mutual capacitance.

6.2 AC-HBT Description

The AC-HBT consists of a Si-MOS device that is AC-coupled to an HBT, which amplifies the SET response to AC source-drain voltage excitation at frequencies higher than around 100 Hz. The SET is integrated into a double quantum dot (QD) device (Figure 6.1(a): SEM image), which is made on a Si-MOS platform (see Section 6.6).

To operate the AC-HBT, the DC base bias is grounded, and the emitter is biased negatively to support a base-emitter bias V_{BE} above the cryogenic HBT threshold (about -1.04 V). The HBT current at the collector is measured through a room temperature transimpedance amplifier (TIA), and the signal is demodulated, filtered, and digitized. The TIA is referenced to ground, so the collector-emitter bias equals the base-emitter bias. This configuration is found to optimize the circuit SNR and also requires only two lines coming from room temperature for the three HBT termi-

nals. Figure 6.1(c) shows the total AC circuit gain and sensitivity vs. the amount of power dissipated by the HBT. The AC gain is measured by comparing the current of a Coulomb blockade (CB) peak with and without the HBT. The SET current can be measured directly by connecting the output of R_S to a room temperature TIA (lowest ground in Figure 6.1(a)). The sensitivity of the circuit is defined as the gate-voltage derivative of collector-current (slope) on the side of a CB peak, which is the typical bias point where readout occurs. Sensitivities of 1–5 μA/V are achieved in the operating region of the AC-HBT. Since the AC-HBT is a linear amplifier, the shape of a CB peak remains unaffected by different gain/sensitivity bias points of the AC-HBT (Figure 6.1(d)). The AC bias across the SET was chosen to be 200 μV_{RMS} in this case to minimize the electron temperature below 200 mK.

Noise spectra are collected for different AC-HBT biases (see Section 6.11), and noise at around 74 kHz is referred to the HBT collector and studied. The noise displays two different behaviors as the power dissipated is increased (Figure 6.1(e)). The transconductance of the transistor ($\frac{dI_C}{dV_{BE}}$) increases with power, so it is important to identify where the transistor begins to add appreciable noise. In the low-power limit, the noise dependence is approximately flat at around 1 pA/$\sqrt{\text{Hz}}$, which is attributed to the noise after the HBT dominating any AC-HBT noise. As the AC-HBT power is increased to > 1 μW, the noise becomes linearly dependent on power. This behavior is predicted by the estimated shot noise for the base current (Figure 6.1(e) orange curve). The estimated total noise is calculated by adding all noise source predictions in quadrature (dark red curve) and aligns well with the total measured noise (blue points).

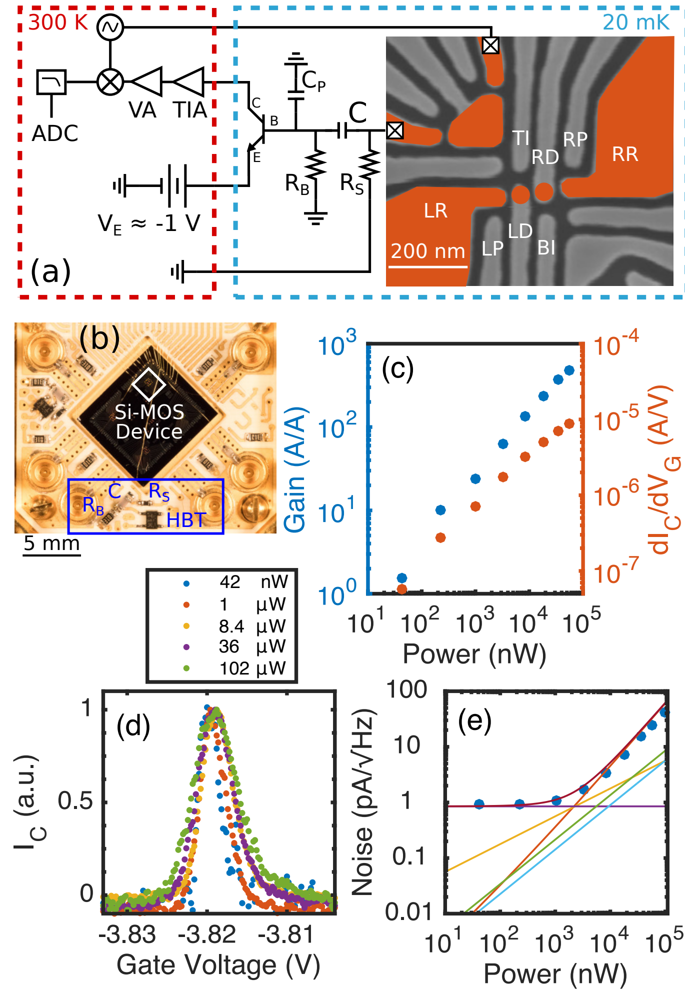

Figure 6.1: AC-HBT Schematic and Measurements
(a) Schematic diagram of AC-HBT and SEM image of the double quantum dot (DQD) device. Areas of electron accumulation are indicated by false color highlighting of enhancement gates. The charge sensor used to measure the DQD state is in the upper left quadrant, whose source is connected to an AC+DC signal generator, and whose drain is connected to a cryogenic AC-coupled HBT amplification stage. The amplification stage is mounted at the dilution refrigerator mixing chamber on the same printed circuit board as the DQD device. Values of the passive elements are $R_B = 1$ MΩ, $R_S = 100$ kΩ, and C = 10 nF. (c) Circuit gain and sensitivity vs. power dissipated by the AC-HBT. (d) Normalized CB peak for different AC-HBT gain/power biases. The blockade region of the CB peak reaches zero current. (e) Noise referred to the collector of the AC-HBT for different powers. The measured noise is plotted as blue points. The noise floor of the fridge (purple), shot noise of the base (orange), collector (yellow), SET (light blue), Johnson noise of the shunt resistor (green), and total estimated noise (dark red) are plotted as solid lines.

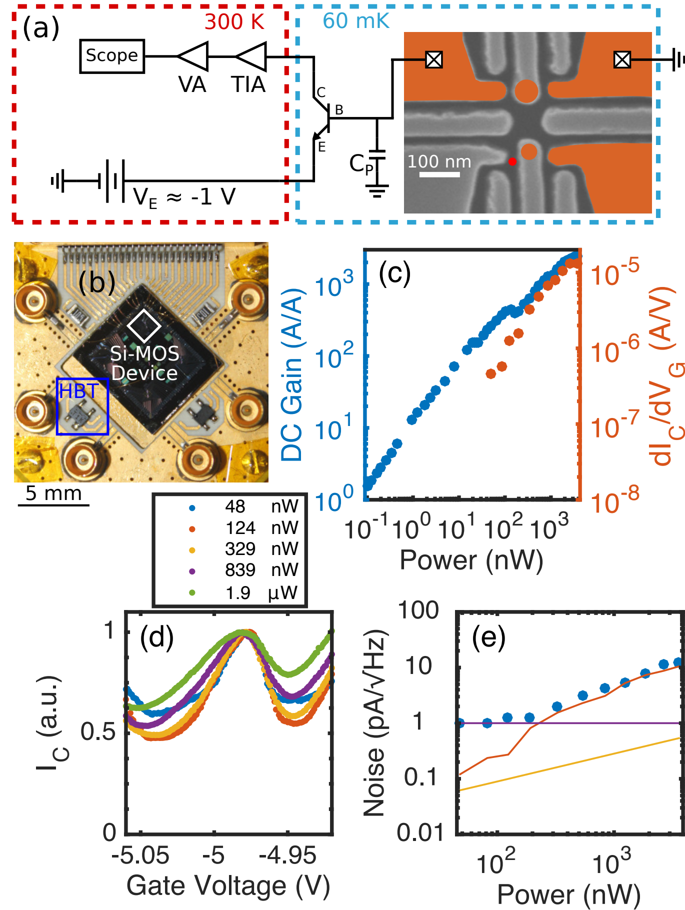

Figure 6.2: CB-HBT Schematic and Measurements

(a) Schematic diagram of CB-HBT readout circuit including room temperature amplification and biasing. The SET is represented by the larger, upper orange circle, and the QD is represented by the smaller, lower orange circle. (b) Image of the PCB which shows the Si-MOS device and HBT mounted close together. (c) DC current gain and sensitivity vs. power dissipated by the CB-HBT. (d) Normalized CB peak for different CB-HBT gain/power biases. The blockaded regions of the CB peak do not reach zero current. (e) Noise referred to the collector of the CB-HBT for different powers. The measured noise is plotted as blue points. For comparison, the noise floor of the fridge (purple curve), base current shot noise (orange curve), and collector current shot noise (yellow curve) are plotted as well.

6.3 CB-HBT Description

The CB-HBT circuit consists of an HBT wire bonded from its base terminal directly to the drain of the SET. The SET is integrated into a double QD system consisting of a lithographic QD and a secondary object that has not been definitively identified (i.e., either a QD [78] or donor [22]). A high-frequency coaxial line is connected to the collector of the HBT which is used to measure the readout current (Figure 6.2(a)). This collector line is connected to a TIA which is set with gain 10^5 V/A and -3 dB bandwidth 400 kHz unless otherwise noted. The output of the TIA is connected to a voltage amplifier used to limit the bandwidth or further amplify the signal. Finally, the output of the voltage amplifier is connected to an oscilloscope with an adjustable sample rate.

Operation of the circuit requires the emitter of the HBT to be connected to a room temperature power supply filtered to 1 MHz (to suppress higher frequency noise) and biased between -1.03 and -1.07 V. The bias of the emitter power supply sets the base current, collector current, gain, and dissipated power of the HBT. In Figure 6.2(b), the DC current gain and sensitivity are plotted as a function of power. The DC current gain is defined as $\frac{I_C}{I_B}$, and the sensitivity is defined as before. The sensitivity of the CB-HBT can reach 5 μA/V between 100–500 nW, whereas the AC-HBT requires > 10 μW to reach a similar sensitivity.

The CB-HBT acts as a current bias, so there is always current through the SET (see Section 6.7). In regions of Coulomb blockade, the HBT base-emitter voltage will shift on the order of the charging energy of the SET in order to maintain a relatively constant current through the circuit. To show the current-biasing effect, a CB peak is plotted for different CB-HBT gain values in Figure 6.2(d), and the current is normalized to the value at the top of the CB peak. Although the current in the blockaded regions of the CB peak is much different from a voltage-biased

configuration, the slope of the sides of the CB peak appears to be less affected by the current-biasing (sensitivities of 1–5 μA/V are achieved for either circuit). Note that the effect of current bias on Coulomb blockade is independent of the HBT presence (Figure 6.7).

As with the AC-HBT, the noise referred to the collector of the CB-HBT is examined at around 7 kHz (Figure 6.2(d)). Similar qualitatively, the lower power region is dominated by noise after the HBT around 1 pA/$\sqrt{\text{Hz}}$ (purple curve). As power is increased, the measured noise (blue points) begins to increase, which follows the estimated behavior of the base current shot-noise (orange curve) (see Section 6.11).

6.4 Amplifier Performance Comparison

The performance of both amplifiers with respect to the power dissipated is compared in several different ways. The first metric examined is gain as power is increased. The gain of the AC-HBT is simply the measured gain of the amplifier, however, the gain of the CB-HBT circuit is not as simple to extract. The small-signal resistance of the SET (r_{set}) must be known in order to calculate the CB-HBT gain (see Section 6.10). Since the SET is directly connected to the HBT, it is difficult to measure r_{set}. Instead, the value of r_{set} (3 MΩ) is used which best follows the measured noise behavior in Figure 6.2(e) to estimate the gain. This estimated gain of the CB-HBT circuit is plotted and compared to the measured gain of the AC-HBT circuit in Figure 6.3(a). It is observed that the CB-HBT circuit achieves higher gain at lower powers, including operating with gain over 400 at a power around 1 μW.

Next, the noise referred to the input of the HBT is compared for each circuit. Noise is referred to the input using the gain values in Figure 6.3(a). The noise spectrum for each circuit is measured at different bias points and the frequency is chosen to minimize noise. The frequency chosen for the AC-HBT circuit was around

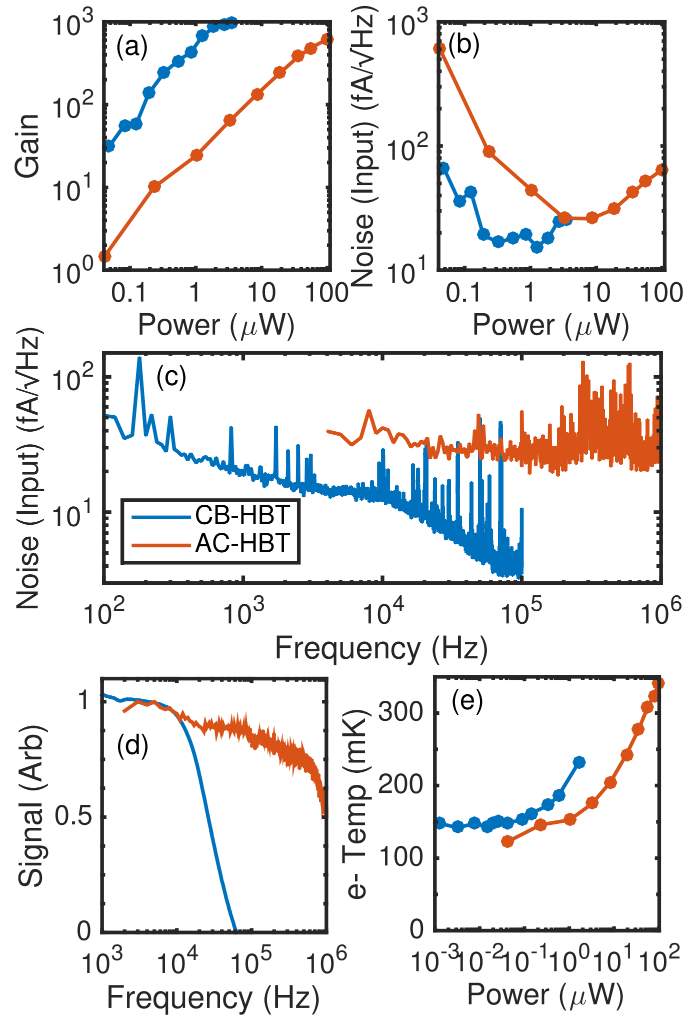

Figure 6.3: HBT Amplifier Performance Comparison

(a) The gain of both circuits as a function of power. The calculated gain of the CB-HBT is shown (Section 6.10). (b) Minimum input-referred noise as a function of power. CB-HBT has minimum of 19 fA/$\sqrt{\text{Hz}}$ at 800 nW, and AC-HBT has minimum of 26 fA/$\sqrt{\text{Hz}}$ at 8.4 μW. (c) Input-referred noise spectrum of both circuits for power that minimizes noise. (d) Signal response (in normalized arbitrary units) for both circuits as a function of frequency. The CB-HBT has a -3 dB point at around 20 kHz, and the AC-HBT has a -3 dB point at around 650 kHz. (e) Electron temperature vs. power for both circuits. Base electron temperatures are between 120–150 mK.

74 kHz, and the frequency for the CB-HBT circuit was around 7 kHz. When the input-referred noise is plotted as a function of power (Figure 6.3(b)), a minimum noise operating point for either circuit is observed. At low powers, the noise is likely dominated by triboelectric noise due to the fridge and input noise of the room temperature TIA. At higher powers, the HBT amplifiers begin injecting appreciable noise into the circuit, therefore the overall noise increases. The CB-HBT circuit achieves a minimum noise of 19 fA/$\sqrt{\text{Hz}}$ at a power around 800 nW, while the AC-HBT circuit achieves a minimum noise of 26 fA/$\sqrt{\text{Hz}}$ at a power around 8.4 μW.

For the powers that minimize noise for each circuit, the input-referred noise spectrum is plotted for both circuits as a function of frequency (Figure 6.3(c)). The noise spectrum of the CB-HBT is plotted out to 100 kHz, since its bandwidth is less than 100 kHz. The 1/f-like behavior of the noise at lower frequencies is assumed to be due to charge noise in the Si-MOS device. In the overlapping region around 10 kHz, the noise for the CB-HBT is significantly lower than the noise for the AC-HBT.

Figure 6.3(d) shows the frequency dependence of an input signal for both amplification circuits up to 1 MHz. The AC-HBT has a -3 dB point at around 650 kHz, and the CB-HBT has a -3 dB point at around 20 kHz, which implies significantly lower BW than the AC-HBT. The origin of this lower BW is not well understood. Using pessimistic numbers, the frequency pole of the SET resistance (assuming 1 MΩ) and the parasitic capacitance between the SET and the base junction (assuming 1 pF) should only limit the -3 dB point to around 160 kHz. In addition, 4 K simulations of this circuit also yielded around 160 kHz -3 dB BW [155]. Improvements and understanding of the BW of the CB-HBT will be important in future work.

Heating of electrons in the QD due to the operation of the connected HBT is a concern, therefore the dependence of electron temperature on HBT amplifier bias (Figure 6.3(e)) is examined. For the CB-HBT, the minimum electron temperature observed is around 150 mK. Heating of the QD begins where the CB-HBT is oper-

ating with over 100 gain at 100 nW, therefore the CB-HBT circuit can amplify well with an electron temperature around 160–200 mK. For the AC-HBT, the minimum electron temperature was around 120 mK. When the AC-HBT bias is increased up to 3.24 μW, the electron temperature remains near the minimum temperature. For powers above this threshold, the electron temperature increases approximately linearly with power. Nonetheless, an electron temperature of 200 mK is used for the bias condition that provides the minimum amplifier noise.

6.5 Single-Shot Results Comparison

Both HBT amplifiers are compared by performing single-shot readout of latched charge states [5]. Both Si-MOS quantum dot devices are tuned to the few-electron regime and the spin filling of the last few transition lines are verified with magnetospectroscopy. Figure 6.4(a) shows the result of a three-level pulse sequence in the AC-HBT device where: 1) the system is initialized into (1,0), 2) ground and excited states are loaded in (2,0), and finally 3) the measurement point (signal plotted) is rastered about the (2,0)-(1,1) anti-crossing. When measuring for 30 μs, three latched lines are present, which indicates spin blockade for an excited state triplet (T), a second excited state triplet (O), and a lifting of the spin blockade for the ground state singlet (S). T is assigned as a valley triplet with valley splitting of 140 μeV and the O is assigned as an orbital triplet with an orbital splitting of 280 μeV. For all single-shot measurements, the state O is removed from the available state space by energy selective loading of the (2,0) state.

For both circuits, a mixture of (2,1) and (2,0) charge states are read out in the reverse latching window. Figure 6.4(b) shows 100 individual single-shot traces of the readout portion of the pulse for the AC-HBT device. Significant feedthrough is observed in the first few μs of the readout pulse, likely due to attenuators connecting

the conductor of the high BW lines to the ground of other lines including the emitter bias line. State distinguishability does not begin to occur until about 4 μs, and then the pulse relaxes to two distinct states after about 7 μs. Extracting the SNR from these traces is done by waiting a certain amount of time, t_{delay}, and then averaging the signal for a certain amount of time, $t_{integration}$. Histograms of the delayed and averaged shots are compiled and fit to a double Gaussian distribution (Figure 6.4(c)). The signal is defined as the separation of the center of the Gaussian peaks, and the noise is defined as the average of the standard deviations of the Gaussian peaks. The SNR is defined as the signal divided by the noise.

The extracted SNR for a given delay and total time ($t_{delay} + t_{integration}$) is plotted in Figures 6.4(d)&(e). Contours are drawn for each SNR integer on both plots, where the leftmost part of a contour line reveals the minimum total measurement time required to reach a given SNR. The SNR vs. minimum total measurement time is plotted in Figure 6.4(f) for both circuits. The CB-HBT reaches greater SNR at any given time in the 15 μs plot range. Both circuits achieve SNR > 7 in $t_{total} < 10$ μs, which corresponds to a bit error rate $< 10^{-3}$ and marks a significant improvement over the equivalent $t_{total} = 65$ μs in previous work [5]. In particular, the CB-HBT is able to reach SNR > 7 in $t_{total} \approx 6$ μs, which represents over a factor of ten improvement from the previous work [5]. The charge sensitivity for the CB-HBT is 330 $\mu e/\sqrt{\text{Hz}}$ ($\tau_{int} = 6$ μs, SNR $= 7.4$), and the charge sensitivity for the AC-HBT is 400 $\mu e/\sqrt{\text{Hz}}$ ($\tau_{int} = 9$ μs, SNR $= 7.5$). Note that the SET in the CB-HBT device had around 34% more signal due to the larger mutual capacitance (Section 6.6) which may contribute to the larger SNRs.

The AC-HBT requires more relative overhead for implementation than the CB-HBT. The AC-HBT includes three additional surface-mounted passive elements (Figure 6.1(a)), which can be optimized to produce better SNR. Additionally, the AC-HBT has a two-dimensional bias space via the base bias and emitter bias, whereas

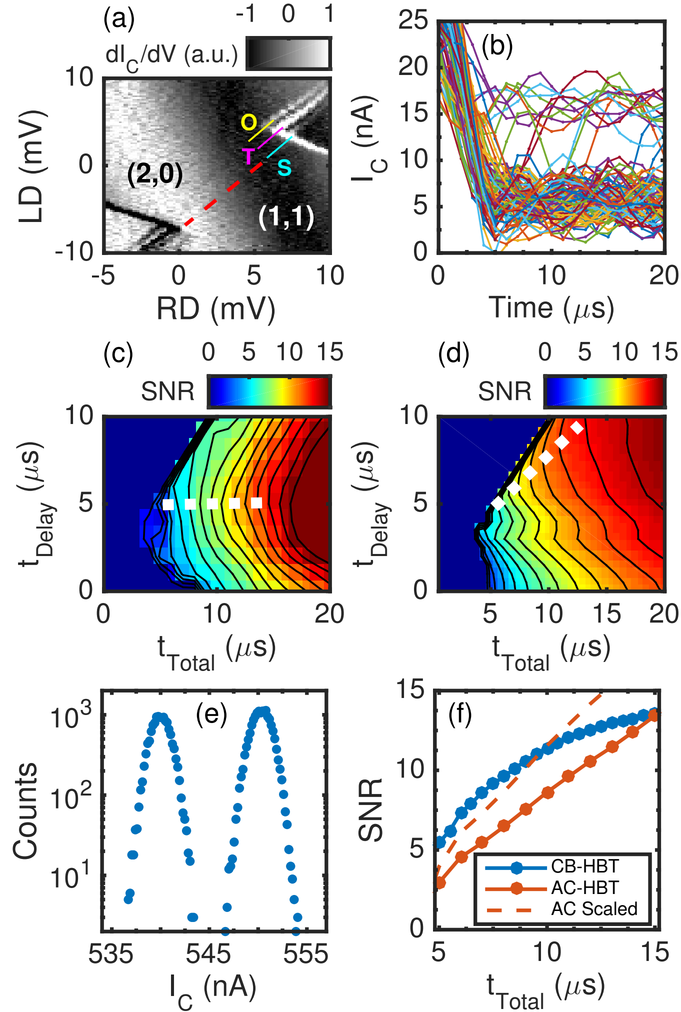

Figure 6.4: Single-Shot Results Comparison

(a) The measurement pulse signal (derivative) rastered about the (2,0)-(1,1) anti-crossing for the AC-HBT device. Three distinct latched lines are present. (b) 100 single-shot traces of the readout portion of the pulse for the AC-HBT device. Signal separation begins to occur around 4 μs. (c) Example histogram from the CB-HBT readout. (d) 2D SNR plot for the CB-HBT readout. (e) 2D SNR plot for the AC-HBT readout. (f) SNR vs. minimum total measurement time for both circuits, which corresponds to the white dashed line in (c) and (d). The greater gain of the CB-HBT compensates for the lower bandwidth relative to the AC-HBT. The AC-HBT is also shown scaled by 34% to compare more directly to the CB-HBT, which had a larger SET signal.

the CB-HBT is only biased via the emitter bias. However, the AC-HBT is a linear gain circuit and can be used with discrete HEMTs [156] and HBTs, providing more opportunity to optimize the transistor. Ideally, the transistors would have greater transconductance (g_m) and a more ideal dependence on I_C than the HBTs used in this work (see Section 6.9). In the present demonstration of the AC-HBT, heating of electrons occurred at powers which minimized noise. Introducing a second AC-HBT stage is relatively straightforward and may allow the first stage to run at powers which don't heat the electrons and minimize the noise further. In addition, the second stage could be mounted further away from the Si-MOS PCB and reduce local heating.

6.6 SET Geometries And Details

The SET connected to the AC-HBT uses a single layer doped poly-Si electrode structure on 50 nm thick SiO_2, providing a mobility of 19,500 cm^2/Vs at 4 K. The poly-Si gate layer is etch-defined into electrodes that control the formation of the SET (upper left in Figure 6.1(a) SEM image) and two quantum dots (under gates RD and LD). Regions of electron enhancement are indicated by the highlighted regions.

The Si-MOS device in the CB-HBT circuit is similar to the Si-MOS device in the AC-HBT circuit with the exception that the SiO_2 layer is 35 nm thick and the bottom layer is isotopically purified silicon (500 ppm ^{29}Si). The ^{28}Si isotope has no net nuclear spin, therefore it is ideal for qubits to be formed in because decoherence due to magnetic noise is highly suppressed. Phosphorous (^{31}P) donor atoms are embedded in the ^{28}Si layer using ion implantation near where the quantum dot is intended to be formed (red dot in Figure 6.2(a) SEM image).

The CB-HBT and AC-HBT were characterized using different Si-MOS devices possessing different electrostatic gate layouts (Figure 6.5). The geometry of the

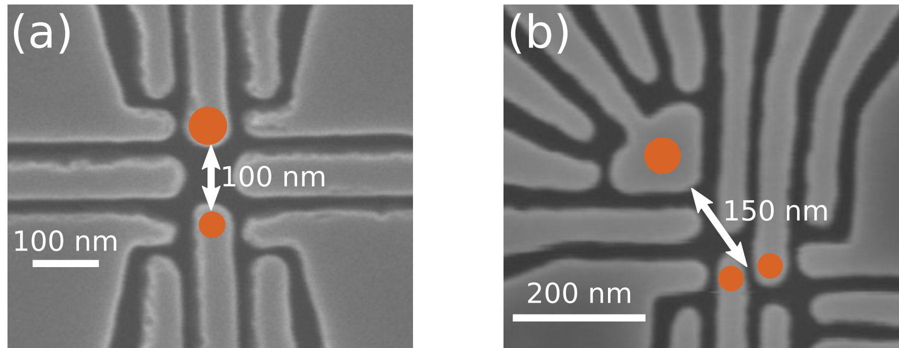

Figure 6.5: SET Geometry Comparison
(a) SEM image of Si-MOS device used in CB-HBT circuit. The edge of the SET (larger orange dot) is roughly 100 nm away from the quantum dot (smaller orange dot). (b) SEM image of the Si-MOS device used in the AC-HBT circuit. The proximity of the SET to the double quantum dot system is 50% further away at roughly 150 nm.

gate layout affects the mutual capacitance between the SET and the quantum dot. More capacitive coupling results in larger changes in the electrochemical potential of the charge-sensor for a given quantum dot charging event [51]. Since changes in electrochemical potential of the charge-sensor result in changes in current through the charge-sensor, larger changes result in a larger signal. Therefore, more mutual capacitance leads to larger readout signals, faster readout times, and higher readout fidelity.

The gate geometry used in the Si-MOS device connected to the CB-HBT had the SET 33% closer to the quantum dot than in the Si-MOS device connected to the AC-HBT. The closer SET proximity in the CB-HBT resulted in an increase in sensitivity of approximately 34%. The sensitivity of both circuits is compared by dividing the voltage shift of the dot occupancy transition by the charge-sensor Coulomb blockade peak period. For the CB-HBT, the voltage shift was 18 mV and the charge-sensor period was 337 mV (5.34% change). For the AC-HBT, the voltage shift was 12 mV and the charge-sensor period was 350 mV (4% change). Therefore, the SET in the

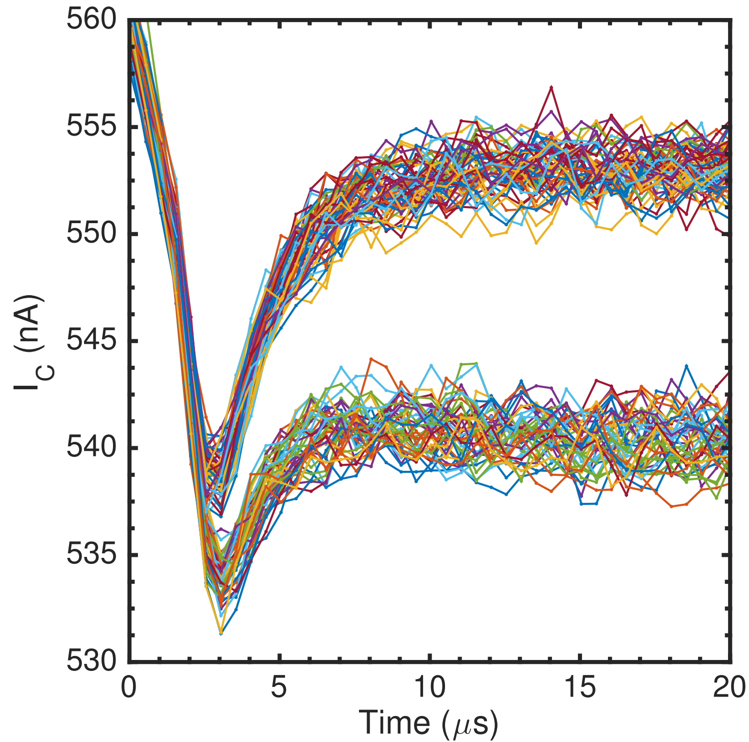

Figure 6.6: CB-HBT Single-Shot Readout Traces
100 single-shot traces for the CB-HBT charge readout. Slower response time is compensated for by larger signal separation at earlier times relative to the AC-HBT readout.

CB-HBT was around 34% more sensitive to charging events than the AC-HBT.

6.7 Current-Biasing Effect of CB-HBT Circuit

Since the node that connects the SET source to the HBT base is floating, the bias across the SET cannot be set to a fixed voltage in the CB-HBT circuit. Verilog-A models were created to simulate the behavior of the circuit when biasing the SET through multiple regions of Coulomb blockade via an electrostatic gate. As the SET resistance changes due to Coulomb blockade, the source-drain bias across the SET changes to allow current to flow into the base of the HBT (Figure 6.7(b)). In

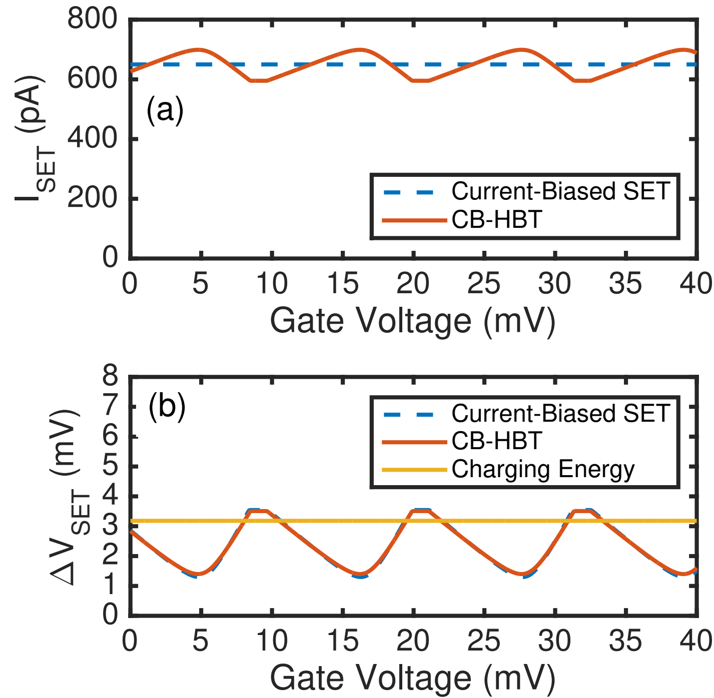

Figure 6.7: Current-Biasing Effect Model
Comparison of CB-HBT and current-biased SET Verilog-A models. The top plot shows the drain current of the SET as a function of gate voltage. The current is modulated much less in this condition than in a constant voltage-biased circuit. The bottom plot shows voltage across the SET as a function of gate voltage. The overlap between the two curves shows that the CB-HBT circuit is effectively equivalent to current-biasing the SET.

order for this to happen, the HBT trades base-emitter voltage for minimal impact to operation. Although the trade in voltage results in a relatively small change in HBT collector current during, for example, a single-shot readout event, this signal is approximately 100 larger than the SET source-drain signal without an HBT (e.g., $\Delta I_C = 10$ nA vs. $\Delta I_{SET} = 100$ pA).

The Verilog-A model estimates the small signal resistances as: $r_{set} = 200$ kΩ and $r_\pi = 10$ MΩ (where r_π is the small signal resistance of the base-emitter junction).

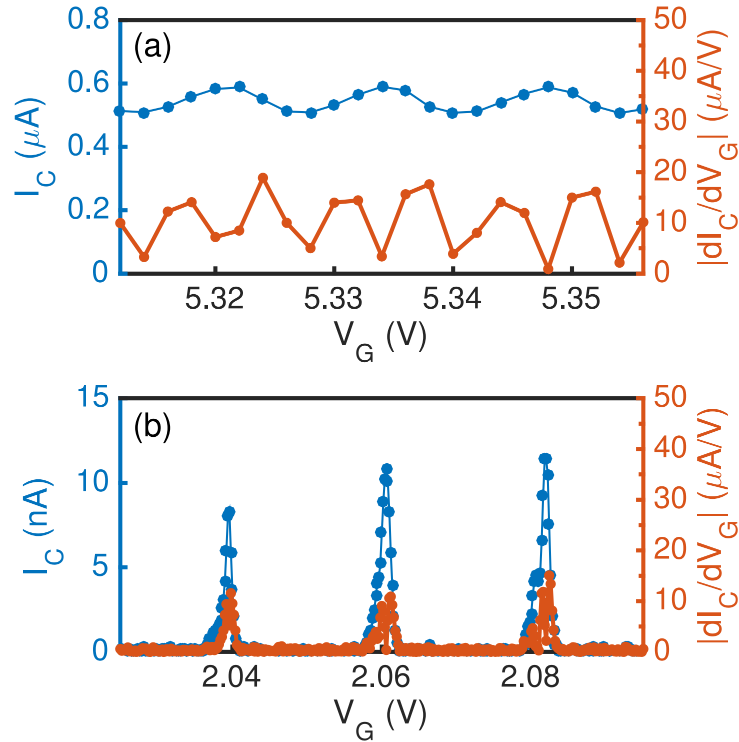

Figure 6.8: Current Biasing Effect Signal and Sensitivity Comparison
(a) Coulomb blockade peaks for the CB-HBT (blue). The absolute value of the sensitivity is plotted as orange points. Since there is almost always a positive or negative blockade slope, the absolute value of the sensitivity remains positive for most of the range plotted. (b) Coulomb blockade peaks for the AC-HBT (blue). The absolute value of the sensitivity is plotted as orange points as well.

Most of the emitter bias voltage is across the base-emitter junction at all times (since $r_{set} << r_\pi$), therefore the CB-HBT is a current-biasing circuit. The current-biasing behavior is highlighted in Figure 6.8(a), where three Coulomb blockade peaks are plotted. For comparison, three Coulomb blockade peaks are plotted for the AC-HBT case (Figure 6.8(b)). The CB-HBT amplified peaks are broadened by the current-biasing effect and the blockade region never reaches zero current as it would with a smaller constant voltage bias. The AC-HBT amplified peaks are much narrower and minimally broaden due to having a constant, small voltage bias regardless of HBT

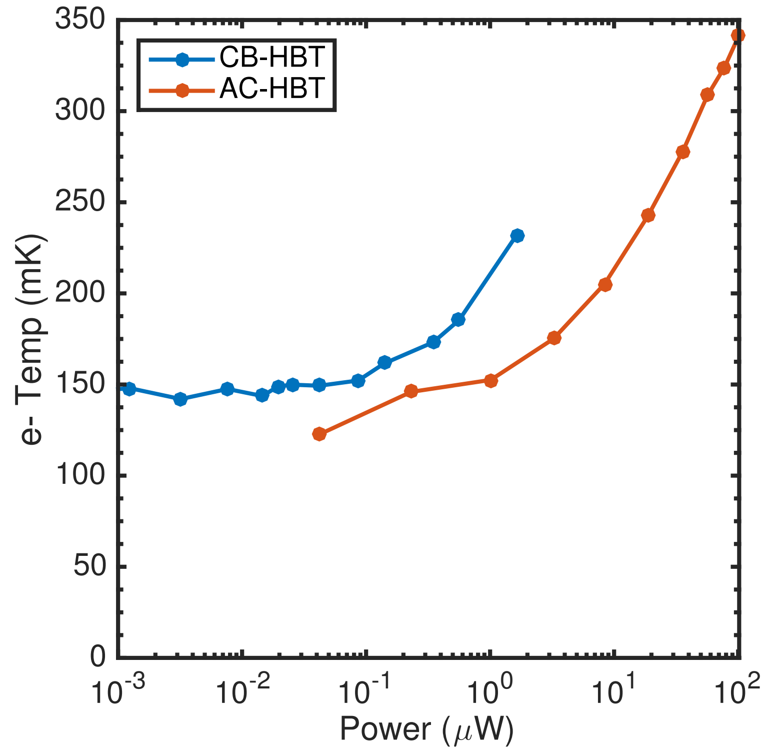

Figure 6.9: Electron Temperature Comparison
Electron temperature vs. power for both circuits. Base temperatures are between 120–150 mK. Both circuits operate in the 160–200 mK range for single-shot data taken.

power. Comparable sensitivities can be achieved for either circuit around 10 μA/V.

6.8 Electron Temperature Measurement

Heating of electrons in the quantum dot due to the operation of the connected HBT is a concern, therefore the dependence of electron temperature on HBT amplifier bias (Figure 6.3(e)) is examined. For the CB-HBT, The electron temperature of the QD was measured by extracting the width of a Coulomb blockade peak as a function of fridge temperature. The QD was tuned to a transport regime where the QD was

approximately equally tunnel-coupled to both reservoirs and there were around 10 electrons in the QD. The source-drain bias was reduced to 5 μV_{rms} to avoid bias heating. A Coulomb peak was chosen where a minimum width was observed in Coulomb diamond measurements. After extracting the lever-arm of the gate used to measure the broadening (13 μeV/mV), it is found that the minimum linewidth yields an electron temperature around 150 mK. Heating of the QD begins where the CB-HBT is operating with over 100 gain, therefore the CB-HBT circuit can amplify well while heating the electrons to 160–200 mK.

For the AC-HBT setup, the base electron temperature was around 120 mK. This is confirmed by the measurements of the electron temperature when measuring the SET signal directly through the shunt resistor (R_S in Figure 6.1(a)) with the HBT turned off. With the HBT on, The electron temperature is deduced by measuring the Fermi-Dirac linewidth of the (1,0)-(2,0) charge transition. When the AC-HBT bias is increased up to 3.24 μW, the electron temperature remains near the base temperature (Figure 6.9). For powers above this threshold, the electron temperature increases approximately linearly with power. This might be due to local heating of the PCB and wires, which increase the temperature of the nearby device [157]. No effort has been made to heat sink the AC-HBT in this experiment, so further tests with various heat sinking options will be performed to minimize the increase in electron temperature. Nonetheless, an electron temperature of 200 mK is achieved for the bias condition that provides the minimum amplifier noise.

6.9 HBT Characterization

Before being used in either amplification circuit, HBTs are initially characterized in liquid helium at 4 K using PCBs with eight HBTs mounted on them. It is found that HBT performance at 4 K—particularly current gain vs. base current—changes

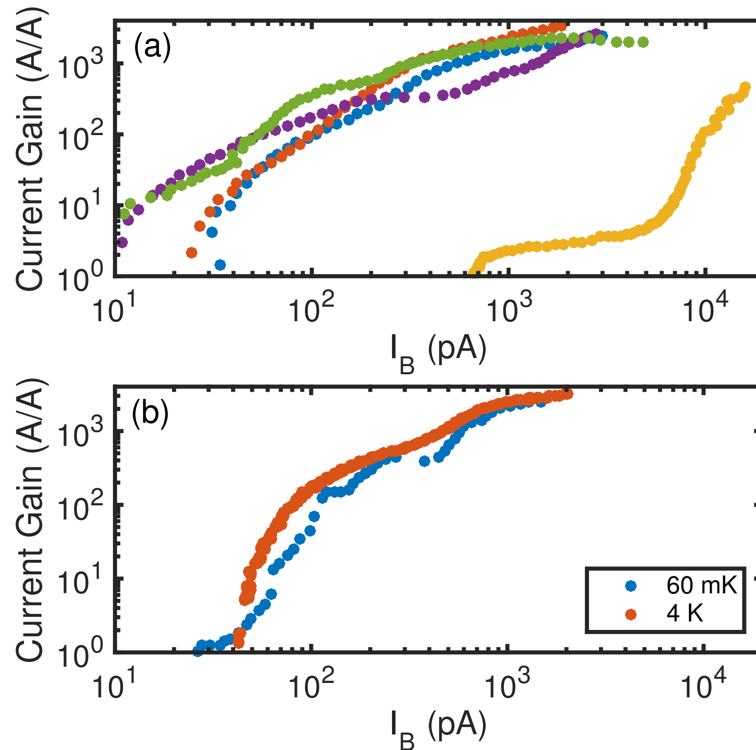

Figure 6.10: HBT DC Characterization

(a) Example plots of current gain vs. base current for different HBTs. Several curves reach current gain > 1000 for base currents < 500 pA. The HBT corresponding to the yellow curve is subpar since it requires base current > 10 nA to reach current gain < 1000. (b) Current gain vs. base current at different temperatures for HBT used in the CB-HBT circuit. There is a slight difference in the two curves, however, the performance at 60 mK is enough to efficiently amplify and perform single-shot readout.

minimally when HBTs are cooled down to 20–60 mK in a dilution refrigerator (Figure 6.10(b)). This is most likely due to the charge-carrier transport mechanism changing from a drift-diffusion regime (temperature dependent) to a tunneling regime (barrier dependent) at around 30 K [153].

In order to characterize HBTs, Keithley 2400 source-measure units are used as current meters and connected to the HBT base and collector terminals. A power supply (emitter bias) is connected to the HBT emitter terminal and used to bias the HBT to different operating regimes. The emitter bias has to reach approximately -1 V for the HBT to begin operating in an amplifying regime. As the emitter bias is changed from -1.00 V to around -1.07 V, the collector and base current begin to increase exponentially. The current gain, defined by dividing the collector current by the base current, also increases exponentially as emitter bias changes.

Previous measurements without HBT amplification circuits indicate that the SET current should be below several hundred pA in order to avoid QD electron heating. For the CB-HBT, HBTs are selected based on their current gain at low base currents. Around 20% of HBTs characterized will have a current gain $>$ 100 at base current $<$ 200 pA (Figure 6.10(a)). For the AC-HBT, the transconductance ($\mathrm{g_m}$) is the only metric required for selection. Since the HBTs were fabricated with $\mathrm{g_m}$ as a primary metric, $>$ 80% of HBTs are usable for the AC-HBT circuit even at low temperatures. However, $\mathrm{g_m}$ does not scale ideally in these HBTs at cryogenic temperatures. For a given HBT, $g_m \propto I_C^n$, where $n = 1$ in normal conditions. In the HBTs used in this work, $n \approx 0.8$, which leads to suboptimal SNR at higher power.

6.10 CB-HBT Small Signal Gain

The gain of the CB-HBT is calculated using a standard BJT small-signal model. A small voltage fluctuation at the base node is usually converted to a large current

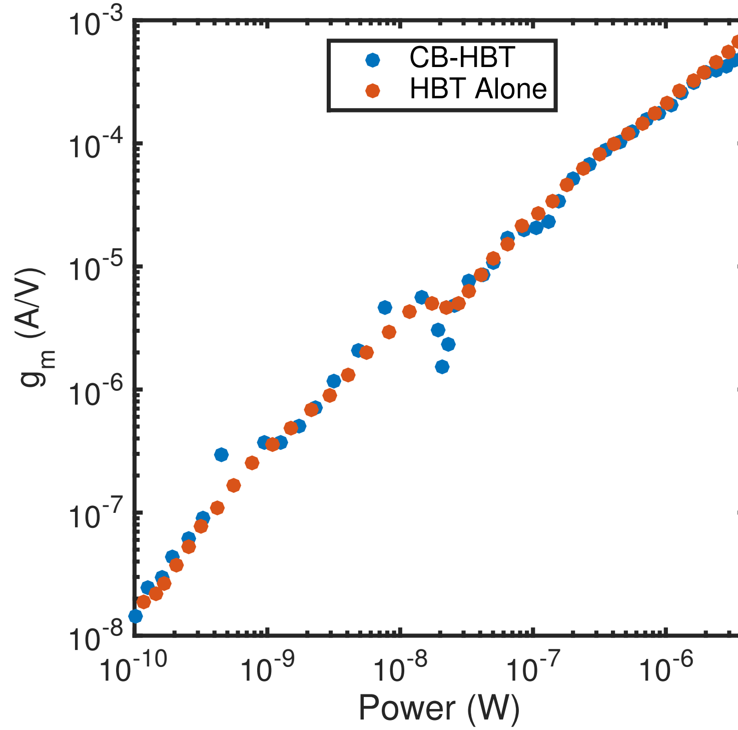

Figure 6.11: Transconductance of HBT With and Without SET Connected Transconductance vs. power for the CB-HBT (SET connected to HBT) and the same HBT without an SET connected. The data overlaps for both cases, therefore the transconductance can be reliably measured directly in the CB-HBT (assuming $r_{set} \ll r_{\pi}$).

fluctuation at the collector node by the transconductance, $\mathrm{g_m} = \frac{di_c}{dv_{be}}$. This voltage fluctuation is usually the small-signal base-emitter junction resistance, $\mathrm{r_\pi}$, multiplied by the base current. However, in the case of the CB-HBT, $r_{set} \,||\, r_{\pi}$, therefore the parallel combination of the two resistances is required to calculate gain:

$$\text{gain} = \frac{i_c}{i_{set}} = g_m(r_{set} \,||\, r_{\pi}). \tag{6.1}$$

6.11 Noise Models

Sources of noise in the HBT amplification circuits include: shot noise, Johnson noise, triboelectric noise associated with the coaxial lines coupled to fridge vibration [66], room temperature amplifier noise, and other instrumental noise. At relatively low power operation regimes ($< 1\ \mu$W for the AC-HBT and < 200 nW for the CB-HBT), the noise due to vibrations in the fridge dominates at around 1 pA/$\sqrt{\text{Hz}}$. The input noise spectral density of the room temperature amplifier is relatively low (100–500 fA/$\sqrt{\text{Hz}}$), therefore noise sources much more dominant are focused on. When either circuit is operating in a regime appropriate for single-shot readout, the base shot noise is greater than the collector shot noise (Figures 6.1(e) and 6.2(e)). For the SET shot noise, in either case, a Fano factor is not considered, which would reduce the noise for a given power [158, 159]. The total noise for either circuit is calculated by assuming noise sources are independent processes and adding noise sources in quadrature.

Noise modeling for the CB-HBT circuit is nontrivial because of the current division at the HBT base node since $r_{set} \ll r_\pi$. The SET and base current are reduced to a Norton equivalent circuit, and the HBT is reduced to $\mathrm{r_\pi}$ connected to a current source which takes voltage fluctuations ($\mathrm{v_{be}}$) across $\mathrm{r_\pi}$ and converts them to collector current via the transconductance, $\mathrm{g_m}$. For the CB-HBT, the noise model is a shot noise current source ($i_{b-shot} = \sqrt{2\, e\, I_B\, \Delta f}$, where I_B is the DC base current, and Δf is the bandwidth centered on frequency f) in parallel with $\mathrm{r_{set}}$ and $\mathrm{r_\pi}$ (Figure 6.12(b)). Since $r_{set} \ll r_\pi$, most of the shot noise current goes through the SET to the ground, and a much smaller amount enters the HBT base and is amplified. The amplified base shot noise is shown in Equation 6.2:

$$i_{\text{b-shot-amp}} = i_{\text{b-shot}}\ \text{gain} = i_{\text{b-shot}}\ g_m\ (r_{set}\,||\,r_\pi). \tag{6.2}$$

This amplified base shot noise is estimated in Figure 6.2(e) as the orange curve where

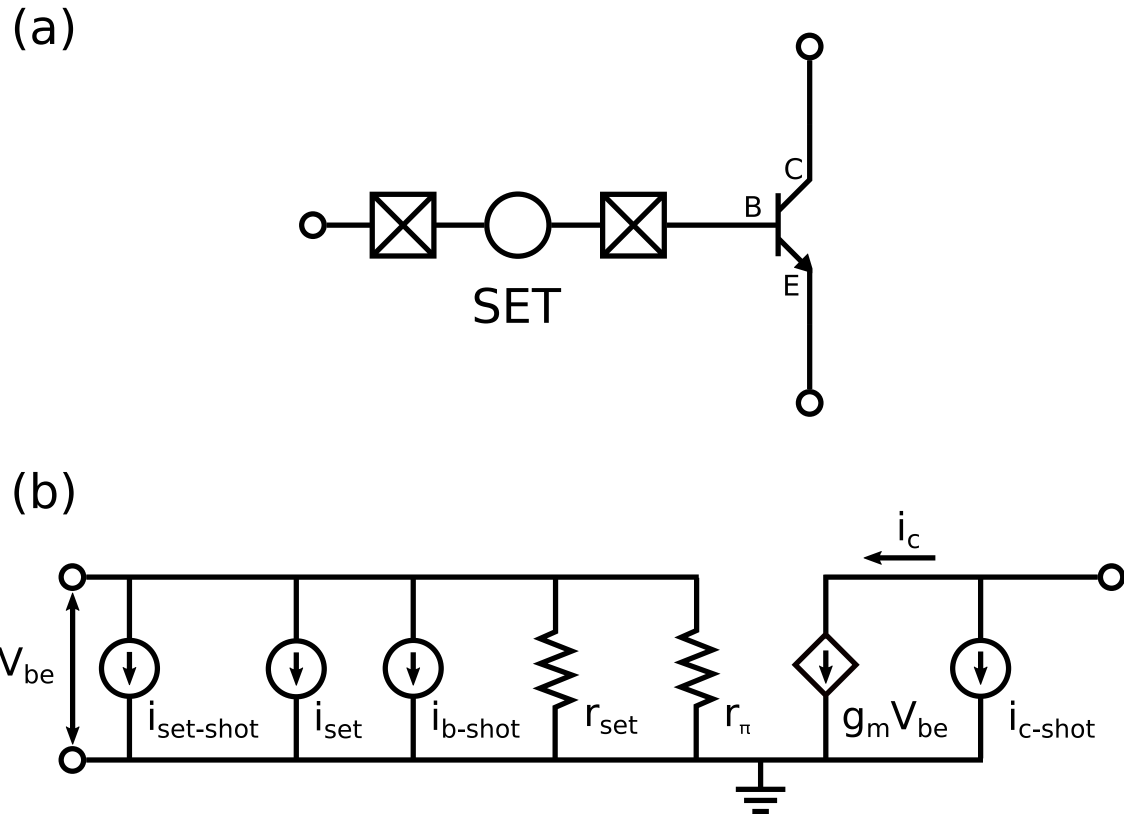

Figure 6.12: CB-HBT Circuit Model
(a) CB-HBT circuit schematic for reference. (b) CB-HBT effective circuit model. The shot noise current source, $i_{b\text{-}shot}$, is in parallel with r_{set} and r_π. Most of the shot noise does not enter the base of the HBT because $r_{set} << r_\pi$. The signal, i_{set}, is also shown, which is amplified according to Equation 6.1.

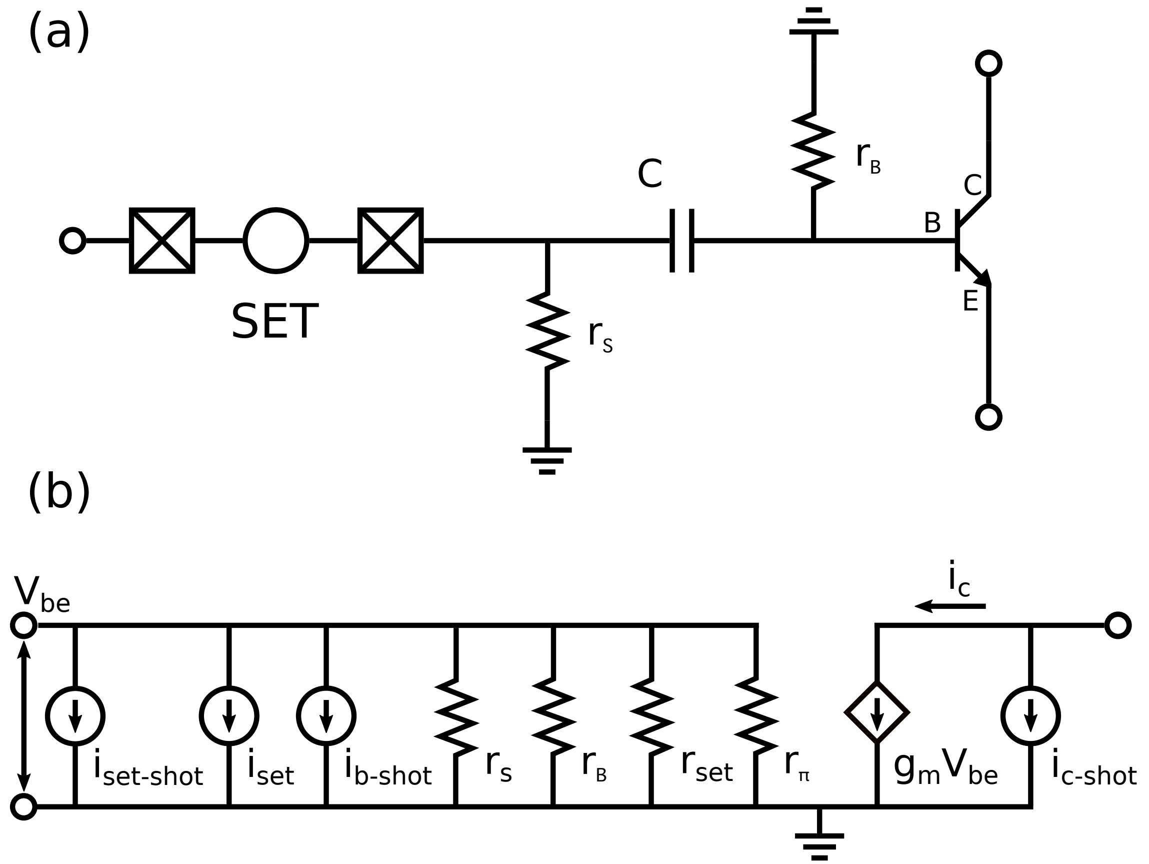

Figure 6.13: AC-HBT Circuit Model
(a) AC-HBT circuit schematic for reference. (b) AC-HBT effective circuit model with signal, i_{set}, also shown. The model is similar to the CB-HBT with two new resistors added in parallel: r_S and r_B.

g_m and r_π are calculated from Gummel plots of the HBT and r_{set} is assumed to be 3 MΩ, which was verified in later measurements with the HBT disconnected from the Si-MOS device.

The noise model for the AC-HBT is similar to the CB-HBT with r_S and r_B added in parallel to r_{set} and r_π. The coupling capacitor, C, is considered a short at the frequencies appropriate to model noise in the AC-HBT. The Johnson noise of R_S in the AC-HBT circuit is $v_{s-jn} = \sqrt{4\, k_B\, T\, R_S\, \Delta f}$ (where T is the temperature) and does not contribute significantly in the single-shot operation regime. Since the AC-HBT has a separate current to bias the base-emitter junction, $I_{SET} \neq I_B$, therefore the base shot noise and SET shot noise are considered separately. However, $I_{SET} < I_B$, so the base shot noise is always dominant in amplifying regimes.

6.12 AC-HBT Bias Tee Parameters

The bias tee parameters for the AC-HBT were chosen to be R_S = 100 kΩ and C = 10 nF, which sets a high pass filter at 160 Hz. Operating the circuit at frequencies higher than 160 Hz aids in avoiding higher noise levels at a lower frequency due to 1/f-like noise behavior in the system. The shunt resistance value is chosen to be less than r_{set} (100s of kΩ) so that most of the SET bias voltage drops across the SET.

6.13 CB-HBT Circuit Effective Gain Method

This section contains the first method that was used to estimate the CB-HBT gain. Essentially, the slope of the current in the CB-HBT charge sensor is divided by the slope of the current in the AC-HBT charge sensor with the AC-HBT gain divided out. The idea is to extract the CB-HBT gain by assuming that the slope of the current in

the CB-HBT charge sensor is similar to the equivalent slope in the AC-HBT. This method was accurate within a factor of two or three. The main assumption that was made was the charging energy of the charge sensor in the CB-HBT (which was not able to be measured directly).

Since it is difficult to directly measure r_{set} in the CB-HBT, the sensitivity of the SET in the CB-HBT is referenced to the sensitivity of the SET in the AC-HBT instead. To make a fair sensitivity comparison, the SET current-vs-voltage slope is converted to current-vs-energy slope via the lever arm of the appropriate electrostatic gate. For the SET in the CB-HBT circuit, the lever arm was calculated using the fact that the charge-sensor peaks are separated by about 81 mV and by assuming a charging energy of 2 meV from a similar device tuned to a similar regime. The current-vs-energy slope of the SET in the AC-HBT circuit was 2 pA/μeV.

Equation 6.3 shows the calculation of the effective gain as a function of HBT power. $\text{gain}_{CB}(P)$ is the small signal gain of the CB-HBT and $m_{CB}(P)$ is the slope of the Coulomb blockade in the CB-HBT, where $\text{gain}_{CB}(P)m_{CB}(P)$ can be directly measured. $\alpha_{CB/AC}$ is the lever-arm of the appropriate gate in either circuit.

$$\text{gain}(P) = \frac{\text{gain}_{CB}(P)\, m_{CB}(P)\, \alpha_{CB}^{-1}}{m_{AC}\, \alpha_{AC}^{-1}}. \tag{6.3}$$

6.14 Conclusion

The performance of two cryogenic amplification circuits is compared (the CB-HBT and the AC-HBT). The power dissipated by the CB-HBT ranges from 0.1 to 1 μW, whereas the power of the AC-HBT ranges from 1 to 20 μW. Referred to the input, the noise spectral density is low for both circuits and is measured to be around 15 to 30 fA/$\sqrt{\text{Hz}}$. The charge sensitivity for the CB-HBT and AC-HBT is 330 μe/$\sqrt{\text{Hz}}$ and 400 μe/$\sqrt{\text{Hz}}$, respectively. For single-shot readout performed, both circuits achieve

SNR > 7 and bit error rate $< 10^{-3}$ in times less than 10 μs.

Chapter 7

Conclusion

7.1 Summary of Results

The work in this dissertation focuses on improving the readout of singlet-triplet qubits in silicon. Chapter 1 covered the history of classical computers and why it is important to move forward with the development of quantum computers. In Chapter 2, background material was introduced for understanding semiconducting qubits. The chapter started with a discussion on semiconducting devices beginning with the MOSFET device. Then the definition and formation of quantum dots were introduced with several measurement techniques outlined. Next, the singlet-triplet qubit was covered along with its operation and measurement. Finally, a review of the current semiconducting readout techniques was done with the focus on cryogenic amplification and its benefits. Chapter 3 covered the experimental methods used to tune and operate the singlet-triplet qubits in this work. This included tuning the tunnel rate to the reservoir for reliable qubit initialization, minimizing electron temperature, verifying the energy scales via magnetospectroscopy, tuning the tunnel coupling between the quantum dot and donor, and performing readout to characterize

the benefits of cryogenic amplification. Chapter 4 focused on the Si-MOS devices fabricated at Sandia National Laboratories for improving the single-electron regime tunability. One contribution from this dissertation was simulations of the devices used to verify the tuning orthogonality between the quantum dot occupancy and the tunnel rate, which lead to a co-authored paper [70]. Chapter 5 showed the initial design and results from a SiGe HBT amplifier circuit, the CB-HBT, at 4 K. The amplifier was characterized by increasing the frequency of the input signals as well as monitoring random telegraph signal as the bandwidth of the room temperature amplifier was increased. This work led to a first-author publication [63]. Finally, in Chapter 6, the CB-HBT circuit is compared to a circuit using a previous AC-coupled circuit design [6], the AC-HBT. The HBT amplification circuits are characterized by performing single-shot latched charge readout. The chapter starts by describing the differences between the two circuits. Then, a comparison of noise, bandwidth, power, and electron temperature is done to highlight the performance differences between the two circuits. Finally, single-shot results are compared and both circuits are able to perform high-fidelity readout, improving upon performance without a cryogenic amplifier and leading to a manuscript currently in preparation.

Through this work, an HBT that operates cryogenically has been identified. A novel non-linear design, the CB-HBT, has been examined and compared to a linear, AC-coupled approach, the AC-HBT. The two amplification circuits can operate at powers between 1 and 10 μW and not significantly heat electrons, which is a critical early concern for amplification within the dilution refrigerator. The noise spectral density referred to the input for both circuits is around 15 to 30 fA/$\sqrt{\text{Hz}}$, which is low compared to previous cases such as the dual-stage, AC-coupled HEMT circuit at $\sim$ 70 fA/$\sqrt{\text{Hz}}$ [6]. Both circuits achieve charge sensitivity between 300 and 400 μe/$\sqrt{\text{Hz}}$, which approaches the best alternatives (e.g., RF-SET at $\sim$ 140 μe/$\sqrt{\text{Hz}}$) but with much less implementation overhead. For the single-shot latched charge readout performed, both circuits achieve high-fidelity readout in times < 10 μs with

bit error rates $< 10^{-3}$, which is a great improvement over previous work with readout time > 70 μs [5]. All of these results are possible with relatively simple transistor circuits which can be mounted close to the qubit device at the mixing chamber of the dilution refrigerator.

7.2 Outlook

The readout times quoted in Chapter 6 (9 μs and 6 μs) are an improvement relative to not using any cryogenic amplification. However, faster readout times may be possible and should be sought after. For high-fidelity readout, the decay time of the excited state can be tuned to order of 10 ms. This decay time is sensitive to the tunnel coupling optimization for the qubit and often can be faster than 1 ms. If this decay time cannot be tuned and is less than 10 ms in the future, then faster readout times will be necessary to even achieve the same low readout error rates. The parasitic capacitance at different locations is believed to limit the bandwidth and thus the measurement time of these circuits. Minimizing the parasitic capacitance at the die level and elsewhere is a possible future direction. Transistors with higher transconductance or DC current gain for similar base currents would also improve performance.

It is an open research question what the long term extensibility is for these amplifiers. For example, scalable RF dispersive readout schemes are garnering significant attention currently [160, 161]. Nevertheless, a two-dimensional array of charge sensors on a layer near the qubits is a promising possibility for scalable semiconducting readout and can even take advantage of cryogenic amplification [162, 163]. An overall consequence of this work has been the frequent adoption of cryogenic, single-transistor amplification in the SNL group as well as reports around the world [4, 6, 152, 153, 163–170]. The work also spurred interest in improving T < 1 K SiGe

HBTs and understanding the underlying physics [153]. It is likely that cryogenic, single-transistor amplifiers will be an active research area for many years.

Appendix A

HBT Background

The concept of heterojunction bipolar transistors (HBT) began in the 1950s [171]. An HBT is a type of bipolar junction transistor (BJT) which uses different semiconducting materials (e.g., silicon and silicon-germanium) for its junctions. In contrast, a standard BJT typically uses only one type semiconducting material (e.g., silicon) to form a device consisting of a p-type "base" region (holes as charge-carriers) surrounded by an n-type "collector" region (electrons as charge-carriers) and a heavily-doped n-type "emitter" region (electrons as charge-carriers). The p-type and n-type regions form two p-n junctions with depletion regions: the base-emitter junction and the base-collector junction. The depletion region has the opposite charge of the bulk charge-carriers (e.g., positive charge in the n-type region), therefore an electric field is formed which repels holes and electrons from the depletion region. The depletion region decreases in size when a p-n junction is forward biased and eventually allows current to flow, since the repelling electric field also decreases in magnitude. The depletion region increases in size if a p-n junction is reversed biased and prevents current from flowing. Figure A.1 shows a schematic of the basic operation of a BJT with both energy band diagrams and semiconducting material diagrams. The idea is to modulate electron diffusion through the p-type region by changing the voltage bias

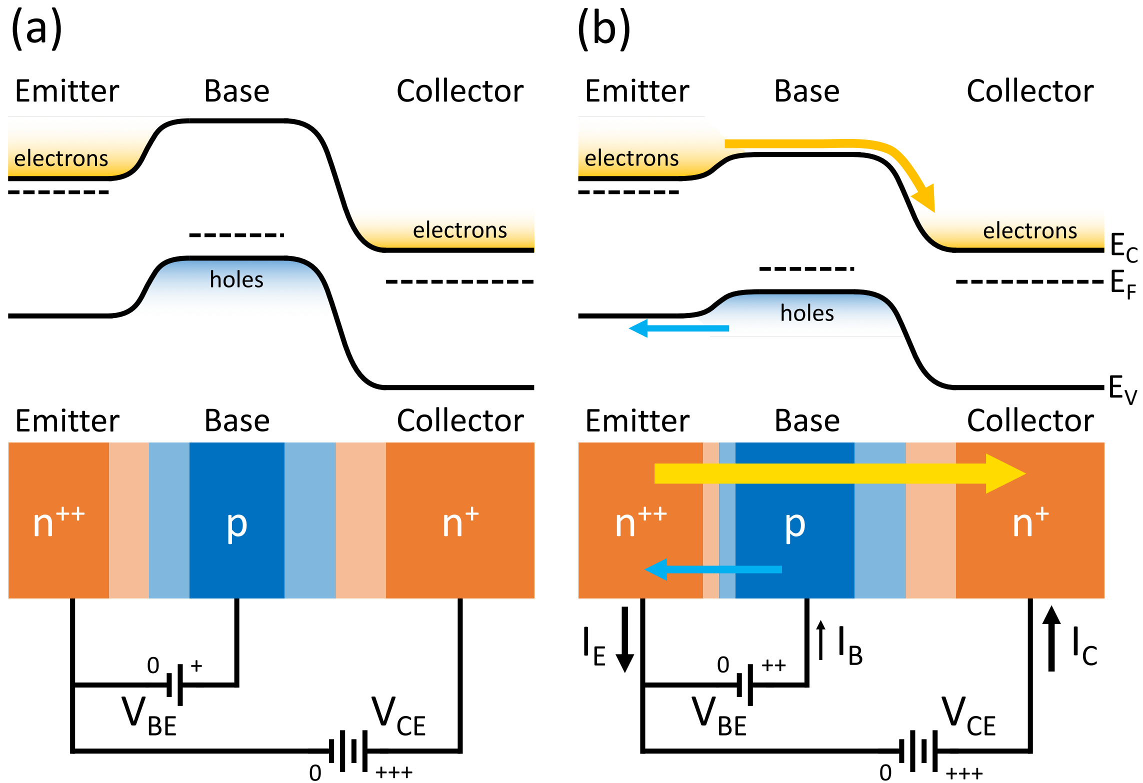

Figure A.1: BJT Operation

Schematic showing basic BJT operation. The upper part depicts band diagrams and the lower part shows semiconducting material diagrams with depletion regions portrayed in lighter colors. In the energy band diagrams, electron occupancy is depicted in orange (with occupancy dictated by a Fermi-Dirac distribution, e.g., Equation 2.2), and hole occupancy is shown in blue. Note that an equivalent picture for holes would be to have less electron occupancy below the valence band edge (white near the edge becoming orange lower in energy). (a) The base-emitter junction does not have sufficient bias to inject electrons into the base and cause current to flow. (b) The base-emitter junction has sufficient bias for current to flow. The electrons diffusing into the base region are able to enter the collector region without significantly recombining with holes. The holes entering the emitter recombine with electrons as they do in a standard semiconducting diode. Electron movement is shown with orange arrows, and hole movement is shown with blue arrows.

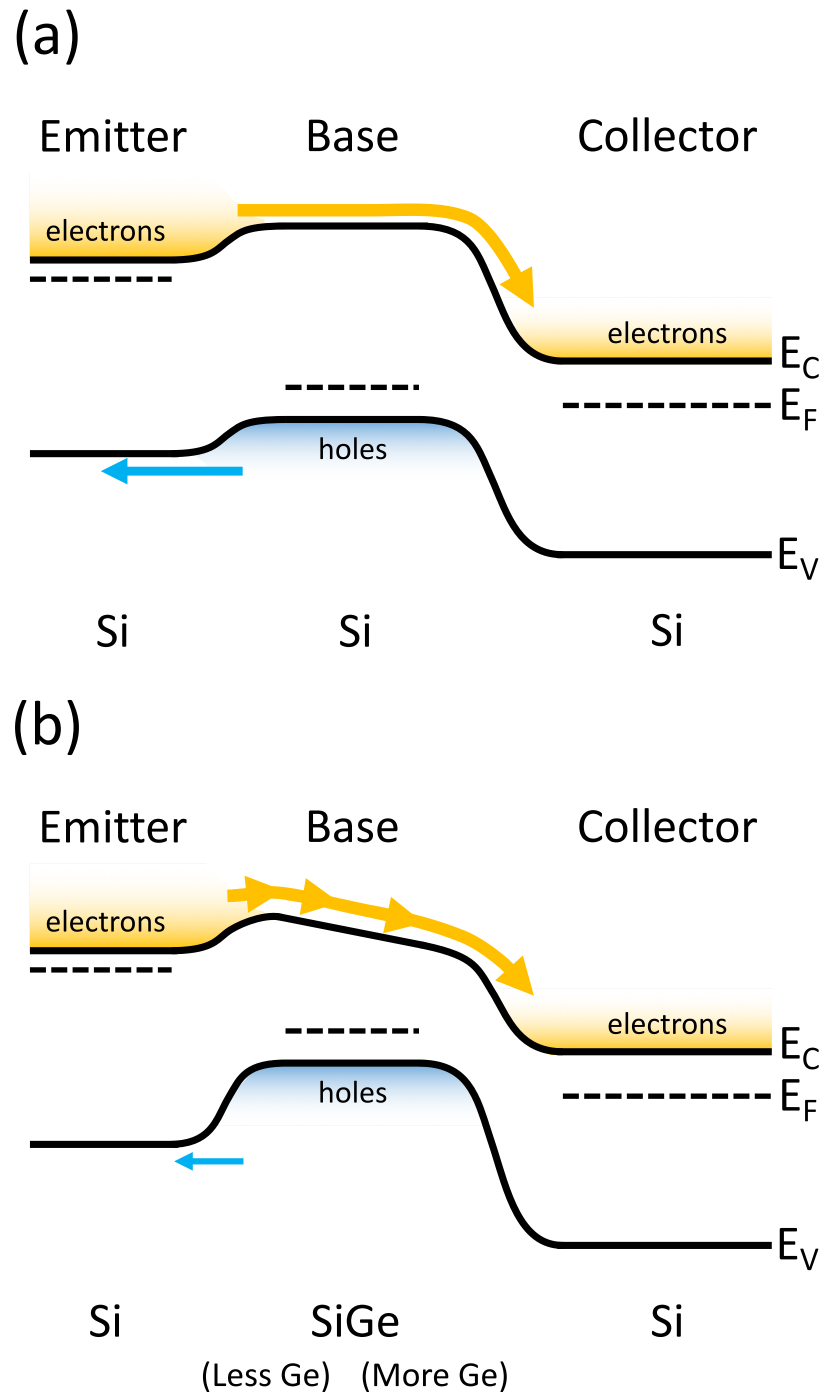

Figure A.2: BJT and HBT Band Diagrams
Band diagrams for a silicon BJT and a SiGe HBT. Features are exaggerated to highlight the conceptual differences between a BJT and an HBT. (a) Silicon BJT band diagrams. (b) SiGe HBT band diagrams.

of the base relative to the emitter. By changing the base-emitter bias, the width of the depletion region between the base and emitter junctions changes and modulates injection of electrons into the base region (and eventual diffusion to the collector region). The collector-base junction is reverse biased to allow a much lower energy path for electrons diffused through the base region to drift to. Figure A.1(a) shows the condition where no current flows since there is not sufficient base-emitter bias to allow electrons to diffuse. When there is sufficient base-emitter bias, the depletion region is decreased such that the electric field no longer prevents electrons from diffusing into the base region. Figure A.1(b) shows the condition where electrons diffuse into the base region and drift into the collector region. A small amount of electrons recombine with holes in the base region, which can be minimized by making the base region thin relative to the diffusion length of the electrons (typically micrometers).

HBTs operate similarly to BJTs with several key differences. Typically, the emitter and collector use a larger bandgap material than the base (e.g., silicon at 1.12 eV, and germanium at 0.66 eV). This is done to decrease the difference between the conduction band edges and increase the difference between the valence band edges in the base and emitter regions. The result is that more electrons are injected into the base for less base current. Also, the doping in the base region can be increased, therefore, the resistance of the base region can be decreased. Finally, the ratio of germanium to silicon in the SiGe base region can be increased from the emitter side to the collector side. This results in the conduction band edge lowering relative to the valence band, and the electrons in the base will experience an effective electric field [128]. Transport speed through the base is increased, therefore, the bandwidth of the transistor is increased. Figure A.2 shows the differences in the band structure between a silicon BJT and SiGe HBT. The features previously mentioned are exaggerated to show the conceptual differences.

Low temperature operation of an HBT changes the conceptual picture in several

ways. Since the HBT can be heavily doped and still have high current gain and high transconductance, carrier freeze-out does not occur at cryogenic temperatures. For temperatures as low as $\sim$ 30 K, the Fermi-Dirac distribution of the charge-carriers tightens such that more forward base-emitter bias is required to allow for electron diffusion into the base. It is believed that at temperatures less than $\sim$ 30 K the transport mechanism of the electrons moving through the base changes from the standard drift-diffusion mechanism to a tunneling mechanism [153]. Base-emitter bias now modulates the height of an effective tunnel barrier separating the emitter from the collector. The tunneling mechanism is not temperature dependent, therefore, the performance characteristics of the HBT fortuitously stay similar from 4 K to 60 mK (Figure 6.10(b)).

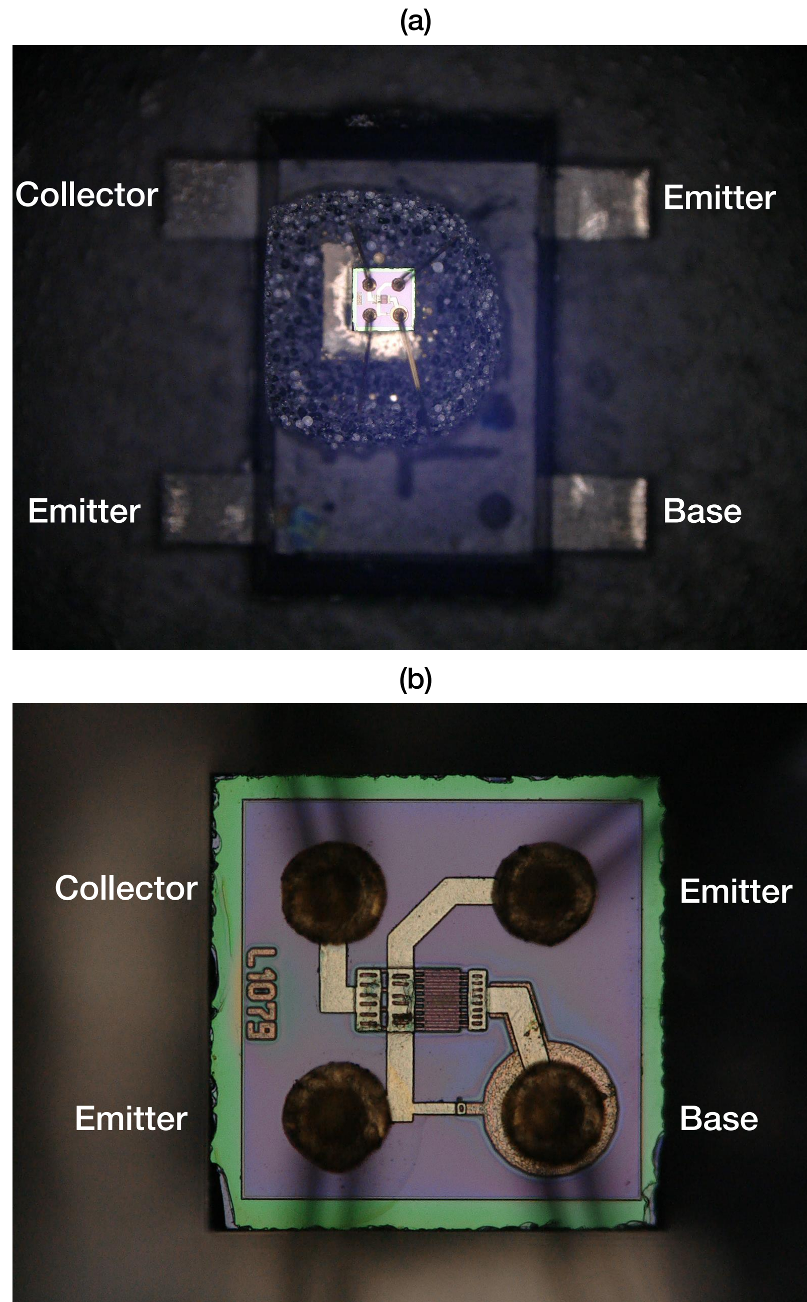

Figure A.3: Decapped HBT
Images of equivalent HBT model used throughout this dissertation with protective epoxy removed (decapped). (a) Image of entire decapped HBT (top view). (b) Closeup of decapped HBT showing the surface of the transistor.

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