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Optimising heat flow in wide and ultra-wide bandgap devices

Optimising heat flow in high performance wide and ultra-wide bandgap devices

The application of diamond in heat spreading.

By

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ABSTRACT

Wide and ultra-wide bandgap materials are able to give the high performance necessary for applications such as LIDAR and wide bandwidth communications. These applications result in high power densities that must be managed, making innovative heat extraction techniques vital. In this work, heat flow and diamond heat spreading solutions are studied in novel device designs fabricated in GaN, AlGaN, and $\beta - Ga_2O_3$ to ensure that these materials can be utilised to their full potential.

GaN-on-diamond material properties are studied through nanoparticle assisted Raman thermography and transient thermoreflectance. Seeding and growth conditions are shown to impact the thermal properties, with an optimal seed size suggested to be $\approx$ 50 nm. The impact of GaN buffer thickness on GaN-on-diamond device operating temperature is assessed using photoluminescence. Excellent electrical performance and thermal resistances as low as 9 ± 1 K/(W/mm) are demonstrated in devices with a buffer thickness of 354 nm.

Superlattice castellated field effect transistors are efficient RF switches, but power density is localised periodically along the gate. The operating temperature of these devices was found through micro-Raman thermography, gate resistance thermometry, and finite element simulations. The 3D gate was found to aid heat flow by providing a high thermal conductivity heat pipe; the devices have a thermal resistance of 19.1 ± 0.7 K/(W/mm) which is similar to that of GaN-on-SiC devices.

The first thermal study of $\beta - Ga_2O_3$ devices is presented, with a thermal resistance of 88 ± 3 K/(W/mm) found, as well as the first study of it's phonon lifetimes. Devices fabricated in low thermal conductivity materials such as $\beta - Ga_2O_3$ will need innovative thermal management. This is explored using simulations, with a diamond passivation layer recommended.

Dedication and acknowledgements

I would like to begin by thanking my fiancée Sarah for her support, and her patience, through this writing process. I am sure I have not been easy to live with, and Sarah kept me well supplied with tea and snacks. Similarly, I would like to thank all my family and friends who were supportive during the writing process and didn't get offended when I turned down invitations because 'sorry, I'm writing'.

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AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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CHAPTER 1

INTRODUCTION

1.1 Development of high power, high frequency transistors

Solid state electronics have been integral to our way of life since the invention of the first point contact transistor at Bell Laboratories in 1947 [1]. That work is most commonly attributed to Shockley, Brattain, and Bardeen, and was followed by a bipolar junction transistor orginally made in germanium due to its lower melting point and higher carrier mobility when compared to silicon, which earned the trio the Nobel prize in physics in 1956 [2]. However germanium's low bandgap (0.67 eV) gave high leakage currents and hence came the first silicon bipolar transistor, developed independently at both Bell Laboratories and Texas Instruments [3]. The theory for Field Effect Transistors (FETs) actually preceded these first transistors, and can be dated back to Lilienfeld in 1928 and then Shockley and Pearson in 1948 [4, 5]. However it was not until 1953 that Dacey and Ross showed the first unipolar FET using germanium. Khang and Atalla then developed the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in silicon in 1960, an enabling technology for Complimentary Metal Oxide Semiconductors (CMOS) on which so much of the worlds computing relies today [6].

Although silicon transistors continue to be imperative in our lives, alternative materials with improved fundamental properties have been sought since the early days of the transistor. GaAs

technology was used as an alternative for high frequency operation as its electron mobility is almost 6 times higher than that of silicon [7, 8]. MOSFET technology is not compatible with all compound semiconductors as the lack of a native oxide often led to surface traps at the gate, meaning new architectures were required. As a result, the first GaAs MEtal-Semiconductor Field Effect Transistor (MESFET) was fabricated by Mead in 1965, utilising a Schottky gate contact [9]. The desire for higher frequency operation also led to the development of the High Electron Mobility Transistor (HEMT) in GaAs by Mimura *et al* in 1980 [10]. In these devices, the formation of a 2 Dimensional Electron Gas (2DEG) at the interface of a GaAs-AlGaAs heterostructure leads to an enhancement in the electron mobility [11].

Interest in Wide BandGap (WBG) materials developed from the desire for higher power, higher temperature operation. Silicon's 1.1 eV bandgap means that the thermal activation of carriers, which follows an Arrenhius relationship with respect to bandgap, is significantly larger than in materials such as wurtzite gallium nitride (GaN) and 4H silicon carbide (SiC), which have bandgaps of 3.4 eV and 3.2 eV respectively at room temperature [7, 12–14]. The wider bandgap of these materials affords them higher critical fields which allows for higher voltage operation and increased power densities [15]. Of these two WBG materials SiC has the advantage in thermal conductivity with a value of up to 450 W/m.K, compared to 160 W/m.K for GaN [16]. However, issues remain with the cost efficient production of high quality SiC due to basal plane dislocations, although in spite of this 15 kV devices are currently used in power conversion [17]. GaN has an advantage in that heterostructures can be created with AlGaN to allow for the fabrication of HEMTs. This, coupled with its larger bandgap make it ideal for both high power and high frequency applications [18]. In the high power electron device sector, GaN HEMTs will compete with SiC FETs and silicon Insulated Gate Bipolar Transistors (IGBTs) as an enabling technology in fields such as electric vehicle power transformation and high speed charging [19].

An ideal transistor has zero resisitance when it is on, and zero current when it is off. It should also be able to withstand infinite electric fields such that it can block whatever voltage necessary, and to switch between off and on instantaneously. As all materials have a finite breakdown voltage, when exceptionally high voltages must be blocked it is often accomplished in stages, which increases the switching inefficiencies in the circuit. Whilst all wide bandgap materials

can operate at higher voltages, GaN offers low ON-resistance and faster switching because of its heterostructures [20]. Ultimately, the maximum operating voltage of GaN power devices is limited by the available GaN buffer thickness, which in turn is limited by the shortage in native substrates. The use of non-native substrates leads to an inherent stress in the GaN layers, meaning there is a critical thickness above which the GaN cracks and delaminates.

In the RF sector GaN technology has been available since 2005, originally on sapphire substrates until SiC substrates were shown to enable devices to operate at significantly higher powers [21, 22]. Whilst GaAs HEMTs perform well at high frequency, the wide bandgap of GaN allows for smaller device footprints and higher operation temperatures [23]. In addition to this, GaN's high mobility allows for higher frequency operation. This makes GaN the material of choice in high power Ku and Ka band applications such as LIDAR, high bandwidth communications, and military uses [18, 24, 25].

However GaN device reliability continues to be a concern. The high drain voltages and small device dimensions result in extremely high electric fields which peak at the gate edge, causing mechanical stress due to GaNs piezoelectricity and activating a range of trap states which degrades device performance [26, 27]. This peak in electric field also causes a local maximum in the power dissipation and temperature. It is important to understand the device channel temperature as device efficiency is impacted by ON resistance and threshold voltage, both of which are temperature dependent. The Mean Time To Failure (MTTF) of a device is also temperature dependent, following the Arrenhius relationship

$$\mathrm{MTTF} = A \exp \frac{-E_a}{k_b T}, \tag{1.1}$$

where A is a constant of proportionality, E_a is the activation energy of the lowest energy failure mechanism which can be thermally induced, k_b is the Boltzmann constant and T is the channel temperature [28, 29]. Because of this, to ensure the reliability of GaN devices the maximum operating conditions are often de-rated.

The desire for higher and higher power densities, either through increased operating voltage or reduced device footprint, makes near junction thermal management necessary to utilise devices to their full capacity and avoid temperature related accelerated breakdown. Heat extraction from

the channel is impeded by low thermal conductivity materials such as the interfaces between epitaxial layers or the epitaxial layers themselves, and their effect can be minimised either by changing the device design or introducing high thermal conductivity elements to aid in heat spreading.

Diamond is often considered as the ideal candidate to assist in effective heat spreading due to is wide bandgap and high thermal conductivity which is the highest known in a bulk material at over 2000 W/m.K [30]. However, the integration of diamond with other WBG semiconductors is non-trivial as there is often a large mismatch in coefficients of thermal expansion, and diamond is also incredibly stiff [31]. In 2010 Francis *et al.* demonstrated the first four inch GaN-on-Diamond wafer with polycrystalline diamond grown onto the GaN as the substrate material [32]. The grain boundaries present in polycrystalline diamond mean it has a somewhat reduced thermal conductivity when compared to single crystal diamond, meaning it is not as efficient at heat spreading. Wafer bonding of single crystal diamond substrates onto GaN has been attempted, although this has not been scaled up to large areas and often results in poor thermal boundary resistances [33–35]. Currently the state-of-the-art GaN-on-polycrystalline diamond devices have a thermal resistance of 10 K/(W/mm), compared to 19 K/(W/mm) for GaN-on-single crystal diamond, and 15 K/(W/mm) for GaN-on-SiC [35, 36].

Whilst the use of diamond is most commonly as a substrate for heat spreading in high power dissipation devices, this is not the only way diamond can be used. Reduced temperatures were demonstrated by Tadjer *et al.* in GaN HEMTs where nanocrystalline diamond films were grown as a passivation layer, before the deposition of the gate [37]. However, they found that the ON-resistance of these devices increased, which was attributed to the diamond putting the channel under tensile stress and creating a non-uniform 2DEG density [38]. Nanocrystalline diamond which has been heavily boron doped has also been used to create a rectifying gate contact which provides decreased on resistance and off state leakage, but also induces a negative threshold voltage shift and adds little in terms of heat spreading due to its small volume [39].

As GaN has entered a more commercial stage in its life cycle, academic research has adjusted to study "generation after next technology", primarily ultra-wide bandgap materials (UWBG) [40]. The major contenders in this field are diamond, gallium oxide (predominantly in its β polymorph)

and AlGaN HEMTs (an $Al_{1-x}Ga_xN$ buffer with AlN heterojunction) [30]. Diamond-based devices have long been proposed as the ultimate in power electronics due to the combination of UWBG and exceptional thermal conductivity, however devices have been held back due to a lack of low level dopants and low mobilities [41, 42]. To get around this, attempts have been made to create diamond HEMTs through surface transfer doping and nanometric delta doping. Power dissipation is not likely to be an issue in such devices [43, 44], but power dissipation is likely to be an issue for both AlGaN and $\beta - Ga_2O_3$ devices as both have low thermal conductivities with respect to other semiconductors. In the case of AlGaN, alloy scattering reduces the phonon mean free path and hence the thermal conductivity, with values of approximately 20 W/m.K for alloying concentrations greater than 10% [45]. $\beta - Ga_2O_3$ has an anisotropic thermal conductivity which is 27 W/m.K along the [010] direction and 10 W/m.K otherwise [46].

The main theme of this work is understanding and thereby improving the thermal performance of novel FETs by measuring and simulating their temperature profiles. The goal is to aid device development such that they can be utilised efficiently and reliably in an industrial environment. The GaN-on-diamond interface is a key component of wafer epitaxies; if this thermal bottleneck were removed devices would be able to be operated at significantly higher power densities, making them more economically viable. This work improves the understanding of what causes the interface effective thermal boundary resistance, how it can be improved, and how it must be considered in device design. For new materials or devices which are aiming to enter the market it is important that their thermal performance is studied such that reliability concerns can be addressed. Two device structures which have not been thermally characterised are investigated, the superlattice castellated FET and the $\beta - Ga_2O_3$ MOSFET. Both device sets have thermal challenges which must be addressed. The particular problems are identified, and recommendations made for the next generation of device sets.

1.2 Thesis outline

To understand the heat flow in novel FET designs, micro-Raman thermography, nanoparticle assisted Raman thermography, and photoluminescence will be used to probe active device tem-

peratures. These measurements will then be combined with finite element simulations of device structures to provide an insight into how the devices behave thermally and to understand their peak temperatures. Finite element simulations will also be used to explore how diamond can be used most effectively with the latest UWBG materials. An understanding of key material parameters in WBG and UWBG systems will also be established by the use of Raman thermometry and transient thermoreflectance.

Chapter 2 will focus on the theoretical background of this work. Phonons and their origins are discussed. The inherent properties, growth, and applications of GaN, AlGaN, $\beta - Ga_2O_3$, and diamond, the key materials in this work, will be discussed. Each material has its own advantages and challenges that make it suitable for certain applications, and interesting for research and these will be highlighted. A discussion of heat transport will then follow, with reference to the specific nature of heat flow in device structures.

Chapter 3 will explore the experimental techniques utilised in this work, discussing both their theory and laboratory implementations. The two major experimental techniques utilised are Raman scattering, which is used for both spectroscopy and thermography, and photoluminescence, which is also used for thermography. Transient thermoreflectance, which is used for material characterisation, is also explained. Finally the underlying principles behind finite element analysis are discussed. This is used as a tool to further the understanding gained from experimental results, and must be optimised to make the process accurate and efficient.

Following this will be the research segment of this work. Chapter 4 studies how GaN-on-diamond material and devices can be optimised. Transient thermoreflectance is used to measure the effective thermal boundary resistance of GaN-on-diamond systems. Nanoparticle assisted Raman thermography will be employed to measure the temperature profile of suspended thin diamond films which allows for the thermal conductivity of the film to be determined through comparison with finite element simulations. Following this, the thermal resistance of two GaN-on-Diamond wafers which have different buffer thickness is determined. Photoluminescence is performed to determine the temperature in the device active area, before finite element analysis is used to determine the device peak temperature. The results show that using ultra-thin buffer layers of as low as 350 nm is not detrimental to device performance. As effective thermal boundary

resistances are optimised, thinner buffers have the ability to offer improved thermal and electrical characteristics.

Chapter 5 discusses thermal transport in SuperLattice Castellated FETs (SLCFETs), of which there are no thermal examinations in the literature. The small feature sizes and localised power dissipation in SLCFETs makes heat extraction more complex. Raman thermography is used to measure their buffer temperatures, whilst gate resistance measurements are used to measure gate temperatures. These measurements are used as an input to a finite element simulation of the structures, highlighting how the three dimensional gate structure aids thermal transport by providing a high thermal conductivity heat pipe through to the device buffer.

Finally, Chapter 6 studies the UWBG materials AlGaN and $\beta - Ga_2O_3$. The lifetimes of certain optical phonons in $\beta - Ga_2O_3$ are determined using Raman spectroscopy. The likely decay mechanisms of these phonon's modes is found by studying the temperature dependence of the lifetime. Nanoparticle assisted Raman thermography is used to show the high thermal resistance of $\beta - Ga_2O_3$ devices. Finite element simulations will then be used to investigate how diamond can be used to address the challenge of efficient heat extraction in these low thermal conductivity materials.

CHAPTER 2

MATERIAL AND DEVICE THEORY

For the analysis of heat transport in high performance electronic devices it is necessary to understand the nature of heat flow, how this is impacted by the materials and device structures used, and how the heat is generated. A discussion of heat flow in metals, semiconductors and amorphous materials is provided, as well as a more in depth discussion on the properties of phonons; the primary heat carrier in semiconductors. For each of the semiconductors studied in this work, the microscopic and macroscopic properties are explored. A discussion of the relevant growth processes and device designs follows this, considering the industrially relevant aspects which impact their use. Finally, these are amalgamated for a discussion on how the device structures generate heat and how this is spread throughout a wafer containing both high and low thermal conductivity elements.

2.1 Phonons and heat transport

2.1.1 Phonon theory

Phonons are quasiparticles used to describe quantised lattice vibrations. They are a useful tool for understanding heat flow in solids, as heat itself is energy stored in crystals, often through vibrations. Consider an infinite, one-dimensional, monatomic lattice as demonstrated in Figure

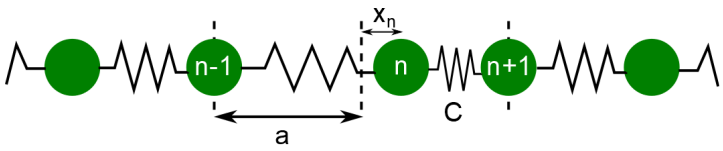

FIGURE 2.1. A sketch of a monatomic 1D lattice with the atoms shown in green and the bonds represented by springs with spring constant C. The atomic spacing is a, and the atom n is displaced by an amount x_n

.

2.1 where each atom is a point mass, the bonds are represented by springs of constant C, and the atoms only interact with their nearest neighbour. If the n^{th} atom is at position x_n Newton's second law of motion states that the force of displacement F on this atom is

$$F = m\frac{d^2x_n}{dt^2}, \tag{2.1}$$

where m is the atom's mass. For the central mass of a linear 3 mass system connected by springs, Hooke's law states that the force on this atom will be

$$F = C(x_{n-1} - x_n) - C(x_n - x_{n+1}) = C(x_{n+1} + x_{n-1} - 2x_n) \tag{2.2}$$

where the subscripts $n-1$ and $n+1$ refer to the preceding and proceeding atoms in the chain respectively. By equating Equations 2.1 and 2.2 there results a second order differential equation in x_n

$$m\frac{d^2x_n}{dt^2} = C(x_{n+1} + x_{n-1} - 2x_n). \tag{2.3}$$

By substituting in a trial wave solution of

$$x = Ae^{i(kna-\omega t)} \tag{2.4}$$

where A is the wave amplitude, a is the inter-atomic spacing, ω is the frequency of the wave, and k is the wavevector, the differential equation takes the form

$$-\omega^2 m e^{i(kna-\omega t)} = C(e^{i(k(n+1)a-\omega t)} + e^{i(k(n-1)a-\omega t)} - 2e^{i(kna-\omega t)}). \tag{2.5}$$

By cancelling the common terms in the exponentials this reduces to

$$-\omega^2 m = C(e^{ika} + e^{-ika} - 2). \tag{2.6}$$

Using Euler's formula to simplify the right hand side and rearranging for the frequency gives

$$-\omega^2 = \frac{C}{m}(2\cos(ka) - 2) = \frac{-2C}{m}(\sin^2(\frac{ka}{2})), \tag{2.7}$$

where the final step employs the cosine double angle formula. Hence solving for frequency gives the dispersion relation

$$\omega = \sqrt{\frac{2C}{m}} \mid \sin\frac{ka}{2} \mid \tag{2.8}$$

confirming the wave like nature of lattice vibrations in crystals, and it is these waves that are named phonons [47].

The Brillouin zone is a tool commonly used in crystallography and the definition of phonons. It is the reciprocal space equivalent of the Wigner-Sietz unit cell in that it defines the smallest repeating unit in the reciprocal lattice. As it is in reciprical space, the size of the Brillouin zone is given in terms of wavevector $k = \frac{2\pi}{\lambda}$ where λ is the wavelength. The Γ point is always considered the centre of the unit cell where $k = 0$, and other high symmetry reciprocal lattice directions are denoted by letters. The wavevector-frequency dispersion curves in the Brillouin zone are shown in Figure 2.2 (a). In the one-dimensional, monatomic case considered here the Brillouin zone has width $k = \frac{\pi}{a}$. From Equation 2.8 the phonon frequency is zero at the Γ point, at its maximum at the Brillouin zone edge, and is repeating in 2π. Phonons of this nature are named acoustic phonons [48].

When a diatomic lattice is considered, the differential equation shown in Equation 2.3 becomes a paired system of two differential equations of the same form. The solution to these equations in matrix form is

$$\begin{bmatrix} 2C - m_1\omega^2 & -2C\cos ka \\ -2C\cos ka & 2C - m_2\omega^2 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} = 0 \tag{2.9}$$

where the subscripts distinguish between the properties of the different atoms of the lattice. There are non-zero solutions to this equation system when the determinate of the matrix on the left hand side is zero, i.e when

$$(2C - m_1\omega^2)(2C - m_2\omega^2) - (-2C\cos ka)^2 = 0. \tag{2.10}$$

This can be rearranged to

$$\frac{m_1 m_2}{2C}\omega^4 - (m_1 + m_2)\omega^2 + 2C(1 - \cos^2 ka) = 0 \tag{2.11}$$

which is a quadratic equation in ω^2 and hence can be solved by the quadratic equation giving solutions of

$$\omega^2 = C(m_1^{-1} + m_2^{-1}) \pm C\sqrt{(m_1^{-1} + m_2^{-1})^2 - \frac{4sin^2ka}{m_1 m_2}}. \tag{2.12}$$

This adds an extra branch of solutions to the earlier discussed acoustic phonons as shown in Figure 2.2 (b). At the Γ point the second term under the square root is zero, resulting in

$$\omega_\Gamma = \sqrt{C(m_1^{-1} + m_2^{-1}) \pm C(m_1^{-1} + m_2^{-1})} \tag{2.13}$$

which gives zero when the minus sign is taken but is non-zero when the positive sign is taken. These phonons which have non zero energy at the Γ point are named optical phonons. They can have energy at the Brillouin zone centre as they represent a symmetric oscillation of the two atoms about their lattice point, meaning there is no long range translation. It is these optical phonons that are of interest later in this work as Raman scattering, one of the primary techniques used, probes zone centre phonons. Optical phonons also have higher energy than acoustic phonons as they have higher frequencies, meaning they are the primary heat carrier at room temperature. As is implied by Equation 2.12, the phonon dispersion is still symmetrical about the Γ point although the Brillouin zone now has width of $k = \frac{\pi}{a}$, as the two atom system means the unit cell of the 1D lattice now has length $2a$. As the complexitiy of the lattice is increased to more realistic systems, the solutions become more varied, but they are still separated into acoustic and optical phonons. The modes can also be longitudinal, oscillating in the direction of the bond, or transverse, oscillating normal to the direction of the bond and these will have different energies [49].

Another property of phonons which is important for thermal transport is that they have zero spin. This makes them Bosons and as such they obey Bose-Einstein statistics, meaning the population n of an energy level E is given by

$$n(E,T) = \frac{1}{\exp(E/k_b T) + 1} \tag{2.14}$$

where k_b is the Boltzmann constant and T is the temperature. As will be discussed in Section 2.1.2, heat transport in a material is dependent on the phonon population as phonons are the dominant heat carrier in many dielectric systems. As Bosons do not obey the Pauli exclusion

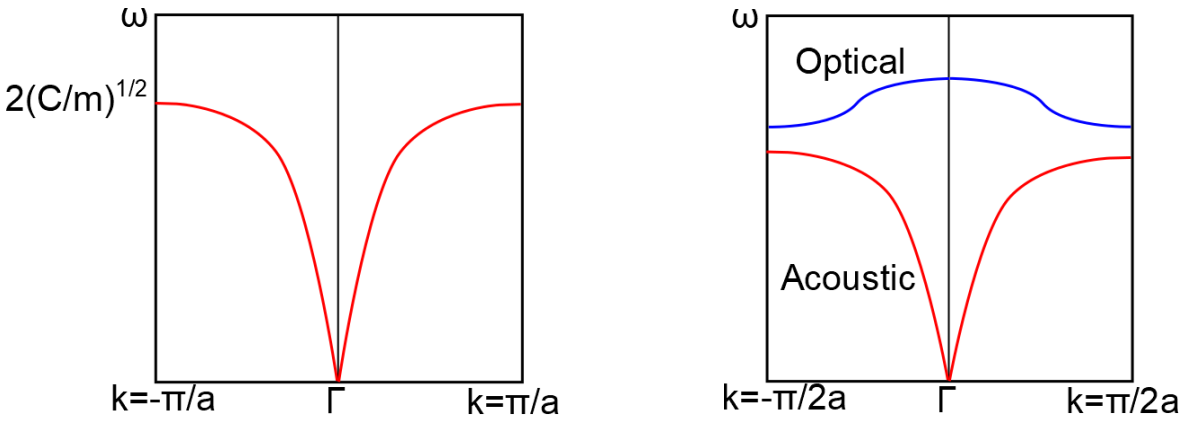

FIGURE 2.2. (a) The wavevector-frequency dispersion curve of a monatomic one-dimensional lattice in the Brillouin zone. (b) The dispersion curve of a diatomic one-dimensional lattice. There are now two phonon branches known as the acoustic phonons (red) which are linear close to the Brillouin zone centre, and the optical phonons (blue) which are non-zero at the zone centre.

principle they form a Bose-Einstein condensate as T tends to 0 K and hence n tends to zero. This means all phonons will accumulate in their ground state, meaning there will be no thermal carriers. As the temperature increases, the number of carriers increases following Equation 2.14. In the case where the thermal energy $k_b T \gg E$ the Bose-Einstein statistics approach the Rayleigh-Jeans law which states that

$$n = \frac{k_b T}{E} \tag{2.15}$$

suggesting that the phonon population, and hence the thermal carriers, will increase linearly with temperature.

This is of importance when considering the heat capacity of a dielectric material. Debye theory states that the specific heat capacity tends to a constant value of $3k_b$ at high temperatures. This value is found from the Dulong-Petit law and is derived from the equipartition theorem which states that the vibrations in all three axis directions will have thermal energy $k_b T$. This law holds at temperatures above the Debye temperature, which is defined as

$$T_D = \frac{hv}{2k_b}^3 \sqrt{\frac{6N}{\pi V}} \tag{2.16}$$

where h is Planck's constant, v is the sound velocity, N is the number of atoms, and V is is the

volume. The Debye temperature physically represents the temperature needed to excite the highest energy vibrational mode. Above this temperature, all the modes are activated and hence the specific heat capacity ceases to increase. However below this value, the specific heat capacity is temperature dependent following approximately a T^3 relationship as the occupation of the modes in three dimensions increases.

2.1.2 Heat flow in solids

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Phonons also play a crucial role in the thermal conductivity of semiconductors. The thermal conductivity of a material in one dimension x is defined as the κ which relates the heat flux in one dimension j_x to the temperature gradient in that direction via Fourier's law [50]

$$j_x = -\kappa_x \frac{dT}{dx}. \tag{2.17}$$

The thermal conductivity can be found by assuming that the quasiparticles carrying the heat in a solid, such as phonons in semiconductors and electrons in metals, act as an ideal gas [49]. These quasiparticles have a flux of nv_x where n is the number of particles per unit volume and v_x is their mean velocity. Now consider the situation where these particles are in an area of relative high temperature and are moving to an area of relative low temperature. Once they reach the low temperature area, each of these particles will possess energy equivalent to $c \times \Delta T$ where c is the heat capacity of a single quasiparticle and ΔT represents the difference in temperature between the hot and cold areas. For a particle that travels a distance d_x, this change in temperature will be the rate of change of temperature with respect to distance, multiplied by that distance, i.e

$$\Delta T = \frac{dT}{dx} \times d_x. \tag{2.18}$$

The flux of heat is the carrier flux multiplied by the carrier energy. Assuming the particles travel a distance l_x before they are scattered, the heat flux becomes

$$j_x = -nv_x c\Delta T = -nv_x c l_x \frac{dT}{dx}, \tag{2.19}$$

and by comparison with Equation 2.17 it can be seen that

$$\kappa = nv_x c l_x. \tag{2.20}$$

The heat capacity of the quasiparticle gas per unit volume C is given by $n \times c$ which gives

$$\kappa = \frac{1}{3} C v l, \tag{2.21}$$

when generalised to three dimensions [48]. Therefore changes in any of these parameters will result in changes in the thermal conductivity. The temperature dependence of a material's thermal conductivity can be explained through the temperature dependence of C, the heat capacity, and l, which is commonly referred to as the mean free path of the quasiparticle. This will now be discussed in more detail for metals, semiconductors, and amorphous materials.

Heat transport in metals

Metals are used as contacts and heat sinks in semiconductor devices and as such play a role in heat spreading in high power density electronics. In the case of ideal metals, thermal transport is dominated by free electrons. To understand the thermal properties of metals it is important to understand the energy population statistics of the electrons which are carrying the heat. As electrons are Fermions, they obey Fermi-Dirac statistics which state that the probability of an energy level E being occupied is given by

$$f(E) = \left(\exp\left(\frac{E - E_f}{k_b T}\right) + 1 \right)^{-1} \tag{2.22}$$

where E_f is the Fermi energy [47]. By definition, the Fermi energy is the energy level which has a 0.5 probability of occupation, as can be seen by setting $E = E_f$. In the case where $E \gg E_f$ the probability of occupation is effectively 0, meaning there are no electrons of sufficient energy to occupy these states. In the case of $E \ll E_f$ the probability of occupation is 1. An electron in one of these energy levels cannot be thermally excited, as all energy levels within $k_b T$ of its original energy level are also occupied and as electrons must obey the Pauli exclusion principle the electrons cannot be excited to an already occupied level. Therefore, only electrons which occupy an energy level within $\approx k_b T$ of the Fermi energy can be excited and the mean energy of thermally active electrons can be approximated as the Fermi energy. As both the Fermi energy E_f, and the electron effective mass m_e can be approximated as constant with respect to temperature, the electron velocity v_e can also be approximated as temperature independent due to the kinetic

energy relationship

$$E_f = \frac{1}{2} m_e v_e^2. \tag{2.23}$$

However, the remaining thermal conductivity parameters from Equation 2.21 are not temperature independent, meaning the thermal conductivity is not constant at all temperatures.

As temperature increases, so does the thermal energy and hence the number of thermally active electrons increases. As stated in Equation 2.20, the specfic heat capacity of the electron gas increases as the electron density in that gas increases since there are now more particles which can store energy. This results in an increase in the heat capacity of the metal with the relationship [48]

$$C \propto T. \tag{2.24}$$

This linear increase competes with the temperature dependence of the electron mean free path, which has two major contributing factors; electron-phonon scattering and defect scattering. At temperatures significantly lower than the Debye temperature of the material the optical phonon population is low meaning the electron scattering is dominated by lattice defects and the mean free path is approximately constant as the number of lattice defects is temperature independent [51]. Electron self scattering interactions are weak at all temperatures and therefore have minimal impact on the thermal conductivity. However as temperature increases and the population of the optical phonon modes increases, the electron-phonon interactions become significant. This causes a decrease in the mean free path with a T^{-2} dependence at low temperature which then saturates at T^{-1} once all phonon modes are activated. This T^{-1} dependence counteracts the heat capacity increase due to the activation of new carriers, resulting in an approximately constant thermal conductivity in metals at room temperature and above. In alloys, the secondary atoms are effectively defects, and as such they limit the electron mean free path resulting in a lower thermal conductivity [51].

Heat flow in semiconductors

In materials where there are few free electrons such as the wide and ultra-wide bandgap semiconductors which make up the majority of the devices studied in this work, the main method of heat transfer is through phonons. The thermal conductivity can still be approximated

by Equation 2.21 [47]. The heat capacity obeys Debye theory, which results in the thermal conductivity increasing rapidly at low temperatures as the phonon modes are activated, and the mean free path is limited by scattering from static defects or the boundaries of the material. As the temperature approaches the Debye temperature and the heat capacity is approximately constant, the phonon mean free path becomes limited by the interactions of the phonons with themselves. Phonon interactions in crystals must obey conservation of momentum, meaning their wavevectors during interactions are constrained. If two phonons of wavevectors $\vec{K_1}$ and $\vec{K_2}$ interact with each other, the wavevector of the resulting phonon $\vec{K_3}$ is given by the relationship

$$\vec{K_1} + \vec{K_2} = \vec{K_3} + \vec{G} \tag{2.25}$$

where $\vec{G}$ is a reciprocal lattice vector. The simplest type of scattering is called the normal process, shown in Figure 2.3, where $\vec{K_3}$ exists in the Brillouin zone and $\vec{G}$ is zero. This type of scattering does not inhibit heat transport as it is simply a linear combination of the momentums of the two orginal phonons [51]. However if $\vec{K_3}$ exists outside of the Brillouin zone it can be the case that $\vec{G}$ does not equal 0 and the wavevector of the resulting phonon is mapped back into the Brillouin zone. This scattering does inhibit the heat flow as the wavevector, and hence the momentum, of the resulting phonon is less than that of the two original phonons, and the non-zero $\vec{G}$ represents a contribution from the phonons to the momentum of the whole lattice. This is called umklapp scattering, with a visual representation shown in Figure 2.3, and it results in a thermal resistance [52]. Only phonons of high enough energy can scatter oustide of the Brillouin zone in this way, which is why there is limited umklapp scattering at low temperatures. As temperature rises the higher energy modes become occupied as described in Equation 2.14 and the phonon mean free path and hence the thermal conductivity sees an exponential decay. As the temperature approaches the Debye temperature all phonon modes are active and the umklapp scattering results in a T^{-1} decay [48]. It is this umklapp process which dominates at room temperature and above, and hence most material thermal conductivities in this work have a temperature dependence of close to T^{-1}, although the exponent is often larger than -1 as thermal expansion of the lattice also causes a decrease in the phonon velocity and four phonon process can contribute to a reduced mean free path [51].

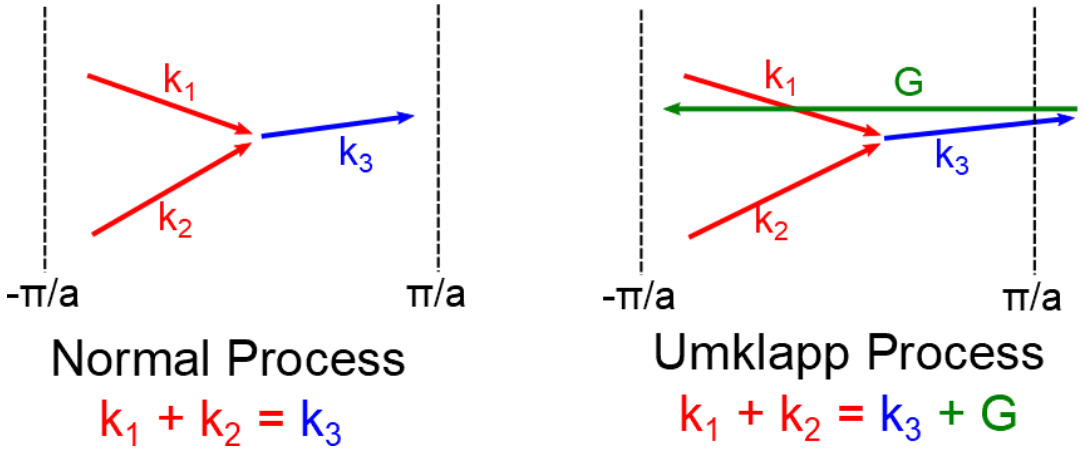

FIGURE 2.3. A visual representation of the normal phonon scattering process and the umklapp scattering process. The Brillouin zone is marked by the dashed lines. In the normal process there is no resistance to heat flow. In the umklapp process the phonons scatter outside of the Brillouin zone and interact with a lattice vector G, which inhibits heat flow.

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In this work diamond is studied as a passive heat spreader due to its exceptionally high thermal conductivity. More detail will be given on the properties of diamond in Section 2.4, but this high thermal conductivity is due to high phonon velocities v_p and long phonon mean free paths l_p, although the heat capacity of diamond is similar to many other semiconductors. The exceptionally high phonon velocities can be sustained as diamond's stiff bonds and low density which, when considering the Hooke's law approximation of bonding, gives a large 'spring constant' and restoring force [53]. These properties result in a phonon velocity which has been measured as high as 17500 ms^{-1}, which is 2× higher than in Si and 1.5× higher than in silicon carbide [54]. The long phonon mean free path is due to a low probability of umklapp scattering relative to other semiconductors. One model for the umklapp scattering frequency τ^{-1} is

$$\tau^{-1} = B\omega^2 T e^{-T_D/3T}, \tag{2.26}$$

where ω is the phonon frequency, T_D is the Debye temperature, and T is the temperature. The value B determines the likelihood of umklapp scattering, and can be approximated by

$$B = \frac{\hbar\gamma^2}{M v_p^2 T_D} \tag{2.27}$$

where M is the average atomic mass and γ is the Grüneisen parameter [55]. In addition to the large sound velocities possible in diamond, the Debye temperature is also relatively large. The

average Grüneisen parameter describes how the phonon properties vary with volume and for diamond is of a similar magnitude as for other semiconductors, making the overall umklapp scattering probability low [54].

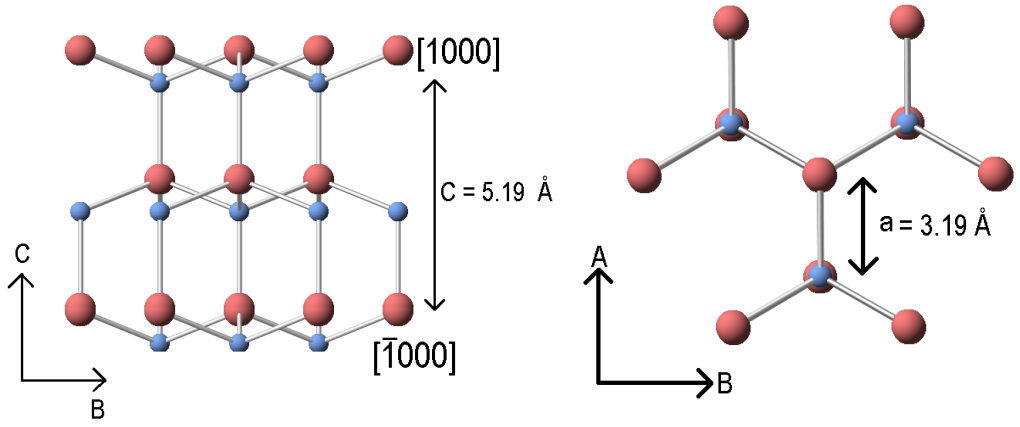
Heat flow in amorphous solids

In a device stack, amorphous materials such as silicon nitride are often used in passivation layers or gate dielectrics where they are adjacent to the heat source, and in interfacial layers to non-native substrates as their amorphous nature means they are insulating, preventing leakage currents, and they can conform to their surrounding structures [56]. In both cases, although the amorphous layer is very thin (nanometre scale), it can still pose a problem for heat flow as they have thermal conductivities of approximately 1 W/m.K. This low thermal conductivity is caused by the lack of long range order inherent in amorphous materials. The quasi-random arrangement of atoms means that phonons cannot be sustained over long periods, and electrons are still bound to their ion cores. This results in a lack of available heat carrying quasi-particles and instead the majority of heat diffuses through the material, which is a slower process [57].

2.2 GaN and AlGaN high electron mobility transistors.

2.2.1 Material properties

Gallium nitride (GaN) is a III-V compound semiconductor which is studied in this work as the buffer and channel material for HEMTs. It has a metastable zinc blende allotrope, but more commonly exists in a hexagonal wurtzite structure, shown in Figure 2.4, which is used for devices and hence will be the focus of the following discussion [58]. The wurtzite unit cell contains a pair of gallium atoms and a pair of nitrogen atoms with a bond length of 1.95 Å, a c parameter of 5.19 Å and an a parameter of 3.19 Å [59]. One of the key reasons that GaN is considered an exciting option for high performance electronics is that it has a wide bandgap of 3.4 eV, which is over 3 times that of silicon (1.1 eV) and two and a half times that of gallium arsenide (1.4 eV). A key property of the III-nitride semiconductors is that they can be alloyed together to give a continuous range of possible bandgaps ranging from the 0.7 eV of InN to the 6.2 eV of AlN



(a) (b)

FIGURE 2.4. Wurtzite structure of GaN with gallium atoms in red and nitrogen in blue. (a) shows the structure from the m-plane and (b) shows the structure from the c-plane.

[60]. This tunability has already made GaN a key opto-electronic material in LEDs, but it is also important in transistors as it allows for the formation of heterostructures [61]. GaN has a refractive index which varies from 2.25 in the far infra-red to 2.615 at its bandgap edge, which can make light extraction difficult [62].

The GaN band structure is shown in Figure 2.5. The curvature of the conduction and valence bands can be used to predict the mobility of the electrons and holes respectively, as carrier effective mass is proportional to the second derivative of the dispersion relation. Based on this it would be predicted that electrons are more mobile than holes, and that proves to be the case with reported electron mobilties in undoped GaN of 1150 $cm^2V^{-1}s^{-1}$ and hole mobilities of 170 $cm^2V^{-1}s^{-1}$ literature [63, 64]. These values are lower or comparable to narrow bandgap semiconductors such as silicon, germanium and gallium arsenide, but are higher than GaN's main wide bandgap competitor SiC, which has an electron mobility of 700 $cm^2V^{-1}s^{-1}$ [15]. Furthermore the AlGaN/GaN heterostructure, a key factor in high electron mobility transistors, gives an enhancement to these mobilities, and this will be discussed in more detail in Section 2.2.4.

The mechanical properties of semiconductors impacts the fabrication of hetero-epitaxial

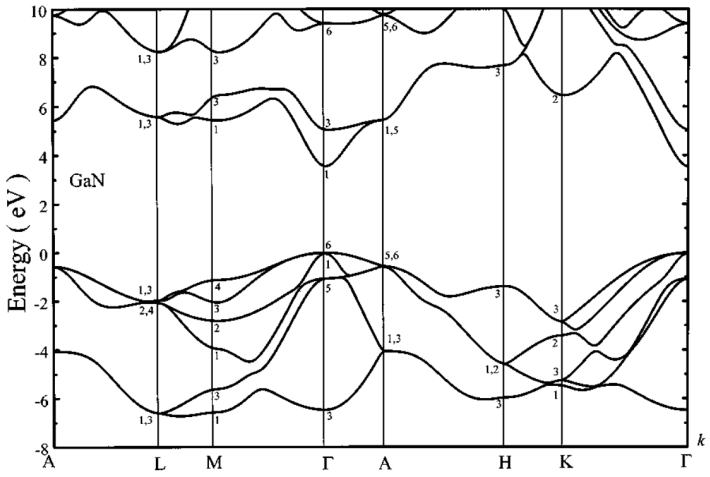


FIGURE 2.5. The electronic band structure of wurtzite GaN along high symmetry directions. There is a direct bandgap along the Γ direction of 3.4 eV. Image adapted from Yeo *et al.* [65]. Reprinted with permission from AIP Publishing.

wafers, where strain is often incorporated during the growth processes. GaN has a fracture toughness of 0.8 MPa.m$^{1/2}$ and a direction averaged Young's modulus of 287 GPa. The elastic constants of GaN suggest it is less stiff than AlN and BN, but is otherwise more stiff than most other compound semiconductors [66]. A more stiff material can be difficult to integrate with other semiconductors as it can result in greater amounts of strain at interfaces when they expand and contract at different rates. This is most commonly seen in wafer fabrication when the materials are integrated at high temperatures and have different coefficients of thermal expansions. GaN has a room temperature coefficient of thermal expansion of 3.95×10^{-6} K^{-1} in the a-plane and 3.53×10^{-6} K^{-1} in the c-plane, which is comparable with most compound semiconductors [15, 67].

The thermal conductivity of GaN was found to be heavily dependent on the dislocation density present in the material. Zou *et al.* found that below densities of $\approx 10^{11}$ cm^{-3} the room temperature thermal conductivity was constant at approximately 160 W/m.K , but at higher dislocations it dropped off rapidly with values of 30 W/m.K at dislocation densities of $\approx 10^{13}$ cm^{-3} [68]. Computational methods have found ideal thermal conductivities of 180 W/m.K and phonon mean free paths of approximately 50 nm [69, 70]. Materials with higher thermal conductivities are desirable since the heat which is generated during device operation can be extracted more efficiently from hot spots and this will result in lower device temperatures. The GaN thermal

conductivity values are comparable to silicon, but lower than silicon carbide, meaning thermal management must be considered more carefully in GaN devices. The heat capacity of GaN is 0.44 $Jmol^{-1}K^{-1}$, and its Debye temperature is 912 K [70].

2.2.2 Material synthesis

As it stands, bulk growth of GaN is expensive and difficult when compared to silicon which limits its scalability in terms of industrial production. Whereas other semiconductors such as silicon can be synthesised through cost effective melt-growth techniques, the high binding energy of the Ga-N bond means GaN is susceptible to decomposition rather than melting except at high pressures [71, 72]. Melt growth techniques can provide low cost material because the growth rate is high and large area synthesis is possible, and the material is typically of high quality as the defects do not crystallise. Whilst melt growth techniques are desirable, alternative methods must be sought for GaN synthesis. The synthesis of GaN can be split into two main branches, the growth of bulk GaN which can be used for substrates and the growth of GaN films which can be used as active layers in devices.

There are four main techniques for growing bulk GaN, and as these cannot be from the melt they focus on the crystallisation of GaN on seeds from a solution or a gas phase. Ammonothermal growth is very commonly used. In this process a GaN containing starting mixture is heated in super-critical ammonia until it dissolves. It then moves via convection to a hotter part of the growth chamber and crystallises on the GaN seeds located there [73]. For ammonia to become supercritical it requires pressures of approximately 250 MPa and temperatures of approximately 500°C, which is the lowest growth temperature of all the bulk growth techniques discussed here. An alternative which uses higher pressures of approximately 2 GPa and temperatures of approximately 1400°C is High Nitrogen Pressure Solution (HNPS) growth, where the nitrogen is instead dissolved in a gallium solution containing GaN seeds. The seeds are placed in a cooler part of the chamber, so when the nitrogen in the solution reaches them via convection, it is in a supersaturated state which drives crystallisation on the seeds [74]. The third solution growth technique is the sodium flux technique, which uses the lowest pressures at between 5 and 10 MPa and temperatures of approximately 750°C. In this technique GaN synthesises on a seed

from a starting solution consisting of gallium and sodium nitride. The mixture is heated in an isolated environment containing the GaN seed until a melt is created. The GaN then crystallises on the seed as the temperature is reduced [75]. Of these growth techniques ammonothermal growth appears to be the most industrially scalable, although the sodium flux technique has been used to produce free standing 6-inch high quality GaN crystals [76]. Denis *et al.* report that HNPS and sodium flux can give lower dislocation densities than ammonthermal growth, but that all techniques can incorporate significant oxygen concentrations if care is not taken, which can reduce wafer resistivity [72].

A common alternative to these solution crystallisation techniques is the gas phase crystallisation technique Hydride Vapour Phase Epitaxy (HVPE). HVPE growth takes place in a chamber filled with an inert gas, where the precursor materials flows in a gaseous form. The first step is to flow chlorine gas over a solid gallium source such that they react and form gallium chloride gas. Separately, ammonia is introduced into the system, and mixes with the gallium chloride in a high temperature zone of the chamber. This gas mixture then flows to the seed crystal which is in a cooler part of the chamber to encourage GaN nucleation [77]. The advantages of HVPE, that high quality material can be grown very quickly at growth rates up to 1870 μm h^{-1}, have led to HVPE becoming the most common technique for the growth of commercial GaN substrates [78, 79]. However a major issue with HVPE technology is the seed crystal on which the GaN grows epitaxially. If the seed is not GaN, the growth can still occur hetero-epitaxially but there will be an inherent wafer bow caused by the difference in coefficient of thermal expansion of GaN and the host substrate of choice, which makes device processing difficult [77, 80]. Alternatively, a GaN crystal can be used as the seed. It is common to use a GaN substrate grown via the ammonothermal process as this will be unstressed, but the growth area is limited by the seed size. Ammonothermal crystals can also have high dislocation densities which will then propogate through the HVPE grown material [20, 79].

2.2.3 Wafer epitaxy

An alternative to bulk GaN growth is to grow the GaN device layers hetero-epitaxially on substrates such as silicon, silicon carbide, or diamond. Because of the high material quality and

high level of control necessary for the GaN device layers, gas phase crystallisation techniques are preferred to the solution crystallisation techniques discussed in Section 2.2.2. Whilst HVPE has many advantages for bulk GaN growth, the highly reactive chloride bond means it lacks the control necessary for device layers where layer thickness can be of the order of nanometres and the dopant profile must be carefully controlled [81]. Therefore the two most common techniques for growth of GaN device epitaxies are Metal Organic Vapour Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE). In MOVPE metal organic compounds containing gallium and nitrogen flow across the substrate in a hydrogen carrier gas and nucleate [82]. The growth takes place in a low pressure chamber ($\approx$ 100 Torr), and with the precursor gases mixed with a hydrogen carrier gas. This has the benefit of producing high quality, atomically flat material which grows quickly and is easy to dope [83]. MBE differs in that the growth takes place at ultra-high vacuum ($\approx 1 \times 10^{-9}$ Torr) and there is no carrier gas. Pure elemental sources are disassociated in their own feed chambers with controllable shutters, and when the shutter is open the elemental radicals diffuse to the substrate and nucleate. The ultra-high vacuum is necessary to give the feed elements a long mean free path and ensures the purity of the grown material. The shutter system means dopants can be easily controlled and sharp interfaces can be formed [84]. MBE also has the advantage that there is minimal waste material. Originally, MOVPE produced higher quality material, but this is no longer the case and the main disadvantage to MBE comes from the requirement for ultra-high vacuum which can cause production issues in commercial environments [83]. Current research into MBE growth centres on the nitrogen source used. Ammonia is commonly used but this causes impurity corporation, whilst nitrogen plasma sources are difficult to control.

The substrate used for GaN wafers has implicatons for the rest of the device epitaxy, meaning the device application should be considered when choosing the design. For instance if cost is the driving factor, silicon is the cheapest available substrate and provides an option for integration into the already existing CMOS infrastructure, although GaN growth uses [1 1 1] substrates and CMOS uses [1 0 0] substrates [20]. Silicon carbide and diamond are more suitable for high performance electronics as both have high thermal conductivities making them suitable for applications which require high power densities and enhanced reliability such as LIDAR for

autonomous vehicles and high bandwidth satellite communications [21, 32]. Vertical devices are sometimes preferred for high voltage applications in which case GaN substrates are preferable as they have less stress meaning thicker device layers can be grown. Vertical structures are typically used for power devices as it is desireable for electric fields to be as large as possible. Interfaces are often points of breakdown as they contain defect states, as is the substrate if it has a smaller bandgap than GaN. As a result, GaN-on-GaN devices will typically have higher operating voltages than GaN on non-native substrates. Homoepitaxial material can also have fewer threading dislocations which are electrically active and provide direct leakage paths through the device [63, 85].

As the devices studied for this work are designed for high power density RF applications, the focus will be on diamond and silicon carbide substrates. GaN can be grown directly onto silicon carbide with the help of an AlN interface layer, however the most common approach for GaN-on-diamond devices is to grow GaN on silicon, attach a handle wafer to the GaN surface, remove the silicon, grow the diamond on the GaN, and then remove the handle wafer [86]. This process is discussed in more detail later in Section 4.3, however it is clear that for both GaN-on-diamond and GaN-on-SiC, good quality GaN growth on silicon and silicon carbide is imperative. In both cases there is a nucleation layer such as a 100 nm AlN film at the interface between the GaN and the substrate to prevent silicon diffusion and to isolate the devices from the substrate [87].

Due to the mismatch in the lattice parameter and the coefficient of thermal expansion between the GaN and the substrate there will be an inherent stress in hetero-epitaxial GaN layers once the wafer is cooled back to ambient conditions. This must be managed as stress can limit the buffer thickness, the maximum operating voltage, and the 2DEG properties since it can alter the piezoelectric polarisation at the AlGaN/GaN heterojunction [20, 88]. To counter this, strain relief layers are often incorporated in the device structure. These can be either a graded AlGaN layer, where the Al concentration decreases gradually from the interface layer to the GaN buffer, or an AlGaN superlattice where the Al concentration reduces with each layer as you move away from the interface [89, 90]. As well as managing stress, such layers also reduce the dislocation density at the heterojunction since the reducing Al content changes the stress environment in the material which causes the dislocations to divert away from the growth axis and eliminate

each other.

Following the strain relief layer there is often a doped buffer layer designed to be highly resistive and prevent breakdown at high power operation. The doping is necessary since nominally undoped GaN will have oxygen defects present from the growth chamber which act as donors, meaning a compensating acceptor is necessary. Initially iron doping was used to achieve this effect, but carbon doping has since been found to be more effective, with resistivities of approximately 10^9 Ω.cm and 10^{13} Ω.cm respectively [91, 92]. On top of this doped region is a thinner (≈ 500 nm) channel, on which the hetero-junction sits. The channel region can be doped if required, but care must be taken not to reduce the conductivity of the 2DEG which forms below the heterojunction. The heterojunction is typically a 1 nm AlN layer, below a 25% aluminium concentration AlGaN layer which is approximately 25 nm thick [18, 93]. There can also then be a thin GaN capping layer on top of this, and a final passivation layer, typically made of amorphous silicon nitride, which suppresses the impact of surface traps on device operation and reduces surface conduction [94].

2.2.4 High electron mobility transistor operation

Two-dimensional electron gas formation

The first demonstration of a HEMT in GaN was published by Asif Khan *et al.* in 1993 using a 100 nm $Al_{14}Ga_{86}N$ barrier on top of a 600 nm GaN buffer[95]. In this device they observed an order of magnitude increase in both the carrier mobility and density in comparison with bulk material, signifying the occurance of a 2DEG [96]. This 2DEG is essential to the development of GaN as a leading semiconductor material. At the interface of the GaN channel and the AlGaN barrier layer the material is stressed due to the lattice mismatch between the two materials. This results in an electric field as wurtzite III-nitride semiconductors are piezoelectric. A material is considered piezoelectric if an applied mechanical deformation results in a change in potential difference. The potential V of an electric dipole is

$$V(\vec{r}) = \frac{1}{4\pi\epsilon_0}\frac{\vec{r}\cdot\vec{p}}{r^3} \tag{2.28}$$

where $\vec{r}$ is the direction from the dipole to the calculation position and $\vec{p}$ is the polarisation vector. If a dipole exists within a crystal, and that crystal then undergoes a mechanical deformation along the axis of the dipole, the polarisation vector will change, as it is given by

$$\vec{p} = q\vec{d} \tag{2.29}$$

where $\vec{d}$ defines the separation of the two charges in the dipole. In the case of GaN this dipole exists along the c-axis, since, as can be seen in Figure 2.4 (b), the surface is polar along this direction. This lack of inversion symmetry results in both a spontaneous polarisation, σ_{sp} and a piezoelectric polarisation σ_{pe} at the interface which, combined with the fact that III-nitrides have larger piezoelectric constants than other compound semiconductors, makes them ideal candidates for HEMTs [97, 98]. The spontaneous polarisation in AlGaN is higher than in the GaN, so the net polarisation is given by

$$\sigma_{net} = \sigma_{sp-Al} - \sigma_{sp-Ga} + \sigma_{pe} \tag{2.30}$$

where the subscript Al refers to the AlGaN layer and Ga refers to the GaN layer. HEMT technology is helped because, as mentioned in Section 2.2.2, most growth technologies have preferential growth along the c-axis, meaning the polar faces are always presented for fabrication. The polarisation vector defined in Equation 2.29 is typically defined as pointing from the negative charge in the dipole towards the positive. In the case of GaN this means it points away from the nitrogen face and towards the gallium face, as nitrogen is quintvalent whereas gallium is trivalent. Hence, if GaN is grown along the $[0\,0\,0\,\bar{1}]$ direction the induced potential will be negative, resulting in the accummulation of positive charge and the formation of two-dimensional hole gas. Alternatively, if GaN is grown along the [0 0 0 1] direction the induced potential will be positive and negative charge will form, resulting in the formation of a 2DEG [99]. The ideal barrier layer is one which maximises the strain in the system, as this will lead to greater polarisation charges in the heterojunction, but it must also be stable if it is to be used to make a functioning device. The lattice constant of AlGaN is proportional to the aluminium concentration and the interface strain increases with increased lattice constant. However there is a maximum possible aluminium concentration of 33%, as above this value macroscopic relaxation occurs in the barrier which reduces the strain at the interface.

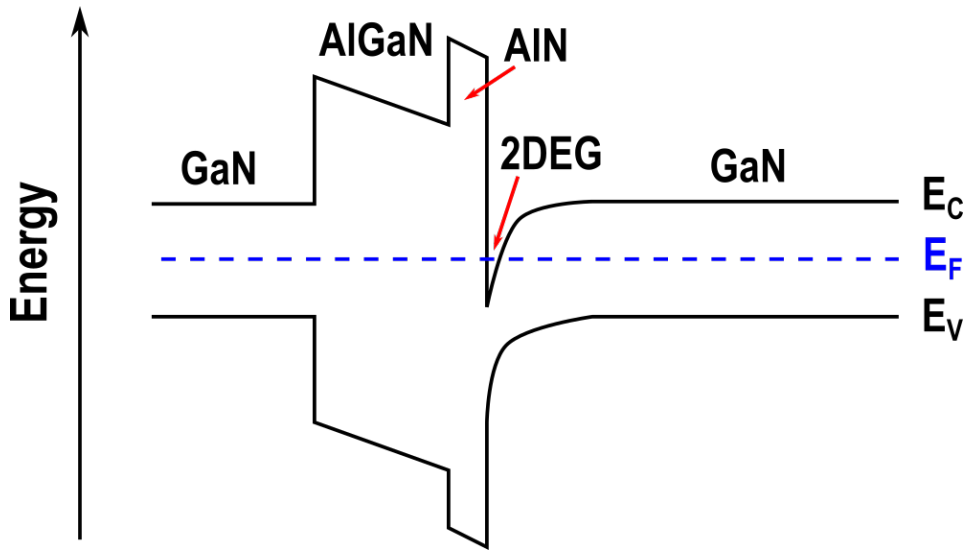


FIGURE 2.6. A sketch of the bandgap at a AlGaN/AlN/GaN heterojunction where E_C is the conduction band, E_V is the valence band, and E_F is the Fermi energy. The strain at the AlN/GaN interface creates a local electric field due to the piezoelectric effect, which in turn causes the conduction band to drop below the Fermi level which leads to charge accumulation and confinement. The opposite effect at the GaN/AlGaN interface is often suppressed with dopants.

A band diagram showing the impact of this polarisation charge on the electronic structure of a GaN/AlGaN/GaN heterostructure is shown in Figure 2.6. The positive potential causes a sharp drop in the conduction band into which the electrons flow. There is a critical thickness of the barrier layer for which the 2DEG will form, as stress will increase with barrier layer thickness and so will the piezoelectric polarisation. The greater the net polarisation at the interface the greater the bending in the conduction band, and the 2DEG will not form until the conduction band is lowered beneath the Fermi energy [100]. The conduction band minima at the GaN/AlGaN interface can be considered as a quantum well, which will have within it discretised energy levels which electrons can occupy. The initial energy level will have a probability density function with a single maxima at in the quantum well which the electrons will occupy if possible. The density of states for the energy levels can be found by solving the Schrödinger equation for a triangular quantum well. Following this process it is found that a 2DEG density of $1.8 \times 10^{13} \text{cm}^{-2}$ is required to occupy this second energy level which is higher than most 2DEG densities found in the literature, suggesting the 2DEG is infact confined to the initial energy level [101].

The confinement of the electrons in the 2DEG leads to a significantly higher charge density in this region than in the rest of the epitaxy. This is a key reason for the excellent performance of GaN HEMTs as the conductivity of a semiconductor σ is

$$\sigma = qn\mu \tag{2.31}$$

where q is the fundamental charge, n is the number of carriers and μ is the mobility. Therefore if n is increased, the resistance of the device is reduced and it will operate more efficiently. The 2DEG concentration can be found through Hall-van der Pauw measurements with values typically in the region of 1×10^{13} cm^{-2}. In addition to this, the conductivity in HEMT structures is also aided by an increase in the carrier mobility in the 2DEG [95]. There are 4 main scattering mechanisms for carriers in a 2DEG, namely, scattering at ionized impurities (I), scattering at lattice defects such as dislocations (L), scattering by optical phonons (P), and scattering due to the alloy concentration and surface roughness of the AlGaN heterostructure (A). Matthiessen's rule states that the resistivity ρ is the sum of the scattering components suggesting

$$\frac{1}{\mu} \propto \rho = \rho_I + \rho_L + \rho_P + \rho_A \tag{2.32}$$

In comparison to a standard FET, confining the carriers to a quasi-two-dimensional sheet increases the mobility as the carriers are now spatially separated from many of the lattice based defects which occur in the device buffer, reducing ρ_L and ρ_I [11]. These scattering mechanisms are further reduced by the increased carrier concentration, as the electrons screen each other from many defects. However there are also negative impacts to the increased carrier concentration, although these effects are weaker than those just mentioned. A higher 2DEG concentration leads to the wavefunction becoming more tightly bound to the interface, resulting in a greater proportion of electrons being in the AlGaN barrier layer where there are many alloying atoms which increases ρ_A. The use of a thin AlN layer increases the asymmetry of the quantum well causing carriers to be more concentrated in the GaN than the AlGaN. Finally, the phonon scattering is weakly dependent on carrier concentration as more carriers increases the probability of a scattering event and the phonon scattering gives the mobility a temperature dependence. As discussed in Section 2.1.1 phonons obey Bose-Einstein statistics and as such their population is temperature dependent and a higher number of phonons results in an increased scattering

probability and a decresed mobility. Altogether these effects result in mobilities of up to 2000 $cm^2V^{-1}s^{-1}$, which is a 74% increase on bulk GaN values [102–105].

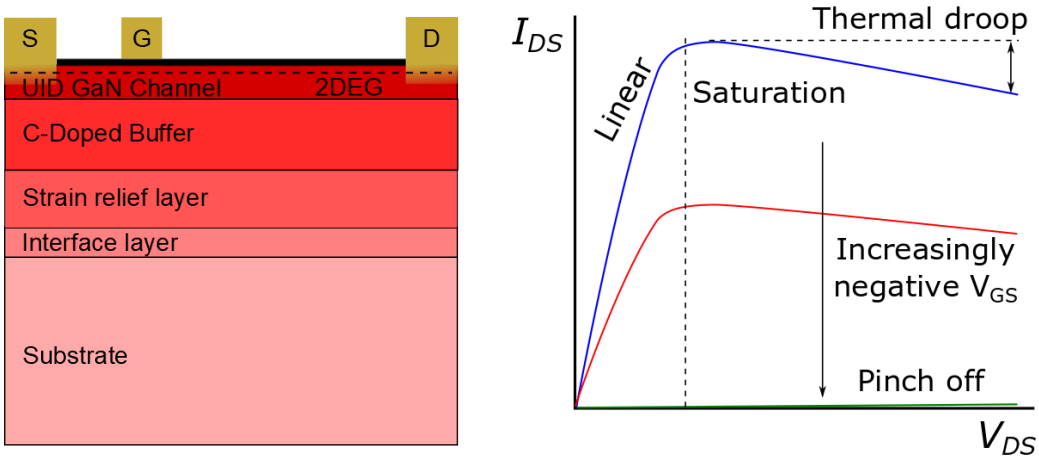
Transistor operation

The 2DEG supplies the conductive path for current to flow in a HEMT, which will have three contacts fabricated on its surface as shown in Figure 2.7 (a); the source, the gate, and the drain. The source and the drain are Ohmic contacts and the drain current (I_{DS}) flows through these when a drain voltage (V_{DS}) is applied. It is typical to define the source as the ground contact, and then any bias applied to the gate and drain are defined relative to this, with the gate used to control the current flowing through the channel. Figure 2.7 (b) is a schematic example of the current-voltage (IV) characteristics of a typical HEMT structure. Initially, as the drain bias is increased from $V_{DS} = 0$ V, the current also increases following Ohms law as the channel resistance can be approximated as constant. In this region the electron drift velocity v follows the relation

$$v = \mu E \tag{2.33}$$

where μ is the mobility and E is the electric field, where it is assumed the current flow and field are one-dimensional. Above a certain voltage the drain current will cease to increase and the current is said to be at saturation. This saturation is caused because Equation 2.33 breaks down and the electrons reach their saturation velocity, where the kinetic energy of the electrons is high enough that they can emit phonons which scatter the electrons and limit the mobility. At higher drain voltages the device heats up and the phonon population increases. As a result, there will be a further reduction in the mobility of the carriers and the drain current will experience a 'thermal droop' from its maximum value.

Also shown in Figure 2.7 (b) is the impact of the gate voltage on the IV characteristics. The applied gate voltage can either enhance the polarisation charge at the heterojunction in the case of a positive bias, or diminish it in the case of a negative bias. This impacts the number of carriers which are present in the channel and, as shown in Equation 2.31, this will impact the conductivity of the channel. When the gate voltage enhances the conductivity of the channel this shows as a higher current for the same drain voltage. The converse is true for a negative gate



(a) (b)

FIGURE 2.7. (a) A schematic diagram of a typical GaN HEMT structure fabricated on a non-native substrate. The barrier layer is omitted for clarity. The 2DEG is isolated from the gate by the black passivation layer. The source and drain contacts diffuse in to the GaN, to allow contact with the 2DEG. (b) A sketch of typically drain voltage (V_{DS}) vs drain current (I_{DS}) characteristics for a HEMT at three different gate voltages (V_{GS})

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bias. The gate voltage which fully depletes the carriers is named the threshold voltage (V_{Th}) and for $|V_{GS}| > |V_{Th}|$ there will be no current flow in the channel for all drain voltages and the device is said to be pinched off.

Given that current flows through the source and drain contacts it is necessary for these to be ohmic contacts. An ohmic contact forms when the work function of the metal is lower than that of the semiconductor. When the materials are brought into contact, band bending occurs such that the Fermi levels are aligned. This creates an electric field and allows electrons to flow from the metal and into the semiconductor with no barrier. For GaN HEMTs, the ohmic contacts are typically fabricated using a titanium, aluminium, nickel, gold stack which is annealed at 800°C so that metal ions diffuse to the 2DEG and charge can flow through the circuit. Whilst his provides the desired low resistance, the annealing results in rough edges which limit how small the devices can be made. In addition, the gold means the devices cannot be introduced to silicon CMOS production lines as gold is extremely detrimental to silicon MOSFET performance [18, 106, 107].

A Schottky contact occurs when the work function of the metal is higher than that of the

semiconductor, resulting in the formation of a barrier and a depletion region at the interface between the materials. This barrier results in a rectifying contact which inhibits current flow below a critical voltage, but allows it above that voltage. A Metal-Insulator-Semiconductor contact prevents conduction in either direction as the interface layer provides a large barrier to electron transport in either direction. This type of contact is used for the gate contact as it is not desireable for electrons from the 2DEG to be ejected through the gate. A thin dielectric layer is often incorporated to further limit the gate leakage currents. The gate metal stacks for a GaN HEMT will typically be made of nickel and gold [108].

As the 2DEG forms spontaneously, GaN HEMTs made from this heterojunction architecture are normally-on devices; the gate is used to pinch off the device channel rather than enhance it. This tends to be incompatible with many industry power switch applications which require devices to be normally-off. A normally-off device acts as a fail-safe since if the device breaks the circuit is broken. This has lead to the development of GaN cascode circuits, shown in Figure 2.8, where a silicon MOSFET is used in conjunction with the HEMT. For operation, the HEMT's source is connected to the MOSFET's drain, and the HEMT's gate is connected to the MOSFETs source. This effectively makes the V_{DS} of the MOSFET the negative of the V_{GS} of the HEMT. When the MOSFET is off, the V_{DS} is high, and so the HEMT is also off, turning it effectively into a normally-off device. However, once the MOSFET is switched on, the V_{DS} decreases until it drops below the threshold voltage of the HEMT, which then begins to conduct [109].

2.3 $\beta - Ga_2O_3$ FETs

2.3.1 Material properties

Gallium oxide has many polymorphs (α, β, γ, δ, ϵ), but the most commonly used for devices is $\beta - Ga_2O_3$, which is stable at all temperatures up to its melting point [111]. $\beta - Ga_2O_3$ has a monoclinic crystal system with its unit cell and relative dimensions shown in Figure 2.9. In contrast to the GaN unit cell which contains just four atoms, the $\beta - Ga_2O_3$ unit cell has a total of 30 atoms, 12 of which are gallium and 18 of which are oxygen. It is convention that materials which have a bandgap wider than that of GaN are defined as ultra-wide bandgap materials, and

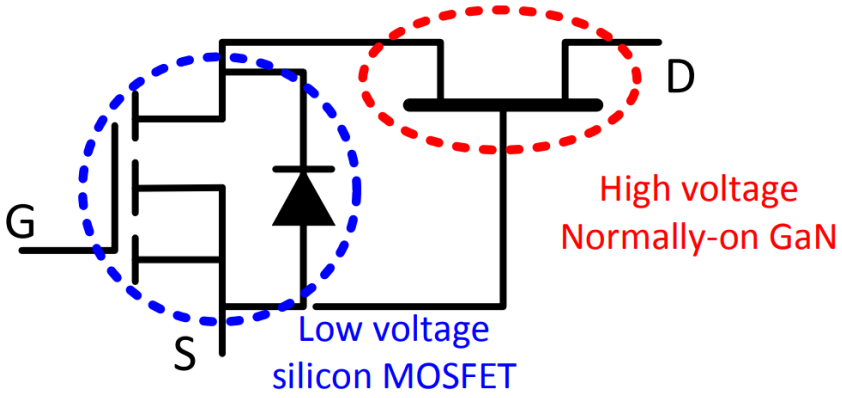
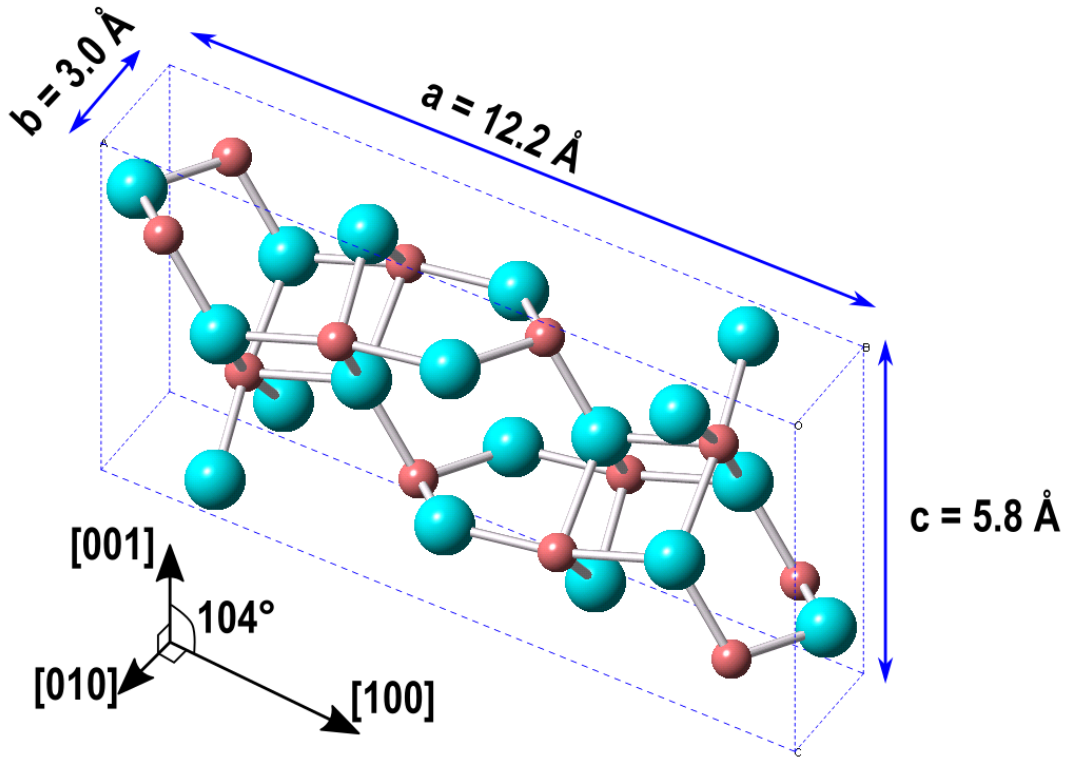


FIGURE 2.8. A circuit diagram of a GaN HEMT in a cascode configuration with a silicon MOSFET. This arrangement allows the GaN HEMT to be a normally-off device, which is required for industrial applications. Image from Huang *et al.* [109]. Reprinted with permission of the IEEE.

$\beta - Ga_2O_3$ fits this classification as it has an indirect bandgap of 4.85 eV, and a direct bandgap which is only slightly larger at 4.9 eV. It was discussed in Section 2.2.1 how holes have a lower mobility than electrons in GaN, and this can be judged by the curvature of the band structure. The same effect is seen in $\beta - Ga_2O_3$, but as shown in Figure 2.10, it is more exaggerated. The valence band is almost flat across all crystal directions, meaning the hole effective mass is larger (40 m_e) whereas the conduction band is parabolic about the Γ point meaning the electron effective mass is significantly smaller at approximately 0.28 m_e [111]. Because of this the electron mobility is found to be approximately 100 $cm^2V^{-1}s^{-1}$ whereas holes are predicted to have mobilities of order 10^{-6} $cm^2V^{-1}s^{-1}$ due to strong localisation at the oxygen atoms, making p-type conductivity challenging [112, 113].

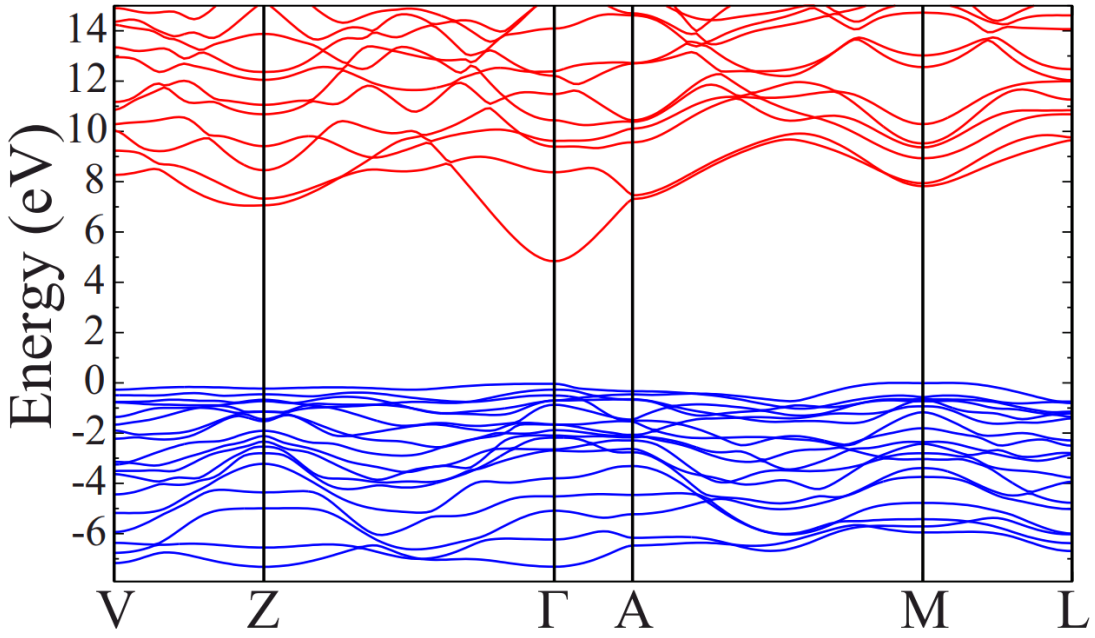
Therefore, devices fabricated in $\beta - Ga_2O_3$ use electrons as the primary carrier, although the electron mobility is still only a tenth of that of GaN. The dielectric constant of $\beta - Ga_2O_3$ was calculated to be 13.9 by Lee *et al.* [114]. Due to its ultra-wide bandgap, $\beta - Ga_2O_3$ is transparent at wavelengths above 270 nm which makes probing of the bandgap in absorption spectroscopy difficult due to the lack of availability of short wavelength probe sources [115]. It has a slightly anisotropic room temperature refractive index which is 1.99 at 400 nm and drops to 1.91 at 1500 nm in its direction of maximum, [0 1 0] [116].



(a)

FIGURE 2.9. The unit cell of $\beta-Ga_2O_3$ is shown along with selected material parameters taken from Ahman *et al.* [110]. The oxygen is represented by blue balls and the gallium by red balls. It is a monoclinic crystal system with 12 Gallium atoms and 18 Oxygen atoms in the unit cell.

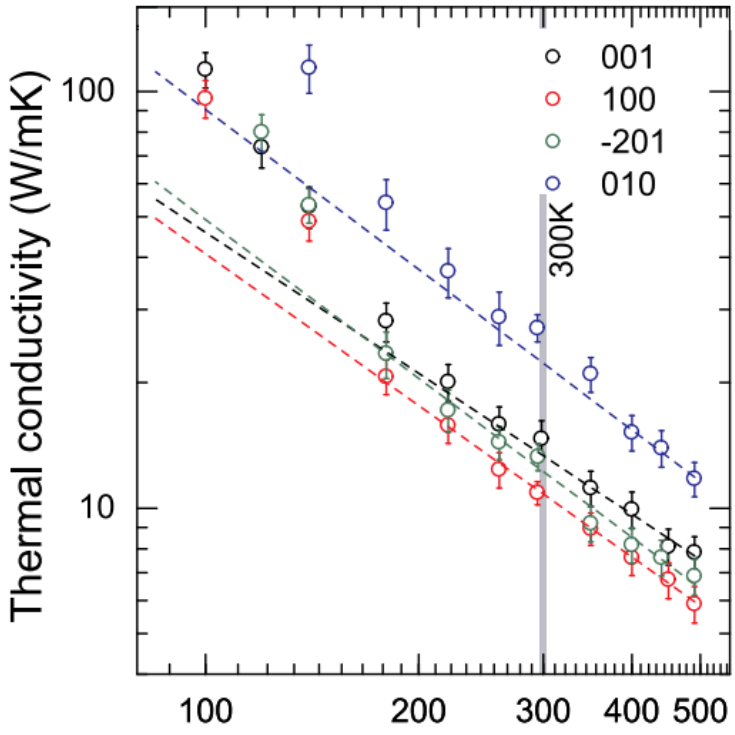
Similarly, the thermal conductivity of $\beta-Ga_2O_3$ is also anisotropic with a maximum along the [0 1 0] direction. This maximum has been determined to be 27 ± 2 W/m.K, along with values of 15 ± 2 W/m.K and 11 ± 1 W/m.K along the [0 0 1] and [1 0 0] directions respectively [46]. These thermal conductivities are significantly lower than most other semiconductors, with the maximum being 17% of the GaN thermal conductivity and 7% of the SiC thermal conductivity. The reason for the low thermal conductivity of $\beta-Ga_2O_3$ can be seen by studying Equations 2.26 and 2.27, which state the umklapp scattering rate is dependendent on the square of the Grüneisen parameter, the negative exponential of the Debye temperature, the inverse of the average atomic mass and the inverse of the square of the phonon velocity. For $\beta-Ga_2O_3$ the average atomic mass is 37.4 amu, which is slightly lower than GaN (42 amu), although both are significantly higher than



(a)

FIGURE 2.10. The band structure of $\beta - Ga_2O_3$ as calculated by Varley *et al.* [117]. There is a close to direct bandgap of 4.9 eV at the Γ point. The valence band is flat, meaning holes are heavy. Reprinted with permission from AIP Publishing.

diamond (12 amu). Guo *et. al* reported that the Grüneisen parameter of $\beta - Ga_2O_3$ is similar to that of GaN and diamond, but the phonon velocity, and Debye temperature are both lower, which results in the lower thermal conductivity [46]. This brings challenges when designing high power density electronics as the active device layers will not spread heat effectively. However one slight benefit is that the temperature dependence of the thermal conductivity is lower than in GaN, meaning there will be less of a degradation in the thermal transport as the device is operated. The thermal conductivity follows a typical T^{-x} relationship as shown in Figure 2.11, with x being 1.12 along [0 0 1], 1.21 along [1 0 0] and 1.27 along [0 1 0]. The specific heat capacity is 0.56 $Jg^{-1}K^{-1}$, and the Debye temperature is 872 K [118, 119]. The mechanical properties of $\beta - Ga_2O_3$ are relatively unexplored with no results in the literature for fracture toughness or coefficient of thermal expansions. However Nikolaev *et al.* found the Young's modulus to be approximately 230 GPa, making it slightly less stiff than GaN [120].

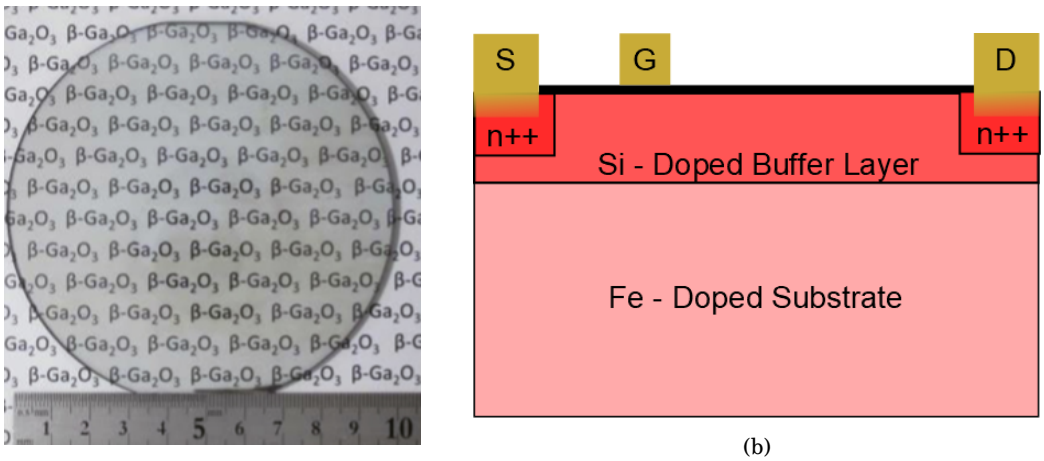


(a)

FIGURE 2.11. Thermal conductivity of $\beta - Ga_2O_3$ along the different crystallographic orientations. Image adapted from Guo *et al.* [46]. Reprinted with permission from AIP Publishing.

2.3.2 Material synthesis

One of the major benefits that $\beta - Ga_2O_3$ holds over its wide and ultra-wide bandgap competitors is that it can be synthesized from a variety of melt-growth techniques, making substrates affordable and scalable at an industrial level [121]. Initially the floating zone technique was used by Villora *et al.* to produce large single crystals and wafers along the 3 major crystal orientations ([1 0 0], [0 1 0], [0 0 1]) [122]. In this technique, a feed rod is prepared from a Ga_2O_3 powder precursor which is cold pressed and annealed to form the rod. This rod is then placed in contact with a seed crystal of the desired orientation, and a heating coil is used to form a molten interface between the rod and the seed. The heating coil is moved along the rod at a rate of a few mm per hour which decreases the temperature of the molten region causing it to crystallise on the seed. Then, as the heating coil moves up the rod, a new molten interface is formed between the now smaller rod and larger seed. Whilst this technique was effective, wafers were limited to 50 mm in



(a) (b)

FIGURE 2.12. (a) Image of a Ga_2O_3 wafer grown by Higashiwaki *et. al* via the edge defined film fed growth technique [125]. Reprinted with permission from IOP Publishing. (b) A sketch of a possible Ga_2O_3 FET structure utilising heavily doped buffer regions under the contacts to reduce contact resistance. The latest generation of devices also have field plates on both the source and drain side of the gate.

diameter. As a result, edge defined film fed growth has become the preferred synthesis method, with an example of a 100 mm diameter wafer grown by edge defined film fed growth shown in Figure 2.12 [123]. In this process, liquid is pulled up from a Ga_2O_3 melt using capillary forces [124]. A pressure gradient is used to pull the material through an aperture which has a seed at the end [123]. Growth rates are approximately 15 mm per hour, although unintentional dopants included during growth require compensation defects to be introduced such as iron or magnesium to ensure the substrate is insulating [125].

To complete wafers suitable for the fabrication of lateral devices it is necessary to perform epitaxial growth of high quality material on top of these bulk substrates [125]. Similar to GaN, the preferred techniques for this deposition are MBE and HVPE, although in the case of the latter the 'H' stands for Halide. MBE is the most advanced technique for $\beta - Ga_2O_3$ growth, with the oxygen supplied as either ozone which gives faster growth rates, or oxygen radicals disassociated with a plasma. Higashiwaki *et al.* found that the surface roughness was dependent on the growth temperature, with the smoothest surfaces having a RMS roughness of 0.4 nm when grown at 600°C [125]. Whilst MBE may be the most advanced laboratory growth technique, it is a difficult technique to include in an industrial process due to the ulta-high vacuum required. This isn't

required for HVPE, where chlorine is flowed over a gallium source to form gallium chloride. This then flows over a substrate with an oxygen source to grow the $\beta - Ga_2O_3$. HVPE has a higher growth temperature at around 1000°C, but there are not concerns over stress and wafer bow due to the availability of native substrates. N-type doping of these layers is necessary for FET fabrication and this is done by including either silicon or tin in the source gas [126]. Alternatively, doping can be achieved by ion implantation of Si^+, which allows for selective area doping as shown in Figure 2.12 (b) [127]. By controlling the doping concentration, the conductivity can span continuously from 10^{-2} $\Omega^{-1}cm^{-1}$ to 10^2 $\Omega^{-1}cm^{-1}$ with minimal impact on the mobility [128].

2.3.3 FET operation

The most common devices developed in $\beta - Ga_2O_3$ are MESFETs and MOSFETs, being originally developed by Higashiwaki *et al.* at the National institute of Information and Communication Technology in Tokyo, Japan [129]. The MESFET structure came first with a 300 nm thick Sn doped channel, Ti/Au ohmic source and drain contacts, and a Pt/Ti/Au Schottky gate contact [129]. The devices were found to perform well, with a pinch off voltage of 20 V and a breakdown voltage of 257 V, but issues with surface leakage led to the development of MOSFET structures. These devices came with both Sn and Si doped channels topped by a 20 nm Al_2O_3 layer. These improvements were effective in reducing the leakage current such that the ratio of I_{DS-on} to I_{DS-off} was as large as 10^{10}, and the breakdown voltage increased to 370 V. The Ohmic contact linearity was also improved by heavy Si^+ doping underneath the contacts to produce n++ regions [127]. The next iteration in the improvement of the $\beta - Ga_2O_3$ MOSFET was the incorporation of a T-gate field plate which, when optimised, resulted in a greater than 50% reduction in the electric field at the gate edge and an increase in the breakdown voltage to 755 V [126].

MOSFET $\beta - Ga_2O_3$ devices have also been developed at the Air Force Research Laboratory. These devices are similar in many ways with a few key differences. For instance several gate oxide materials were tested, with HfO_2 and SiO_2 used in addition to AlO_2 [130]. However, a separate finFET structure was also developed which turns the device into an enhancement mode device. In this finFET structure, 600 nm long trenches were etched into the gate with the peaks being 300 nm wide. These peaks act as the channel, and the gate dielectric and gate are applied

such that they wrap around the fins and deplete the channel, making the devices normally off [131]. The breakdown voltage in these devices is still high at 612 V, but the ON current is lower such that the I_{DS-on} to I_{DS-off} ratio is just 10^5, which the authors attribute to trapping around the edge of the fin structures.

Finally, one of the latest $\beta-Ga_2O_3$ device developments is the δ-doping of the channel. δ-doping is so called because the doping profile resembles a δ function, and it requires the thickness of the doped layer to be less than the de Broglie wavelength of the electrons [132]. The carriers will diffuse into the bulk but will also have an attraction to their ion cores resulting in the formation of a 2DEG just outside this δ-doped layer. This was achieved in $\beta-Ga_2O_3$ by Krishnamoorthy *et al.*, who used MBE to create 100 nm thick Si doped layers which resulted in 2DEGs approximately 10 nm thick [133]. Although mobilities measured in these 2DEGs are currently low (≈ 100 cm^{2}V^{-1}s^{-1}), their formation leads to the exciting prospect of a HEMT made in an affordable UWBG material [134].

2.4 Diamond for heat spreading

2.4.1 Material properties

GaN and $\beta-Ga_2O_3$ are of interest for devices as their wide bandgaps mean devices can operate at higher and higher voltages. However this results in ever increasing power densities which lead to increased device channel temperatures if not managed properly. Diamond is widely considered to be the optimal heat spreading material since it has the highest bulk thermal conductivity known to man. Whilst graphite is the thermodynamically stable form of carbon at standard atmospheric conditions, diamond exists as a metastable polymorph. It has a zincblende structure, a two atom basis on a face centred cubic Bravais lattice shown in Figure 2.13, and is of interest in many fields due to a variety of properties. Its bonds are relatively short at 1.5 Å and its lattice parameter is 3.567 Å giving it a density of 3.51 g/cm^3 [135, 136]. The thermal conductivity can reach over 3000 W/m.K in isotopically pure, single crystal diamond [137]. There are two main reasons for this exceptionally high thermal conductivity, the short strong covalent bonds which promote high phonon velocities, and a low propensity to umklapp scattering as discussed in Section 2.1.2

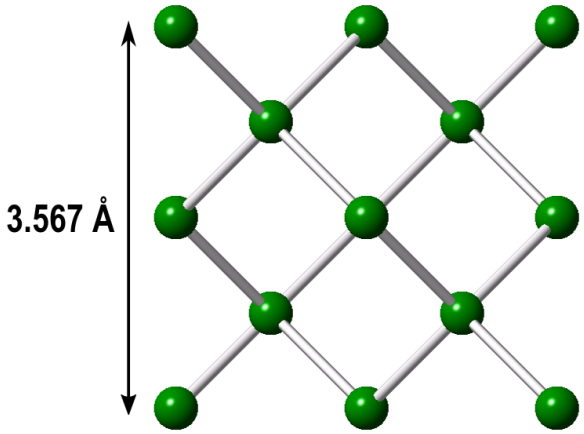


FIGURE 2.13. The [1 0 0] face of diamond crystal structure with carbon atoms in green. It is a face centred cubic lattice with a two atom basis.

[53]. For this high quality diamond the thermal conductivity is found to have a temperature dependence relationship of $T^{-1.26}$ [138]. Whilst the thermal conductivity is remarkable, the heat capacity is not, with a reported value of 600 $JK^{-1}kg^{-1}$ at room temperature, which approaches 2150 $JK^{-1}kg^{-1}$ at diamond's Debye temperature of 1860 K [53, 139]. The phonon mean free path in single crystal diamond is estimated to be 180 nm, making deviations from the perfect crystal which occur on this length scale particularly inhibitive to the thermal conductivity [140].

Diamond is renowned for being an exceptionally hard material, as its strong bonds make it difficult to compress [141]. However it is prone to brittle fracture, as its high order means there are crystal planes along which it cleaves particularly easily, such as along the [1 1 1] direction. In spite of this, its fracture toughness of 6.7 $MPa.m^{1/2}$ is still higher than that of GaN [142–144]. It's Young's modulus of approximately 1200 GPa makes it one of the stiffest bulk materials and as such it has low room temperature coefficient of thermal expansion of 1.06×10^{-6} K^{-1}, which is lower than most traditional semiconductors [145, 146]. The coefficient of thermal expansion is of particular importance for wafer fabrication, which often takes place at high temperatures meaning there will be a significant difference in the rate of expansion and contraction between diamond and its partner which can result in strain at the interface. As an example, the coefficient of thermal expansion of GaN, discussed in Section 2.2, is approximately three times larger.

Diamond has the widest bandgap of all the materials discussed in this work with an indirect ultra-wide bandgap of 5.5 eV [147]. Carrier mobilities in single crystal diamond are large

in comparison to the semiconductors previously discussed, again due to its ordered nature. With 4500 $cm^2V^{-1}s^{-1}$ electron mobilities and 3800 $cm^2V^{-1}s^{-1}$ hole mobilities quoted in the literature for room temperature, diamond devices seem to be an attractive research area for high power density devices [148]. However when dopants are introduced into the lattice to increase carrier concentration the mobilities are significantly reduced, with values at approximately 30 $cm^2V^{-1}S^{-1}$ [149, 150]. This is a major reason why diamond is only considered as a heat speader in this work. Holes and electrons have both heavy and light effective masses where for electrons the heavy mass is 1.4 m_e and the light is 0.4 m_e, and for holes these are slightly lower at 1.1 m_e and 0.3 m_e [151, 152]. The dielectric constant of diamond is approxiately 6, and its refractive index is 2.387 at room temperature [153, 154]. Diamond is a material of interest in photonics applications due to its range of colour centres, but it is its clear absorption window, except for the multi-phonon processes in the mid-IR range, that makes these centres accessible [155].

2.4.2 Material synthesis

Diamond has many applications beyond the heat spreading discussed in this work, and the way the diamond is synthesised is specific to each application. In the case of diamond heat spreaders the requirements are that the thermal conductivity is as high as possible, it must be fabricated in a planar fashion such that it can be integrated with wafers, and the growth should be economical, making large sizes and inexpensive processes preferable. There are two common growth methods for synthetic diamond, High-Pressure High-Temperature (HPHT) and Chemical Vapour Deposition (CVD). HPHT growth aims to mimic how diamond is formed naturally in the earth's mantle where the high pressures and temperatures create an environment where diamond is thermodynamically stable [156]. Typically a carbon source of either diamond or graphite powder is combined with a catalyst in a capsule. This capsule is pressurised to approximately 5 GPa and a temperature gradient at approximately 1500°C is applied across the container such that at one end the carbon source dissolves into the catalyst and at the other end it recrystallises as diamond [157]. This technique was used to grow the largest synthetic diamond at 32.26 ct and can produce very high quality material [158]. However it is not suitable for integration with electronics on a

large scale as films cannot be grown, and hence it is difficult to integrate.

Alternatively CVD can be used for more precise diamond growth. A majority hydrogen feed gas containing between 0.5% and 5% methane is disassociated at high temperatures (≈ 3000 K) and low pressures (1-100 Torr) over a substrate [159]. The radical species then nucleate on the substrate and diamond is formed [160]. The two most common flavours of CVD are the Hot Filament (HF CVD) and MicroWave assisted Plasma Enhanced (MW PE CVD). They vary in how they activate the gas with HF CVD using thermal activation brought about by heating a resistive wire, and MW PE CVD using microwaves to inject energy into the chamber and create a plasma [161]. As CVD can grow diamond films and provide more control, it is the most commonly used technique for semiconductor integration with diamond.

CVD growth of single crystal diamond would be ideal, giving the combination of growth control with the high thermal conductivity. Single crystal growth is possible on native diamond substrates and on iridium, although this is limited by the original substrate size and growth rates must be slow [162]. Single crystal diamond also cannot be grown directly onto common semicondutors meaning an extra integration step would be necessary. An alternative is to grow polycrystalline diamond, which can be synthesised faster, giving better economy, and on a greater variety of non-native substrates such as silicon, gallium nitride, aluminium nitride, and cubic boron-nitride [163–166]. However it has the downside that the introduction of grain boundaries leads to a reduced thermal conductivity.

To speed up the nucleation process a variety of techiques are used to create nucleation sites. Mechanical abrasion of the substrate leads to scratches and defect formation which increases nucleation as these sites have lower bonding energies, with the cost of damaging the substrate [167]. Bias enhanced nucleation attracts radical species present in the plasma to the substrate by applying a bias to the substrate. The resulting bombardment of ions leads to the formation of an amorphous carbon layer which aids the nucleation of diamond, although the high energy of the radicals can lead to sub-surface damage of the substrate [168, 169]. Finally, diamond seeds ranging from nanometres to microns in diameter can be deposited onto the surface, typically through the use of electrostatics. One approach changes the ζ potential of the particles by adjusting their surface chemistry such that the charge of the particles is opposite to the surface

potential of the substrate. The substrate is then submerged in the seed solution allowing the seeds to accumulate on the surface [170]. Alternatively the substrate and the solution can have opposing biases, and the solution sprayed at the substrate such that the seeds again accumulate on the surface [171].

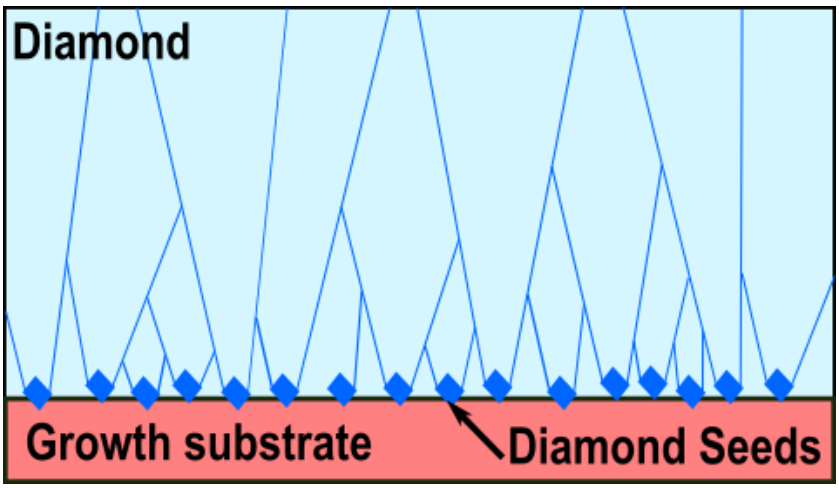
Once the diamond has nucleated, growth begins laterally and conditions should be optimised such that a complete film is formed as quickly as possible to reduce substrate damage and pinhole formation [169]. Once this film is completed the vertical growth begins in earnest from each nucleation site. Certain seeds will grow faster than others, leading to a competitive columnar structure which has fewer grain boundaries as growth continues as shown in Figure 2.14 (a) [172]. The change in the density of the grain boundaries results in an inhomogeneous thermal conductivity throughout the diamond layer, meaning diamond in which the grains expand rapidly is preferred as the density of the grain boundaries will be reduced. However it is also important to consider the quality of the grain boundary. In the ideal case a grain boundary is similar to a dislocation, with a carbon atom incorrectly bonded to another carbon atom. However in reality this layer can have a finite thickness with several incorrectly bonded carbon atoms and it can also include pockets of impurities such as boron or hydrogen. The worse the quality of the grain boundary, the worse the thermal conductance across that boundary will be as the lack of crystallinity and long range order prevents wave transport.

The effect of nanostructure on diamond film thermal conductivity was studied by Anaya *et al.* with the data shown in Figure 2.14 (b) [173]. In a previous paper the authors found the thermal conductivity of a range of diamond films of varying thickness [174]. By studying the microstructure it was found that the thermal conductivity of the film was a convolution of the thermal conductance in the grains and the thermal resistance at the boundary. The thermal conductivity of the individual grains was found to scale with the grain size, whilst the inter-granular thermal resistance increased towards the growth surface, as the amount of impurities increased. With this information in hand they calculated the in-plane and cross plane thermal conductivity of different portions of a 95 μm thick diamond film where the grain structure had been mapped via a transmission electron microscopy cross-section. In all cases the cross-plane thermal conductivity is higher, although the anisotropy decreased as the film thickened.

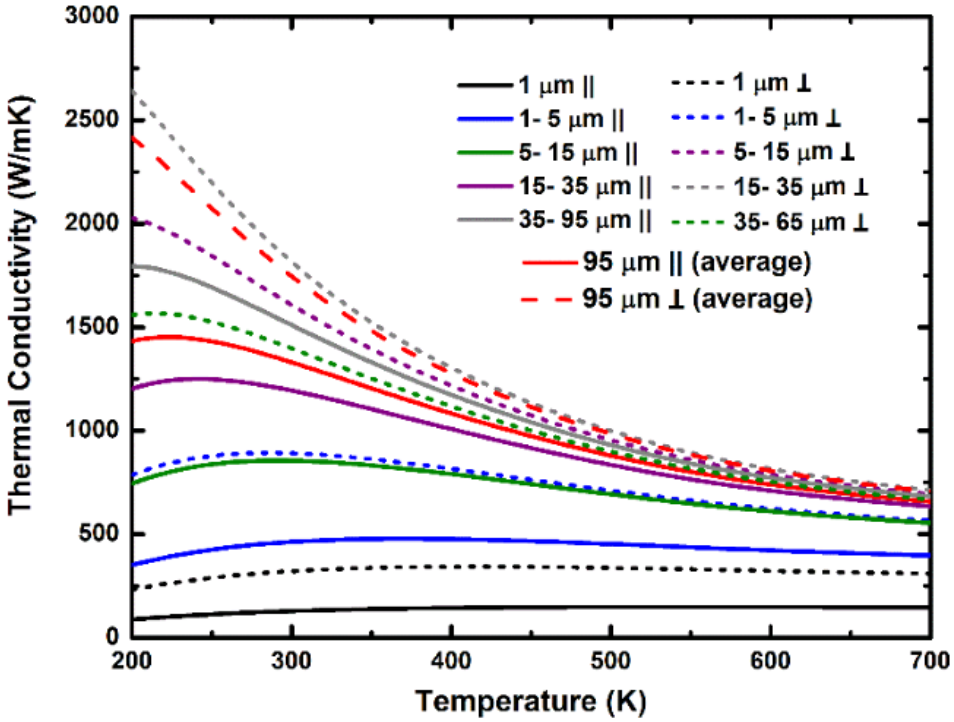
Whilst it is typical for a material's thermal conductivity to reduce as the temperature is increased, it is desirable for this effect to be as small as possible, since reducing the heat spreading capability as temperature is increased compounds the problem. However higher quality material tends to have a higher temperature dependence. This is because the temperature dependence of the thermal conductivity, as discussed in Section 2.1.2, is caused by umklapp scattering reducing the phonon mean free path. When material is poor quality the mean free path is limited by defect scattering which is constant with temperature. The room temperature effective cross-plane thermal conductivity of the 95 μm diamond substrate was approximately 1800 W/m.K, and the in-plane was approximately 1400 W/m.K. As expected this is significantly higher than the room temperature thermal conductivity of the first 1 μm of the film, which is approximately 150 W/m.K in-plane and 300 W/m.K cross-plane.

Hydrogen is of particular importance to CVD diamond growth. Graphitic carbon is preferentially etched by the hydrogen, promoting diamond growth. The hydrogen also suppresses renucleation, which increases grain size, increasing the thermal conductivity, but also surface roughness, making integration more difficult [176]. In the gas phase, the hydrogen radicals react with carbon species, which results in carbon-containing radicals which contribute to diamond growth. It also passivates and stabilizes the surface, but can react with hydrogen radicals to form gaseous hydrogen, leaving a carbon dangling bond on which the gaseous carbon radicals can bond [169]. Increasing the number of hydrogen radicals is therefore ideal for high quality diamond growth such as that required for heat spreading in electronics, but the increase in radicals can only be achieved by an increase in supplied power which increases the cost of the diamond.

Dopants can be incorporated into the diamond through the feed gases. Boron, the most common intentional dopant in diamond, has been incorporated in concentrations over 10^{21} cm^{-3} by introducing trimethylborane [177]. As it is readily incorporated as a substitutional defect, and it provides a relatively low acceptor level at 0.37 eV, boron is the most commonly used dopant when creating electronic devices. Whilst this p-type doping is relatively easy, the n-type doping is significantly more challenging. Nitrogen is a donor and is readily incorporated into the diamond lattice. It is often incorporated into CVD diamond due to air leaks, and is found to increase growth rates, but its donor level is 1.4 eV below the conduction band, making it ineffective [178].



(a)



(b)

FIGURE 2.14. (a) The van der Drift growth process for polycrystalline diamond with grain boundaries shown by dark blue lines. Although grain boundaries are shown as thin lines this is a simplification. In reality grain boundaries can have a finite thickness of disordered carbon with inclusions. The grains grow competitively from the seeds resulting in fewer grain boundaries away from the growth face. (b) Data from Anaya *et al.* showing both the in-plane and cross-plane temperature dependent thermal conductivity of different portions of a 95 μm thick polycrystalline diamond film [175]. Reprinted with permission from AIP Publishing.

Phosphorous is a desirable dopant as it provides a 0.6 eV donor level which may be useful for certain applications, and it can be incorporated in the lattice by using phosphane in the feed gas [179]. Finally, silicon defect centres in diamond have interesting quantum properties, and are often included unintentionally due to etching of quartz components in the reactors, but can be controlled by including other solid sources into the chamber or through including silane in the feed gas [180, 181]. To grow the highest thermal quality diamond possible it would be necessary to limit the incorporation of all of these donors as they will provide scattering points for phonons. However this is not feasible, primarily because the nitrogen is necessary to increase growth rates and reduce costs.

2.4.3 Diamond integration with electronics

Because of diamond's excellent thermal conductivity it has long been considered an ideal solution for heat spreading in high power electronics. The first recorded use of diamond as a heat sink was by Josenhans in 1968, who bonded diodes to a natural single crystal diamond [182]. The simplest place to implement diamond is in the packaging, where single crystal, or polycrystalline diamond, if size is important, can be sintered between the die and the package. This was performed using 1 mm thick polycrystalline diamond with a thermal conductivity of 1200 W/m.K in a GaAs system with a plastic package. The addition of diamond allowed a 20× increase in power dissipation once challenges with surface roughness and coefficient of thermal expansion induced stresses were overcome [183]. If polycrystalline diamond is implemented in this manner it has the added advantage that the defect rich, low thermal conductivity interface layer can be polished away, resulting in a higher average thermal conductivity [184]. However the effectiveness of this approach is limited due to the diamond's distance from the junction. As an approximation, each epitaxial layer can be thought of as a thermal resistor in series with the others. The total thermal resistance of the wafer stack is then the sum of all the resistances of the epitaxial layers where the thermal resistance is the inverse of the thermal conductance. Adding a low thermal resistance element such as diamond to the stack will therefore not reduce the overall thermal resistance at all. However its benefit comes from in-plane heat spreading. As resistance is inversely proportional to area, the thermal resistance is decreased when the in-plane heat

spreading increases the effective area that the heat is spread over increases. By way of an analogy to an electrical circuit, the in-plane heat spreading can be thought of as adding resistors in parallel to all components which follow it. This impact is reduced when there are low thermal conductivity components in the near junction area which will resist heat flow before it reaches the diamond [185].

Because of this, diamond has been developed extensively as a substrate material for gallium nitride [86]. One approach for diamond substrates is to grow the GaN onto single crystal or polycrystalline diamond. Devices have been fabricated on GaN grown via MBE on (1 1 1) oriented single crystal diamond. Whilst the material quality is high, the scale is limited by the diamond size and the thermal benefit is limited by the low thermal conductivity strain relief layers necessary to prevent the GaN cracking [186]. It has been found to be more effective to grow the GaN on a sacrificial substrate and attach the diamond to the pre-grown GaN. A process was developed for low temperature bonding of GaN to polycrystalline diamond and produced thermal boundary resistances at the GaN-diamond interface as low as 34 m^2K/GW although how uniform this bond is over large areas, and how much further the interface could be improved is not clear [187]. The bonding takes place at 150°C which is much lower than the diamond growth temperature. This means there is less stress in the GaN layers as the impact of the difference in coefficient in thermal expansion is less exaggerated. Also, the devices can be fabricated whilst the GaN is still on the sacrificial wafer allowing well developed techniques, processes, and infrastructures to be used.

Because of the integration and scaling issues associated with the bonding of single crystal material, it is more common to grow diamond on gallium nitride, although there are still several challenges which must be overcome. As discussed in Section 2.4.2, diamond growth must be performed at high temperature (≈ 800°C) to ensure good quality diamond is produced. This makes wafer bow and internal stresses a significant issue, since, as discussed earlier in this Section, diamond is incredibly stiff and has a coefficient of thermal expansion mismatch with GaN. When the diamond is deposited, it is at the high growth temperature, meaning the GaN will have expanded. When the wafer is cooled following the diamond growth, the GaN will shrink more than the diamond resulting in a bowed wafer. In spite of this, it is possible to grow diamond

uniformly and produce 4 inch wafers [32]. The hydrogen rich environment necessary for high quality diamond growth also poses problems as it can etch the GaN buffer, meaning it is necessary to limit the exposure of the GaN [163]. If the GaN is exposed for too long the etching will cause pits and voids at the interface which could inhibit the heat flow across the interface as air is a poor thermal conductor. One way to protect the GaN is to adjust the diamond seed surface chemistry to maximise the seeding density such that a continuous diamond film is formed almost immediately upon growth starting [188]. However in this case the bonding between the substrate buffer and the diamond is a van der Waals attraction. Whilst it is possible to transport heat across a van der Waals bond, it is not as effective as heat spreading through covalent bonding.

There are also issues with adhesion, as the van der Waals bond are easily broken, and as mentioned above, there is a large amount of stress at the interface because of the mismatch in coefficient of thermal expansion. Together these can lead to delamination of the diamond substrate and the GaN buffer. Therefore it is common to use a carbide forming interlayer such as silicon nitride, with aluminium nitride being considered as an alternative. This layer will protect the GaN from the hyrdogen radicals in the feed gas to prevent pit and void formation, and it will also form strong covalent carbide bonds to the diamond which offer a better thermal conductance than other amorphous materials [189]. Despite the positive impacts of a carbide forming interlayer, its thickness must be limited, otherwise it can have an adverse effect on the effective thermal boundary resistance between the diamond and the GaN [190]. For this method of diamond-GaN integration an effective thermal boundary resistances (TBR_{eff}) is often considered to describe the thermal resistance of the GaN-diamond interface. This TBR_{eff} incorporates the resistance caused by phonon scattering at the interface between dissimilar materials, any low thermal conductivity protective interface layers present, and the low thermal conductivity diamond seeding layer. Literature reports for the TBR_{eff} when polycrystalline diamond is grown onto GaN are as low as 12 m^2K/GW, with diamond thermal conductivities of approximately 1500 W/m.K [190]. When devices have been fabricated on this material they have been found to have excellent thermal resistances which out performs equivalent GaN-on-SiC structures by 40% [36]. However the TBR_{eff} is proportional to the interface layer thickness meaning it is important to keep this layer as thin as possible. The danger is then that it becomes too thin, and doesn't provide effective

protection to the GaN.

In an effort to get diamond even closer to the junction, nanocrystalline diamond has been implemented as a passivation layer, and heavily boron-doped nanocrystalline diamond has been implemented as a gate contact [39, 191]. When boron concentrations are approximately 10^{21} cm^{-3} the diamond becomes metallic-like since the mean distance between boron atoms is now less than the Bohr radius of boron, allowing it to act as a rectifying gate contact [192]. However the heavily boron doped diamond gate has minimal thermal benefit as the grain boundaries and the dopants lower the thermal conductivity to a similar or lower level than that of the metals used in gate contacts. However the nanocrystalline diamond passivation layers proved more effective. When the diamond is located on the top of the device heat does not have to go through the buffer before it can be spread in-plane. The diamond was deposited on a 10 nm silicon nitride layer and was found to reduce peak temperatures by 20% [37]. There were unwanted impacts on the electrical properties as the non-unifrom stress induced by the addition of diamond led to a non-uniform 2DEG density [38]. The gate contact would also be damaged by the harsh diamond growth environment meaning the diamond must be grown first. This requires either etching of the diamond, which can damage the buffer, or a sacrificial gate which can help keep the gate area clear from diamond via a lift off process [193].

2.5 Heat flow in device structures

Temperature increases in transistors occur due to Joule heating in the channel, where the charge carriers interact with each other and the lattice, losing some of the energy which they have gained from the applied electric field. The magnitude of the temperature rise is dependent on the power density in the device P_D which is given by the Joule-Lorenz law

$$P_D = \vec{j} \cdot \vec{E}, \tag{2.34}$$

where j is the current density and E is the electric field. In a transistor, it can be approximated that the current density and electric field are one-dimensional, acting from the drain to the source, meaning the total power dissipation is given by the product of the drain voltage and the drain current. In an ungated transistor, the current density will be constant and the voltage will

be dropped evenly over the channel, meaning the electric field is constant, and the power will be dissipated evenly between the source and the drain. This is not the case however in a full transistor structure. In a normally on device such as the GaN HEMTs and $\beta - Ga_2O_3$ MOSFETs discussed in this work the gate is grounded relative to the source when the device is on and hence is at a lower voltage than the drain. This results in a potential difference between the channel and the gate metal. This means that whilst the current density j can be approximated as constant throughout the channel, there is a local spike in the electric field E on the drain side of the gate. The resulting power density P_D is localised, due to the abrupt nature of the gate edge, and large, due to the high voltage operation possible in GaN HEMTS. Simulation studies have shown that this hotspot can be less than 0.5 μm wide in a GaN HEMT, and its magnitude is signficantly larger than that of the rest of the channel although the maximum electric field is highly dependent on device geometry [18].

This electric field peak is troubling from a device reliability point of view as it can cause local avalanche breakdown or excite hot electrons, whose kinetic energy is sufficient to activate high energy trap states or jump passivation layers to give leakage currents. However, of greatest importance in this work is that the resulting high power density will cause device heating. One solution for the management of this electric field hotspot is the use of field plates; metal overhangs from the gate which are at the same voltage as the gate[194]. If these field plates extend towards the drain, they will cause secondary spikes in the electric field which will reduce the peak electric field at the gate edge, effectively smearing it over a larger area such that the power density is lower [195]. In $\beta - Ga_2O_3$ MOSFETs and AlGaN HEMTs the channel is more resistive, resulting in a less localised hotspot [126, 196]. In the case of $\beta - Ga_2O_3$, the carriers are supplied by doping of the buffer which results in an increased channel resistance and lower mobility because of the carriers scattering from donor ions. Similarly, the alloying atoms in an AlGaN HEMT will scatter carriers in the 2DEG which reduces electron mobility, increasing resistance [196].

The heat generated in this hotspot will flow laterally away from the heat source, but the primary heat flow will be vertical throughout the wafer epitaxy to the heat sink. First it must pass through the buffer, which is the active material in the device. In the case of low thermal conductivity semiconductors, this presents the first major challenge as they themselves will provide

a significant thermal resistance [45, 197]. For GaN HEMTs the first major sources of thermal resistance are any strain relief layers such as graded AlGaN layers or AlGaN superlattices, as these can have thermal conductivities as low as 6 W/m.K [198]. The purpose of including diamond in the wafer epitaxy is to increase the in-plane heat spreading, as in all successive layers the heat will be flowing through a much larger area which reduces their relative thermal resistance. The closer to the channel the diamond is incorporated, the more effective it can be, although the major challenge with diamond substrates at the moment is to get the heat into the diamond in an efficient manner.

This is because there is an inherent thermal resistance associated with heat flow across an interface between two dissimilar materials. There are two common models to describe heat transfer at interfaces, the acoustic mismatch model and the diffuse mismatch model. The acoustic mismatch model assumes that the materials are continuums, there is no scattering at the interface and the impedance at the interface is due to differences in phonon velocity and density between the two materials [199]. Effectively, phonons will only cross the interface if there is a corresponding, available, state in the second material. Conversely the diffuse mismatch model assumes all phonons reaching the interface scatter, with the probability of transmission determined by the difference in the phonon density of states [200]. Due to the assumptions made in both models, the truth typically lies somewhere in the middle but the acoustic mismatch model is often thought of as an upper bound, and the diffuse mismatch model as a lower bound. The buffer-substrate interface of wafer epitaxy is often a multilayer system with an interface layer included, in the case of diamond to protect the GaN and improve adhesion. This interface layer is often amorphous meaning that, as discussed in Section 2.1.2, it will have a thermal conductivity of approximately 1 W/m.K. As the mean free path of the heat carriers is smaller than the thickness of the layer, the resistance of this multilayer system can be considered as the sum of this material's thermal resistance and the interface resistances [201]. Surface roughness, often introduced when diamond is grown through seeding or hydrogen etching, also increases thermal boundary resistances when the roughness is of a similar order as the phonon mean free path [189, 202].

CHAPTER 3

EXPERIMENTAL METHODS

This chapter summarises the experimental techniques used in this work. The relevant theoretical background will be explored, and this will be complimented by an explanation of the experimental set up in the laboratory and the general measurement procedure. The specifics of how each technique was applied will be given in the relevant results chapter. The most commonly utilised technique was Raman spectroscopy. This was used to measure the temperature in the buffer layers of FETs (micro-Raman thermography), characterise the thermal properties of diamond films (nanoparticle assisted Raman thermography), and measure the lifetimes of phonon modes. Photoluminescence was employed to measure device temperatures where micro-Raman thermography was not applicable. Transient thermoreflectance was used to characterise the TBR_{eff} of GaN-on-diamond technology. Finite element analysis was also a key compliment to the experimental techniques in this work. Experimental data were used to calibrate the finite element models of device structures which were then used to determine values which could not be measured experimentally.

3.1 Raman spectroscopy and thermography

3.1.1 Raman scattering

Raman scattering is the inelastic scattering of light when it interacts with matter [203]. The most probable form of scattering is elastic, or Rayleigh scattering, where the incoming photon promotes an electron to an excited virtual energy level, and then after a short period of time the electron relaxes back to its ground state. As it relaxes the electron radiates a scattered photon whose frequency ω_s is equal to the frequency of the incoming photon ω_i. Alternatively, whilst the electron is in its excited virtual state, the electron can lose energy through the creation of a phonon. If an incoming photon with frequency ω_i promotes the electron to an excited virtual state, it can create a phonon of frequency ω_p whilst excited, where ω_p corresponds to one of the normal modes of the lattice. When the electron relaxes back to its ground state it will emit a photon of frequency

$$\omega_s = \omega_i - \omega_p. \tag{3.1}$$

Here the scattered photon has lost energy with respect to the incoming photon, i.e it has been inelastically scattered. Alternatively, the electron can annihilate a phonon of frequency ω_p whilst excited to increase its own energy. If the electron is excited with a photon of frequency ω_i then when the electron radiatively relaxes the resulting phonon will have a frequency of

$$\omega_s = \omega_i + \omega_p. \tag{3.2}$$

This is still an example of inelastic scattering, although in this instance the scattered photon has gained energy with respect to the incoming photon. A schematic diagram showing these transitions is given in Figure 3.1. Whilst the overall effect is named Raman scattering, the case where energy is lost is called the Stokes shift, whereas when it is gained it is called the anti-Stokes shift [204]. From here on the discussion will focus on the Stokes shift variety of Raman scattering as this is the most intense at room temperature, and hence the most useful for the experimental procedures in this work. It is the most intense since, as phonon population is governed by the Bose-Einstein statistics discussed in Section 2.1.1, the majority of phonons are in their ground state, making creation more likely than annihilation. As the population is

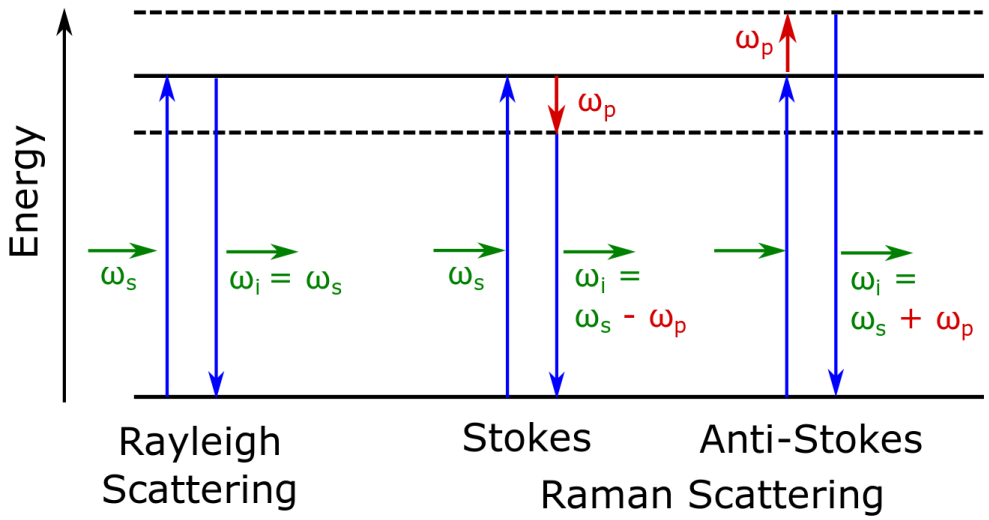


FIGURE 3.1. Diagram showing the quantum interpretation of the different forms of the scattering when light interacts with a crystal. The horizontal black lines represent electron virtual energy levels, and the green arrows represent photons with their frequency labelled. The dashed lines represent vibrational energy level which are accessed through electrons interacting with phonons, represented by the red arrows.

temperature dependent it is possible to use the ratio of Stokes scattered light to anti-Stokes scattered light to probe the temperature of a material, but this is not commonly used as it lacks precision [205].

Up until this point, this has been a quantum mechanical discussion of Raman scattering based on the creation and annihilation of quasiparticles. It is also possible to consider Raman scattering from a macroscopic perspective. The Raman scattering is an interaction between an electromagnetic wave and a crystal, meaning it is necessary for a vibration to induce a polarisation change for the vibration to be Raman active. This induced polarisation $\vec{P}$ is related to the incoming light which has electric field $\vec{E}$ and frequency ω through the relationship

$$\vec{P}(t) = \mathbf{R}\vec{E}e^{-i\omega t} \tag{3.3}$$

where $\mathbf{R}$ is the tensor of polarisability. As $\mathbf{R}$ is a tensor and $\vec{E}$ is a vector, the induced polarisation is also a vector, making it a directional quantity. A vibration which induces a stronger polarisation will result in a more intense scattering. Hence, as the intensity of the scattered light is proportional to the induced polarisation, if the elements of $\vec{P}$ are all zero there will be no light emitted (dark mode) and if the vector is a mixture of zero and non-zero elements the light will

only be scattered in the non-zero directions [206]. Raman scattering is generally stronger in more covalently bonded materials as the electrons are more loosely bound and hence the polarisability is higher [58]. The invention of the laser was a key enabler for many Raman scattering experiments as it allows intense, monochromatic, polarised, and collimated stimulation which enhances signal intensity and allows the study of directionally dependent Raman scattering [207].

In reciprocal space, light which is probing the crystal is represented by a wavevector rather than a wavelength. The wavevector k of a wave in a medium is given by

$$k = 2\pi \times n \times \omega \tag{3.4}$$

where n is the refractive index of the medium and ω is the frequency of the light in wavenumbers. The wavelength of the lasers used to stimulate the Raman emission in this work are 488 nm and 532 nm which equates to wavenumbers of approximately 10^5 cm^{-1} in GaN which is less than one thousandth of the Brillouin zone width of approximately 7×10^9 cm^{-1} meaning the light can only probe phonon modes at or very close to the Γ point, corresponding to $k = 0$. [207]. As was shown in Section 2.1.1, at the Brillouin zone centre the acoustic phonons have no energy, but the optical phonons do. Scattering by acoustic phonons is named Brillouin scattering, and appears very weakly in first order Raman scattering and can instead be probed through second order Raman scattering, where the light interacts with multiple phonons, although this effect is weak and hence the majority of Raman spectrsocopy is focussed on the optical phonons [208].

The phonon dispersion of GaN is shown in Figure 3.2 (a) [209]. Group theory can be used to produce the polarisability tensors $\mathbf{R}$ which, when normalised to volume become known as the Raman tensors $\mathbf{R}'$. The Raman tensor can then be used to predict the intensity of the Raman scattered light I_{RS} through the relationship

$$I_{RS} \propto | \vec{e_s} \mathbf{R}' \vec{e_i} |^2 \tag{3.5}$$

where $\vec{e_i}$ and $\vec{e_s}$ are the polarisation of the incoming and scattered photons respectively. In this work the Raman scattering measurements are performed exclusively in the backscattering geometry, meaning the probe light is at normal incidence to the sample, and the light which is scattered back along the same optical path is measured. If it is assumed that the sample is in the

xy plane, and the light is parallel to the z direction the incident light will have polarisation

$$\vec{e_i} = (\cos\theta \hat{e_{ix}}, \sin\theta \hat{e_{iy}}, 0) \tag{3.6}$$

and the scattered light must have a polarisation

$$\vec{e_s} = (-\sin\theta \hat{e_{sx}}, \cos\theta \hat{e_{sy}}, 0). \tag{3.7}$$

As discussed in Section 2.2, GaN and AlGaN, two of the primary materials studied in this work, have wurtzite crystal structures. This means they have a total of 6 optical phonon modes labelled A_1, B_1, E_1, and E_2, where the B_1 and E_2 modes both have high and low frequency variations. A sketch of these Raman modes is shown in Figure 3.2 (b). The high and low frequency varieties of the modes comes from the two atom basis, where if the higher mass atom is the one displaced the frequency will be lower, and vice versa. The B_1 modes are Raman inactive and so must be measured using IR absorption spectroscopy.

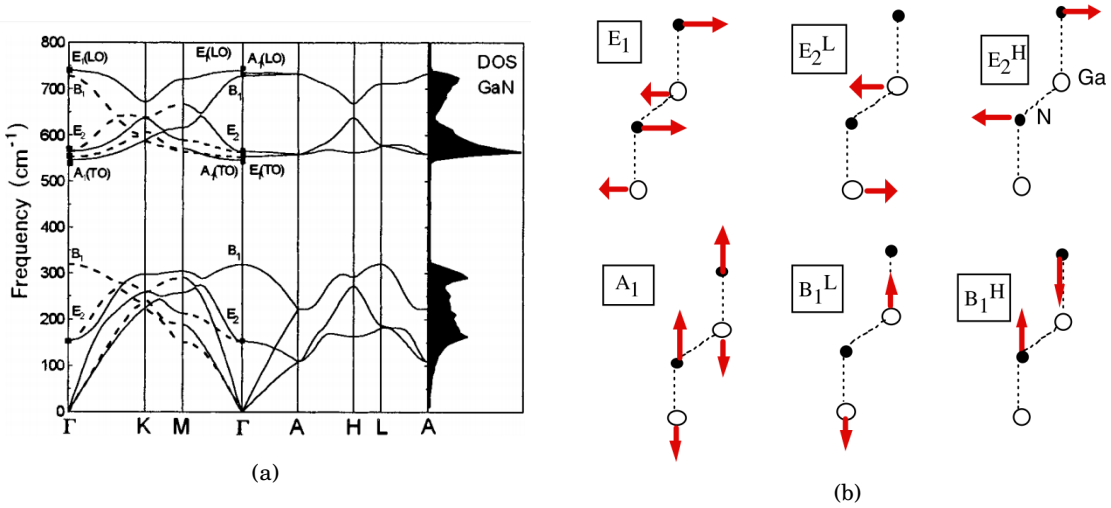
If it is assumed that the sample is a GaN wafer which has been grown along the c-axis, this will correspond to the z axis in the example above. The modes which are then measureable in the back-scattering geometry are the A_1(LO), E_2^H, and E_2^L, where the H and L superscripts refer to the high and low frequency variety of the E_2 mode, and LO denotes the longitudinal variety of the A_1 mode, meaning the oscillation is in the direction of the wave propogation. Both E_2 modes are unpolarised, wheres the A_1(LO) mode is polarised, which can be seem in the Figure 3.2 (b), as this is the only mode which oscillates along the c-axis [58]. The Raman tensors for these modes are,

$$A_1 = \begin{pmatrix} a & - & - \\ - & a & - \\ - & - & b \end{pmatrix}, \quad E_2^L = \begin{pmatrix} c & - & - \\ - & -c & - \\ - & - & - \end{pmatrix}, \quad E_2^H = \begin{pmatrix} - & c & - \\ c & - & - \\ - & - & - \end{pmatrix}, \tag{3.8}$$

where a, b, and c are constants.

3.1.2 Raman thermography

In this work Raman thermography is used to measure temperature in operating transistors. Two variations of the technique will be used, micro-Raman thermography is used on AlGaN HEMTs to measure the temperature of the device buffer, and nanoparticle assisted Raman thermography,



(a) (b)

FIGURE 3.2. (a) The phonon dispersion curve and density of states for high symmetry directions in GaN adapted from [209]. Also labelled along the Γ direction are the phonon modes. Reprinted with permission from Elsevier. (b) Schematic representations of the unit cell vibrations corresponding to each phonon mode. The nitrogen atoms are shown in black whereas the gallium is in white. This image is adapted from Harima [58]. Reprinted with permission from AIP Publishing.

which uses anatase nanoparticles as thermometers to measure the surface temperature of $\beta - Ga_2O_3$ MOSFETs and GaN-on-Diamond HEMTs, as well as to characterise the thermal conductivity of diamond films.

The $A_1(LO)$ and E_2^H Raman modes are most commonly used for temperature measurements due to their relative intensity and temperature dependence [210]. It was shown in Section 2.1.1 how the vibrations of a crystal lattice can be found by a simple 'ball and spring' approximation, and it is the resonant modes of these vibrations that are probed in Raman spectroscopy. As the system is similar to a simple harmonic oscillator, the normal frequencies ω of the vibrations obey

$$\omega \propto \sqrt{\frac{C}{m}}, \tag{3.9}$$

where C is the spring constant and m is the average mass of the oscillators. In the case of a real crystal, C represents the bonding, and if the bond length is increased the crystal 'spring constant' will decrease and so will the normal frequency. When a crystal undergoes a temperature change, the anharmonicity of the inter-atomic potential results in a change in the lattice constant, typically decreasing the 'spring constant' and hence the Raman frequency. As both strain and

temperature can change the lattice constant and hence the 'spring constant', Raman spectroscopy is an effective technique for probing both [211, 212]. However in the case of micro-Raman thermography of GaN or AlGaN based devices it is necessary to decouple the strain induced Raman shift from the temperature induced Raman shift to ensure temperature measurements are accurate [213]. When the device is operated, the strain will increase through two mechanisms. First, the temperature increase in the device will cause the buffer layers to expand, and if they are on a non-native substrate the rates of expansion of the two materials will be different, resulting in a thermomechanical strain. Secondly, there will be an added component to the strain due to the piezoelectric effect. Biasing the device will create an electric field in the GaN buffer, which will then induce an electromechanical strain because of the inverse piezoelectric effect [214].

The temperature induced change in the phonon frequency $\Delta\omega$ follows the Cui equation

$$\Delta\omega = \omega_0 - A(e^{B\hbar c\omega/k_b T} - 1) \tag{3.10}$$

where ω_0 is the Raman frequency at 0 K, h and k_b are Plancks and Boltzmann constant respectively, c is the speed of light and A and B are empirical fitting parameters [215]. In the high temperature case, this approximates as a linear function

$$\Delta\omega = \frac{-Ak_b\Delta T}{Bhc\omega_0}. \tag{3.11}$$

Because of the static component of the strain, the parameters ω_0, A, and B will vary depending on how the sample was prepared. Therefore it is necessary to calibrate each different type of sample by measuring the Raman modes over a range of temperatures. The inverse piezoelectric effect-induced electromechanical strain can be accounted for by measuring the induced shift in the Raman frequency whilst the device is pinched OFF, since in this case there is still a high electric field but no current is flowing so there should be no temperature increase. A relationship between drain voltage and Raman frequency can then be found and used to calibrate the temperature measurements. Bagnall and Wang reported that this effect could be as large as 0.4 cm^{-1} for drain biases of 50 V and above, meaning that if this effect is not accounted for it can result in inaccurate temperature measurments. The thermomechanical strain is more difficult to account for. It is necessary to measure at least two phonon modes for a range of device operating conditions. Then, as each mode will have an individual response to each of the temperature and thermomechanical

strains it is possible to decouple the two through simultaneous equations. If this approach is not taken, it can result in errors of approximately ±5°C when temperature rises are of the order of 200°. Whether the thermomechanical strain causes and increase or decrease in the calculated temperature depends on whether the GaN layer is in compressive or tensile strain.

3.1.3 Renishaw Invia spectrometer

All Raman scattering based measurements in this work were performed using a Renishaw Invia spectrometer, a schematic of which is shown in Figure 3.3. The sample itself is placed on a steel stage which is below the microscope objective. This stage is large enough to support probe micro-positioners which attach magnetically to the stage, allowing the device under test to be operated during the measurement whilst preventing the micro-positioners from drifting. The micro-positioners themselves allow micron scale, 3-axis translation of the probe, which is typically a tungsten needle probe. The microscope has a lamp attached to illuminate the sample, and a camera interfaced with a computer to allow the sample to be viewed. When the device is under test, the light from the lamp is blocked such that only the laser light is incident on the sample, reducing noise.

Two separate laser sources were used; a frequency doubled Nd:YAG laser emitting at 532 nm and the 488 nm line of an Argon ion laser. These enter the spectrometer behind Mirror A in Figure 3.3. The Mirrors A and B are both used to direct the beam path and ensure the correct optical alignment for the proceeding components. The beam expander is adjustable, allowing the beam waist of the laser to be varied, which will change the focal plane of the laser once it goes through the focussing objective. In the preparation of the system it is vital to ensure that the focal planes of the imaging camera and the laser are the same. As the sample cannot be viewed during the measurement, the sample must be brought into focus using the white light. Then, when the measurement begins, the laser is also focussed on the sample if the two focal planes have been adjusted so that they are coincidental. The Raman scattered light follows back along the same optical path as the laser until it reaches the filters. These are notch filters which attenuate the laser light, allowing the scattered light, which is of a much lower intensity, to pass. As it is a notch filter, rather than a low pass or high pass filter, both the Stokes and anti-Stokes

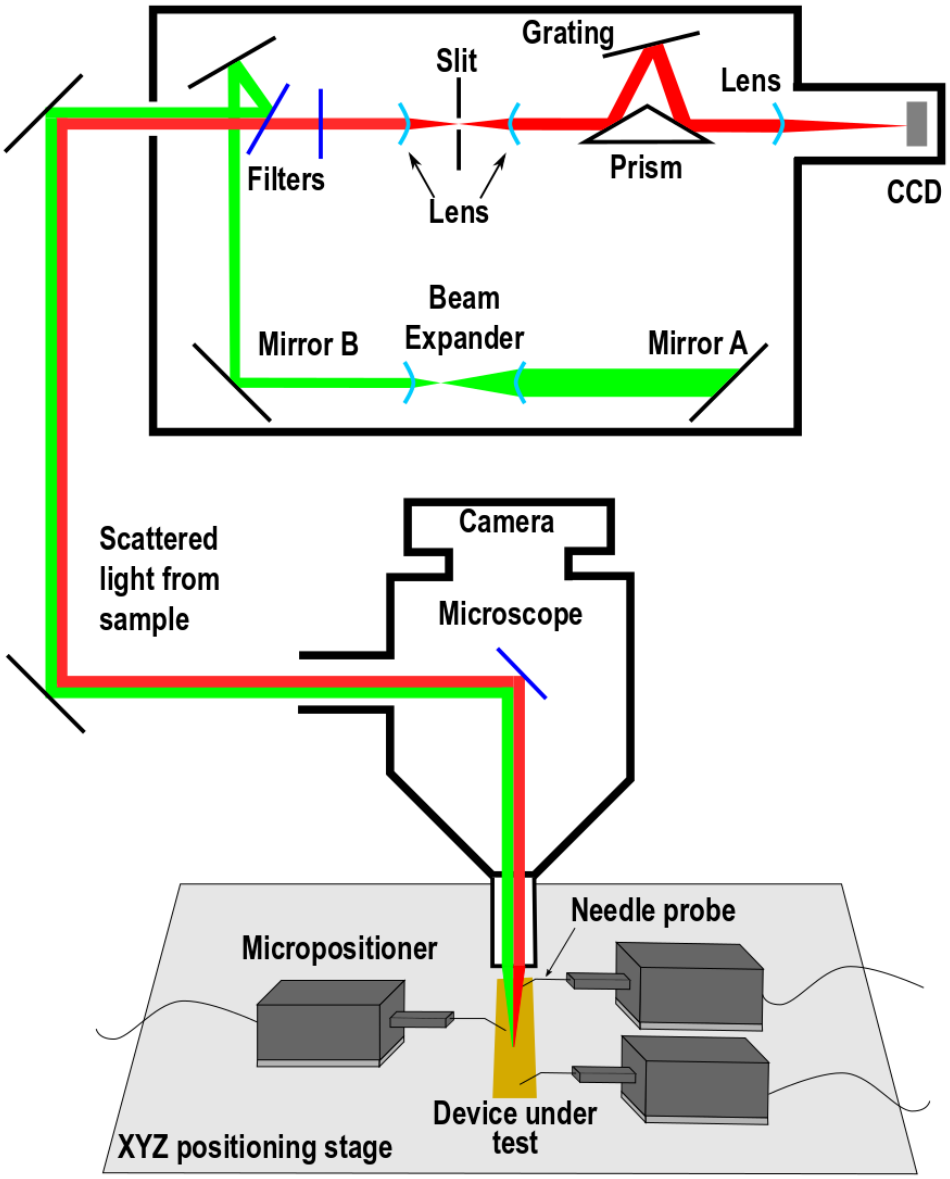


FIGURE 3.3. Schematic diagram showing the key components of the Renishaw Invia spectrometer used for micro-Raman thermography, nanoparticle assisted Raman thermography, and phonon lifetime measurements. The laser light enters the spectrometer behind Mirror A, and the measurement is made at the CCD. The green line shows the incident light, and the red line shows the reflected light. Black components are reflecting, dark blue components are filters, and light blue components are lenses. Needle probes are used to operate the devices.

shifts are measurable.

Next the scattered light is focussed onto the slit whose width can be adjusted to improve the lateral resolution of the measurement. Light which is from the centre of the laser spot will be collimated after it has passed the filters and hence will be focussed effectively by the lens. The light away from the centre of the spot will be divergent so it will not be focussed to a sharp point at the slit. The divergence of the light is proportional to its distance from the laser spot on the sample, and narrowing the slit width reduces the amount of divergent light which can pass. This improves the spatial resolution of the measurement but it also reduces the signal strength, so the optimal slit width should be determined based on the experiment.

Once it is past the slit, the light is collimated by the second lens and reflected off the prism onto the reflective diffraction grating. The grating is used to disperse the light so that the wavelengths can be distinguished later. The grating has a ridged or 'lined' surface with a separation d between the lines. Constructive interference will occur at an angle θ which satisfies the relationship

$$\lambda = d \sin\theta \tag{3.12}$$

where λ is the wavelength of the scattered light. For each wavelength which is incident on the grating, there will be a different corresponding θ, meaning the different wavelengths become spatially separated. If a grating has a higher density of lines, leading to a lower value of d, the dispersion of the wavelength is increased. This increases the spectral resolution of the measurement but also decreases the spectral measurement window. The diffraction grating can be replaced in the spectrometer with a high line per millimetre value desirable for analysis of individual peaks, and a lower line per millimetre value preferred for the measurement of multiple peaks simultaneously.

The dispersed light is then focussed at the final lens on to the charge coupled device (CCD). The CCD is an array of pixels, where each pixel is a capacitor. The measurement begins when the shutter is opened. When a photon is incident on a pixel, the photoelectric effect is used to free an electron which then adds charge to a capacitor. Once the measurement is complete the shutter closes, and the charge on each pixel is measured. The CCD is cooled by a Peltier device to $-70°$C to limit the thermally activated carriers intrinsic to the CCD, which improves the signal-to-noise

ratio of the experiment. The longer the shutters are open (the integration time), the more photons are incident on the CCD, increasing the signal. However there is a limit to the amount of charge which can be stored on the capacitor, and if the number of photons is too great, the detector will be saturated and no further photons can be recorded. If this threshold is reached without the signal being sufficiently clear, an alternative is to repeat the measurement at a lower integration time and aggregate the data. Alternatively the signal-to-noise ratio can be improved by increasing the slit width to allow more scattered light through, or reducing the stray light which is incident on the CCD to reduce the noise level. The wavelength which corresponds to each pixel must be calibrated before the measurement. This is done using a reference silicon sample which has a known Raman spectral line at 520.3 cm^{-1}. As silicon is available with an exceedingly high crystal quality the repeatability of the measurement is high, making it ideal for calibration. Care must be taken to ensure the laser does not heat the sample as this will cause the spectral line to shift.

All Raman thermography measurements in this work are performed using scanning confocal set ups. This means each measurement is of a single point in the device and the resolution of each measurement is determined by the point spread function. When the focus is diffraction limited the lateral resolution r_{lat} is given by

$$r_{lat} = \frac{0.51\lambda_i}{\mathrm{NA}} \tag{3.13}$$

where λ_i is the wavelength of the laser and NA is the numerical aperture of the focussing objective [216]. For all Raman scattering measurements in this work a 50× focussing objective is used which has an NA of 0.6, giving a spot size of approximately 0.4 μm for the excitation sources used in this work. As GaN is transparent to most common laser wavelengths it is necessary to consider the axial sampling depth. However as this tends to be a few microns, which is significantly larger than the GaN buffers looked at in this work, it can be assumed that the measured Raman modes are an average over the entire depth of the buffer [213]. The measurement depth will lead to significant contributions to the spectra from the substrate. To get the peak temperature of the device, these measurements are then compared with finite element models of the system. To minimise the extrapolation necessary, it is typical to measure the Raman shift as close as possible to the gate edge, although the temperature gradient can reach close to 100 K/μm in the device, making a significant extrapolation necessary when calculating the peak temperature in a device

from the Raman thermography measured temperature [213].

3.1.4 Nanoparticle assisted Raman thermography

Nanoparticle assisted Raman thermography is used as both an alternative and a complimentary technique to micro-Raman thermography. The nanoparticles can be used as a nano-thermometer when the material whose temperature to be tested is not Raman active and they can provide surface temperatures as oppose to bulk measurements. The process for temperature measurements with nanoparticle assisted Raman thermography is much the same as the process described in 3.1.3.

The measurement is performed using the same experimental set up as described in Section 3.1.3, but instead of measuring the GaN buffer, nanoparticles are deposited on the device surface to act as nano-thermometers. Nanoparticle assisted Raman thermography has been performed using silicon nanowires, diamond nanoparticles, and titanium dioxide nanoparticles in the anatase allotrope, the latter of which will be used in this work [33, 175, 217]. Anatase has a ditetragonal pryamidal structure which gives it 6 Raman active modes, the most intense of which is the low frequency E_G mode which occurs at approximately 144 cm^{-1} [218]. This peak also shows a strong temperature dependence with approximately 8 cm^{-1} change between 200 K and 600 K [219]. A strong temperature dependence is important for Raman measurements as it reduces the percentage error which is propagated from the Raman shift calculation. When using nanoparticles, the room temperature phonon frequency can vary as the particles all have different amounts of inherent strain, but the temperature dependence remains consistent and can be fit by a quadratic function.

For deposition, the nanoparticles are suspended in an organic solvent such as methanol and drop cast onto the sample. Dilution is used to achieve the optimal density of approximately 5 g/l of nanoparticles and the sample is heated to increase the rate of solvent evaporation when the solution is deposited which helps the uniformity of the coverage and prevents 'coffee ring' effects. The nanoparticles are typically less than a micron in diameter, allowing good spatial resolution. The size of the nanoparticles means there is negligible heat transfer from them to the surroundings, making them an accurate probe for the surface temperature [220]. Avoiding

agglomeration of the nanoparticles is important, as thick layers may have a temperature gradient which results in the measured temperature being lower than the surface temperature. The small size of the nanoparticles means that they are easily heated by the optical stimulus, and therefore lower laser powers must be used. However, it is desirable to use the highest laser power possible to enhance the signal, as the nanoparticles small size means the amount of light incident on them is low. It is therefore necessary to find the highest laser power which does not cause the temperature of the nanoparticle to increase. For this, the nanoparticle is measured first at a high laser power, which is then decreased in subsequent measurements. When there is no change in the Raman shift between successive measurements, the point of no laser heating, and hence the maximum laser power which can be used, is found. The slit width can also be widened to increase the Raman signal. In the case of micro-Raman thermography the slit width must be used to control the spatial resolution of the measurement, but that is not the case with nanoparticle assisted Raman thermography as the spatial resolution is determined by the particle size.

The fact that the nanoparticles act as a thermometer for the sample surface is a key advantage of this technique when compared to micro-Raman thermography, as the surface temperature, particularly if the nanoparticles are on the gate, is closer to the device channel temperature, making extrapolation to the peak temperature easier [221]. It is of particular use for devices where the active layers are on a native substrate, as in this case the micro-Raman thermography measurement will be an average over several microns depth. The nanoparticles do not have an inverse piezoelectric stress to contribute to the Raman shift. The downside of nanoparticle assisted Raman thermography is the lack of control over the nanoparticle deposition. This means it is not possible to produce a fine map of the device access region. The nanoparticles are also non-trivial to remove, although as they do not impact device performance this is only a minor issue.

3.2 Photoluminescence

Photoluminescence is the emission of light due to optical stimulus. When a photon is incident on a semiconductor, it can interact with the electrons present in that material. If the photon is

absorbed the electron will gain energy E equivalent to

$$E = hf \tag{3.14}$$

where h is Planck's constant, and f is the frequency of the incoming photon. Depending on the frequency of the light, this energy can be sufficient to excite the electron to higher energy levels, such as any defect states that are present or the conduction band. The electron will then relax back to its ground state. If it interacts elastically it can fall directly from the conduction band to the valence band, and emit a photon in the process whose energy is equal to the bandgap. Alternatively it can decay via defect levels in which case the photon released will have energy equivalent to the energy difference between the defect level and the valence band, or it can decay non-radiatively though interactions with phonons. Because of these properties, photoluminescence is a widely used technique for characterisation of semiconductor crystals [222, 223].

Photoluminescence can also be used for temperature measurements since, as described in Section 3.1, the lattice parameter is temperature dependent. When the lattice expands, the increased lattice parameter results in a reduced bandgap as there is less overlap between the electronic orbitals of the neighbouring atoms [224, 225]. The temperature dependence of the bandgap energy E_G is given by the modified Varshni equation

$$E_G = E_0 - \frac{\alpha T^2}{T + T_0} + \frac{1}{2} k_b T, \tag{3.15}$$

where E_0 is the bandgap at 0 K, and α and T_0 are fitting parameters which can be found from calibration with a thermal stage [226]. The first two terms of the right hand side are the original Varshni equation which is an empirical fit to the experimental data. The final term on the right hand side is then an addition to account for the kinetic energy of the electrons whilst they are in the conduction band before they relax back to the valence band.

As the bandgap is being probed, the laser used to excite the photoluminescence must have an energy greater than the bandgap. For probing GaN devices this means the laser wavelength must be less than 364 nm to excite carriers from the valence band to the conduction band. When performing temperature measuments, photoluminescence has the advantage of producing a stronger signal than micro-Raman thermography since it is a first order process, Raman scattering requires the interaction of the incoming photon with the electrons and with a phonon, whereas

with photoluminescence it only needs to interact with the electron. Photoluminescence also probes the surface temperature rather than averaging through the buffer depth, giving it an advantage as the measured temperature is closer to the peak temperature in the device. However as electrons are excited into the conduction band the measurement impacts the operation of the device, increasing the current and heating the device beyond its standard operating temperature. This means the device must be tested with different laser powers and the temperature measurements extrapolated to the case of no laser power [227].

A 325 nm HeCd UV laser is used as the excitation source. As a result, the measurements were performed on a system that was similar to that described in Figure 3.3, but with UV compatible components. The laser spot is not visible to the eye or the camera systems available, so an alignment routine, separate to that described in Section 3.1.3, is necessary. To ensure that the focal plane of the UV laser is the same as the focal plane of the camera, the laser was directed onto a smooth reflecting surface such as a metal contact pad. The beam path was then adjusted to avoid any absorbing or dispersive optical elements such as the filters and the grating. The remaining image on the UV-enhanced CCD is therefore a direct reflection of the laser. The beam expander could then be adjusted to change the focal plane of the laser resulting in a change in the laser spot seen at the CCD, allowing it to be optimised to the smallest possible spot. The spot size can then be determined by a knife edge measurement, where the laser spot is scanned over a sharp edge of a metal structure on a GaN wafer and the photoluminescence intensity recorded. When the laser spot is entirely on the contact the intensity will be effectively zero, and there will be a maximum intensity when the laser spot is solely incident on GaN, with a transition in between. The width of this transition region gives the spot size of the laser. The smallest possible step size of the motorised stage in this setup is 1 μm, so the alignment was considered successful when the intensity of the photoluminescence went from zero to maximum in one step, meaning the spot size is less than 1 μm. The minimum spot size and hence the lateral resolution will again be limited by Equation 3.13.

For the photoluminescence measurements a 40× reflecting focussing objective is used which has a NA of 0.5, resulting in a theoretical minimum spot size of 0.33 μm. The photoluminescence spectra is then measured in the device channel, looking for emission of energy equal to the

material bandgap. As the photoluminescence peak is asymmetric, a reliable fitting routine is difficult to implement and so the peak value is found through observation, with a precision of less than 0.003 eV. This result can then be input into Equation 3.15 to find the temperature. The most typical way to determine the random error associated with the measurement is to repeat the measurement several times and find the standard error on the mean. As is the case with the Raman thermography, a measurement can be performed to ascertain the chip temperature for a given power density. This can then be subtracted from the temperature measured in the channel to give a more complete picture of the temperature rise in the device. The penetration of a 325 nm laser in GaN is of the order of tens of nanometres, meaning the measurement is effectively a probe of a surface spot of diameter 1 μm.

3.3 Transient thermoreflectance

Transient ThermoReflectance (TTR) exploits the temperature dependence of the dielectric constant and therefore the refractive index of a material to use the reflectance as a temperature probe. The relationship between the refractive index and the permittivity of a medium will first be shown. This will be followed by a derivation of the temperature dependence of the permittivity. Finally the relationship between the reflectance of a surface and the refractive index will be shown, completing the picture of how the temperature dependence of the reflectance can be utilised. The refractive index, n, is a dimensionless quantity which describes the relative speed of light in a material, v, compared to in a vacuum, c, determined by

$$n = \frac{c}{v}. \tag{3.16}$$

The speed of light in a material can be derived from Maxwell's equations if it is assumed that there is no free charge present

$$\nabla \times \vec{E} = -\mu \frac{\partial \vec{H}}{\partial t}, \tag{3.17}$$

$$\nabla \times \vec{H} = \epsilon \frac{\partial \vec{E}}{\partial t}, \tag{3.18}$$

$$\nabla \cdot \vec{E} = 0, \tag{3.19}$$

$$\nabla \cdot \vec{H} = 0, \tag{3.20}$$

where $\vec{H}$ is the magnetic field, $\vec{E}$ is the electric field, ϵ is its permittivity, μ is its permeability and, t is time [228]. By taking the curl of Equations 3.17 and 3.18 it can be found that

$$\nabla \times \nabla \times \vec{E} = -\mu \frac{\partial(\nabla \times \vec{H})}{\partial t}, \tag{3.21}$$

and

$$\nabla \times \nabla \times \vec{H} = \epsilon \frac{\partial(\nabla \times \vec{E})}{\partial t}. \tag{3.22}$$

By applying the 'curl of the curl' identity, which states that the curl of the curl of a vector field is equivalent to the gradient of the divergence of the vector field minus the Laplacian of the vector field, on the left hand side of these equations and substituting Equations 3.17 and 3.18 into the right hand side these become

$$\nabla(\nabla \cdot \vec{E}) - \nabla^2 \vec{E} = -\mu\epsilon \frac{\partial^2 \vec{E}}{\partial t^2} \tag{3.23}$$

and

$$\nabla(\nabla \cdot \vec{H}) - \nabla^2 \vec{H} = -\epsilon\mu \frac{\partial^2 \vec{H}}{\partial t^2}. \tag{3.24}$$

By implementing Equations 3.19 and 3.20 on the left hand side of these equations they reduce to

$$\nabla^2 \vec{E} = \mu\epsilon \frac{\partial^2 \vec{E}}{\partial t^2} \tag{3.25}$$

and

$$\nabla^2 \vec{H} = \mu\epsilon \frac{\partial^2 \vec{H}}{\partial t^2} \tag{3.26}$$

which can be recognised as the Wave Equation with velocity

$$v = \frac{1}{\sqrt{\mu\epsilon}}. \tag{3.27}$$

Therefore the velocity of light in a medium is dependent on the permittivity of that medium. As a result, the refractive index must also be dependent on the permittivity, following from the relationship shown in Equation 3.16.

It is the temperature dependence of the permittivity which provides the basis of the TTR measurement. The permittivity is a measure of how a material responds to an applied electric field and as such the refractive index is closely linked to the band structure and the bandgap E_g via the Moss formula which approximates

$$n^4 \times E_g = \xi \tag{3.28}$$

where ξ is a constant [229]. It was discussed in Section 3.2 how the bandgap is temperature dependent. This can now be viewed by study of the relative permittivity ϵ_r which is the ratio of a medium's permittivity and the permittivity of free space, also known as the dielectric constant. Approximating a static dielectric constant, the Lorentz-Lorenz Law states that

$$\frac{\epsilon_r(T)-1}{\epsilon_r(T)+2} = \eta\rho(T) \tag{3.29}$$

where η is a constant and ρ is the density of the medium, then taking the derivative of this with respect to temperature gives [230]

$$\frac{d\epsilon_r}{dT} = \frac{1}{3}(\epsilon_r-1)(\epsilon_r+2)\frac{1}{\rho}\frac{d\rho}{dT}. \tag{3.30}$$

The end term in this equation is a change in density with respect to temperature, as would occur when the lattice thermally expands. Hence if the change in refractive index can be measured, this will give a measure of the change in temperature.

As is implied by the name, TTR uses the reflectivity of material to measure the temperature change. The Fresnel equations give the amplitude for the reflected light, r, at an interface between two materials with refractive indices n_1 and n_2,

$$r_s = \frac{\cos\theta - \sqrt{n^2(T)-\sin^2\theta}}{\cos\theta + \sqrt{n^2(T)-\sin^2\theta}}, \tag{3.31}$$

$$r_p = \frac{-n^2(T)\cos\theta - \sqrt{n^2(T)-\sin^2\theta}}{n^2(T)\cos\theta + \sqrt{n^2(T)-\sin^2\theta}}, \tag{3.32}$$

where the subscripts represent the polarisation of the light, n is the ratio of n_2 to n_1 and θ is the angle of incidence. In the TTR measurements performed in this work the laser light is at normal incidence to the sample surface and the sample is always in air, which has a refractive index of one, reducing Equations 3.31 and 3.32 to

$$r = \frac{n_2(T)-1}{n_2(T)+1}, \tag{3.33}$$

where the amplitude of the reflected light is now independent of the incoming polarisation [228]. This, coupled with the temperature dependence of the refractive index allows the use of reflected intensity to measure temperature.

Jellison and Burke found that the change in refractive index is linear with respect to temperature following the relationship

$$n(\lambda, T) = n_0(\lambda) + a(\lambda)T, \tag{3.34}$$

where n_0 is the refractive index at 0 K and a is the thermo-optic coefficent [231]. The thermo-optic coefficient is the derivative of refractive index with respect to temperature $\frac{\partial n}{\partial T}$, and dictates the magnitude of the reflection change for a given temperature change. In the case of GaN, which is measured in this work, this thermo-optic coefficient is approximately 1×10^{-4} K^{-1} at the wavelength used in this experiment, 532 nm [232]. This is larger than the thermo-optic coefficients of AlN (0.4×10^{-4}), ZnSe (0.8×10^{-4}), and diamond (0.16×10^{-4}) at similar wavelengths [232–234]. This makes GaN a suitable semiconductor for TTR, as a larger thermo-optic coefficient results in a larger signal-to-noise ratio. The thermo-optic coefficent also increases as the band-edge is approached making shorter probe wavelengths preferable. A possible alternative to improve the signal-to-noise ratio is to coat the sample surface in a metal such as gold, which has a thermo-optic coefficient of -3×10^{-4} at 532 nm [106]. Whilst this may increase the signal seen in experiment, it is not a preferred solution as the deposition of gold damages the GaN and prevents the fabrication of devices on the samples after they have been measured. The extra gold layer also reduces the fitting sensitivity of the system since it introduces an extra parameter to the material system which must be fit, namely the thermal boundary resistance between the gold and the GaN.

A schematic diagram of the experimental set-up used in this work is shown in Figure 3.4. The experiment used a continuous wave frequency doubled Nd:YAG laser at 532 nm to monitor the reflectance. The sample is heated using a pulsed, frequency tripled Nd:YAG laser at 355 nm which has a pulse width of 9 ns and a repetition rate of 30 kHz. The two lasers were combined at a dichroic filter which transmitted the green laser but reflected the UV laser. This filter was adjusted such that the two beams were concentric. Before this dichroic filter, the UV laser passes through a beam expander, making its beam waist significantly larger than that of the green laser. The two lasers then enter the microscope and pass through a 15× focussing objective lens before reaching the sample. Due to the difference in beam waist, the lasers have different focal planes. This distance between the sample and the lens is adjusted such that the green laser is at its focal

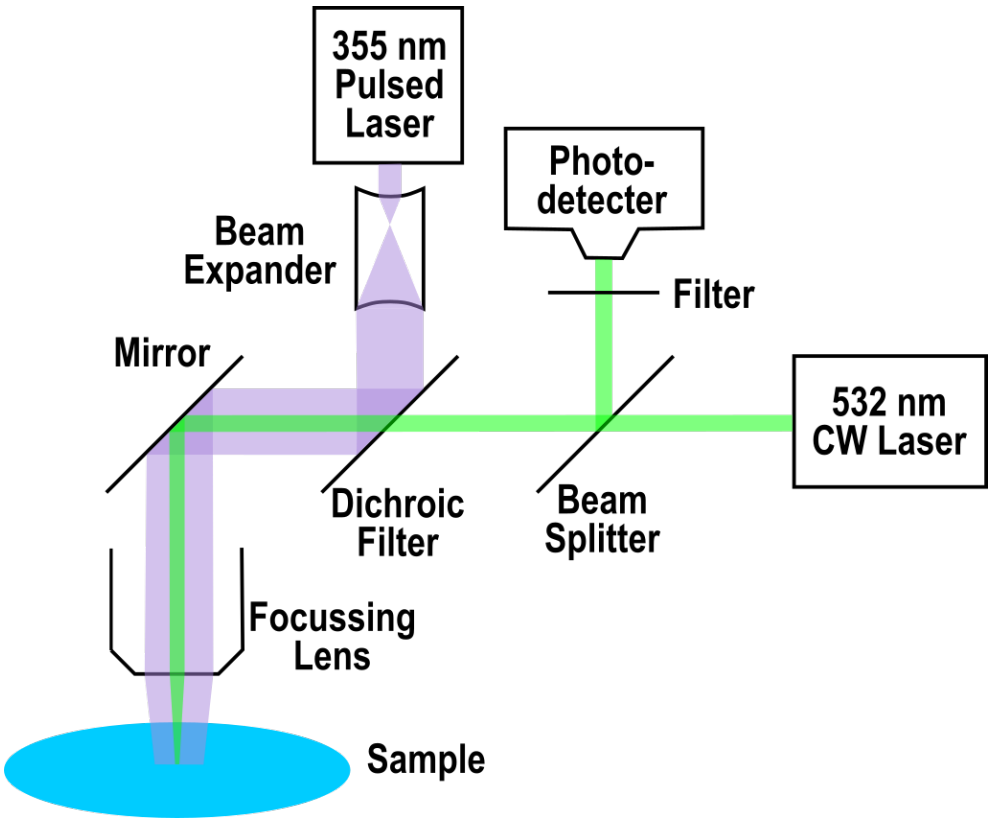


FIGURE 3.4. Schematic diagram of the TTR experimental setup used in this work. The 355 nm pulsed laser is used to heat the sample. It has a 9 ns pulse width and 30 kHz repetition rate. It is expanded such that its spot size is much larger than that of the 532 nm continuous wave (CW) laser which is used to monitor the reflection from the sample surface. This reflection is used to determine the temperature at the sample surface.

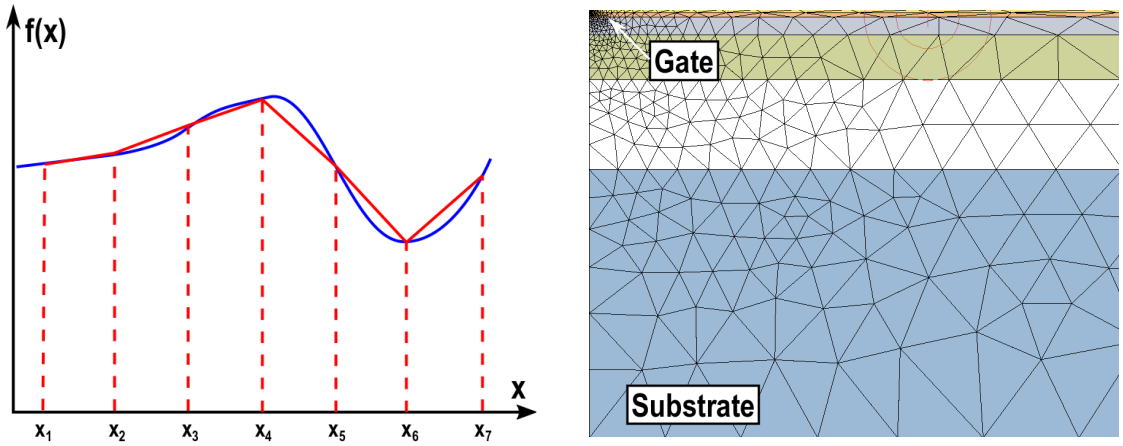
point with a spot size of approximately 2 μm, which results in a corresponding UV spot size of 70 μm. The reflected light then follows back along the same beam path. The UV and green light is this time separated at the dichroic filter, and a beam splitter is used to direct the reflected light through a final filter, to a detector.

The data are averaged over 60 000 laser shots. They are then fit using an analytical model which replicates the heating pulse of the laser and calculates the surface temperature based on how the heat flows through the wafer stack. The model was developed by a colleague Dr Anaya. The alignment is such that the probe laser is at the centre of the pump laser spot, meaning it is also possible to apply axial symmetry to the calculations. Also, since the pump laser spot is significantly larger than the probe laser spot, a transmission line model can be

applied which uses current and voltage as analogies for heat flux and temperature [189, 235]. A heat source is defined on the sample surface, and the heat flow is allowed to evolve following Fourier's law through each layer in the system, which are represented by thermal resistors and capacitors. Where well defined literature values were available, the material's parameters in the model were fixed. As it is a transient solution, each material must have a heat capacity, density, thermal conductivity, and thickness defined. The model cannot take into account inhomogeneity in material properties. In the case of a GaN-on-Diamond wafer, the GaN thermal conductivity could be defined as 160 W/m.K, and the diamond thermal conductivity as 1500 W/m.K, to represent polycrystalline diamond. The heat capacity and density of these materials are well defined, leaving only the interface layer parameters to be input. The density and heat capacity can be approximated as that of silicon nitride, but as this layer is so thin, the model is not sensitive to these parameters. The only remaining free parameter is then the thermal conductivity of the interface layer. As discussed in Section 2.5, the TBR_{eff} is an amalgamation of the thermal resistances of the diamond nucleation layer, the dielectric layer, and the material interfaces. The interface thermal conductivity in the model takes all of these into account, so it is the inverse of the effective thermal boundary resistivity. The validity of the model was confirmed by a comparison to a finite element simulation of the experiment developed in ANSYS which yielded the same results.

3.4 Finite element analysis

Throughout this work, finite element analysis is a vital tool to complement the experimental work performed. The finite element method was developed as a method of numerically solving complex problems over a geometry. It works by discretising a body into finite sized elements connected at nodes to form a mesh. The relevant equations are solved at the nodes to find the variable of interest and the results are interpolated in the elements. As the solution is calculated at discrete points in space, the spatial derivatives are equal to zero, simplifying the partial differential equations of the system. The interpolation is then an approximation of the dependent variable at all points between the nodes. A linear interpolation is computationally less intensive but is less



(a) (b)

FIGURE 3.5. (a) A 1D example of the principles behind a finite element simulation. The blue line represents the true solution of the function f(x). The red line is the approximate solution found from an interpolation of the solution at discrete intervals. It can be seen that the finite element approximation is more accurate when the gradient is smaller. (b) An example mesh of a simple transistor. The gate is in the top right corner, and the mesh is more dense here as this is where the temperature gradient is highest.

accurate than a quadratic interpolation.

This makes the mesh design particularly important. A mesh with smaller node-to-node separations is desirable as this reduces the amount of interpolation necessary, and a mesh with the nodes spaced too far apart will result in inaccurate simulations. However a denser mesh has a counteracting effect, as the number of times the differential equations must be solved expands, increasing the computation time. Therefore a balance must be struck on the spacing of the nodes, with the optimal mesh being the one which gives an accurate result in the fastest time. To achieve this, the density of the mesh can be varied in different areas of the simulation.

As seen in Figure 3.5 (a), the interpolation is more accurate when the gradient of the function is lower. Taking the example of self-heating in a simple transistor structure shown in Figure 3.5 (b), the mesh around the gate should be much more dense as this is where the temperatures are highest and there is a large temperature gradient. Conversely, in the sample holder the temperatures are close to ambient and the temperature gradients are low. This allows a more coarse mesh to be used, which can greatly reduce the number of nodes as the volume of the

sample holder is much larger than that of the gate. To confirm that the mesh is at its optimal configuration, an iterative process can be used where the temperature is calculated for a series of meshes, each more fine than the last. As the mesh gets finer, the temperature is calculated at more points, meaning the solution tends towards the case where the the temperature is calculated at all points, which would be the true solution of the system. Therefore increasing the mesh density gives temperature values which are convergent towards this true value. It will be an asymptotic approach towards the true value, meaning the solution from two meshes will never be exactly the same, but the mesh was deemed sufficiently fine once a significant change in mesh density resulted in temperature discrepancies of less than 0.1°C. As a final step to improve accuracy, nodes can be inserted at the element edge midpoint.

The element shapes can either be cuboids or tetrahedrons. Tetrahedrons are the most commonly used as they are simplex, meaning they can be used to fill any 3 dimensional shape, which is not true of cuboids. However tetrahedrons are not efficient at filling spaces which have a high aspect ratio, meaning one dimension of the body is either much smaller or much larger than the others. For this reasoning, cuboids are typically used to build the mesh in and around the gate, whereas tetrahedrons may be used to mesh the sample holder. There were two computers available for computing the finite element simulations; the first had 16 GB of RAM with a quad core Intel I7 processor and the second had 32 GB of RAM and the same quad core Intel I7 processor. The higher RAM PC could compute simulations whose meshes had upto approximately 3 million elements. This was sufficient for all the simulations performed in this work.

The software used for this work is ANSYS academic release [236]. This allows both steady state and transient analysis of heat flow in systems, and the following is a discussion of the physics used to solve these problems. The first law of thermodynamics states that energy must be conserved. In the case of a 3D body where mass is conserved and the heat is generated in a portion of that body, the first law of thermodynamics can be expressed as

$$\rho c\Big(\frac{\partial T}{\partial t} + \vec{v}\nabla T\Big) + \nabla \cdot \vec{q} = \dot{U}, \tag{3.35}$$

where ρ is the density of the material, c is its specific heat capacity, T is the temperature, $\vec{v}$ is the heat velocity vector, $\vec{q}$ is the heat flux vector, and $\dot{U}$ is the rate of heat generation per unit

volume. ANSYS solves this by using Fourier's law which states

$$\vec{q} = -\kappa_{ij}\nabla T \tag{3.36}$$

where κ is the thermal conductivity and is in matrix form since it can be anisotropic. Combining these two equations then gives

$$\rho c\big(\frac{\partial T}{\partial t} + \vec{v}\cdot\nabla T\big) = \nabla\cdot(\kappa_{ij}\nabla T) + \dot{U} \tag{3.37}$$

which is solved numerically in ANSYS, meaning each material requires an input thermal conductivity, density, and heat capacity. This is a transient equation, but when the system is in a steady state the terms on the left hand side become zero and it essentially reduces back to Fourier's law. In this case, only the thermal conductivity matrix κ_{ij} and the heat source $\dot{U}$ is needed to be input.

Once the design and the mesh are completed, the thermal energy can be input into either surfaces or volumes. The boundary conditions and initial conditions are essential for the solution of the partial differential equations to be solved. Typically the initial conditions are given by setting the entire geometry at the ambient temperature. The boundary conditions must be selected for all exterior surfaces. There are two types of boundary conditions which can be input. The first is a Dirichlet boundary condition where the dependent variable T is constant at the boundary b, for example

$$T(b) = \alpha, \tag{3.38}$$

where α is a constant. In the context of this work a Dirichlet boundary condition is used to set a constant temperature on a surface. The second type of boundary condition is the Neumann boundary condition where the derivative of the dependent variable at a boundary is constant, given by

$$\dot{T}(b) = \beta, \tag{3.39}$$

where β is a constant. For heat flow, if $\beta = 0$, this is a perfectly insulating surface as the heat flux across the surface is zero. Most surfaces have Neumann boundary conditions, where the heat flux across the interface is set to zero, which is often used to approximate surfaces which are in contact with air. Whilst it is possible to make the heat flux through the surface non-zero

to approximate a convective air flow, this effect is deemed minimal and is often ignored. The Neumann boundary conditions are also used to define symmetry planes, as a perfectly insulating interface is mathematically equivalent to having the mirror image of the structure on the other side of the interface. The Dirichlet boundary condition is used with the temperature kept at ambient to define the heat sink. The finite element simulations in this work typically have a transistor structure at the top of a wafer epitaxy, which is placed on a larger metal block which represents the sample holder. The sample holder is allowed to heat up, but the Neumann boundary condition is placed on its reverse.

CHAPTER 4

OPTIMISATION OF GaN-ON-DIAMOND MATERIALS AND DEVICES

This chapter reports on research performed with the goal of understanding and enhancing the thermal properties of GaN-on-diamond wafers used for high power density applications. This chapter specifically considers wafers where polycrystalline diamond has been grown onto GaN, with an amorphous silicon nitride layer at the interface. This variation of GaN-on-diamond material has been shown to give the lowest device thermal resistances, and is the only preparation technique which allows the fabrication of 4-inch wafers. In these GaN-on-diamond systems, the TBR_{eff} between the GaN buffer and the diamond substrate can account for half of the overall wafer thermal resistance [237]. As a result, improving the TBR_{eff} is key to unlocking the full potential of GaN-on-diamond devices.

There are three major contributions to the TBR_{eff} of a GaN-on-diamond wafer where polycrystalline diamond is grown onto GaN. First there is the fundamental phonon scattering between dissimilar materials at the interface. This is an inherent property of the material system and cannot be changed, however the thermal resistance caused by such interface phonon scattering is small relative to that of the two other components of the TBR_{eff}, the interface layer, and the diamond nucleation layer. As the interface layer is amorphous, there is no long range thermal transport, whereas in the diamond nucleation layer the high density of grain boundaries limits the phonon mean free path. This chapter will consider the TBR_{eff} as a whole, as well as its

individual components. First, the TBR_{eff} of four-inch GaN-on-diamond wafers is studied using TTR, to map the inhomogeneity of the TBR_{eff} across the wafer. This is followed by a study of the spatial resolution of the TTR technique. The impact of the diamond nucleation layer on the TBR_{eff} is then considered by studying the thermal conductivity of suspended diamond membranes, which are determined by a nanoparticle assisted Raman thermography study. Finally, HEMTs fabricated on two separate GaN-on-diamond wafers are studied using photoluminescence and nanoparticle assisted Raman thermography. The wafers differ in their buffer layer thickness and interface layer thickness, with one sample being thinner than the other. Both the thermal and the electrical characteristics of the wafers are found. The impact of buffer thickness on wafer thermal resistance is then explored further through the use of finite element simulations.

4.1 GaN-on-diamond wafer mapping

4.1.1 Method

The TBR_{eff} of GaN-on-Diamond wafers and dies supplied by Element 6 were determined using TTR. TTR provides a non-contact, non-destructive measurement of the TBR_{eff} of GaN-on-diamond material, and has previously been used to show that the TBR_{eff} is proportional to the interface layer thickness, and that diamond grown through PE MW CVD gave an improved TBR_{eff} when compared to HF CVD grown diamond [190]. An automated wafer mapping routine which allowed the efficient measurement of the TBR_{eff} over 4 inch wafers was developed for this project. This process uses an XYZ mapping stage with a 0.1 μm step size and a maximum travel of 60 mm. The mapping routine can scan over this entire square area, at any desired grid size.

The wafer fabrication process developed by Francis *et al.* is described in Figure 4.1 [32]. It starts with a GaN-on-Si wafer which then has a handle wafer attached to the GaN surface. The original silicon wafer is removed along with the strain relief layers, and the interface layer (typically a dielectric such as SiN_x) is deposited on the now exposed GaN surface. This interface layer is seeded with diamond particles and the diamond is grown to approximately 100 μm thick. The handle wafer is then removed to leave the final GaN-on-Diamond wafer.

Due to wafer bow, the samples are not perfectly flat and as a result the focus of the TTR

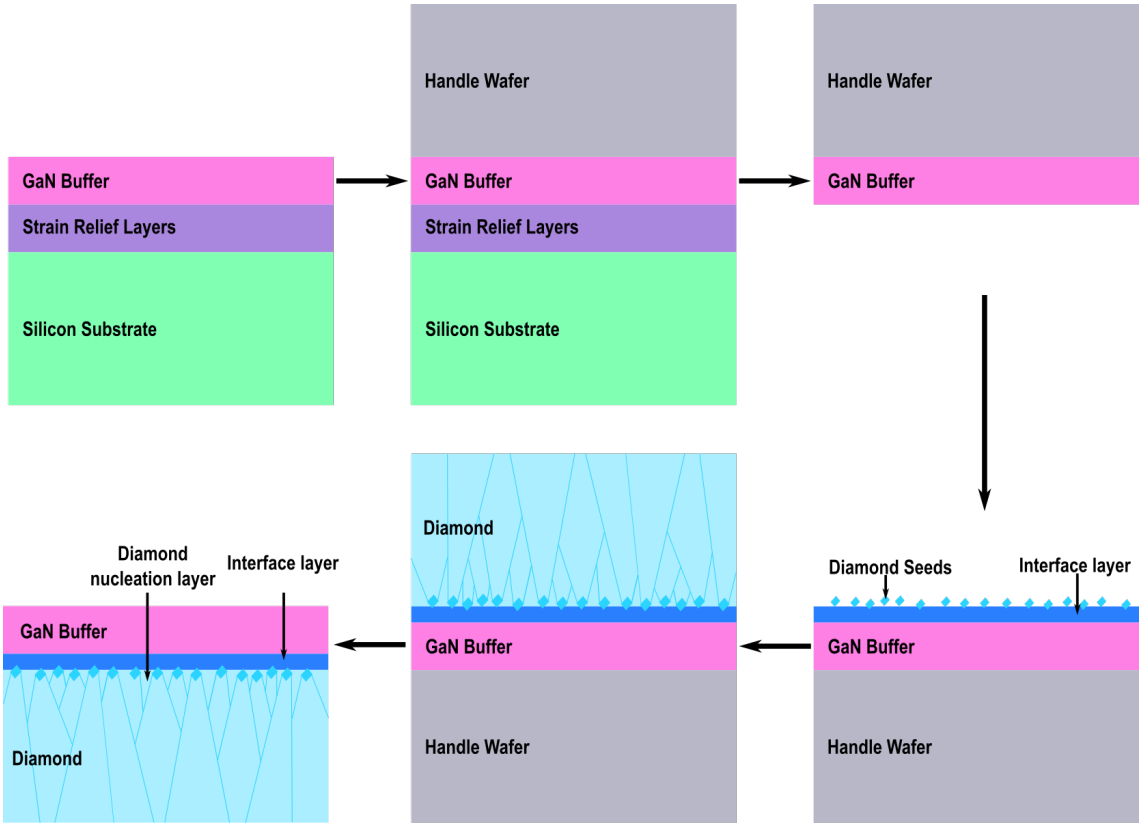


FIGURE 4.1. Process flow developed by Francis *et al.* for the growth of polycrystalline diamond on GaN [32]. Using this process homogeneous four inch wafers have been fabricated.

measurement must be adjusted for each measurement point. This is performed by imaging the probe laser spot intensity across a range of sample depths and counting the number of pixels which are saturated. Using a large step size, the number of saturated pixels will increase as the focus is approached, and the point of maximum saturated pixels can be used to approximate a coarse focus. Once this is found, a more refined search can find the true focus. By using a smaller step size, a local minima in the number of saturated pixels will be found as the laser spot converges.

Once the true focus is found, the mapping routine then takes the reflectance measurement, averaging over the desired number of laser shots. The routine then removes the baseline and background signal, and normalises to the peak reflectance so that the data format is compatible with the fitting software. The mapping routine then moves onto the next point, completing the

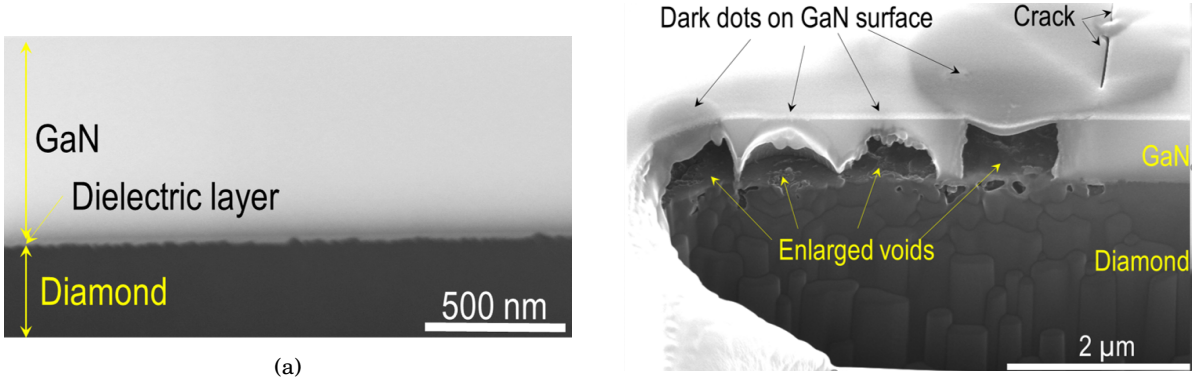
grid in a serpentine manner. Once the mapping was completed the temperature decay could be fit using the process discussed in Section 3.3.

In total, 14 samples were studied for this work, of which 6 were full 4 inch wafers and the remaining 8 were dies cut from wafers. A comparison of the homogeneity across the wafers will be made. The interface layers vary between 15 nm and 35 nm thick and the GaN buffer thicknesses vary from 358 nm to 960 nm. A comparison is also made between the use of large (100 nm) and small (30 nm) seeds as discussed in Reference [238].

4.1.1.1 Spatial resolution of transient thermoreflectance

Whilst mapping full wafers is important for understanding the consistency of industrial growth processes, mapping of smaller areas can aid the understanding of micron scale variations at the interface. The spatial resolution of the TTR measurement will determine the smallest feature size which can be distinguished. For instance, if the spatial resolution is similar in size to the defects which may occur at the interface, then measurements made near such defects may be biased towards larger TBR_{eff} values. Conversely, if the spatial resolution is larger than any interface defects present, the measured TBR_{eff} will be an average of the defective areas and the non-defective areas. The finest map possible is defined by the step size of the stage, but the resolution of the measurement is determined by the thermal transport in the wafer. The experiment uses a pump laser with a diameter of 70 μm and a probe laser with a diameter of 2 μm. A sample with voids at the interface was studied, with a SEM cross section of example voids shown in Figure 4.2. During the measurement process, the laser was scanned over a void of size ≈ 2 μm with a step size of 5 μm and the TBR_{eff} at each point calculated .

A two dimensional finite element model of the experiment was created. The model is axially symmetric about the centre of the Gaussian heating pulse which was used to replicate the pump laser in the experiment. Different void heights were considered, each located at the interface in the centre of the laser heat pulse. The temperature was then measured adjacent to the void; measuring directly on the void is not possible as reflections from the void interfere with the reflections from the surface, resulting in a spurious signal [239]. The GaN was 1 μm thick and the void had a radius of 1 μm. The sample TBR_{eff} was 39 m^2K/GW and the diamond's assumed



(a) (b)

FIGURE 4.2. (a) SEM cross section taken from a sample with no voids. The interface dielectric layer shows some roughness. (b) Examples of interface voids. The voids can vary in size and be visible from the GaN surface. Samples were prepared using FIB and imaged by a collaborator Dr Liu. The images are adapated from Reference [238].

thermal conductivity was 1500 W/m.K.

4.1.2 Results

An example of the collected TTR data and the corresponding simulations are shown in Figure 4.3. The measurement and fitting procedure are described in more detail in Section 3.3. The immediate increase in the temperature is caused by the pump laser. When the pump laser is switched off the temperature starts to decrease as heat flows from the surface, through the sample, to the heat sink which is attached to the bottom of the sample. The rate at which the temperature decays is determined by the thermal properties of the materials in the wafer. The TBR_{eff} primarily impacts the heat flow between 50 ns and 250 ns after the pump laser is switched off. Figure 4.3 shows simulated temperature decay curves with the TBR_{eff} varied by ±10% and all other parameters kept constant.

A summary of the TBR_{eff} for all samples measured is shown in Figure 4.4, plotted against both interface layer thickness and buffer thickness. There is no strong correlation between the interface layer thickness and the TBR_{eff}, which disagrees with work reported in the literature where it is suggested that a thinner interface layer would give a lower TBR_{eff}. As the interface layer is amorphous and has a low thermal conductivity of ≈ 1 W/m.K, it is considered a thermal

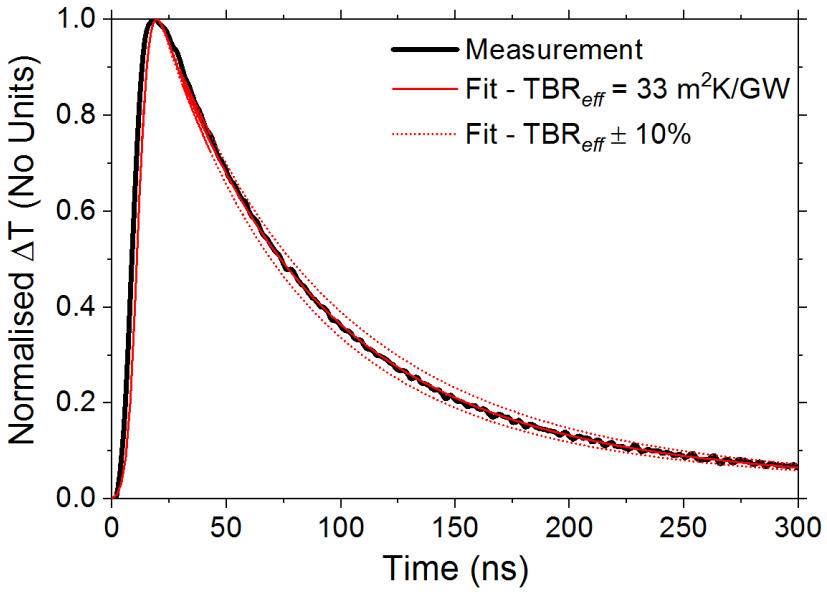
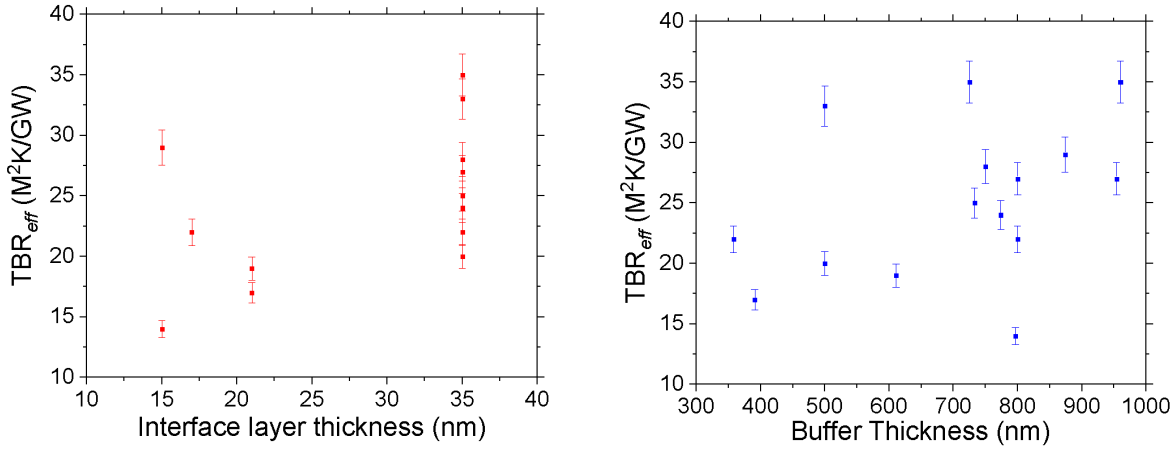


FIGURE 4.3. An example TTR measurement taken from a GaN-on-diamond wafer. This particular location was found to have a TBR_{eff} of 33 m^2K/GW. Also shown is simulated curves with the TBR_{eff} varied by 10%, showing how this impacts the temperature decay.

resistor and thus reducing its thickness should lower the thermal resistance at the interface. As this trend is not distinguishable in the measurements, the data implies that other factors in the fabrication process, such as the seeding or the diamond growth, can also impact the TBR_{eff} and hence must be optimised for thermally efficient GaN-on-diamond devices. The individual contributions to the TBR_{eff} cannot be distinguished by the TTR measurements, and as growth conditions are not known, it can only be speculated as to why there is no correlation. An increase in the amount of power supplied to a plasma during MW PE CVD growth can increase the number of hydrogen radicals which then etch the interface layer, and the resulting rough surfaces can lead to an increased TBR_{eff}. Alternatively, using lower power costs less, but promotes renucleation on the diamond grains which inhibits phonon transport and thermal conduction, again causing an increase in the TBR_{eff}. The diamond growth rate is often inversely proportional to the quality of the diamond, suggesting that an industrial process would need to strike a balance between device performance and the economy of production. Whilst changing growth conditions will change the thermal conductivity of the diamond, the TTR measurement is not sensitive enough to pick up these variations. The seeding method can also impact the thermal properties of the interface, and



(a) (b)

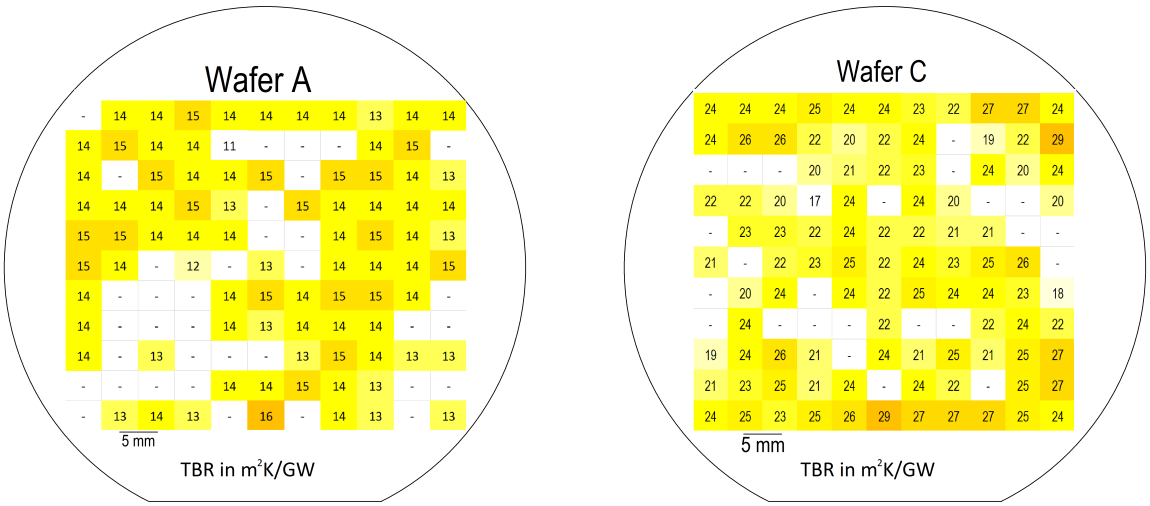
FIGURE 4.4. A summary of the TBR$_{eff}$ measured for each sample of GaN-on-Diamond material. The results are plotted against interface layer thickness (a) and buffer thickness (b). The errors are estimated at 5% of the TBR$_{eff}$ value calculated due to the sensitivity of the fitting process.

TABLE 4.1. A summary of the results of the wafer mapping performed on GaN-on-Diamond samples. The TBR$_{eff}$ values shown are the mean of the measured values, and the errors are the standard deviation of the the value across the wafer.

Wafer	Buffer thickness (nm)	Interface layer thickness (nm)	TBR$_{eff}$ (m^{2}K/GW)
A	774	35	26 ± 2.3
B	874	15	23 ± 2.3
C	797	15	14 ± 0.8
D	725	35	35 ± 2.9

this will be discussed further.

Unlike interface layer thickness, the lack of correlation between buffer thickness and TBR$_{eff}$ is to be expected. The GaN-on-Si growth process is more comprehensively understood than the diamond growth process. This makes the GaN-on-Si growth process more repeatable and means the surfaces are of a high quality. Therefore the GaN side of the interface will be consistent in all the samples, irrespective of the GaN thickness. The measurements align with this expectation

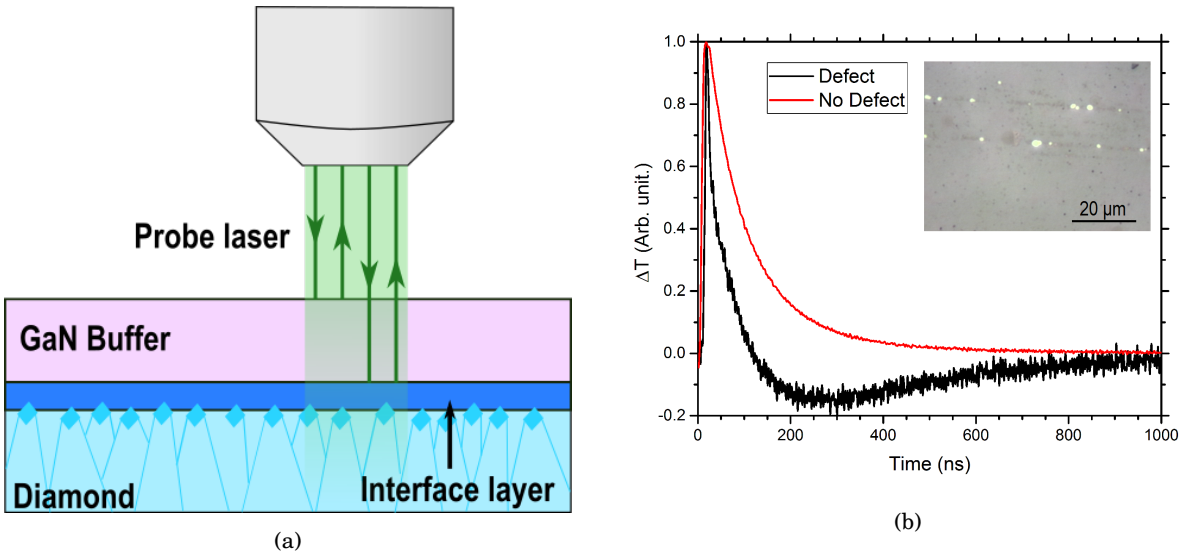


(a) (b)

FIGURE 4.5. Two examples of wafer maps with (a) corresponding to wafer A and (b) corresponding to wafer C in Table 4.1. The points at which no value is recorded are where destructive interference caused a loss of signal.

and imply that the GaN buffer thickness can be varied to find the optimal structure for thermal performance without negatively impacting the TBR_{eff}.

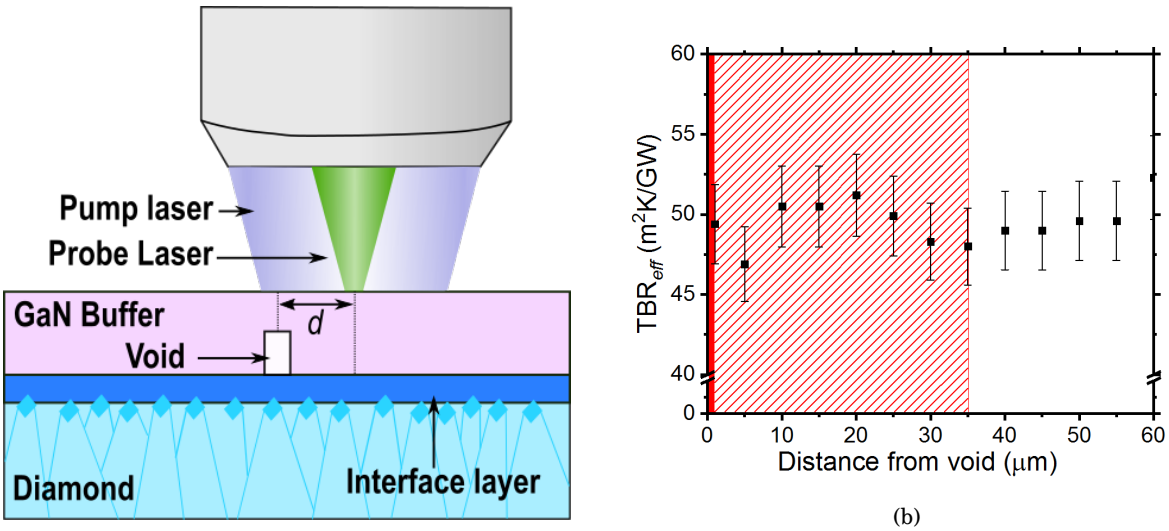
TBR_{eff} maps were made for four wafers, with two examples shown in Figure 4.5, and a summary shown in Table 4.1. The error on each measurement point is approximated at 5% due to the sensitivity of the fitting routine, and the average standard deviation across the wafers was 2.1 m^2K/GW, which is approximately 10%. There does not appear to be a trend in this inhomogeneity, suggesting the variation is caused by random fluctuations. Possible causes for this variation could be defects present on the interface layer which form due to contaminants or an imperfect growth surface, or an inhomogeneous seeding density which can lead to pinhole formation in areas where seeds are sparse. As can be seen in the wafer maps in Figure 4.5, at certain points the TBR_{eff} could not be calculated. This was due to interference effects, where reflections off the GaN surface and the interface layer are out of phase, which causes destructive interference and results in a spurious signal, as shown in Figure 4.6. Subtle changes in GaN thickness and interface layer thickness could result in this condition being met. This issue was solved at a later date by the use of an above bandgap probe laser.



(a) (b)

FIGURE 4.6. (a) Schematic diagram showing the TTR measurement of a GaN-on-diamond wafer when a below bandgap probe laser is used. The pump laser is not shown for clarity. When reflections from the interface layer are out of phase with reflections from the GaN surface, the signals can destructively interfere. (b) Difference in TTR curves when measured on defect and on a defect free location. The inset is an optical micrograph of voids as seen from the sample surface.

Wafer B in Table 4.1 was seeded using seeds of mean size 30 nm and was compared to a similar sample, measured by a colleague Dr Sun, whose seeds had a mean size of 100 nm [238]. It was found that the TBR_{eff} of the sample with larger seeds was approximately 40 m^2K/GW, almost twice as high as that for Wafer B. The use of larger seeds was expected to improve the TBR_{eff} as larger seeds should produce a diamond nucleation layer with a higher thermal conductivity, due to a greater ratio of diamond bonded carbon to graphitic carbon. However it was found by Liu *et al.* that the larger seeds led to a highly defective interface with voids and cracks forming since, as was found by Williams *et al.*, larger seeds result in lower seeding densities [170, 238]. As these voids, shown in Figure 4.2, constitute a small proportion of the interface it is unlikely that they are the cause of the high TBR_{eff} measured. Instead it is likely that they are a symptom of a poor quality, weakly bonded, highly stressed interface which is the cause of the high thermal resistance.



(a) (b)

FIGURE 4.7. (a) Schematic of the experiment used to determine the spatial resolution of the TTR setup. The TBR$_{eff}$ is measured for varying d. (b) Measured TBR$_{eff}$ as a function of central measurement location distance from the void (d in (a)), which has a diameter 2 μm. The red lined box indicates the locations where the void is in the pump laser beam diameter.

4.1.2.1 Spatial resolution of transient thermoreflectance

Part (a) of Figure 4.7 is a schematic diagram of the experiment used to test the lateral spatial resolution of the TTR experiment, with the results shown in Figure 4.7 (b). The void, which is chosen to be similar to those shown in Figure 4.2, is approximately 2 μm in diameter, but its depth is unknown as focussed ion beam cross sectioning would destroy the sample. The measurement starts with the void outside of the diameter of the probe beam, where it would not be directly heated but it may impede lateral heat spreading. Because of the Gaussian heat profile of the laser, the intensity at the GaN surface will be lower at the edges of the beam diameter, and there is no noticeable change in the measured TBR$_{eff}$ as the void enters this region. Whilst the impact of the void on the TBR$_{eff}$ may be expected to increase as it enters the central, most intense region of the pump beam, there is no change in the TBR$_{eff}$ measured. This suggests that the measurement averages over an area similar to the pump beam diameter. A pump laser spot size of diameter 70 μm as defined by the standard e^{-2} definition will have 86.5% of the intensity focused in ≈ 220 μm^2 area. If the void has a 2 μm diameter it will only account for 3% of the

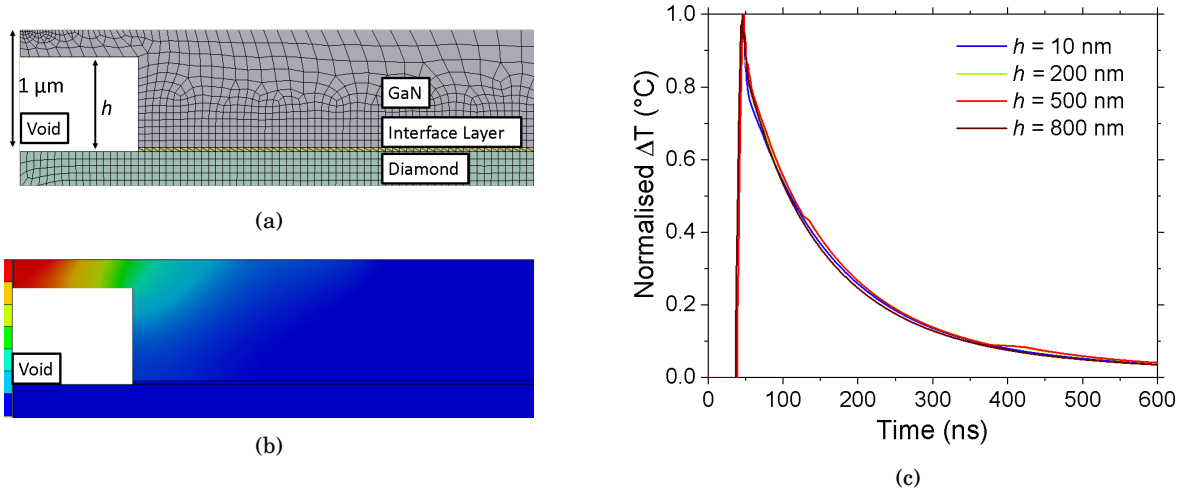


FIGURE 4.8. (a) Two dimensional simulation of the GaN-on-diamond system with a void of height h = 0.8 μm and radius 1 μm at the interface. The mesh used to calculate the temperature is shown. (b) Calculated heat profile in the sample at the time of maximum temperature. c) Temperature decay curve for several void heights h, which is labelled in (a). The radius is constant at 1 μm.

area heated. Hence it should not be surprising that the impact of the relatively small void is not recognisable within the precision of the measurement. This suggests that the presence of the voids is not responsible for the high TBR_{eff} measured in the large seeded sample as these are not resolved in the measurement. Instead these voids are a symptom of a poor quality interface which is likely to have a high TBR_{eff}. It also means that any high TBR_{eff} results seen from wafer mapping must be due to longer range defects.

The finite element model, shown in Figure 4.8 (a), agrees with this conclusion. In Figure 4.8 (b) the heat profile is shown at the point of peak temperature. There is a large temperature gradient above the void which is likely due to the fact that heat in this region can only flow in the plane of the wafer. However, as is shown in Figure 4.8 (c), there is no significant change to the TTR curves for all defect heights. The curves are independent of the defect height at all times which again suggests that the measurement is an average over a much larger area than just the probe laser spot. Any temperature gradient caused by the defect must return to the standard case of no defect on time scales faster than could be measured. If it is desirable to measure the TBR_{eff} impact of a specific defect of this size it would be necessary to use a faster heating pulse

and measurement equipment, and to use a reduced pump laser spot size such that the void takes up a larger proportion of the heated area.

4.2 Diamond film thermal conductivity

4.2.1 Method

The diamond nucleation layer contains many grain boundaries and inclusions which reduce it's thermal conductivity, meaning it contributes to the TBR_{eff} in GaN-on-diamond wafers. In this section, the thermal conductivity of suspended diamond films is studied to aid understanding of how growth conditions can be optimised to give a higher quality diamond nucleation layer. The suspended diamond films were supplied as part of a Defense Advanced Research Agency (DARPA) round robin program, and a schematic of the diagrams is shown in Figure 4.9. Assuming the radiative heat transfer to the surroundings is negligible, the heat will flow through the diamond film, to the bulk silicon. The diamond was grown and processed by the Naval Research Laboratory. The test structures were fabricated before the silicon was selectively etched to leave the diamond films. Electrical power is supplied through the gold heater which runs through the centre of the film. There are six contact pads connected to this heater, two at either end and two towards the centre. The current can be supplied through two of the end contacts, with the voltage measured on the other two; this allows accurate determination of the power dissipated across the heater as it avoids the resistance contribution from components which are in series with the power supply. The fifth and sixth contact are included to allow a measurement of the power dissipated through the central portion of the heater.

Anatase nanoparticles were dropcast onto the sample to act as nano-thermometers as described in Section 3.1.4. The films are designed such that the heat flow at the centre of the heater, between the fifth and sixth contact tracks, is perpendicular to the heater track as seen in Figure 4.9 (d). Nanoparticles in this area are measured for the thermal conductivity calculations as only knowledge of the perpendicular distance from the heater is required to map the heat flow. Four different varieties of film were measured, with dimensions of 250×500 μm, 450×1000 μm, 700×2100 μm, and 330×1900 μm. The gold heater is 5 μm thick, and the space between the

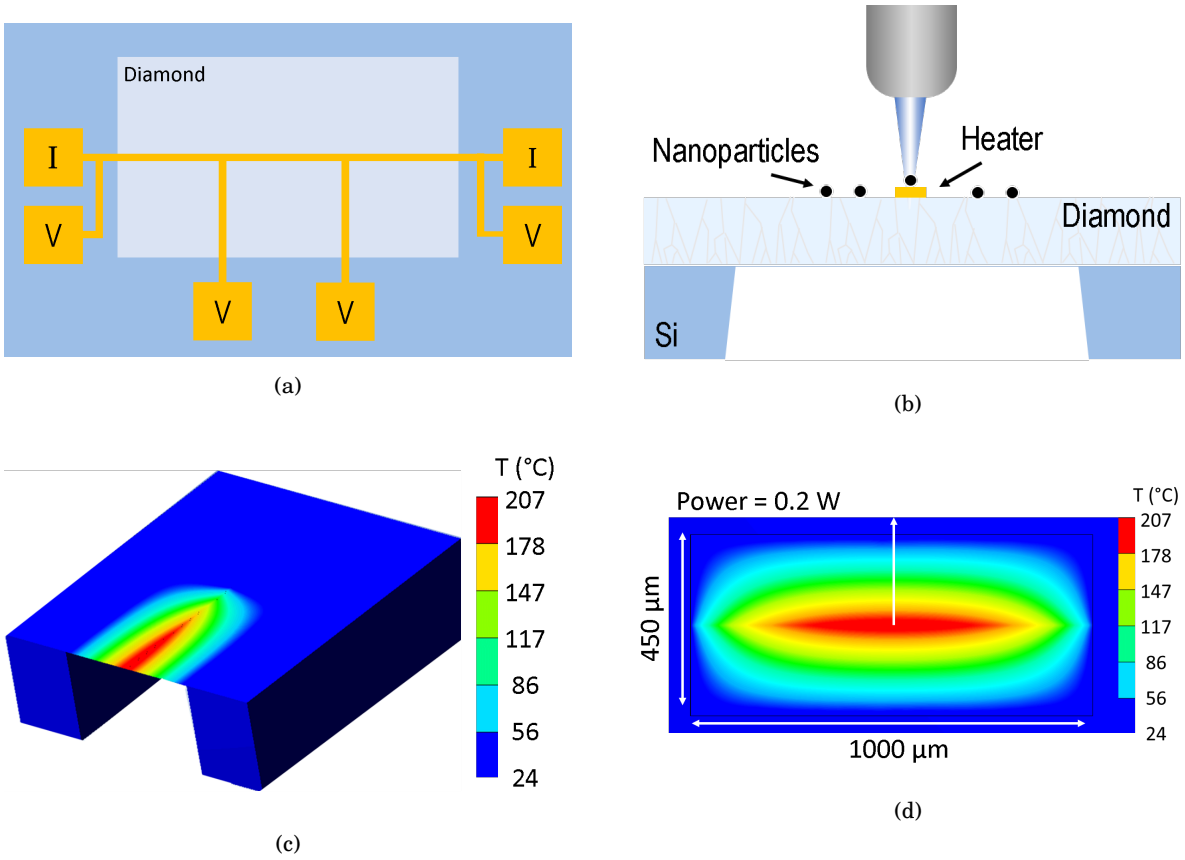


FIGURE 4.9. (a) Schematic diagram of the films measured in this work. Contacts labelled I are used to supply the power to the heater and contacts labelled V can be used to measure the voltage. The two central contacts also define the area where the heat flow is linear and perpendicular to the heater. (b) Cross-section of a film showing the Raman measurement of nanoparticles. (c-d) Simulated temperature profile in an example film. The central white arrow in (d) shows the linear heat flow direction. These models have the thermal conductivity of the diamond adjusted such that the temperature profile matches the nanoparticle measurement.

central contact pads varies but is approximately one fifth of the total width.

For each film, the Raman shift of the nanoparticles is measured at a range of electrical powers that result in temperature rises of up to 400°C. Nanoparticles at the centre of the heater are used for determining the maximum temperature increase and hence the diamond thermal conductivity. Nanoparticles are also measured both along the heater and perpendicular to the heater to ensure the power is being dissipated as expected. Error bars are judged by taking repeat measurements of the Raman shifts and propagating this through to the temperature calculation. The results are then compared to finite element simulations of the films in which the thermal conductivity is varied to match the results. The error in the thermal conductivity is established by lines of worst fit.

In total, 21 films from 15 samples from 4 wafers were analysed as part of the DARPA project. The samples were 20 by 20 mm and the wafers were 3" in diameter. A summary of the wafers growth conditions are shown in Table 4.2. The number of films studied allows for a check of homogeneity across samples and wafers.

4.2.2 Results

As each of the DARPA supplied samples contained multiple films, it was possible to explore the spatial variation in the thermal conductivity for each sample. For diamond films on the same sample, and hence located within 20 mm of each other, the maximum difference in thermal conductivity was 13% and the average difference was 6%. The mean thermal conductivity of all measured films for each wafer can be seen in Table 4.2, where the quoted error value is the standard error from all measurements on that wafer. This variation is approximately 3% of the measured value and could partially explain the variation in the TBR_{eff} wafer maps discussed earlier. However it is worth noting that the sample supplier is different so growth conditions may vary. Sample δ has the largest thermal conductivity. This is expected as this sample was 3 μm thick whereas the others were just 1 μm thick. As discussed in Section 2.4.2, the diamond columnar growth structure means that as films grow thicker, grains overgrow each other, resulting in fewer grain boundaries and higher thermal conductivities. It was found by Anaya *et al.* in Reference [174] that an increase from 1 μm to 3 μm thick should see an increase of at least 2×

TABLE 4.2. A summary of the growth conditions and thermal conductivity data measured on the diamond films. The seed size for wafers β and δ are unknown. The thermal conductivity values are the mean of all films measured on that wafer and the errors are the standard deviation of those measurements.

Wafer	α	β	γ	δ
Thickness (μm)	1.05	1.01	1.06	3.02
Growth Power (W)	2200	1400	2300	800
Seed size (nm)	4	-	40	-
Thermal conductivity (W/m.K)	75 ± 2	75 ± 3	106 ± 2	112 ± 4

in the thermal conductivity, but this was not the case in the samples studied here. Sample δ was grown with 800 W microwave powers whilst the next lowest was 1400 W. Lower microwave powers are ideal for industrial scaling as they are less energy intensive, but they have been shown to produce lower quality diamond by facilitating renucleation. This will impact thermal performance by the introduction of more grain boundaries and graphitic bonded carbon [169].

The impact of seed size can be seen in the comparison between wafers α and γ. In this instance the larger seeds are a similar size to the smaller seeds discussed in Section 4.1.2 and in Reference [238]. As expected, the larger seeds give a larger thermal conductivity as there are fewer grain boundaries, suggesting that larger seeds should improve the wafer thermal performance. However this contradicts the earlier work which shows that if the seeds are too large, this can lead to a lower TBR_{eff} value as well as to the formation of cracks and defects at the interface. This suggests there is an optimal seed size to provide the best possible TBR_{eff}, a balance between the size of the grains and the seeding density. Both of the seed sizes studied in this experiment give an equivalent standard deviation which suggests that seeds do not impact the homogeneity of the films.

4.3 GaN-on-diamond devices

Two samples from GaN-on-diamond wafers supplied by Element 6 and processed at the University of Sheffield are studied in this section. The wafers were fabricated using the process discussed in Section 4.1.1 and in Reference [32]. The samples differ in their GaN buffer thickness and

interface layer thickness. The wider sample (Sample W) has a buffer thickness of 700 nm and an interface layer thickness of 36 nm, whereas the narrower sample (Sample N) has a buffer thickness of 354 nm and an interface layer thickness of 17 nm, chosen to test the importance of the diamond substrate being as close as possible to the device channel. Finite element simulation studies have previously shown than the optimal buffer thickness is a function of the thermal boundary resistance, although this has not been tested experimentally [240, 241].

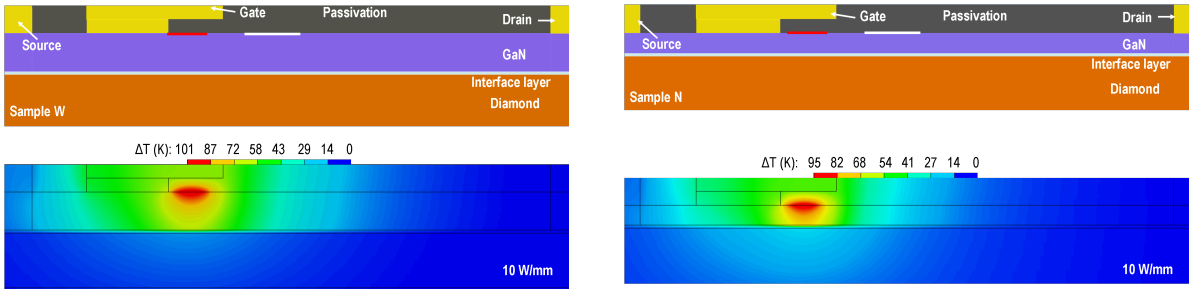
4.3.1 Method

The devices studied are 2×50 μm gated HEMTs with an L_{GD} of 7 μm, an L_{GS} of 1 μm, and an L_G of 1.5 μm. The gate has a 1 μm field plate attached which extends to the drain side. Despite there being two fingers to each device, for the thermal measurements only one finger was operated due to space limitations in the optical set up.

As micro-Raman thermography is most commonly used for measuring device temperatures, this was the first technique used to measure the samples. However, the thin buffers led to a weak Raman signal, and the diamond provided a large luminescence background, making the signal to noise ratio too poor to provide reliable measurements. Because of this, a combination of nanoparticle assisted Raman thermography and photoluminescence was used in conjunction with finite element simulations.

Before the thermal measurements were taken, the electrical characteristics of the devices were found through IV measurements. The devices were tested by a colleague, Mr Manikant, at drain voltages between 0 V and 40 V, and gate voltages between 1 V and -4 V, which is sufficient to pinch off the devices. The tests were performed under DC operation and both stressed and unstressed pulsed operation using a pulse width of 200 ns and a frequency of 1 kHz. There where two separate stress conditions, the first had quiescent biases of $V_{DS} = 0$ V and $V_{GS} = -6$ V and the second had quiescent biases of $V_{DS} = 40$ V and $V_{GS} = -6$ V. The measurements were analysed to find the ON-resistance and trapping characteristics of the devices, as well as to provide an insight into their thermal performance by calculating the thermal droop in the current under high voltage operation.

The photoluminescence measurements were performed using a 40× focussing objective and



(a) (b)

FIGURE 4.10. Cross-section at the centre of each device, as modelled in the finite element simulations. (a) shows the thicker Sample W, which has the 700 nm thick buffer and 36 nm thick interface layer and (b) shows the thinner Sample N which has a 354 nm thick buffer and a 17 nm thick interface layer. The red line underneath the field plate shows the heat deposition area, and the white line in the gate-drain access region shows the measurement location, over which the temperature is averaged to provide a comparison to the experimental photoluminescence results. Also shown is an example of the heat flow in each of the structures. The thinner sample has a lower thermal resistance and less in-plane heat spreading.

an XYZ translation stage with a minimum step size of 1 μm. The laser spot size, and hence the lateral resolution of the measurement was approximately 1 μm. The devices were tested at 5 V increments in the drain voltage, up to a maximum V_{DS} of 30 V, which corresponds to a power density of approximately 12 W/mm. Due to the presence of the gate field plate, the measurement was taken 2 μm from the gate edge. As discussed in Section 3.2, the above bandgap laser used to probe the photoluminescence excites carriers and increases the temperature. Batten *et al.* calibrated for this effect by measuring at multiple laser powers and extrapolating to the case of no laser power [227]. They found that at 4 μW of laser power, the laser induced temperature change was less than 5 K. On this basis measurements at 4 μW and 40 μW, with a linear extrapolation to no laser power were performed. For each measurement condition, 3 repeats are made to estimate the random errors, and integration times of approximately 5 minutes are required. As with micro-Raman thermography, a reference measurement is performed approximately 300 μm away from the device to give the thermal resistance between the wafer and the sample holder. Throughout the measurement process, the environment temperature is kept constant at 22°C.

The device dimensions were input into a finite element model, shown in Figure 4.10 along with representative examples of the heat flow in the system. The diamond substrate is 95 μm thick,

and is split into 5 different layers which allows the model to take into account the improvement in diamond quality that occurs as growth continues. The thermal conductivities were taken from Reference [173] and are temperature dependent and anisotropic, representing the diamonds columnar growth structure. The layers expand away from the growth surface; the first layer is 1 μm thick, the second 4 μm, the third 10 μm, the fourth 20 μm and the fifth and final diamond layer is 40 μm thick. The temperature on the backside of the diamond was set to replicate the thermal resistance between sample and the sample holder. The diamond was connected on the top side to the GaN through a 100 nm thick interface layer whose thermal conductivity was adjusted to set the TBR_{eff} for the system. The GaN was then atop this layer with buffer thickness adjusted between the two samples and the thermal conductivity set to 160 W/m.K and a $T^{-1.4}$ temperature dependence as laid out in Section 2.2. The space between the gate, source, and drain was filled by a passivation layer of thermal conductivity 1 W/m.K as is typical of the amorphous materials used such as silicon nitride.

The heat was deposited both parallel and adjacent to the gate edge on the drain side in a 0.75 μm wide area on the GaN surface, underneath the field plate. The temperature was then averaged over a 1 μm area at the GaN surface, centred 1 μm from the field plate edge on the drain side. The average temperature in this measurement position was matched to the photoluminescence measurement by varying the TBR_{eff} of the model. Once this was completed for each power dissipation, a mean TBR_{eff} was input into the model and the model was then used to predict the wafer thermal resistance.

The nanoparticle assisted Raman thermography used anatase nanoparticles drop cast onto the surface as described in Section 3.1.4. One nanoparticle which had landed on the gate for each sample had their Raman frequencies measured with the drain voltage varied up to 30 V. The random error was found by repeating the measurements 5 times, finding the standard error on the mean and propagating this error through to the final temperature calculation. As the exact gate structure is not known it is not possible to perform a direct comparison to the finite element simulations, but the results can still be used to add context.

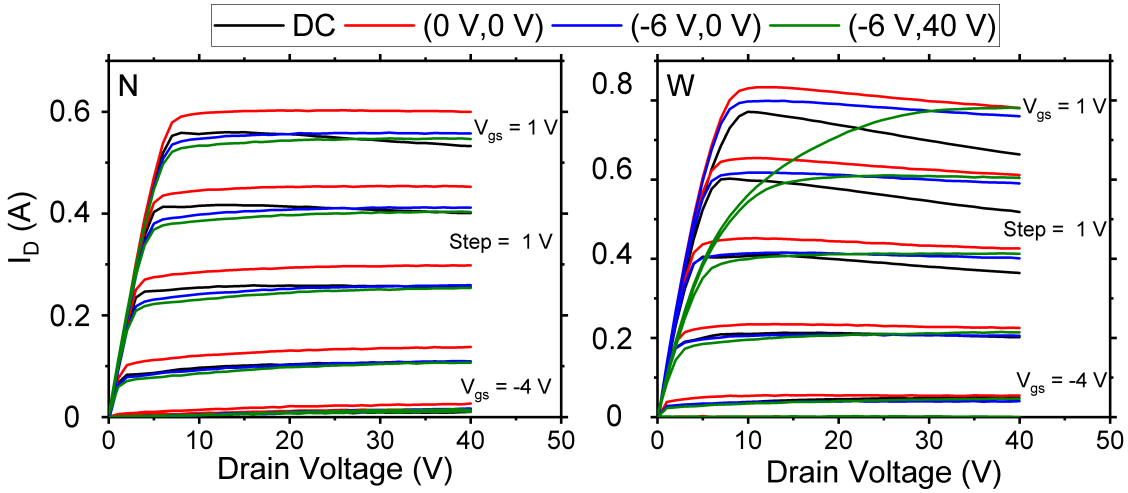


FIGURE 4.11. IV characteristics from the thicker sample with 700 nm thick buffer and 36 nm thick interface layer (W) and the thinner sample with the 354 nm thick buffer and 17 nm thick interface layer (N). Measurements were performed in both DC and pulsed IV mode with a pulse width of 200 ns and duty cycle of 0.02%. The pulsed IV measurements were performed unstressed ($V_G = 0$ V, $V_D = 0$ V), under gate lag stress ($V_G = -6$ V, $V_D = 0$ V), and under both gate and drain lag stress ($V_G = -6$ V, $V_D = 40$ V).

4.3.2 Results

IV characteristics of devices on both GaN-on-diamond wafers are shown in Figure **??**. A discussion of the IV characteristics of a depletion mode device is given in Section 2.2.4. The thermal effects most commonly manifest in these measurements as an increase in ON resistance. They can be seen by comparing the DC operation, where the temperature in the device reaches a steady state, with the unstressed pulsed operation, where the heat has less time to build up. This heat build up is quantified by calculating the difference between the maximum and minimum current in the device whilst it is in the saturation regime, for both the DC and pulsed operation. For Sample W and Sample N the difference was 8% and 4% respectively suggesting that Sample W has a larger thermal resistance.

The threshold voltage of the devices is the minimum applied gate voltage which draws a source to drain current and is found by plotting a straight line through the linear region of a I_{DS} vs V_{GS} curve and finding its x-axis intercept. For Sample N the applied gate lag stress caused a

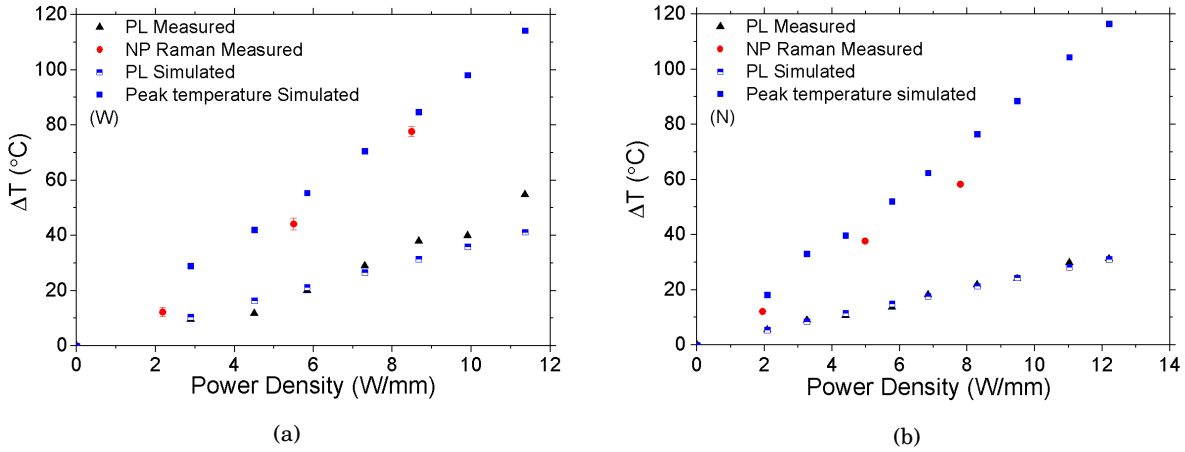


FIGURE 4.12. A summary of the photoluminescence (PL), nanoparticle assisted Raman thermography (NP Raman), and simulated results in the PL measurement location and at the peak. (a) shows the results for the wider Sample W (700 nm buffer and 36 nm interface layer) and (b) shows the results for the narrower Sample N (354 nm buffer and 17 nm interface layer). The TBR_{eff} of the model is adjusted to get the best possible match between the simulated and measured photoluminescence results. The measured nanoparticles are located on the gate, so their temperature should be similar to the peak temperature.

small positive shift in the threshold voltage of 180 mV, which suggests that negative charges are being trapped below the gate. The ohmic ON-resistance is found by calculating the gradient of the IV curve in the linear regime and is an important parameter to consider as it plays a key role in the overall efficiency of a device. This is unaffected by stress in Sample N, but there is a significant impact when drain lag stress is applied to Sample W. The ON-resistance increased by 44% which is attributed to trapping in the device. It is possible that 'virtual gate' trapping occurs in the sample surface; a phenomenon where the applied stress causes carriers to occupy surface trap states which act as a second gate and depletes carrier concentrations in the 2DEG [242]. It is also possible that the trapping occurs in the device buffer, and as the trapping is not seen in Sample N, the region where the trapping occurs may have been removed. A comparison of the two samples shows there is no significant negative impact from the thinning of the buffer as there is no change in current collapse and no signs of bulk trapping, despite the fact that the diamond nucleation is much closer to the channel.

The results from the thermal measurements along with simulated predictions can be seen in

TABLE 4.3. A summary of the properties found from the photoluminescence measurements and finite element simulations. The narrower Sample N has a substantially lower TBR_{eff}, but its overall thermal resistance is similar to the thicker Sample W.

Sample	TBR_{eff} (m^2K/GW)	Thermal Resistance (K/(W/mm))
W	20 ± 3	10.0 ± 0.5
N	12.6 ± 0.4	9 ± 1

Figure 4.12. The measured gate temperature from nanoparticle assisted Raman thermography is expected to be larger than the photoluminescence measured temperature, but not as high as the peak simulated temperature, which is consistent with the findings. The results show the temperature increase due to the thermal resistance of the wafer with the impact of the thermal resistance between the wafer and the sample holder, found from the reference measurement, removed. The TBR_{eff}, found by fitting the simulation to the experimental data, and thermal resistances, found by a linear fit of the peak temperatures from the simulation, are summarised in Table 4.3. This TBR_{eff} was used to calculate the simulated temperatures for the photoluminescence measurement and the peak channel temperature seen in Figure 4.12.

It can be noted that the thinner Sample N has the lowest thermal resistance, although the error boundaries of the measurements overlap. The TBR_{eff} of Sample N is lower, which agrees with the results displayed in Figure 4.4, that a low TBR_{eff} can still be achieved when a thin buffer is implemented. This lower TBR_{eff} results in a similar thermal resistance, suggesting that if the samples had the same TBR_{eff}, then a thicker buffer would give a lower thermal resistance. This corresponds with the simulations performed in the literature which suggest that a TBR_{eff} of approximately 5 m^2K/GW is necessary for a lower overall thermal resistance in the thinner buffer [241].

The finite element simulations of the devices with a 354 nm buffer and a 700 nm are used to extract the the peak temperature increase for a range of TBR_{eff}, shown in Figure 4.13 (a). At 10 W/mm, similar to the power used in this experiment, it suggests that a TBR_{eff} as low as 5 m^2K/GW would be required to get a lower overall thermal resistance, again similar to results published elsewhere [241]. However, as power dissipation increases this cross over point shifts to a higher TBR_{eff}, suggesting that thinner buffers will be optimal as power density increases.

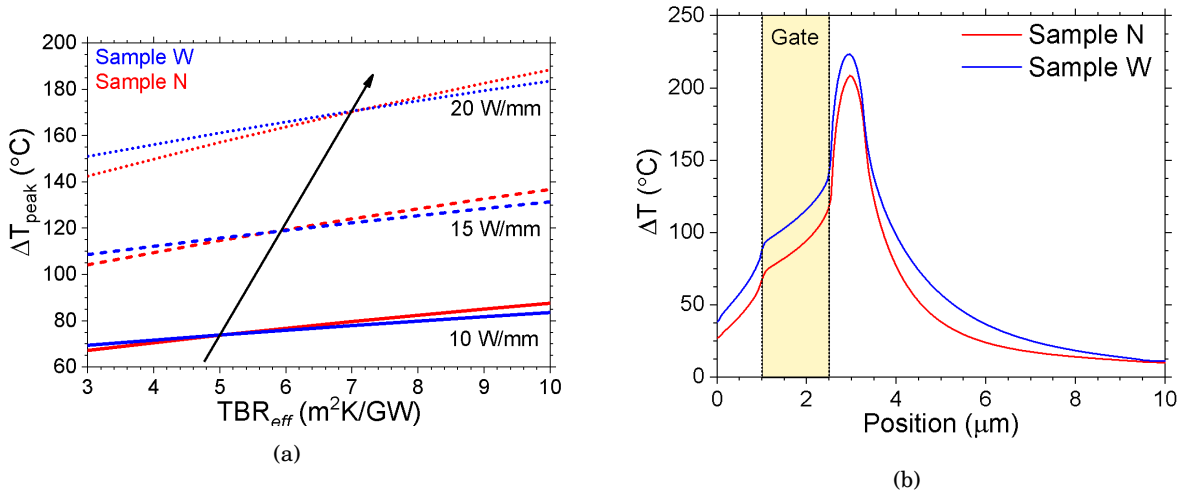


FIGURE 4.13. (a) Peak simulated temperature as the TBR_{eff} is varied. This is performed for the two buffer thickness used in this experiment and at the power dissipations displayed. The TBR_{eff} at which the thinner buffer provides a lower overall thermal resistance increases with temperature. (b) In-plane spreading at the GaN surface in the centre of the device from source to drain at a power dissipation of 5 W/mm. Despite similar thermal resistances, the source-drain temperatures are lower

The finite element simulations can also be used to study the in-plane heat spreading of the system. The results displayed in Figure 4.12 show that the two devices have similar thermal resistances and hence peak temperatures. The temperature measured by photoluminescence is lower in the narrower sample, suggesting that there is less in-plane heat spreading. This is confirmed in Figure 4.13 (b). This graph shows the temperature at the surface of the GaN, in the centre of the device, from the source to the drain. The peak temperatures at the gate edge are similar because of the similar thermal resistances, but there is a more pronounced difference in the gate-drain access region. The electrical characteristics of a device is impacted by the temperature throughout the channel, meaning that a narrower temperature profile will have less of a negative impact than a broader one with the same peak temperature. This is a possible explanation for the difference in thermal droop seen in Figure **??**.

4.4 Summary

The work in this chapter studied the thermal properties of GaN-on-diamond systems for high power density HEMT applications. It focusses on the use of polycrystalline diamond as a heat spreading substrate. A variety of wafers and dies have their TBR_{eff} measured using TTR. An analysis of buffer and interface layer thicknesses show that there is no clear correlation between these parameters and the TBR_{eff} in these samples. Although it was previously shown that TBR_{eff} is proportional to interface layer thickness, this work suggests optimisation of the growth and seeding conditions is of key importance. TTR was also used to compare samples of two different seed sizes, 30 nm and 100 nm. It was found that larger seeds gave a larger TBR_{eff}, as although they may lead to larger grains in the diamond, the lower seeding density led to cracks and voids forming at the interface.

The impact of one of these voids was studied and was linked to the spatial resolution of the TTR technique. The measurements showed that the distance between the measurement location and a 2 μm void had no impact on the measured TBR_{eff}, suggesting that the measurement averages over an area much larger than the defect size. This was confirmed by the use of finite element simulations that showed, irrespective of defect height, the TTR curve remained indistinguishable within the measurement capabilities.

Nanoparticle assisted Raman thermography was then used to measure the thermal conductivity of thin diamond films. These were found to have standard deviations of approximately 3% across wafers. It was found that using 40 nm seeds provided an increased thermal conductivity over 4 nm seeds. When correlated with the earlier TTR study this suggests that there is an optimal seed size which would provide a higher thermal conductivity diamond nucleation layer, as well as a higher quality interface. Again it was found that growth conditions can play a key part in the material quality, with conditions which promote renucleation causing lower thermal conductivities.

Devices fabricated on GaN-on-diamond material were then studied. The variable of note between the two samples was the thickness of the buffer and interface layers. The work presented in this chapter suggests that low TBR_{eff} material can be produced with thinner layers and this

was the case with these devices. However, it was necessary for the narrower sample to have a lower TBR_{eff} than the wider sample for the wafers to have similar thermal resistances. This is because, as was shown with simulation, thinner buffer layers have a negative impact on thermal resistance above a certain TBR_{eff}, which is proportional to the power dissipation. This suggests that as TBR_{eff} values improve and power densities increase, thinner buffers will become beneficial. They were also shown to have the added benefit of reduced in-plane heat spreading which resulted in lower temperatures in the gate-drain access region, which could reduce thermal increases in resistance, improving device efficiency.

CHAPTER 5

THERMAL TRANSPORT IN SUPERLATTICE CASTELLATED FETS

The SuperLattice Castellated Field Effect Transistor (SLCFET) is a novel RF switch designed by Howell *et al.* at Northrop Grumman Mission Systems [243]. The design was developed to improve on current FET and MEMS based RF switch technologies. The most commonly used figure of merit for RF switches is the cutoff frequency f_{CO}, which is the frequency that corresponds to a matched OFF and ON impedance, and above which insertion losses become too large. The cutoff frequency can be derived as

$$f_{CO} = (2\pi \times C_{OFF} \times R_{ON})^{-1} \tag{5.1}$$

where C_{OFF} is the OFF capacitance and R_{ON} is the ON resistance [243]. Hence switch performance can be enhanced by minimising either or both of the C_{OFF} and R_{ON}. With respect to this figure of merit, RF MEMS surpass their solid state transistor counterparts due to the low C_{OFF} achievable [244, 245]. However in terms of reliability, it is solid state components that are superior, and this is what makes SLCFETs so advantageous; they combine MEMS performance with solid state reliability.

To achieve improved performance, it is not possible to simply optimise the dimensions of a standard HEMT since to a first approximation

$$C_{OFF} \propto \frac{1}{d}, \tag{5.2}$$

and

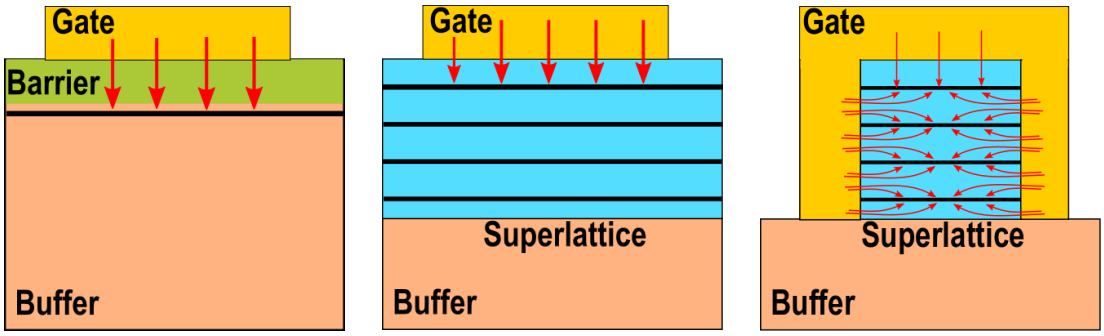
$$R_{ON} \propto d, \tag{5.3}$$

where d is the gate width. This means that any change to the device layout that may reduce R_{ON} will cause an increase in C_{OFF} and vice versa. However, as the OFF capacitance is dominated by fringing fields, there is freedom to exploit how the channel is designed. Multiple channels, and hence 2DEGs, can be stacked on top of each other to make a quasi-three-dimensional electron gas without adversely impacting the C_{OFF}. This was first performed in GaAs by Sheng *et al.* in 1985, with a schematic diagram shown in Figure 5.1 (b), although the devices fabricated could not be pinched off as the 2DEGs higher in the superlattice screen the lower ones from the applied gate field resulting in an unfeasibly high threshold voltage (V_{TH}) [246]. The authors noted however that as more channels are incorporated into the device, the mobility, μ_e, and carrier concentration, n, increase. Hence, as the conductivity, σ, is given by

$$\sigma = n\mu_e e \tag{5.4}$$

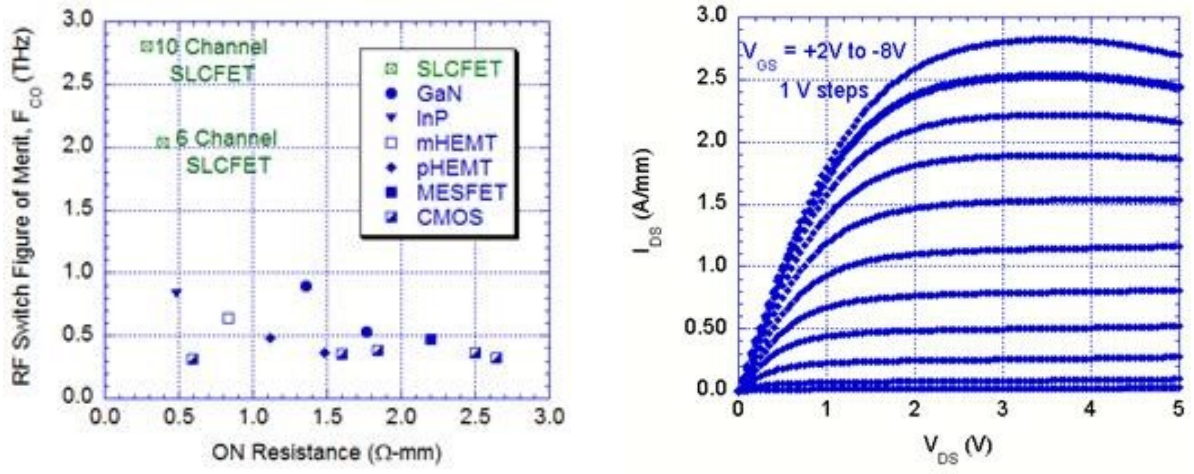
where e is the electron charge, the ON resistance decreases as more channels are added.

The SLCFET looks to exploit this principle [243]. It employs a GaN/AlGaN superlattice with either 6 or 10 2DEGs formed on an AlGaN buffer and a SiC substrate. As is typical in GaN-on-SiC structures, there is an AlN interface layer between the buffer and substrate. To get around the issue of the extremely high V_{TH}, a three-dimensional gate which rises and falls periodically and wraps around the sides of the channel is utilised, as shown in Figure 5.1 (c). This allows the applied electric field from the gate to impinge on the 2DEGs from the side and from above, reducing the V_{TH} to a manageable level. Measurements taken by Northrop Grumman and reported in References [243, 247] show that R_{ON} drops from 1.1 Ω.mm in a single channel device to 0.38 Ω.mm in a 6 channel device and 0.28 Ω.mm in a 10 channel device, a change of 65% and 75% respectively. As C_{OFF} changed by less than 10%, the cutoff frequency of SLCFETs increased from 0.7 THz to 2.0 THz in 6 channel devices and 2.8 THz in 10 channel devices. As seen in Figure 5.2 (a) this value is twice as high as previously reported cutoff frequencies in solid state devices. The castellated gate kept $V_{TH} < -8$ V.



(a) Traditional HEMT (b) Superlattice HEMT (c) SLCFET

FIGURE 5.1. A comparison between how a channel is pinched off in a traditional HEMT (a), a superlattice HEMT (b), and a SLCFET (c). The diagrams show the gate in each device structure, looking from source to drain. The red arrows represent the electric field lines which occur when a bias is applied to the gate, and the black lines represent the 2DEGs. For simplicity the insulator isolating the 2DEGs from the gate is not shown. In the traditional HEMT a single 2DEG forms below the AlGaN barrier and is pinched off by the gate. In the superlattice HEMT multiple 2DEGs form in the superlattice, but the lower 2DEGs cannot be pinched off as the the upper ones screen the electric field from the gate. The SLCFET counters this problem with its 3D gate allowing the lower 2DEGs to be pinched off from the side.



(a) (b)

FIGURE 5.2. (a) A comparison of the cutoff frequency of various FET based RF switches showing the enhancement achieved by the the SLCFET design. Image originally published in Reference [247]. (b) A DC IV curve for a 6 channel HEMT originally published in Reference [243]. The device can be seen to pinch off at $V_{GS} = -8$ V. Reprinted with permission from the IEEE.

A schematic diagram of a SLCFET, along with a SEM image, is shown in Figure 5.3. The devices measured in this work are 6 channel, 2×67.5 μm SLCFETs with a gate width of 250 nm. The dimensions of the castellations are varied across different sample sets, but the repeating castellation unit is less than 160 nm long, meaning the devices consist of approximately 1000 castellations. The device layers are grown via MOCVD. The castellated gate is created in the superlattice using an electron beam lithography-written mask and a dry etch. A gate dielectric is then added to the top and side walls of the castellations. The gold gate contact is then deposited on top of this structure. The devices are symmetrical, meaning that $L_{GD} = L_{SG} = 1$ μm.

When the device is operated as a switch, the power dissipated in the devices is relatively low. However the SLCFET could also be used as an RF amplifier, in which case the power dissipation will be greatly increased. From a thermal perspective, the SLCFET is unique due to the nanometre scale features in the gate causing the dissipated power to be focussed into sections along the gate. This means it is important to understand how the heat flows around these castellations, and whether or not they cause an increase in channel temperatures that may in turn cause reduced efficiency or accelerated breakdown. In this chapter the temperature of these SLCFETs is studied using micro-Raman thermography. The results are used to develop a finite element model of the device, which is then compared to gate resistance thermometry (GRT) measurements taken by a colleague, Dr Dalcanale. The finite element model is then used to explore how heat flows in the system and to test possible design changes which will improve device thermal performance.

5.1 Method

A finite element simulation of the system was developed to aid understanding of the heat flow and to allow extrapolation from the temperature measurements to the channel temperatures, T_C. The first step was to develop a model of a single castellation. This castellation was then repeated several times to get a more realistic representation of a device. However the small feature sizes require many small mesh elements, making it computationally too intensive to create an entire device through this method. Instead, a simplified model which featured a continuous gate on top

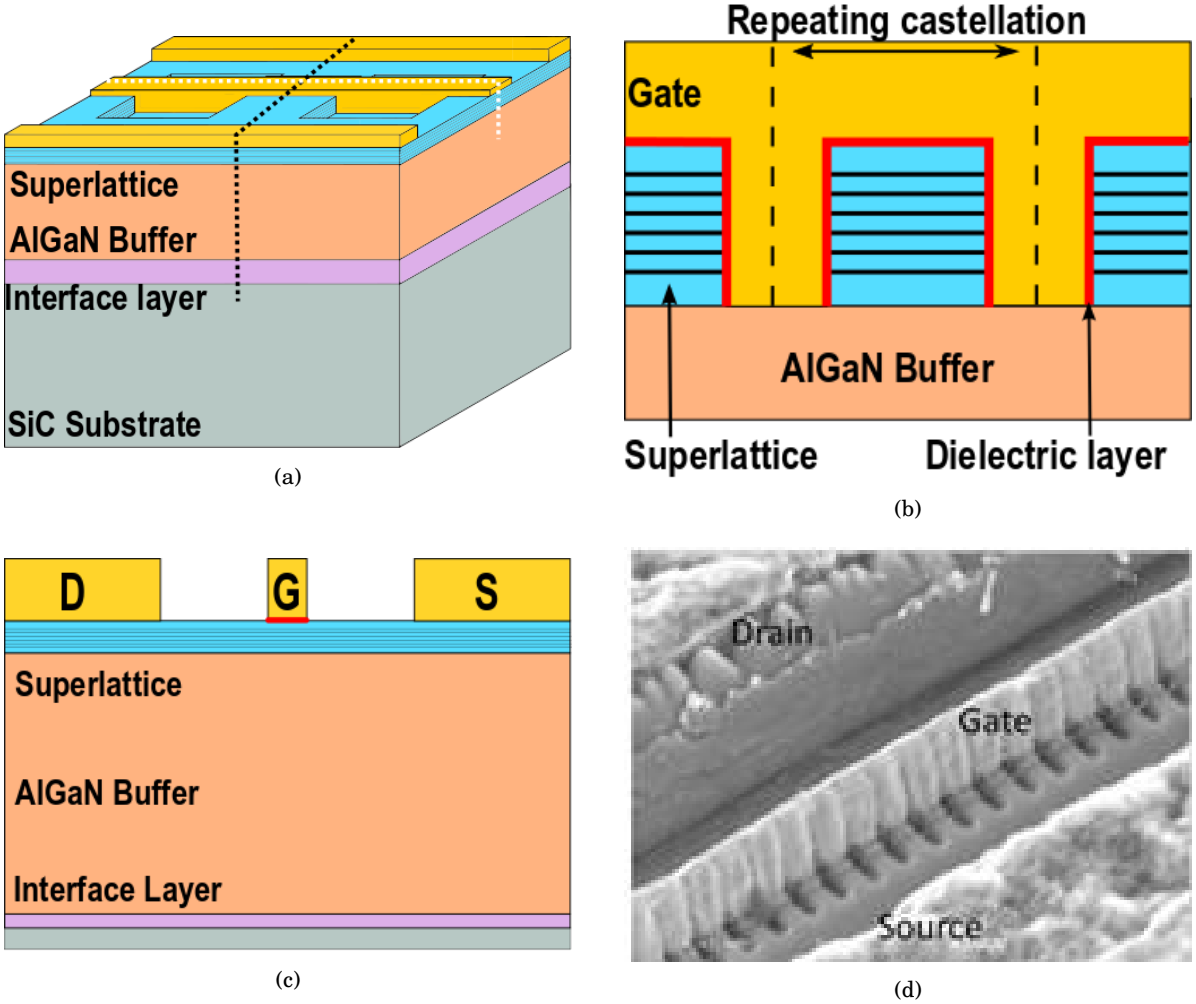


FIGURE 5.3. (a) A schematic diagram of a SLCFET showing the castellations. (b) A zoomed view of the castellations along the white dashed line in (a). The red line represents the gate dielectric. (c) A separate slice view along the black dashed line in (a). (d) A SEM micrograph of a SLCFET gate, originally published in References [243, 247].

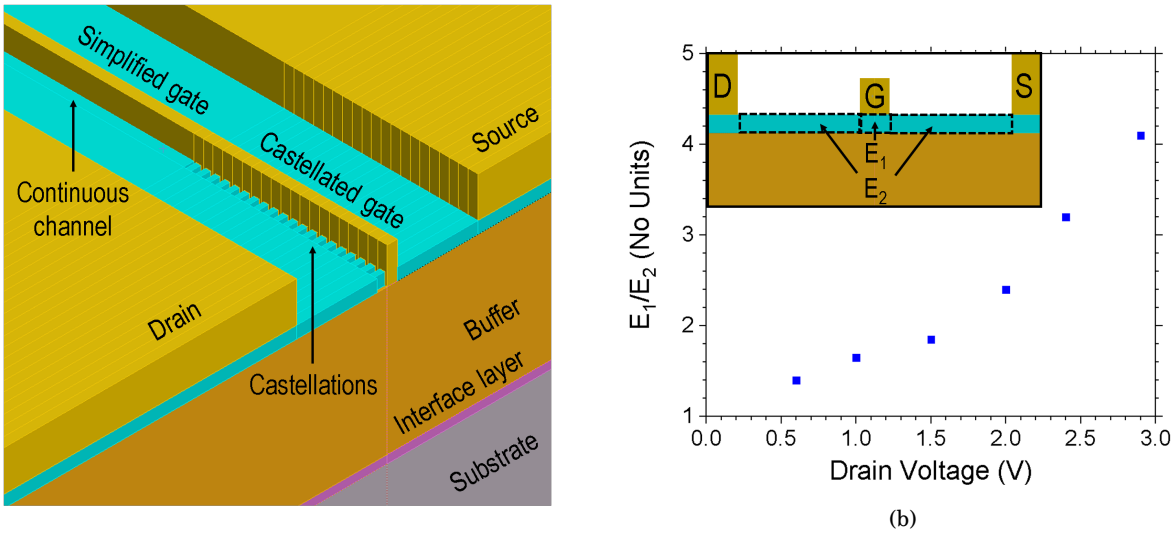
of a continuous superlattice was also created and adjoined to the castellations to approximate the whole device. The castellated and simplified areas of the model are shown in Figure 5.4 (a). One quarter of the device was simulated with insulating boundary conditions along the symmetry planes to replicate an entire device.

The castellations were simulated at the centre of a gate finger with the number of castellations varied to find the fewest for which the temperature at the centre of the device converged, making sure the impact of the simplified area is minimised. This was determined to be 20 castellations. The heat was deposited in the superlattice between the source and drain. To mimic the fact that power dissipation is higher under the gate, the heat generation was separated into 2 regions with different levels of power dissipation, demonstrated in the inset of Figure 5.4 (b). A 3D T-CAD electrical simulation generated by Dr Dalcanale using Silvaco ATLAS software was used to find the electric field profile in a 6 channel SLCFET from source to drain. Due to the high number of assumptions and the lack of a calibration measurement, only the ratio between the electric field under the gate (E_1) and the electric field in the access region (E_2) could be determined. As power density P_D is given by

$$P_D = j \cdot E \tag{5.5}$$

where E is the electric field and j is the current density, the ratio of electric fields under the gate and in the access region could be used to determine the relative power dissipated in these areas, as it can be assumed that the current density is constant.

The thermal conductivities of the SiC substrate (320 W/m.K), superlattice (11 W/m.K) and gold contacts 300 (W/m.K) were taken from literature [90, 248]. However the thermal conductivity of AlGaN is less well defined. Simulations of $Al_xGa_{1-x}N$ thermal conductivity were performed by Liu and Balandin for aluminium concentrations $0 < x < 1$ in steps of 0.1, with the results shown in Figure 5.5 (a). In the intermediatary region where $0.2 < x < 0.8$, the thermal conductivity is relatively constant, if low at approximately 30 W/m.K. However, at both extremes of aluminium concentration there is a sharp change in the thermal conductivity, with x = 0.1 giving a room temperature thermal conductivity of approximately 40 W/m.K, which is a quarter of the GaN thermal conductivity. As there are no measurements with smaller increments in the aluminium concentration a thermal conductivity value cannot be assigned to the AlGaN layer in the finite

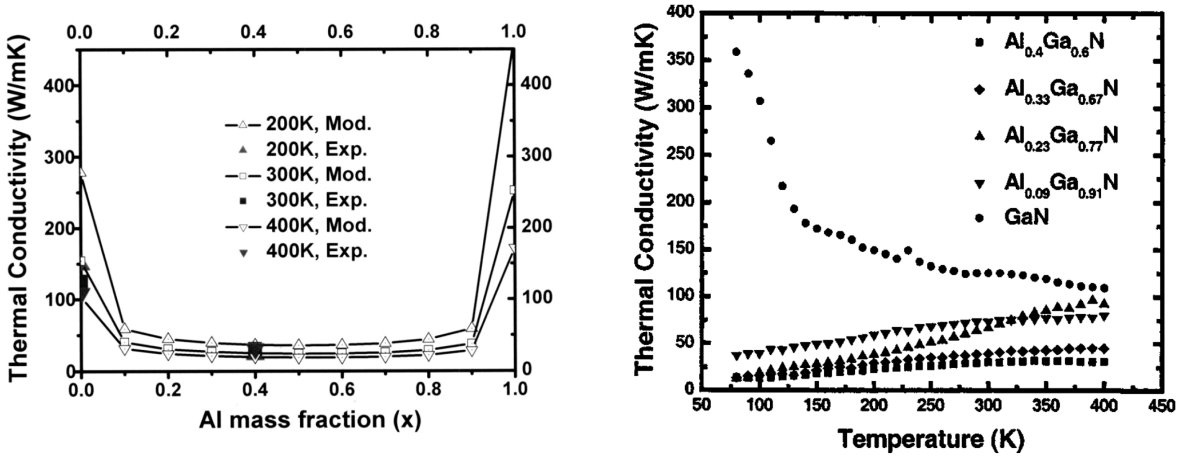


(a) (b)

FIGURE 5.4. (a) The centre of the simulated device showing both the castellated and the simplified area. In the castellated area, the superlattice is etched periodically and the gate fills the voids and hence the power density is higher. In the simplified region the superlattice is continuous and the gate sits atop it. (b) The ratio of electric field in the castellations (E_1) and in the access region (E_2), as found by the T-CAD electrical simulation. Inset is the location where the different electric fields, and hence power dissipations, are applied in the model.

element simulation, meaning this and the thermal boundary resistance between the AlGaN buffer and the SiC substrate must be determined experimentally. This was done by assigning a variable buffer thermal conductivity and thermal boundary resistance in the finite element model, and adjusting these variables until the finite element calculated temperature fit the micro-Raman thermography measurements. However, because the thermal conductivity and thermal boundary resistance cannot be decoupled, a mean thermal conductivity must be found for both layers. A later work by Liu and Balandin studied the temperature dependence of the thermal conductivity and the results are shown in Figure 5.5 (b) [45]. Based on these measurements, the AlGaN thermal conductivity in the finite element simulations was approximated as temperature independent at room temperature and above. This is likely because the alloying provides the dominant source of phonon scattering which is temperature independent, so the impact of umklapp scattering, which is temperature dependent, is less pronounced.

The micro-Raman thermography measurements performed in this work followed the proce-



(a) (b)

FIGURE 5.5. (a) Measurements and simulated predictions of the thermal conductivity of $Al_xGa_{1-x}N$ at varying x. Image adapted from Liu and Balandin [249]. (b) Temperature dependence of the thermal conductivity of AlGaN films. Aluminium alloying greatly reduces the temperature dependence as alloy scattering, rather than umklapp scattering, is now the dominant form of phonon scattering. Image adapted from Liu and Balandin [45]. Reprinted with permission from AIP Publishing.

dure described in Section 3.1. The 488 nm laser line of an argon ion source was used with a 50× objective that has a numerical aperture of 0.6 making the spatial resolution $\approx 0.4\mu$m. This was focussed on the device surface in the centre of the gate-drain access region as shown in Figure 5.6. The temperature dependence of the AlGaN E_2^h peak is used for the temperature determinations with the empirical constants in Equation 3.10, $A = 19.1$ cm^{-1}, $B = 1.2$, and $C = 568.5$ cm^{-1}. These values were taken from a calibration performed by Dr Pomeroy, which was then used in the measurement of the thermal performance of GaN-on-SiC HEMTs [213]. A measurement of the sample temperature approximately 300 μm from the device is taken at maximum power dissipation. This is used to estimate the thermal resistance between the sample and its holder R_{SH} which can then be incorporated into the model. The temperature caused by this thermal resistance is then subtracted from the simulated temperatures in the device, allowing a determination of the thermal resistance of just the sample, R_{Th}.

As can be seen in Figure 5.6 (b), the A_1(LO) peak appears significantly broadened in these samples. This means it cannot be used for temperature, stress or electric field measurements

as the precision is reduced such that the frequency shift cannot be properly distinguished. The reason for this change in peak shape is phonon-plasmon coupling. As discussed in Section 3.1, the A_l(LO) mode is polarised; it is an oscillation along the c-axis that creates a dipole. As it creates a dipole it has an associated electric field which can interact with plasmons, where plasmons are quasiparticles which represent quantised free carrier oscillation. In a typical, undoped, crystal there will not be enough free carriers for the phonon mode to couple to, coupling is however seen when free carriers are introduced, such as when GaN is doped with 1.5×10^{17} cm^{-3} of silicon [250]. When there is sufficient coupling the A_1(LO) mode broadens and red shifts, and two Longitudinal Phonon-Plasmon (LPP) coupled modes appear in the spectra [251]. This effect is not typically seen in GaN HEMTs with a single AlGaN/GaN heterostructure, and as the SLCFETs studied in this work are nominally undoped, the implication is that the superlattice channel results in more free carriers. As the strength of the phonon-plasmon interaction is dependent on the free carrier concentration, it is possible to use the red shift in the A_1(LO) peak to predict the carrier density in the superlattice channel, if it is assumed that there are negligible free carriers in the buffer [252].

GRT is a complementary technique which uses the temperature dependence of the electrical resistance of metals to measure the temperature of the gate [253]. The technique uses a specially designed device structure shown in Figure 5.7 (a). In addition to the source, drain, and gate contacts there are four additional contacts; two at each end of the gate finger. These are used to force a current of less than 10 μA and measure the voltage. Similar to the diamond thin film thermal conductivity measurements made in Section 4.2, by having contact pads specifically available for measuring the voltage, the resistance of other components in series with the current supply are not measured and only the gate metal is tested. The temperature dependence of the resistance was calibrated using a temperature controlled stage. The measurements and initial temperature calculations were performed by a colleague so will just be reported here.

The temperatures measured with this technique cannot be used to directly determine the thermal resistance of a device. It can be seen in Figure 5.7 (a) that the gate extends beyond the active area, meaning the measured gate temperature T_{GM} will be significantly lower than the peak gate temperature T_{GP}, which in turn will be lower than the channel temperature T_C

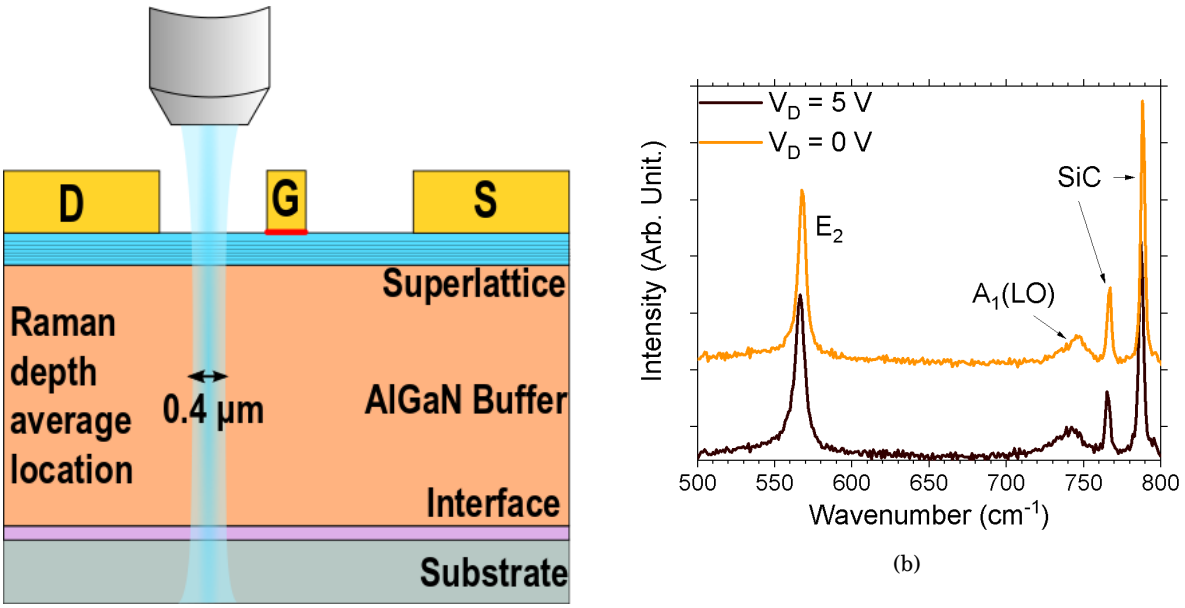


FIGURE 5.6. (a) A schematic diagram of the area measured in micro-Raman thermography looking along the gate finger. (b) An example of Raman spectra collected at two separate drain biases.

because of the dielectric layer separating the channel from the gate. Hence it is necessary to use the finite element simulations to move from T_{GM} to a thermal resistance calculation, as demonstrated in Figure 5.7. However there are challenges associated with this. The complex gate structure means that it is not possible to model an entire gate finger with castellations. Therefore the simplified model with no castellations and a continuous gate was used as an approximation to find a relationship between T_{GM} and T_{GP}. Figure 5.7 (b) shows the effective GRT measurement result, which averages the temperature along the entirety of the gate to give a constant temperature both in and out of the active area.

Due to the sample layout, it was not possible to measure the sample-holder interface thermal resistance R_{SH}, and it could not be assumed to be the same as in the case of the micro-Raman thermography experiments as the experimental set up and sample geometry were different. The finite element model could be used to produce temperature distributions along the gate, as shown in Figure 5.7 (b). The R_{SH} was varied and optimised in the finite element simulation until the integrated area under the gate profile divided by the gate length, is equal to T_{GM} and the model

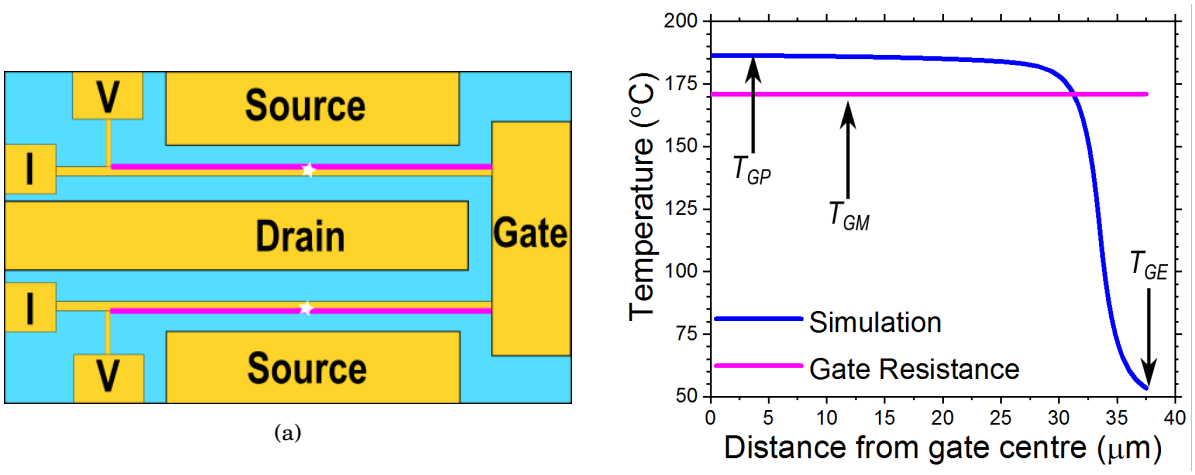


FIGURE 5.7. (a) A schematic of the GRT test structures which contains four extra contact pads. The pads labelled I are used to force the current, whereas the pads labelled V are used to measure the voltage, and hence resistance. The purple lines indicate where the resistance is measured. (b) Simulated temperature profile of the gate in blue. The purple line shows the averaged temperature as would be measured by GRT. In this case the integrated areas of the curve are the same, suggesting the simulation matches the experiment.

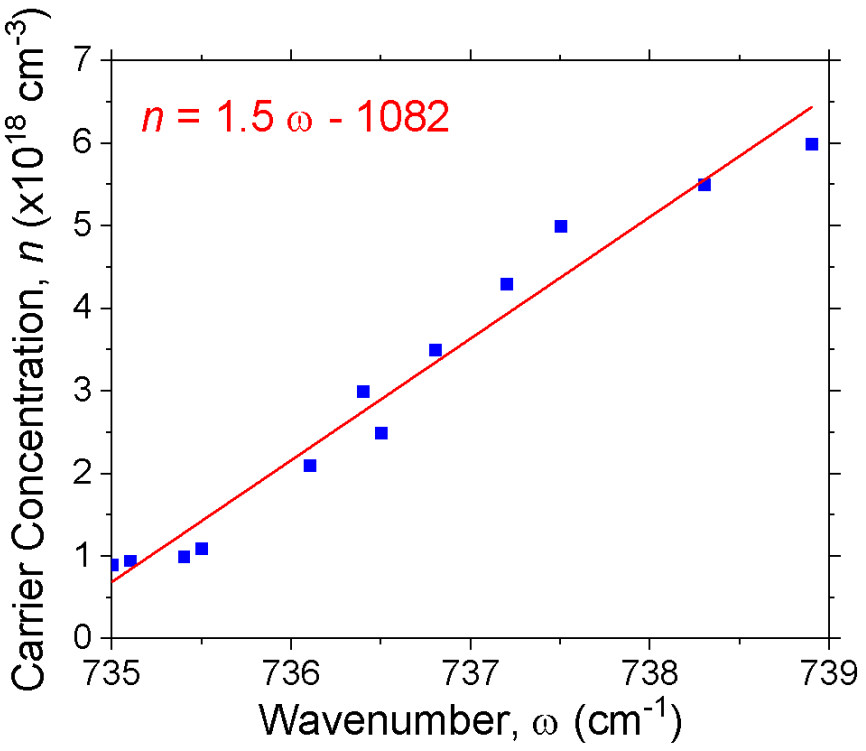
can be said to match the experiment. The simulated gate temperature profile was found to be independent of R_{SH} and so the relationship between peak gate temperature and GRT measured temperature was found as

$$\Delta T_{GP} = 1.11\Delta T_{GM} - 0.11\Delta T_{GE} \tag{5.6}$$

where ΔT_{GE} is the temperature at the end of the gate finger, and all the temperatures are relative to the chip temperature. Once this is applied, T_{GP} is known. It is then possible to vary R_{SH} in the castellated model to make this match the experimental T_{GP} and then predict T_C, and hence R_{Th}.

5.2 Results

The position of the A_1(LO) peak in the Raman spectra is found to be 745 ± 2 cm^{-1}, with the error bars found as the standard error on the mean of a sample of 16 spectra. By fitting a linear curve to the data displayed in Reference [109] this could be converted to a carrier density of



(a)

FIGURE 5.8. Data from Huang *et al.*, showing the correlation between the A_1(LO) peak position and the carrier concentration in GaN. A linear fit is performed, and the resulting equation used to predict the carrier concentration in SLCFETs.

$1.2 \pm 0.2 \times 10^{19}$ cm^{-3}. It is worth noting that this is an extrapolation, as the data reported in Reference [252] and displayed in Figure 5.8 is for A_1(LO) peak positions between 735 cm^{-1} and 739 cm^{-1}. The determined carrier density can be achieved through silicon doping, where values as high as 10^{21} cm^{-3} have been reported by Arakawa *et al.* [254]. However when carrier densities over 10^{19}cm^{-3} are induced by doping, the authors found that the mobility is severely decreased to lower than 200 cm^{2}V^{-1}s^{-1} because of scattering from the donor ions [254]. As discussed in Section 2.2.4, the 2DEG is not induced by dopants, and its confinement means it is spatially separated from lattice defects, meaning the mobility stays high in SLCFETs. This corresponds with what was reported by Sheng *et al.* who found mobility enhancements in superlattices, showing that they are an attractive route for low resistance, high carrier concentration GaN [246].

The micro-Raman thermography measured temperatures, the simulated average temperature

in the measurement location, and the simulated peak channel temperature ΔT_C are displayed in Figure 5.9 (a). As with all temperatures displayed in this section they are a temperature increase with respect to the chip temperature, such that R_{SH} can be disregarded. In the case of the Raman measurements this was measured and subtracted from the temperatures shown. The mean thermal conductivity of the AlGaN buffer and the interface layer (κ_{B+I}) which gave the best match to the micro-Raman thermography measurement was found to be 46.3 W/m.K. Assuming that the buffer and interface layer act as two thermal resistors in series, the thermal resistance of the two layers is simply the sum of the two layers. Noting that the thermal resistance R is given by

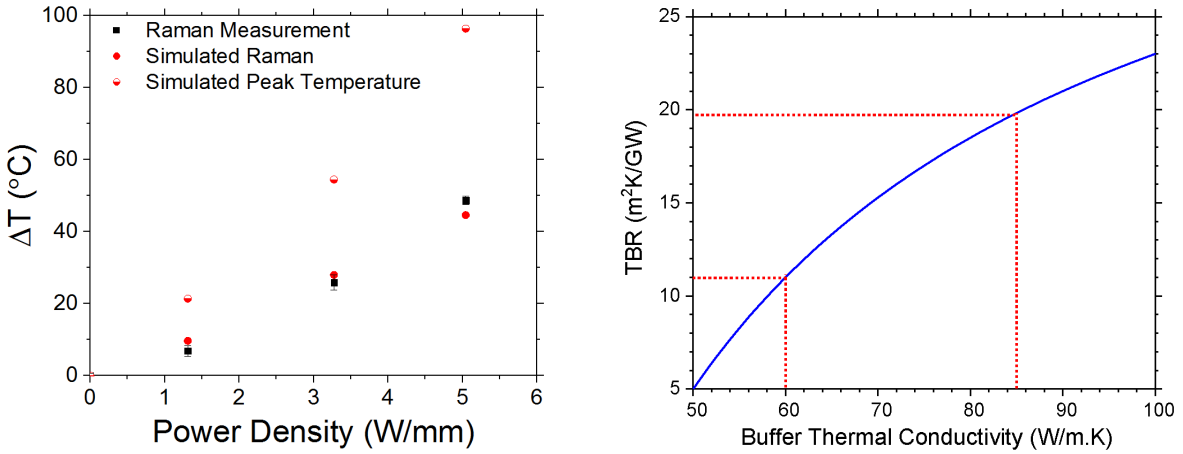
$$R = \frac{d}{\kappa} \tag{5.7}$$

where d is the material thickness and κ is the thermal conductivity, it follows that

$$\frac{d_{B+I}}{\kappa_{B+I}} = \frac{d_B}{\kappa_B} + \frac{d_I}{\kappa_I} \tag{5.8}$$

where the subscripts B and I refer to the properties of the buffer and interface respectively. The last term in this relationship is the thermal boundary resistance (TBR) between the buffer and the substrate. There are an infinite number of buffer thermal conductivities and thermal boundary resistances which satisfy this relationship with a range shown in Figure 5.9 (b), but based on what can be reasonably expected, a range of possible AlGaN buffer thermal conductivities and TBR's can be suggested. Manoi *et al.* reported that the TBR of a GaN-on-SiC system could be between 5-60 m^2K/GW, so this cannot be used to narrow down the potential values [255]. However, in spite of the lack of relevant data points, based on the AlGaN thermal conductivities reported by Liu and Balandin and shown in Figure 5.5 it can be predicted that the thermal conductivity of the AlGaN buffer in these SLCFETs is in the range of 60-85 W/m.K. These boundaries are marked on Figure 5.9 (b), and are found to correspond to a TBR of $\approx 16 \pm 4$ m^2K/GW.

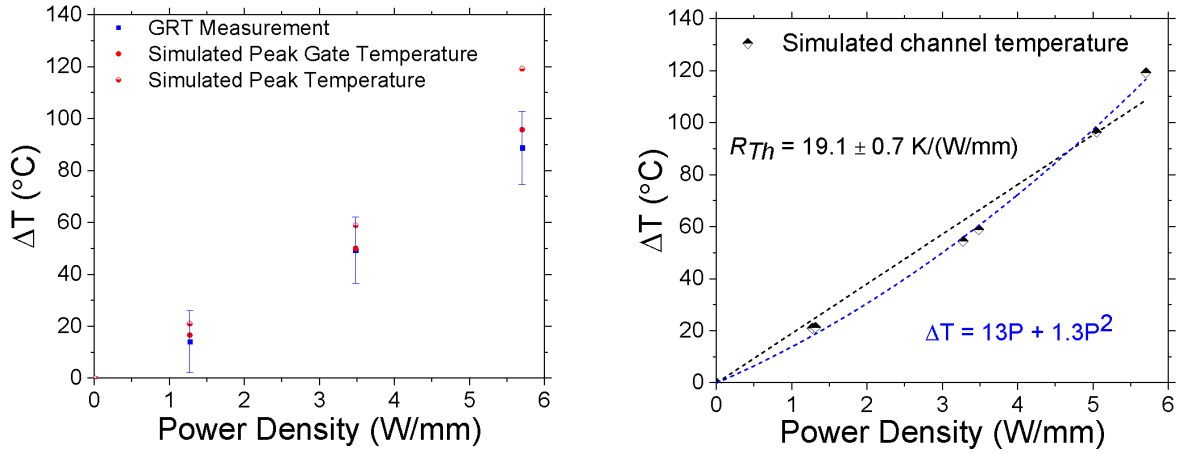
It can be seen in Figure 5.9 (a) that the simulated peak temperature is not linear with respect to power density. This is caused by the temperature dependence of the thermal conductivity of some materials. However the effect is weak as, in the finite element model, the temperature dependence of the superlattice, AlGaN buffer, TBR, and metal contact thermal conductivities are all approximated as constant. The GRT measured temperature ΔT_{GM}, the peak gate temperature



(a) (b)

FIGURE 5.9. (a) Results of micro-Raman thermography measurements along with simulated temperatures in the micro-Raman measurement position and the peak simulated temperatures. (b) The blue line represents the buffer thermal conductivities and TBR's which could match the simulated results. The red lines indicate the area of most likely values, based on the AlGaN thermal conductivity predictions made in Reference [45].

ΔT_{GP} found from applying Equation 5.6 and the simulated channel temperatures ΔT_C are shown in Figure 5.10 (a). The buffer and interface mean thermal conductivity of 46.3 W/m.K found from the Raman measurement was used in the simulation, but as it was not possible to measure R_{SH} this was adjusted in the model until the simulated ΔT_{GP} matched the experimentally determined values. The chip temperature was then subtracted from all measured and simulated temperatures to give the result shown. The same non-linearity in ΔT_C with respect to power density can be seen here. The calculated ΔT_C from both Raman and GRT are shown in Figure 5.10 (b). Typically, a linear fit is performed to determine the thermal resistance R_{Th} and this yielded a result of 19.1 ± 0.7 K/(W/mm). However when trying to predict temperatures experienced at certain power densities a 2nd order polynomial fit proves more accurate. Both the linear and polynomial fits are forced through the origin as there should be no temperature rise when the device is not being operated.



(a) (b)

FIGURE 5.10. (a) Measured and simulated gate temperatures along with predicted peak temperatures. (b) Predicted peak temperatures at the power densities studied in the GRT and Raman measurements. A linear fit is performed to find R_{Th} and a quadratic fit is also performed with parameters shown.

5.3 Discussion

The measured thermal resistance for the device of 19.1 ± 0.7 K/(W/mm) is higher than thermal resistances of GaN-on-SiC wafers with 2 × 100 μm gate finger device structures measured over the same power dissipation range, which have had thermal resistances reported in the literature as low as 14 K/(W/mm) for a TBR of 17 m^{2}K/GW [36]. However it is not possible to say that the SLCFET gate design is culpable for the higher thermal resistance as the areal power density is higher in the SLCFET and the SLCFET utilises an AlGaN buffer. The mean thermal conductivity of the buffer and interface was 46.3 W/m.K which, when a typical TBR of 16 m^{2}K/GW is considered, corresponds to a buffer thermal conductivity of 72 W/m.K; this is less than half the thermal conductivity of GaN. The thermal resistance of AlGaN-on-SiC devices was measured by Kabouche *et al.* and found to be 17.5 m^{2}K/GW, although these devices used a buffer with an 8% aluminium content suggesting the thermal resistance of the buffer will be higher, and the TBR was not measured or estimated [256].

All of the simulations used to provide the thermal resistance calculations rely on optimised parameters, including the buffer and interface thermal conductivity in the case of micro-Raman

thermography and the sample-holder thermal resistance R_{SH} in the case of the GRT measurements. The simplest way to achieve a free-parameterless simulation would be to use micro-Raman thermography to calibrate the buffer and interface thermal conductivities, and use an adjusted form of the GRT measurement where R_{SH} can be measured simultaneously. This was attempted through integrating the GRT measurement set up with the micro-Raman thermography, but was not successful as the optical equipment is secured in place, and there is insufficient space to introduce the 7 probe micropositioners required to bias the device and measure the resistance of the gate. Instead an attempt was made to wire bond the device to a package which could be interfaced easily with the power supply and source-measurement unit, however the contact pads were too small for the wire-bonding equipment available, so this also failed. To measure R_{SH} in the future, a device design with larger contact pads would allow wire-bonding and hence integration with the optical equipment. Alternatively, if a resistor structure was fabricated near the GRT structure, the temperature dependence of the resistor could be calibrated and be used to measure the chip temperature.

To judge the impact of the buffer thermal conductivity on thermal resistance it was varied in the finite element simulation with the TBR kept at 16 m^2K/GW. It was found that utilising a GaN buffer could reduce ΔT_C by 25°C at 5.7 W/mm power dissipation, lowering the thermal resistance to 16.7 K/(W/mm) from 21 K/(W/mm). However the aluminium alloying adds electrical benefits to the device. As discussed in Chapter 1, wider bandgaps are desireable as they allow higher temperature operation, and can allow higher voltage operation as the breakdown field is proportional to the bandgap to the power of 2.5. Alloying GaN with aluminium is an effective means of increasing the bandgap and hence the breakdown voltage, whilst maintaining many of the benefits of a GaN HEMT, so for device applications this may continue to be a requirement. An alternative for improving the R_{Th} is replacing the SiC substrate with a diamond substrate, which was shown in Section 4.3 to produce low thermal resistance devices. In devices with GaN buffers, replacing a SiC substrate with a diamond substrate has been shown to reduce the thermal resistance from 14 K/(W/mm) to 10 K/(W/mm) [36]. However the impact is lower in the SLCFETs studied here due to the large thermal resistance of the AlGaN buffer which sits between the channel and substrate; the thermal resistance was reduced to just 17.5 K/(W/mm)

when a diamond substrate with a constant thermal conductivity of 1500 W/m.K was used in place of the SiC. This approximation of a diamond substrate was used instead of the more detailed layer structure described in Section 4.3 due to constraints on the computational performance available.

A summary of how changes to the device impact the heat profile in the device is shown in Figure 5.11 (a), which shows the temperature in each layer of the epitaxy at 5.7 W/mm of power dissipation. In this Figure, a steep temperature gradient represents a layer with a large thermal resistivity. As per Equation 5.7, it is this gradient combined with the thickness of the layer that defines its thermal resistance. When comparing the standard SLCFET configuration with that of a SLCFET with a GaN buffer, it can be seen that the temperature at the buffer-substrate interface is the same. However the gradient in the GaN buffer is lower, which is why this configuration has a lower peak temperature. Similarly, the temperature gradient in the diamond substrate is significantly lower than that of the SiC substrates, meaning the temperature at the interface of an AlGaN-Diamond system is lower than in an AlGaN-SiC or GaN-SiC system. This results in the temperatures of the layers above the substrate effectively being translated down, without changing the temperature gradient in the AlGaN buffer, and so the reduction in the peak temperature is limited. The temperature at the bottom of the substrate will be lower which eases the heat extraction burden on the packaging. The switch to a GaN buffer results in lower peak temperatures, although the temperature at the back of the substrate is the same as when an AlGaN buffer is used, meaning it does not give this added benefit.

It could be expected that the castellations would localise the power density and result in higher peak temperatures and accelerated device degradation. However as discussed above, the thermal resistance of the devices is similar to reported literature values for devices with 2D gates, and any differences can likely be explained by the different wafer epitaxies. To understand this, the finite element model was used to analyse the heat flux through the device. For the case of maximum power dissipation (5.7 W/mm) the heat flux in a castellation is shown in Figure 5.11 (b). For the heat to be extracted from the wafer it must spread vertically through the buffer and substrate to the heat sink. The gold gate contact plays an important role in the initial heat spreading, pulling the heat laterally before it spreads vertically through the buffer. This is

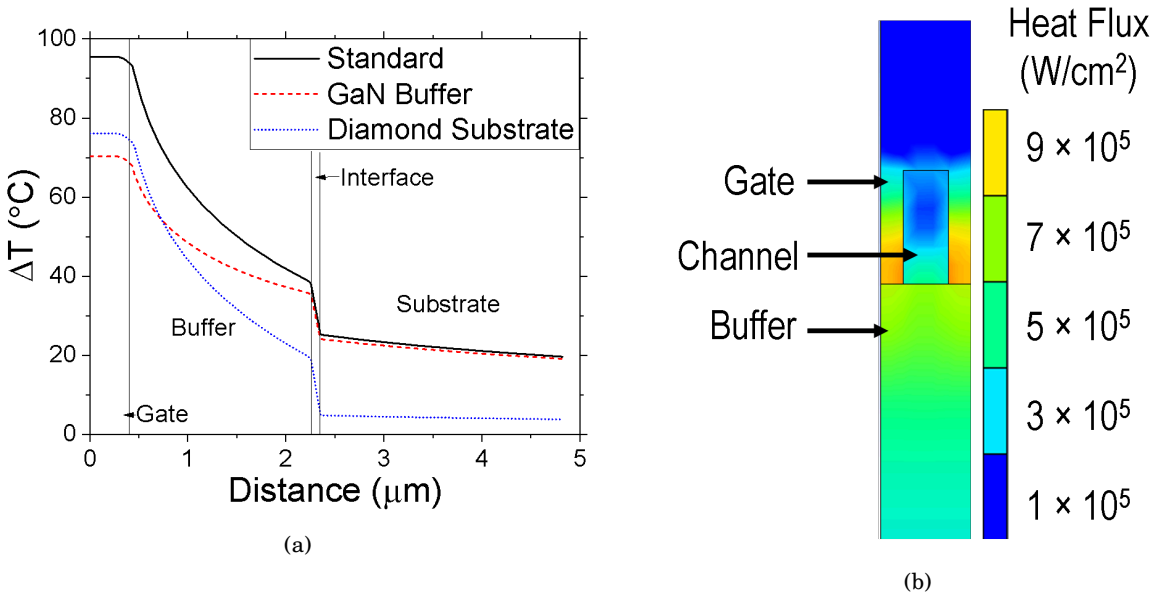


FIGURE 5.11. (a) Finite element simulations of the temperature profile through the epilayers of a SLCFET at the centre of the device. A comparison is made between the standard device structure, a device with a GaN buffer instead of an AlGaN buffer, and a device with a diamond substrate instead of a SiC substrate. (b) Heat flux in a single castellation (looking from source to drain) found through finite element simulations. It can be seen that the heat flux is significantly higher though the base of the gate than through the base of the channel.

evidenced in Figure 5.11 (b), and it is found that there is twice as much heat flow through the gate-buffer interface as there is through the channel-buffer interface. The importance of the gate is highlighted when the gold is replaced with a superlattice. In this case, with the 5.7 W/mm of power dissipation located in the previously described regions, R_{Th} increases to 23.5 K/(W/mm), a 12% increase. The impact of the gate metal on heat spreading is further shown in Figure 5.12. This image shows the temperature distribution at V_D = 1 V, P_D = 1.3 W/mm. From Figure 5.4 (b) it can be seen that the power density is 1.5× higher under the gate than in the access region at this drain voltage. In spite of this higher power density, Figure 5.12 shows that the peak temperatures actually occur in the access regions rather than under the gate. This highlights the fact that the gate aids heat flow, acting as a low resistance heat pipe into the buffer.

The thermal resistance of a SLCFET can be improved by maximising this heat-piping effect provided by the gold gate. Currently the lateral heat flow is inhibited by the presence of the gate

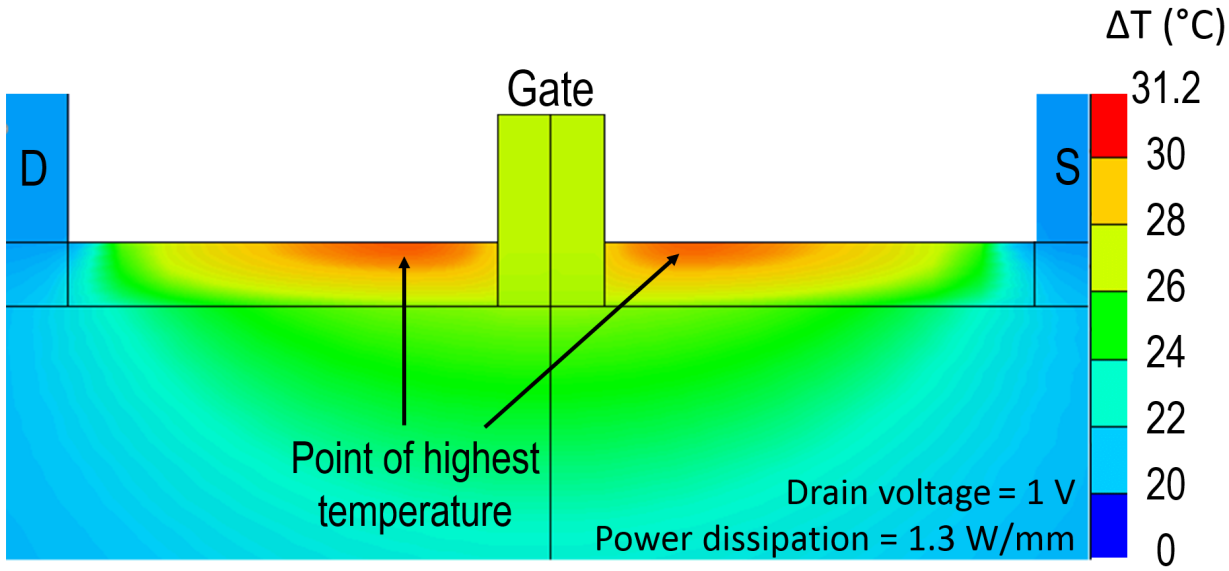


FIGURE 5.12. Finite element simulation of the temperature profile between the source and drain in a SLCFET. At V_D = 1 V the electric field is 1.5× higher under the gate than in the channel. However the point of highest temperature occurs in the access region, as the high thermal conductivity gold gate aids heat spreading in its vicinity.

dielectric. This amorphous material gives an effective thermal boundary resistance ($TBR_{eff\text{-}GD}$) of 15 m^2K/GW. As a result, the temperature in the channel is 21°C hotter than the gate at 5.7 W/mm of power dissipation. If the thickness is reduced to one third, and hence the $TBR_{eff\text{-}GD}$ is reduced to 5 m^2K/GW, then the channel is only 10°C hotter than the gate, and the thermal resistance of the SLCFET is reduced to 17.2 K/(W/mm). This reduced R_{Th} occurs as more heat can flow through the gold gate contact with 3 times as much heat flowing through the base of the gate as through the base of the channel, increased from 2 times as much heat flow when the gate dielectric is thicker.

5.4 Summary

Superlattice castellated field effect transistors are a promising technology for broadband, low loss, high reliability RF switches. The superlattice channel reduces the ON resistance whilst not

impacting the OFF capacitance, resulting in an improved cutoff frequency as cutoff frequency is proportional to on resistance. The 3D castellated gate is necessary to lower the threshold voltage but is also found to impact the heat flow in the device.

Micro-Raman thermography measurements were used to determine the temperature in the device buffer, which was then used to calibrate the buffer and interface layer thermal conductivities in a finite element simulation of the device. The gate temperature was measured using gate resistance thermometry. The finite element model was then used to extrapolate from these measurements and predict the channel temperatures. From these channel temperatures the device thermal resistance was found to be 19.1 K/(W/mm) for power dissipations up to 5.7 W/mm. This is higher than the thermal resistances found for GaN-on-SiC but the majority of this difference can be attributed to the AlGaN buffer, which has a lower thermal conductivity than a GaN buffer [36]. The measured thermal resistance is closer to that of GaN HEMTs which have an AlGaN back barrier, implying the SLCFET gate design has a low impact on the thermal resistance.

The reasons behind this were investigated using the thermal finite element model. It was found that heat flows primarily through the high thermal conductivity gate contact which acts as a heat pipe into the buffer. Without this high thermal conductivity material, the thermal resistance was found to increase by 12%. Methods for improving the thermal performance of the devices were investigated. The heat piping effect can be increased by thinning of the gate dielectric. The largest improvement came from replacing the AlGaN buffer with a GaN buffer, which reduced the thermal resistance at 5.7 W/mm to 16.7 K/(W/mm). Replacing the SiC substrate with a diamond substrate was found to have a similar impact, although it was not as large as seen in GaN devices due to the thermal resistance of the AlGaN buffer.

CHAPTER 6

ULTRA-WIDE BANDGAP MATERIALS FOR HIGH PERFORMANCE DEVICES

The work presented in this chapter was undertaken to further our understanding of materials which may form the future of high performance electronics, in particular $\beta - Ga_2O_3$ and AlGaN. Relative to GaN, research into these materials is immature, meaning device structures are yet to be optimised and some fundamental properties are yet to be explored. The effect of a materials bandgap on the electrical properties of devices was discussed in detail in Chapter 2. A wider bandgap gives less thermal noise and allows higher voltage operation, which improves efficiency and allows smaller device architectures. The importance of having a wide bandgap is highlighted when figures of merits are considered. Some common examples are the Lateral Baliga Figure Of Merit (LBFOM) which was derived for power devices

$$\text{LBFOM} \propto \mu E_b^2, \tag{6.1}$$

the Johnson's Figure Of Merit (JFOM) which was derived for RF devices

$$\text{JFOM} = \left(\frac{E_b v_s}{2\pi}\right)^2, \tag{6.2}$$

and the Combined Figure Of Merit (CFOM) which attempts to provide a generic view of a material's electronic properties

$$\text{CFOM} = \kappa \epsilon \mu v_s E_b^2. \tag{6.3}$$

In these figures of merit κ is the thermal conductivity, ϵ is the dielectric constant, μ is the carrier mobility, v_s is the carrier saturation velocity, and E_b is the breakdown field [257, 258]. The breakdown field is a dominant term in each of these figures of merits, and

$$E_B \propto (E_G)^{2.5} \tag{6.4}$$

where E_G is the bandgap, stressing the benefit of a wider bandgap [15].

The most mature UWBG materials being studied include, diamond, AlGaN, and $\beta-Ga_2O_3$. Diamond has a significantly higher thermal conductivtiy than GaN and SiC, but the opposite is true for AlGaN and $\beta-Ga_2O_3$. The thermal conductivity of AlGaN was discussed in Chapter 5, where it was found that low alloying of aluminium in a GaN buffer possibly reduced its thermal conductivity by half. Liu and Balandin showed that, for between 10% and 90% alloying concentration, the thermal conductivity was approximately 25 W/m.K at room temperature, which is 16% and 10% of the thermal conductivity of unalloyed GaN and AlN respectively [249]. This severe decrease is due to phonon scattering at the alloying atoms. The thermal conductivity was also found to have minimal temperature dependence as umklapp scattering is not the dominant scattering mechanism [45]. $\beta-Ga_2O_3$ has an inherently low thermal conductivity due to a large probability of umklapp scattering which was shown through Equation 2.26 to be due to the low phonon velocity and Debye temperature in $\beta-Ga_2O_3$ [46]. There are conflicting reports of the thermal conductivity in the literature, with variation in measured and calculated values, but the consensus places the maximum thermal conductivity along the [0 1 0] direction between 22 and 27 W/m.K, whilst the minimum appears to be along the [1 0 0] direction between 11 and 16 W/m.K [46, 197]. There is a T^{-x} temperature dependence with x between 1.1 and 1.4 [197].

These low thermal conductivities make device design in $\beta-Ga_2O_3$ and AlGaN particularly challenging. Whilst an UWBG may allow higher electric fields to be sustained, this will lead to higher power densities and hence temperatures if the heat cannot be efficiently extracted. This chapter first studies how phonons decay in $\beta-Ga_2O_3$ crystals by analysing the temperature dependence of the phonon lifetimes. Temperature measurements performed on $\beta-Ga_2O_3$ MOSFETs are then discussed, which highlight the need for effective thermal management. Finite element simulations are then used to explore possible solutions to the thermal challenges

presented by these UWBG materials.

6.1 Phonon lifetimes and decay mechanisms in $\beta - Ga_2O_3$

Study of the decay mechanisms of phonons in semiconductor crystals is important for the understanding of how 'hot electrons' relax in devices. Hot electrons is a name given to those electrons with sufficiently high kinetic energy to overcome potential barriers in devices. They are particularly prevelant in RF devices due to the fast switching speeds and can degrade device performance through trapping in defect states not typically reachable for standard electrons or by increasing leakage through dielectric layers [100]. Most commonly, hot electrons relax through interactions with phonons. For the electrons to thermalise with their surroundings they must emit phonons at rate G_e. Then for the system to be in equilibrium, the rate of change of the phonon population is

$$\frac{dn_p}{dt} = G_e - \frac{n_p - n_{p-0}}{\tau_p} = 0 \tag{6.5}$$

where n_p is the phonon population n_{p-0} is the equilibrium phonon population, and τ_p is the phonon lifetime [259]. Hence the hot electron relaxation rate is dependent on the phonon relaxation rate, making this parameter important for optimising device design. If the relaxation time is longer, the electron relaxtion rate G_e will be lower, which will increase hot electron related degradation effects.

Because of the role phonon lifetimes play in hot carrier relaxation they have been measured and predicted in a wide range of semiconductors. The first recorded measurements of phonon lifetimes were performed by analysing the linewidth of Raman modes in silicon and germanium with results of 15 ps and 13 ps respectively [260]. A similar technique found much shorter lifetimes in GaAs with values between 0.6 and 1.3 ps, although a separate experiment which used a laser to excite the phonon modes and measured the lifetime through changes in the reflectivity found the lifetime to be approximately 2 ps [261, 262]. Tsen *et al.* performed time resolved Raman measurements on GaN samples. They used a short laser pulse to excite electron-hole pairs which would decay with the aid of a phonon. A 2 fs laser pulse was then used to measure the intensity of the Raman signal, the decay of which could be used to determine the phonon lifetime. By

performing this at a range of temperatures the decay mechanism of the phonon modes were also found [263]. These techniques have been used to find lifetimes in AlN, InN, InAs, InP, GaP, and ZnSe among others [264–268].

In this section Raman spectroscopy linewidth measurements are used to determine the phonon lifetimes in two $\beta - Ga_2O_3$ crystals supplied by the Air Force Research Laboratory; one [1 0 0] orientated crystal and one [$\bar{2}$ 0 1] orientated crystal. The temperature dependence of these lifetimes is then analysed to ascertain the probable decay mechanisms, correlating these with phonon density of states for other compound semiconductors published in the literature.

6.1.1 Method

The phonon lifetimes were found via the Raman spectroscopy linewidth method similar to that used in References [260, 264, 265]. The Raman modes in the system represent the excited states of phonons, and as such they follow the uncertainty principle

$$\Delta E \Delta t \geq \frac{\hbar}{2} \tag{6.6}$$

where E is the energy of the excited state and t is its lifetime [269]. As energy is related to frequency f via

$$E = hf \tag{6.7}$$

it follows that the frequency of a Raman mode cannot be known precisely. This uncertainty is represented in the width of Raman spectral lines which do not represent δ-functions as may be expected if the energy were measured precisely. As is suggested in Equation 6.6 the magnitude of this energy uncertainty, and hence the linewidth, is inversely proportional to the lifetime of the state, meaning it can be used as a measure of lifetime. This natural broadening can be represented by a Lorentzian line profile.

However it is not solely the energy uncertainty that causes the spectral lines to have a finite linewidth. It is possible for broadening to occur in the sample due to imperfections in the crystal. The resonant frequencies of the phonon modes is reliant on the atomic masses and the bonding. If the bond length changes because of local strain, or the defects change the atomic mass, this will cause subtle variations in the resonant modes which will result in a broadening of the

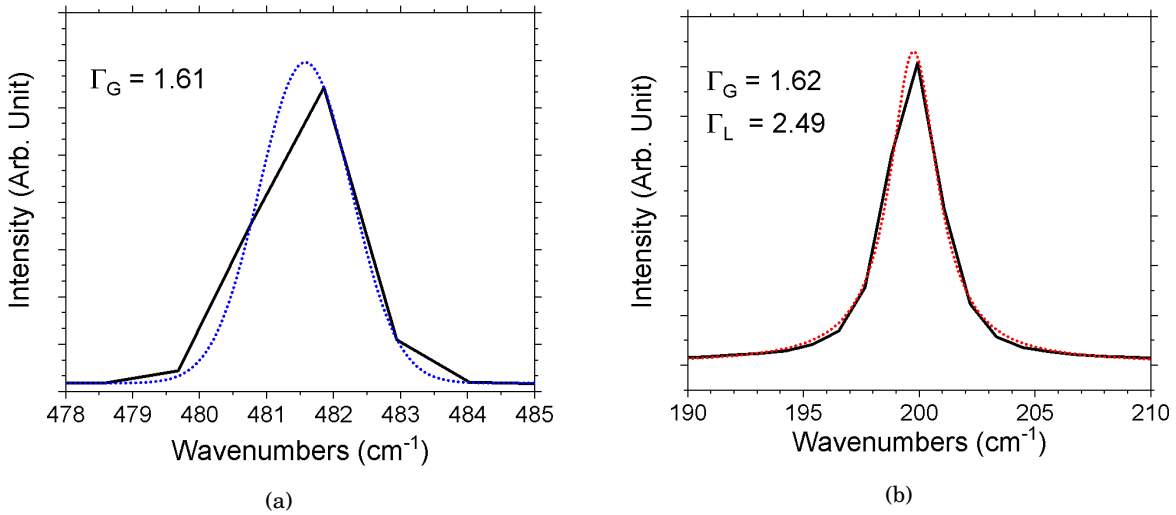


FIGURE 6.1. (a) Gaussian fit of the spectrometer-induced broadening of a monochromatic light source which had a full width at half maximum value of $\Gamma_G = 1.61$. (b) Psuedo-Voigt fit of the A_G^3 Raman mode in $\beta - Ga_2O_3$. The pseudo-Voigt fit has its (Γ_G) fixed to the width caused by the spectrometer broadening, allowing determination of the Lorentzian width (Γ_L) which is used to determine the phonon lifetime.

linewidth. The lifetime measurements, like all Raman spectroscopy measurements in this thesis, were performed using a Renishaw Invia spectrometer described in Section 3.1.3. The spectral resolution of a spectrometer is primarily determined by the diffraction grating which disperses the light, the detector pixel size, and the light entrance slit width.

For this experiment a 532 nm frequency doubled Nd:YAG laser was used as the excitation source. A 50× focussing lens with a NA of 0.6 was used. The slit width was set to 10 μm, and a diffraction grating with a line density of 300 lines per mm was used. With these parameters, five measurements of a monochromatic source were taken, with a mean full width at half maximum of 1.62 ± 0.02. With this known, a pseudo-Voigt fit of the $\beta - Ga_2O_3$ Raman spectral peaks can be performed. A Voigt profile is a convolution of Lorentzian and Gaussian profiles, and as such is often used to fit spectral lines. In this work the pseudo-Voigt profile is used which is a linear combination of the Lorentzian and Gaussian profiles rather than a true convolution, making it simpler to compute. It takes the form

$$y = y_0 A \times \left[\mu \left\{ \frac{2\Gamma_L}{\pi(4(x-x_c)^2 + \Gamma_L^2)} \right\} + (1-\mu) \left\{ \frac{\sqrt{4\ln 2}}{\sqrt{\pi}\Gamma_G} \exp\left(\frac{-4\ln 2}{\Gamma_G^2}(x-x_c)^2 \right) \right\} \right], \tag{6.8}$$

where the first term in curly brackets is the Lorentzian part of the profile and the second term in curly brackets is the Gaussian part of the profile. Here Y_0 is the baseline factor, A is an amplitude factor, μ is a shape factor which designates how 'Lorentzian' or 'Gaussian' a peak is, x_c is the peak centre in wavenumbers, and Γ_L and Γ_G are the widths of Gaussian and Lorentzian peaks respectively. By fixing the Γ_G to the value for spectrometer broadening, a value for Γ_L can be found in the Raman spectra. An example of a pseudo-Voigt fit is shown in Figure 6.1 (b). The relationship between this linewidth and the phonon lifetime τ_p is

$$\frac{\Gamma_L}{\hbar} = \tau_p^{-1} \tag{6.9}$$

which is a rearrangement of Equation 6.6 and where $\hbar$ is $5.3 \times 10^{12}\text{cm}^{-1}\text{s}$ [265].

To understand how the phonon modes decay it is necessary to measure the lifetime at a range of temperatures. The sample is varied using a temperature controlled stage with a liquid nitrogen pump attached which allowed measurements to be performed between 88 K and 573 K in 25 K intervals. The stage has a quartz window which isolates the sample chamber from the ambient atmosphere but still allows optical access for the laser. It has been shown that the most common path for a phonon at the Γ point to decay is into 2 phonons (3-phonon process) with the same energy but opposite wavevectors, following the relationship

$$\frac{\omega_0}{2} = \omega_1 = \omega_2, \qquad k_1 = -k_2, \tag{6.10}$$

where ω_0, is the frequency of the original phonon, ω_1, ω_2 are the frequencies of the phonons it decays into, and k_1, k_2 are the wavevectors of these phonons [270]. However in materials which have a phonon bandgap such as InN and GaN this is not always possible and as such assymmetric decays and a decay into 3 phonons (4-phonon process) are also observed [265, 271, 272]. The phonon dispersion curves and the corresponding density of states for $\beta - Ga_2O_3$ are shown in Figure 6.2. It can be seen that there is only a small gap at approximately 580 cm^{-1}, suggesting a symmetric decay will be the most prevalent.

As can be seen in Figure 6.3 (a), the phonon linewidth is temperature dependent, due to the fact that the phonon population is temperature dependent. Hart *et al.* used pertubation theory to show that for a symmetrical 3 phonon process the temperature dependence of the lifetime can be

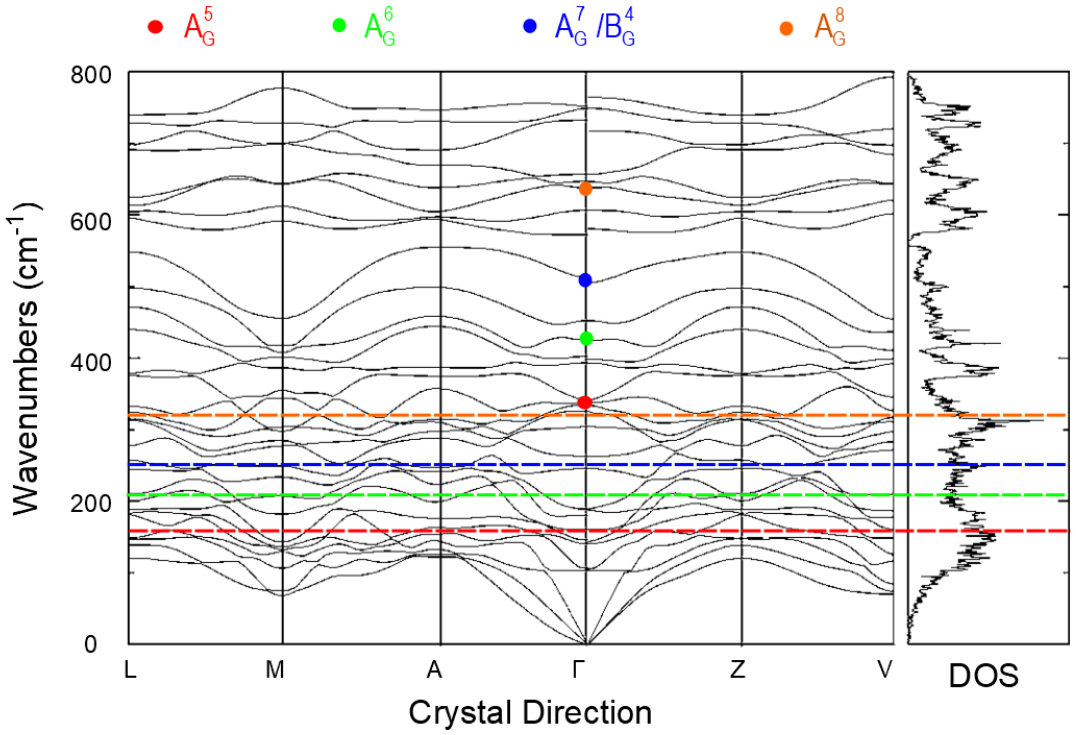


FIGURE 6.2. Phonon dispersion curves for $\beta - Ga_2O_3$ along high symmetry directions. Also shown is the Density Of States (DOS) which shows there is no large phonon bandgap. The DOS can be used to predict which phonon decay paths may be more or less likely. The phonon modes which have their decay paths determined are labelled as dots at the Γ point, and the phonon frequency which corresponds to a 3-phonon symmeterical decay is labelled as a dashed line. Image adapted from Liu *et al* [273]. Reprinted with permission from AIP Publishing.

fit by [274]

$$\tau_p(T) = \left(\Gamma_Q + 2n(T, \omega_0/2)\right)^{-1} \tag{6.11}$$

where Γ_Q is the line broadening due to impurities and defects, and $n(T,\omega)$ is the Bose-Einstein function

$$n(T,\omega) = \left(\exp(\hbar\omega/k_b T) - 1\right)^{-1}. \tag{6.12}$$

This was shown to fit well at low temperatures but it underestimated the scattering rate at higher temperatures. Therefore it was extended by Balkanski *et al.* to include a second decay path to 3 phonons of the same frequency

$$\tau_p(T) = \left(\Gamma_Q + A[1 + 2n(T, \omega_0/2)] + B[1 + 3n(T, \omega_0/3) + 3n^2(T, \omega_0/3)]\right)^{-1} \tag{6.13}$$

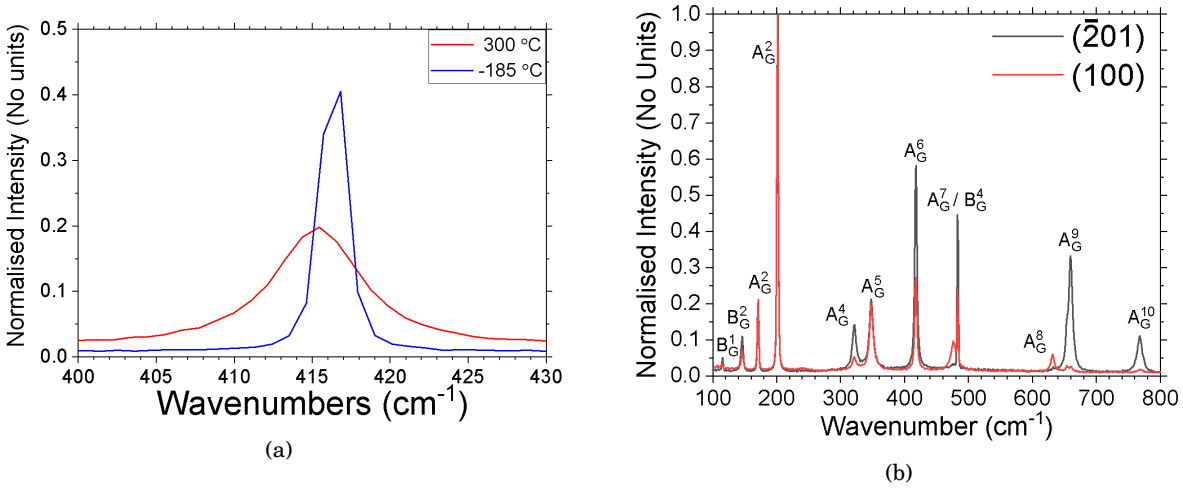


FIGURE 6.3. (a) The temperature dependence of the phonon linewidth is shown with the A_G^6 mode in the (100) crystal at 573 K and 98 K. (b) Raman spectra for the $\{\bar{2}01\}$ and $\{100\}$ crystals at room temperature. It can be seen that certain peaks, for example at 660 cm^{-1}, are visible in one sample but not the other.

where A weights the probability of a 3 phonon process, and B weights the probability of a 4 phonon process [265, 275].

6.1.2 Results and Discussion

An example of the Raman spectra for the (100) and $(\bar{2}01)$ crystals is shown in Figure 6.3 (b). Due to the Raman selection rules discussed in Section 3.1, Raman modes will scatter with different intensities depending on the crystal orientation with respect to the incident light. This makes measurements using two samples ideal, as it allows for a comparison of the mode lifetimes which are common to both samples, and also for a wider range of modes to be measured. Whilst the lifetimes of the modes should be similar in both samples, differences may occur due to differences in the crystal quality and carrier density which has been shown to decrease lifetimes in longitudinal modes in GaN [272]. Although both samples were nominally undoped, the carrier concentration was $5.5 \times 10^{17} cm^{-3}$ in the (100) sample and $3 \times 10^{17} cm^{-3}$ in the $(\bar{2}01)$ sample.

The measured phonon linewidths for the (100) and $(\bar{2}01)$ samples are shown in Figures 6.4 (a) and (b) respectively. As demonstrated in Figure 6.3 (a) the intensity of the Raman mode peak decreases as temperature increases meaning that not all of the peaks seen in Figure 6.3 (b) could

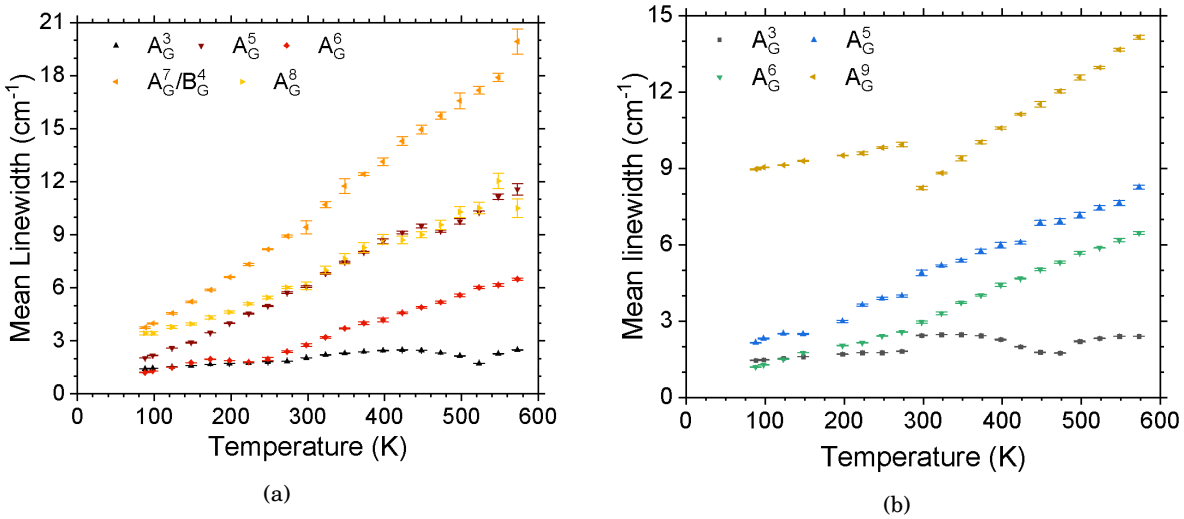
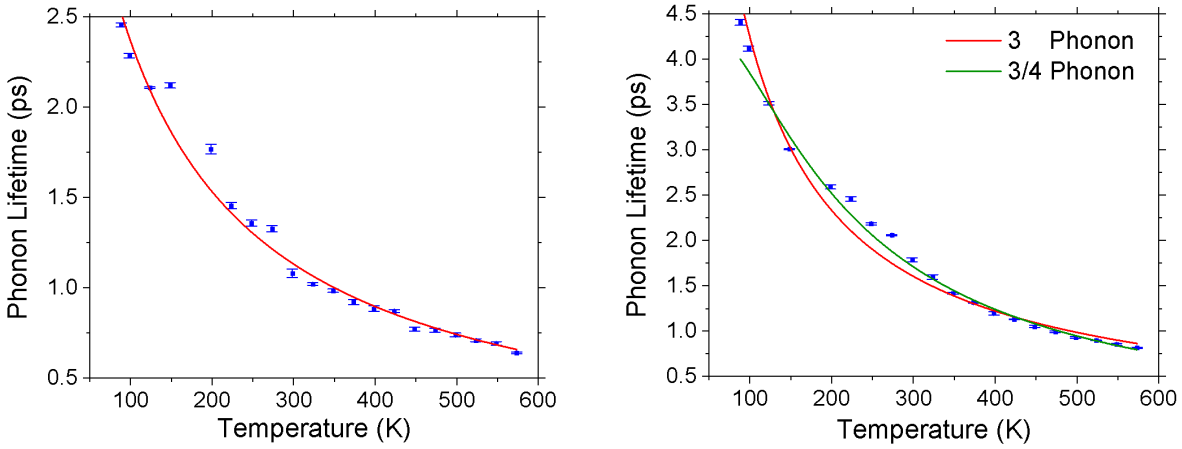


FIGURE 6.4. The measured phonon linewidths for the (100) (a) and $(\bar{2}01)$ (b) samples. Each data point is the mean of 5 repeat measurements. The error bars are the standard error on the mean calculated from these repeats.

be measured over the whole temperature range. In both samples the A_G^3 mode has very little temperature dependence. The broadest linewidth at all temperatures belongs to the A_G^7/B_G^4 mode, which implies this has the shortest lifetime. There is a discontinuity in the relationship between the A_G^9 mode linewidth with respect to temperature in the $(\bar{2}01)$ sample, which is likely to be a measurement artefact. As a result, the A_G^9 mode could not have its decay path determined.

The lifetimes and corresponding fits of the A_G^5 and A_G^6 modes in the $(\bar{2}01)$ sample are shown in Figure 6.5. Both show short lifetimes with room temperature values of approximately 1 ps and 1.5 ps for the A_G^5 and A_G^6 modes respectively. Whilst the A_G^5 mode can be fit by a 3 phonon process (i.e B = 0 in Equation 6.13), this is not the case for the A_G^6 mode which requires a 4 phonon process. The reason for this is not immediately clear, as looking at phonon density of states in Figure 6.2 shows there is no gap which would limit a 3 phonon process. The 3 phonon scattering factor A is 0.212 ± 0.006 THz whereas the 4 phonon scattering scattering factor B is 0.017 ± 0.002 THz, suggesting the 3 phonon process dominates. The crystal scattering factor Γ_Q was found to be 0.19 ± 0.01 THz for the A_G^5 mode, but was negligible in the A_G^6 mode. As the measurement was taken in the same location, the crystal properties should not differ. This could imply that the A_G^5 mode interacts more readily with its environment, although it is possible that fitting a 4



(a) A_G^5 (b) A_G^6

FIGURE 6.5. The phonon lifetimes as a function of temperature and the relevant fit, described by Equation 6.13. The A_G^5 mode can be fit by a 3 phonon process, however this is not the case for the A_G^6 mode which requires a 4 phonon process.

phonon process results in the fit becoming insensitive to the crystal scattering factor. Because of the lack of temperature dependence, the decay mechanism of the A_G^3 mode could not be fit in either sample.

The phonon lifetimes for the (100) oriented sample can be seen in Figure 6.6. In this sample the A_G^5, A_G^7/B_G^4, and A_G^9 modes could be measured and fitted with a decay process. Of these the A_G^5 and A_G^7/B_G^4 could be fit by 3 phonon processes, whereas the A_G^9 mode requires a combination of 3 and 4 phonon processes. For the A_G^9 mode, the 3 phonon process dominates again with A in Equation 6.13 being 0.61 ± 0.02 THz and B being 0.063 ± 0.008 THz. This mode also shows the weakest temperature dependence with its 573 K lifetime being 33% of its 88 K lifetime. In contrast, for the A_G^5 and A_G^7/B_G^4 modes the phonon lifetime at 573 K is 19% of the phonon lifetime at 88 K. The defect broadening Γ_Q is too small to be fitted for the A_G^9 mode but in the A_G^5 and A_G^7/B_G^4 modes it is 0.03 ± 0.01 THz and 0.15 ± 0.02 THz respectively. The large error (33% in the A_G^5 mode) suggests there is a lack of sensitivity to crystal scattering factor.

The room temperature lifetimes in these modes are similar to that for the $(\bar{2}01)$ oriented sample with values ranging between 0.5 ps and 2 ps. The A_G^5 mode is the only one which could be fit in both samples, decaying through 3 phonon processes in both samples. The room

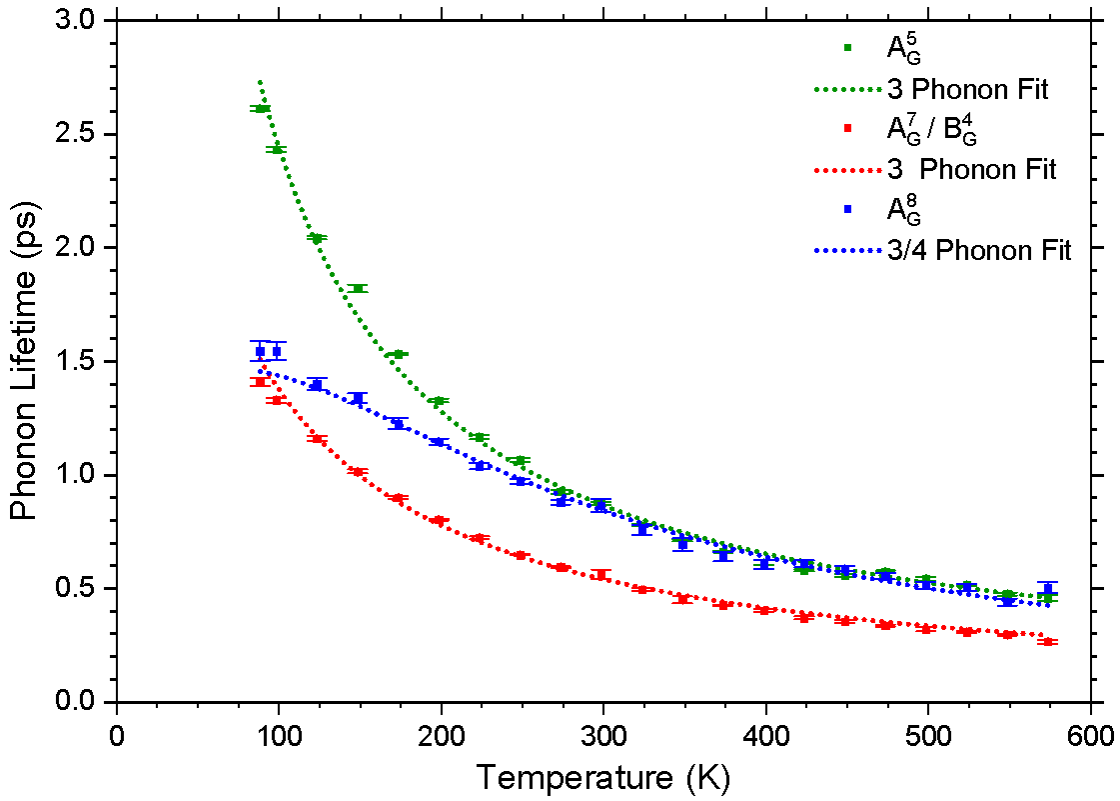


FIGURE 6.6. Phonon lifetimes versus temperature for the A_G^5, A_G^7/B_G^4, and A_G^9 modes in the (100) oriented sample. The A_G^8 mode is the only one that requires a combination of 3 and 4 phonon processes to be fit. This mode has a much lower temperature dependence than the others.

temperature lifetime is 0.9 ps in the (100) oriented sample and 1.1 ps in the $(\bar{2}01)$ oriented sample, suggesting it is consistent on both samples. These lifetimes are similar to those reported for other semiconductors in the literature, of which the shortest is for AlN at 0.1 ps and the longest is for Si at 15 ps. [261, 263–266]. Grann *et al.* suggest that the phonon lifetime is dependent on the elastic constants and the bond length in a material, as shorter bond lengths result in more mobile phonons which will result in greater scattering [266]. The bond length is 1.86 Å for AlN and 2.35 Å for Si. For $\beta - Ga_2O_3$ the bond lengths are between 1.83 and 2.07 Å, which correlates with the phonon lifetimes being closer to AlN than Si [110, 276, 277].

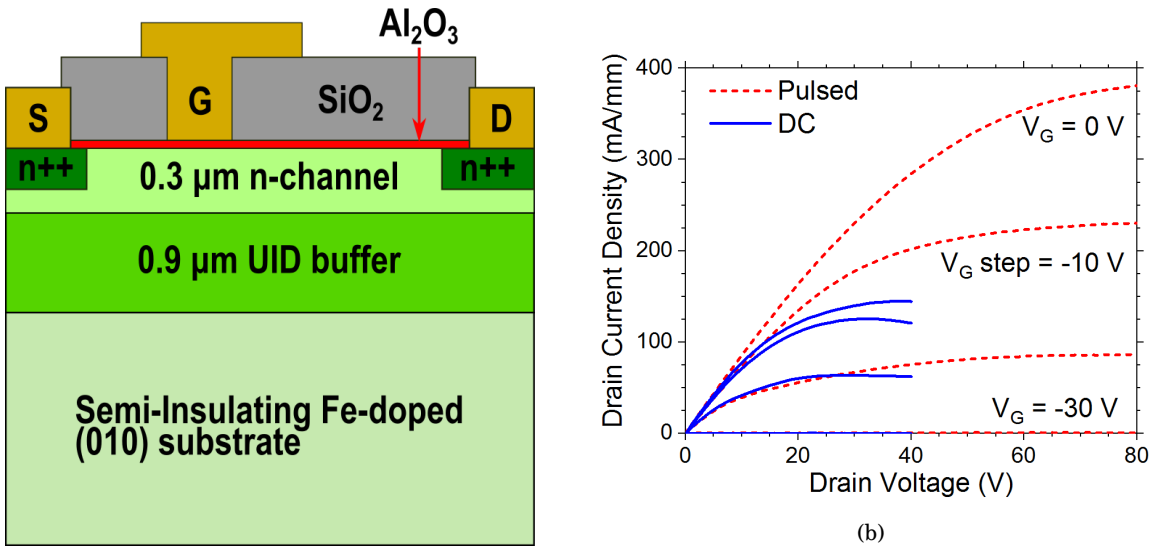


FIGURE 6.7. (a) Schematic diagram of a cross-section of a $\beta-Ga_2O_3$ MOSFET produced by Higashiwaki *et al.* [125]. (b) The IV characteristics of a device with W_G 200 μm and L_G 4 μm. Under DC testing the devices failed above V_D = 40 V. The pulsed operation used quiescent biases V_G = 0 V, V_D = 0 V.

6.2 Thermal Resistance of $\beta-Ga_2O_3$ MOSFETs

Devices were supplied by Higashiwaki *et al.* at the National institute of Information and Communication Technology (NICT) in Tokyo, Japan [129]. The MOSFETs, a schematic of which is shown in Figure 6.7 (a), are fabricated on Fe-doped semi-insulating (0 1 0) substrates grown using the Edge-defined Film-fed Growth (EFG) technique discussed in Section 2.3.2. The epitaxial device layers are grown via MBE. These are an unintentionally doped 0.9 μm thick buffer, and a 0.3 μm n-type channel doped by Si ion implantation which gives carrier concentrations of approximately 10^{19} cm^{-3} and sheet resistances as low as 1.5 mΩ.cm. Heavily doped regions underneath the drain and source contacts are formed to reduce the contact resistance [278]. A 20 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition. The whole device is then passivated with SiO_2.

The device tested had an L_G of 4 μm, a W_G of 200 μm, an L_{GD} of 25 μm, and an L_{GS} of 8 μm. The gate connected field plate is 2 μm long on the source side and 2.5 μm long on the drain side. The devices were first tested electrically by a colleague, Mr Manikant, with pulsed and DC IV curves as shown in Figure 6.7 (b). The reduced current density in DC operation could be

due to increased ON-resistance caused by Joule heating in the device. The difference between the DC and pulsed operation is substantial if compared with the results displayed in Section 4.3, for example, suggesting the devices have a large thermal resistance R_{Th}. This is expected because of the low thermal conductivity of $\beta - Ga_2O_3$, but must be authenticated by temperature measurements.

6.2.1 Method

The ultra-wide bandgap of $\beta - Ga_2O_3$ makes it transparent to most available laser sources meaning micro-Raman thermography would provide a depth average temperature measurement and as the device is on a native substrate the measurement would penetrate approximately 6 μm into the sample. The low thermal conductivity means there will be a large temperature gradient in the device buffer which, coupled with this broad measurement location, would result in a highly imprecise measurement.

Instead, nanoparticle assisted Raman thermography is used to measure the surface temperature of the device as described in Section 3.1.4. Again the particles were dispersed in methanol and dropcast onto the sample. In total, five nanoparticles were measured. The locations are shown in Figure 6.8 (a); one on the gate at the edge of the device active area, one on the gate at the centre of the device active area, and three at the centre of the device active area, spaced in the gate-drain access region. The nanoparticle at the centre of the device allows determination of the peak device temperature, and hence the device thermal resistance. Because of the low thermal conductivity of $\beta - Ga_2O_3$ a large thermal gradient along the gate is expected and the nanoparticle at the gate periphery allows for this gradient to be calculated. The measurements in the gate-drain access region allow a comparison to the thermal simulations of the device structure, and provide an understanding of the in plane heat-spreading in the device. This will impact the mean channel temperature which in turn impacts ON-resistance and device efficiency. The peak temperature is measured at drain voltages up to 50 V in 10 V steps, resulting in power dissipation up to 1.87 W/mm. The heat spreading is measured at drain voltages of 30 V and 50 V. A reference nanoparticle approximately 350 μm from the device centre was measured to provide the chip temperature.

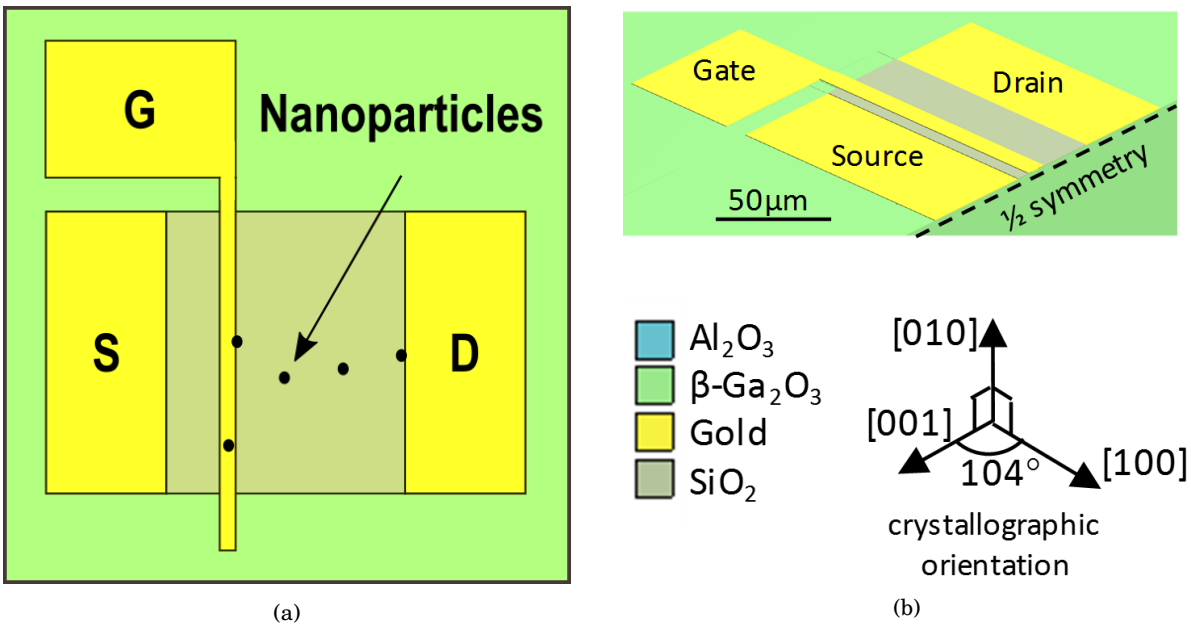


FIGURE 6.8. (a) Vertical view of the device measured, with approximate nanoparticle locations located. (b) Schematic diagram of the finite element model developed by a colleague, adapted from Pomeroy *et al.* [279].

The results are compared to a finite element simulation of the device structure which was developed by a colleague, Dr Pomeroy [279]. The model recreates one half of the device structure with an insulating boundary condition at the centre of the device replicating the other half of the device, as shown in Figure 6.8. The $\beta-Ga_2O_3$ has an anisotropic, temperature dependent thermal conductivity of $23.4 \times (300/T)^{1.27}$ W/m.K along the [0 1 0] orientation, $10.7 \times (300/T)^{1.21}$ W/m.K along the [1 0 0] orientation, and $13.7 \times (300/T)^{1.12}$ W/m.K along the [0 0 1] orientation [46]. The heat was deposited underneath the gate, rather than at the gate edge as is the case with GaN HEMTs. This is because, as discussed in Section 2.5, the channel resistance is higher in these devices since there is no 2DEG which results in lower channel mobility, a higher channel resistance, and a less localised electric field. The sample was mounted on a heat sink and the thermal resistance between the heat sink and the sample was adjusted such that the temperature 350 μm from the device matched the measurement on the reference nanoparticle.

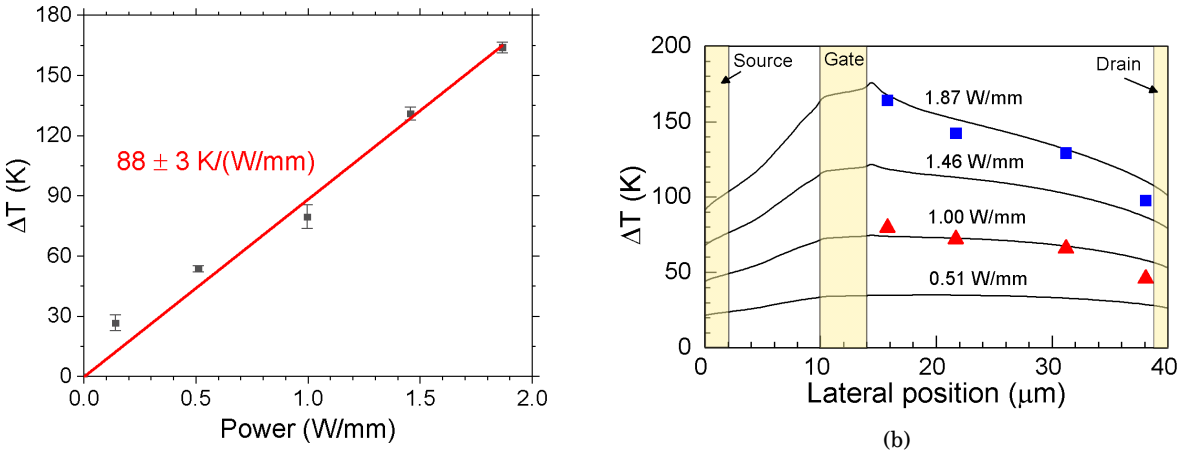


FIGURE 6.9. (a) Temperature increase with respect to the chip temperature measured at the central nanoparticle on the gate edge. A linear fit forced through the origin is used to determine the thermal resistance at 88 ± 3 K/(W/mm) over this power dissipation range. (b) Comparison between the measurement in the gate-drain access region and the simulation. Image adapted from Pomeroy *et al.* [279].

6.2.2 Results and Discussion

The thermal resistance over this power dissipation range is determined from the data shown in Figure 6.9 (a). The temperature shown is the tempertature measured on the central nanoparticle minus the temperature measured on the reference nanoparticle, such that only the impact of the $\beta - Ga_2O_3$ wafer is considered. As the nanoparticle is located on the gate, the measured temperature should be similar to the peak channel temperature. Based on this assumption, the thermal resistance is determined by finding the gradient of a linear fit to the data, forced through the origin. Over the power range studied it is found that the thermal resistance is 88 ± 3 K/(W/mm), almost 10 times larger than the state-of-the-art GaN-on-Diamond devices measured in Section 4.3, and 4.6 times higher than the SLCFETs measured in Section 5.2 which utilised an AlGaN buffer.

At the maximum power dissipation of 1.87 W/mm, the temperature of the nanoparticle on the gate, 50 μm from the centre of the active area, is 20 K lower than the temperature of the central nanoparticle. This large temperature gradient is in contrast to the simulations performed in Section 5.2 where the temperature is close to constant along the gate outside of the final 5 μm.

The gate length in these $\beta-Ga_2O_3$ devices is almost four times longer, which likely accounts for some of the effect seen, however the low in-plane thermal conductivity is also likely to be a cause. Figure 6.9 (b) shows that the temperature at the drain edge is 59% of the temperature at the gate edge. In contrast, the GaN-on-Diamond devices studied in Section 4.3 have a temperature at the drain edge which is less than 10% of the temperature at the gate edge. The ON-resistance is impacted by the temperature at all points in the channel, and so temperatures which remain high between the source and drain will have a greater negative impact than if the high temperature was just localised at the gate edge. This suggests that $\beta-Ga_2O_3$ devices will have greater thermal inefficiencies than GaN HEMTs even if the device is de-rated such that the the peak temperature is similar.

6.3 Modelling of ultrawide bandgap devices

6.3.1 Method

The large thermal resistances reported in Section 6.2 highlight the importance of thermal management techniques if devices fabricated in low thermal conductivity UWBG materials are to be operated at their maximum capacity. In this section finite element simulations are used to test possible device designs. The device will not be specifically a $\beta-Ga_2O_3$ or AlGaN device, instead a generic buffer material with a thermal conductivity of 30 W/m.K is used. A single device configuration will be used, shown in Figure 6.10. The device has an L_G of 1 μm, a W_G = 100 μm, an L_{GD} = 10 μm and an L_{GS} = 2 μm. The heat is deposited in a 1.5 μm area below the gate extending towards the drain, because, as described in Section 2.5, the lower mobility in UWBG devices leads to a more resistive channel and a less localised electric field. The TBR_{eff} between the buffer and the substrate is constant at 20 m^2K/GW in all cases examined.

The use of diamond in three passive cooling designs is investigated. First is polycrystalline diamond used as a substrate, the second is nanocrystalline diamond used as a passivation layer, and the third is single crystal diamond used as a flip-chip mount. The polycrystalline diamond substrate arrangement will be similar to the material studied in Section 4.3 with the UWBG buffer mounted on the diamond substrate. The diamond substrate will be made up of five layers

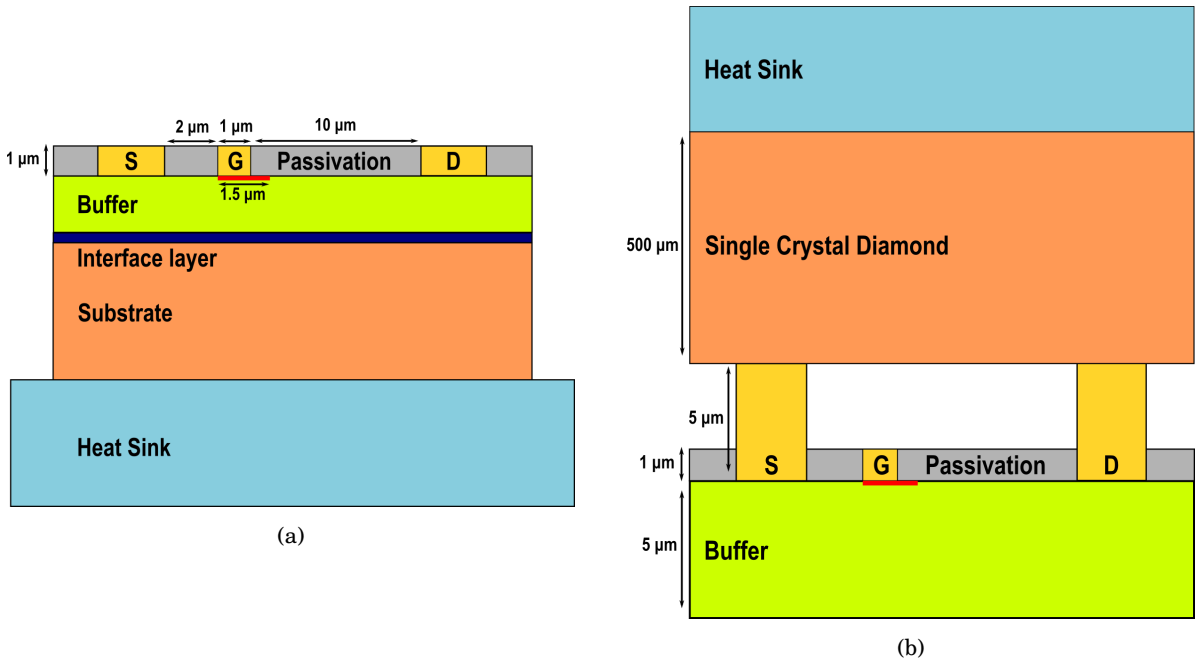


FIGURE 6.10. (a) Schematic diagram of the finite element model produced for the testing of near-junction thermal management in UWBG device systems. The heat is deposited in the red area below the gate. The temperature at the back of the heat sink is kept constant at room temperature. There is a constant thermal resistance between the heat sink and wafer representing 25 μm of solder. (b) Schematic diagram of the flip-chip mounted UWBG device. The temperature at the top is fixed at room temperature.

to represent how the crystal structure evolves from the growth face due to CVD polycrystalline diamond's columnar growth structure, and this growth structure was discussed in more detail in Section 2.4.3. The first layer is 1 μm thick, the second is 4 μm thick, the third 10 μm,thick, the fourth 20 μm thick, and the last 40 μm thick. Due to the columnar growth structure, the through-plane thermal conductivity of diamond is higher than the in-plane thermal conductivity and this is accounted for in the model, as is the temperature dependence of the thermal conductivity, with the data taken from References [173, 174]. The UWBG material-on-diamond system will be compared to GaN-on-diamond and UWBG material-on-SiC systems. The importance of buffer thickness, investigated for GaN-on-diamond systems in Section 4.3, will also be investigated here.

Devices are typically passivated with an amorphous material such as silicon nitride which will

have a low thermal conductivity of approximately 1 W/m.K and hence the passivation layers have a negligible impact on the heat spreading. It was shown in Section 5.2 that having a high thermal conductivity material adjacent to the channel can help reduce peak temperatures in devices, and diamond passivation layers have been shown to reduce peak temperatures in GaN HEMTs by 20% at 10 W/mm [280]. However it was found that stress caused by the diamond growth impacted the 2DEG. As discussed in Section 2.2.4, GaN is a piezoelectric material and the 2DEG forms at heterostructures because of stress caused by an AlGaN/GaN interface. The combination of the elevated diamond growth temperature, the difference in coefficent of thermal expansion between the diamond and the buffer, and the high stiffness of diamond results in additional, inhomogenous stress being imparted on the channel. This can degrade the device electrical performance as the heterostructure is optimised to give the maximum carrier concentation and mobility. Any additional stress will be an issue in AlGaN HEMTs which rely on a similar heterostructure to form a 2DEG, but should not be a problem in the case of the $\beta - Ga_2O_3$ MOSFETs, where the carriers are introduced by doping the buffer. The thickness of the passivation layer will be kept constant at 1 μm, but its thermal conductivity will be varied between 20 and 200 W/m.K to assess the impact of diamond quality on heat spreading. Since the nanocrystalline diamond is grown on the device, low temperatures must be used to protect the device which leads to renucleation and graphitic carbon formation, lowering the thermal conductivity [174]. It is also worth noting that as nanocrystalline diamond is not commonly used for passivation layers it is not known whether it is effective at preventing surface traps and surface conduction through the graphitic carbon at grain boundaries. In this instance it is assumed that there is no thermal barrier between the diamond and the buffer, although this would not be the case if a dielectric interface layer is required to suppress parasitic electrical effects.

Flip chip mounting of GaN HEMTs was performed by Das *et al.* who found that as long as the device flip chip mount is bonded directly to the source and drain contacts, this configuration can allow the devices to be operated at higher powers [281]. There are two major advantages of flip-chip mounting when compared to the other configurations discussed above. The first is that, as it is a packaging solution, changes to existing device production techniques are not required. This means that devices can continue to be developed for the desired electrical characteristics and

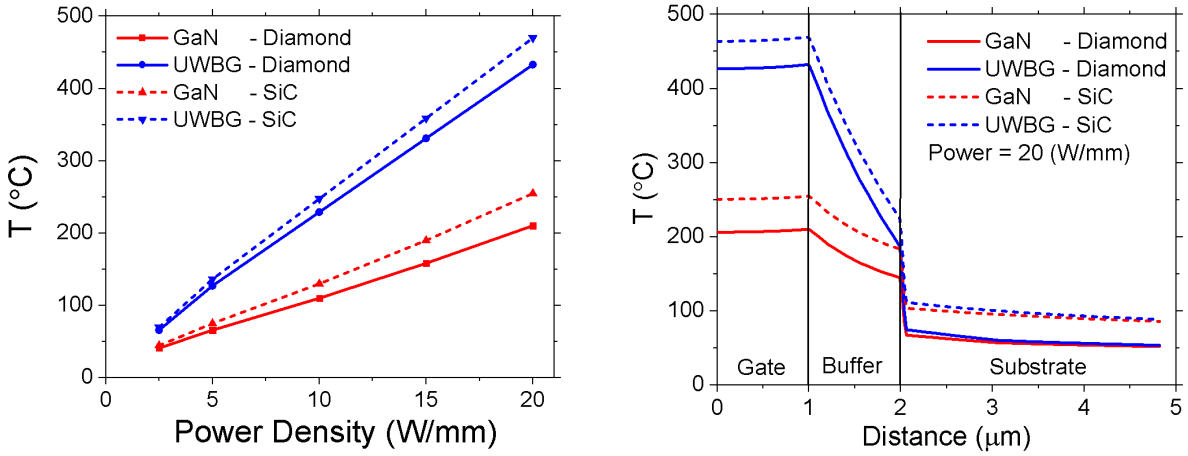
costs, with the thermal management coming later. Secondly, the diamond used is not restricted in its growth conditions as it is fabricated away from the rest of the device. Hence it is possible to use single crystal diamond or high quality polycrystalline diamond which has had its growth face polished away, both of which will have thermal conductivities close to or above 2000 W/m.K. A schematic image of how the flip-chip mounted UWBG device is designed is shown in Figure 6.10 (b). The substrate has been removed and the temperature at the top of the flip-chip mount is set to room temperature, meaning heat will flow from the device through the contacts to the diamond. The diamond itself has a constant thermal conductivity of 2000 W/m.K, representing single crystal material.

6.3.2 Results and Discussion

Figure 6.11 shows the peak temperatures in the simulated device for four separate designs: GaN-on-SiC; GaN-on-Diamond; UWBG material-on-SiC; and UWBG material-on-Diamond. For these simulations the TBR_{eff} is kept constant at 20 m^2K/GW. The UWBG buffers have a significantly higher thermal resistance than the GaN equivalent for both non-native substrates. The improvement from SiC to diamond is less pronounced in the UWBG devices with an 8% lower peak temperature at 20 W/mm compared to 20% for the GaN devices. This is because the low thermal conductivity buffer acts as a bottle neck to heat flow and limits the impact that the substrate can have. However, irrespective of buffer material, the temperature in the substrate is lower when it is made of diamond, as opposed to SiC. This makes heat extraction from the substrate easier, which makes designing effective packaging easier.

If the buffer is the main cause of thermal resistance, one solution would be to remove as much buffer material as possible. This is not possible with a SiC substrate as its lower bandgap of 3.2 eV would reduce the breakdown voltage of the device. However as diamond has a bandgap of 5.5 eV this is not an issue for diamond substrates and, as shown in Section 4.3, moving the substrate within 350 nm of the channel does not inhibit the electrical performance of the device.

Figure 6.12 (a) shows how the peak temperature increases steeply as the buffer thickness increases and then tends towards a maximum temperature which would represent the limit where the UWBG device is on a native substrate. Figure 6.12 (b) shows how the depth profile

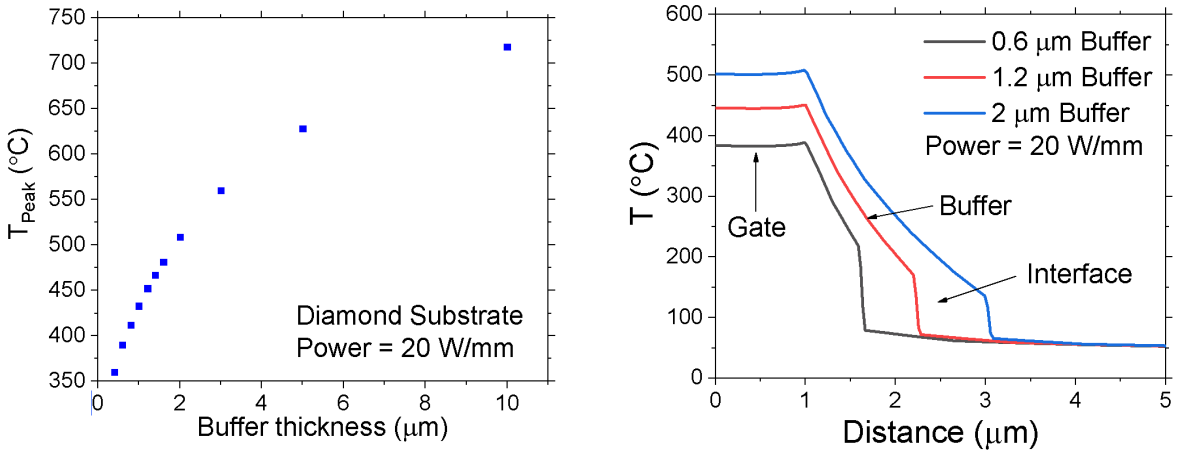


(a) (b)

FIGURE 6.11. (a) Peak temperatures in devices with a 1 μm thick buffer and a TBR_{eff} of 20 m^2K/GW. (b) The temperature distribution through the centre of the device at 20 W/mm power dissipation. This highlights each layers contribution to the temperature increase.

of the temperature varies with buffer thickness. It can be seen that the temperature increase over the buffer increases with thickness. However, there is a countering effect as well, where the temperature increase at the interface is inversely proportional to the buffer thickness. This is because, as the interface moves closer to the channel, the heat flux across it is larger, and hence any thermal resistance is amplified. Therefore, for thinner buffers to be an effective means of thermal management in UWBG systems the TBR_{eff} must be optimised so as not to restrict heat flow.

Figure 6.13 (a) shows the peak temperature in a device on a diamond substrate when the thermal conductivity of the passivation layer is varied from 1 W/m.K, through to 200 W/m.K, representing amorphous silicon nitride and nanocrystalline diamond. The peak temperature follows an exponential-like decay with respect to increasing thermal conductivity in the passivation layer. This means that introducing even poor quality diamond can drastically reduce the peak temperatures seen; a 32% reduction occurs for a 40 W/m.K thermal conductivity compared to 1 W/m.K. However this exponential-like behaviour also means that there are diminishing returns as the quality of the diamond is improved. Increasing the nanocrystalline diamond from 100 W/m.K to 200 W/m.K lowers the peak temperature by 19% which, whilst significant, is lower



(a) (b)

FIGURE 6.12. (a) Peak temperature in the simulated device at a range of buffer thicknesses and a power dissipation of 20 W/mm. There is a a large temperature increase as the buffer thickness is increased due the low thermal conductivity of UWBG materials. It tends to a limit where the whole wafer is made of UWBG material. (b) The temperature profile through the depth of the device at its centre. When the buffer is thinned the temperature increase over the interface increases, despite the constant TBR_{eff}.

than the adjustment from 1 W/m.K to 40 W/m.K. The total decrease in peak temperature when the thermal conductivity is increased from 1 W/m.K to 200 W/m.K is 58%. This is much larger than the 8% achieved by the introduction of a diamond substrate which is likely to be due to the fact that for the passivation layers to aid thermal management, the heat does not have to spread through the low thermal conductivity buffer first.

Finally the flip-chip design is considered. The contacts are 100 μm long and as the gate width is 100 μm, the contact area of each contact pad is 1000 μm^2. At 20 W/mm the peak temperature in a flip chip device is 744°C, which is 26° higher than a device with a 10 μm buffer and a diamond substrate shown in Figure 6.12. The thermal resistance is higher in the flip-chip scenario as the amount of UWBG material the heat must flow through is larger. This results in the higher temperature and limits the influence of the single crystal plate. However this can be partially mitigated by the use of diamond passivation layers in combination with the flip-chip mount although a 200 W/m.K passivation layer leads to a peak temperature of 245°C, which is still higher than temperatures calculated in Figure 6.13.

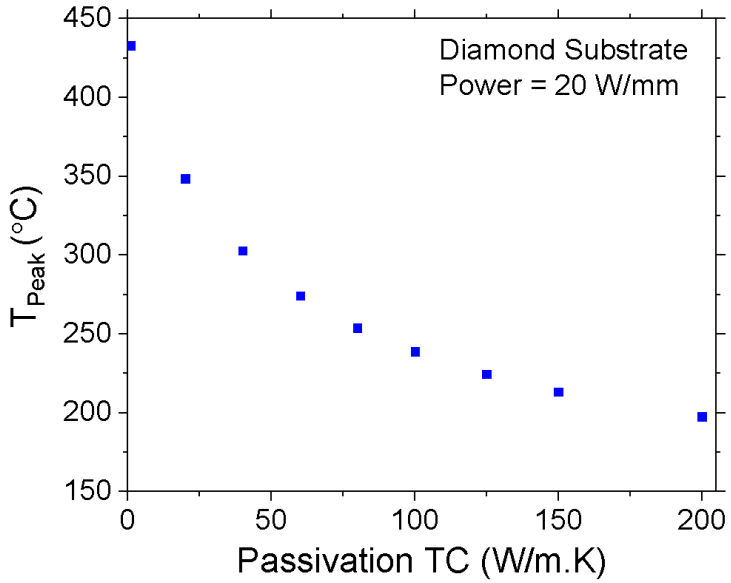


FIGURE 6.13. Peak temperatures in a simulated device where the thermal conductivity of the passivation layers has been adjusted to represent different qualities of nanocrystalline diamond. The peak temperature drops as the thermal conductivity initially increases, but the impact is lessened as it continues to increase.

6.4 Conclusions

As UWBG materials look to satisfy ever increasing demands for higher power, higher frequency operation devices, this section studied the thermal challenges associated with low thermal conductivity materials such as AlGaN and $\beta - Ga_2O_3$, and how optimal device designs may differ in these materials when compared to the current high performance electronic materials.

The lifetime of phonons in $\beta - Ga_2O_3$ crystals was studied by Raman spectroscopy, utilising the inversely proportional relationship between the linewidth of the Raman mode and the phonon lifetime. The phonon lifetime limits how quickly hot carriers can relax, and as such play an important role in device reliability. Four Raman modes (A_G^5, A_G^6, A_G^7/B_G^4, and A_G^8) were studied, with the longest room temperature lifetime of 1.8 ps belonging to the A_G^6 mode and the shortest room temperature of 0.5 ps belonging to the A_G^7/B_G^4 mode. By studying the temperature dependence of the lifetimes it is possible to assess the decay mechanism of the phonons. It was found that the A_G^5 and A_G^7/B_G^4 modes decay through a 3 phonon process to 2 symmetric phonons, whereas the A_G^6, and A_G^8 modes decay through a combination of this 3 phonon process and a 4

phonon process to 3 phonons of equal frequency. The lifetimes calculated are similar to those reported for other compound semiconductors and follow the trend suggested by Grann *et al.* that lifetime is proportional to bond length [266].

The thermal resistance of devices fabricated from $\beta - Ga_2O_3$ was found through nanoparticle assisted Raman thermography measurements. IV characteristics had shown substantially higher currents when the device was operated in pulsed operation compared to DC operation, suggesting that Joule heating could be causing increases in resistance. This was confirmed by the Raman measurements which found the thermal resistance to be 88 K/(W/mm). The measurements also showed a large temperature gradient along the gate and low temperature gradients in the gate drain access regions which can prove detrimental to device performance through increasing ON-resistance. This implies the $\beta - Ga_2O_3$ devices will need near-junction thermal management designs to allow them to operate at maximum performance.

Possible designs for near junction thermal management were considered through finite element simulations. The simulation used a generic low thermal conductivity buffer and a typical device design to test the use of diamond as a substrate, as a passivation layer, and as a flip-chip mount. It was found that diamond substrates are not as effective as in GaN systems as the low thermal conductivity buffer provides a bottle neck to heat flow before it reaches the substrate. However diamond passivation layers appeared to be more effective, spreading the initial hot spot over a larger area to reduce the peak temperature. The flip-chip mount proved less successful than both alternatives as the heat must travel further through the buffer until it reaches the primary heat spreading element.

CHAPTER 7

SUMMARY

Optimising the heat flow in high performance wide and ultra-wide band gap electronic devices is necessary to ensure reliability and to increase the device performance. The activation of failure modes in devices is more probable at higher temperatures, and efficiency is reduced when elevated temperatures cause ON-resistance increases and current collapse. As a result, wide and ultra-wide bandgap devices are often operated below their peak performance to increase their lifetime. This work studied the latest device structures to find the designs which give the optimum heat flow, such that wide and ultra-wide bandgap devices can be utilised more effectively in applications such as LIDAR, power switching, and wide bandwidth communications.

In semiconductors, phonons are the primary form of heat transport and the thermal conductivity is proportional to the phonon mean free path. As a result, at room temperature and above, the thermal conductivity is limited either by umklapp scattering or by crystal defects such as dopants, dislocations, and grain boundaries, if the density is high enough. Whilst the umklapp scattering rate is an inherent material property, it is possible to improve the thermal conductivity of a material by improving its quality, such that there are fewer crystal defects.

Gallium nitride is a wide bandgap (3.4 eV) material which is already being used for high performance RF and power applications. The AlGaN/GaN heterostructure used in high electron

mobility transistors results in a two dimensional electron gas formation. This two dimensional electron gas has higher mobilities and carrier concentrations than is achievable in the bulk, and is key to GaN being used for RF applications as it allows high frequency operation. However, the performance of GaN high electron mobility transistors is limited by the self-heating that arises from high voltage operation.

GaN is typically grown onto non-native substrates as the growth of bulk GaN is costly. These substrates influence the device thermal resistance, with silicon being less expensive, but lower in thermal conductivity than SiC and diamond. Diamond is the ideal choice for a substrate as it has a 5.5 eV bandgap and the highest known bulk conductivity at over 3000 W/m.K in single crystal, isotopically pure material. Issues with cost of production and integration with semiconductors means that single crystal diamond is rarely used in heat spreading. Instead it is much more common to use polycrystalline diamond, where the grain boundaries and defects present mean that the thermal conductivity is significantly reduced to around 1500 W/m.K. In spite of this, polycrystalline diamond is still currently the best substrate for GaN devices. For GaN-on-diamond devices to become common place it is necessary to study their integration such that they can be utilised effectively. A major obstacle is the GaN-on-diamond interface, which can cause thermal bottlenecks that reduce the heat-spreading impact of the diamond. This interface consists of an amorphous interface layer and the diamond nucleation layer. The amorphous layer is necessary to protect the GaN from the diamond growth environment and aid adhesion, whilst the diamond nucleation layer is a necessary part of the diamond growth process. However both have low thermal conductivities which inhibit heat flow.

GaN-on-diamond wafers were studied by transient thermoreflectance, which is a non-destructive, non-contact technique. A pulsed UV laser is used to heat the sample for 9 ns, and the resulting temperature increase and decay induce a change in the reflectance of the sample surface. This reflectance change is monitored using a continuous wave 532 nm laser. The rate of temperature decay is dependent on the material properties of the wafer being studied, and as such it can be used to determine the effective thermal boundary resistance between the GaN and the diamond. It was used to show that the Element Six growth process of attaching a GaN wafer to a handle wafer, growing the diamond, and then removing the handle wafer, is capable of producing material

with a low thermal boundary resistance (≈ 14 W/m.K), which is homogeneous over a four inch wafer.

To further the understanding of the effective thermal boundary resistance, it was attempted to isolate the impact of the diamond nucleation layer thermal conductivity. For this, thin suspended diamond films were prepared with heaters at their centre. The temperature of the heater was measured at various power dissipations using nanoparticle assisted Raman thermography. By depositing nanoparticles on the sample surface, they can be used as nano-thermometers which are not impacted by the thermo-mechanical stress of the films below them, meaning the measurement is quicker, and more precise. The thermal conductivity of the diamond film was then determined by plotting the heater temperature against the power dissipation. The films studied in this work varied in seed size and growth power. Larger seeds were found to give a higher thermal conductivity, as would be expected as larger seeds should give a lower density of grain boundaries. However, the transient thermoreflectance study found that larger seeds gave worse effective thermal boundary resistances, as larger seeds resulted in pinhole formation and cracks at the GaN-diamond interface, suggesting there is an optimal seed size which gives a balance between thermal conductivity and interface quality.

Two device sets fabricated in GaN-on-diamond were studied using photoluminescence and nanoparticle assisted Raman thermography. The purpose of the study was to determine the electrical and thermal benefit of reducing the thickness of the GaN buffer and the interface layer. The thinner sample had a buffer thickness of 354 nm and an interface layer thickness of 17 nm, whilst the thicker sample had a buffer thickness of 700 nm and an interface layer thickness of 35 nm. Photoluminescence can be used to measure temperature as the bandgap is temperature dependent. It was applied as an alternative to micro-Raman thermography as the diamond substrate gave a large luminescence background which obscured the Raman signal from the buffer, which was weak because of the thin layers used. Photoluminescence does not have this problem as the probe laser is absorbed at the sample surface. It does however, have the added difficulty that it induces an additional current in the sample which can increase the heating.

Finite element simulations were used to determine the effective thermal boundary resistance of the thinner sample as 12.6 ± 0.4 m^2K/W and of the thicker sample as 20 ± 3 m^2K/W. The

wafers had similar thermal resistances of 9 ± 1 K/(W/mm) for the thinner sample and 10.0 ± 0.5 K/(W/mm) for the thicker sample. Finite element simulations were also used to show that the optimal buffer thickness is a function of the effective thermal boundary resistance between the GaN and the diamond, and that as effective thermal boundary resistance decreases, thinner buffers become preferable. The data showed that the thinner sample had half the temperature induced current drop when compared to the thicker sample. This was because there is less in-plane heat spreading in the thinner sample, which results in a lower mean channel temperature, despite the fact that the peak temperature is similar. Therefore the thin buffer is preferable if the effective thermal boundary resistance is low enough to prevent the total device thermal resistance being too large.

Beyond GaN, research has begun to focus on materials which may allow higher voltage operation; so called ultra-wide bandgap materials. One of these is AlGaN, where aluminium alloying of GaN is used to enhance the bandgap and critical field such that the device can operate at higher voltages. Alternatively, $\beta-Ga_2O_3$ is a very interesting competitor since it has a bandgap of 4.9 eV and can be fabricated from cost-effective melt-growth techniques. In this work, the thermal properties of both AlGaN and $\beta-Ga_2O_3$ devices have been studied. This is of particular importance in ultra-wide bandgap devices, as the higher voltage operation results in an even higher power density than in GaN devices. The thermal management problem is compounded by the fact that both AlGaN and $\beta-Ga_2O_3$ have significantly lower thermal conductivities than the other semiconductors discussed in this work. The thermal conductivity of AlGaN is dependent on the aluminium alloying concentration, but at concentrations greater than 10%, the thermal conductivity is approximately 30 W/m.K. This is larger than the thermal conductivity of $\beta-Ga_2O_3$, which is anisotropic but has a maximum of 27 W/m.K.

The superlattice castellated FET is a novel design of GaN based RF switch which has a 3D gate and an AlGaN buffer. Temperature measurements were performed using a combination of micro-Raman thermography and gate resistance thermometry. The channel of the devices is an AlGaN/GaN superlattice which results in a stack of two dimensional electron gases. This reduces the device ON resistance, but also increases the threshold voltage. Therefore the channel is etched periodically to form crenellations, and a three-dimensional gate is used which pinches

of the channel from the sides as well as from above. As a consequence, the heat is localised inside the channel crenellations, but this was not found to inhibit the heat flow as the total device thermal resistance was found to be 19.1 ± 0.7 K/(W/mm), which is similar to GaN-on-SiC devices. Finite element simulations showed that the gate acts like a heat pipe, aiding heat flow into the buffer. Without the high thermal conductivity gate metal, the device thermal resistance would increase to 23.5 K/(W/mm). Potential improvements to the device structure were explored using the finite element simulations, with the most impact coming from enhancing the heat piping effect by reducing the thickness of the gate dielectric, resulting in a predicted device thermal resistance of 17.2 K/(W/mm).

As devices in $\beta-Ga_2O_3$ are relatively novel, the fundamental material properties are relatively unexplored. The room temperature phonon lifetimes were found to be approximately 2 ps, which is similar to that of other compound semiconductors. The temperature dependence of the phonon lifetime was used to show that, most commonly, the modes decayed through a symmetrical Klemens process.

$\beta - Ga_2O_3$ devices were studied using nanoparticle assisted Raman thermography. This showed that the thermal resistance of the devices was 88 ± 3 K/(W/mm). This high thermal resistance is caused by the low thermal conductivity of the $\beta - Ga_2O_3$, and manifested itself by causing failure in devices operated at DC drain voltages of 40 V. This is a challenge shared by devices fabricated in both $\beta - Ga_2O_3$ and AlGaN, as both can have thermal conductivities of less than 30 W/m.K. Finite element simulations were used to assess how thermal performance may be enhanced in these structures in the future, with a focus on the utilisation of diamond. It was found that using diamond as a substrate, a very effective technique for heat spreading in GaN, would be less useful in the case of low thermal conductivity ultra-wide bandgap devices. This is due to the buffer acting as a thermal bottleneck. Thinning the buffer was effective in reducing the peak device temperature, but this requires a low thermal boundary resistance between the buffer and the substrate. The most effective heat spreading came from the use of diamond passivation layers, with even poor quality diamond having a significant impact on heat spreading. Altogether, devices fabricated from these ultra-wide bandgap devices will likely require a combination of a thin buffer, a low thermal boundary resistance, a diamond substrate and a diamond passivation

layer if there are to be utilised effectively.

7.1 Future Work

The most effective design of GaN-on-diamond wafer will ultimately be determined by the best achievable thermal boundary resistance between the GaN and the diamond. As demonstrated in this work, if the effective thermal boundary resistance becomes sufficiently low (≈ 5 m^{2}K/GW), ultra-thin buffer devices will offer the best performance from both a thermal and electrical perspective. Therefore a significant focus should be on improving the effective thermal boundary resistance in GaN-on-diamond systems.

Whilst the fundamental phonon scattering between dissimilar materials cannot be altered, the interface layer and the diamond nucleation layer can be optimised to give the most efficient heat transport. With respect to the diamond nucleation layer, a more detailed study of the optimal seed size should be carried out. A variety of GaN-on-diamond samples with seed sizes varying from 10 nm to 500 nm should be fabricated with membranes created. This would allow for the measurement of the thermal conductivity of the diamond film and the measurement of the effective thermal boundary resistance on the same sample, allowing a correlation to be found. The results could then be correlated with transmission electron micrographs of the microstructure.

For the interface layer, amorphous silicon nitride is currently the most commonly used material. It is essential for the interface layer to contain a carbide forming element, such as silicon, to provide good adhesion and thermal transport. However, the thermal transport across an amorphous material is limited by the lack of long range order. Therefore, crystalline materials should be explored for the interface layer. A suitable option to be explored would be AlGaN or AlN, as the lattice mismatch can be low and aluminium carbide forms readily. Sample sets with varying thickness and aluminium concentration could be fabricated. Then the effective thermal boundary resistance and the mechanical adhesion of the interface could be measured to find the optimal conditions.

For GaN-on-diamond devices to become widespread industrially, fabrication costs would ideally be lower. A key part of this will be the ability to grow GaN-on-diamond wafers larger

than four inches in diameter. The challenge is ensuring the diamond growth is homogeneous across the wafer. The shape of the plasma in microwave plasma enhanced chemical vapour deposition is dependent on the reactor design, and if it is not consistent over the wafer area, it will result in areas of slower, or, lower quality, diamond growth. Therefore it will be important to use the autonomous transient thermoreflectance experimental setup to map the effective thermal boundary across the wafer.

This work showed that the gate design does not significantly inhibit the heat flow in superlattice castellated FETs. Now that the thermal characterisation has been established, the next step in their development is to test some of the suggested improvements. The two adjustments which gave the best predicted improvement, the switch to a GaN buffer and the thinning of the gate dielectric, will both impact the electrical performance of the devices. A detailed electrical characterisation of the devices should be carried out in addition to a thermal characterisation to ensure that they perform satisfactorily. If the suggested adjustments prove detrimental, replacing the SiC substrate with a diamond substrate should provide a thermal benefit without impacting the electrical performance of the device.

The field of ultra-wide bandgap devices is less mature than that of wide bandgap devices. Many of the lessons learnt about the integration of diamond with wide bandgap semiconductors can be applied to ultra-wide bandgap devices. However, this work showed that the challenges faced in AlGaN and $\beta-Ga_2O_3$ devices will differ in some ways due to the low thermal conductivity of these materials. Therefore devices should be explored with diamond passivation layers implemented. In the case of GaN, this gave moderate improvements in thermal resistance but was detrimental to the two dimensional electron gas because of stress imparted on the GaN by the passivation layers. This is likely to be the case in AlGaN high electron mobility transistors since they also use a two dimensional electron gas. However as the carrier concentration in $\beta-Ga_2O_3$ MOSFETs is not dependent on strain, diamond passivation layers should prove more successful. This could be validated experimentally using nanoparticle assisted Raman thermography.

All of the experiment and simulations in this work have been performed with the devices in a steady state. For the ultra-wide bandgap materials which could be used in power switching, it is necessary to consider the thermal time constant of a device; a measure of the time taken

for a device to return to ambient temperature after it has been heated. This can be predicted using finite element analysis and measured experimentally using time resolved micro-Raman thermography. This is possible in devices which are on a non-native substrate, but for the $\beta - Ga_2O_3$ devices studied in this work it would be necessary to use nanoparticle assisted Raman thermography. Time-resolved nanoparticle assisted Raman thermography has not been performed previously and is likely to be a challenging endeavour as the measurements must have a short acquisition time (≈ 10 ns) and the nanoparticles give weak Raman signals because of their small size. However the data gathered would provide information on the possible operating conditions of the devices.

APPENDIX A

A.1 List of Publications

- C. Middleton, H. Chandrasekar, M. Singh, J. W. Pomeroy, M. J. Uren, D. Francis, M. Kuball, *Impact of thinning the GaN buffer and interface layer on thermal and electrical performance in GaN-on-diamond electronic devices*, Applied Physics Express, 2019 **12** (2) 024003.

- C. Middleton, S. Dalcanale, J. W. Pomeroy, M. J. Uren, J. Chang, J. Parke, I. Wathuthanthri, K. Nagamatsu, S. Saluru, S. Gupta, R. Howell, M. Kuball, *Thermal transport in superlattice castellated field effect transistors*, IEEE Electron Device Letters, Submitted 2018.

- J. W. Pomeroy, C. Middleton, M. Singh, S. Dalcanale, M. J. Uren, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, M. Kuball, $\beta - Ga_2O_3$ *MOSFET self heating and thermal management*, IEEE Electron Device Letters, 2019 **40** (2), 189-192.

- R. Kabouche, R. Pecheux, E. Okada, M. Zegaoui, J. Derluyn, S. Degroote, M. Germain, F. Gucmann, C. Middleton, J. W. Pomeroy, M. Kuball, F. Medjdoub, *High efficiency AlN/GaN HEMTs for Q-band applications with an improved thermal dissipation*, IEEE Transactions on Electron Devices, Submitted 2018.

- D. Liu, D. Francis, F. Faili, C. Middleton, J. Anaya, J. W. Pomeroy, D. Twitchen, M. Kuball, *Impact of diamond seeding on the microstructural properties and thermal stability of GaN-on-diamond wafers for high power electronic devices*, Scripta Materialia, **128**, 2017, 57-60.

- S. Mandal, E. L. H. Thomas, C. Middleton, L. Gines, J. T. Griffiths, M. J. Kappers, R. A. Oliver, D. J. Wallis, L. E. Goff, S. A. Lynch, M. Kuball, O. A. Williams, *Surface zeta potential and diamond seeding on gallium nitride films*, ACS Omega, **2**, 2017, 7275-7280.

- J. W. Pomeroy, R. B. Simon, C. Middleton, M. Kuball, *Transient thermoreflectance wafer mapping for process control and development: GaN-on-diamond*, IEEE Compound Semiconductor Integrated Circuit Symposium 2017, 1-4.

A.2 List of Presentations

- C. Middleton, J. Anaya, A. Taylor, M. Kuball, *Rapid thermal characterisation of ultra-thin nanocrystalline diamond films*, Hasselt diamond workshop, 2016, Poster presentation.

- C. Middleton, J. W. Pomeroy, S. Graham, K. Hobart, M. Kuball, *Measurement of diamond thin film thermal conductivity*, 68th De Beers Diamond Conference, 2017, Poster Presentation.

- C. Middleton, F. Gucmann, S. Dalcanale, J. W. Pomeroy, J. Chang, J. Parke, I. Wathunthanthri, K. Nagamatsu, E. Stewart, S. Gupta, R. Howell, M. Kuball, *Thermal analysis of castellated GaN high electron mobility transistors*, MRS Fall Meeting, 2017, Oral presentation.

- C. Middleton, S. Dalcanale, J. W. Pomeroy, M. J. Uren, M. Kuball, *The Superlattice Castellated Field Effect Transistor (SLCFET)*, Northrop Grumman University Symposium, Baltimore, 2018, Poster Presentation.

- C. Middleton, J. W. Pomeroy, M. Kuball, *Near-junction heat spreading applications of diamond in ultra-wide bandgap devices*, 69th De Beers Diamond Conference, 2018, Oral Presentation.

- M. Singh, J. W. Pomeroy, C. Middleton, M. J. Uren, M. A. Casbon, P. J. Tasker, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, M. Kuball, *Evaluation of electrical and thermal performance of* $\beta - Ga_2O_3$ *MOSFETs for RF operation.*, Compound Semiconductor Week, 2018, Oral Presentation.

- J. W. Pomeroy, M. Singh, C. Middleton, M. J. Uren, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, M. Kuball, *Thermal characterisation of* $\beta - Ga_2O_3$ *MOSFETS*, 60th Electronic Materials Conference, 2018, Oral Presentaion.

APPENDIX B

APPENDIX B

B.1 List of Acronyms and Abbreviations

- 2DEG - Two Dimensional Electron Gas
- CCD - Charge Coupled Device
- CFOM - Combined Figure of Merit
- CMOS - Complimentary Metal Oxide Semiconductors
- CVD - Chemical Vapour Deposition
- CW - Continuous Wave
- DARPA - Defense Advanced Research Project Agency
- EFG - Edge defined Film fed Growth
- FET - Field Effect Transistor
- GRT - Gate Resistance Thermometry
- HEMT- High Electron Mobility Transistor

- HF CVD - Hot Filament Chemical Vapour Deposition
- HNPS - High Nitrogen Pressure Solution
- HPHT - High Pressure High Temperature
- HVPE - Halide/Hydride Vapour Phase Epitaxy
- IGBT - Insulated Gate Bipolar Transistor
- JFOM - Johnson's Figure Of Merit
- LBFOM - Lateral Baliga Figure Of Merit
- LPP - Longitudinal Phonon-Plasmon
- MBE - Molecular Beam Epitaxy
- MESFET - MEtal Semiconductor Field Effect Transistor
- MOSFET - Metal Oxide Semiconductor Field Effect Transistor
- MOVPE - Metal Organic Vapour Phase Epitaxy
- MTTF - Mean Time To Failure
- MW PE CVD - MicroWave Plasma Enhanced Chemical Vapour Deposition
- NA - Numerical Aperture
- NICT - National institute of Information and Communications Technology
- SLCFET - SuperLattice Castellated Field Effect Transistor
- TBR_{eff} - Effective Thermal Boundary Resistance
- TTR - Transient ThermoReflectance
- UWBG - Ultra-Wide BandGap
- WBG - Wide BandGap

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