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DESIGN AND ANALYSIS OF A NON-ISOLATED HIGH GAIN STEP-UP CUK CONVERTER

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A Dissertation

Presented to

the Faculty of the Daniel Felix Ritchie School of Engineering and Computer Science

University of Denver

_____

In Partial Fulfillment

of the Requirements for the Degree

Doctor of Philosophy

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by

Yasser Almalaq

June 2019

Advisor: Dr. Mohammad Matin

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Title: DESIGN AND ANALYSIS OF A NON-ISOLATED HIGH GAIN STEP-UP CUK CONVERTER
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Abstract

Renewable energy sources, such as solar energy, are desired for both economic and ecological issues. These renewable energy sources are plentiful in nature and have a terrific capability for power generation. The only drawback of solar energy, which is one of the best forms of energy sources, is that the output has a low voltage and needs to be stepped up in order to be inserted into the DC grid or an inverter for AC applications. To overcome this drawback, a high gain DC-DC power converter is required in this kind of system. These power converters are needed for a better regulation capability with a small density volume, lightweight, high efficiency, and low cost.

In this dissertation, different topologies of a non-isolated high gain step-up Cuk converter based on switched-inductor (SL) and switched-capacitor (SC) techniques for renewable energy applications, such as photovoltaic and fuel cell, are proposed. These kinds of Cuk converters provide a negative-to-positive step-up DC-DC voltage conversion. The proposed Cuk converters increase the voltage boost ability significantly using the SL and SC techniques compared with the conventional Cuk and boost converters. Then, a maximum power point tracking (MPPT) technique is employed in the proposed Cuk converter to get the maximum power point (MPP) from the PV panel.

The proposed Cuk converters are derived from the conventional Cuk converter by replacing the single inductor at the input, output sides, or both by a SL and the transferring energy capacitor by a SC. The main advantages of the proposed Cuk converters are

achieving a high voltage conversion ratio and reducing the voltage stress across the main switch. Therefore, a switch with a lower voltage rating and thus a lower $R_{DS\text{-}ON}$ can be used, and that will lead to a higher efficiency. For example, the third topology of the proposed Cuk converter has the ability to boost the input voltage up to 13 times when D=0.75, D is the duty cycle. The voltage gain and the voltage stress across the main switch in all topologies have been compared with conventional converters and other Cuk converters used different techniques. The proposed topologies avoid using a transformer, coupled inductors, or an extreme duty cycle leading to less volume, loss, and cost.

The proposed Cuk converters are analyzed in continuous conduction mode (CCM), and they have been designed for 12V input supply voltage, 50kHz switching frequency, and 75% duty cycle. A detailed theoretical analysis of the CCM is represented, and all the equations have been derived and matched with the results. The proposed Cuk converters have been simulated in MATLAB/Simulink and the results are discussed.

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First and foremost, I thank my God for giving me the effort to complete my PhD program and gave me all the blessings and gifts I enjoy in my life.

I would like to thank my advisor, Dr. Mohammad Matin, for accepting me in his research group and all help and encouragement he gave me during my study. Dr. Matin supported me during my doctoral program from the first day at the University of Denver until the last day. This dissertation could not have been accomplished without his help and guidance.

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List of Acronyms

Acronym	Definition
AC	Alternating current
CCM	Continuous conduction mode
CSC	Canonical switching cell
D	Duty cycle
DC	Direct current
DCM	Discontinuous conduction mode
EMI	Electro-magnetic interference
f	Switching frequency
IncCond	Incremental conductance
I_{in}	Input current
I_{out}	Output current
I_{ph}	Photo-generated current
I_{SC}	Short circuit current
Δi_L	Peak-to-peak variation of the inductor's current
M	Voltage gain
MOSFET	Metal-oxide-semiconductor field-effect-transistor
MPPT	Maximum power point tracking
N	Number of levels
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse width modulation
P&O	Perturbation and observation
$R_{DS\text{-}ON}$	Drain-source on resistance
SC	Switched-capacitor
SEPIC	Single-ended primary-inductor converter
SL	Switched-inductor
T	Time period
VMC	Voltage multiplier cell
V_C	Voltage across a capacitor
V_D	Voltage across a diode
V_{in}	Input voltage
V_L	Voltage across an inductor
V_{OC}	Open circuit voltage
V_{out}	Output voltage
V_S	Voltage across a switch
Δv_C	Peak-to-peak variation of the capacitor's voltage
W_P	Watt peak capacity
η	Efficien

Chapter One: Introduction

Due to expectations of depleting of traditional energy sources, pollution, and noise, the world pays growing attention to alternative ones. Nowadays, the most attention goes to the photovoltaic (PV) energy source due to pollution free, stable system, and continuous reduction in cost. The price of a PV panel goes from \$4.90/W_P in 1998 down to \$1.28/W_P in 2011 which means 74% of reduction. PV systems are used today in many applications, such as water pumping, battery charging, home power supply, etc. [1]–[5].

Fig. 1.1 shows a block diagram of a typical sustainable energy system, which composed of renewable energy sources, a high step-up DC-DC converter, a DC grid, and an inverter for AC applications. Usually, the rated voltage of renewable energy sources, such as photovoltaic and fuel cell, is at low level, and thus, a high gain DC-DC converter is required in this kind of system. A DC-DC converter or "switching regulator" converts a fixed voltage DC source, such as a solar panel, battery, or fuel cell, from one level to a different level either to supply a DC load or to be an input to an inverter for AC applications [6], [7]. Generally, the most commonly used topology to supply a high output voltage is the conventional boost converter. However, when the conventional boost converter is operated at a high output voltage, the duty cycle will become unity. This will lead inducing a high current ripple, low efficiency, and will result in severe reverse-recovery as well as high electromagnetic interference (EMI) problems [8]. Many high step-up DC-DC converters have been proposed and are utilized in renewable energy applications [9]–[17].

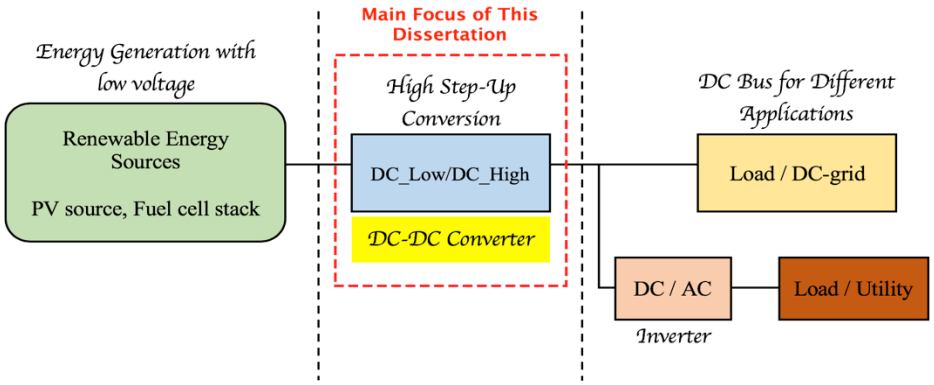


Fig. 1.1 Grid tied renewable energy sources with high gain DC-DC converter

It is essential to operate the PV panel at the maximum power point (MPP) because of nonlinearity in the power and voltage. This happens when there is a change in atmospheric conditions like the change in irradiance due to partial shading and the change in temperature. Maximum power point tracking (MPPT) is used to extract the MPP from the PV panel at maximum efficiency. Therefore, it can deliver all the power it generates [18].

In some special industrial applications such as automobiles, space stations, and manufacturing industries, DC-DC converters that can achieve the negative to positive voltage conversion play an important role [19]. In such applications, the negative DC voltage source requires a DC-DC converter that realizes the polarity inversion to provide the positive voltage to the load with respect to the common ground. In designing the DC-DC converter for the negative DC voltage bus, two features should be taken into account: a negative to positive voltage conversion path and high voltage conversion ratio [20].

In this dissertation, the main focus is to design a DC-DC converter with a high voltage gain and low voltage stress on the main semiconductor switch. This is achieved by

integrating both switched-inductor (SL) and switched-capacitor (SC) techniques into the conventional Cuk converter. The Cuk converter has many advantages over other non-isolated converters, such as having non-pulsating input and output currents, a low output voltage ripple, and a good steady-state performance [21], [22]. Then, a MPPT technique is used in the proposed Cuk converter to get the MPP from the PV panel.

1.1 DC-DC Converter Design Characteristics

The main criteria of having a DC-DC step-up converter in PV applications is the ability to produce a high output voltage from a low input voltage. A high voltage is essential for different DC applications, and also for efficient conversion to AC when using an inverter for AC applications.

One option to increase the output voltage of a PV is having a series combination of multiple PV modules. However, this solution has many disadvantages. One disadvantage is reducing reliability. In case of a failure of at least one PV module in a series string, that will result in the entire string being unavailable. The other disadvantage is that the current through the series-connected components must always be equal, and the total string current will be determined by the lowest performing current in the string. This is a problematic in the case of a partial shading. Therefore, a shading of a single PV module will reduce the output power of the entire string. Thus, it is more advantageous to have parallel PV modules and use a high gain DC-DC converter [23], [24].

1.2 Research Objectives

In this dissertation, the concept of switched-inductor (SL) and switched-capacitor (SC) techniques have been integrated to the conventional Cuk converter, and consequently,

new step-up Cuk converters are proposed. From the viewpoint of a circuit topology (combining a SL with a SC in a Cuk converter), the proposed converters are different from any other existing Cuk converter. The main objectives of the proposed Cuk converters are summarized as follows.

- provide a non-isolated negative to positive voltage path with respect to a common ground;
- higher voltage conversion ratios than the conventional Cuk and boost converters due to the SL and SC techniques;
- lower voltage stress across the main switch than the conventional Cuk and boost converters, therefore, a switch with low voltage rating and low $R_{DS\text{-}ON}$ can be used;
- the main advantage of the conventional Cuk converter which is having a continuous current in the input and output sides due to the input and output inductors has been kept when designing the proposed topologies.

1.3 Dissertation Organization

Chapter 2 of this dissertation introduces a literature review of different step-up boost-based converters. This includes different conventional step-up converters and different step-up topologies.

Chapter 3 will introduce an overview of the need for a PV in today's world. In addition, it introduces a PV module and how it behaves in a system. Also, it gives a description of a MPPT technique includes two algorithms that are P&O and IncCond.

Chapter 4 will give a detailed explanation of the proposed topologies of a Cuk converter includes a power circuit, modes of operation, and circuit analysis.

Chapter 5 will present a comparison between the proposed Cuk converter topologies with conventional converters and other Cuk converters using different techniques in terms of the voltage gain, voltage stress across the main switch, and cost.

Chapter 6 will present the results of testing the proposed topologies. This chapter will show the simulated results of the proposed topologies in MATLAB/Simulink software with a brief discussion.

Chapter 7 will summarize the current work and give some recommended points of future work on this topic.

Chapter Two: Literature Review

2.1 Introduction

Various DC-DC converter topologies include isolated converters and non-isolated converters have been developed to achieve a high voltage gain without an extremely high duty cycle for renewable energy applications. In this chapter, a description and a comparative analysis has been mentioned and made for isolated and non-isolated DC-DC converters. A possible classification of step-up DC-DC converters (boost-based) is proposed in Fig. 2.1. The rated voltage of renewable energy sources such as photovoltaic and fuel cell is at low levels. Therefore, a high gain DC-DC converter with a high efficiency is required in this kind of system [25]. Here, the main attention goes to the non-isolated DC-DC converters.

2.2 Isolated Converters

Usually, isolated DC-DC converters using a transformer is used when a high step-up ratio is required because the voltage gain can be adjusted by increasing the turns ratio of the transformer [26]–[31]. An electric isolation in isolated DC-DC converters using a transformer is needed for three reasons which are safety, different reference potential, and voltage matching [32]. However, isolated converters have some difficulties in achieving a high efficiency due to the power transformer losses and the leakage inductance besides the heavy weight and large volume of the converter. Also, another disadvantage is that the input current is pulsating, and that makes the life of the PV array shorter. Therefore, the

best solution is to take advantage of a non-isolated converter with additional techniques associated to achieve a high voltage gain [33]–[35]. Main isolated DC-DC converters include flyback converter (derived from buck-boost), forward converter (derived from buck converter), full-bridge converter, half-bridge converter (both derived from buck converter), and push-pull converter [32].

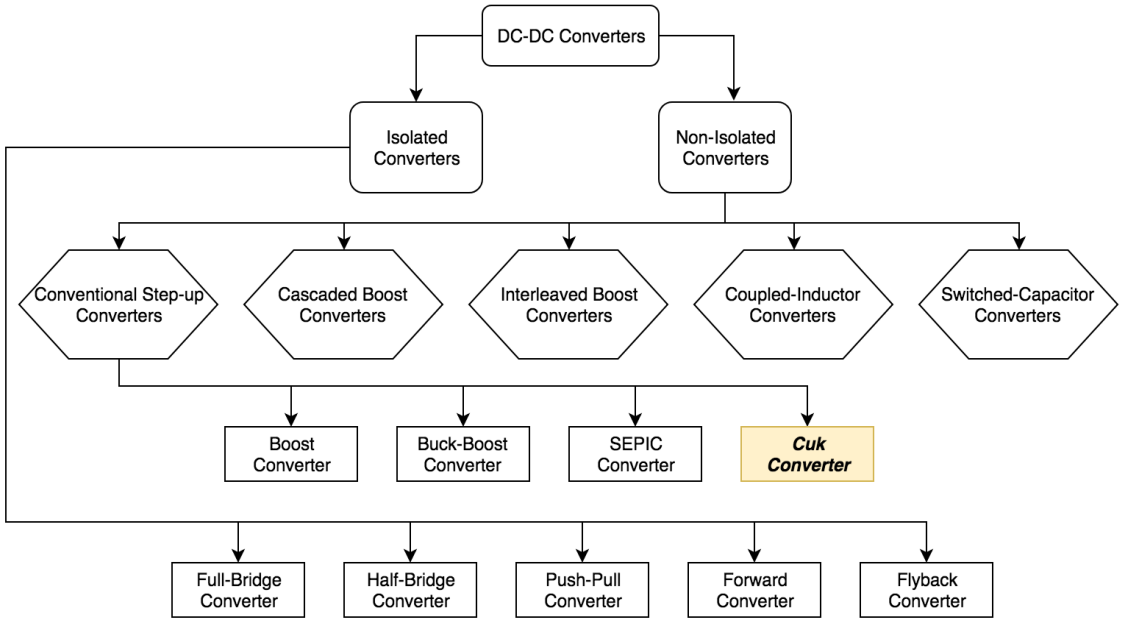


Fig. 2.1 Classification of DC-DC converters

2.3 Non-Isolated Step-Up DC-DC Converters

Non-isolated DC-DC converters can be utilized to accomplish a voltage step-up or step-down with inverting or non-inverting polarity in applications that do not require a galvanic isolation. Using non-isolated converters will reduce the size, weight, and volume compared with the isolated converters due to the lack of the high-frequency transformer [36], [37]. These non-isolated converters consist of three parts which are magnetic field storage components (inductors or coupled inductors), electric field storage components

(capacitors), and various active or passive switching elements (power switches and diodes) [38].

2.3.1 Boost Converter

Circuit diagram in Fig. 2.2 is called boost converter because the output voltage level is larger than the input voltage level as the name implies [39]. It consists of one active switch, one diode, one inductor, and one capacitor. The two main applications of the boost converter are in the regulated DC power supplies and regenerative braking of DC motors [40]. Also, boost converters are widely used in DC-DC and AC-DC power conversions to accomplish the preferred electric energy, such as PV systems and power factor correction (PFC) converters [41]–[43].

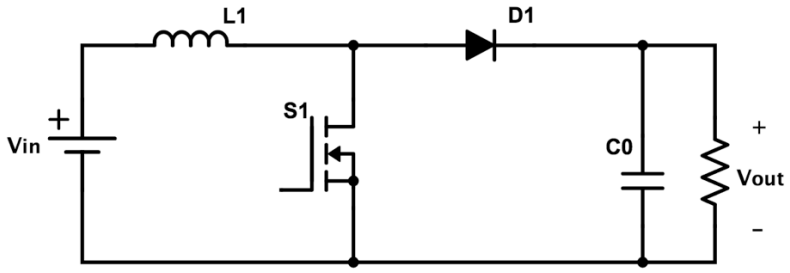


Fig. 2.2 Conventional Boost Converter

The voltage conversion ratio equation for the conventional boost converter is as described in (2.1).

$$M_{boost} = \frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)} \tag{2.1}$$

When a conventional boost converter is operated in extreme duty cycle (D > 0.8), the single diode has a tiny period of time to turn off. Thus, it has a long period of time to conduct. This causes a huge voltage and current stress on the diode. Also, at extreme duty cycles, there will be an enormous power loss across the diode [44]. A conventional boost

converter with a high output voltage requires a MOSFET with a high current and voltage ratings. Therefore, this MOSFET has a high on-resistance, which increases the cost, size, and conduction loss [45]. Also, the switching losses and the reverse recovery problems are significant. Despite the disadvantages mentioned previously, the conventional boost converter still has some attraction because of many advantages, such as using fewer components which leads to a cheaper price, having non-pulsating input current (if used in CCM), and simple drive circuit [46].

2.3.2 Buck-Boost Converter

Circuit diagram in Fig. 2.3 is called buck-boost converter which has the ability to increase or decrease the input voltage level with a polarity inversion [39]. This converter is also known as an inverting or flyback converter [47]. As in the conventional boost converter, the buck-boost converter consists of one active switch, one diode, one inductor, and one capacitor. The conventional buck-boost converter is obtained by cascading the conventional buck (step-down) and conventional boost (step-up) converters. The main application of the conventional buck-boost converter is in regulated DC power supplies, where a negative output with respect to the ground is required [40].

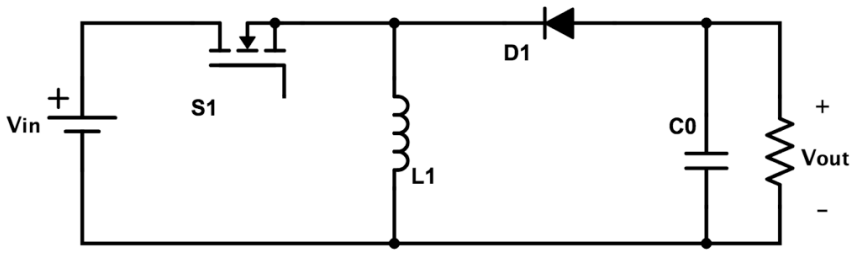


Fig. 2.3 Conventional buck-boost converter

The voltage conversion ratio equation for the conventional buck-boost converter is as described in (2.2).

$$M_{buck-boost} = \frac{V_{out}}{V_{in}} = -\frac{D}{(1-D)} \tag{2.2}$$

2.3.3 Cuk Converter

The circuit diagram in Fig. 2.4 is called Cuk (named after its inventor) which has the capability to increase or decrease the input voltage level with a polarity inversion like the buck-boost converter. It consists of one active switch, one diode, two inductors, and two capacitors. Like the conventional buck-boost converter, the main application of the conventional Cuk converter is in regulated DC power supplies, where a negative output with respect to the ground is required [40].

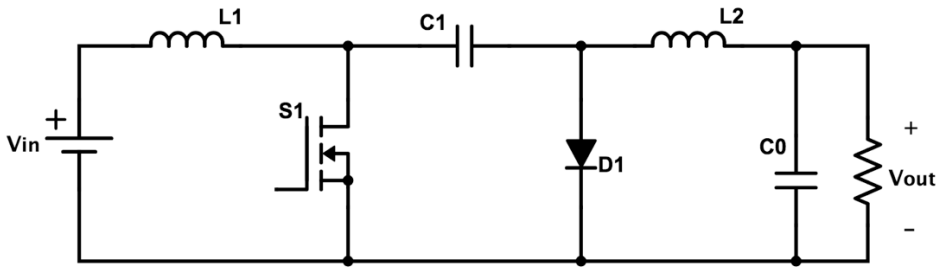


Fig. 2.4 Conventional Cuk converter

The voltage conversion ratio equation for the conventional Cuk converter is as described in (2.3).

$$M_{Cuk} = \frac{V_{out}}{V_{in}} = -\frac{D}{(1-D)} \tag{2.3}$$

Conventional Cuk and buck boost converters are two DC-DC converters that have an output voltage magnitude which is either greater or less than the input voltage with a polarity inversion due to their voltage conversion ratio. The polarity inversion is represented as a negative sign as described in (2.2) and (2.3). The value of D which is the duty cycle cannot be too high (more than 0.8) and consequently, their boost voltage abilities

have been restricted due to the effect of parasitic components [20]. The conventional Cuk converter has three modes (buck mode, boost mode, and buck-boost mode) [48]. The conventional Cuk converter has advantages such as having an energy transfer capacitor, a good steady-state performance, continuous input and output currents, and a low output voltage ripple [49].

Advantages compared with the buck, boost, buck-boost, single ended primary inductor converter (SEPIC), zeta, Luo, and canonical switching cell (CSC) converter in terms of the continuousness of input and output currents, MPPT operating region, and switch drive circuitry are summarized in Table 2.1 [50]. From Table 2.1, it is obvious that the Cuk converter is more advantageous compared with any conventional non-isolated DC-DC converter. The conventional Cuk converter offers an unbounded MPPT operating region, non-pulsating input and output currents which avoid external filtering, and the switch control terminal is connected to ground which simplifies the gate drive circuitry [50]. [51]–[55] present Cuk converters using different techniques, however, the voltage conversion ratio is low. A number of switched-inductor and switched-capacitor topologies are presented in [56] to achieve a higher voltage gain.

Table 2.1 Comparison of conventional non-isolated DC-DC converters

Converter	MPPT Region	Input Current	Output Current	Switch Drive
Buck [57]	Bounded	Pulsating	Non-pulsating	Floated
Boost [57]	Bounded	Non-pulsating	Pulsating	Grounded
Buck-Boost [57]	Unbounded	Pulsating	Pulsating	Floated
Cuk [57], [58]	Unbounded	Non-pulsating	Non-pulsating	Grounded
SEPIC [57]	Unbounded	Non-pulsating	Pulsating	Grounded
Zeta [57], [59]	Unbounded	Pulsating	Non-pulsating	Floated
Luo [60]	Unbounded	Pulsating	Non-pulsating	Floated
CSC [61]	Unbounded	Pulsating	Pulsating	Floated

2.4 Voltage Multiplier

Voltage multiplier circuits are simple topologies that consist of a combination of a set of diodes and inductors, capacitors, or both. Voltage multiplier cell (VMC) is integrated in the middle of a circuit usually after the main switch to increase the voltage gain and reduce the voltage stress. VMCs are popular for their high boosting ability as they are simple to integrate in any circuit. Fig. 2.5 shows a VMC which is implemented in a circuit contains of a single active switch, two inductors, and a capacitor [38].

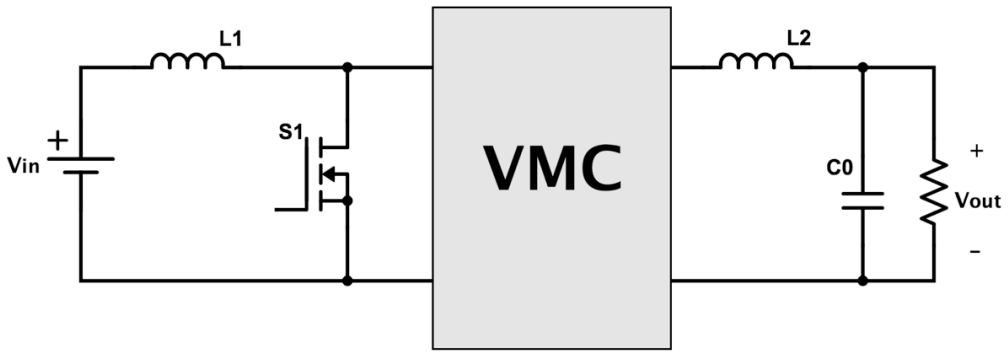


Fig. 2.5 VMC location in step-up mode converter

2.5 Switched-inductor based Boost Converters

Fig. 2.6 shows a switched-inductor (SL) cell-based boost converter. The SL-cell composes of two inductors and three diodes. The two inductors will charge in parallel by the input supply voltage when the active switch is on. Then, they will discharge in series when the active switch is off. Both inductor windings of the SL-cell can be accommodated into a single core, which is an advantageous criterion. Also, smaller conductors can be utilized because the input current in this circuit is small. Compare to the conventional boost converter, the voltage gain is higher when a SL-cell is combined. However, there are two issues that need to be solved. First, the active switch suffers from a very high voltage stress

almost equals to the output voltage. Second, the output diode encounters reverse recovery problems [46], [56].

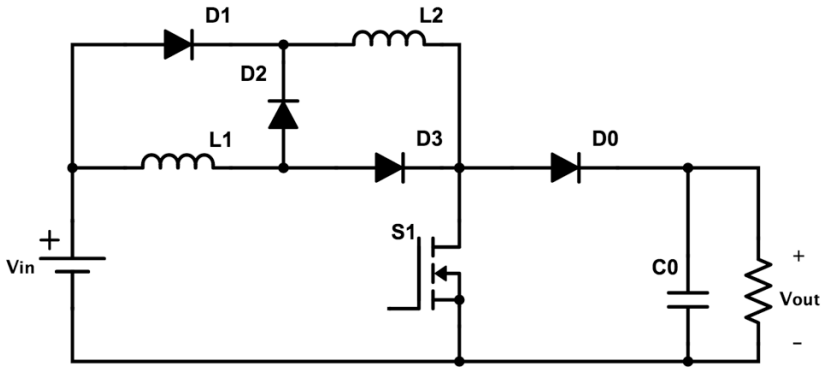


Fig. 2.6 SL based boost converter

2.6 Cascaded Boost Converters

Fig. 2.7 shows a cascade boost converter. It consists of two active switches, two diodes, two inductors, and two capacitors. This circuit shown is two boost DC-DC converters cascaded, and also more than two can be cascaded. In the first stage and to improve the power density, the cascade boost converter can be operated with a high switching frequency because the voltage stress is low. In the second stage and to reduce the switching losses, the converter can be operated with a low switching frequency [33]. The main advantage of using this cascade boost converter topology is having higher DC voltage gain, and therefore, lower duty cycle can be used. However, this topology has disadvantages which are doubling the number of components and increasing the losses compared with the conventional single stage boost converter. Also, this topology has a major problem is a system stability, and the electromagnetic interference (EMI) problem is severe. So, this topology achieves high voltage gain at the expense of having more components count, higher cost, and lower efficiency [44], [46], [62].

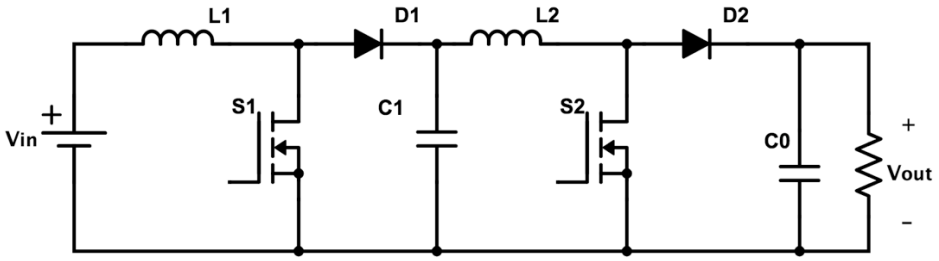


Fig. 2.7 Cascade boost converter

In [63], a cascade boost converter is presented. It can supply a load with a high voltage and relatively high efficiency. The major drawbacks of using this topology are higher cost because of using two DC-DC converters and the complexity.

2.7 Quadratic Boost Converters

Fig. 2.8 shows a conventional single-switch quadratic boost converter which has a low efficiency because of the effect of cascading, and a higher voltage gain is achieved compared with the conventional boost converter. It consists of a single active switch, three diodes, two inductors, and two capacitors. According to its name, the voltage gain equation is a quadratic function of the duty cycle D [64], [65]. One advantage of this approach is that the diode reverse recovery problem is lower. However, when a very high voltage gain is desired, this topology has to operate in extreme duty cycles. Therefore, the diode reverse recovery problem starts to show up [44]. Also, the voltage stress of the active switch equals to the output voltage, and the current stress is high because the current of the two inductors flow through the active switch. That means that the active switch suffers from high voltage stress and current stress [33]. This leads to use very expensive one.

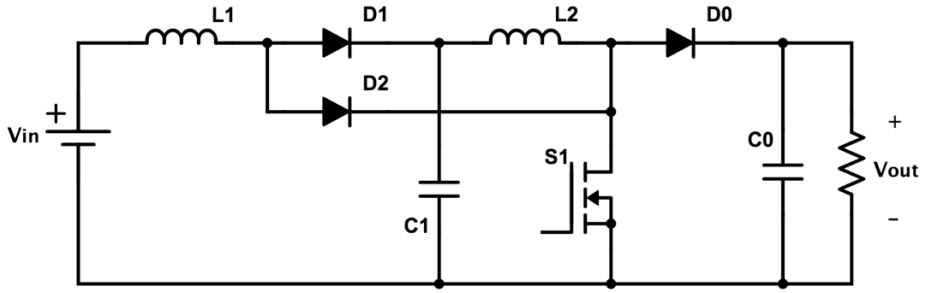


Fig. 2.8 Single-switch quadratic boost converter

2.8 Interleaved Boost Converters

Fig. 2.9 shows a conventional interleaved boost converter. It consists of two active switches, two diodes, two inductors, and a capacitor. This topology is not suitable for high voltage gain applications because it offers almost the same gain as in the conventional boost converter at higher duty cycles. In on-mode, there will be a large current ripple. Therefore, this will increase the conduction loss. In off-mode, this approach will encounter severe reverse recovery problems at the output diode [46], [66].

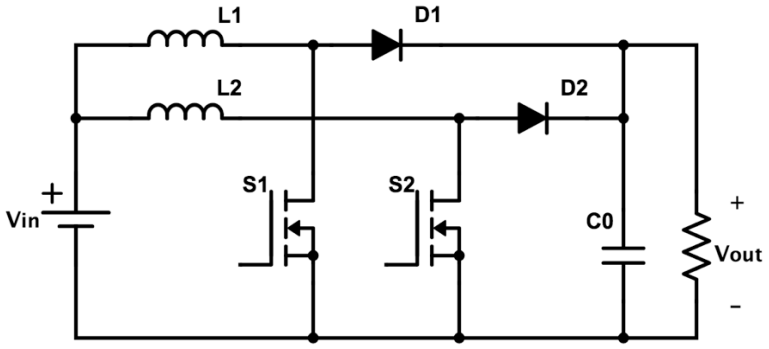


Fig. 2.9 Interleaved boost converter

2.9 Coupled-Inductor Converters

Converters with coupled inductors topology can accomplish a high voltage gain by choosing properly the winding ratio, and thus, using extreme duty cycle is avoided [67]–[70]. Besides higher voltage gain, the reverse recovery of the output diode is improved.

However, using coupled inductors topology will reduce the efficiency due to the losses associated with the leakage inductance. To overcome this leakage inductance, active clamp circuits are used. Adding these clamp circuits to the main topology will increase the price and complexity. Other drawbacks are requiring a high voltage rated switch and suffering from EMI problems [45], [46].

2.10 Switched-Capacitor Converters

The capacitor can be considered as another voltage source to achieve high voltage gain, which is switched and recombined by the switches [33]. For low power, a switched-capacitor converter can be used to provide a high voltage gain. The main advantage of using switched-capacitor converters is the fact that it uses only number of semiconductor switches and capacitors without using any magnetic components, such as inductors or transformers. However, as more voltage gain is required, more components have to be added. That makes the circuit structure more complicated and costly [71], [72].

2.11 Comparison Study

In Table 2.2, a comparison has been made between the conventional boost converter, single switch quadratic boost converter, SL boost converter, cascade boost converter, and interleaved boost converter in terms of the voltage gain, voltage stress across the main switch, voltage stress across the output diode, number of active switches, number of diodes, number of inductors, and number of capacitors.

Table 2.2 Several boost-based converters comparison

Topology	Boost	Quadratic	SL Boost	Cascade	Interleaved
Active Switches	1	1	1	2	2
Diodes	1	3	4	4	2
Inductors	1	2	2	2	2
Capacitors	1	2	1	4	1
Voltage gain	$\frac{1}{1-D}$	$\left(\frac{1}{1-D}\right)^2$	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Switch voltage stress	V_{out}	V_{out}	$\frac{V_{out}+V_{in}}{2}$	$\frac{V_{in}}{1-D}$	V_{out}
Output diode voltage stress	V_{out}	V_{out}	$\frac{V_{out}+V_{in}}{2}$	$\frac{V_{in}}{1-D}$	V_{out}

Chapter Three: PV System

3.1 Introduction

In this chapter, a PV system is fully discussed. Also, two MPPT methods which are perturb & observe (P&O) and incremental conductance (IncCond) methods are discussed in this chapter. The importance of solar energy source is that the installation of PVs is growing year by year. The capacity of the global solar PV energy growth is shown in Fig. 3.1. As can be observed from the chart, there is a large percentage increase of 87.5% and 75% in 2008 and 2011, respectively. Also, the capacity reached 228GW and 303GW in 2015 and 2016. By 2040, PV sources are expected to become the largest contributors to electricity generation among all renewable energy candidates. If PV cells are manufactured at adequately large scale with involving technologies, a $1 US per watt price for a PV cell can be accomplished [73]–[75].

3.2 PV Cell

The PV cell, also known as solar cells, is the smallest component in a PV module. A DC electric power can be obtained from the PV by semiconductors when they are illuminated by photons. The solar cell generates electric power as long as the sunlight is shining on it. The equivalent circuit of a PV cell is shown in Fig. 3.2 which contains both the ideal and practical components. It consists of an ideal photovoltaic current (I_{ph}) connected in parallel with a diode, a parallel resistor R_p, and a series resistor R_s. The ideal PV cell simply contains a current source and a diode, in which the output current is directly

proportional to the amount of sunlight falling on the cell. On the other hand, a parallel resistor and series resistor are added to configure the practical PV cell because the ideal PV cell does not exist [76]–[78]. The efficiency of the PV cell depends on many factors such as solar radiation, temperature, dust particles, and series and shunt resistances. That is therefore important to use MPPT technique to increase the efficiency [79].

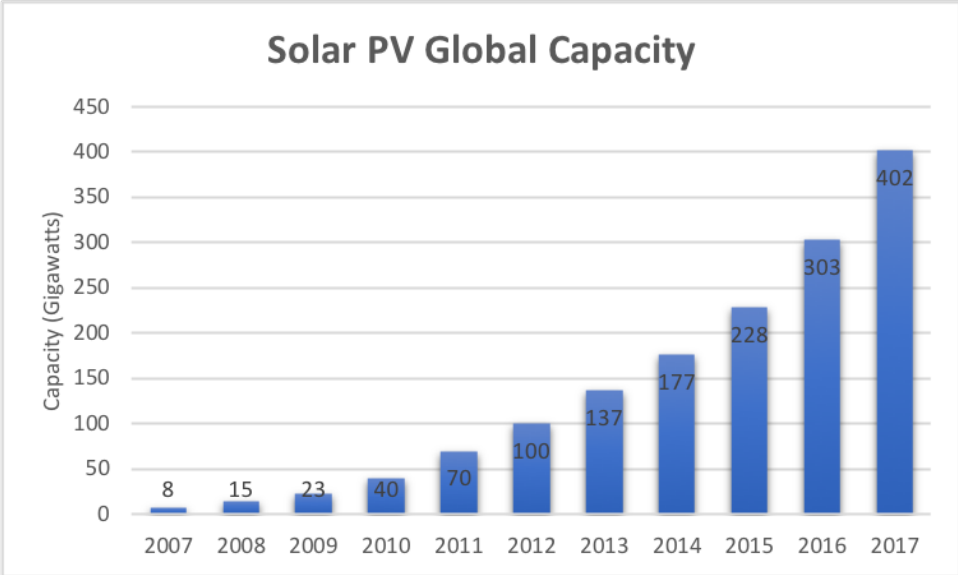


Fig. 3.1 Global annual growth of solar energy [80]

3.3 PV Module

A PV system consists of many PV modules which are made of series and parallel-connected solar cells because of the inadequate power of one PV cell [81]. The difference between series-connection and parallel-connection of the PV module is illustrated in Fig. 3.3. Series-connection will increase the voltage with the current being constant. However, parallel-connection will increase the current with the voltage being constant. In order to accomplish a certain amount of voltage and current, it is required to connect a number of PV cells either in parallel or in series [76]–[78].

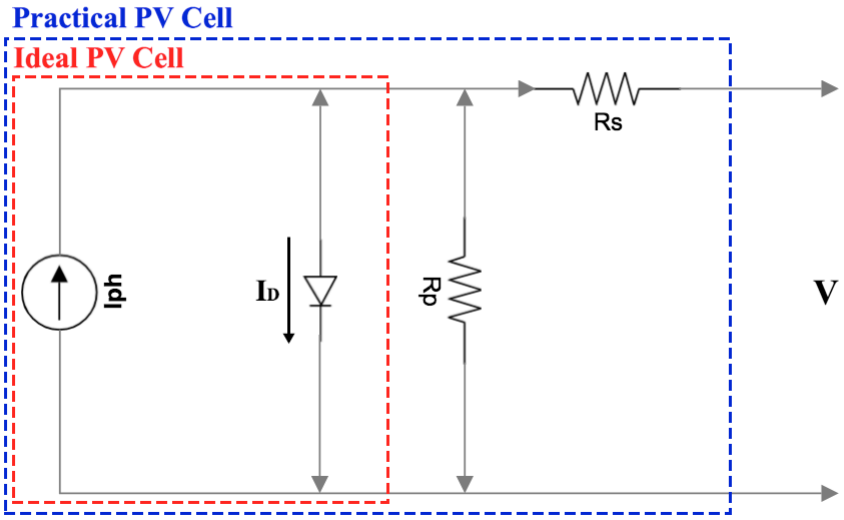
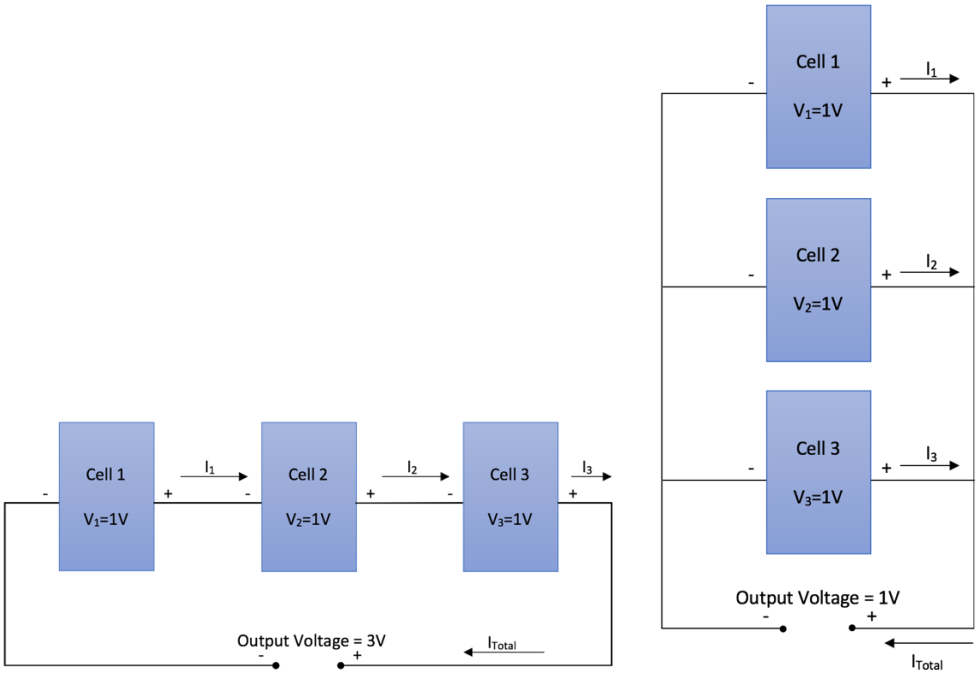


Fig. 3.2 PV cell



(a) (b)

Fig. 3.3 PV connections to increase voltage and current (a) series connection (b) parallel connection

The relation between current and voltage can be settled from the diode characteristic equation which is expressed in 3.1 and 3.2.

$$I = I_{ph} - I_0 \left\{ \exp\left[\frac{e(V + IR_S)}{KT_{cell}} \right] - 1 \right\} \quad (3.1)$$

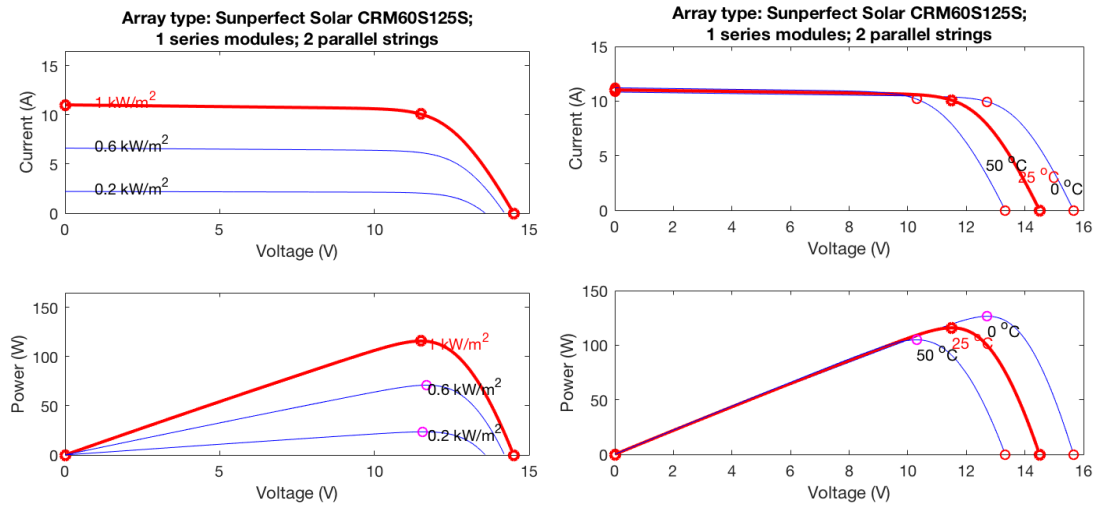
$$V = V_t \ln\left(\frac{I_{ph}}{I_0} \right) \quad (3.2)$$

Where:

I	Cell output current (A)
I_{ph}	Photogenerated current (A)
I_0	Diode saturation current (A)
V	Cell output voltage (V)
R_s	Series resistor (Ω)
e	Electronic charge 1.6x10-19 (coul)
K	Boltzman constant (j/K)
T_{cell}	Cell temperature (K)
V_{OC}	Open circuit voltage (V)
V_i	Thermal voltage (V)

(I_{ph}) is proportional to solar radiation. (I_{SC}) which produced under short circuit conditions (V=0) is the maximum value of (I). (V_{OC}) is the maximum voltage at zero current [77]. Fig. 3.4 shows current against voltage (I-V) and power against voltage (P-V) characteristic curves of a PV module (Sunperfect Solar CRM60S125S). There are unique points on I-V and P-V curves that indicate the maximum generated power for different values of irradiance and temperature. As can be observed from Fig. 3.4, the PV module's current is proportional to the amount of irradiance (or amount of sunlight). However, the PV module's voltage is inversely proportional to the temperature of the PV module. In

most applications, PWM DC-DC converters are used as the power interface between the PV and the load where the duty cycle (D) is the control variable [76], [78]. Consequently, the MPPT technique is a necessity for PV systems to ensure that the converter operates at MPP.



(a) (b)

Fig. 3.4 I-V and P-V for varying (a) irradiance (b) temperature

3.4 MPPT Methods

The efficiency of PV modules can be highly reduced due to atmospheric conditions, such as temperature and solar radiation variations, which varies depending on the time of the year and the weather of the day [82]. The output current of the PV will increase due to the increase in solar radiation, whereas the voltage at the PV terminals will decrease due to the increase of the temperature [83]. To overcome this change in atmospheric conditions and always supply the maximum power as possible, a special technique called maximum power point tracker (MPPT) is applied. MPPT is employed in PV systems to allow imposing continuously the PV module operation point to maximum power point (MPP) or close to it [84]. In [85]–[89], several MPPT methods are studied to overcome these

atmospheric conditions and operate the PV panel at its MPP. The most used methods among these mentioned are perturb & observe (P&O) and incremental conductance (IncCond) algorithms as MPPT techniques for PV systems [90]. Nowadays, most PV designs use MPPT for MPP generation despite any change in atmospheric conditions and their effect on PV modules. Fig. 3.5 shows the general view of the system under study where v and i are the voltage and current drawn from the PV array and D is the duty cycle of the DC-DC converter.

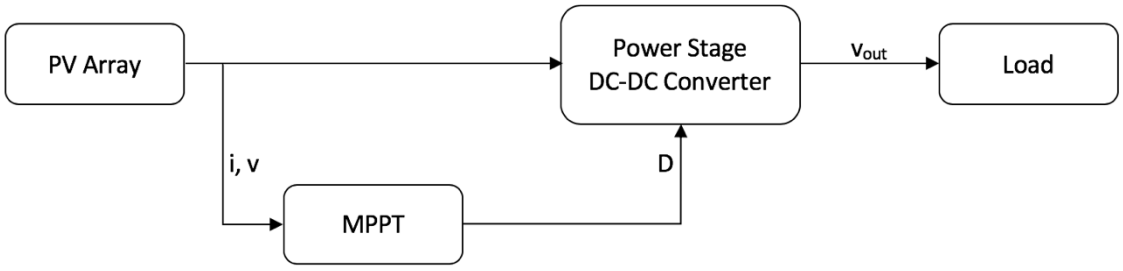


Fig. 3.5 The system under study

3.4.1 P&O MPPT Method

The perturbation and observation (P&O) method has been commonly used because of two main reasons which are simplicity of the feedback structure and fewer measured parameters. In the P&O method, the maximum power tracker operates by periodically incrementing or decrementing the solar array voltage. By using this process of maintaining the voltage, the maximum power is possible to be tracked [91]. From its name, it introduces a perturbation to the operating point of the system in order to obtain the maximum output power. The output power is calculated by sensing the values of the voltage and current of the PV module. After a small perturbation is added, the new value of the power is measured by sensing the new values of the voltage and current. If the new value of the power is

positive, the system will keep adding a perturbation. However, if the new value of the power is negative, the system will add a negative increment to bring the output power back to the MPP [92]. Although P&O algorithm is very simple to apply, there are drawbacks of using this method as an MPPT. First, if there is a slowly varying in atmospheric conditions, there will be an oscillation around the MPP resulting in a power loss. The amount of power loss depends on the size of the perturbation. Second, if there is a rapid change in atmospheric conditions, the P&O algorithm can be confused. Third, P&O algorithm is not capable of tracking the global peak under partial shading condition in its original form [93], [94]. In order to reduce this steady state oscillation in P&O algorithms, several proposed techniques are proposed [95]–[99]. The control flowchart of P&O algorithm is shown in Fig. 3.6.

3.4.2 IncCond MPPT Method

Incremental conductance (IncCond) method is widely used as a MPPT technique. That because of the high tracking accuracy at steady state condition and great adaptability to the rapidly changing atmospheric conditions. In this method, the steady state oscillations would be removed in theory due to disappear in the derivative of the power with respect to the voltage at MPP [100]. The IncCond method tracks the MPPT accurately by comparing the incremental conductance and the instantaneous conductance of a PV array [101]. As can be observed in (3.3) and (3.4), the IncCond is based on the derivative of the output power of the PV with respect to the voltage.

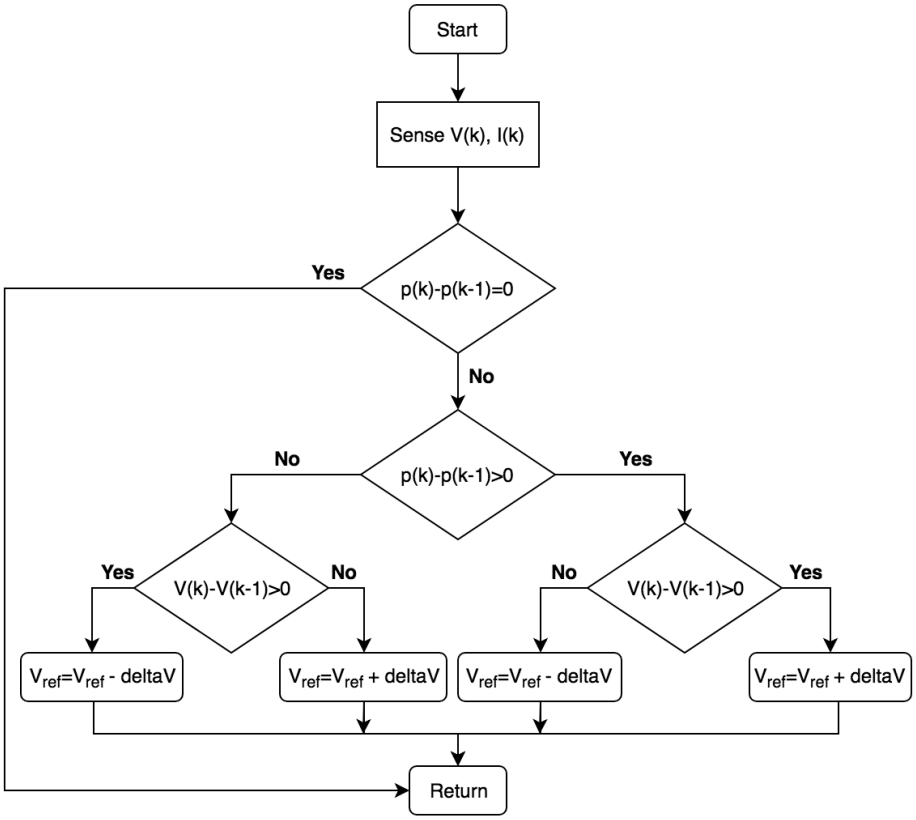


Fig. 3.6 Control flowchart of P&O

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I\frac{dI}{dV} + V\frac{dI}{dV} = I + V\frac{dI}{dV} \tag{3.3}$$

When the PV array operates at the MPP, dP/dV=0 as in (3.4).

$$I + V\frac{dI}{dV} = 0 \Rightarrow \frac{dI}{dV} = -\frac{I}{V} \tag{3.4}$$

Where dI/dV is the incremental conductance and I/V is the instantaneous conductance of the PV array. By comparing these two which are the incremental and the instantaneous conductance, it illustrates the position of currently operating point in relation with MPP [102]. Table 3.1 summarizes the IncCond algorithm situations [103].

Table 3.1 Summary of IncCond algorithm situations

$\frac{\mathbf{dP}}{\mathbf{dV}} = \mathbf{0}$	At MPP	Hold voltage at $V_{PV} = V_{MPP}$
$\frac{\mathbf{dP}}{\mathbf{dV}} > \mathbf{0}$	Left of MPP	Increase voltage until $V_{PV} = V_{MPP}$
$\frac{\mathbf{dP}}{\mathbf{dV}} < \mathbf{0}$	Right of MPP	Decrease voltage until $V_{PV} = V_{MPP}$

In the IncCond method, the PV terminal voltage can be attuned relative to the MPP voltage by measuring the incremental and instantaneous array conductance. Although four sensors are mandatory to perform the computations, IncCond method offers a good performance under rapidly changing atmospheric conditions [91]. The control flowchart of IncCond algorithm is shown in Fig. 3.7. At the MPP, the derivative of the power with respect to the voltage should be zero in IncCond algorithm. The IncCond method offers a better tracking comparing with P&O method in case of abrupt changing atmospheric conditions, and IncCond method reduces the oscillation around the MPP under the steady-state condition [104].

3.5 PV Power System

Fig. 3.8 shows a typical PV system block diagram. A PV array is connected to a high gain DC-DC boost converter to step-up the PV voltage to the desired level. A bidirectional DC-DC converter is positioned between a battery energy storage and the DC link to step-up the battery voltage to the DC link level. Also, the bidirectional DC-DC converter has the capability to allow power to flow from the battery to the DC link which is a discharging process, or from the DC link to the battery which is a charging process. An inverter and LCL filter are placed between the DC-DC converters and the AC load

because the first converts the DC to AC power and the second limits the harmonics. The AC power comes from the inverter will supply utility grid and any AC load [24], [105].

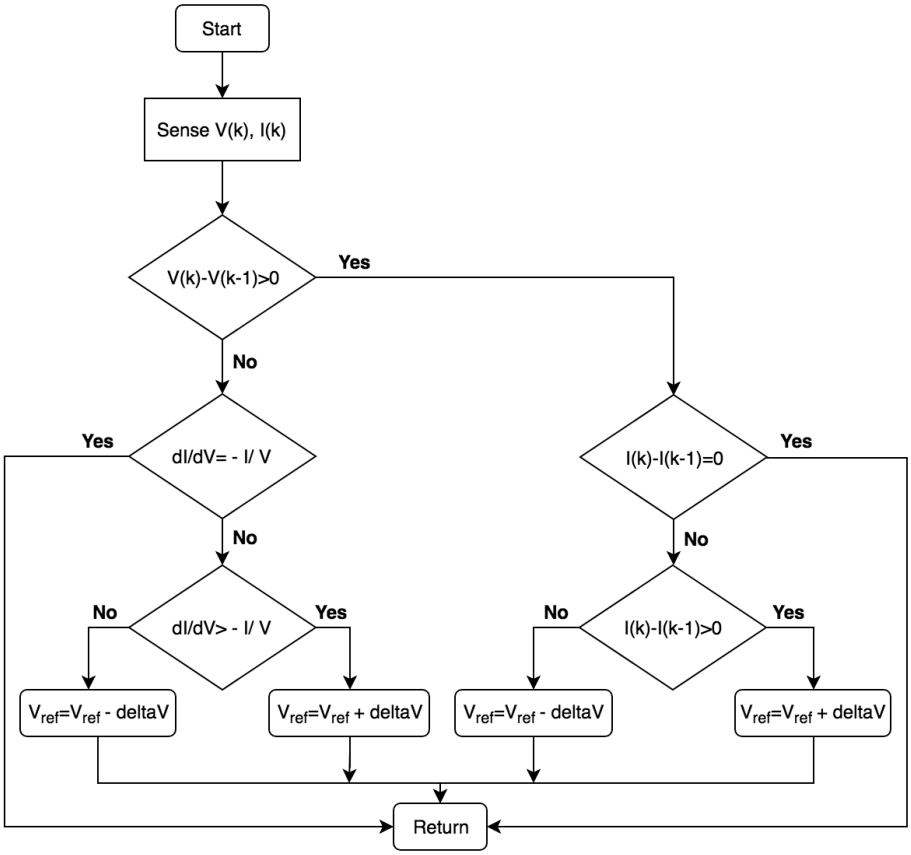


Fig. 3.7 Control flowchart of IncCond

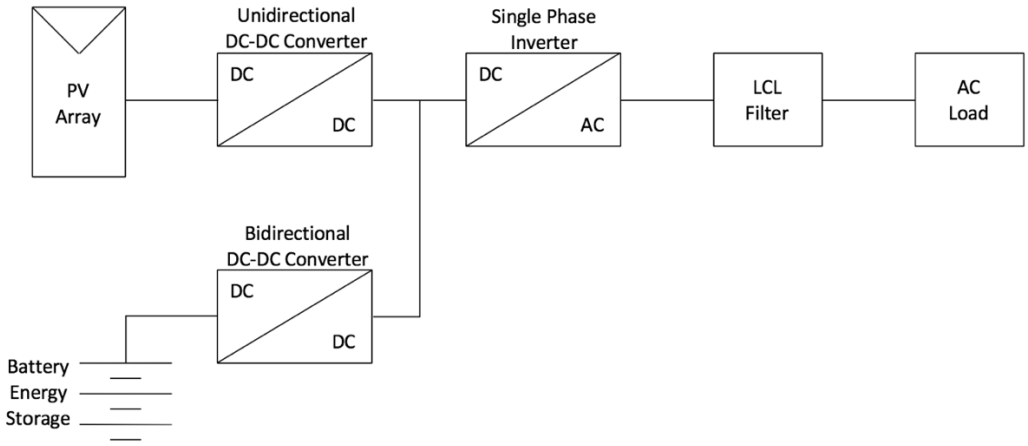


Fig. 3.8 A typical PV power syste

Chapter Four: Proposed Cuk Converter Topologies

4.1 Introduction

Several proposed topologies are investigated in this chapter in order to have a higher voltage gain, reduced voltage stress across the main switch, and higher efficiency compared with many conventional non-isolated DC-DC converters. These topologies include combining the multilevel Cuk converter with a switched-inductor and combining the conventional Cuk converter with switched-inductor (SL) and switched-capacitor (SC) techniques.

4.2 Switched-Inductor Multilevel Cuk Converter

A non-isolated high gain switched-inductor DC-DC multilevel Cuk converter is presented, which combines a switched-inductor with a voltage multiplier. By doing so, the conversion ratio is increased. A high voltage gain cannot be possible if using the traditional Cuk converter. The output voltage can be boosted negatively by using a combination of capacitors and diodes without disturbing the main circuit is the key advantage of the proposed design. This switched-inductor multilevel Cuk converter topology is suitable for photovoltaic application where the voltage is required to be increased with a negative polarity. 2N capacitors, 2N+2 diodes, three inductors, single switch, and single input supply are used to design N level of a switched-inductor multilevel Cuk converter. The proposed converter is designed for three levels. The proposed switched-inductor multilevel

Cuk converter consists of switched-inductor, voltage multiplier (multilevel Cuk converter), and low-pass filter as shown in Fig. 4.1. Fig. 4.2 shows the power circuit diagram of the proposed three levels non-isolated high gain switched-inductor DC-DC multilevel Cuk converter.

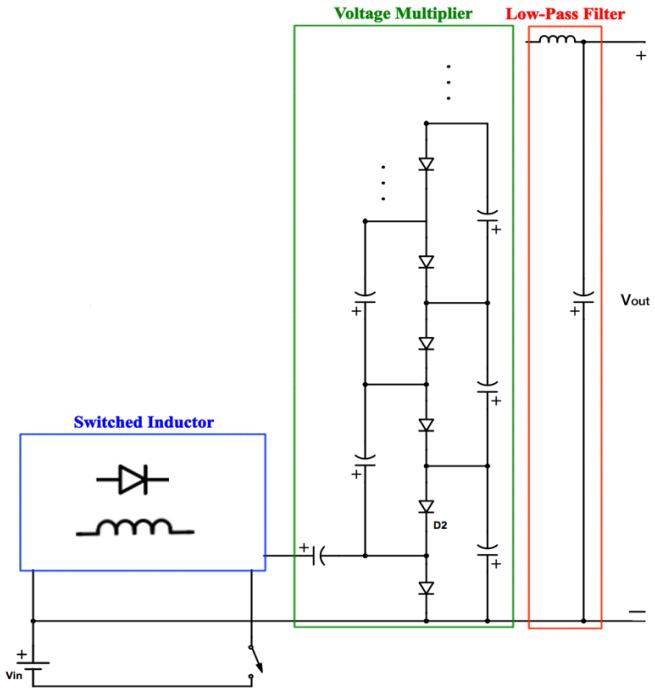


Fig. 4.1 Parts of proposed switched-inductor multilevel Cuk converter

4.2.1 Modes of Operation

The operation of three-level non-isolated high gain switched-inductor DC-DC multilevel Cuk converter has two different scenarios when the switch S_1 is conducting and when it is not.

When switch S_1 is conducting (turned on), both inductors L_1 and L_2 charge in parallel by input supply voltage V_{in} through diodes D_6 and D_8, respectively. When diode D_2 is forward biased, capacitor C_1 is charged by V_{in} and voltage across capacitor C_2 through diode D_2. Likewise, V_{in} and voltage across capacitor C_2 and C_4 charge capacitors C_1 and

C_3 through diode D_4. Finally, inductor L_3 is charged by input supply voltage V_{in} and capacitors C_1, C_3, and C_5 through switch S_1. Fig. 4.3(a)-(c) describe the scenarios when S_1 is conducting.

When switch S_1 is not conducting (turned off), because of energy stored in inductors L_1 and L_2, both diodes D_6 and D_8 are reversed biased. At the same time, both inductors L_1 and L_2 are discharged in series through D_7 which is forward biased. Capacitor C_1 is charged by inductors L_1 and L_2 through diodes D_7 and D_1 when diodes D_7 and D_1 are forward biased. Capacitor C_2 is charged by capacitors C_1, C_3 and voltage across L_1 and L_2 through diodes D_7 and D_3 when D_7 and D_3 are forward biased. Capacitors C_2 and C_4 are charged by capacitors C_1, C_3, C_5, and voltage across L_1 and L_2 through diodes D_7 and D_5 when D_7 and D_5 are forward biased. At the same time inductor L_3 is discharged. Fig. 4.3 (d)-(f) describe the scenarios when S_1 is not conducting.

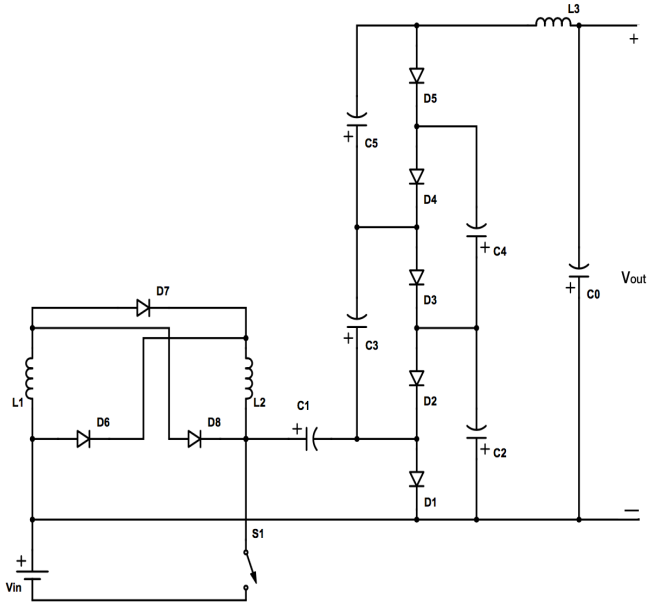


Fig. 4.2 Power circuit diagram of proposed multilevel Cuk converter

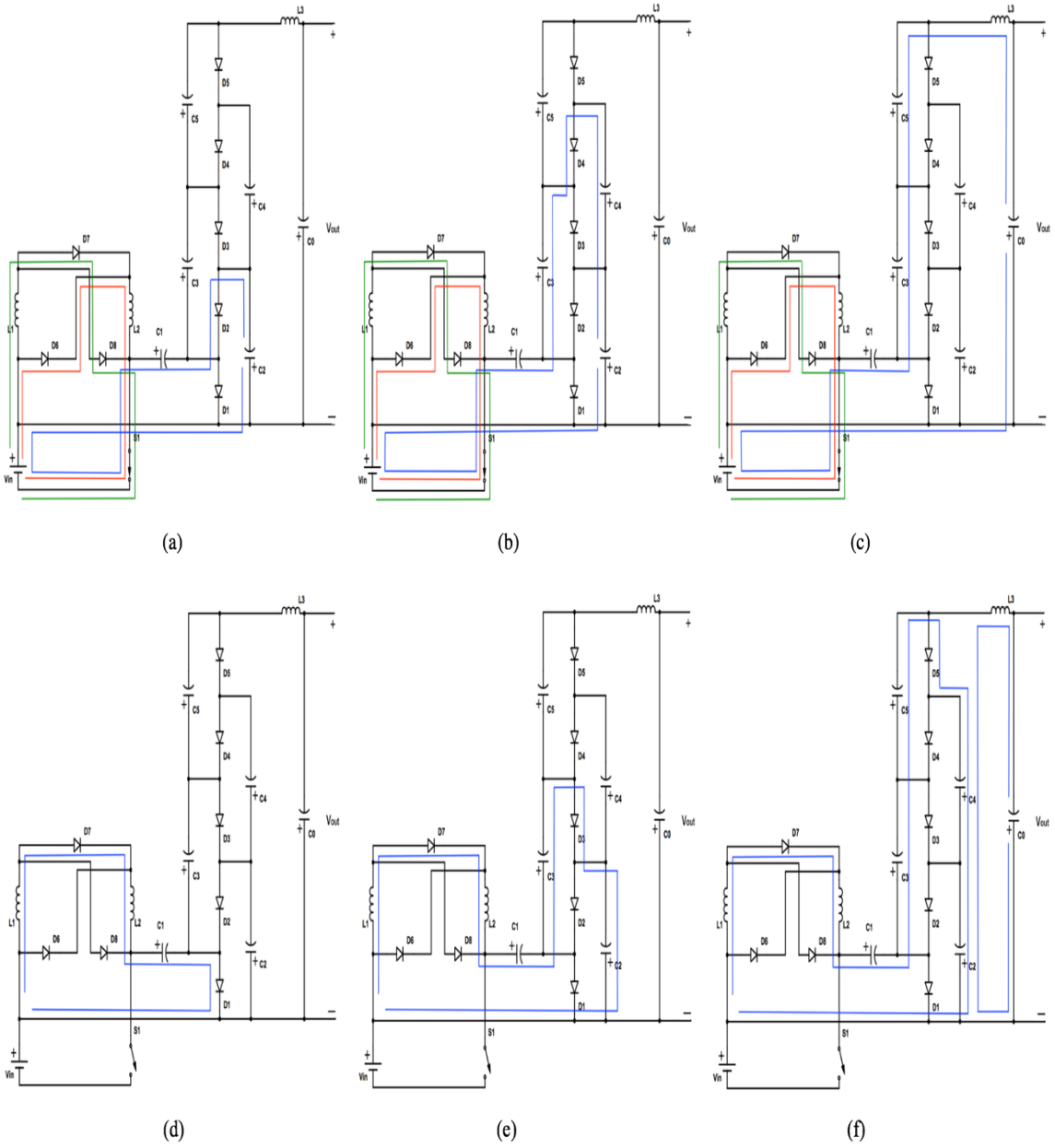


Fig. 4.3 (a)-(c) operation modes when S_1 is conducting (d)-(f) operation modes when S_1 is not conducting

4.2.2 Circuit Analysis

In case of 3-level conventional multilevel Cuk converter with 75% as a duty cycle, the gain reaches -11. However, in the proposed switched- inductor multilevel Cuk

converter, the gain reaches almost -19 which cannot be possible without using switched-inductor.

In the proposed design, when switch S_1 is conducting, L_1 and L_2 are charging in parallel by input supply voltage V_{in}.

$$V_{L_1} = V_{in} \tag{4.1}$$

$$V_{L_2} = V_{in} \tag{4.2}$$

When switch S_1 is not conducting, L_1 and L_2 are discharging in series.

$$-V_{c_1} - V_{L_1} - V_{L_2} = 0 \tag{4.3}$$

$$-V_{c_1} - 2V_L = 0 \tag{4.4}$$

$$V_L = \frac{-V_{C_1}}{2} \tag{4.5}$$

To get the desired power, the load is calculated using equation (4.6).

$$R_{Load} = \frac{V_{out}{}^2}{P} \tag{4.6}$$

The three inductors can be calculated using expression (4.7), where D is the duty cycle, R is the value of the load, and f is the switching frequency.

$$L = \frac{(1 - D)R}{2f} \tag{4.7}$$

4.3 Topology-I

The SLSC Cuk converter topology-I is obtained from the conventional Cuk converter by replacing the input side inductor with a SL and the transferring energy capacitor with a SC. Fig. 4.4 shows the power circuit diagram of the SLSC topology-I. Compared with the Cuk prototype, one inductor, one capacitor, and four diodes are added into the proposed circuit of Fig. 4.4.

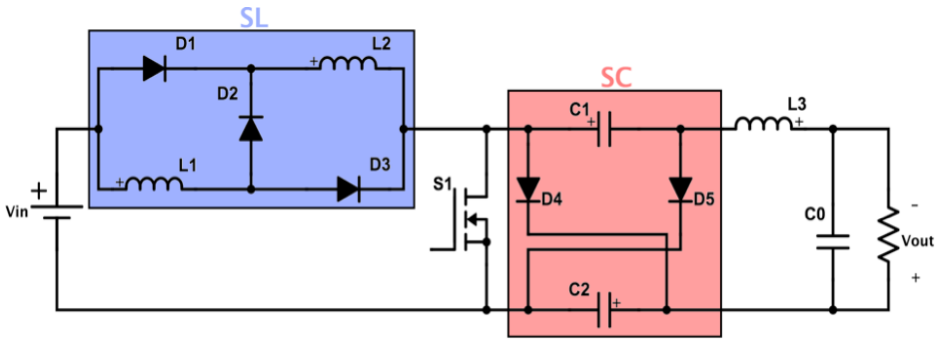


Fig. 4.4 Proposed topology-I SLSC Cuk converter

4.3.1 Modes of Operation

The proposed three topologies SLSC Cuk converters are analyzed in continuous conduction mode (CCM). In CCM, the operation of the proposed three topologies is divided into two modes. The on-mode when switch S_1 is conducting and the off-mode when switch S_1 is not conducting.

When switch S_1 is conducting (turned on), the current direction is shown in Fig. 4.5. Inductors L_1 and L_2 are charged in parallel by input supply voltage V_{in} through diodes D_1, D_3, and switch S_1. Diodes D_2, D_4, and D_5 are reversed-biased. Input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductor L_3 through switch S_1. Equal amount of current flowing through inductors L_1 and L_2 since both inductors are the same.

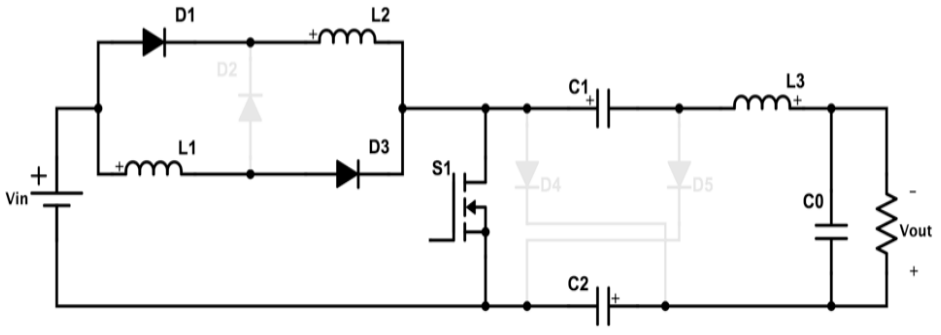


Fig. 4.5 On operation mode of topology-I

When switch S_1 is not conducting (turned off), the current direction is shown in Fig. 4.6. Input supply voltage V_{in} with the discharged energy of inductors L_1 and L_2 charge capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductor L_3 charges capacitors C_1 and C_2 and supplies the load. Diodes D_1 and D_3 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-I are shown in Fig. 4.7.

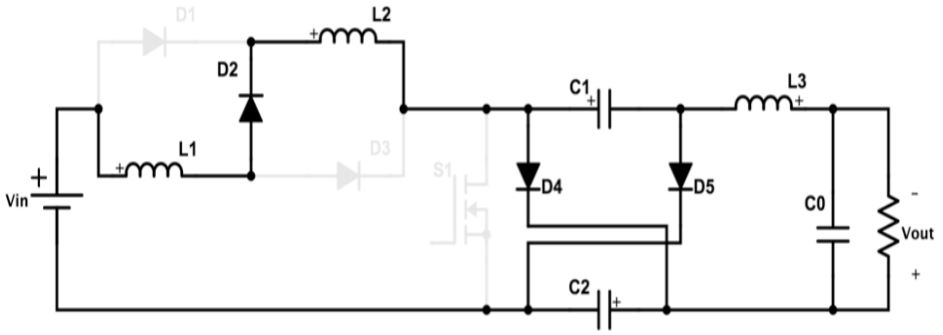


Fig. 4.6 Off operation mode of topology-I

4.3.2 Circuit Analysis

It is assumed that all three topologies SLSC Cuk converters are operating in steady-state to simplify the analysis. Also, the following assumptions are made: all components are ideal (100% efficiency), input voltage V_{in} is a pure DC, and all capacitors are sized to have a relatively small voltage ripple at switching frequency f.

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (4.8) and (4.9). (C_1= C_2=C)

$$V_{L_1} = V_{L_2} = V_{in} \tag{4.8}$$

$$V_{L_3} = 2V_C - V_{out} \tag{4.9}$$

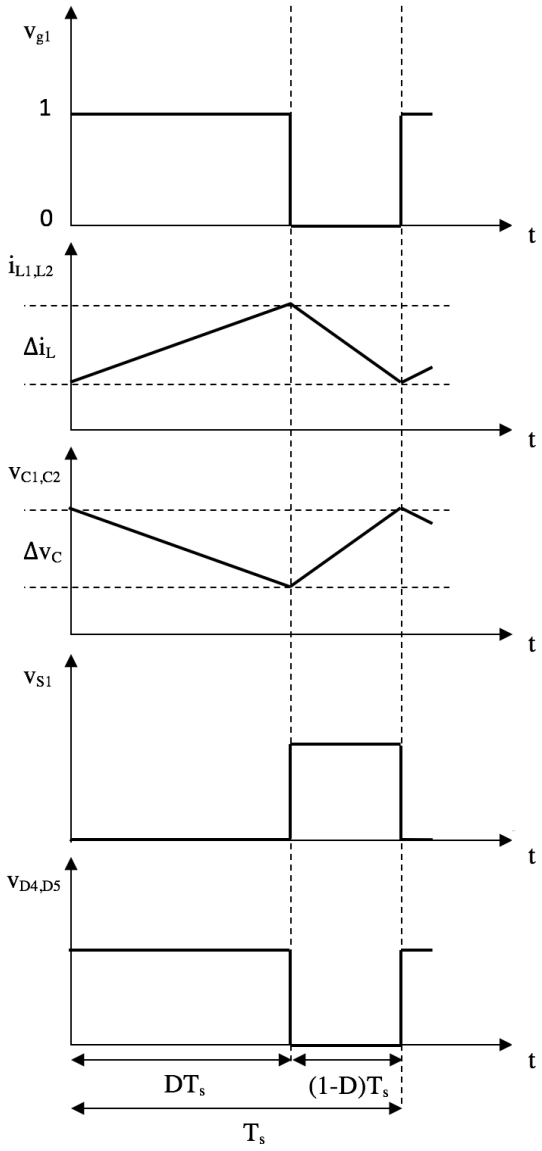


Fig. 4.7 Main steady-state waveforms of topology-I

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (4.10) and (4.11).

$$V_{L_1} = V_{L_2} = \frac{V_{in} - V_C}{2} \tag{4.10}$$

$$V_{L_3} = V_C - V_{out} \tag{4.11}$$

By applying the volt-second method to the inductors L_1, L_2, and L_3 the two expressions in (4.12) and (4.13) can be obtained.

$$V_{in}D + \left(\frac{V_{in} - V_C}{2}\right)(1 - D) = 0 \tag{4.12}$$

$$(2V_C - V_{out})D + (V_C - V_{out})(1 - D) = 0 \tag{4.13}$$

The voltage expression across C_1 and C_2 can be expressed in (4.14).

$$V_C = \frac{(1 + D)}{(1 - D)}V_{in} \tag{4.14}$$

The ideal voltage gain in CCM can be expressed in (4.15).

$$M_{CCM_I} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1 + D)^2}{(1 - D)} \tag{4.15}$$

From Fig. 4.5 and 4.6, it is possible to find an equation to calculate the current of the two input inductors. Because the two input inductors have the same inductance values, $I_{L_1} = I_{L_2} = I_{L_{in}}$ is obtained in (4.17) from (4.16).

$$I_{in} = 2I_{L_{in}}D + I_{L_{in}}(1 - D) \tag{4.16}$$

$$I_{L_{in}} = \frac{I_{in}}{(1 + D)} = \frac{P_{out}}{(1 + D)V_{in}} \tag{4.17}$$

Capacitor C_O acts as low-pass filter, so (4.18) is obtained for $I_{L_3} = I_{L_{out}}$.

$$I_{L_{out}} = I_{out} = \frac{P_{out}}{V_{out}} \tag{4.18}$$

The reverse voltage across D_1 and D_3 applied when they are blocked (off-mode) is expressed in (4.19).

$$V_{D_1} = V_{D_3} = \frac{D}{(1 - D)}V_{in} \tag{4.19}$$

The reverse voltage across D_2 applied when it is blocked (on-mode) is expressed in (4.20).

$$V_{D_2} = V_{in} \tag{4.20}$$

The reverse voltage across D_4 and D_5 of the SC applied when they are blocked (on-mode) is expressed in (4.21).

$$V_{D_4} = V_{D_5} = \frac{(1+D)}{(1-D)} V_{in} \tag{4.21}$$

The voltage stress across the power switch S_1 when it is blocked (off-mode) is expressed in (4.22).

$$V_{S_1} = \frac{(1+D)}{(1-D)} V_{in} \tag{4.22}$$

The peak-to-peak variation of the inductor's current at the input $\left(\Delta i_{L_1} = \Delta i_{L_2} = \Delta i_{L_{in}}\right)$ and output $\left(\Delta i_{L_3} = \Delta i_{L_{out}}\right)$ sides are expressed in (4.23) and (4.24), respectively.

$$\Delta i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{4.23}$$

$$\Delta i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{4.24}$$

The peak-to-peak variation of the capacitor's voltage $\left(\Delta v_{C_1} = \Delta v_{C_2} = \Delta v_C\right)$ is expressed in (4.25).

$$\Delta v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_I} V_{in} fC} \tag{4.25}$$

4.4 Topology-II

The SLSC Cuk converter topology-II is obtained from the conventional Cuk converter by replacing the output side inductor with a SL and the transferring energy

capacitor with a SC. Fig. 4.8 shows the power circuit diagram of the SLSC Cuk converter topology-II. Compared with the Cuk prototype, one inductor, one capacitor, and four diodes are added into the proposed circuit of Fig. 4.8.

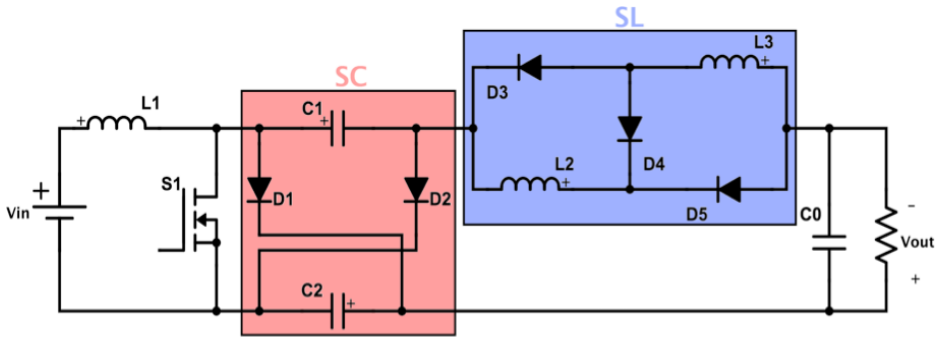


Fig. 4.8 Proposed topology-II SLSC Cuk converter

4.4.1 Modes of Operation

When switch S_1 is conducting, the current direction is shown in Fig. 4.9. Inductor L_1 is charged by input supply voltage V_{in} through switch S_1. Input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductors L_2 and L_3 which is connected in parallel through diodes D_3, D_5, and switch S_1. Diodes D_1, D_2, and D_4 are reversed-biased. Equal amount of current flowing through inductors L_2 and L_3 since both inductors are the same.

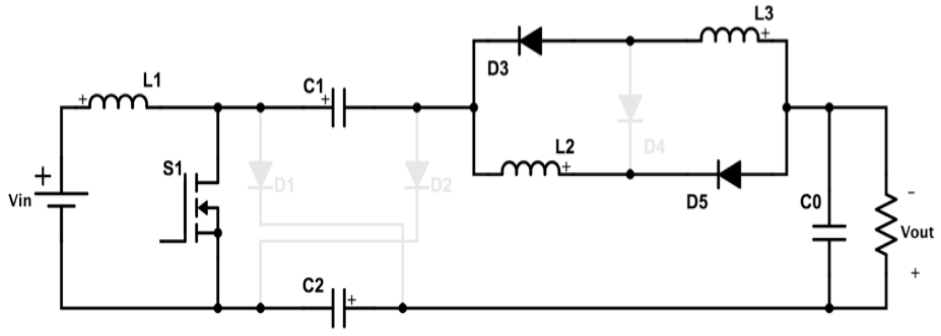


Fig. 4.9 On operation mode of topology-II

When switch S_1 is not conducting, the current direction is shown in Fig. 4.10. The input supply voltage V_{in} and the discharged energy of inductor L_1 charge capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductors L_2 and L_3 charges capacitors C_1 and C_2 and supplies the load. Diodes D_3 and D_5 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-II are shown in Fig. 4.11.

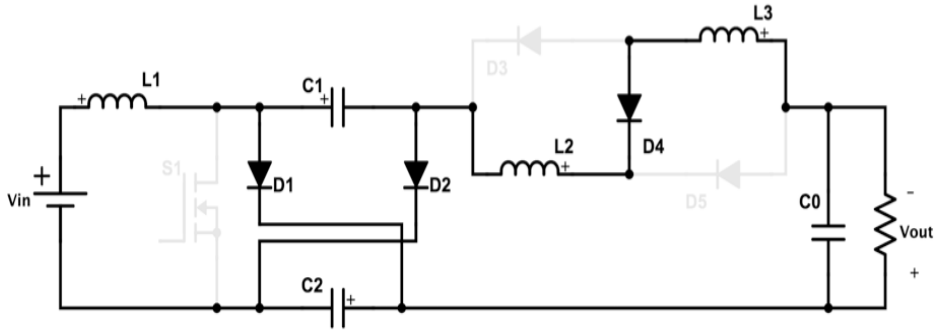


Fig. 4.10 Off operation mode of topology-II

4.4.2 Circuit Analysis

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (4.26) and (4.27). (C_1=C_2=C)

$$V_{L_1} = V_{in} \tag{4.26}$$

$$V_{L_2} = V_{L_3} = 2V_C - V_{out} \tag{4.27}$$

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, and L_3 are expressed in (4.28) and (4.29).

$$V_{L_1} = V_{in} - V_C \tag{4.28}$$

$$V_{L_2} = V_{L_3} = \frac{V_C - V_{out}}{2} \tag{4.29}$$

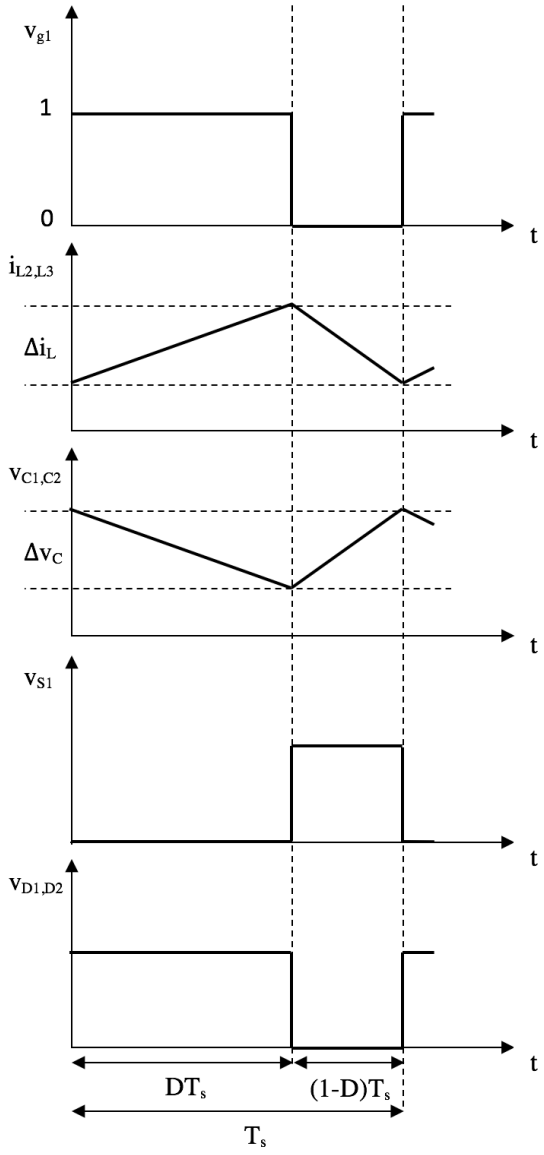


Fig. 4.11 Main steady-state waveforms of topology-II

By applying the volt-second method to the inductors L_1, L_2, and L_3 the two expressions in (4.30) and (4.31) can be obtained.

$$V_{in}D + (V_{in} - V_C)(1 - D) = 0 \tag{4.30}$$

$$(2V_C - V_{out})D + \left(\frac{V_C - V_{out}}{2}\right)(1 - D) = 0 \tag{4.31}$$

The voltage expression across C_1 and C_2 can be obtained in (4.32).

$$V_C = \frac{1}{(1-D)} V_{in} \tag{4.32}$$

The ideal voltage gain in CCM can be expressed in (4.33).

$$M_{CCM_{II}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1+3D)}{(1+D)(1-D)} \tag{4.33}$$

The input inductor current $\left(I_{L_1} = I_{L_{in}}\right)$ is obtained in (4.34) from (4.33).

$$I_{L_{in}} = I_{in} = \frac{(1+3D)}{(1+D)(1-D)} I_{out} = \frac{(1+3D)P_{out}}{(1+D)(1-D)V_{out}} \tag{4.34}$$

From Fig. 4.9 and 4.10, it is possible to find an equation to calculate the current of the two output inductors. Because the two output inductors have the same inductance values, $I_{L_2} = I_{L_3} = I_{L_{out}}$ is obtained in (4.36) from (4.35).

$$I_{out} = 2I_{L_{out}} D + I_{L_{out}}(1-D) \tag{4.35}$$

$$I_{L_{out}} = \frac{I_{out}}{(1+D)} = \frac{P_{out}}{(1+D)V_{out}} \tag{4.36}$$

The reverse voltage across D_1 and D_2 of the SC applied when they are blocked (on-mode) is expressed in (4.37).

$$V_{D_1} = V_{D_2} = \frac{1}{(1-D)} V_{in} \tag{4.37}$$

The voltage stress across the power switch S_1 when it is blocked (off-mode) is expressed in (4.38).

$$V_{S_1} = \frac{1}{(1-D)} V_{in} \tag{4.38}$$

The reverse voltage across D_3 and D_5 applied when they are blocked (off-mode) is expressed in (4.39).

$$V_{D_3} = V_{D_5} = \frac{D}{(1+D)(1-D)} V_{in} \tag{4.39}$$

The reverse voltage across D_4 applied when it is blocked (on-mode) is expressed in (4.40).

$$V_{D_4} = \frac{1}{(1+D)} V_{in} \tag{4.40}$$

The peak-to-peak variation of the inductor's current at the input $\left(\Delta i_{L_1} = \Delta i_{L_{in}}\right)$ and output $\left(\Delta i_{L_2} = \Delta i_{L_3} = \Delta i_{L_{out}}\right)$ sides are expressed in (4.41) and (4.42), respectively.

$$\Delta i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{4.41}$$

$$\Delta i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{4.42}$$

The peak-to-peak variation of the capacitor's voltage $\left(\Delta v_{C_1} = \Delta v_{C_2} = \Delta v_C\right)$ is expressed in (4.43).

$$\Delta v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_{II}} V_{in} fC} \tag{4.43}$$

4.5 Topology-III

The SLSC Cuk converter topology-III is obtained from the conventional Cuk converter by replacing both the input and output side inductors with two SLs and the transferring energy capacitor with a SC. Fig. 4.12 shows the power circuit diagram of the SLSC Cuk converter topology-III. Compared with the Cuk prototype, two inductors, one capacitor, and seven diodes are added into the proposed circuit of Fig. 4.12.

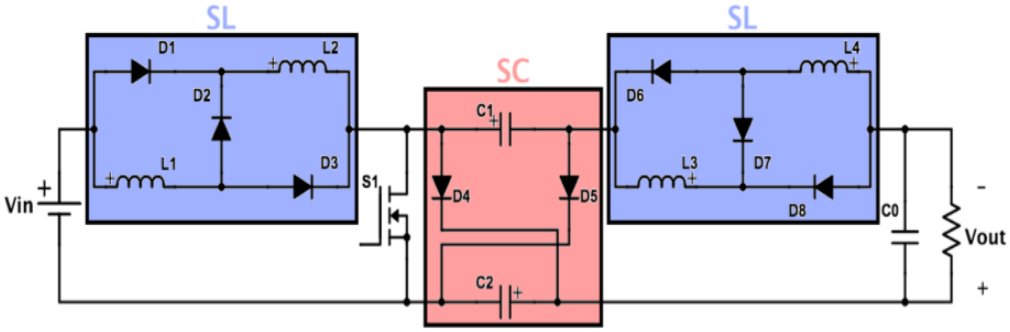


Fig. 4.12 Proposed topology-III SLSC Cuk converter

4.5.1 Modes of Operation

When switch S_1 is conducting, the current direction is shown in Fig. 4.13. Inductors L_1 and L_2 are charged in parallel by the input supply voltage V_{in} through diodes D_1, D_3, and switch S_1. On the other hand, the input supply voltage V_{in} with the discharged energy of capacitors C_1 and C_2 supply the load and charge inductors L_3 and L_4 connected in parallel through diodes D_6, D_8, and switch S_1. Diodes D_2, D_4, D_5, and D_7 are reversed-biased. An equal amount of current flowing through inductors L_1 and L_2 since both inductors are the same. Likewise, an equal amount of current flowing through inductors L_3 and L_4 since both inductors are the same.

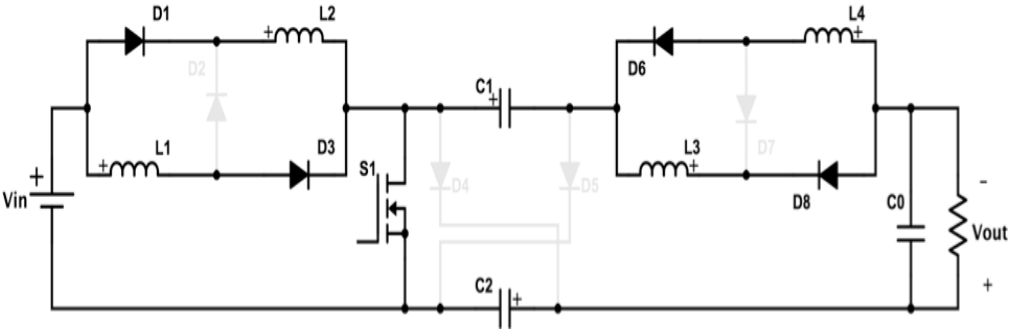


Fig. 4.13 On operation mode of topology-III

When switch S_1 is not conducting, the current direction is shown in Fig. 4.14. The input supply voltage V_{in} with the discharged energy of inductors L_1 and L_2 charge

capacitors C_1 and C_2 connected in parallel. Likewise, the discharged energy of inductors L_3 and L_4 charges capacitors C_1 and C_2 and supplies the load. Diodes D_1, D_3, D_6, and D_8 are reversed-biased. Switching diagrams in CCM of the main steady-state waveforms with enlarged variations for the SLSC topology-III are shown in Fig. 4.15.

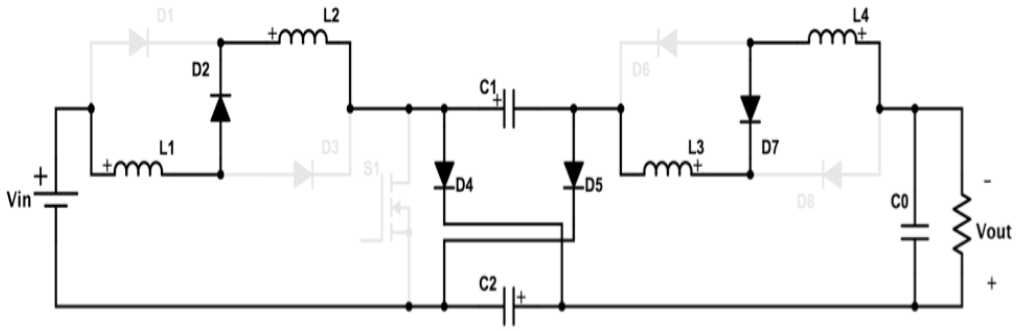


Fig. 4.14 Off operation mode of topology-III

4.5.2 Circuit Analysis

When MOSFET S_1 is conducting, the voltage across inductors L_1, L_2, and L_3, and L_4 are expressed in (4.44) and (4.45). (C_1=C_2=C)

$$V_{L_1} = V_{L_2} = V_{in} \tag{4.44}$$

$$V_{L_3} = V_{L_4} = 2V_C - V_{out} \tag{4.45}$$

When MOSFET S_1 is not conducting, the voltage across inductors L_1, L_2, and L_3, and L_4 are expressed in (4.46) and (4.47).

$$V_{L_1} = V_{L_2} = \frac{V_{in} - V_C}{2} \tag{4.46}$$

$$V_{L_3} = V_{L_4} = \frac{V_C - V_{out}}{2} \tag{4.47}$$

By applying the volt-second method to the inductors L1, L2, and L3, and L4, the two expressions in (4.48) and (4.49) can be obtained.

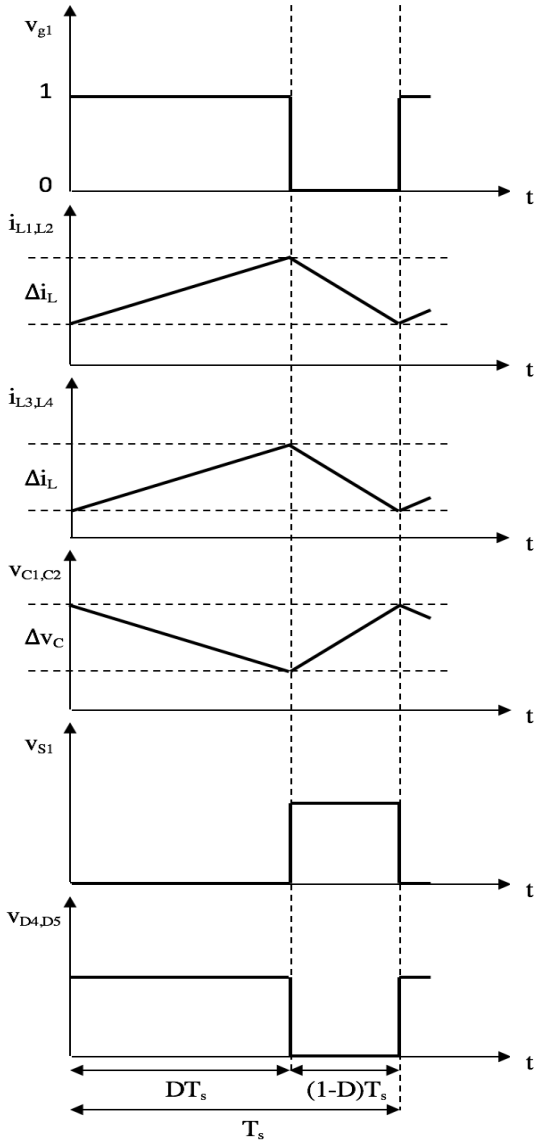


Fig. 4.15 Main steady-state waveforms of topology-III

$$V_{in}D + \left(\frac{V_{in} - V_C}{2}\right)(1 - D) = 0 \tag{4.48}$$

$$(2V_C - V_{out})D + \left(\frac{V_C - V_{out}}{2}\right)(1 - D) = 0 \tag{4.49}$$

The voltage expression across C_1 and C_2 can be obtained in (4.50).

$$V_C = \frac{(1+D)}{(1-D)} V_{in} \tag{4.50}$$

The ideal voltage gain in CCM can be expressed in (4.51).

$$M_{CCM_{III}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1+3D)}{(1-D)} \tag{4.51}$$

From Fig. 4.13 and 4.14 and as done in (4.16) and (4.35), $I_{L_1} = I_{L_2} = I_{L_{in}}$ and $I_{L_3} = I_{L_4} = I_{L_{out}}$ are expressed in (4.52) and (4.53), respectively.

$$I_{L_{in}} = \frac{I_{in}}{(1+D)} = \frac{P_{out}}{(1+D)V_{in}} \tag{4.52}$$

$$I_{L_{out}} = \frac{I_{out}}{(1+D)} = \frac{P_{out}}{(1+D)V_{out}} \tag{4.53}$$

The reverse voltage across D_1, D_3, D_6 and D_8 applied when they are blocked (off-mode) is expressed in (4.54).

$$V_{D_1} = V_{D_3} = V_{D_6} = V_{D_8} = \frac{D}{(1-D)} V_{in} \tag{4.54}$$

The reverse voltage across D_2 and D_7 applied when they are blocked (on-mode) is expressed in (4.55).

$$V_{D_2} = V_{D_7} = V_{in} \tag{4.55}$$

The reverse voltage across D_4 and D_5 of the SC applied when they are blocked (on-mode) is expressed in (4.56).

$$V_{D_4} = V_{D_5} = \frac{(1+D)}{(1-D)} V_{in} \tag{4.56}$$

The voltage stress across the power switch S_1 when it is blocked (off-mode) is expressed in (4.57).

$$V_{S_1} = \frac{(1+D)}{(1-D)} V_{in} \tag{4.57}$$

The peak-to-peak variation of the inductor's current at the input $\left(\Delta i_{L_1} = \Delta i_{L_2} = \Delta i_{L_{in}}\right)$ and output $\left(\Delta i_{L_3} = \Delta i_{L_4} = \Delta i_{L_{out}}\right)$ sides are expressed in (4.58) and (4.59), respectively.

$$\Delta i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{4.58}$$

$$\Delta i_{L_{out}} = \frac{DT(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{fL_{out}} \tag{4.59}$$

The peak-to-peak variation of the capacitor's voltage $\left(\Delta v_{C_1} = \Delta v_{C_2} = \Delta v_C\right)$ is expressed in (4.60).

$$\Delta v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM_{III}} V_{in} fC} \tag{4.60}$$

4.6 Two-Switch Cuk Converter

To perform the proposed Cuk converter a MOSFET, diode, capacitor, and an inductor have been added to the conventional Cuk converter to maintain a high voltage gain and low voltage stress as shown in Fig. 4.16. A MOSFET and inductor are added to perform the switched-inductor in which the two inductors are charged in parallel when the two MOSFETs are on, and they get discharged in series when the two MOSFETs are off. Moreover, a diode and capacitor are added to perform the switched-capacitor in which the two capacitors are discharged in series when the two MOSFETs are on, and they get charged in parallel when the two MOSFETs are off.

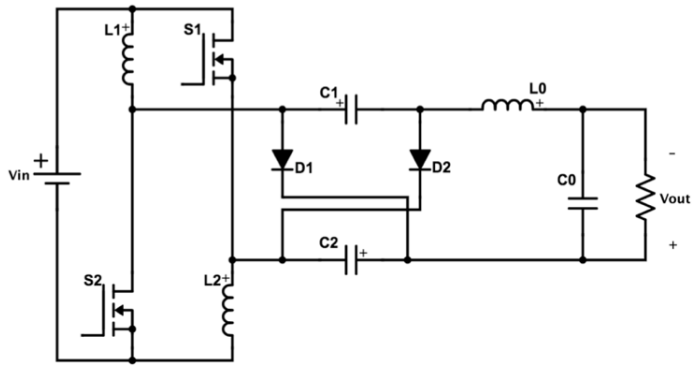


Fig. 4.16 Proposed two-switch Cuk converter

4.6.1 Modes of Operation

The proposed Cuk converter is analyzed in continuous conduction mode (CCM). The operation of the proposed converter is either both the two MOSFETs are simultaneously on or off. Thus, two modes of operation are existed.

When the two MOSFETs S_1 and S_2 are simultaneously on, the two inductors L_1 and L_2 get charged in parallel by the input voltage source V_{in} as shown in Fig. 4.17. The two diodes D_1 and D_2 are reversed biased and the two capacitors C_1 and C_2 of the switched-capacitor get discharged in series. The input voltage V_{in} and the discharged energy from the two capacitors charge the output inductor L_{out} and supply the load.

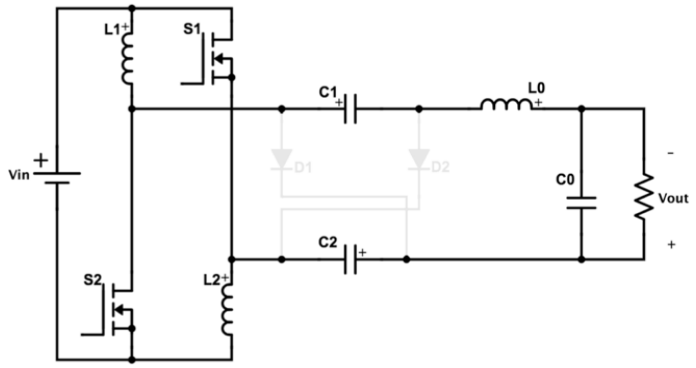


Fig. 4.17 Proposed two switch-Cuk converter in on-mode

When the two MOSFETs S_1 and S_2 are simultaneously off, the two inductors L_1 and L_2 get discharged in series to supply the load and charge the two capacitors C_1 and C_2 which are connected in parallel as shown in Fig. 4.18. Also, the output inductor L_{out} will discharge through the load and charge the two capacitors C_1 and C_2. The switching diagram of the steady-state waveforms with enlarged variations in CCM of the proposed Cuk converter is shown in Fig. 4.19.

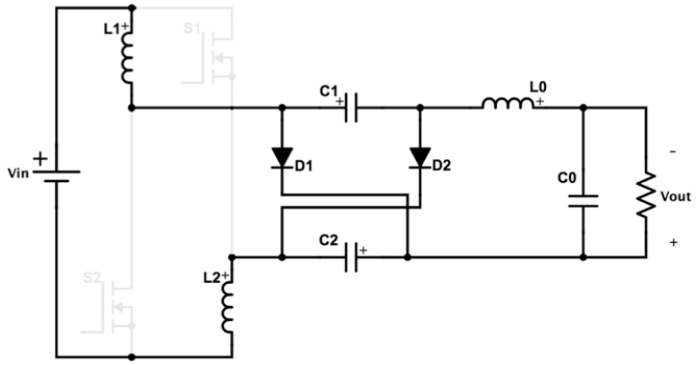


Fig. 4.18 Proposed two-switch Cuk converter in off-mode

4.6.2 Circuit Analysis

To simplify the analysis, it is assumed that the proposed Cuk converter is operating in steady-state. Likewise, the following assumptions are made: all components are ideal (100% efficiency), input voltage V_{in} is a pure DC, and all capacitors C_1, C_2, and C_{out} are sized to have a relatively small voltage ripple at a switching frequency (f).

When the two MOSFETs S_1 and S_2 are on, the voltages across the inductors L_1, L_2, and L_{out} are expressed in (4.61) and (4.62). (C_1=C_2=C)

$$V_{L_1} = V_{L_2} = V_{in} \tag{4.61}$$

$$V_{L_{out}} = V_{in} + 2V_C - V_{out} \tag{4.62}$$

Where V_C stands for the voltage across capacitors C_1 and C_2.

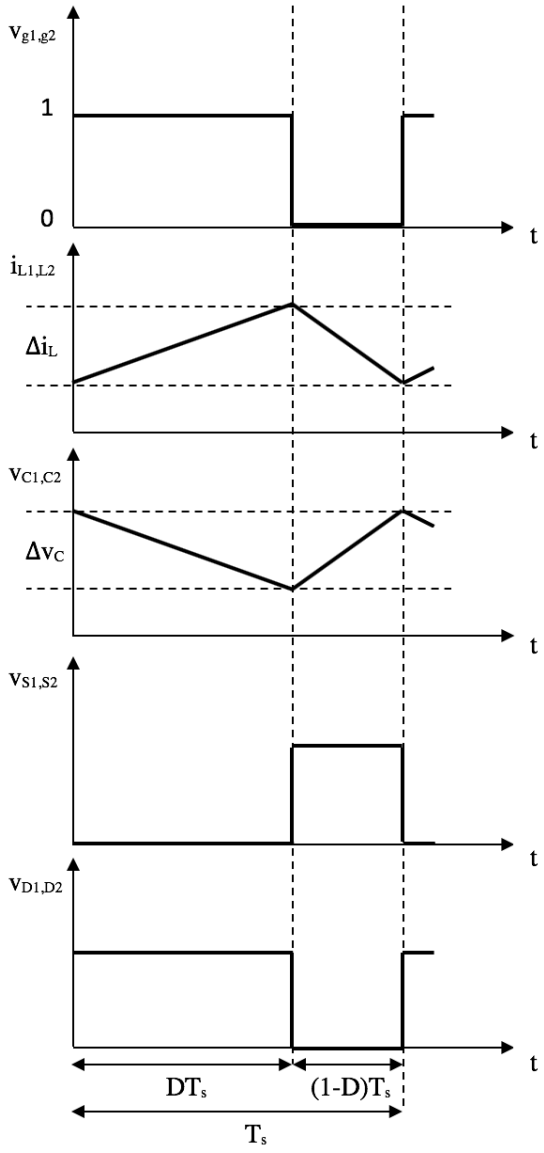


Fig. 4.19 Main steady-state waveforms of proposed two-switch Cuk converter

When the two MOSFETs S_1 and S_2 are off, the voltage across the inductors L_1, L_2, and L_{out} are expressed in (4.63) and (4.64).

$$V_{L_1} = V_{L_2} = \frac{V_{in} - V_C}{2} \tag{4.63}$$

$$V_{L_{out}} = V_C - V_{out} \tag{4.64}$$

The two expressions in (4.65) and (4.66) can be obtained by applying the volt-second method to the inductors L_1, L_2, and L_{out}.

$$V_{in}D + \left(\frac{V_{in} - V_C}{2}\right)(1 - D) = 0 \tag{4.65}$$

$$(V_{in} + 2V_C - V_{out})D + (V_C - V_{out})(1 - D) = 0 \tag{4.66}$$

From (4.65), The voltage across C_1 and C_2 is expressed in (4.67).

$$V_C = \frac{(1 + D)}{(1 - D)} V_{in} \tag{4.67}$$

By substituting (4.67) into (4.66), the ideal voltage gain in CCM for the proposed Cuk converter is expressed in (4.68).

$$M_{CCM} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{(1 + 3D)}{(1 - D)} \tag{4.68}$$

The output inductor average current $I_{L_{out}}$ can be considered equal to the output average current I_{out}. Therefore, (4.69) is obtained form (4.68).

$$I_{L_{out}} = I_{out} = \frac{(1 - D)}{(1 + 3D)} I_{in} \tag{4.69}$$

Also, the input inductor currents can be obtained in (4.71) by using (4.70).

$$I_{in} = \left(2I_L + I_{L_{out}}\right)D + I_L(1 - D) \tag{4.70}$$

$$I_L = I_{L_1} = I_{L_2} = \frac{(1 + D)}{(1 + 3D)} I_{in} = \frac{(1 + D)P_{out}}{(1 + 3D)V_{in}} \tag{4.71}$$

The voltage stress across the two diodes D_1 and D_2 are expressed in (4.72).

$$V_{D_1} = V_{D_2} = \frac{2}{(1 - D)} V_{in} \tag{4.72}$$

The voltage stress across the two MOSFETs S_1 and S_2 are expressed in (4.73).

$$V_{S_1} = V_{S_2} = \frac{1}{(1-D)} V_{in} \tag{4.73}$$

The peak-to-peak variation in input inductor's currents $\left(\Delta i_{L_{in}} = \Delta i_{L_1} = \Delta i_{L_2}\right)$ is expressed in (4.74).

$$\Delta i_{L_{in}} = \frac{DTV_{in}}{L_{in}} = \frac{DV_{in}}{fL_{in}} \tag{4.74}$$

The peak-to-peak variation in output inductor's current $\Delta i_{L_{out}}$ is expressed in (4.75).

$$\Delta i_{L_{out}} = \frac{DT(V_{in} + 2V_C - V_{out})}{L_{out}} = \frac{D(V_{in} + 2V_C - V_{out})}{fL_{out}} \tag{4.75}$$

The peak-to-peak variation in capacitor's voltage Δv_C is expressed in (4.76).

$$\Delta v_C = \frac{DTI_{out}}{C} = \frac{DP_{out}}{M_{CCM} V_{in} fC} \tag{4.76}$$

4.6.3 Circuit Extensions

More switched-inductors can be attached to the proposed Cuk converter instead of the single inductors at the input side. This will lead to increase the voltage gain ratio even more. Also, to reduce the size of magnetic components, the inductors can be integrated into one magnetic core.

In order to increase the voltage gain even more, the single inductors at the input side of the proposed Cuk converter can be replaced with a switched-inductor. In this case, the voltage gain reaches more than 23. The power circuit is shown in Fig. 4.20.

The voltage gain can be expressed as in (4.77).

$$M_{CCM} = \frac{V_{out}}{V_{in}} = D + (1+D)\frac{(1+3D)}{(1-D)} \tag{4.77}$$

Actually, all the inductors presented in the last section share the same value of inductance and have the same operation condition. Therefore, to reduce the size of magnetic components, the inductors can be integrated into one magnetic core as shown in Fig. 4.21.

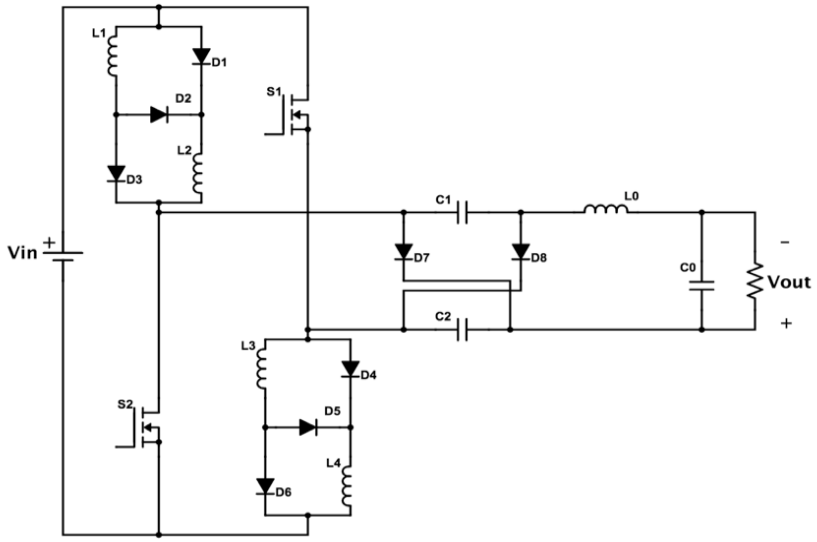


Fig. 4.20 More switched-inductors attached

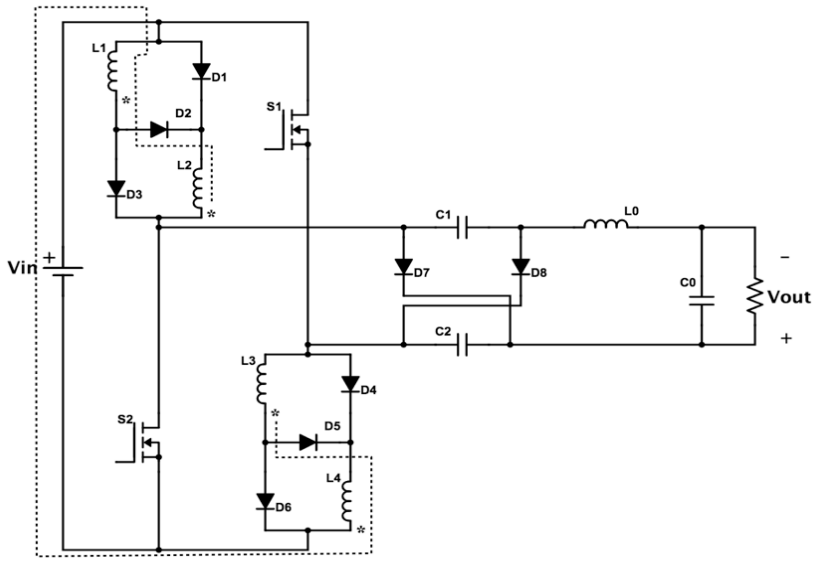


Fig. 4.21 Magnetic components integration

Chapter Five: Comparison Analysis

5.1 Introduction

In this chapter, a comparison has been made between different levels of multilevel Cuk converter based on voltage gain. Also, a comparison has been made between the proposed three topologies SLSC Cuk converters with the conventional Cuk and boost converters based on voltage gain and voltage stress on the main switch. Furthermore, a voltage gain and voltage stress comparisons have been made between the proposed two-switch Cuk converter and other Cuk converters used different techniques. Finally, a cost analysis comparison has been presented.

5.2 Switched-Inductor Multilevel Cuk Converter

Fig. 5.1 shows the voltage gain versus duty cycle for different levels ranging from 1 to 5. Obviously, as more voltage multipliers are added as the voltage gain increases. A comparison is made between 3-level conventional multilevel Cuk converter and the proposed 3-level switched-inductor multilevel Cuk converter as shown in Fig. 5.2. As can be observed, the proposed 3-level multilevel Cuk converter has a higher voltage gain compared with the 3-level conventional multilevel Cuk converter.

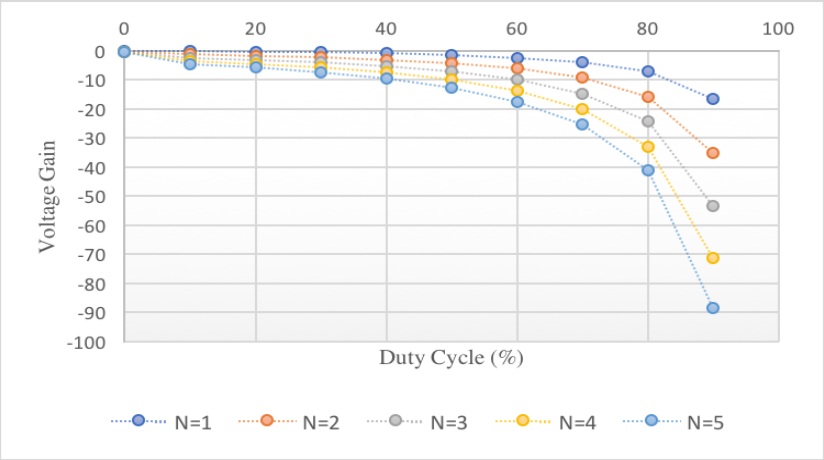


Fig. 5.1 Voltage gain versus duty cycle for different levels

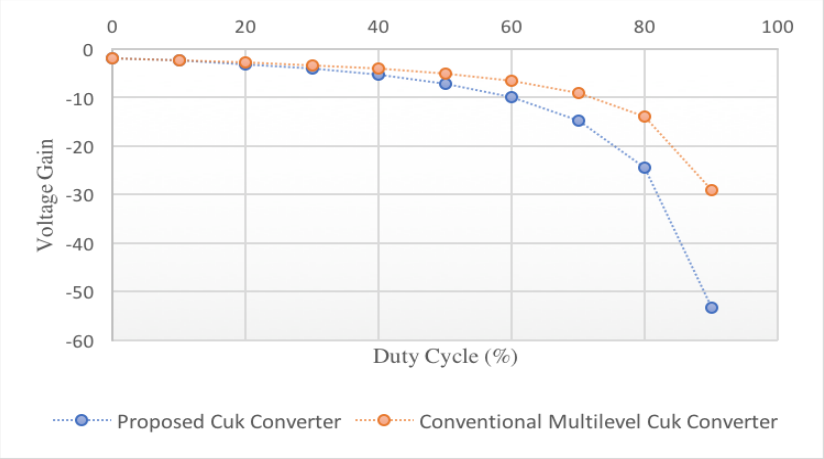


Fig. 5.2 A comparison between proposed and conventional Cuk converter

5.3 Three Topologies of Cuk Converter

A voltage gain comparison has been made between the proposed three topologies SLSC Cuk converters with the conventional boost and Cuk converters as given in Table 5.1 in terms of the number of active switches, diodes, inductors, capacitors, and the voltage gain. The voltage gain is graphically represented in Fig. 5.3.

Table 5.1 Comparison between boost Converter, Cuk Converter, and three proposed Converters

Topology	Boost	Cuk	Topology-I	Topology-II	Topology-III
Active Switches	1	1	1	1	1
Diodes	1	1	5	5	8
Inductors	1	2	3	3	4
Capacitors	1	2	3	3	3
Voltage Gain	$\frac{1}{(1-D)}$	$\frac{D}{(1-D)}$	$\frac{(1+D)^2}{(1-D)}$	$\frac{(1+3D)}{(1+D)(1-D)}$	$\frac{(1+3D)}{(1-D)}$

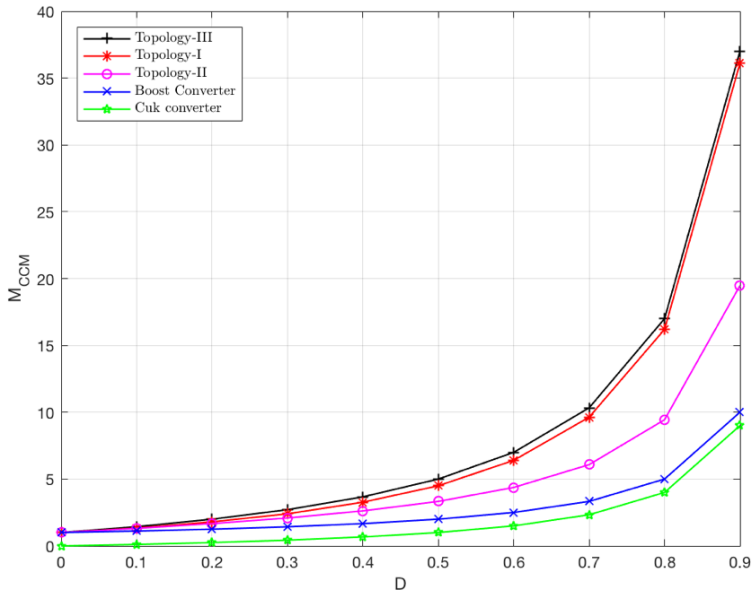


Fig. 5.3 Voltage gain comparison

A voltage gain comparison has been made between the proposed three topologies Cuk converters and other Cuk converters using different techniques, such as a conventional Cuk converter, single-switch high voltage Cuk converter [51], hybrid switched-capacitor Cuk converter [52], Enhanced Self-lift Cuk converter [20], self-lift Cuk converter using voltage lift technique [55], and conventional boost converter. As shown in Fig. 5.4, the Single-switch Cuk converter has a higher voltage gain for duty cycles less than 0.3, but

topology-I and topology-III Cuk converters have a higher voltage gain among all other Cuk converters for duty cycles higher than 0.3.

The normalized voltage stress $\left({}^{V_S}/_{V_{in}}\right)$ on the main switch which describes the voltage stress across semiconductor device MOSFET S_1 of these three topologies is compared with those in the conventional Cuk and boost converters and graphically represented in Fig. 5.5. As can be observed the three topologies have a lower voltage stress and the lowest is topology-II.

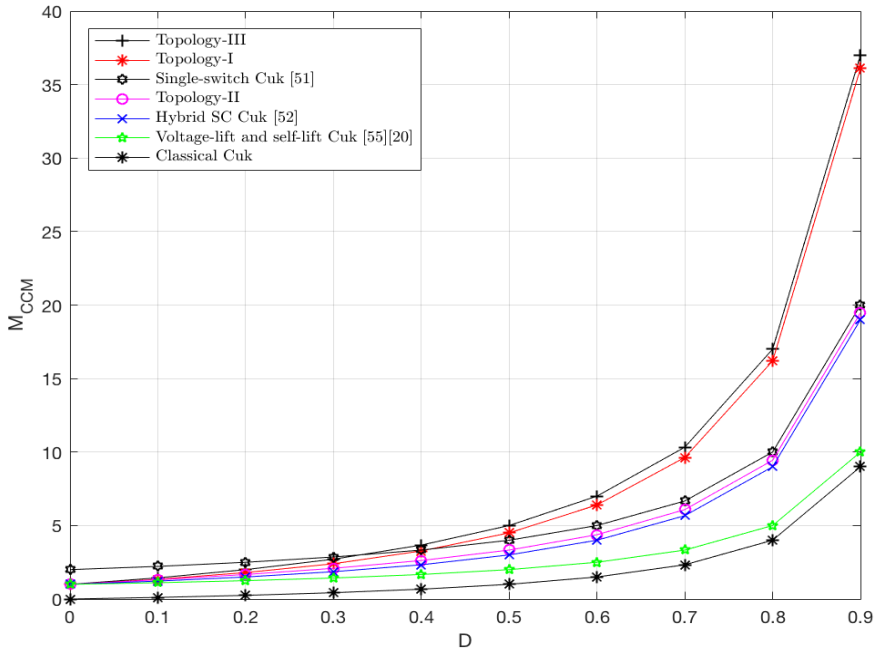


Fig. 5.4 Voltage gain comparison

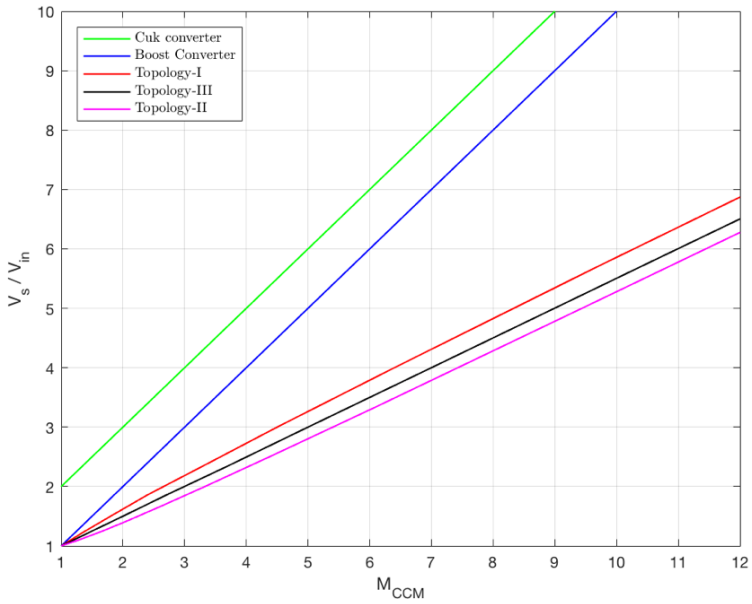


Fig. 5.5 Voltage stress comparison on active switch S_1

5.4 Two-Switch Cuk Converter

A comparison has been made between the proposed two-switch Cuk converter, single-switch Cuk converter [51], hybrid switched-capacitor Cuk converter [52], three-switch Cuk converter [54], and conventional Cuk converter in terms of the voltage gain, voltage stress, and number of components as described in Table 5.2. The voltage gain and the normalized voltage stress $\left({}^{V_S}/_{V_{in}}\right)$ are graphically represented in Fig. 5.6 and Fig. 5.7, respectively.

As can be observed in Fig. 5.6, the highest voltage gain can be accomplished by using the proposed Cuk converter. However, the converter having the lowest voltage gain is the conventional Cuk converter. Single-switch Cuk converter has a higher voltage gain

for duty cycles less than 0.3. However, the proposed two-switch Cuk converter has a higher voltage gain for duty cycles larger than 0.3.

Table 5.2 Comparison between proposed two-switch Cuk converter and other Cuk converters

Cuk Converters	Gain (M_{CCM})	Switches count	Diodes count	Capacitors count	Inductors count
Proposed	$\frac{(1+3D)}{(1-D)}$	2	2	3	2
Single-Switch [45]	$\frac{2}{(1-D)}$	1	3	3	1
Hybrid SC [46]	$\frac{(1+D)}{(1-D)}$	1	2	3	2
Three-Switch [48]	$\frac{1}{(1-D)}$	1	2	2	1
Conventional Cuk	$\frac{D}{(1-D)}$	1	1	2	2

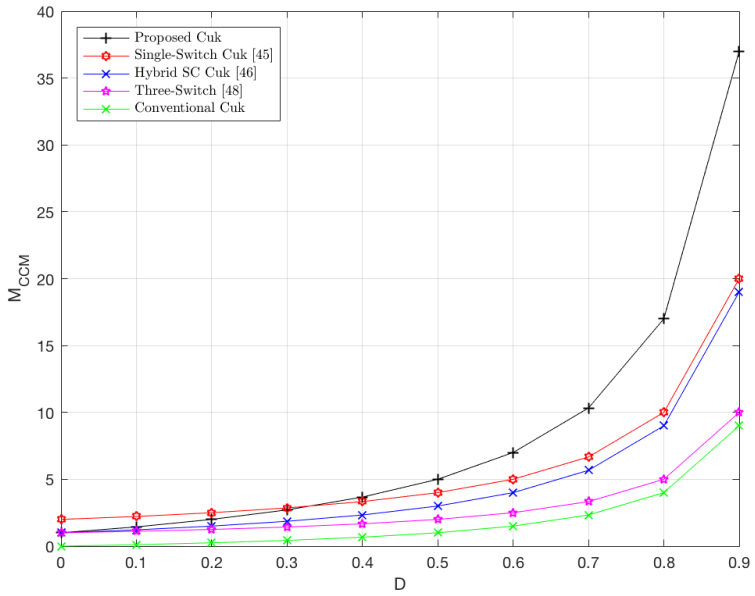


Fig. 5.6 Voltage gain comparison

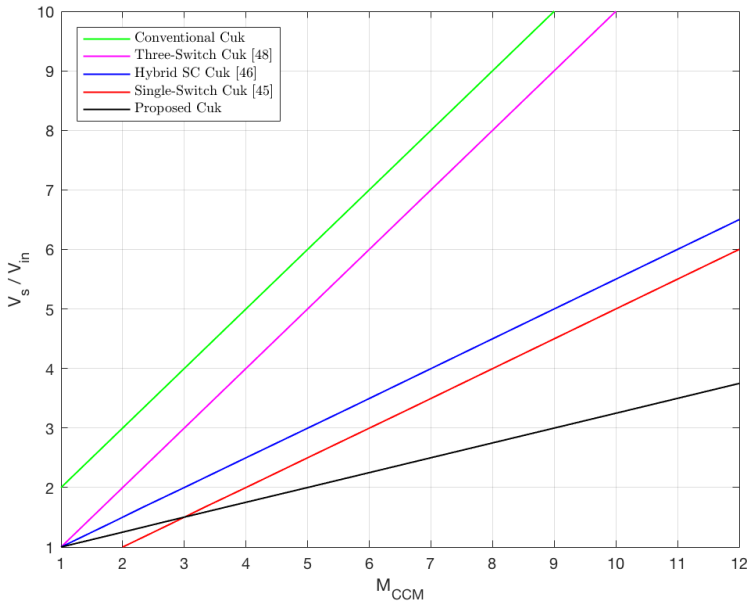


Fig. 5.7 Voltage stress comparison on active switches

As can be observed in Fig. 5.7, the converter having the highest voltage stress is the conventional Cuk converter. On the other hand, the lowest voltage stress can be maintained using the proposed Cuk converter. Therefore, the proposed Cuk converter is suitable for applications require higher voltage gain with lower voltage stress. Single-switch Cuk converter has a lower voltage stress for voltage gains less than 3. However, the proposed two-switch Cuk converter has a lower voltage stress for voltage gains larger than 3.

5.5 Cost Comparison

Choosing of power diodes and power MOSFET is based on the following four characteristics:

- Voltage rating which is the maximum instantaneous voltage that the device is required to block in its off-state.

- Current rating which is the maximum current that the device can carry in its on-state.
- Switching speeds which is the speed at which a device can make a transition from its on-state to off-state, or vice versa.
- On-state voltages which is the voltage drop across the device during its on-state while conducting a current. The smaller this voltage, the smaller will be the on-state power loss.

According to the previous four characteristics and [106], a comparison analysis includes the cost is provided in Table 5.3.

Table 5.3 Percentage comparison between proposed topologies and Cuk converter

Converter Type	Voltage Gain	Voltage Stress	Cost	Cost Range
Topology-I	$+308.3\%$	-47.3%	$+3.5\%$	$\$5 - \$7$
Topology-II	$+147.6\%$	-52.5%	-12.7%	$\$5 - \$7$
Topology-III	$+333.3\%$	-50%	$+23\%$	$\$5 - \$7$
Two-Switch	$+333.3\%$	-52.5%	$+4.6\%$	$\$5 - \$7$

Chapter Six: Results and Discussion

6.1 Introduction

In this chapter, simulation study of proposed Cuk converter topologies is presented and discussed. They are designed for 12V input voltage, 50kHz switching frequency, and 75% duty cycle. They all have been simulated in MATLAB/Simulink. A total of five different DC-DC non-isolated Cuk converter topologies are simulated and analyzed.

6.2 Switched-Inductor Multilevel Cuk Converter

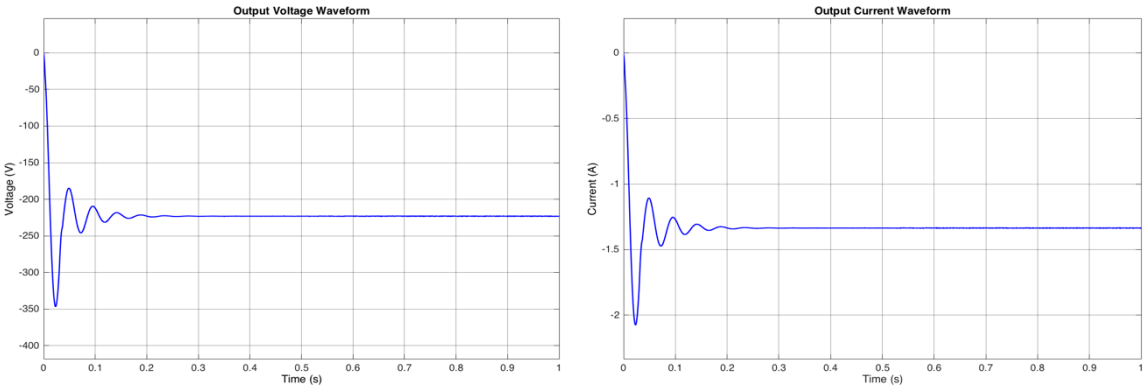
The proposed switched-inductor multilevel Cuk converter has the rated output parameters 300W and -225V. 12V is the input voltage, 75% is the duty cycle, and 50 kHz is the switching frequency. Table 6.1 gives the parameters and their values used in the MATLAB/Simulink simulation.

Table 6.1 Specifications of proposed switched-inductor converter

Sr. No	**3-Level Proposed Converter Specifications**	
	Parameter	***Value***
1	C_1, C_2, C_3, C_4, C_5, and C_o	220 µF
3	L_1, L_2, and L_3	0.5 mH
4	Load	170 Ω
5	Input Voltage (V_{in})	12V
6	Duty Cycle (D)	0.75
7	Switching Frequency (f)	50 kHz

Fig. 6.1 shows the output voltage and output current waveforms of the load. Fig. 6.2 shows the output power waveform of the load. The current waveforms of L_1, L_2, and L_3 are shown in Fig. 6.3. Applied gate voltage with the voltage stress across the switch is

shown in Fig. 6.4. The voltage stress across switch S_1 is approximately 80V. Finally, the voltage waveform across capacitors C_2 and C_4 are shown in Fig. 6.5. Simulation of proposed 3-level switched-inductor multilevel Cuk converter is carried out using MATLAB/Simulink software.



(a) (b)

Fig. 6.1 (a) Output voltage waveform (b) Output current waveform

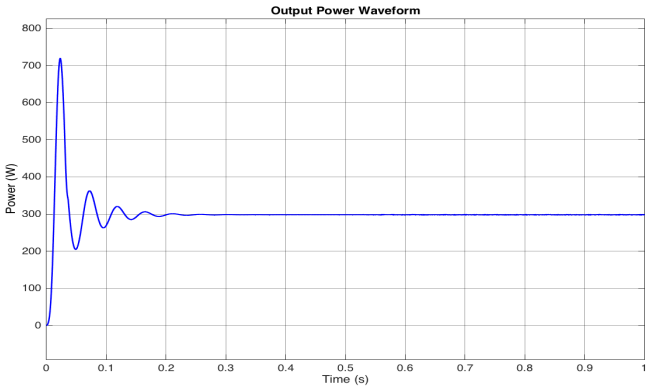
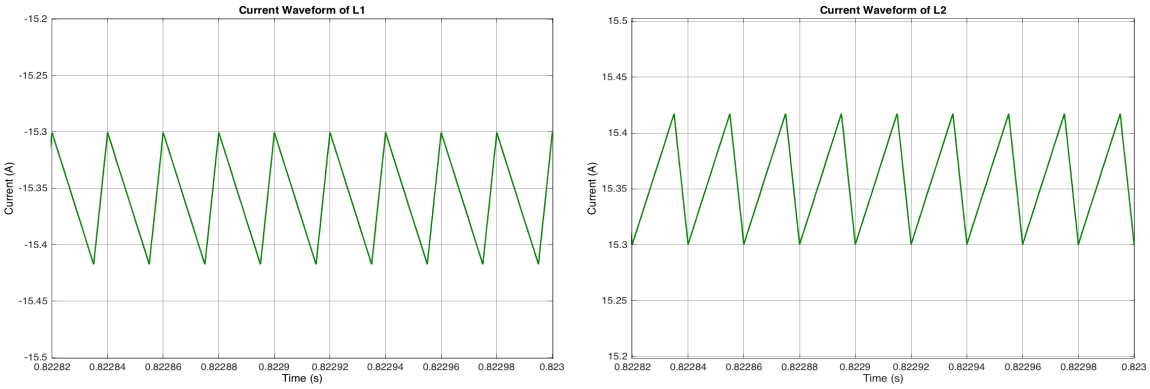
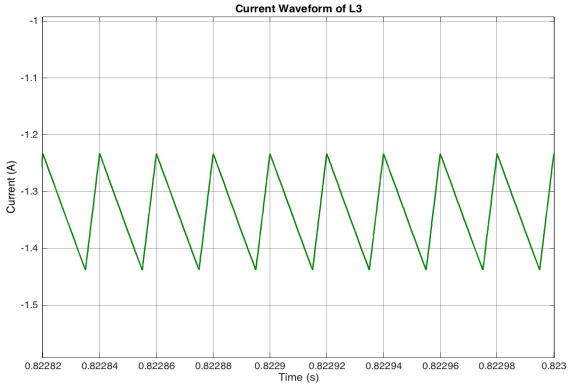


Fig. 6.2 Output power waveform

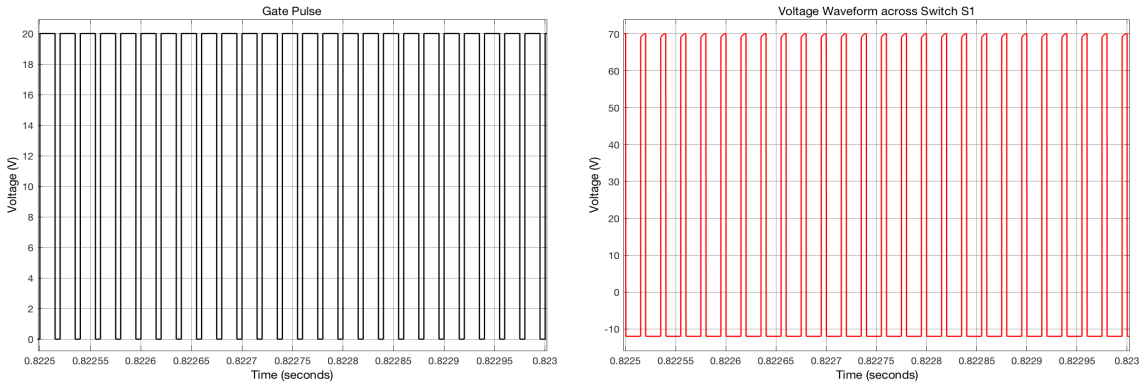


(a) (b)



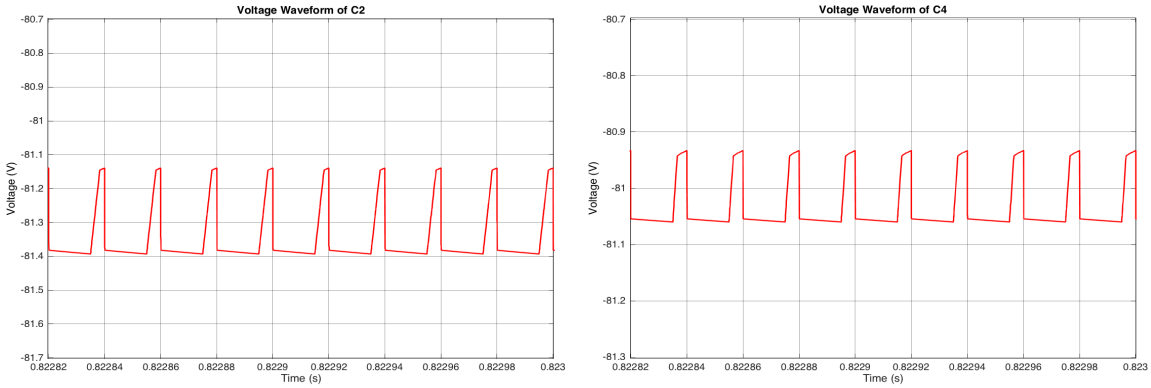
(c)

Fig. 6.3 Current waveforms of inductors (a) L_1 (b) L_2 (c) L_3



(a) (b)

Fig. 6.4 (a) Gate pulses waveform (b) Voltage waveform across switch S_1



(a) (b)

Fig. 6.5 Voltage waveform at output capacitors nodes (a) C_2 (b) C_4

6.3 Three Topologies of Cuk Converter

The three proposed topologies are designed for 12V input voltage, 100W rated power, 50kHz switching frequency, and 75% duty cycle. They all have been simulated in MATLAB/Simulink. Specifications of the proposed SLSC Cuk converters are given in Table 6.2.

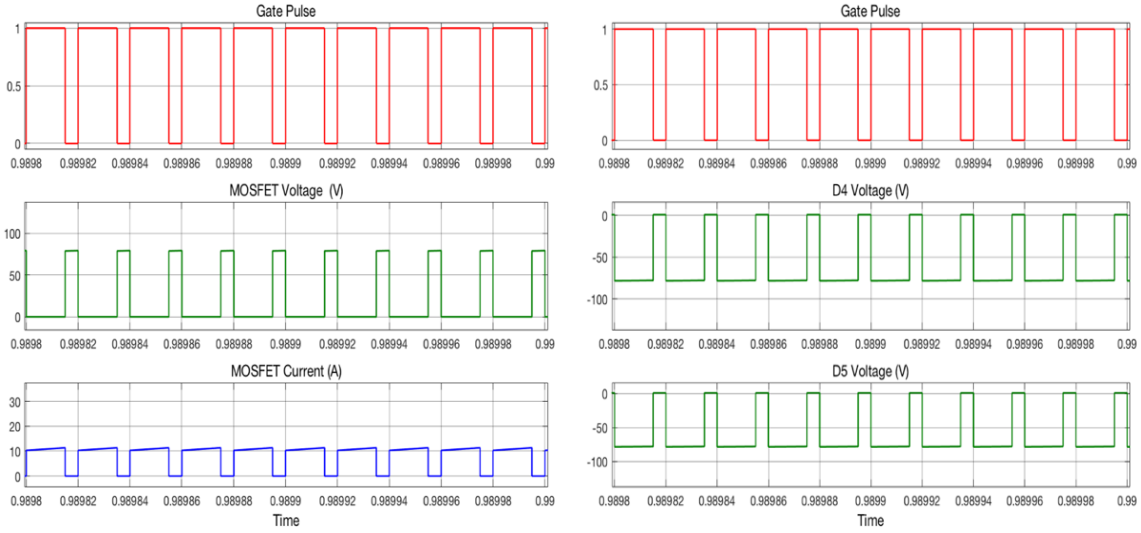
Table 6.2 Components Specifications

Parameter	Symbol	Value	Unit
Input Voltage	V_{in}	12	V
Output Voltage	V_{out}	-137/-87/-145	V
Rated Power	P_{out}	100	W
Switching Frequency	f	50	kHz
Duty Cycle	D	75%	-
Inductors	$L_1 \sim L_4$	600	μH
Capacitors	C_1, C_2	22	μF
Load	R_L	190/75/210	Ω

6.3.1 Topology-I

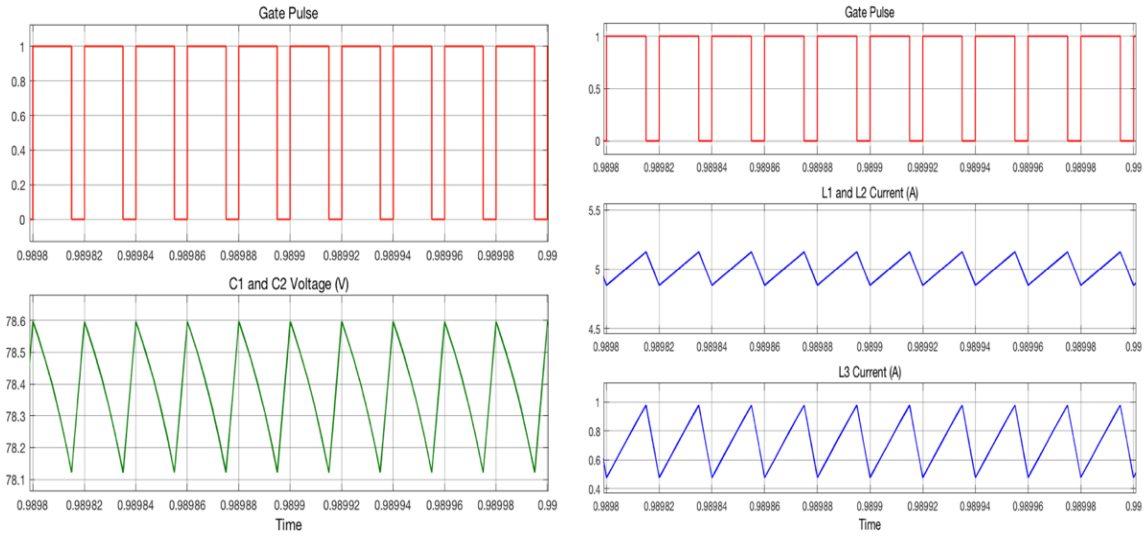
The SLSC Cuk converter topology-I is designed for -137 output voltage. The voltage stress and current stress on MOSFET S_1 are shown in Fig. 6.6(a). The voltage stress and current stress are approximately 78V and 10A, respectively. The voltage stress on the

two diodes D_4 and D_5 of the SC is shown in Fig. 6.6(b). The voltage stress across the two diodes of the SC is -78V. Diodes D_4 and D_5 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Fig. 6.6(b). The voltage waveforms of capacitors C_1 and C_2 are shown in Fig. 6.7(a). From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Fig. 6.7(b). The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Fig. 6.8.



(b) (b)

Fig. 6.6 (a) Voltage and current stresses on S_1 (b) Voltage stresses on D_4 and D_5



(a) (b)

Fig. 6.7 (a) Voltage waveforms of C_1 and C_2 (b) Current waveforms of L_1, L_2, and L_3

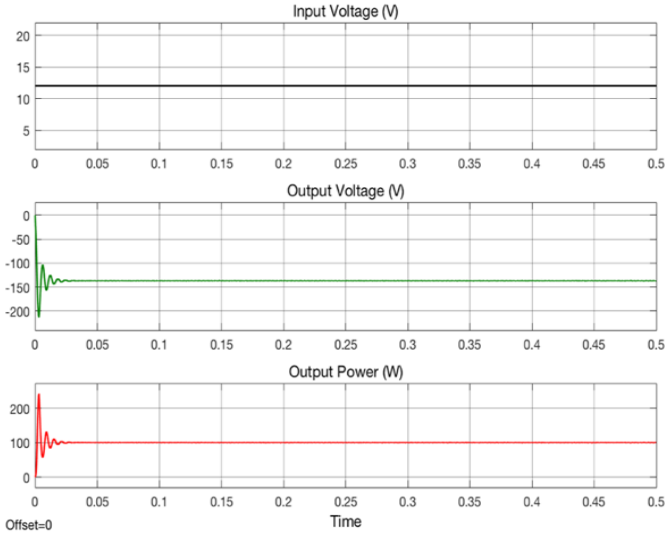
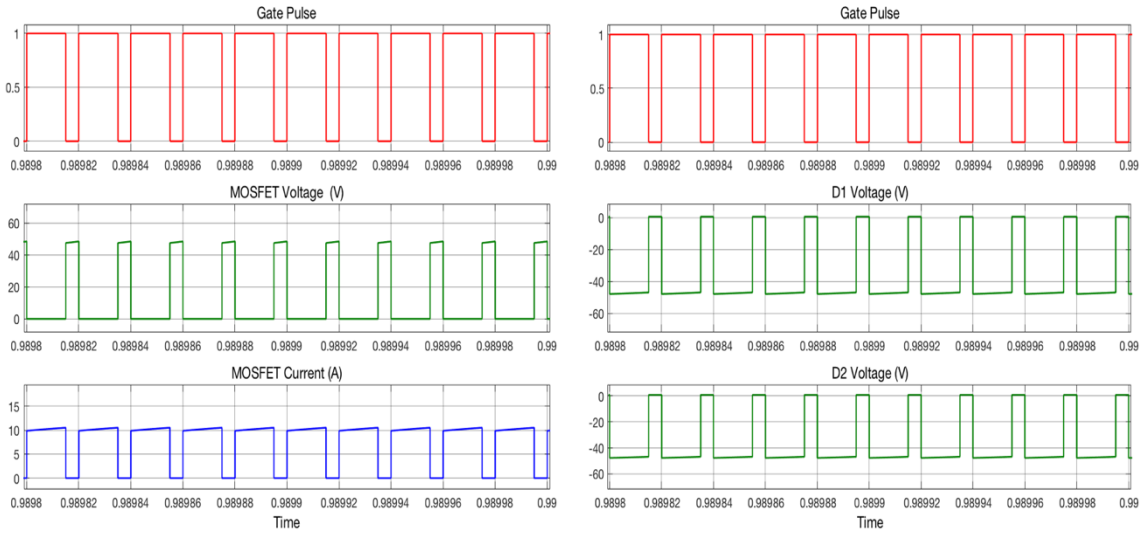


Fig. 6.8 V_{in}, V_{out}, and P_{out} waveforms of topology-I

6.3.2 Topology-II

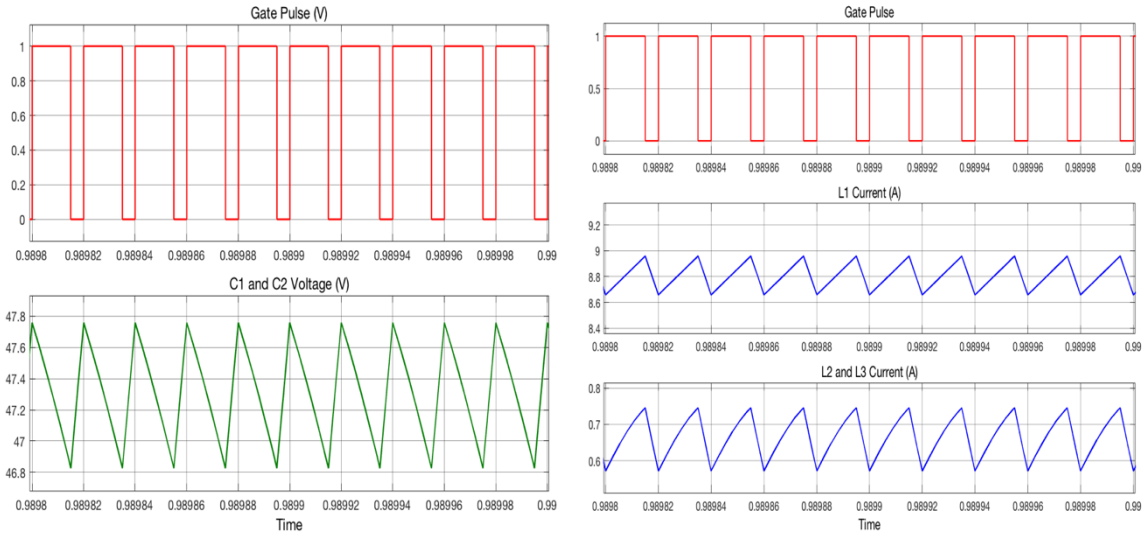
The SLSC Cuk converter topology-II is designed for -87 output voltage. The voltage stress and current stress on MOSFET S_1 are shown in Fig. 6.9(a). The voltage stress and current stress are approximately 48V and 10A, respectively. The voltage stress on the

two diodes D_1 and D_2 of the SC is shown in Fig. 6.9(b). The voltage stress across the two diodes of the SC is -48V. Diodes D_1 and D_2 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Fig. 6.9(b). The voltage waveforms of capacitors C_1 and C_2 are shown in Fig. 6.10(a). From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Fig. 6.10(b). The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Fig. 6.11.



(a) (b)

Fig. 6.9 (a) Voltage and current stresses on S_1 (b) Voltage stresses on D_1 and D_2



(a) (b)

Fig. 6.10 (a) Voltage waveforms of C_1 and C_2 (b) Current waveforms of L_1, L_2, and L_3

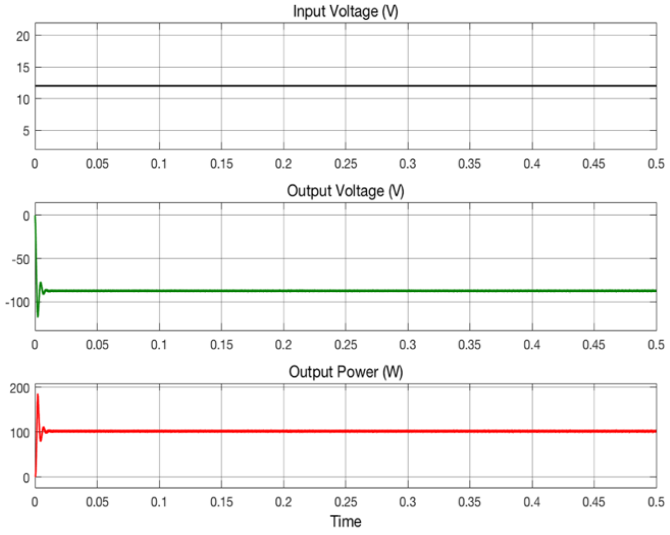
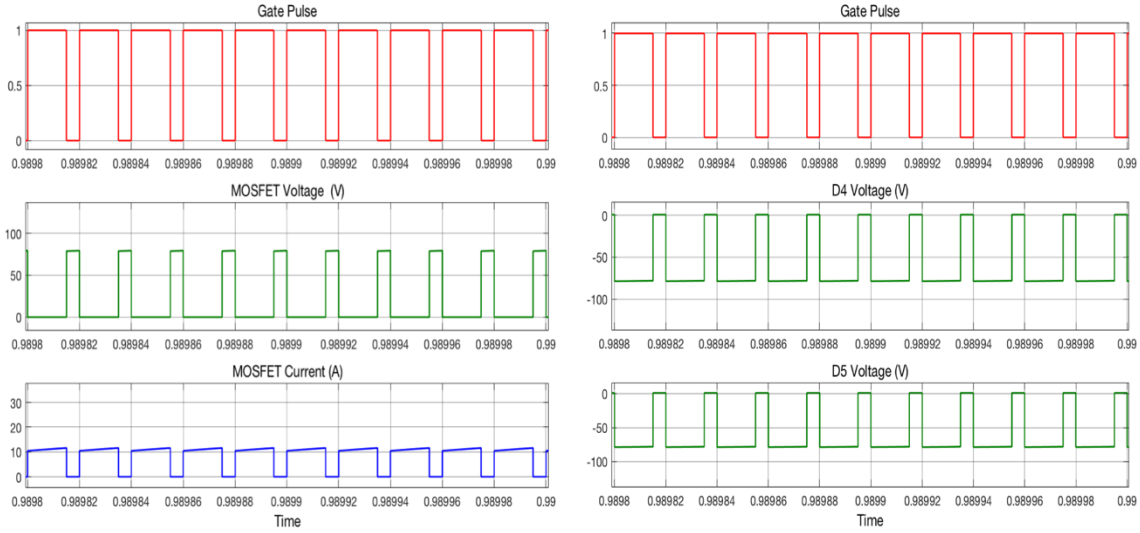


Fig. 6.11 V_{in}, V_{out}, and P_{out} waveforms of topology-II

6.3.3 Topology-III

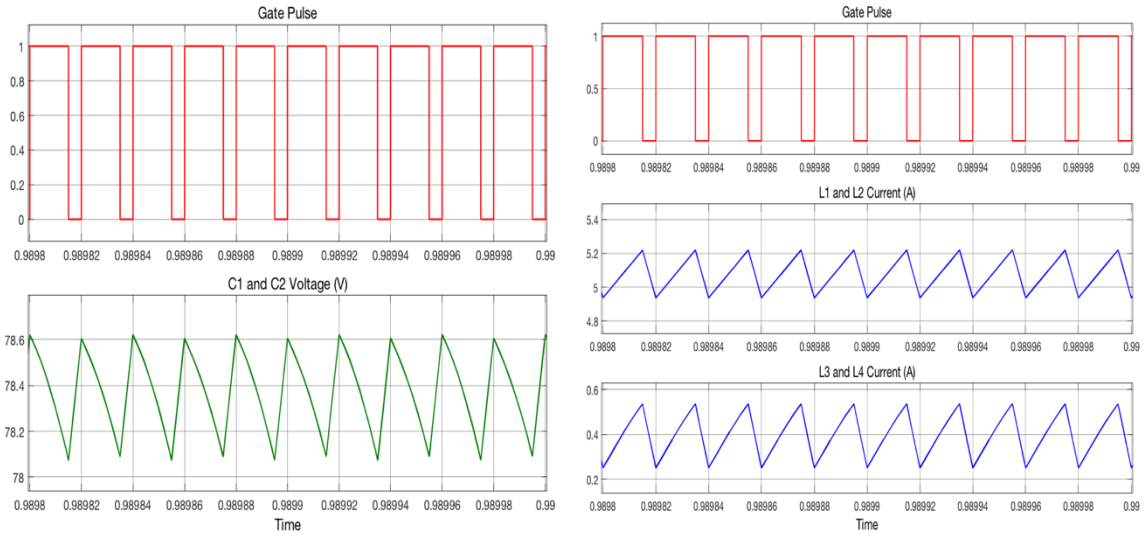
The SLSC Cuk converter topology-II is designed for -145 output voltage. The voltage and current stress on MOSFET S_1 are shown in Fig. 6.12(a). The voltage and current stress are approximately 78V and 10A, respectively. The voltage stress on the two

diodes D_4 and D_5 of the SC is shown in Fig. 6.12(b). The voltage stress across the two diodes of the SC is -78V. Diodes D_4 and D_5 are conducting during the off time period of MOSFET S_1, and they are not conducting during the on time period of MOSFET S_1 as shown in Fig. 6.12(b). The voltage waveforms of capacitors C_1 and C_2 are shown in Fig. 6.13(a). From the figure, the two capacitors get charged when MOSFET S_1 is off, and they get discharged when MOSFET S_1 is on. The current waveforms of inductors L_1, L_2, and L_3 are shown in Fig. 6.13(b). The three inductors get charged when MOSFET S_1 is on, and they get discharged when MOSFET S_1 is off. The input voltage, output voltage, and output power waveforms are shown in Fig. 6.14.



(a) (b)

Fig. 6.12 (a) Voltage and current stresses on S_1 (b) Voltage stresses on D_4 and D_5



(a) (b)

Fig. 6.13 (a) Voltage waveforms of C_1 and C_2 (b) Current waveforms of L_1, L_2, L_3, and L_4

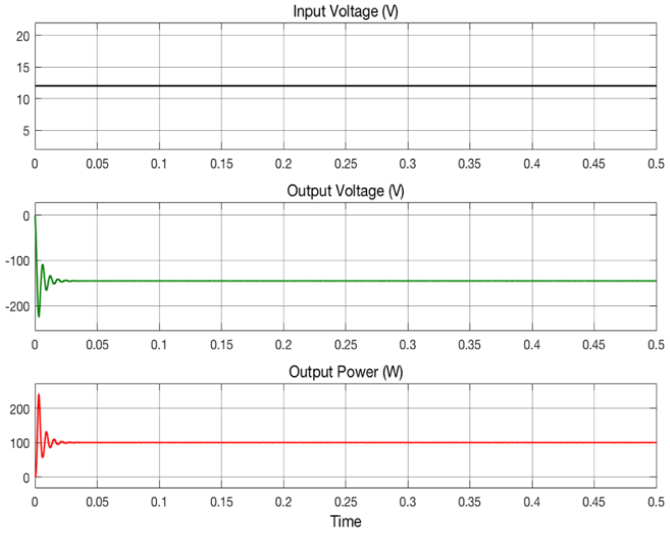


Fig. 6.14 V_{in}, V_{out}, and P_{out} waveforms of topology-III

An efficiency comparison between the three topologies of the proposed SLSC Cuk converter has been made using the numerical values assumed for parasitic parameters of the semiconductor switches given in Table 6.3. The efficiency is graphically represented in Fig. 6.15. Peak efficiencies of 86% for topology-I, 94.33% for topology-II, and 85% for

topology-III are achieved when the output power is 120W and the input voltage is 12V. As highlighted by [107] , The efficiency increases for higher input voltages because the input current decreases, and therefore, the conduction losses of power switches are reduced.

Table 6.3 Parasitic parameters of semiconductor switches

R_{DS-ON}	V_D	R_D
15 mΩ	0.7 V	30 mΩ

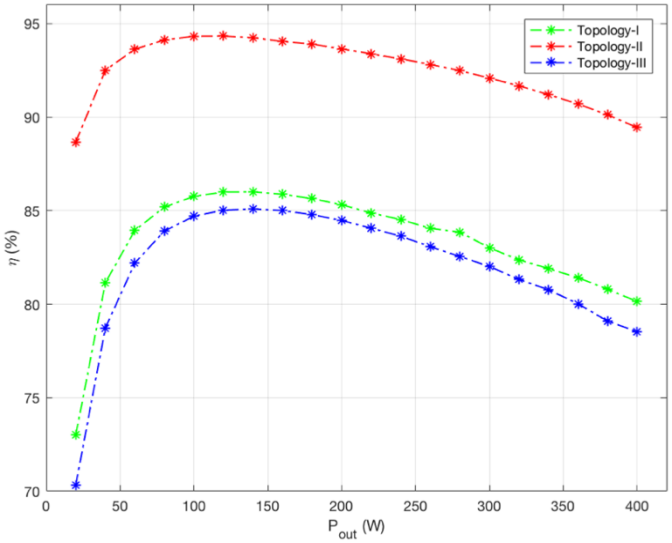


Fig. 6.15 Efficiency curves as a function of the output power

6.4 Two-Switch Cuk Converter

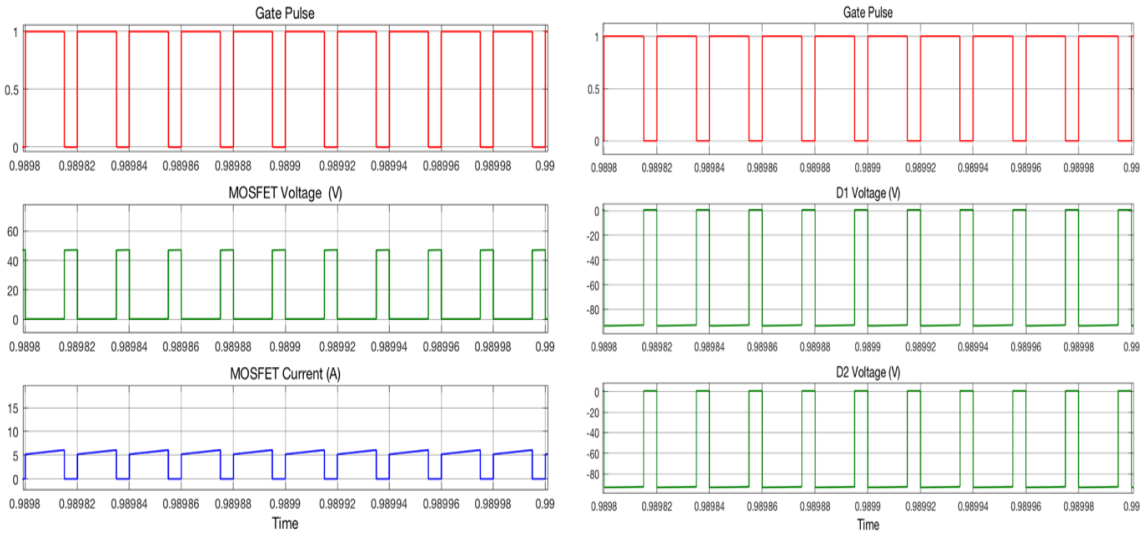
By using MATLAB/Simulink, a prototype 12/-152V circuit is carried out to verify the performance of the proposed Cuk converter. The simulation parameters of the proposed Cuk converter are 12V input voltage, -152V output voltage, 100W rated power, 50kHz switching frequency, and 75% duty cycle. Specifications of the proposed Cuk converter are given in Table 6.4.

Table 6.4 Detailed design parameters of the proposed two-switch Cuk converter

Parameter	Symbol	Value	Unit
Input Voltage	V_{in}	12	V
Output Voltage	V_{out}	-152	V
Rated Power	P_{out}	100	W
Switching Frequency	f	50	kHz
Duty Cycle	D	75%	-
Inductors	L_1, L_2, L_{out}	600	μH
Capacitors	C_1, C_2	22	μF
Load	R_{Load}	230	Ω

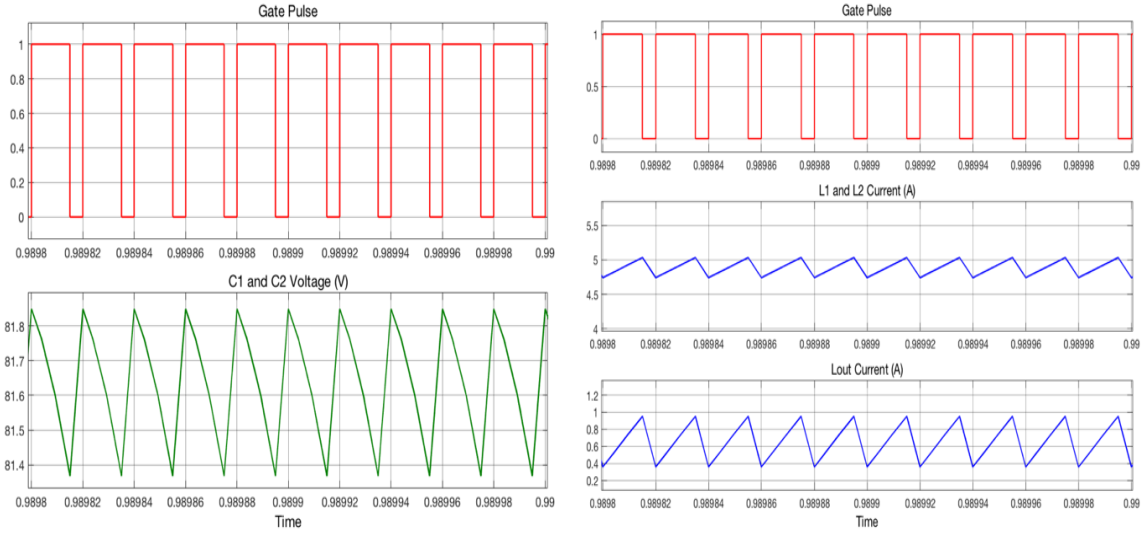
The voltage stress and current stress across the two MOSFETs S_1 and S_2 are 47V and 5A, respectively. The voltage stress and current stress waveforms are shown in Fig. 6.16(a). Fig. 6.16(b) shows the voltage waveforms of diodes D_1 and D_2 which each one has a voltage stress of -90V. Diodes D_1 and D_2 are reversed biased when the two MOSFETs S_1 and S_2 are on, and they are forward-biased when the two MOSFETs S_1 and S_2 are off. The voltage waveform of the two capacitors C_1 and C_2 is shown in Fig. 6.17(a). The current waveforms of the three inductors L_1, L_2, and L_{out} are shown in Fig. 6.17(b). Finally, the input voltage V_{in} (12V), output voltage V_{out} (-152V), and output power P_{out} (100W) waveforms are shown in Fig. 6.18.

The efficiency of the proposed Cuk converter is calculated as the output power increased as shown in Fig. 6.19. The highest efficiency is 92% when the output power is 180W. When the input voltage is increased, the efficiency of the proposed Cuk converter is increased because the input current decreases. Therefore, the conduction losses on switches get reduced.



(a) (b)

Fig. 6.16 (a) Voltage and current stress on S_1 and S_2 (b) Voltage stresses on D_1 and D_2



(a) (b)

Fig. 6.17 (a) Voltage waveform of C_1 and C_2 (b) Current waveforms of L_1, L_2, and L_{out}

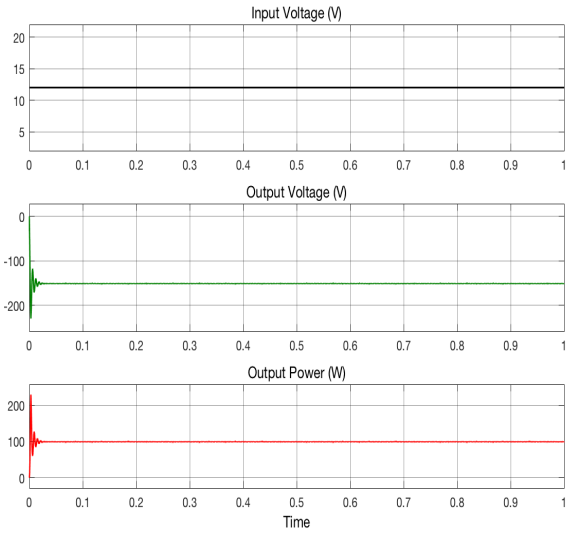


Fig. 6.18 V_{in}, V_{out}, and P_{out} waveforms of proposed two-switch Cuk converter

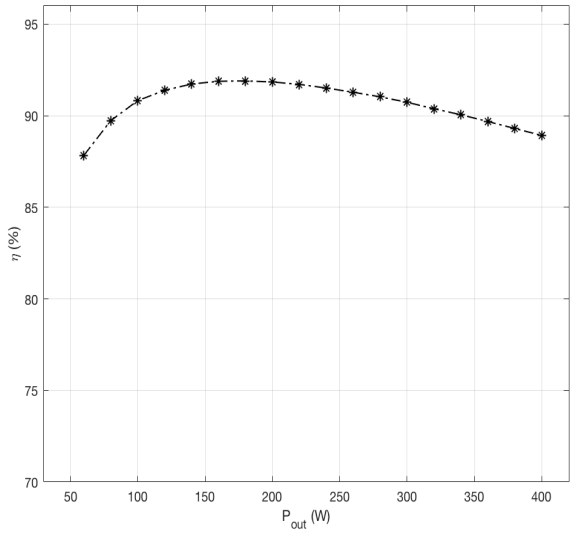


Fig. 6.19 Efficiency curve as a function of the output power

Output results summary for the three topologies and the two-switch topology in terms of the output voltage, voltage stress across the active switch, voltage stress across two diodes of the SC, and efficiency are given in Table 6.5.

Table 6.5 Summary of proposed topologies

Topology	Output voltage	Voltage stress on S_1 and S_2	Voltage stress on diodes of SC	Voltage across C_1 and C_2	η
Topology-I	-137V	78V	-78V	78.35V	86%
Topology-II	-87V	48V	-48V	47.3V	94.3%
Topology-III	-145V	78V	-78V	78.35V	85%
Two-Switch	-152V	48V	-88V	81.6V	92%

6.5 System Design

A whole system is designed by MATLAB/Simulink to test topology-II converter. In this system, a PV is used as an input source followed by topology-II DC-DC converter to boost the voltage of the PV. Then, a full bridge inverter is designed to supply an AC load. The circuit is shown in Fig. 6.20. The input voltage, output voltage of the topology-II DC-DC converter, the output voltage of the full bridge inverter, and the output power waveforms are shown in Fig. 6.21.

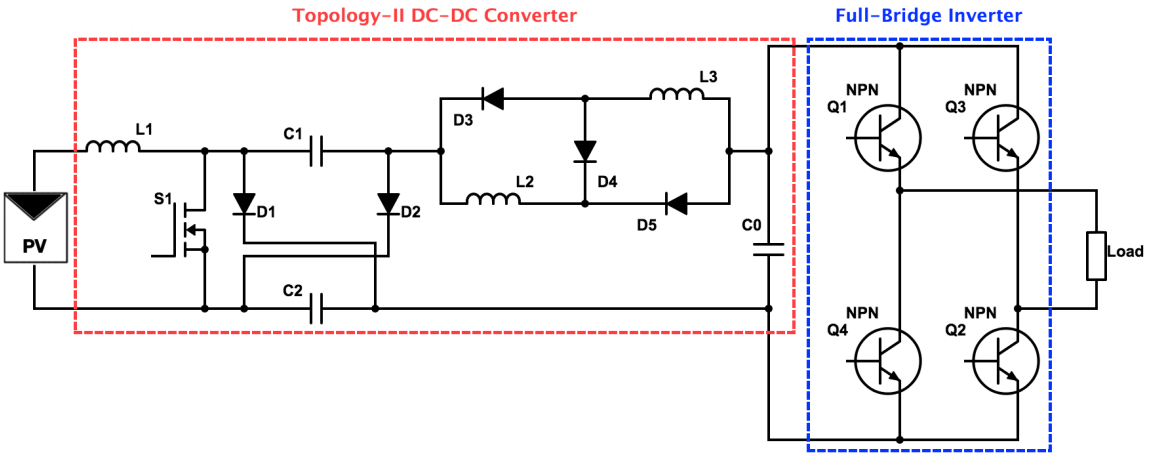


Fig. 6.20 Whole system design circuit

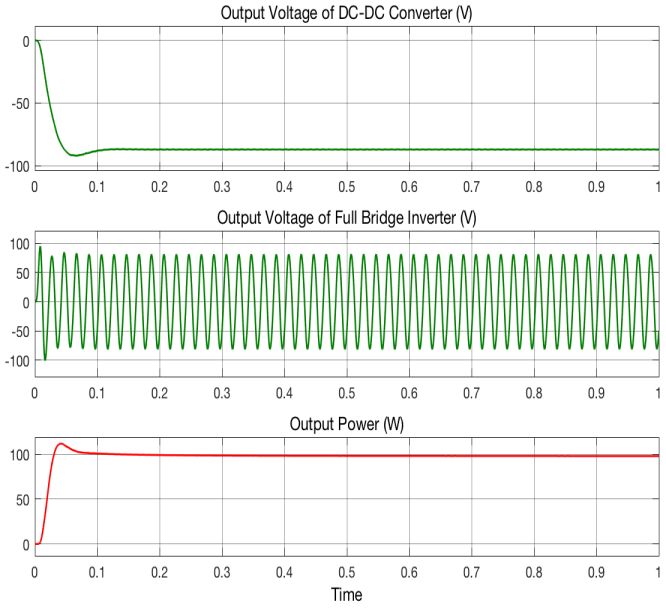


Fig. 6.21 V_{in}, V_{out} of topology-II, V_{out} of inverter, and P_{out} waveforms

6.5.1 PV Connected with MPPT and Topology-II

The block diagram of MPPT system is shown in Fig. 6.22 which consists of the Sunperfect Solar CRM60S125S as the PV array, proposed topology-II as a DC-DC converter, and IncCond algorithm as a MPPT technique. The output voltage of the PV array is fed to topology-II DC-DC Cuk converter. The voltage and current from the PV array are used as two inputs of the MPPT, and therefore they are processed by the MPPT and changed accordingly. Table 6.6 gives the electric characteristics of the selected PV array which is "Sunperfect Solar CRM60S125S". The whole system was simulated using MATLAB/Simulink.

The irradiance decreases and increases linearly from 1000W/m^2 to 200W/m^2 and vice versa. Also, the temperature increases linearly from 25° to 50°. The resulted waveforms are shown in Fig. 6.23. As can be clearly seen from Fig. 6.23 that the duty cycle changes in order to maintain the maximum power as the irradiance and temperature change.

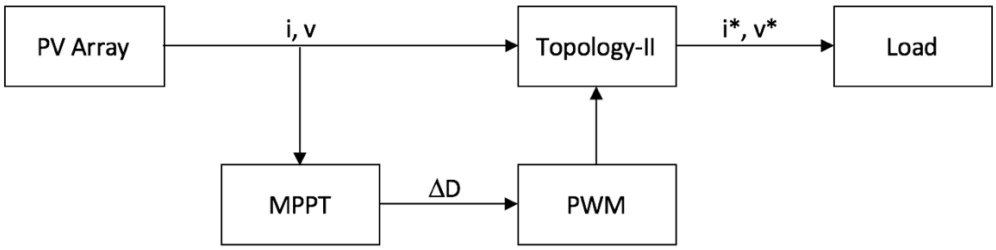


Fig. 6.22 MPPT block diagram

Table 6.6 Electrical characteristics of PV array

Parameter	Symbol	Value	Unit
Cells Per Module	N	24	Ncell
Maximum Power	P_{Max}	57.96	W
Open Circuit Voltage	V_{OC}	14.5	V
Short Circuit Current	I_{SC}	5.51	A
Voltage at Maximum Power	V_{MP}	11.5	V
Current at Maximum Power	I_{MP}	5.04	A
Total Number of Cells in Series	N_S	1	-
Total Number of Cells in Parallel	N_P	2	-

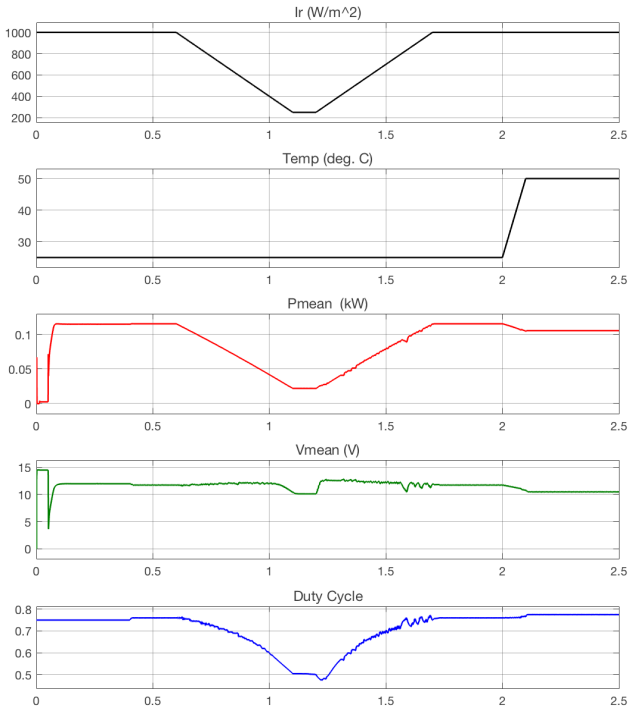


Fig. 6.23 PV and MPPT waveforms

Chapter Seven: Conclusion and Future Research

7.1 Conclusion

This study has successfully developed different Cuk converter topologies with high voltage gain and low voltage stress across the main switch. These types of Cuk converters can be used in renewable energy applications such as photovoltaic and fuel cell in which a high voltage gain is required. The main reason for reaching a high voltage gain with low voltage stress is using switched-inductor and switched-capacitor techniques in the conventional Cuk converter. In the proposed Cuk converter topologies, a high voltage gain is accomplished without using a transformer, coupled inductors, or an extreme duty cycle. Avoid using a transformer or coupled inductors leads to less volume, loss, and cost. Also, avoid using an extreme duty cycle leads to less loss and voltage stress on semiconductor switches. The main advantages of the proposed Cuk converter topologies include a high voltage, a low voltage stress which leads to select an active switch with a lower voltage rating and a lower $R_{DS\text{-}ON}$, non-pulsating input and output currents, a relatively high efficiency, and the simplicity of the designs.

All Cuk converter topologies are analyzed in the continuous conduction mode (CCM). A comparison has been made between the proposed Cuk converter topologies with conventional converters and other Cuk converters used different techniques. The operating modes and steady-state analysis of the proposed Cuk converter topologies are discussed. The resulted waveforms agree with the operating modes and steady-state analysis.

7.2 Future Research

There are more areas need to be further investigated which are not covered in this dissertation. In the current work, only the mathematical analysis and simulation study were performed. Although the mathematical analysis and the simulation study by MATLAB/Simulink were matched and prove the feasibility of the circuit, an experimental work can be achieved to overcome any unexpected problems happening in the real circuit. Therefore, modifications to the proposed circuits are required. Also, the effect of the parasitic elements was not investigated. The effect of parasitic elements due to losses associated with the capacitor, inductor, MOSFET, and diode can be calculated and compared with the simulation results and the experimental results. The proposed circuits are regulated by PWM technique at a constant frequency. It is worth trying to make a control design for the proposed circuits, and also a small signal analysis can be performed. Finally, a reliability analysis in case of one of the switches failed to operate can be accomplished.

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Appendix

List of Publications

Journal Papers

- **Y. Almalaq** and M. Matin, "Three topologies of a non-isolated high gain switched-inductor switched-capacitor step-up cuk converter for renewable energy applications," Electronics, vol. 7, no. 6, p. 94, 2018.
- A. Alateeq, **Y. Almalaq**, and M. Matin, "A Performance of the Soft-Charging Operation in Series of Step-Up Power Switched-Capacitor Converters," *Journal of Low Power Electronics and Applications*, vol. 8, no. 1, p. 8, Mar. 2018.
- **Y. Almalaq** and M. Matin, "Two-Switch High Gain Non-Isolated Cuk Converter," *International Journal of Power and Energy Systems*. (submitted)

Conference Papers

- **Y. Almalaq**, A. Alateeq, and M. Matin, "A non-isolated high gain switched-inductor switched-capacitor step-up converter for renewable energy applications," in IEEE International Conference on Electro Information Technology (EIT), 2018, pp. 134–137.
- **Y. Almalaq**, A. Alateeq, and M. Matin, "A transformerless high gain switched-inductor switched-capacitor Cuk converter in step-up mode," in IEEE International Conference on Electro Information Technology (EIT), 2018, pp. 138–141.
- **Y. Almalaq**, A. Alateeq, and M. Matin, "Non-isolated high gain switched inductor DC-DC multilevel Cuk converter for photovoltaic applications," in North American Power Symposium (NAPS), 2017.

- A. Alateeq, **Y. Almalaq**, and M. Matin, "A switched-inductor model for a non-isolated multilevel boost converter," in *2017 North American Power Symposium (NAPS)*, 2017, pp. 1–5.

- **Y. Almalaq**, A. Alateeq, and M. Matin, "Simulation and performance comparison of Si and SiC-based interleaved boost converter," in Proceedings of SPIE, 2017, vol. 10381, p. 103810C 1-5.
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