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Auxiliary Resonant Source Charge Extraction Circuitry for Enabling the Use of Super Junction MOSFETs in High Efficiency DC-DC converters

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***Abstract*— In this paper a high efficiency DC-DC converter power stage employing silicon Super-Junction (SJ) MOSFETs is presented. These devices have low on-state resistances and fast switching capabilities. However, their intrinsic body diode has a very poor reverse recovery behavior and they have an output capacitance that has a highly non-linear inverse relationship with voltage. These characteristics lead to problematic charging currents when they are used in bidirectional voltage source converters. These problems are addressed through implementation of an auxiliary resonant source charge extraction circuit in conjunction with anti-series MOSFETs. The result is a 5-kW power converter with a power semiconductor stage full-load efficiency exceeding 99% and requiring no forced cooling.**

Keywords— auxiliary resonant topology, diode reverse recovery, MOSFET, output capacitance, super-junction, switching-aid circuit.

I. INTRODUCTION

In electric vehicles, power conversion stages facilitate the power flow between storage elements, on-board loads and drive-train propulsion systems, hence, efficiency, cost and volume are key design drivers in automotive power electronics. Extending electric vehicle range, reducing converter volume and mass, and enabling significant cost savings through the reduction or elimination of active cooling are just a few of the system level benefits of maximizing the efficiency of power conversion stages in electric vehicles.

Insulated Gate Bipolar Transistors (IGBTs) are typically the favored choice of switching device in bidirectional Voltage Source Converters (VSCs) in the 200-400-V range. However, they have limitations if high efficiencies are to be attained, due to their high on-state forward voltage drop, low minority carrier recombination rates at turn-off, and conductivity modulation lag at turn-on. SiC MOSFET costs, reliability concerns related to gate oxide [1] and body diode degradation [2], and non-trivial gate driver circuitry design [3] (due to their low transconductance, low gate breakdown voltages and crosstalk) are challenges that require consideration before they can be applied in VSCs. Super-Junction (SJ) silicon MOSFETs are therefore an attractive alternative due to their reasonable cost, fast switching capability and low on-state resistances [4]. However, they suffer from two inherent problems which hamper their widespread adoption in bidirectional VSCs. Namely, SJ MOSFETs exhibit poor reverse recovery of their intrinsic body diodes and have an output capacitance C_{oss} that has a highly non-linear inverse relationship with voltage [5].

Fig. 1 shows a schematic circuit diagram of a bidirectional half-bridge converter using MOSFETs. The devices' C_{oss} capacitances are included for clarity. In the buck mode of operation, S1 is the incoming device and S2 the Synchronous Rectifier (SR). Whereas in the boost mode, S1 is the synchronous rectifier and S2 the incoming device.

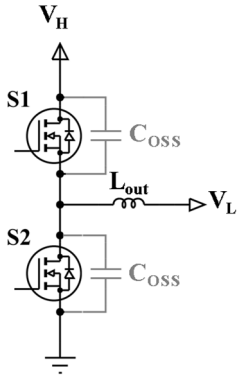


Fig. 1. Bidirectional half-bridge converter topology.

Fig. 2 shows the charge-voltage QV curve for a typical SJ MOSFET's C_{oss} [6], where the area beneath the curve (the sum of Regions B and C) represents the co-energy (energy dissipated in the course of charging the device's C_{oss}) and the highlighted area above the curve and bounded by the peak charge (Region A), represents the much lower self-discharge energy (energy dissipated in the channel as the MOSFET's C_{oss} is discharged).

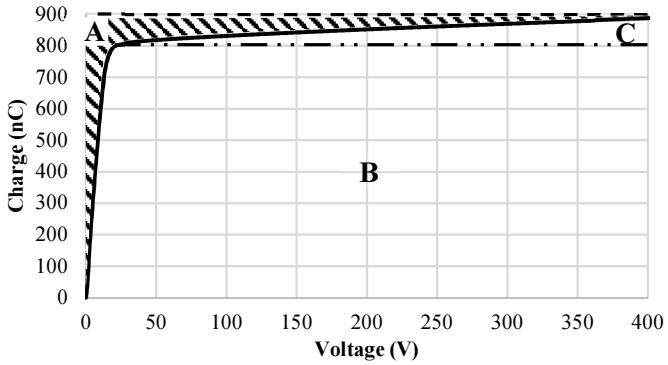


Fig. 2. Output capacitance charge versus voltage relationship for the IPW65R019C7 SJ MOSFET [6].

These two characteristics of SJ MOSFETs lead to very large and detrimental transient currents drawn through the incoming device of a VSC phase leg at turn-on. This results in both significant losses dissipated in its channel and high EMI due to the large peak current sourced. The di/dt of this charging current can be limited dissipatively through control of the incoming device's gate voltage [7][8]. However, this leads to significant additional losses as shown in [9]. SJ MOSFETs can achieve high efficiencies when implemented in single-ended VSCs with complementary SiC diodes [10]. In this case, the low self-discharge losses of the MOSFET in conjunction with the low reverse recovery charge of the SiC diode results in low switching losses. When bidirectional power flow is required, techniques that control C_{oss} charging and achieve intrinsic diode deactivation must be used. Some examples of these techniques include; auxiliary bridge legs [11], series switching-aid circuits [12], auxiliary resonant switching aid circuits [13] and dual unidirectional topologies [14]. The use of anti-series MOSFETs is a technique [15] that has been shown to deactivate the intrinsic diode [16], by forcing the load current into a parallel SiC Schottky diode shortly prior to the SR MOSFET commutating off. The anti-series MOSFET requires only a low blocking voltage rating and hence an inexpensive device with a low on-state resistance can be readily sourced. However, this technique does not address the problems associated with charging of the SJ device's highly non-linear output capacitance.

Drain Current Injection (DCI), an auxiliary resonant switching-aid circuit technique which addresses the aforementioned problems with SJ MOSFETs, is reported in [17] and [18]. In DCI, a current is injected into the drain of the synchronous rectifying MOSFET before it commutates off reversing the net drain current flowing through it and consequently deactivating its intrinsic diode. The injected current also pre-charges the output capacitance to above the 'knee' of the QV curve prior to the incoming device commutating on. This results in a significantly reduced co-energy as represented by Region C of Fig. 2. Estimated efficiencies of 99.4% were achieved using this technique. However, a costly SiC diode with both high voltage and current ratings is required, and significant injection current must flow in the DCI circuit, equal to approximately twice the load current which contributes to loss (approximately 20% of the total power stage losses) and reduced efficiency. The blocking voltage ratings for the DCI components must also be sufficiently high to prevent unwanted device avalanching.

This paper presents a novel auxiliary resonant switching-aid circuit technique referred to as Source Charge Extraction (SCE). The proposed circuitry is implemented in conjunction with anti-series MOSFETs in a multi-kilowatt DC-DC converter with an estimated power stage efficiency of >99.4%.

II. Device Datasheet Comparisons

IGBTs, SJ MOSFETs, and wide band-gap (WBG) devices such as SiC MOSFETs and GaN HEMTs are all available with ratings suitable for applications in the 200-400-V range. Where high efficiency operation is required, SJ MOSFETs, SiC MOSFETs and GaN HEMTs are favoured over the IGBT due to their availability with low on-state resistances. Three similarly rated state-of-the-art devices, detailed in Table I, were selected to make a qualitative comparison of the relative merits of the three technologies. The data shown in Figs. 3, 4 and 5 was derived from graphical data presented in the manufacturer's datasheets using the Engauge Digitizer program [19].

TABLE I. Similarly Rated Low On-State Resistance State-of-the-Art Semiconductor Devices

Device type	Manufacturer/part number	Blocking voltage rating	On-state resistance ($R_{ds(on)}$) @ 25°C
Si SJ MOSFET	Infineon IPW65R019C7 [6]	650 V	19 mΩ
SiC MOSFET	Rohm SCT3022AL [20]	650 V	22 mΩ
GaN E-HEMT	GaN Systems GS66516T [21]	650 V	25 mΩ

Figs. 3 and 4 show the C_{oss} and Q_{oss} against drain to source voltage v_{ds} respectively for the three similarly rated devices. The change in charge above the knee in the QV curve for the SJ MOSFET is similar to the SiC MOSFET and GaN HEMT. Assuming the C_{oss} of the SJ MOSFET is charged to above the knee voltage, prior to commutation of the incoming device in a bridge leg, the loss profile incurred in the circuit will become more similar to that experienced when using WBG devices.

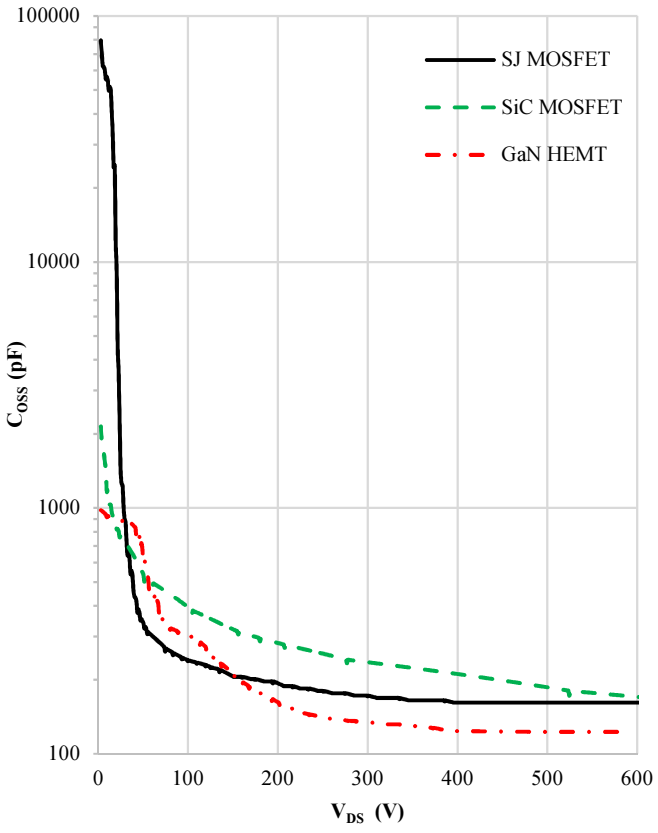


Fig. 3. Output capacitance against drain to source voltage (v_{ds}) for a similarly rated SJ MOSFET, SiC MOSFET, and GaN HEMT.

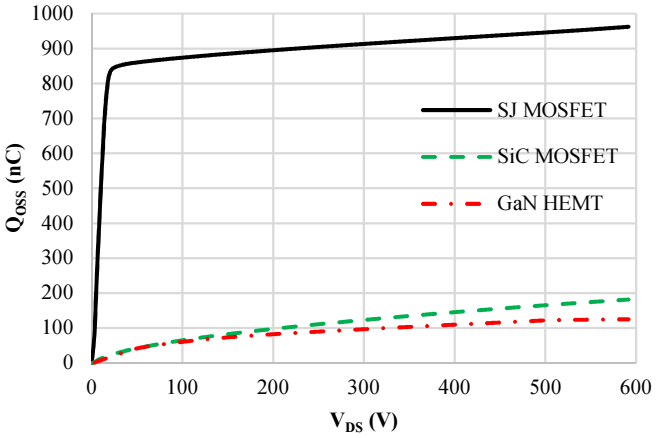


Fig. 4. Output capacitance charge (Q_{oss}) against drain to source voltage (v_{ds}) for the three similarly rated devices.

Fig. 5 shows the lower dependency of $R_{DS(on)}$ against junction temperature T_j for the SiC MOSFET compared to that of the SJ MOSFET and GaN HEMT. The $R_{DS(on)}$ of the SJ MOSFET has a lower temperature dependency than the GaN HEMT. Fig. 6 highlights the impact of the SiC MOSFET's low transconductance. A gate-source voltage v_{gs} close to the gate breakdown voltage is required to achieve optimal performance. The SJ MOSFET benefits from a low variation of $R_{DS(on)}$ with gate to source voltage, enabling application of a v_{gs} value far below its breakdown voltage, whilst still achieving low conduction losses.

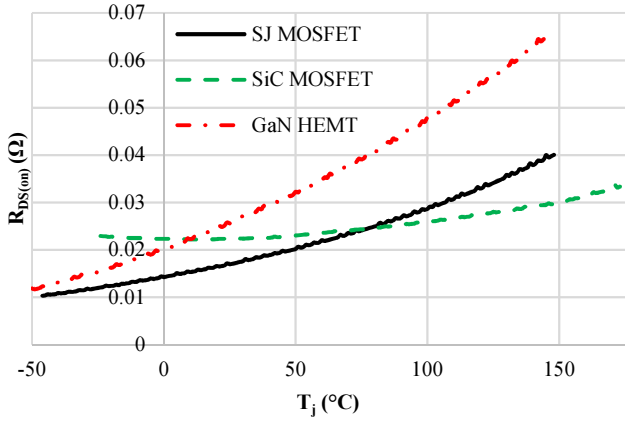


Fig. 5. On-state resistance ($R_{ds(on)}$) against junction temperature (T_j) for the three similarly rated devices.

At the time of writing this paper, for low quantities, the SiC MOSFET and GaN HEMT have a cost per unit of 2.2 and 3.3 times that of the SJ MOSFET respectively. These increase to 2.5 and 4.2 times that of the SJ MOSFET as the quantity increases above 250 units. Reliability concerns relating to WBG devices must also be considered. SiC MOSFETs benefit from the material's higher thermal conductivity enabling operation at higher ambient temperatures. The maximum operating temperature for the SiC MOSFET shown here is 175°C, 25°C higher than the two competitors. However low channel mobility and gate oxide reliability at high temperature and high electric fields have been reported in the literature [22].

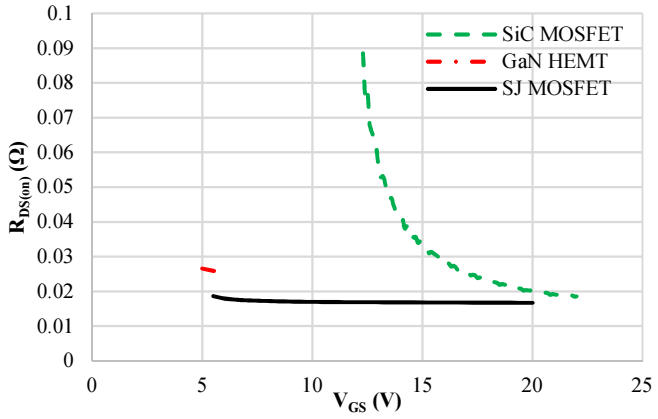


Fig. 6. On-state resistance ($R_{ds(on)}$) against gate-source voltage (v_{gs}) for the three similarly rated devices. SiC MOSFET data was obtained from the datasheet curve of $R_{ds(on)}$ against v_{gs} at an ambient temperature of 25°C and a current of 36 A. Both the SJ MOSFET and GaN HEMT data were determined from the datasheets' $R_{ds(on)}$ against drain current (I_D) profiles. The resistance was extracted from the curves at 36 A. Junction temperatures of 125°C and 150°C are quoted for the SJ MOSFET and GaN HEMT respectively.

III. Source Charge Extraction (SCE)

Fig. 7 shows the proposed converter arrangement. Operation in the buck mode only is considered here for experimental purposes and hence the SCE circuitry and anti-series MOSFET (S2a) are only present around the synchronous rectifier (S2). A second SCE circuit, anti-series MOSFET and anti-parallel SiC diode would be required for the incoming device (S1) if bidirectional power flow is required. The SCE circuitry is sourced by a low voltage supply. This could be the gate driver supply for the S2 and S2a MOSFETs as a floating supply is already required here. A separate floating gate drive is required for Q1, hence a multiple output isolated gate driver topology, for instance a design based upon a flyback converter, would be appropriate. The switching timings between the SJ MOSFET (S2) and the anti-series MOSFET (S2a) are controlled through selection of a Zener diode (connected in series with the gate of S2a) and the two devices' gate resistances, enabling a single PWM signal to drive both devices.

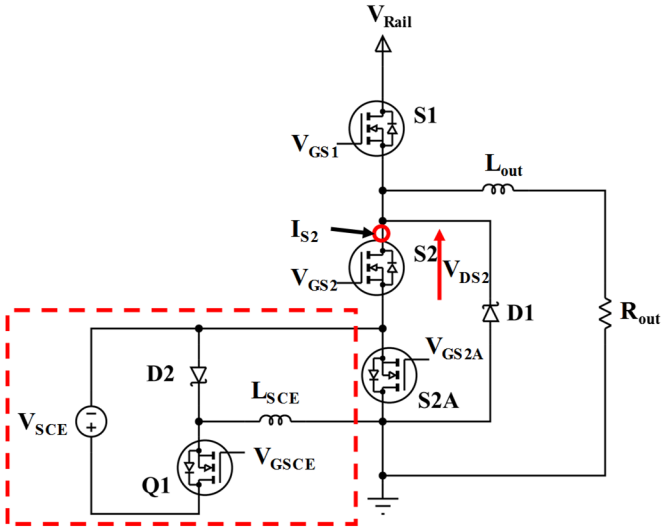
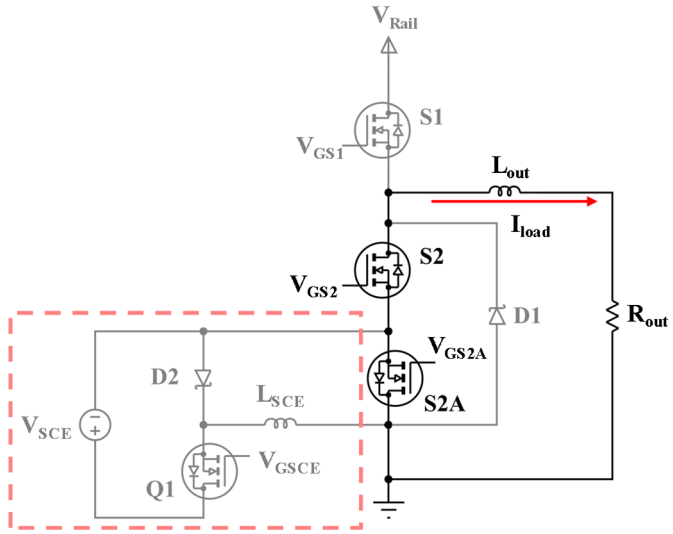
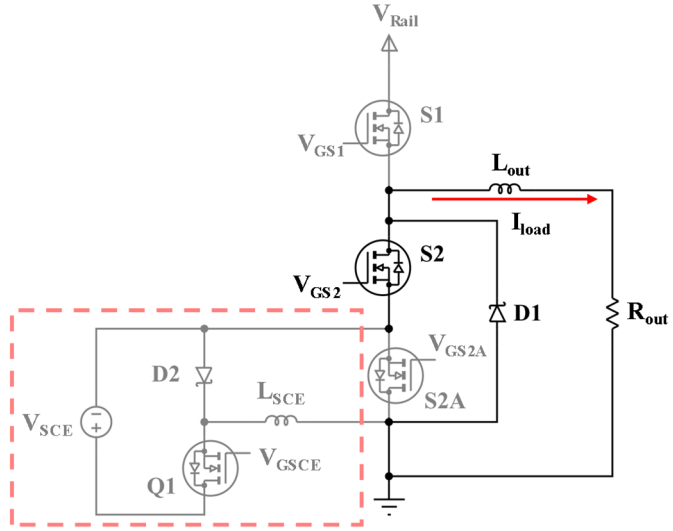


Fig. 7. Proposed converter power stage and SCE circuitry (enclosed by the dotted square).

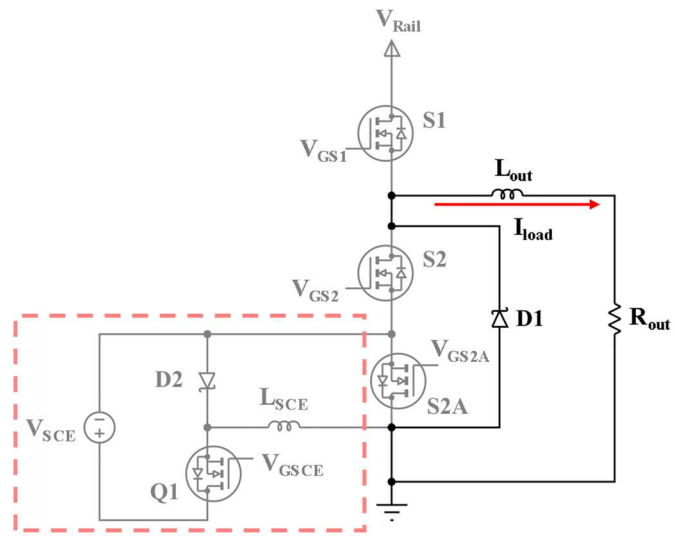
Fig. 8 shows the stages of operation for the SCE circuitry. The SCE circuit operation starts at the end of the synchronous rectification phase, Stage 1. The load current flows through the channels of the SJ MOSFET S2 and the anti-series MOSFET S2a. S2a commutates off at the start of Stage 2, the beginning of the dead time, and the current is forced into the SiC anti-parallel diode D1. The SJ MOSFET commutates off soon after under a Zero-Current Switching (ZCS) condition and hence its intrinsic body diode does not conduct, Stage 3. Following this, the SCE MOSFET Q1 commutates on and the SCE circuit is activated. A resonance occurs between the C_{oss} of the two anti-series connected MOSFETs (represented by the two capacitances in Fig. 8, Stage 4) and the SCE inductance L_{SCE}. An oscillatory current flows into the C_{oss} of the two devices raising the v_{ds} of the SJ MOSFET to approximately twice the value of the SCE supply and above the knee in the QV curve. The SCE MOSFET Q1 subsequently commutates off at the end of the dead-time and D2 conducts as Stage 5 begins. The incoming device, S1, now commutates on (Stage 6), charging the C_{oss} of the SJ MOSFET, S2, to the rail voltage.



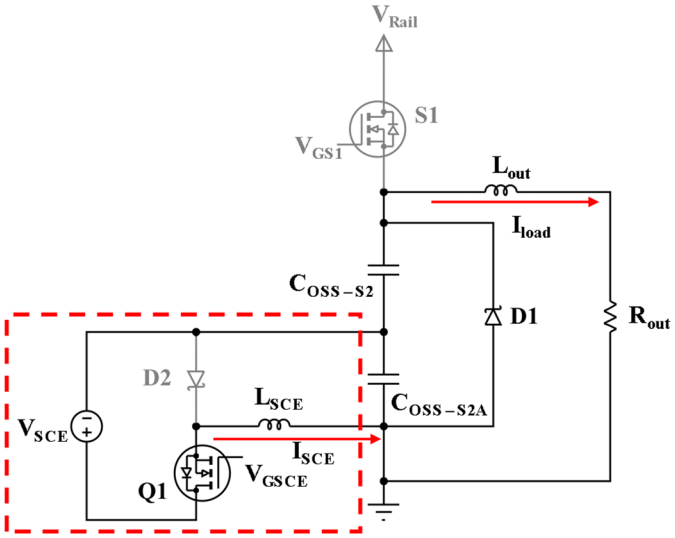
Stage 1



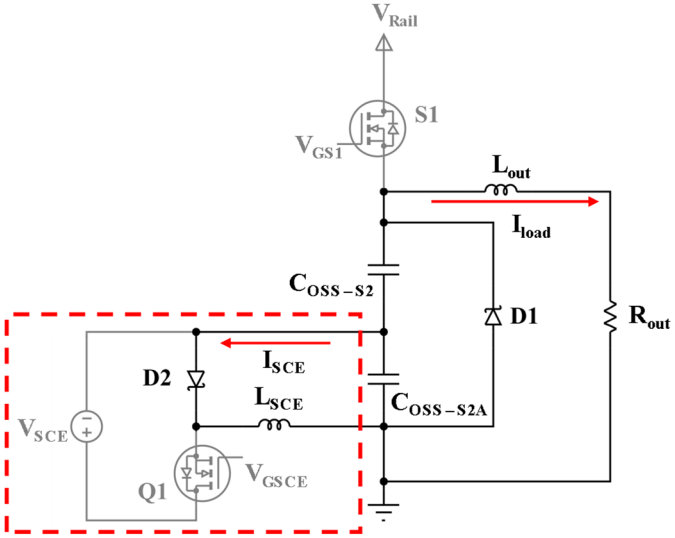
Stage 2



Stage 3



Stage 4



Stage 5

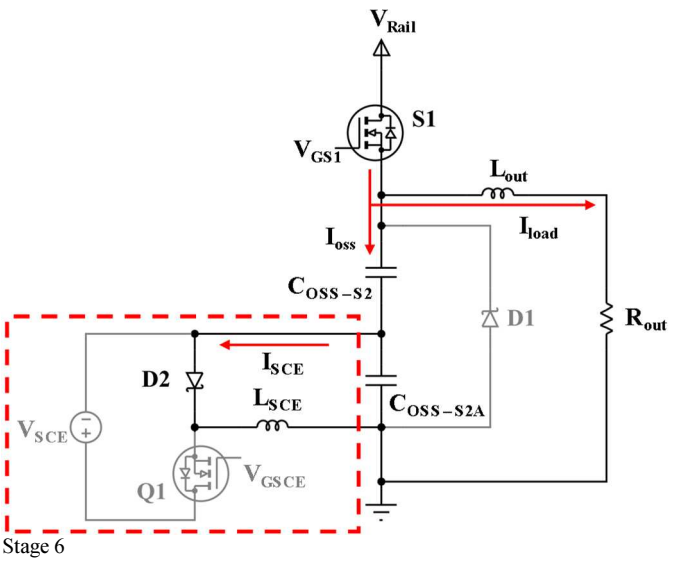


Fig. 8. Six stages of circuit operation.

As shown in Figs. 2 and 4, the bulk of Q_{oss} for the IPW65R019C7 SJ MOSFET is sourced below 40 V. Region C in Fig. 2, represents the energy dissipated in the incoming device during the charging of the synchronous rectifier's (SR) C_{oss} if pre-charging has taken place. A significant reduction is observed when compared to the case where pre-charging has not occurred (the area under the curve i.e. Regions B and C in Fig 2).

IV. Experimental Hardware

Fig. 9 shows a photograph of the experimental power stage. No forced cooling was applied, and the power stage was operated in the buck mode from a 400-V supply, and delivered 22 A and 5 kW to the load. The switching frequency was set to 25 kHz. The SCE inductor L_{SCE}, shown at the bottom of the photograph in Fig. 9, consisted of 10 turns of Litz wire evenly distributed around a Micrometals T37-2 toroidal core [23] giving a measured inductance of 660 nH. Litz wire, constructed from 50 strands of 0.05-mm wire, was used here to help mitigate skin effect losses. The current experienced by the SCE inductor has a high crest factor, which consequently results in a low skin depth. This device is largely a placeholder to enable proof of the SCE concept.

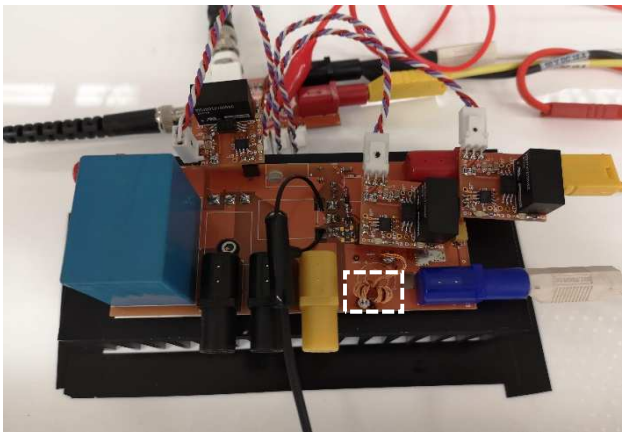


Fig. 9. Photograph of the experimental hardware. The SCE inductor is highlighted by the dotted square.

The semiconductor devices were, as labelled in Fig. 7: S1 and S2 = IPW65R019C7, S2a = NDPL180N10BG, D1 = IDH16G65C6XKSA1, Q1 = IRF135S203, D2 = VB30100S-E3/8W. The SJ MOSFET selected here was chosen using the figure of merit presented in [24]. Assuming the C_{oss} is fully addressed by the SCE circuit the conduction losses become the most dominant loss mechanism. Devices with a low $R_{DS(on)}$ also have a more non-linear QV curve. This benefits circuits employing the SCE technique as the resulting lower knee voltage enables the use of a lower value of V_{SCE}. The SJ MOSFETs were fitted with 8-Ω external gate resistances. These were not optimized here and were selected to achieve low switching losses whilst demonstrating the benefits of implementing the SCE circuitry.

The anti-series MOSFET, S2a, had a 100-V voltage rating, this is higher than required. The anticipated maximum voltage across this device is approximately twice V_{SCE}, at 30 V. Applying a 50% margin results in a 45-V rated device being sufficient and enabling a cheaper part with an equivalent $R_{DS(on)}$ to be used here.

Diode D1 was selected based on its current rating and was a SiC Schottky barrier type. At turn-on, this diode type does not have the same conductivity modulation behaviour of the silicon fast-recovery p-n diode and this is desirable to avoid high transient voltages appearing across the anti-series MOSFET S2a. A device with a lower forward current rating and therefore cost may be implemented, however, this was not explored further here.

The selection of Q1 has also not been optimized and a device with a low $R_{DS(on)}$ was selected to minimise conduction losses during testing. This device was selected to enable a large range of inductance values and SCE circuit conduction periods to be explored.

Adding the current market cost of the SCE circuitry to the SJ MOSFET device cost results in only a small reduction in the cost benefit over a WBG device. The high-volume cost per unit becomes 1.4 and 2.3 times that of the combined SJ MOSFET and SCE circuitry for the SiC MOSFET and GaN HEMT respectively. The cost to implement this technique is therefore significantly lower than a circuit using WBG devices.

For initial experimental purposes, three identical isolated gate drivers were used to control S1, S2/S2a and Q1. A separate 12-V floating supply was used for V_{SCE} to enable investigation of the SCE timings. The PWM signal for S1 was produced using a twin-channel signal generator. A dead-time generation circuit was used to create the complementary signal for the S2/S2a gate driver and introduced 500-ns of delay between the two switching transitions. The second channel of the signal generator was used to provide the PWM waveform for the SCE MOSFET Q1, enabling simple adjustment of the phase and duty for experimental purposes.

V. Experimental Results

Fig. 10 shows initial experimental results obtained using the circuit in Fig. 9. The circuit was operated at a reduced supply voltage V_{Rail} of 40 V with and without the SCE circuitry activated. This allowed an initial comparison to be made without risking device destruction when the SCE circuitry was

deactivated. Peak voltage and current measurements of 140 V and 30 A were measured respectively at the S1 turn-on switching instance without the SCE circuitry. The waveforms show high rates of change. As the supply voltage increases, these peaks and rates of change will also increase, limited only by the channel resistance of the incoming device and stray parasitic inductance. A significant reduction of these peak values can be observed in Fig. 10 when the SCE circuitry is implemented.

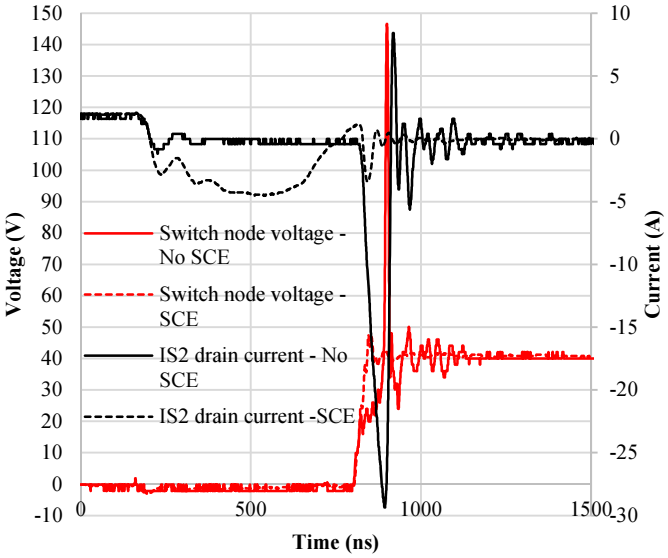


Fig. 10. Drain-source voltage (V_{DS2}) and drain current (I_{S2}) waveforms of the SJ MOSFET S2 (as shown in Fig. 7) with and without SCE.

The supply, V_{Rail}, was disconnected and the SCE circuitry activated to explore the non-forced resonant response of L_{SCE} and the SJ MOSFET C_{oss}. Fig. 12 shows the drain-source voltage and drain current waveforms for the SJ MOSFET S2 using two sizes of inductance (380 nH and 660 nH). Five turns were removed from the inductor outlined in Section IV to attain the 380-nH inductance. The measured inductances differ from those calculated using the toroid's inductance factor, provided by the manufacturer. As the turns number was halved, a four-fold reduction of the inductance was anticipated. The measurement of small inductances is, however, non-trivial. The results show that the performance of the technique is fairly tolerant of variations to L_{SCE} in that the peak voltage attained for the two cases are broadly similar.

Applying a voltage to an LC circuit results in a non-forced resonant response. The time period, T, starting at the instance where the voltage is first applied and ending when the peak voltage is experienced across the capacitance, can be calculated using:

$$T = \pi\sqrt{LC}. \quad (1)$$

The C_{oss} of an SJ MOSFET, however, has a highly non-linear relationship with voltage resulting in a response where the resonant frequency increases as the C_{oss} is charged. The impact of this non-linear relationship on the response is shown in Fig. 11. The large change in capacitance between 0 V and the knee voltage (approximately 17 V), results in the time for the voltage to rise across the C_{oss} up to the knee voltage being significantly longer than that for it to rise from the knee to the peak voltage.

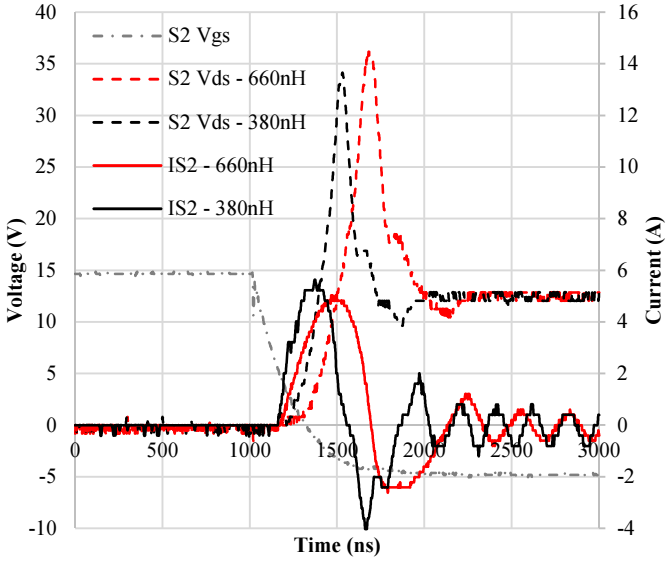


Fig. 11. Drain-source voltage (v_{DS2}) and drain current (I_{S2}) waveforms of the SJ MOSFET S2 (as shown in Fig. 7) for two sizes of L_{SCE} (380 nH and 660 nH).

The SCE circuitry was now activated with the 660-nH L_{SCE} inductor in place. Fig. 12 shows key circuit waveforms from the S1 turn-on switching transition when operating from a 400-V supply voltage and delivering 22 A and 5 kW to the load. Very little overshoot can be observed (approximately 50 V). At approximately 500 ns the C_{oss} of S2 begins to charge as the extraction process commences. The voltage across the SJ MOSFET continues to rise to 35 V where S1 commutates on at 1000 ns.

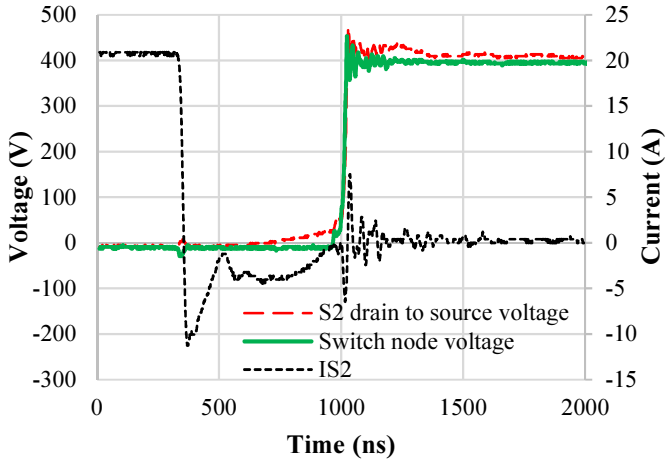


Fig. 12. Drain-source voltage (V_{DS2}), drain-ground voltage (V_{DG2}), and drain current (I_{S2}) waveforms of the SJ MOSFET S2 (as shown in Fig. 7). Measurements were obtained using differential voltage probes and a Rogowski current probe.

Fig. 13 shows a thermal image of the experimental hardware captured at full-load and at thermal steady state. A thermal superposition test was carried out to enable an approximation of

the losses [25]. Through-hole packaged devices were selected to enable their connection to a single heatsink. This facilitated a thermal loss measurement to be carried out which included losses derived from the power stage components, excluding the SCE circuitry. The SCE components were not connected to the main heatsink and a separate electrical loss measurement was carried out. A power stage loss of 29 W was measured using this method and an additional 1 W was recorded at the input of the SCE circuit. This equates to a pessimistic efficiency for the converter of 99.4% at 5 kW. A proportion of the SCE input power will be dissipated by the devices (D1, S2 and S2a) connected to the heatsink and therefore double-counted.

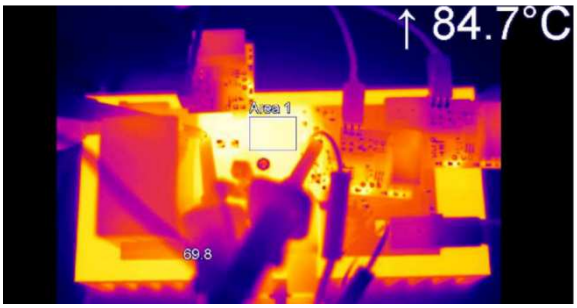


Fig. 13. Thermal image of experimental hardware when running at full-load and in the hard thermal steady-state.

VI. Discussion

The components of the SCE circuitry and the anti-series MOSFETs are readily available low-voltage and inexpensive parts. A significant benefit of SCE over DCI is the reduced current rating requirement of the SiC diode. Both techniques require a SiC Schottky diode, however the injection current and therefore forward current experienced by the diode in the DCI case is significantly higher than that in the SCE circuit. This results in a costlier component being needed due to its higher current rating. Ongoing work is looking into the sizing of these diodes in both cases and the trade-off in the quantity of losses due to the SCE circuits anti-series MOSFET.

State of the art wide band-gap devices are significantly costlier than similarly rated low $R_{DS(on)}$ SJ MOSFETs (at the time of writing this paper low $R_{DS(on)}$ SiC MOSFETs cost approximately 40% more than that of a similar rated SJ MOSFET with SCE circuitry) making this technique an attractive alternative if cost and efficiency are key design criteria. Device selection has, however, not been fully optimized and hence further cost reductions may be achievable.

In this paper, only a non-forced resonant response has been examined using this circuit. Further work is to explore the benefits of a forced response. A novel feature of the circuit is that the anti-series MOSFET provides an L_{SCE} current pre-charging path. Pre-charging L_{SCE} would enable a higher current to be reached prior to commencement of C_{oss} charging. This is expected to result in a faster rise of v_{DS} as the anti-series MOSFET commutates off.

From the initial experimentation carried out in this paper, the results suggest that the gate signal for the SCE MOSFET (Q1) may simply be derived from the dead-time of the complementary PWM signals of the power stage. This significantly reduces the complexity of the gate signal timing. Ongoing work is exploring the impacts of batch variation of the devices' C_{oss} capacitances on the timing instances and the required inductance. Additionally, the optimization of the design of L_{SCE} is also being investigated.

VII. Conclusion

A novel auxiliary resonant switching-aid circuit has been presented for enabling the use of super-junction MOSFETs in bidirectional DC-DC power converters. A full-load efficiency of 99.4% has been measured, which is comparable to that achieved in the literature for the drain current injection technique. The demonstration circuit operated without forced cooling and from a 400-V source whilst delivering 22 A and 5 kW to the load. Although some complexity is added using this technique, the problems associated with the MOSFET's intrinsic diode reverse recovery and output capacitance characteristic have been addressed, enabling high efficiencies to be attained. Significant system-level benefits result from increasing the power stage efficiency, specifically the reduced volume and size of necessary cooling systems.

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