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Hot-Carrier Degradation in Power LDMOS: Selective LOCOS- Versus STI-Based Architecture

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ABSTRACT In this paper, we present an analysis of the degradation induced by hot-carrier stress in new generation power lateral double-diffused MOS (LDMOS) transistors. Two architectures with the same nominal voltage and comparable performance featuring a selective LOCOS and a shallow-trench isolation are investigated by means of constant voltage stress measurements and TCAD simulations. In particular, the on-resistance degradation in linear regime is experimentally extracted and numerically reproduced under different stress conditions. A similar amount of degradation has been reached by the two architectures, although different physical mechanisms contribute to the creation of the interface states. By using a recently developed physics-based degradation model, it has been possible to distinguish the damage due to collisions of single high-energetic electrons (single-particle events) and the contribution of colder electrons impinging on the silicon/oxide interface (multiple-particle events). A clear dominance of the single-electron collisions has been found in the case of LOCOS structure, whereas the multiple-particle effect plays a clear role in STI-based device at larger gate-voltage stress.

INDEX TERMS Hot-carrier degradation/stress, on-resistance degradation, LOCOS, STI, single-particle process, multiple-particle process, TCAD simulation.

I. INTRODUCTION

Lateral double-diffused MOS (LDMOS) power transistor is broadly used for relatively high voltage applications and smart power technologies due to its low on-resistance (R_{ON}) [1], [2] and to its compatibility with standard CMOS process [3], [4].

As the technology scales down, the development of the devices in the new technology platforms becomes more challenging in terms of optimization of performance and reliability [5]. Usually, the shallow-trench isolation (STI) is adopted in the drift region as field insulator to further increase the voltage rate with limited device area [6]. R_{ON} can be further reduced by optimizing the doping concentration. However, it is well known that current crowing at the STI corner leads to significant hot-carrier degradation, worsening the device reliability [7]. In particular, when the device operates in ON-state regime, electrons can gain sufficient kinetic energy (hot-carriers) necessary to create interface states followed by charge trapping causing the reduction of the device performance [8]. For this reason, the LOCOS process has been recently re-engineered for power devices in order to obtain customized shapes [9].

Although the first observation of hot-carrier degradation phenomenon in LDMOS transistors dates back to over twenty years ago [10], the underlying different physical mechanisms and their playing role in device degradation are not completely clear yet. As a result, there is still a strong interest in understanding and controlling the hot-carrier related degradation in power LDMOS transistors, especially for the Semiconductor Industries.

Recently, many studies have been proposed in [11]–[18]. Li *et al.* [11] have shown that by optimizing the drift region layout, more specifically, by reducing the overlap between N-drift region and poly-gate and by extending the overlap implantation between N-drift and P-well, the hot-carrier degradation is attenuated since the lateral electric field is

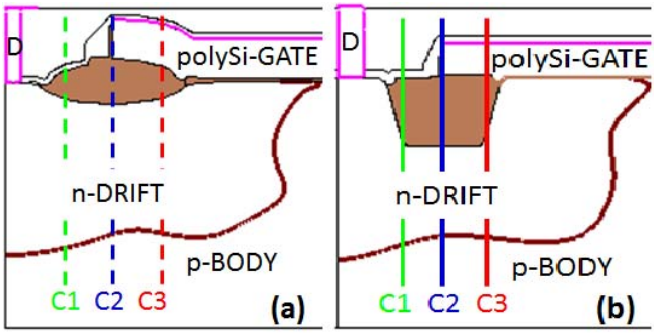

FIGURE 1. Sketch of the N-drift region in the case of (a) selective LOCOS- and (b) STI-based LDMOS transistors (not in scale). Cuts C1, C2, and C3 represent the sections where interface (oxide/N-drift) trapped charge is monitored.

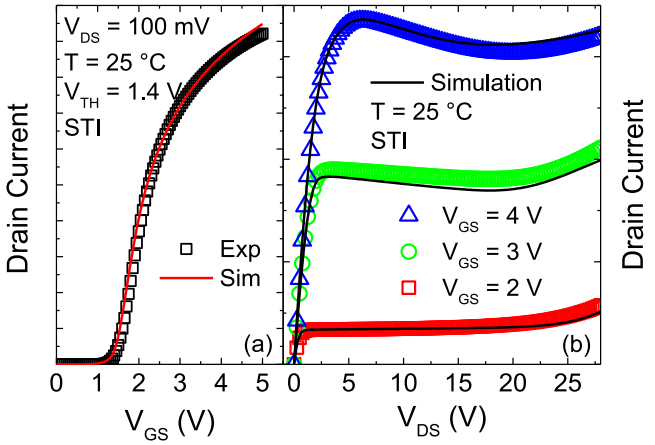

FIGURE 2. Experimental (symbols) and simulated (line) (a) transfer- and (b) output-characteristics of the STI-based architecture reported in Fig. 1b. Similar curves for LOCOS have been reported in [18].

reduced and the impact ionization is moved away from the Si/SiO_2 interface.

In [13], a novel device structure with a poly-gate partly recessed into the field oxide has been presented to optimize the on-resistance degradation at the worst HCS condition, whereas the impact of the STI angle on hot-carrier stress has been investigated in [15].

Sharma *et al.* [17], by studying the hot-carrier degradation in n- and p-channel LDMOS transistors found out that the role of the colder (multiple) carriers must be taken into account in order to numerically and accurately reproduce the on-resistance degradation for both short and long stress times.

Finally in [18], by performing long-term HC stress at different biases and temperatures, we have demonstrated that in the case of a customized thick oxide architecture (selective LOCOS), the dominant role inducing hot-carrier degradation is played by the single highly energetic electrons.

In this paper, a comparison study of the degradation induced by hot-carrier stress in selective LOCOS- and STI-based n-channel LDMOS transistors is reported, aiming at understanding the different underlying mechanisms and how their roles depend on the type of device architecture. By combining experimental and simulation analyses, it has been demonstrated that similar degradation shifts can be achieved in architectures with similar performances, although different physical mechanisms contribute to the interface-trap generation.

II. DEVICES STRUCTURE AND TCAD CALIBRATION

N-channel selective LOCOS- and STI-based power LDMOS transistors, fabricated on 200mm silicon wafers by STMicroelectronics, are considered and sketched in Fig. 1a and 1b, respectively. Doping profiles and key geometrical dimensions have been properly designed to secure same medium voltage capability with the two different field oxide architectures. A sketch of the drift region is shown in Fig. 1, representing the region where, as detailed in the following, the major contribution to degradation during hot-carrier stress is localized.

In order to investigate the device degradation due to hot-carrier stress (HCS) and to understand which are the dominant underlying physical mechanisms, experimental analyses have been performed combined with TCAD simulations.

The device degradation has been experimentally carried out on-wafer by means of constant voltage stress (CVS) measurements. Consequently, HCS induced degradation is extracted by monitoring the R_{ON} shift in linear regime.

Finally, the simulated structures have been defined and calibrated in the frame of the Sentaurus TCAD simulator [19] considering the geometric characteristics and the material properties of the devices under test (DUT). In particular, the transport problem has been solved by using the electro-thermal model, which couples the drift-diffusion transport with the heat flow equation. Special consideration has been given to the choice of the simulation set-up. The impurity concentration within the cross section has been inferred from process simulation results. All measured devices have widths that are significantly large so to prevent undesired non-uniformity along the width of the device.

A tuning of the deck was carried out through the comparison with measured turn-on and output curves. More specifically, acceptor traps have been added at the Si/SiO_2 interface of the channel region in order to accurately predict the measured threshold voltage and trans-conductance, as shown in Fig. 2a for the STI-based device.

In order to reproduce the self-heating effects, proper thermal boundary conditions have been applied in the numerical set-up calibrated against the measured output curves. In addition, the UniBo impact-ionization model available in the Synopsys tool has been selected due to its extended field and temperature validity range [19], [20]. It has been slightly tuned to find an accurate prediction of the avalanche onset at larger V_{DS} in the STI-based device (Fig. 2b).

The same procedure has been adopted also for the case of the selective LOCOS device as reported in detail in [18].

III. HOT-CARRIER STRESS DEGRADATION MODEL

In order to model hot-carrier stress, the numerical solution of the full-band Boltzmann Transport Equation (BTE) implemented in [19] has been used to predict the energetic distribution of hot electrons. The physics-based model recently developed in [21] has been adopted in the numerical analysis as it has been demonstrated to be specifically suited for the TCAD analysis of the parameter drifts under electrical stress of LDMOS devices.

Different competing mechanisms such as single-particle (SP), multiple-particle (MP) and field-enhanced thermal interaction (TH) may contribute to the de-passivation of the electrically inactive bonds at the silicon/oxide interface.

SP process is related to a single high energetic particle which can induce a bond-breakage event in a single collision [17], [21], whereas MP-process is triggered by a series of colder carriers which subsequently impinge the interface causing the bond breaking [21], [22]. Finally, the TH-process is related to thermal interactions with the lattice. In particular, due to high lattice temperature, phonons can excite the silicon interface molecules and eventually break their bonds [21], [23].

The degradation model gives as output the interface-trap density $N_{it}(t)$ mapped at each (x, y) position along the Si/SiO_2 interface of the device, allowing to directly simulate the turn-on curve in stressed conditions at any stress time. The generated N_{it} distribution has been incorporated in the simulation set-up by assuming an acceptor trap density with a single energy level at mid-gap, leading to fully occupied interface states. The degradation model parameters have been calibrated against experiments and validated over an extended range of biases and temperatures on both devices as illustrated in the following.

IV. RESULTS AND DISCUSSION

Fig. 3 shows the simulated body current for both selective LOCOS- and STI-based LDMOS transistors. It is worth noting that it was not possible to experimentally monitor the body current because body and source contacts are internally short-circuited in the real devices.

In both devices, an initial body current rise is shown. It is attributed to the steep increase of the channel current in the near-threshold regime, with carriers experiencing a region of high electric field close to the channel. Subsequently, by further increasing the gate bias the impact ionization peak moves toward the drain (shown in [18]) and the body current rises again to larger values due to the Kirk effect at the drain edge.

By comparing the two architectures, it is possible to note that the STI-device features a lower body current peak at relatively low gate voltages, hence a lower impact-ionization generation. Vice versa, when the electric field peak is moved to the drain region at high V_{GS}, the STI-LDMOS shows a larger body current increase, indicating a larger local electric field in the structure. The different body current values

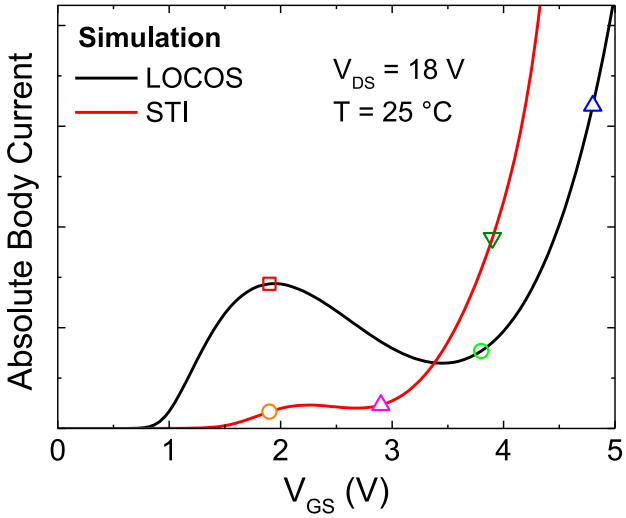

FIGURE 3. Simulated body current in the case of selective LOCOS- and STI-based LDMOS transistors. Higher impact ionization generation (body current peak) is shown in the case of LOCOS architecture. No y-axis is displayed for confidentiality reasons.

are the global result of the different field plate architectures leading to different doping profiles and geometrical dimensions for device optimization.

By considering the trend of the simulated body currents in Fig. 3, three different stress conditions for each architecture have been chosen to verify a possible correlation between impact ionization (hot-carrier) and device HCS degradation.

The experimental (symbols) and simulated (lines) on-resistance degradation curves extracted in linear regime for the three selected stress conditions in the case of selective LOCOS- and STI-based devices is reported in Figs. 4a and 4b, respectively.

First, by focusing on the experimental data (symbols) it is possible to notice that a clear correlation between simulated body current (Fig. 3) and R_{ON} degradation is only shown in the case of LOCOS devices (Fig. 4a). More specifically, the higher the body current (absolute value), the larger the extracted ΔR_{ON}. Differently, the STI-LDMOS shows significant changes in the degradation curves even if the body current values are similar (see the curves at $V_{GS} = 1.9$ V and 2.9 V in Fig. 4b). Moreover, at larger gate biases ($V_{GS} = 3.9$ V) the significant higher body current does not result in a higher ΔR_{ON} as for the LOCOS case ($V_{GS} = 4.8$ V). These differences suggest that the on-resistance degradation in the two architectures is triggered by different underlying physical mechanisms.

In general, a clear link between body current, hence impact ionization generation, and R_{ON} degradation suggests that the single high energetic carrier (hot-carrier) is the dominant source causing a bond-breaking event in a single collision, leading to interface-traps generation. For this reason, only the single-particle process was incorporated in the HCS degradation model in order to simulate the R_{ON} degradation in the LOCOS devices [18]. The accurate agreement

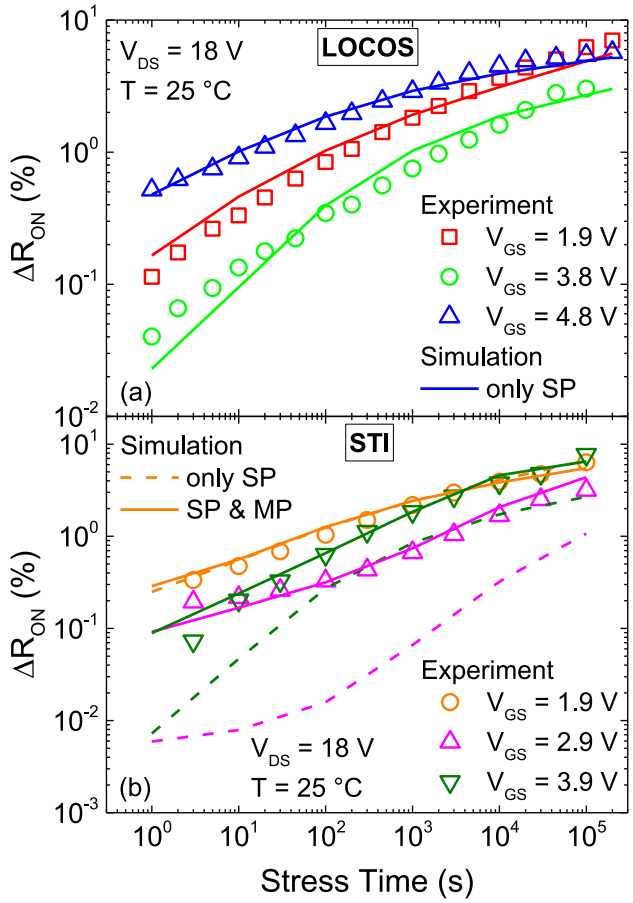

FIGURE 4. Experimental and simulated R_{ON} degradation in (a) selective LOCOS- and (b) STI-based LDMOS. While a direct correlation between body current (Fig. 3) and ΔR_{ON} is shown in LOCOS devices (a), same behavior is not reported for STI devices (b).

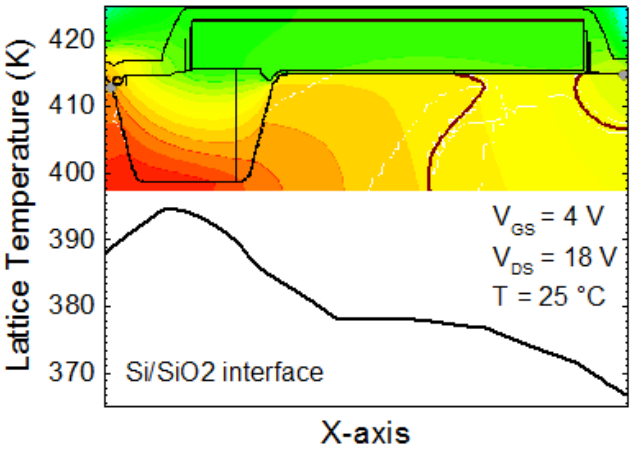

FIGURE 5. Lattice temperature, due to self-heating effect, along the silicon/oxide interface in the case of STI architecture at high gate voltage. It is worth noting that LOCOS device feature a lower temperature (not shown).

of the numerical predictions with experiments shown in Fig. 4a confirms that the single-electron HCS process is the most relevant one for this kind of architecture.

Differently, by adopting the same approach in the case of STI-based LDMOS, i.e., simulating the R_{ON} degradation by simply accounting for the SP process, a significant underestimation of the degradation curves has been obtained as shown by the dashed lines in Fig. 4b, except for $V_{GS} = 1.9$ V where the single particle process turns out to be the dominant degradation mechanism.

Therefore, in addition to the SP contribution, the multiple-particle process has been incorporated in the TCAD degradation simulation and the experimental R_{ON} degradation curves have been accurately reproduced also in the case of the STI device (solid lines in Fig. 4b), confirming that different physical degradation mechanisms occur in the two architectures.

It is worth noting that the corresponding models (single- and multiple-particle contributions) have been initially calibrated against the R_{ON} degradation experiments, mainly by changing the fitting parameters which modulate the reaction cross-section and the probabilities of defect generation [18], [21], in order to tune the magnitude and slope of the drift curves. Slightly different parameters have been adopted for the two architectures. In particular, the different probabilities for defects generation are due to the simultaneous presence of two competing mechanisms in STI (SP and MP) rather than only one in LOCOS (SP), whereas the different constant in the reaction cross-section should be ascribed to the different oxide interface in the two structures. More specifically, the silicon is chemically etched and differently crystal-oriented (side walls) in STI devices.

The thermal contribution (TH process) to HCS degradation has not been accounted for in the simulation since it is strongly dependent on the lattice temperature and thus becomes crucial in high power devices where the current rating induces relevant self-heating effects. By observing Fig. 5, a relatively low lattice temperature along the Si/SiO_2 interface of the STI device is shown. In particular, a temperature lower than 125 °C is shown although a high gate voltage is applied (close to the maximum nominal value), confirming that TH-related trap generation is negligible for this device class voltage.

It is worth noting that the maximum temperature in the case of LOCOS devices at the same drain and overdrive voltage is even lower than the STI-based LDMOS one (not shown).

No relevant threshold voltage shift (within 1% at 10^5 s of stress) has been experimentally observed for the examined gate-voltage window in long-term stressed devices in both structures (not shown). Therefore, no significant degradation is expected in the channel region and hence the field-enhanced thermal contribution at large gate biases, usually found in high power/voltage LDMOS transistors, is negligible. This is also consistent with the limited increase of temperature induced by self-heating in the channel region (Fig. 5).

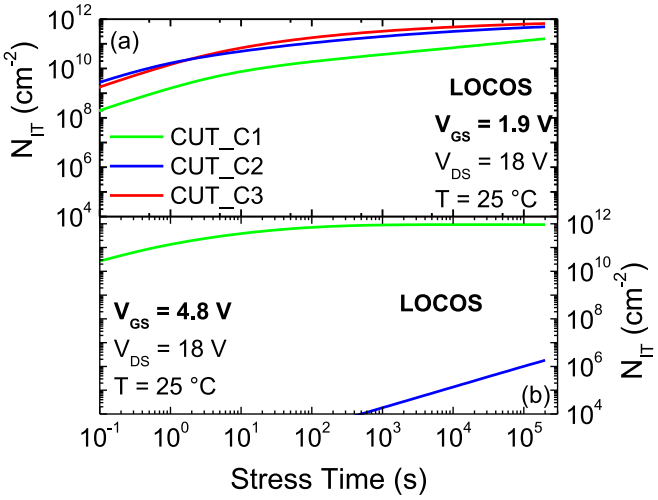

FIGURE 6. Interface trap concentration versus the stress time in correspondence to the cuts shown in Fig. 1 (C1 is the closest cut to the drain side) for the stress conditions (a) V_{GS} = 1.9 V and (b) V_{GS} = 4.8 V at V_{DS} = 18 V and T = 25 °C. It is worth noting that cut C3 is not shown in (b) because the N_{IT} generation is below 10^4 cm^{-2}, hence negligible.

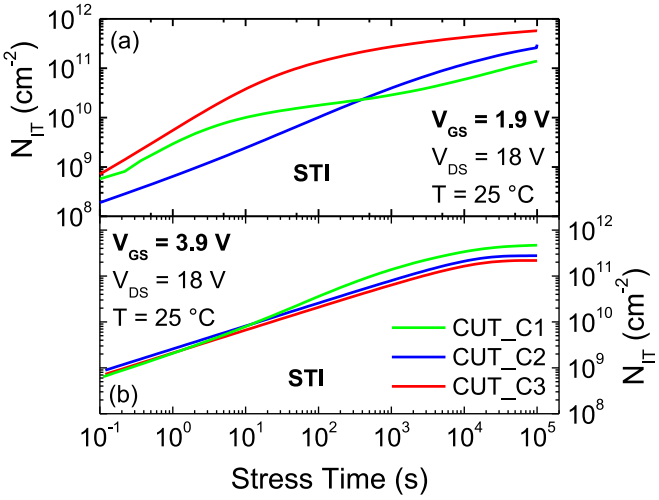

FIGURE 7. Interface trap concentration versus the stress time in correspondence of the cuts shown in Fig. 1 (C1 is the closest cut to the drain side) for the stress conditions (a) V_{GS} = 1.9 V and (b) V_{GS} = 3.9 V at V_{DS} = 18 V and T = 25 °C. Similar results have been shown in [18] for LOCOS devices.

As shown in the case of LOCOS devices in [18], the simulated interface trap creation can be monitored during the stress at different positions along the Si/SiO_2 interface. Similar cut positions have been monitored also in the STI device as indicated in Fig. 1, allowing for a direct comparison of the critical hot spots in both devices at different stress biases. In Figs. 6 and 7, the interface-trap concentrations as a function of time are reported for the LOCOS and STI structures, respectively.

By observing Fig. 7, it is possible to note that at relatively low gate voltages (a) the highest and dominant interface trap creation occurs close to the source-side corner of the STI (C3 of Fig. 1), whereas at relatively high V_{GS} (b) the

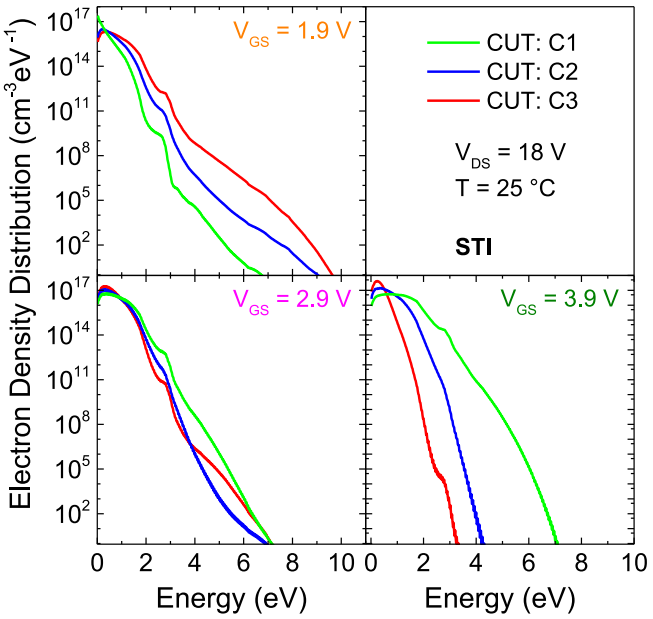

FIGURE 8. Electron density distribution as a function of different gate voltages, evaluated at the Si/SiO_2 interface of the STI in correspondence of the cutline shown in Fig. 1.

trap generation is spread on the whole STI bottom part, and becomes slightly pronounced at the drain edge (C1) for longer stress times.

This is consistent with the physical mechanisms behind the interface trap generation. In particular, at low gate voltages the single-particle is the dominant process causing R_{ON} degradation in both devices. At such bias condition electrons experience a region of high electric field close to the channel, hence close to the STI corner or to the LOCOS bird's beak on the source side, gaining high kinetic energy and favoring interface-trap creation in that region.

By increasing the gate bias, in both structures the longitudinal electric field peak is redistributed and moves toward the drain contact alleviating the hot-carriers contribution. On the other hand, the higher drain current density provides many colder carriers at the STI interface able to interact with molecules and break bonds. The STI depth induces a large current density at the Si/SiO_2 interface, leading to a significant trap formation along the whole path (Fig. 7b), which was not visible in the LOCOS case.

Fig. 8 strengthens the latter statements showing the electron energy distribution as a function of different gate biases at the Si/SiO_2 interface in correspondence of the cut lines shown in Fig. 7. In particular, it is possible to note that by increasing the gate voltage the electron density remains high in all three positions along the STI, while energy distribution shows a clear reduction of the hot electrons, suggesting a dominant presence of colder carriers and the reduction of hot electrons.

In the case of selective LOCOS, the electron density at the interface tends to decrease by increasing the gate voltage,

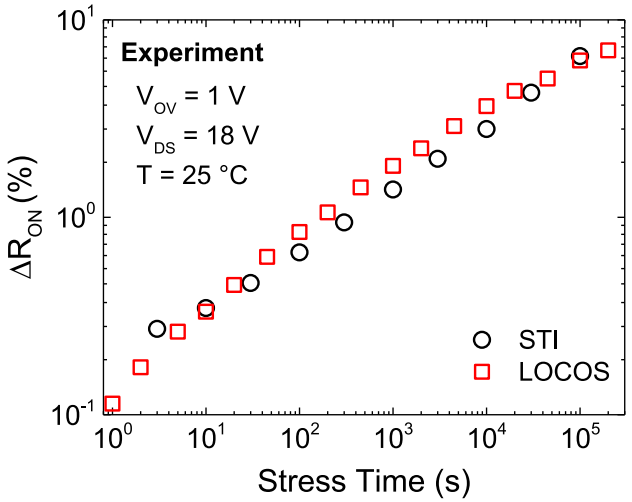

FIGURE 9. Experimental on-resistance degradation in the case of selective LOCOS- and STI-based LDMOS transistors at the same overdrive and drain voltage.

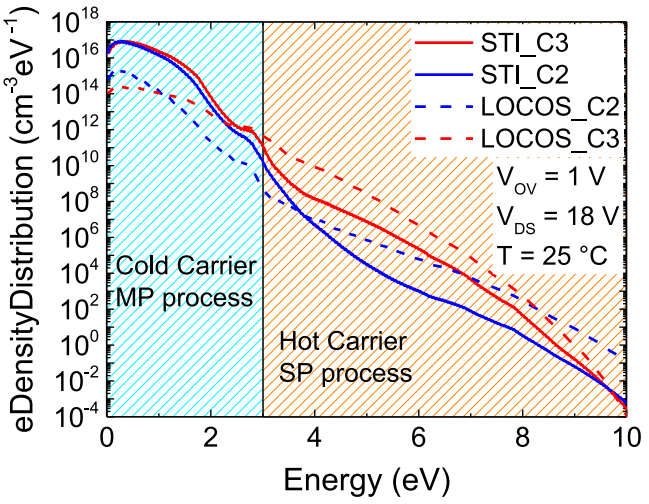

FIGURE 10. Electron density distribution evaluated at the Si/SiO_2 interface (cuts C2 and C3) of the STI and LOCOS devices at the stress condition considered in Fig. 9.

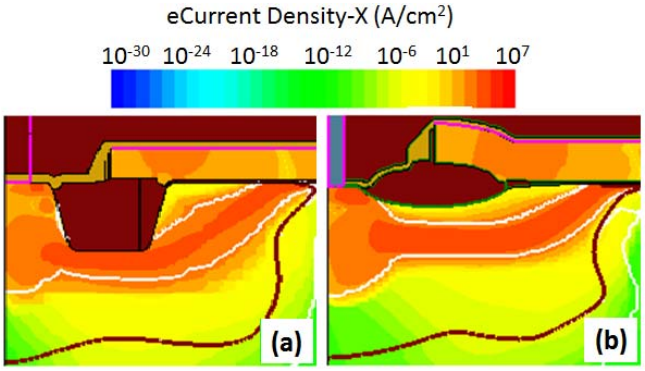

FIGURE 11. Longitudinal electrons current density in the case of (a) STI- and (b) selective LOCOS-based LDMOS transistors at V_{OV} = 1 V, V_{DS} = 18 V and T = 25 °C. Since STI region is deeper than LOCOS one, electrons current is confined at the STI bottom.

thus no cold particles are available to damage the oxide. Since the single high energetic electron is the dominant degradation mechanism independently of the gate bias, the region interested to interface trap creation is linked to the position of the impact ionization peak, i.e., the region where electrons experience the highest kinetic energy. In particular, by increasing the gate voltage the interface trap generation clearly moves from source-side to drain-side of the LOCOS region [18].

Finally, in order to further and directly compare selective LOCOS- and STI-based architectures, hot-carrier stresses at the same overdrive voltage have been performed and shown in Fig. 9. A similar amount of R_{ON} degradation is reported for both architectures although different underlying physical mechanisms occur. As an overdrive of 1 V has been considered, the most significant contribution to degradation is expected to be localized at the source-side corner and in the middle of the isolation region (C2 and C3 positions). By comparing the body currents in Fig. 3, a much lower amount of hot electrons is expected in the STI case. In Fig. 10, the electron energy distribution at the Si/SiO_2 interface is shown in both architectures for the stress condition considered in Fig. 9. It is clearly found that the STI device features a higher density of colder carriers (< 3 eV), whereas the LOCOS architecture shows a higher density of hot-carriers (> 3 eV).

On the overall, the selective LOCOS architecture is significantly sensitive to hot-carrier induced degradation (single-particle), whereas in the STI device the lower single high energetic electron contribution is compensated by the colder carriers (multiple-particle), resulting in a similar R_{ON} degradation.

The role played by the insulator depth is clearly visible in Fig. 11, showing the current density in the two devices at the same gate overdrive. In the case of the LOCOS structure, the source-to-drain current flows far away from Si/SiO_2 interface, thus a low number of colder electrons is present at the interface. In the case of the STI device, being the etched trench deeper in silicon, the current flows confined/compressed at the interface of the STI bottom. As a result, a higher number of electrons interact with the molecules at the interface. A similar result was found in [12], showing the simulated HCS drift curves of STI-based LDMOS devices with different oxide thicknesses: in a thinner STI case, the concurrent effects of a lower surface current density and a higher carrier temperature are observed with respect to the thicker one, leading to limited HCS drift variations.

V. CONCLUSION

In this paper, we investigated the degradation induced by hot-carrier stress in new generation power LDMOS transistors, exploiting two different architectures such as selective LOCOS and Shallow-Trench Isolation.

In particular, the on-resistance degradation in linear regime has been experimentally evaluated under different stress conditions and numerically reproduced to understand the different underlying physical mechanisms affecting the device reliability during ON-state operation.

As the device technology is very similar, the performance and reliability can be directly compared to understand the role played by the different insulating structures on the hot-carrier stress degradation. The main results of this investigation is the determination of the role played by single-particle and multiple-particle processes in the two cases.

The STI devices clearly show a significant improvement in terms of reduced impact-ionization contribution to the body current due to the global result of different doping profiles and geometrical dimensions, which leads to a clear reduction of the single-particle events during long-term hot-carrier degradation. However, due to the depth of the STI trench, a high current density is experienced at the STI bottom promoting trap generation due to multiple-particle processes, which eventually leads to comparable hot-carrier stress degradation.

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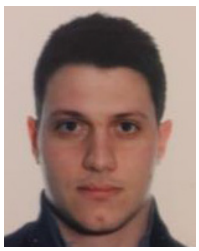

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