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**REVIEW**

# Perovskite solar cells: short lifetime and hysteresis behaviour of current–voltage characteristics

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## Abstract

Perovskite solar cells have shown an impressive efficiency improvement over the past ~ 10 years achieving ~ 23% to date. However, the lifetime and instability of device characteristics are real issues to understand and solve before scaling up and commercialisation of these devices. Researchers have attempted to understand the hysteresis behaviour of current–voltage (I–V) curves in terms of mechanisms such as migration of several ions across the device and the effects of electronic defects during measurements. This review contributes to this scientific debate by presenting similar behaviour observed and reported for devices based on inorganic semiconductors. In established inorganic semiconductor thin film solar cells, both short lifetime and hysteresis have been observed, described and understood in terms of effects of numerous electronic defect levels. Therefore, the situation may be very similar and it is important to identify and reduce defects to remove this un-desirable behaviour from perovskite solar cells. After considering the wealth of experimental results reported in the literature, the conclusion made is the dominating mechanism of I–V hysteresis is due to electronic defects available within the device structure. Suggestions have been made for potential researchers to experimentally investigate the phenomenon in order to finally put an end to this debate. As the defect levels and their concentrations are reduced, the initial efficiency, stability and the lifetime of perovskite solar cells should improve further, beyond the current situation.

## 1 Introduction

Perovskite solar cells (PSCs) have shown a remarkable efficiency improvement in recent years achieving lab scale devices with ~ 23% conversion efficiency [1]. However, the stability and lifetime of these devices are real challenges and researchers are focussing to solve these issues at present. Variations of the measured current–voltage (I–V) characteristics of these devices are puzzling the research community for past few years. One major hindrance in the way of understanding these phenomena probably is a lack of mutual interpretation of concepts and different presentation habits developed in the two communities of electrochemists working with dye sensitised or PSCs and solid-state physicists working with inorganic thin film solar cells. Our group has recently attempted to bridge this gap, by analysing PSCs as compared to inorganic thin film solar cells [2]. The aim of this review is to explain the I–V hysteresis and other instabilities of PSCs in parallel to that of the inorganic thin film solar cells.

The shape and the device parameters; open circuit voltage ($V_{oc}$), short circuit current density ($J_{sc}$), fill factor (FF) and the conversion efficiency ($\eta\%$) depend on how the I–V curves are measured. The rate and the voltage range of data collection, and the direction of applying external bias voltage change the shape of I–V curves and hence the device parameters. In general I–V curves measured starting from reverse bias voltages show better characteristics than those measured starting from forward bias voltages [3–10]. This behaviour can also be other way around depending on the materials and device processing steps used [5]. Researchers have attempted to explain this behaviour in terms of ionic migration, polarisation effects and electronic charge trapping and de-trapping process within these devices [11–16].

The aim of this review paper is to share main author's similar experiences with devices based on commercially established inorganic semiconductors like cadmium telluride (CdTe), gallium arsenide and its aluminium alloy (GaAs/AlGaAs) and copper indium gallium di-selenide (CuInGaSe$_2$ or CIGS). Authors summarise their experimental results observed and reported in the literature [17–19], and explain

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**Fig. 1** A typical hysteresis observed for ITO/PEDOT:PSS/ Perovskite/PCBM/BCP/Au perovskite solar cells when measured from reverse to forward and forward to reverse directions with scan rate of 10 mVs⁻¹
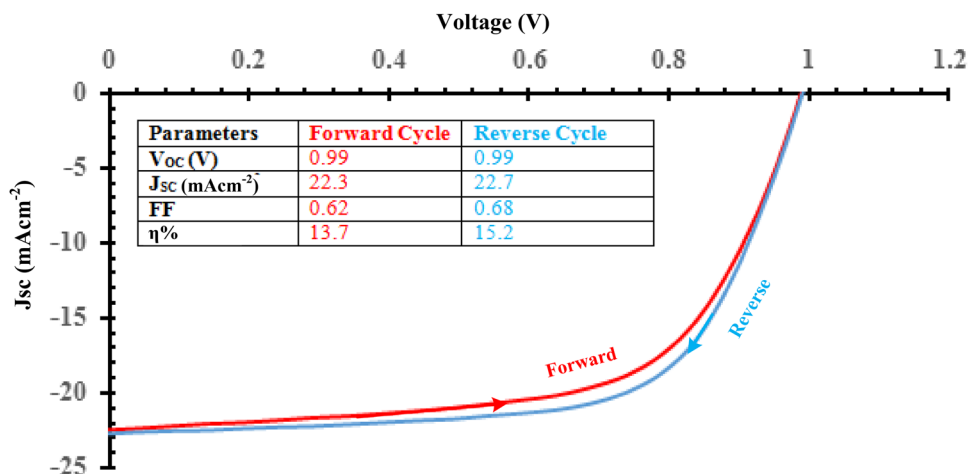


these variations with the effects of electronic defects. Instead of ionic migration and polarisation affects the behaviour of these I–V characteristics, the phenomenon is described in terms of slow "trapping" and "de-trapping" of charge carriers in defects within the materials and the device structure. The voltage biasing of the devices and exposure to light intensity, change the occupation of native defects within solar cells and drastically change the shape and nature of the I–V curves. This review is to share this experience with the perovskite research community to help understand the PSCs and hence improve the stability, lifetime, and conversion efficiency beyond the reported highest value of ~23%.

## 2 Experimental observations on perovskite solar cells

Reading through the wealth of experimental results on PSCs with high efficiencies (say above ~15%) show two clear challenges to solve. The first is the short lifetime of the devices; initially observed high efficiencies rapidly reduce down removing its rectifying properties and hence the photovoltaic (PV) activity. The second issue is the stability of the device when measuring the initial conversion efficiency. These two issues are the main subjects discussed in this review article. Most of the reported results show better I–V characteristics when measurements have been carried out by scanning from reverse bias end towards high forward bias voltages. If the measurement direction changes from forward bias end towards reverse bias, a deteriorated I–V curve is produced yielding poor device parameters. For example, a typical measurement carried out with scan rate of 10 mVs⁻¹, in our laboratories is shown in Fig. 1. The details of preparation and measurements are described in reference [2]. Because of this high variability of I–V curves, reporting device parameters can be un-reliable. Trying to understand this detrimental behaviour is the main purpose of this review paper.

## 3 Experimental observations on inorganic semiconductors

Variations in I–V curves measured are common in electronic devices fabricated with commercially established inorganic semiconductors like CdTe, GaAs/AlGaAs and CIGS. The full details can be found in several references [17–19] and only a brief description is given here for comparison with results observed from PSCs.

### 3.1 Rectifying diodes based on n-CdTe

In references [17] and [19], the variation of I–V curves measured under dark conditions are reported for ohmic-contact/n-CdTe/Au-Sb structures (Schottky diodes) fabricated on bulk n-CdTe wafers. These diodes show excellent rectification properties and behave as solar cells under illumination. They do not show any hysteresis when measured under normal conditions. However, the I–V curves measured can be drastically different when a fixed forward or reverse bias voltage is applied under dark conditions, and then immediately measured under dark conditions (see Fig. 2a).

As shown in Fig. 2a, I–V curve deteriorates drastically, when a forward bias is applied and it can be reverted back to the original I–V curve when a fixed reverse bias voltage is applied in dark conditions. For some diodes, this change is reversible but for many others, this variation ceases after a few cycles. Under illumination, the diode is equivalent to forward biasing with voltage $V_{oc}$ and the variation of I–V is similar to that of fixed forward biasing in dark conditions.

There was a lengthy scientific debate in the late 1980s among researchers involved in this work to describe these variations [21]. Both ionic migration and effects of slow electronic traps present at the interface were the main suggestions, but after experimentally detecting a ladder of five defect levels (see Fig. 2b), the latter was confirmed as
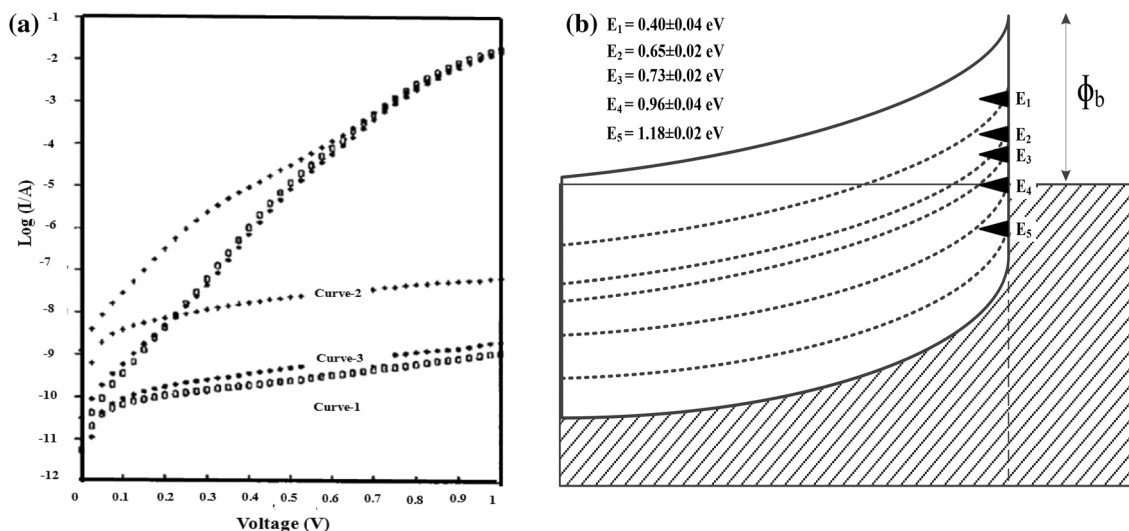
Fig. 2 **a** Typical changes in I–V characteristics of n-CdTe/Au-Sb Schottky diodes fabricated on bulk n-CdTe single crystals, with applied electrical stress. Curve-1: The I–V curve of an as-made diode; Curve-2: The deteriorated I–V curve of the same diode after application of 1.0 V forward bias for 1 h in dark conditions; Curve-3: The improved I–V curve after reversal to the original position when 1.0 V reverse bias was applied for 10 h under dark conditions. **b** The energy band diagram showing the experimentally observed ladder of defect levels ($E_1$,…,$E_5$) at n-CdTe/metal interface [20]
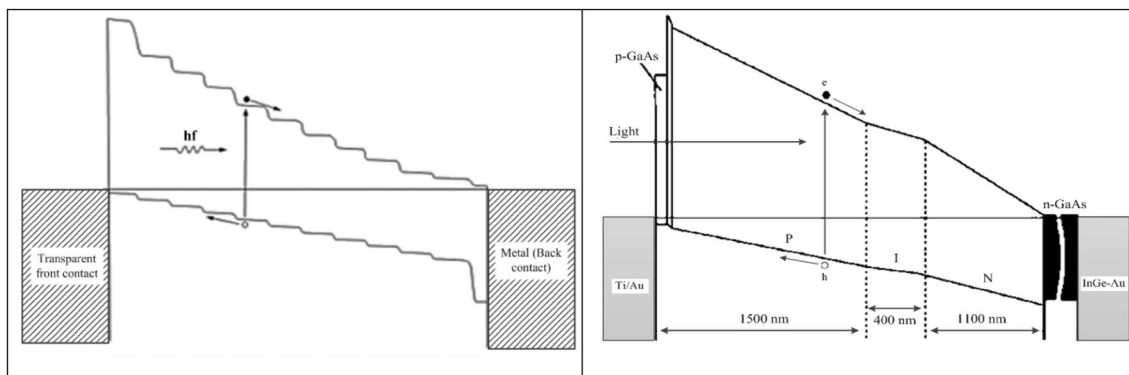


Fig. 3 The design of the graded bandgap solar cell [22, 23] and the closest sketch of the energy band diagram expected for Ti–Au/AlGaAs/GaAs/InGe-Au structure after epitaxial growth using the metalorganic chemical vapour deposition (MOCVD)

the appropriate description. These defects also lead to pin the Fermi level (FL) at one of the defect levels and switch between defects when the conditions are changed. Switching of FL from a position producing high potential barrier to a low potential barrier, suddenly removes the rectifying property and hence its photovoltaic (PV) activity. Subsequent work in this area over the past three decades confirmed the effects of electronic defects, especially in thin film solar cells.

## 3.2 Solar cells based on GaAs/AlGaAs

In references [18] and [19], similar instabilities of GaAs/AlGaAs graded bandgap, lab-scale devices were reported.

The graded bandgap solar cells were designed (see Fig. 3) [22], fabricated using MOVPE grown GaAs/AlGaAs, and the first batch achieved devices with independently verified $V_{oc} = 1175$ mV, $J_{sc} = 12$ mAcm$^{-2}$, FF = 0.85 and efficiency ~ 12% [23] values. The second batch with doping improvements showed enhanced efficiencies of ~ 20% [24]. These devices were tested to observe any variations of I–V curves after applying different electrical stresses. This exercise was mainly performed in order to test this phenomenon in devices fabricated with epitaxially grown crystalline materials.

The above devices with total thickness of ~ 3 μm, showed excellent rectification properties at normal laboratory conditions. The harsh biasing voltages were applied while stored
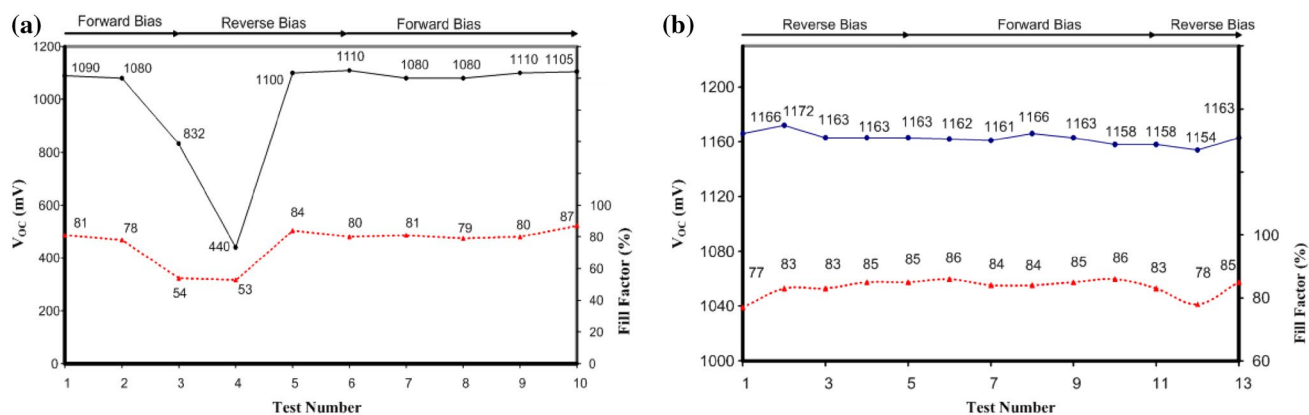
**Fig. 4** Two examples to show the variation of $V_{oc}$ and FF as a function of applied forward- and reverse-bias electrical stresses on a 0.5 mm diameter solar cell, and a $3 \times 3$ mm$^2$ solar cell

in the dark and immediately measured for solar cell parameters under AM1.5 conditions. Examples of harsh conditions were either strong light intensities under many-suns illumination (light soaking) or applications of bias voltages for a longer period, under dark conditions. Figure 4 shows the variations of $V_{oc}$ and FF after fixed forward and reverse biasing. The $V_{oc}$ values were highly variable, changing from ~1080 to ~440 mV and reversible for some diodes. For others, this variation ceased after a while or showed constant values after many stressing cycles. A self-healing nature was observed for some devices.

The devices were fabricated using high temperature (~600 °C) epitaxially grown GaAs/AlGaAs materials. This is one of the well-researched crystalline semiconductors but there are numerous experimentally observed electronic defects [25, 26]. The devices measured under normal conditions were excellent producing similar I–V curves in six different laboratories, including NREL in the US. But application of severe stress showed these variations in I–V curves and device parameters. C–V measurements at high frequencies (1 MHz) gave depletion layer properties avoiding effects of slow traps. Similar to n-CdTe/metal Schottky barriers, the ion migrations in these crystalline materials were ruled out and these variations were explained in terms of filling and emptying of "slow electronic traps". The effects of such traps also disappeared in some cases showing self-healing, presumably due to saturation and stabilisation of some defects during measurement cycles.

### 3.3 Solar panels based on CIGS

These effects were also observed for large area thin film solar panels. Commercial CIGS solar panels manufactured by Showa Shell in Japan also showed this variation and more details can be found in references [19, 27]. The initial conversion efficiency of ~11% reduced drastically to below 9%

after light soaking at concentrated 5.4 suns illumination (see Fig. 5). Leaving the solar panels in the open circuit mode under light intensity is equivalent to an application of a forward bias voltage equal to $V_{oc}$ under dark conditions. Overall efficiency reduces during light soaking and recovers again upon cooling the panels. Cooling process "freeze" activity of defects and increases the efficiency to values over 13%. Frozen defects reduce the recombination and generation (R&G) process within the device causing high efficiency measured at low temperatures.

It is now clear that these variations in I–V curves are not observed only for PSCs, but also observed for solar cells based on well-established inorganic semiconductors such as CdTe, GaAs/AlGaAs and CIGS under severe external stresses. The I–V curves were a function of immediate history of the materials and the device structure.

## 4 Discussion

Sections 2.0 and 3.0 show the variation of I–V curves are common for both perovskite and inorganic semiconductor thin film solar cells. However, the difference is that the PSCs show dramatic instability under atmospheric conditions when compared to solar cells fabricated using well established semiconductors such as CdTe, GaAs/AlGaAs and CIGS. In inorganic solar cells, this instability is shown only when excessive external stresses such as light soaking, cooling and electrical stresses are applied to the devices. Therefore, in both cases similar phenomenon takes place but PSCs are prone to an enhanced effect.

It has paramount importance in understanding this phenomenon taking place in PSCs in order to overcome this detrimental effect. Researchers have been working on this subject and many reports [11–16] are already in the public domain. These reports consider migration of ions such

**Fig. 5** The instability of Showa-Shell CIGS solar panels under harsh external stresses (light soaking under 5.4 suns illumination and cooling), reported by Kushiya et al. in 2003 [27], during stability testing of solar panels
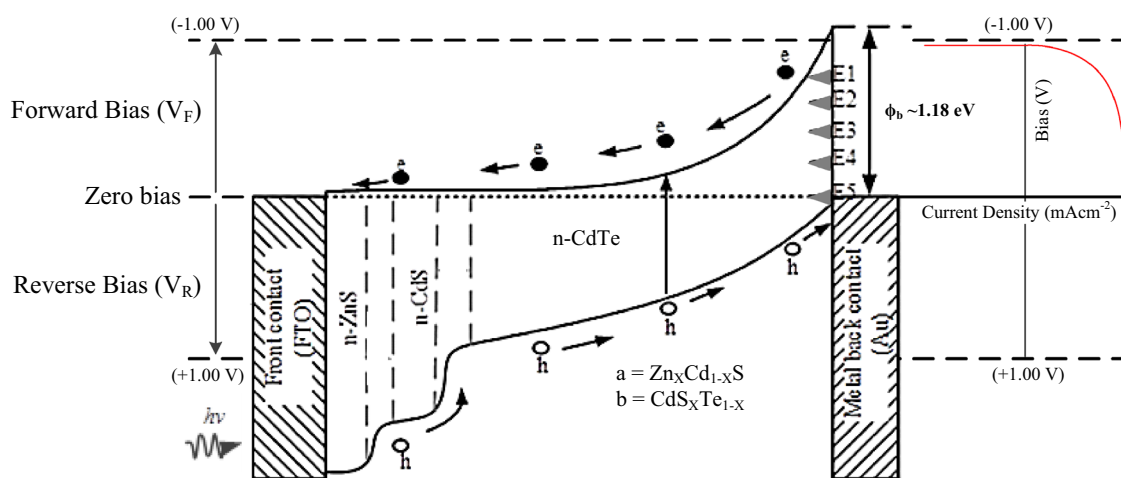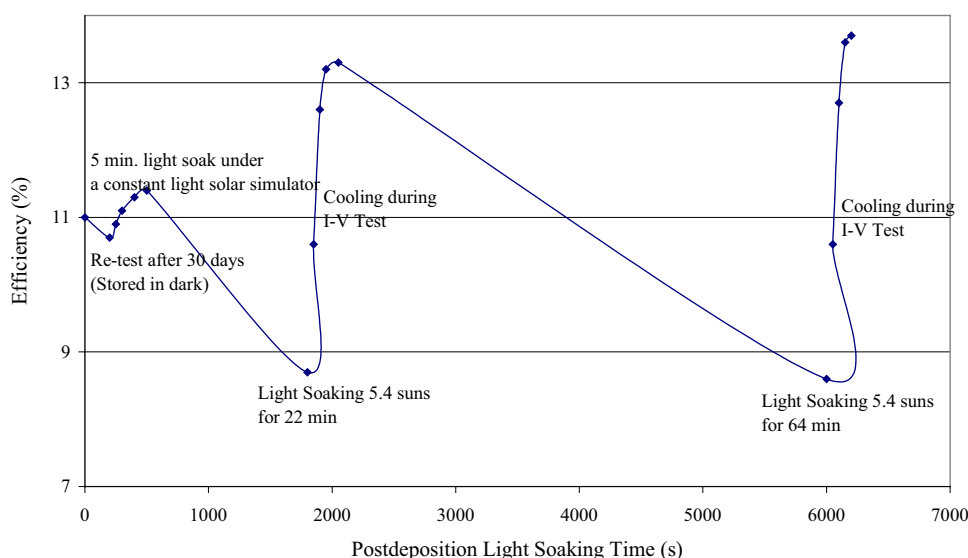


**Fig. 6** A typical example of a solar cell with experimentally confirmed ladder of defect levels [20] at the metal/semiconductor interface. Figure also shows the FL position at +1.00 V reverse bias, zero bias and −1.00 V forward bias positions. During recording of the I–V curves, the FL sweeps across the ladder of defect levels causing "filling" and "emptying" of the defects

as methylammonium ($CH_3 \cdot NH_3^+$), iodide ($I^-$) and various other photo-induced ions within the device, polarisation during I–V measurements, and hence causing the changes in shape of the I–V curves. Indeed, if the ions migrate from one side to the other, charge distribution, capacitance of the device and internal electric field within the device will change, causing the changes in I–V curves. Recent theoretical modelling also shows hysteresis in I–V curves due to ion-migration, very similar to experimentally measured results [13, 14].

However, there has been another suggestion from the perovskite community for these changes in I–V curves due to presence of electronic defects [11, 12, 15, 16]. To understand this explanation in terms of inorganic materials, a

well-known example as shown in Fig. 6 can be considered, where the n-CdTe/metal interface has a ladder of defect levels [20]. These five energy states are experimentally detected for n-CdTe/metal interfaces [20] and similar situation arise for other semiconductors such as GaAs/AlGaAs and CIGS [19]. Situation for perovskite material cannot be very different, and in fact, more defects (i.e. number of defect levels and their high concentrations) are expected due to low temperature processing of these materials and devices. These defects can be within material layers and especially located at interfaces. For this discussion, a recently proposed p-i-n type energy band diagram for perovskite solar cell, ITO/PEDOT:PSS/Perovskite/PCBM/BCP/Au is used [2], showing some possible defect levels at two main interfaces (see
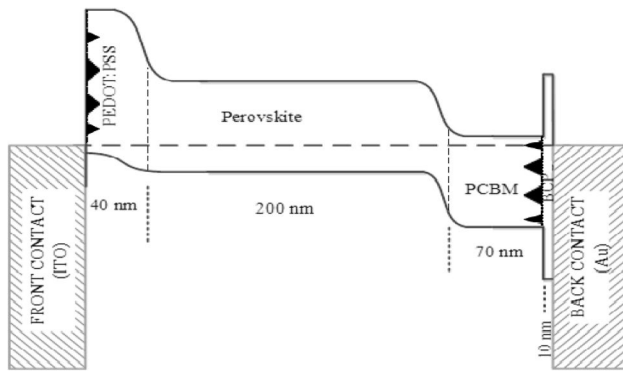
**Fig. 7** Energy band diagram proposed for ITO/PEDOT:PSS/Perovskite/PCBM/BCP/Au perovskite solar cells [2], showing possible ladders of defect levels (not yet experimentally observed) in two main contact interfaces in this device

Fig. 7). In this structure, there are five different interfaces, but possible few defect states are shown only for contact-interfaces for clarity. High concentrations of interface states are usually appear at metal (contact)/semiconductor interfaces rather than semiconductor/semiconductor interfaces due to their vast differences in crystal lattices and electronic properties. These defect levels are not yet identified but indicated only to aid the discussion. In such a situation, with slowly responding defects, I–V curves can be highly variable during measurements. When an external bias voltage is applied, the FL sweeps across all these defect levels, and measured I–V curves can be highly dependent on "filling" and "emptying" status of these defects.

While considering the more familiar inorganic semiconductor solar cell situation as shown in Fig. 6, the semiconducting material in this case is n-type and there are five experimentally observed defect levels at the n-CdTe/metal interface [20]. At zero bias, FL is pinned at $E_5$ and produces a potential barrier height, $\varphi_b \sim 1.18$ eV. If we start the I–V measurement from reverse-bias end (say from +1.00 V), all $E_1$ to $E_5$ defects are empty due to their position above the FL. Then we measure the reverse I–V curve section while the defects are empty. When I–V sweep enters the forward section and increase the bias voltage from zero to −1.00 V, defect levels $E_5$..to..$E_1$ gradually starts to fill. Filling rate of course depends on the nature of the material and the defects. Therefore the forward I–V segment is measured while the defect levels are gradually "filling" and influencing the R&G process. On the other hand, if the I–V curves are measured starting from forward bias end ($V_F = -1.00$ V), all the defects are full at the beginning. In this case, forward I–V segment is measured while the defects are "emptying" and influencing the R&G process accordingly. Clearly, the two conditions are different and hence I–V curves will show some differences as experimentally observed. This is where the "slow" or "fast" nature of traps comes into play. Fast

traps will occupy quickly but slow traps will fill slowly and therefore the "rate of scan" and the "voltage range of measurement" will also affect the I–V curves. While illuminating the device and during measuring period, R&G will take place involving these defects. The shape of the I–V curve can obviously vary according to the scan rate and the range of voltage measured. Some of these defects can be very slow with response time with several seconds.

The description above was purely based on experimental results and solid-state-physics combined with device physics principles. However, Iman Moeini et al. in May 2018 [28], theoretically modelled this situation. They considered this experimentally confirmed multi-trap level situation at the rectifying interface, and used Sah-Noyce-Schockley theory to observe the effect of these defects on resultant I–V curves. Consideration of FL pinning at different levels, and varying recombination rates have produced instability of I–V curves very similar to experimentally observed results.

The above discussion is for a known system with experimentally detected defect levels. Now, let us consider the PSC studied in our laboratories. The energy band diagram of the perovskite solar cell, ITO/PEDOT:PSS/Perovskite/PCBM/BCP/Au, can be drawn with respect to the FL as in Fig. 7 [2]. There are five main interfaces involved in this solar cell and for clarity, possible defect levels are indicated only for two key interfaces. These are drawn only for discussion, and not yet identified experimentally. It should be noted that defects are distributed within the materials and the interfaces in such a device. However, the defect concentrations are extremely high at interfaces involving very different materials. Therefore, "contact" interfaces are prone to have more defects known as "interface states". When the FL is swept across these defects during I–V measurements, all kinds of hysteresis effects can be observed. These depend on the number of defect levels present, their distributions and concentrations, together with their slow or fast nature. Although the explanation above was given for an n-type semiconductor, very similar explanation is valid when the absorbing semiconductor is p-type in electrical conduction.

In a situation with a ladder of defect levels, the FL pinning could also take place, and the pinning position can switch between defect levels when the conditions change during exposure to light or applied external voltages. If the FL switches from one level to another changing a high potential barrier present, to a low potential barrier, the device could completely lose its rectifying property. This effect usually happens in metal/n-CdTe Schottky diodes with five experimentally detected defect levels. This could also easily happen in PSCs with high concentration of defects.

It has been widely reported that the complete disappearance of device performance is due to effects of water vapour and oxygen in the atmosphere. In this case material can be physically and chemically deteriorated. Otherwise, these

exposures could create detrimental defects within the material and completely remove the rectification property from the device structure. In PSCs, both these mechanisms could lead to undesired result of losing the PV action, and hence reducing its lifetime. Future research should be directed to explore chemically stable perovskite materials for fabricating solar cells.

Above discussion shows the behaviour of I–V curves of both inorganic and PSCs are similar. The main difference is that inorganic thin film solar cells show this effect very lightly, and especially when harsh external stresses are applied to the devices. These stresses include light soaking with many-sun intensities and application of constant and large bias voltages. However, PSCs show these effects at one-sun illumination and in normal atmospheric conditions, without severe external stresses applied. The reason must be the presence of high level of defects, both the number of defect levels and their high concentrations. This is expected due to processing conditions used for fabrication of PSCs. The advantage of low-temperature ($< \sim 150\ °C$) processing leaves high concentration of defects in the device causing a disadvantage of instability and short lifetime. On the other hand, inorganic thin film solar cells are fabricated at comparatively high temperatures ($> \sim 450\ °C$ and $< \sim 650\ °C$). It is well known that defects in thin films anneal-out at suitable high temperatures and inorganic solar cells have comparatively low concentration of defect levels, and hence more stable I–V characteristics. By optimising the material processing temperature, adding other chemicals (additives or dopants), changing solvents could minimise defects in perovskite materials improving both the performance and the stability of PSCs. Even then the method of device processing steps could leave high density of defect states at key interfaces. Selecting better contacting materials could immensely reduce the defects at semiconductor/electrical contact interface and boost the device performance.

It is therefore highly relevant to study the defect properties in perovskite materials using relevant techniques such as photoluminescence (PL), Admittance spectroscopy and photo-acoustic spectroscopy (PAS) methods. Deep Level Transient Spectroscopy (DLTS) method may not be suitable to use for early stage perovskite materials due to long time period needed for these measurements. Better understanding of defect structure within the bandgap will enable scientists to reduce these defects and hence achieve better performing devices. Admittance spectroscopy usually detects only low energy-defect levels, but PAS is capable of detecting all defects in the bandgap [20]. PL should be done to detect defects throughout the bandgap rather than a limited range around the band-to-band electron transition [29]. An improved knowledge on electronic defects will lead the research community in the right direction to further develop PSCs removing un-desired hysteresis effects.

Another reason for enhanced hysteresis effects in PSCs could be the experimentally reported high charge carrier mobilities. Literature shows comparatively high mobilities for charge carriers in perovskite materials [30], when compared to those values for poly-crystalline CdTe [31] and CIGS [32] thin films. All three thin film layers considered in this discussion; perovskite, CdTe and CIGS are poly-crystalline and usually show columnar growth. All these three thin films used in devices have thicknesses in the range $\sim 0.2\ \mu m$ to a few microns. Typical grains extend from front surface to the back surface. In general, experimental measurements, usually evaluate the mobility values parallel to the transparent conducting oxide (TCO) surface ($\mu_{||}$). In this direction of motion, charge carriers undergo scattering from a large number of grain boundaries. But during the PV action, both electrons and holes travel normal to the TCO surface. This movement of charge carriers do not experience any scattering due to grain boundaries since charge carriers travel within mainly only in one grain. Therefore, the mobility of charge carriers normal to the TCO surface ($\mu_{\perp}$) could be several orders of magnitude higher than the reported values ($\mu_{||}$). Because of this high mobility of charge carriers in perovskite, the I–V curves can be very sensitive and this must be another reason for enhanced hysteresis in PSCs. For the benefits of both inorganic and perovskite solar cell development, researchers should focus on developing methods for measuring $\mu_{\perp}$ rather than $\mu_{||}$ in the future. This will enable more accurate theoretical simulation of device characteristics using $\mu_{\perp}$ instead of usually reported $\mu_{||}$ for thin film solar cells.

Understanding the device architecture and its PV action are also crucial in developing the PSCs removing un-desired hysteresis effects. Observation of the literature shows the use of energy band diagrams using Anderson's electron affinity rule. This is a good method to explain "ideal" systems with respect to the reference level of the "Vacuum Level". However, in "real" situations such as in thin film semiconductors, electronic defect levels dominate their electrical properties, and FL pinning can take place. In this case, it is highly relevant to use the reference level of "Fermi Level" to draw energy band diagrams. This is clearly applicable for CdTe [33] and CIGS [34] thin film solar cells, and highly appropriate for PSCs. Figure 7 shows the energy band diagram of ITO/PEDOT:PSS/Perovskite/PCBM/BCP/Au [2] drawn by taking the FL as the reference energy level. With this energy band diagram, there are many improvements could be introduced to enhance the performance and stability of PSCs. This device structure is a graded bandgap solar cell fabricated on a p-type window material [35]. Improving electronic and optical qualities of materials, reduction of defects, improving the bandgap grading, use of electron back diffusion barrier (ebdb) and hole back diffusion barrier (hbdb) layers and selecting better contact materials for the

structure can enhance both the efficiency, stability and the lifetime of PSCs.

Recent experimental results reported by Xiangyue Meng et al. in [36] have developed a planar p-i-n type device similar to a device shown in Fig. 7 [2] and produced ~20% efficiency with 83% fill factor. This structure has significantly reduced trap densities and the interface barrier layer just before the metal (Ag) contact avoiding formation of insulating AgI at the interface. This structure has completely reduced the hysteresis effect of the device. Although the energy band architecture was not explained, this device is a graded bandgap solar cell fabricated on a p-type window layer with a few material layers. This device has the energy band diagram very similar to the one shown in Fig. 7, and has a great potential to develop further. This energy band diagram will direct the way forward for next generation multi-layer graded bandgap solar cells based on perovskite materials [35].

Finally, it is relevant to refer to the work reported by Zhao et al. [37] and Futscher et al. [38] on quantification of ion migration in $MAPbI_3$ PSCs. Zhao et al. clearly demonstrated the migration of ions in the time scale of 0–10 s range, when 2 $V\mu m^{-1}$] electric field is applied across this material. The internal electric fields within PSCs during I–V measurements are comparable to 2 $V\mu m^{-1}$ values and therefore ions migration taking place in $MAPbI_3$ is experimentally proven.

However, Futscher et al. used the same perovskite ($MAPbI_3$) material and produced solar cells with different electrical contacts; (a) $TiO_2$/$MAPbI_3$/spiro-OMeTAD and (b) $NiO_x$/$MAPbI_3$/$C_{60}$. Device (a) exhibited severe hysteresis while device (b) has shown minimal hysteresis effects. In these two cases ions migration is common, since $MAPbI_3$ is used as the main absorber material but some other mechanism must be dominating to control hysteresis effect only in the device (a). This has to be the interface defect states at perovskite/electrical contact interfaces. Filling and emptying of traps are usually fast, taking place in time scales smaller than milli seconds. Therefore, out of the two possible mechanisms, electronic trap effects taking place at high speed is dominating rather than the ions migration taking place at slow speeds in the few seconds time scale. Deep analysis of capacitance of perovskite devices as a function of electrical contacts, frequency and temperature should confirm the final answer to this debate.

## 5 Conclusions

The experimental evidence presented in this review paper leads to conclude that the variation in I–V curves are common to all thin film solar cells based on inorganic (CdTe, GaAs/AlGaAs and CIGS) semiconductors and perovskite materials. However, PSCs suffer hysteresis effects more severely than inorganic solar cells. Devices fabricated with inorganic semiconductors show these effects when harsh conditions such as intense light soaking and external electrical stresses are introduced. But PSCs show dramatic changes under normal conditions, most probably due to extremely high charge carrier mobilities and the existence of excessive defect concentrations in these materials and interfaces within device structures. One reason must be the low-temperature processing of perovskite materials and devices. Inorganic semiconductors are usually processed at higher temperatures and therefore consist of comparatively low defect concentrations. The inorganic poly-crystalline films also have comparatively low charge carrier mobilities and therefore, the I-V hysteresis effects are low. As discussed in this paper, characterisation of defects identification and their removal from the device structure could enhance the initial efficiency, stability and lifetime of PSCs. This has been experimentally shown by Dae-Yong Son et al. [39] recently. Processing of devices at optimum temperatures, adding chemicals (additives and dopants) and use of better solvents could help in reduction of defects. This trend has also been recently shown by Shuang Yu et al. [40]. Understanding the device architecture and taking right steps to develop PSCs has a long way to go for improving efficiency further and fabricate stable devices with long lifetime. Out of the proposed suggestions, the effect of electronic defects on I–V curves seems more relevant to describe the short lifetime and hysteresis behaviour. Comprehensive studies of capacitance of PSCs could remove the idea of ion-migration from the debate and confirm the dominant effects of defects. This should be an interesting confirmation on instabilities of I–V curves and pave the ways to further develop PSCs.

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