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Ultra-thin chips for high-performance flexible electronics

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Flexible electronics has significantly advanced over the last few years, as devices and circuits from nanoscale structures to printed thin films have started to appear. Simultaneously, the demand for high-performance electronics has also increased because flexible and compact integrated circuits are needed to obtain fully flexible electronic systems. It is challenging to obtain flexible and compact integrated circuits as the silicon based CMOS electronics, which is currently the industry standard for high-performance, is planar and the brittle nature of silicon makes bendability difficult. For this reason, the ultra-thin chips from silicon is gaining interest. This review provides an in-depth analysis of various approaches for obtaining ultra-thin chips from rigid silicon wafer. The comprehensive study presented here includes analysis of ultra-thin chips properties such as the electrical, thermal, optical and mechanical properties, stress modelling, and packaging techniques. The underpinning advances in areas such as sensing, computing, data storage, and energy have been discussed along with several emerging applications (e.g., wearable systems, m-Health, smart cities and Internet of Things etc.) they will enable. This paper is targeted to the readers working in the field of integrated circuits on thin and bendable silicon; but it can be of broad interest to everyone working in the field of flexible electronics.

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INTRODUCTION

Flexible electronics is changing the way we make and use electronics. Many existing applications such as implantable systems that require bendability to conform to the curved surface of tisues[1] are driving the progress in the field, which in turn is the enabler for numerous futuristic applications such as mHealth, wearable systems, smart cities, and Internet-of-Things (IoT). Several initiatives from governments and industry have also contributed to the progress and it is now estimated that the market for flexible electronics will reach $300 billion by 2028,[2,3] with growth from $29.28 billion in 2017 to over $63 billion in 2023[4] for printed, flexible and organic electronics alone. The high-performance, at par with today's complementary metal oxide semiconductor (CMOS) electronics, will be critical to this growth in flexible electronics as several current and future electronics would need fast communication and computation. For example, large drive currents and fast readout is needed in application such as interactive flexible displays. Likewise, wireless communication in mHealth or IoT (where wearable sensors patches are needed for continuous measurements) will require data handling in frequency bands up to ultra-high frequencies (0.3 – 3 GHz).[5] The faster communication, higher bandwidth, and efficient distributed computation with very high clock speed will make the high-performance requirement inevitable in connected objects. This high-performance requirement calls for investigations into new materials, fabrication technology, methodologies, and design techniques[6]—all of which influence the device performance. For example, the transistor switching frequency is influenced by the mobility and channel length—while mobility is a material property, the channel length depends on the technology. To demonstrate how various materials link to performance, we have compared in Table 1 some of the materials used in flexible electronics. This comparison is in terms of carrier mobility (μ), channel length (L), transit frequency (f_t), and the I_{on}/I_{off} ratio of transistors that use these semiconducting materials as current channel. Assuming fixed FET parameters such as channel width, oxide capacitance etc. and the voltages such as terminal and threshold voltage, the dependency of transit frequency (which is a measure of transistor speed) boils down to mobility and channel length and can be written as:

$$f_T = k\frac{\mu}{L^2} \tag{1}$$

where k is the proportionality constant arising from above stated assumption. Normalizing Eq. (1) with respect to the proportionality constant, the normalized transit frequency can be written as:

$$f_{T_{\text{norm}}} = \frac{f_T}{k} = \frac{\mu}{L^2} \tag{2}$$

Thus, the $f_{T\text{norm}}$ is directly proportional to the mobility and inversely to square of channel length when the devices have similar parameters other than the mobility and the channel length. Putting the μ and L values from some of the recent works in Eq. (2), the comparison in Table 1 shows that the monocrystalline silicon based devices with channel length in nanoscale regime will have high $f_{T\text{norm}}$ and as a result they will outperform most of the other semiconductor materials. Interestingly, the devices from high mobility materials such as graphene, carbon nanotubes,[7] and some the 2D materials are slower than silicon. Clearly, the channel length or device technology plays a significant role in the final performance of devices. Therefore, instead of fixating on high-mobility materials, a holistic view with inputs from both material science and engineering is important. With technological advances, the devices from high mobility materials such as graphene, and carbon nanotube etc. could eventually catch up

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Table 1. Comparison between mobility, channel length and normalized transit frequency of transistors fabricated using different materials

Material	Mobility (μ) [cm^2/V-s]	Channel length (L) [nm]	Normalized transit frequency (f_{Tnorm}) [GHz]	I_{on}/I_{off}	Ref.
Monocrystalline Si	300–1200	14	4250	10^9	169,170
Amorphous Si	5–32	12,500	0.00115	10^5	171,172
III–V Semiconductors	400–12,000	75	165	10^4	173–176
MoS_2	700	300	42	10^8	177–180
WS_2	234	6000	3.8	10^8	181,182
Pentacene	1.5	2000	0.0114	10^2	183–185
CVD Graphene	24,000	40	100	10^2	186–188

and possibly may have better performance than monocrystalline silicon, but this is unlikely in next few year as related technology is still in the nascent stage of development and is far from commercialization.[8,9] Considering these facts, the monocrystalline silicon appears to be the best bet to meet immediate high-performance needs of flexible electronic systems. This also explains why silicon and other materials such as compound semiconductors have attracted significant interest in recent years. Nanostructures such as nanomembranes, nanoribbons, nanowires etc. from these materials have been explored for flexible electronics.[10–12] Considering the challenges such as printing of aligned nanostructures, poor density of printed nanostructures, and difficulties in terms of obtaining very large-scale functional integrated circuits (ICs), the silicon-based microelectronics is an obvious choice.

The technology readiness to obtain devices down to nanoscale dimensions and the possibility to exponentially scale the device densities up to billions of devices per mm^2, makes silicon based microelectronics a good candidate for addressing immediate high-performance needs in flexible electronics. For this the first issue that need to be overcome is the lack of flexibility (and hence conformability) of silicon wafers. This has been achieved by thinning the wafers down to <50 µm using a range of technologies, which are discussed here. Silicon chips from such thinned wafers, or ultra-thin chips (UTCs), are ideal for high-performance flexible electronics as they are physically bendable and have stable electronic response for particular bending state.[13] The excellent form factor of UTCs make their integration on flexible substrates better than the conventional thick chips. Further, due to reduced package volume and lower parasitic capacitance, the UTCs have better high-frequency performances and lower power consumption. With these features UTCs can underpin advances in areas such as sensing, computing, data storage, and energy (Fig. 1) and several emerging applications (e.g., robotics, wearable systems, m-Health, smart cities and Internet of Things etc.) they will enable.[14,15]

Given the wide scope of UTCs, a comprehensive review of various technological and applied aspects will complement several other reviews that have mainly focussed on organic semiconductors and their processing techniques such as printing or vacuum deposition etc.[16–18] A few review articles have also discussed layer transfer processes and thin film silicon for solar cells.[19,20] Related to UTCs, only a few review articles have been published and they have covered limited areas such as wafer thinning methods such as back grinding and integration on flexible substrate using stretchable interconnects.[21–24] The analysis of UTCs covering topics such as changes in electrical-mechanical-optical-thermal properties, packaging, and stress-induced response variations, and comparison of various thinning methods has not been reported thus far. The in-depth analysis presented in this paper fills the above gaps in the literature and provide a complete overview of the research related to UTCs.

This paper is organized into seven sections. The section "Historical perspective" briefly provides the historical perspective and introduces various developments including those related to ultra-thin silicon (UTSi) over last 30 years or so. The section "Ultra-thin chip properties" describes the major UTC properties with brief discussion related to approaches, which have been used to study the effect of thinning and bending on device performance. Various technologies reported to obtain UTCs and their comparative study is given in the section "Technologies for realizing UTC". The integration and packaging of UTCs on flexible substrate is described in the section "Integration of UTCs on flexible substrates". Major application areas of UTCs and the potential new application enabled by them are presented in the section "Applications of UTCs". Finally, a summary of key outcomes from this review and outlook are given in the section "Conclusion".

HISTORICAL PERSPECTIVE

The UTSi based devices has gained gradual increasing attention, as can be noted from Fig. 2. Based on the data from Web-Of-Science, the plot shows the trend in the growth of ultra-thin semiconductor and related technologies. The trends are plotted for articles having the phrase "thin silicon" or "thin chip" in their titles. In the early days (in 1960s), the thin silicon was explored as an active material to realize large flexible arrays of solar cells for space applications.[25] In late 90s, the interest in the field of thin wafer or wafer thinning increased due to demands for 3D ICs. Since then, thin Si was mainly pursued through Silicon-on-Insulator (SOI) wafers. This involved bonding a Si wafer over another oxidized Si wafer followed by grinding/thinning of one of the wafers, through what we now know as bond and-etch-back SOI (BESOI) process.[26] A significant number of articles related to SOI technology, but not having "thin-silicon" as a part of their title, may have been excluded in our analysis. The SOI wafers have also been used to realize UTCs with very precise thickness.[27] However, the high cost of SOI wafers (which is approximately an order of magnitude higher than bulk wafers) is driving the researchers to explore alternative techniques for low cost fabrication of UTCs. Overall the field of flexible electronics has witnessed exponential growth in number of publications and in comparison with this overall growth, the thin-chip related research is still in the nascent stage.[28] Nonetheless, it is growing steadily as demand for high-performance flexible electronics has gained momentum only recently. This trend is on expected lines as the flexible electronics research, which in the initial days focussed on tackling materials and fabrication related issues, is now advancing towards system. The requirements related to high-performance are mainly felt at the system level. Importantly, the trend in Fig. 2 indicates that the interest in UTCs will continue to grow as the field flexible

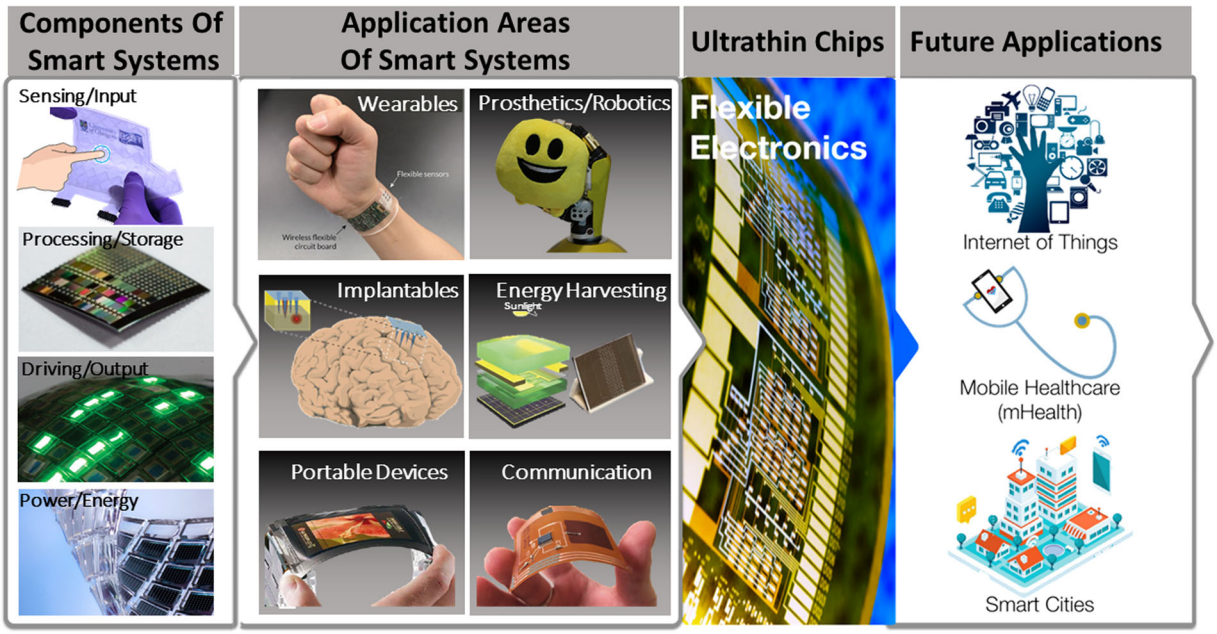

Fig. 1 Applications enabled by UTCs through underpinning research in areas such as sensing, computing, data storage, and energy.[157–162] Figure reproduced with permission from: ref. [158], 2008 © NPG; ref. [157], 2009 © NPG; ref. [159], 2015 © NPG; ref. [160], 2011 © Wiley; ref. [161], 2008 © Wiley; ref. [162], 2016 © NPG

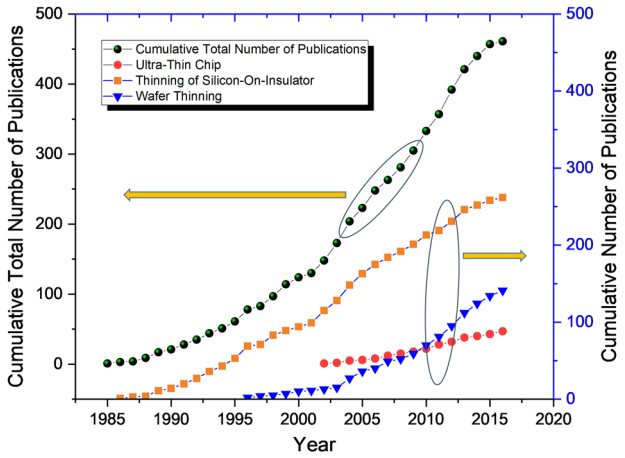

Fig. 2 Cumulative number of publications in major areas related to thin-Si based electronics, including UTCs [*Source*: Web of Science]

electronics advances towards higher technology readiness levels and embraces more applications.

UTC PROPERTIES

The physical dimensions could influence the material properties and carrier transport mechanism and therefore could affect the performance of electronics devices. Compared to their bulk counterparts, the UTCs exhibit different behavior in terms of mechanical flexibility, optical transmittance, and carrier surface mobility (e.g., upon experiencing stress) etc. These variations can be challenging to handle, for example when one attempts to apply on UTCs the methods and designs developed for conventional bulk silicon. At the same time, such variations also offer multiple new opportunities, which are otherwise difficult with bulk silicon. For example, Si starts to become optically transparent for thicknesses below 10 µm—starting in the red region and progressing towards blue region as the wafer gets thinner. Such thinning led variations in optical transparency of Si could be exploited to improve photodetectors and solar cells etc., as explained later in this section. An extensive analysis of variations in properties with respect to thickness has not been reported and this section should fill the gap in literature.

Mechanical properties

The thinning process impacts the mechanical properties of thinned electronic substrate. For example, during thinning by back grinding, the sub-surface damage (SSD) and deep cracks in Si result in poor bendability and eventually lead to early breakage of UTCs. Likewise, the etch pits and hillocks produced during thinning by wet etching could lead to localized stress and can decrease the breaking strength of Si. The localised stress or stress distribution at different locations in UTCs are typically studied with Finite Element Analysis[29] and Micro-Raman Spectroscopy.[30] The FEM analysis can provide an estimate of the residual stress at critical position like hinge and centre and the shift in Raman peak could provide deep insight into localised mechanical stresses.

The physical parameters which are measure of strength of bulk Si such as Young's modulus (E) also change with thinning. The Young's modulus, which normally has a constant value, becomes thickness dependent especially when the thickness hits the nanometer regime. After a certain thickness, h_b, the dependence of Young's modulus on the thickness can be described as:[31]

$$E = 54.872 * h_b^{0.226} \quad (3)$$

For Si, the h_b is about 80 nm and this value depends on parameters such as in-plain strain, Poisson's ratio and the Young's modulus of bulk Si. The nanometre range is hard to achieve with mechanical grinding or wet etching of bulk Si wafer, nonetheless with SOI wafers it is possible to obtain UTCs with nanometre thickness.

The mechanical strength of UTCs is also influenced by their thickness and the stress generated during the bending.

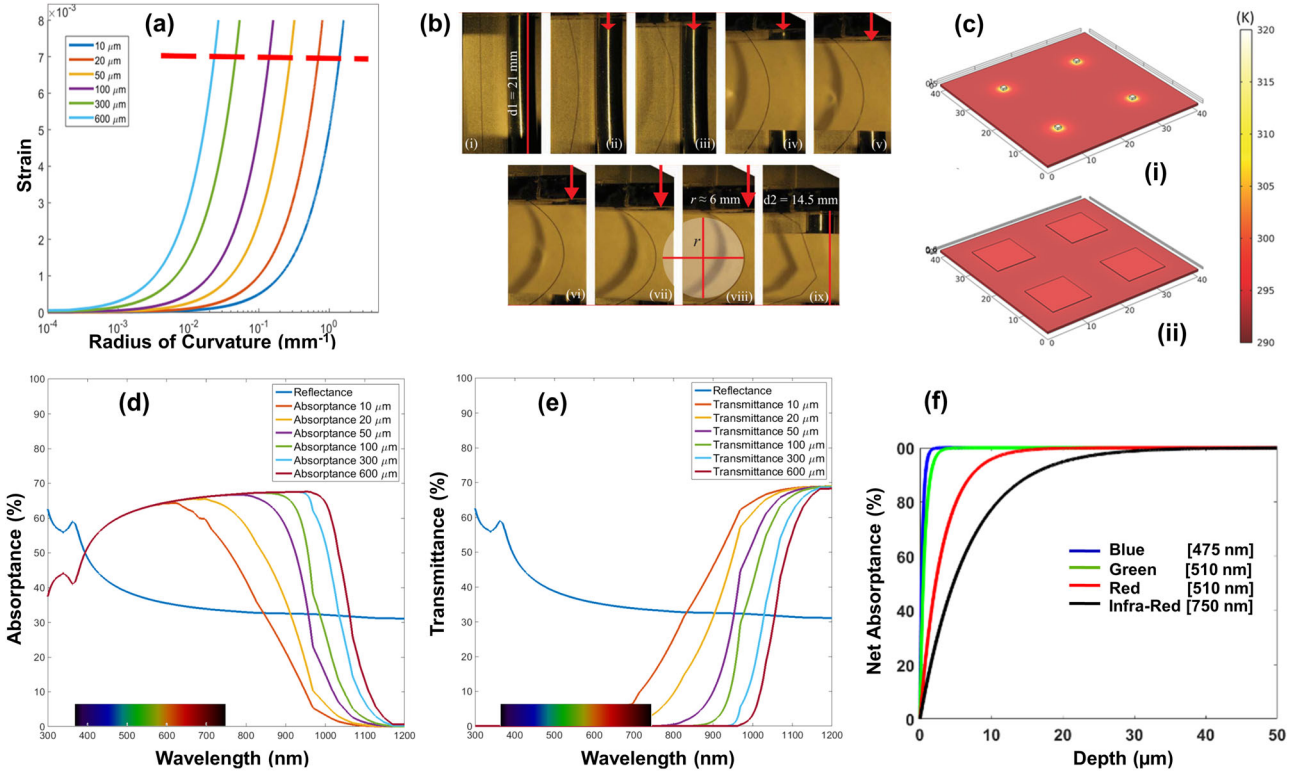

Fig. 3 **a** Plot showing the calculated bending strain vs. radius of curvature for various thicknesses of Si wafer. **b** Bending of Si membranes on PDMS substrate showing breakage at $R = 6$ mm.[33] **c** COMSOL simulation of heat distribution in (i) 500 µm thick chip with area 1 mm^2 showing creation of hot spots—up to 45 °C for a low input power density of 1 W/cm^2.[21] (ii) 100 µm thick with area 100 mm^2, showing temperature rise of only 2 °C above ambient at same power density. **d** Absorptance percentage of light plotted against wavelength for different thickness of silicon. **e** Transmittance and reflectance percentage of light plotted against wavelength for different thickness of silicon. **f** Plot of net-absorptance vs. depth for different wavelength of light. Figure reproduced with permission from: **c** ref. [21], 2015 © Wiley

Mathematically this is expressed as:

$$\sigma_{st} = \frac{E * h}{2R} \quad (4)$$

where h is thickness of UTC and R is the bending radius of curvature. Under bending conditions, the stress is directly proportional to the thickness of UTCs and inversely proportional to the radius of curvature. The ultimate breaking strength of Si is 7 GPa.[32] This means for the same stress; the thinner chip will have lower radius of curvatures or can be bent more. This is also indicated by Fig. 3a, where estimated values of bending strain (calculated using MATLAB code based on equations in ref. [33]) are plotted against radius of curvature for Si with different thicknesses. The dashed line at 0.007 parallel to x-axis indicates typical breaking strain for UTCs. However, in most of the cases, thin chips are packaged over flexible substrate or flexible printed circuit board (FPCB). In a packaged structure with UTC placed over a flexible substrate, Stoney's formula could be used to determine the stress level. In the most common form, it is written as:

$$\sigma_f = \frac{E_s t_s^2}{6(1-\nu) t_f R} \quad (5)$$

where t_s, t_f are substrate and film thickness, and v is Poisson's ratio. The stress experienced by the top surface of UTCs is proportional to Young's modulus of substrate and its thickness. For this reason, for applications requiring polymer substrate, the polydimethylsiloxane (PDMS) ($E = 360$–870 KPa) could be a better than polyimide (PI) ($E = 2.5$ GPa). This is also reflected in Fig. 3b, which shows UTCs over PDMS substrate can bend up to 6 mm without breaking. Often the neutral plane concept is proposed to reduce the stress experienced by the electronics on UTCs. This can be achieved by laminating or encapsulating the UTCs between two layers of suitable thicknesses. In doing so one could improve the bending limits, but in practical terms it is difficult to fabricate or integrate UTCs in the neutral plane. Instead of minimizing or cancelling such effects, it could be useful if an alternative strategy is devised to exploit bending induced variations in the response of UTCs. As an example, variations in the output of devices on UTCs could be exploited to predict the state of bending (e.g., curvature) or the shape of UTC under bending condition. This could be achieved by developing models that accurately capture the electro-mechanical variations in the response of devices on UTCs. The need to model the behavior of electronics on flexible substrates has been felt recently as reports in this field have started to appear.[34–36]

Thermal properties

Temperature is known to have significant impact on the performance and reliable operation of electronics and therefore discussion on thermal properties of UTCs gain importance. The heat dissipation, particularly in the UTCs realized from SOI wafers having top Si thickness in the nanoscale, significantly differ from conventional bulk Si based chips. For example, the thermal conductivity of <100 nm Si is half the value of undoped bulk Si (~148 $Wm^{-1} K^{-1}$).[37] The lower thermal conductivity means the heat generated is not easily transferred to the package and therefore appropriate heat management may also be needed for UTCs, especially for high-performance flexible electronics. Another important factor is the dependence of mobility on temperature, which is determined by four types of scattering (phonon scattering, surface roughness scattering, bulk charge coulombic scattering, and interface charge coulombic scattering). The net effect of this complex dependence is that higher the temperature, lower is the mobility[38] and therefore increase in the temperature

Table 2. Change in device and circuit parameters realized on UTC under bending condition

Device/circuit	Chip thickness [μm]	Bending radius [mm]	Evaluated parameter	% Change	Ref.
NMOS, PMOS	15	20	Drain current	~6	34
Inverter	40	15	Avg. propagation delay Midpoint voltage	~7 ~ 2	189
NMOS current mirror	20	30	Output current	~5	51
Memory	40	5	Remnant polarization	–	138
Ring oscillator	20	25	Output frequency	~1.15	190
Comparator	20	25	Standby current	–	190
Ring oscillator [SOI]	0.006	6.3	Stage delay	–	59

due to low thermal conductivity of UTCs could degrade the system performance. Likewise, the threshold voltage decreases because the metal to semiconductor work function and fermi potential decrease with temperature.[39] The thermal issues can be overcome by incorporating on-chip cooling architecture such as micro-coolers and thermo-electric fluidic cooler.[40] However, this is cumbersome process and will typically require a liquid cooling mechanism.[41] A potential alternative is to use large size UTCs. As an example, with COMSOL simulation (Fig. 3c)[21] it has been shown that a 1 mm × 1 mm conventional chip (0.5 mm thick) on a 0.5 mm thick polyimide can heat up the substrate to 40 °C even with a small power density of 1 Wcm^{-2}. However, in larger chips, the heat is distributed over larger area and therefore local heating is reduced. Applying the same argument to thin chips (~100 μm thick) on polyimide substrates, with same power but bigger area (10 mm × 10 mm), the simulation result show only 2 °C more temperature than ambient. This much increase in the local temperature is within acceptable limit for applications such as biomedical implants and wearables where higher temperatures can damage tissues. Embedding of air-channels in thin chips could alleviate the issue as it helps in the cooling of the chip. However, such solutions put a restriction on the type of methodology used to develop UTCs.

Optical properties

Owing to varying absorption coefficients at different wavelengths, Si starts to become optically transparent as the thickness decreases—starting with the red region and progressing towards blue region. For relatively thicker Si (>10 μm), this behaviour could be approximately explained with Fresnel equation of reflectance (Eq. 6) and Beer-Lambert's law (Eq. 7) as:[42]

$$R(\%) = 100\left|\frac{n_{\mathrm{Air}} - n_{\mathrm{Si}}(\lambda)}{n_{\mathrm{Air}} + n_{\mathrm{Si}}(\lambda)}\right|^2 \quad (6)$$

$$A(\%) = 100\left(1 - \mathrm{e}^{-\alpha_{\mathrm{Si}}(\lambda)x}\right) \quad (7)$$

where, n_{Air} and n_{Si} are the refractive indices of air (~1.00) and Si respectively, λ is the optical wavelength, α_{Si} is the absorption coefficient of Si at a given wavelength and x is the optical path length. Figure 3d shows the optical reflectance and absorptance vs. wavelength for ultrathin Si of various thicknesses. The reflectance spectrum indicates that Si is more reflective in the blue end. Figure 3e shows the net spectral transmittance for ultrathin Si at various thicknesses. A noticeable difference is observed for sub-10 μm Si where it starts to become transparent in the red region. Figure 3f shows the optical net absorptance for various depths of Si, particularly for the typical wavelengths (blue—475 nm, green—510 nm, red—650 nm, and infrared—750 nm). It can be noticed that 90% intensity of these wavelengths gets absorbed within ~750 nm, 1.5 μm, ~7 μm, and 15.5 μm depths. Semi-transparency can be obtained by introducing holes in the wafer using XeF_2 based isotropic dry etching and Al_2O_3 as protective layer.[43] For application such as photodetectors or solar cells, where higher absorptance is required along with flexibility, the optical path length in thin Si can be improved by using special optical trapping techniques such as Lambertian trapping,[44,45] texturing,[46] antireflection coatings.[47] Solar cells made from thin Si with optimal surface passivation show higher open circuit voltage as in this case the photo-generated carriers can be collected effectively before they recombine. This property of varying optical transmittance with thickness could also be exploited to monitor and control Si etching process as the thickness could be seen as a function of transmitted light. Back thinning also contributes to achieving higher quantum efficiency in both charge-coupled device (CCD) as well as active pixel sensor (APS) image sensors.[48] However, their red and infrared response is decreased due to thinning. Nonetheless this could be addressed with special optical trapping techniques as described above. In addition to the change in transmittance due to change in thickness, stress on thin Si results in bandgap narrowing (BGN). This BGN and the change in effective mass, which are related to intrinsic charge carrier concentration, can lead to an increase in the dark current of photodetectors.[49] The changes in optical transparency with thickness means the UTCs could also find use in applications other than those requiring flexible electronics.

Electrical behaviour

The fundamental electrical properties of Si such as its bandgap, dielectric constant, density of states, will not change until the thickness reaches nanoscale.[50] For most of the flexible electronics applications, the flexibility requirements could be fulfilled with UTCs having thickness in the range of 5–50 μm. Therefore, for practical purposes the fundamental electrical properties of ultra thin Si remains unchanged when they are realized by thinning bulk Si. To reach <50 μm, the thickness of a conventional bulk wafer or SOI wafer undergoes thinning process, which is known to induce stress in Si. The Si chip could also be stressed by various fabrication steps such as deposition of different material layers like oxide, dielectrics, and metal etc., which have different elastic modulus. On top of these, there is additional stress when the UTCs are externally loaded or strained, for example, during bending. Whereas the thinning and process induced stress are intrinsic to chip, the bending induced stress during usage is external. These stresses induce changes in the band structure and the piezo-resistive property of Si, which eventually show up as variation in the electrical response of devices on UTCs. Through electro-mechanical tests and modelling, a few works have attempted to capture the stress induced changes in electrical response of devices. For example, in the case of uniaxial bending, n-type

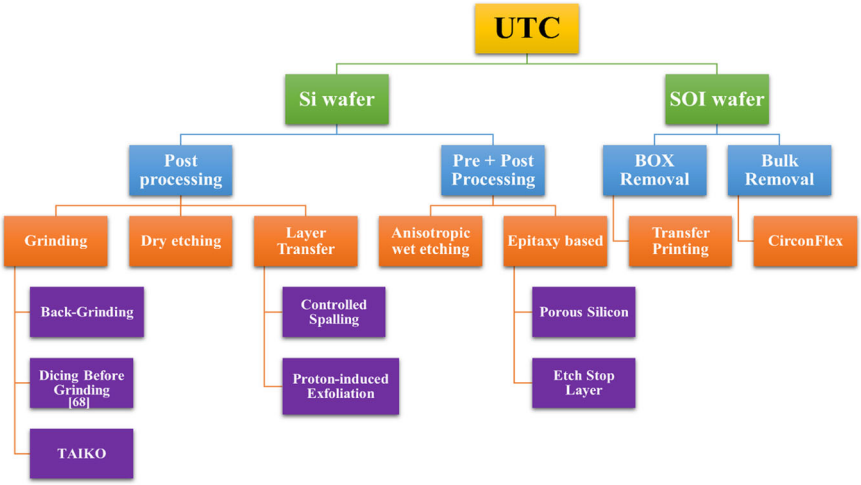

Fig. 4 Classification of various thinning methodologies for realizing UTC

MOSFETs show increase in mobility with increase in bending stress. In n-type MOSFETs, this behaviour is independent of the direction of bending, but variations in the response of p-type MOSFETs is direction dependent.[51] The models in these works have taken into account the process strategies, dimensions of the structure (active Si, dielectric, metal thicknesses, etc.), initial substrate (e.g., Si, SOI, UTSOI, ETSOI etc.), mechanical strain etc. The stressed induced changes could lead to significant deviations in the response of device and circuits from their specified values, as can be oberved from Table 2, where bending induced changes in device and circuit parameters are reported. For complex circuit design in flexible electronics and to predict their response under different bending condition precisely, it is necessary to understand these variations and implement predictive models in electronics design tools.[34,35] The variations in device response could be reduced by using suitable compensation techniques in the layout. On other hand, these changes in the device parameters could also be seen as the signature for a particular bending state and therefore could be used to predict or sense the state/shape of bending.

TECHNOLOGIES FOR REALIZING UTC

A wide range of technologies have been explored for realizing UTCs and a detailed discussion about some of are given in a few review articles.[21,22] For the sake of completeness, the technologies involving either bulk Si wafer or SOI wafer are briefly discussed in this section. Figure 4 also gives a summary of these technologies, classified based on the fabrication stage at which the thinning is carried out. For example, when the thinning is carried out after the fabrication of electronic devices it is termed as post-processing, and when wafer undergoes some processing before the device fabrication then it is termed as pre-processing. Generally, the thinning is carried out after the device fabrication is completed. Following the discussion in previous section, the choice of technological approach to realize UTC requires careful consideration.

Using Si Wafer

UTC via post-processing techniques. In post-processing approaches, the UTCs are typically obtained by physical removal of electronic substrate such as Si through either grinding, dry etching, chemical reaction or combination of these. In these techniques, the crystal structure of active Si area (for example, in the case of MOSFETs, the area up to well-depth) is unaffected and therefore their electrical response is at par with their bulk counterparts. However, as discussed in previous section the possibility of mechanical degradation cannot be ruled out. The techniques used as post-processing step can be broadly divided into: (i) grinding, (ii) dry etching, and (iii) layer transfer.

Grinding: Back grinding is a popular and well established method for wafer thinning. It is carried out in two steps as shown in Fig. 5a—coarse grinding followed by fine grinding to obtain a smooth surface. The protective tape, which holds the wafer to chuck during grinding, plays a significant role in determining the total thickness variation (TTV) as the wafer gets thinner. Wafers with thickness as low as 3 µm have been obtained with this technique.[52] Back grinding is faster with respect to other techniques, but it is also known to damage the crystal structure deep inside the material. The sub surface damage could induce high stress in the thinned wafer and can cause thin wafer or UTCs to warp. This type of stress concentration can also lead to breakage during handling, for example, while removing the thin wafer from chuck or during dicing of thin wafer. Therefore, stress-relieving techniques such as slow ion etching and chemical-mechanical polishing are recommended after back grinding. Dicing before grinding (DBG) is also sometime used to prevent breakage of thinned wafers during dicing. In DBG, the wafers are first partially-grooved and then grinded, as illustrated in Fig. 5c, with die singulation occurring when the wafer is thinned below the level of this cut.[53] A major problem with grinding is that there is high potential for the thin wafer getting damaged while it is being delaminated from the protection tape. This issues could be overcome by TAIKO technique (Fig. 5b) in which back-grinding is done only for non-peripheral part of the rear side of wafer and the periphery is left intact as a ring.[54] The ring-shaped periphery strengthens the overall structure and significantly reduces the issue of warpage during handling.

Dry etching: Physical dislodging of Si atoms from the bulk could also be achieved with high-energy ions and gaseous reactive species. Depending on the mechanism, the process can be classified as: (i) physical ion etching (PIE), and (ii) reactive ion etching (RIE). In PIE, the atoms from the back of the substrate are removed by bombarding it with energetic ions or gas assisted etching.[55] The etch rate depends on parameters such as scanning style, substrate chuck table angle, beam angle etc. There is always some re-deposition in this process, which reduces the effective etch rate and selectivity. In the case of RIE, the high-energy ions impacting the substrate remove the atoms physically and open-up the area for chemical reaction as illustrated in Fig. 5d. RIE gives

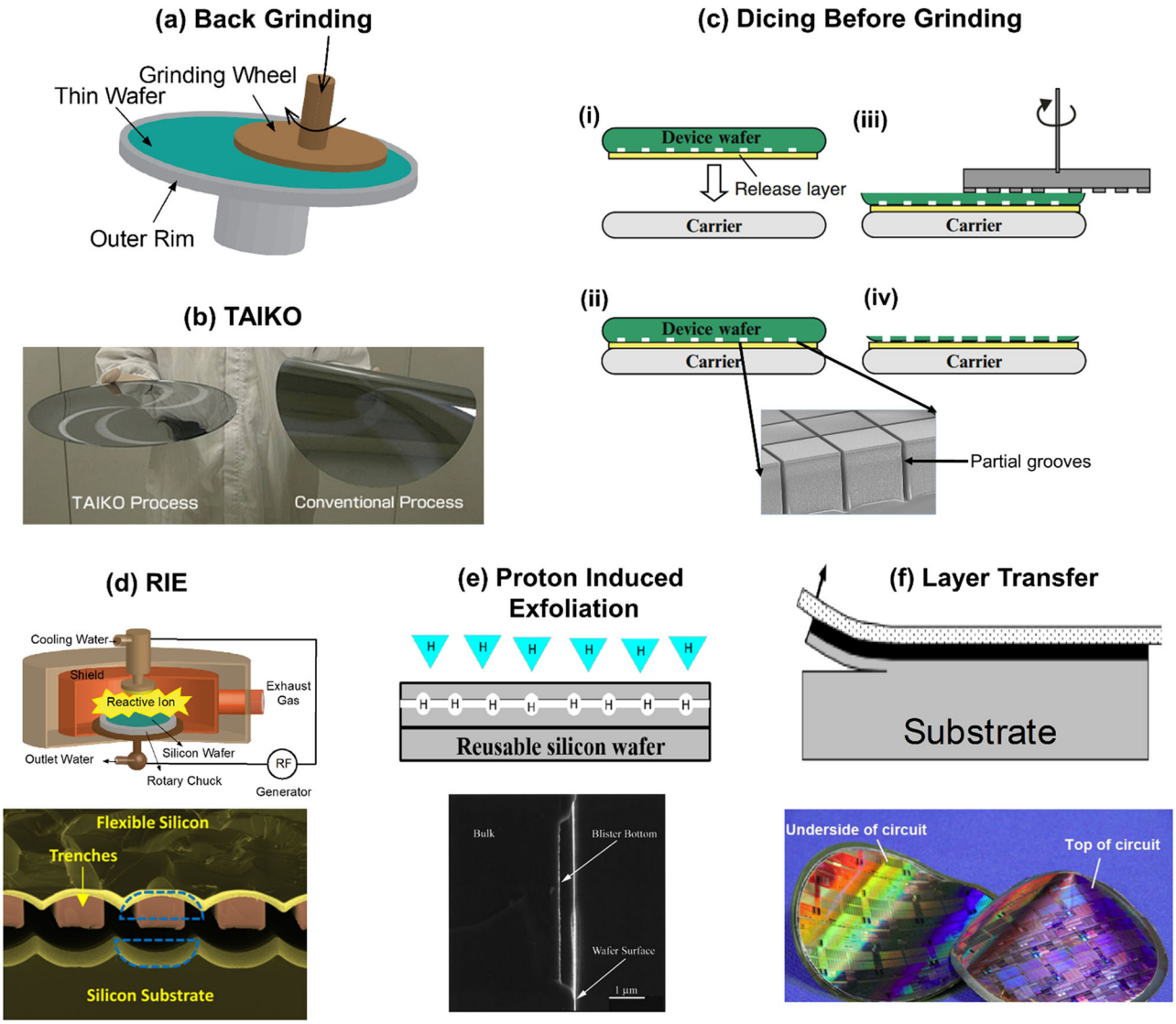

Fig. 5 **a** Illustration of Back Grinding. **b** TAIKO wafer vs. conventionally thinned wafer.[163] **c** Steps involved in Dicing Before Grinding.[164] **d** Illustration of RIE and SEM image of trenches etched between released top layer and bulk substrate.[165] **e** Proton-Induced Exfoliation technique and blister created after heating hydrogen implanted wafer.[166] **f** Illustration of controlled spalling and flexible wafer over polyimide.[155] Figure reproduced with permission from: **b** ref. [163], 2010 © Springer, **c** ref. [164], 2010 © Springer, **d** ref. [165], under a Creative Commons license (https://creativecommons.org/licenses/by/4.0/), **e** ref. [166], 1999 © AIP Publishing LLC and **f** ref. [155], under a Creative Commons license (https://creativecommons.org/licenses/by/3.0/)

high anisotropic behaviour but it comes with low level of selectivity (in absence of any additive) and surface damage. A few examples of RIE based UTCs include a 18 μm thick Si based thermoelectric energy generators[56] and Si probes of thickness 20 μm for floating chronic implantation in the cortex.[57]

Layer transfer processes: This method involves removal or exfoliation of the top processed layer. Two major processes developed based on this technique are: (i) proton-induced exfoliation and (ii) controlled spalling. In the case of proton-induced exfoliation, wafer is placed in a vacuum chamber after device fabrication and exposed to a beam of hydrogen ions. When heated, these ions which were implanted beneath the surface, expand as microscopic hydrogen bubbles—thus causing a very thin Si layer to detach from the surface, as shown in Fig. 5e. The wafer can be reused to exfoliate another layer of ultra-thin Si.[58] However, this method is not suitable for post-processing as electronic devices may be damaged because of high-energy proton exposure. Another layer transfer process is the controlled spalling technique, which takes advantage of strained conditions to obtain thin Si layer. Under specific strain conditions, a fracture on the edge of a brittle substrate can propagate parallel to the surface, as shown in Fig. 5f. This results in the detachment of thin slice of the brittle. This process can be carried out at room temperature and therefore it has advantages in terms of integration on flexible substrates. The techniques has been demonstrated with nanoscale flexible circuits (functional ring oscillators and memory cells) on 60 Å thick ultrathin Si[59] over the oxide of SOI. One of the challenges with controlled spalling is that it requires pre-calculation and monitoring of stress level to minimize the spontaneous fracture. This can be overcome with appropriate material and thickness of top film used as stress layer.

UTC via pre-processing techniques. Some technologies for UTCs require processing of wafers before initiating the device fabrication. These steps are termed as pre-processing steps and the front-end fabrication follows thereafter. The techniques for realizing UTCs which require pre-processing are discussed below:

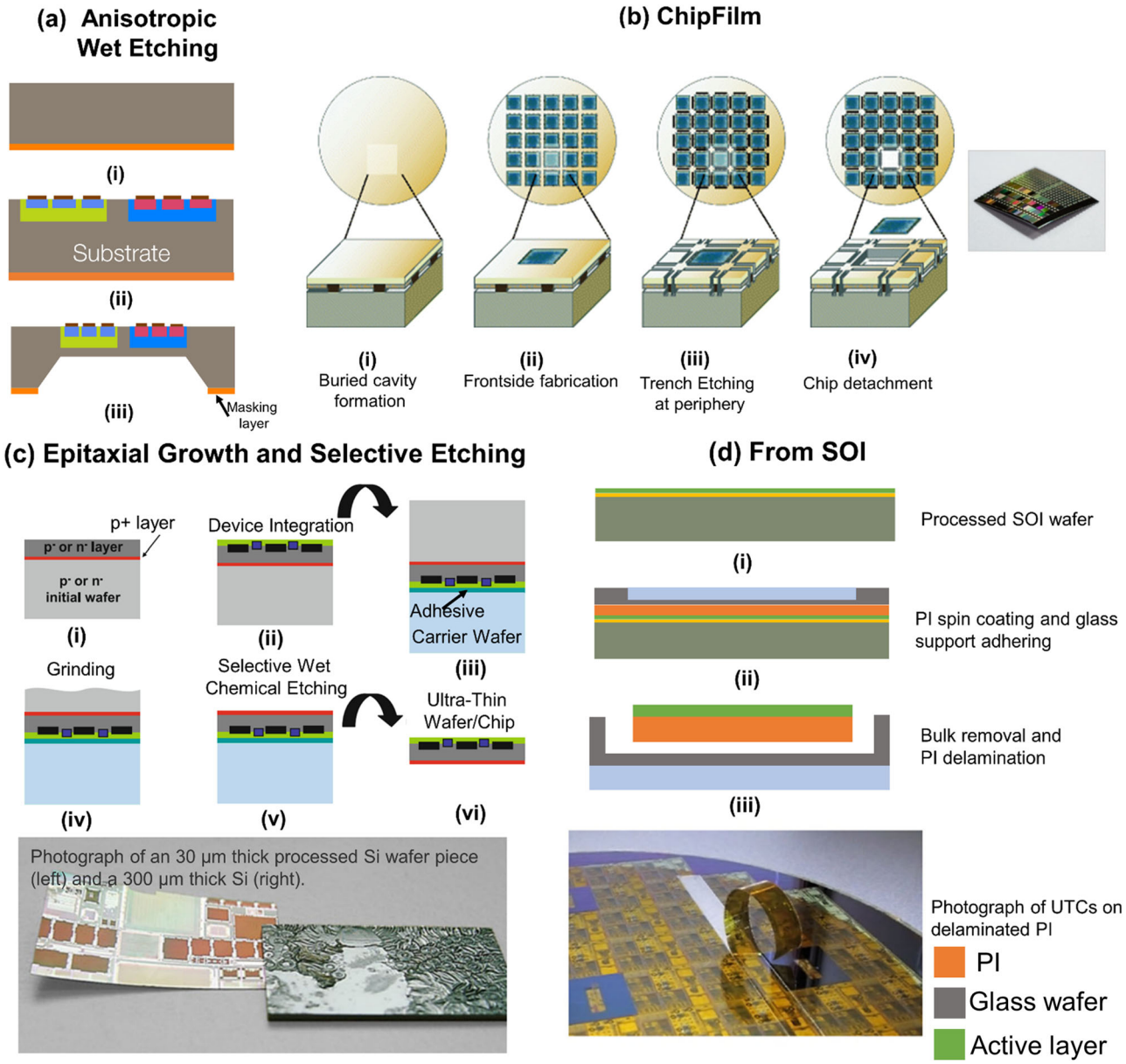

Fig. 6 Illustration of pre-processing and post-processing modules of **a** Wet Etching, **b** ChipFilm,[67] **c** various steps in epitaxial growth and selective etching approach[65] and **d** CirconFlex technique using SOI wafer.[168] Figure reproduced with permission from: **b** ref. [167], 2010 © Springer, **c** ref. [65], 2010 © Springer, **d** ref. [168], 2010 © Springer

Anisotropic wet etching: This well-established technology has been used traditionally to realize MEMS (microelectromechanical systems) structures.[60] The pre-processing steps for realizing UTCs involve depositing suitable mask layers (usually a combination of high quality SiO_2 and Si_3N_4) at defined locations on the back side of the wafer (Fig. 6a). This is followed by the device-processing steps on the front-side, and then etching of wafer from backside. The commonly used etchants for Si are hydrazine, EDP (Ethylene-Diamine-Pyrocatechol), TMAH (Tetra methyl ammonium hydroxide), and KOH (potassium hydroxide). The etching duration can be in hours depending on the concentration of etchant, the temperature and thickness of the wafer. The contamination from etchant and their CMOS compatibility is an important requirement,[61] among others including modulating etching with dopants or electrical bias, surface roughness, availability of suitable masking films, health hazards, and disposal issues. TMAH is the most commonly used etchant as it is IC-compatible, nontoxic, and has very good anisotropic etching characteristics. One drawback with TMAH is that it leads to higher undercutting than other etchants such as KOH. To overcome this issue the isopropyl alcohol (IPA) and surfactants are generally added to TMAH.[62] The wet etching can provide thin wafers at batch scale since many wafers can be processed at once. The wafer scale UTCs with TMAH etching and transfer to flexible substrate has been reported in literature.[13] The protection of front-side of the wafer from etchant is a critical for this route to obtain UTCs as otherwise the etchant may render the devices on the front side useless. To provide front-side protection, a custom wafer holder made from etchant resistant material or polymeric protection layer are used. The concentration of etchant is maintained regularly during this process to have better control over the total etch time leading to UTCs with desired thickness. A potential solution for monitoring

Table 3. Summary and comparison of various thinning techniques

Process	Need for pre-processing	Material removal rate (μm/min)	Typical thickness of semiconductor layer (μm)	Challenges	Ref.
Back grinding	No	0.1–10	5–10	● Deep scratches on backside ● Chipping at the edges	52, 191,192
TAIKO	No	0.1–10	50–100	● Dicing of membrane supported on ring can lead to breakage	193
Dicing before grinding	No	0.1–10	10–25	● >15 μm sawlane is required ● No metal line over sawlanes	194,195
RIE/DRIE	No	0.05–10	5–30	● Non-uniform surface ● Chances of frontside contami- nation due to reactive ions	196
Proton induced exfoliation	No	–	20–30	● Need of specifically designed proton accelerator	197
Controlled spalling	No	–	0.006–10	● Stress continuity across the lateral dimension is tough to maintain	59,198
Anisotropic wet etching	Yes	0.5–2	10–100	● Sensitive to temperature and etchant concentration ● Micro-masking led hillocks formation	13,199
Epitaxial silicon over porous silicon	Yes	–	10–25	● Stacking faults due to sintering ● Warpage on thin chip during detachment from supporting pillars	200
Epitaxial growth and selective etching	Yes	0.17–0.2	20–50	● Low thermal budget in post-processing step due to high temperature sensitivity of etch stop layer ● Extreme control over defects in $p+$ layer	65
SOI box/bulk removal	No	–	12–20	● Fixing and supporting the thin chip during transfer	168,201

the etch process is to exploit the change in optical transmittance with thickness, as discussed in the section "Ultra-thin chip properties".

Epitaxial Si based UTCs: The UTCs with devices having higher operating speed and better bipolar performance can be obtained by lifting-off Si epitaxial layer from the substrate. The two key approaches used for this purpose are: (a) Porous Si Approach, and (b) Etch Stop Layer Approach. The porous Si method, developed in 1990s, involves creation of a porous layer between substrate and the epitaxial layer.[63] Examples for this approach included the ChipFilm technology (Fig. 6b), which uses two layers of porous Si with different porosity and results in ~15 μm thick UTCs.[64] This technology allows good dimensional control and the mother wafer can be used repeatedly until exhausted. The yield of this technology heavily depends on the design and pitch of pillars in porous structure and hence the pre-processing step is critical. While this method is well suited for die-size UTCs needed in 3D ICs, the large area UTCs may not be practical due to cost considerations and risk of breaking due to warpage. One possible solution to address this issue is to use double transfer technique (i.e., using flexible carrier and substrate) instead of pick-place tool.

The etch stop layer method, typically used in a MEMS, takes advantage of the fact that doping could be used to stop etching. It involves developing a highly doped (p^{++} type) film at certain depth (roughly equal to desired thickness of UTCs) on the front side of wafer, followed by lightly doped epitaxial layer which act as active layer for device fabrication. Post device fabrication the wafer is chemically etched from back side until the chemical hits the p^{++} layer, which stops the etch process. The final thickness of UTC is the equivalent to the thicknesses of the epitaxial and p^{++} layer.[65] With a good control over the final thickness and uniformity of UTCs, this method (Fig. 6c) offers an alternative solution to the SOI wafer based approach. During growth process, the diffusion of impurities between Si wafer and p^{++} film may prevent the fabrication of an ideal step junction, which may lead to lower switching current ratio and hence the poor performance of electronics on UTCs. One way to control the impurity diffusion is to adopt low temperature epitaxial growth with a trade-off between high quality epitaxial film and higher impurity diffusion.

Using SOI wafer

SOI wafers provide a range of benefits relative to conventional wafer, such as, lower parasitic capacitance, resistance to latch up, lower leakage current, and immunity to radiation induced soft errors. While these features of SOI wafers enable high-performance electronics, their higher cost (~$1000 vs. ~$25 for a 6-inch bulk Si wafer) is a barrier. Nonetheless, despite this cost-performance trade-off, the SOI wafers are used in many niche applications such as low power high performance RF chips[66] and commercial devices such as IBM's PowerPC,[67] Global Foundry's 22FDX,[68] AMD's dual core module.[69] SOI wafer could also be used for high performance UTCs with precise thickness. This is achieved by fabricating electronic devices on the top active layer of SOI wafer, followed either by: (a) etching the buried oxide layer (i.e., BOX removal), or (b) thinning the backside of the wafer up to the required thickness or buried oxide (i.e., bulk removal) in which case the oxide acts as the etch stop layer.[70]

BOX removal. In this method, the trenches are etched around the chip on the front side and then etchant such as HF or XeF_2 is passed through these trenches to etch the oxide layer underneath, eventually detaching the top chip from the mother wafer. Since the trench formation is critical, the area available for device realization is limited and therefore well laid out design scheme is needed. Moreover, it calls for proper support of top Si layer as soon as it is detached from the bulk. Such challenges can be overcome through transfer printing using PDMS or similar intermediate carrier. Transfer printing of UTC based devices such as transistors, logic gates, RF components has been demonstrated for numerous applications.[16,71–80]

Table 4. Comparison between various flexible substrates used for packaging UTC

Material	Max. process temperature [°C]	Coeff. of thermal expansion [1/°C]	Thermal Conductivity [W/m-K]	Young's Modulus [GPa]	RMS surface roughness [nm]	Ref.
Stainless steel [304]	1023	16	14	190–203	33.8	202
Molybdenum	760	5	140	315–343	85	203
Polyethylene terephthalate	140	39	0.15–0.4	2.0–2.7	1000–1500	204
Polyimide	360	30–40	0.46	2.5	2	205
PDMS	150	310	0.15	$360–870 \times 10^{-6}$	0.88	206,207
Parylene C	109	38	0.08	3.2	13–25	208,209
Polyethylene naphthalate	155	20	0.15	5	0.64–0.68	210,211
Collagen	70	–	0.60	5.0–11.5	100	85,212
Silk fibroin	100	–1060	–	2.8	11.92	213–216

Bulk removal. In this process, the bulk Si is removed from backside by wet etching until the etchant reaches the buried oxide. In this case, the buried oxide acts as the etch stop layer and UTC thickness is sum of active layer and BOX thicknesses. A variant of this technique developed by Philips is named as Circonflex. Based on substrate transfer technology, this process enables the transfer of top functional layer of SOI wafer to practically any flexible substrate as shown in Fig. 6d. The method has been demonstrated for realizing 10 µm thick RF-ID tag chips.[81]

Table 3 summarises above methods with their key specifications and associated challenges.

INTEGRATION OF UTCS ON FLEXIBLE SUBSTRATES

For fully flexible systems with reliable operation, the UTCs need to be packaged over flexible substrates, sometimes with more than one chip on the same substrate. The choice of substrate is critical and depends on the inherent material properties and the intended application. The materials which have been used as flexible substrate can be broadly divided into two categories, i.e., polymeric and metallic (Table 4). An insulation coating is generally needed for electrical isolation of UTCs and to connect them to various components on flexible substrate and external connections. However, there are some exceptions such as solar cells where the required common back contact is achieved by transferring UTSi (Ultra-Thin Si) on flexible metallic or conductive-material-coated polymeric substrates.[82] The metallic substrates for flexible electronics have an added advantage as they can serve as heat sink or means for thermal reliefs. Further, they can be useful in applications such as electrical waveguide or where electromagnetic shielding is required. This can also be achieved with polymeric substrates coated with a thin conductive material including metals.[83] However, metallic substrates have inherent tendency towards retaining the shape on deformation, which may not be desirable. In this regard, thin polymeric substrates are advantageous as they are inherently elastic and flexible with ability to regain their normal shape. An alternative approach is to use a stack of both polymeric and metallic substrates and engineer the structure to realize smart substrates with desired properties. Thermal properties of substrate such as coefficient of thermal expansion and thermal conductivity should also be considered as they influence integration and thermal management of UTCs. As the stress level in UTCs is influenced by elastic properties of the substrate, generally a material with lower Young's Modulus is preferred. With the increasing interest in health or bio related applications such as implantable systems, bio-compatibility of substrate is also an important parameter to consider. Bacterial cellulose membrane, collagen, silicone gel and silk fibroin etc. have been used in such applications as they also offer better integration with tissues.[84–86] A comparison of various flexible substrate used for UTCs is given in Table 4.

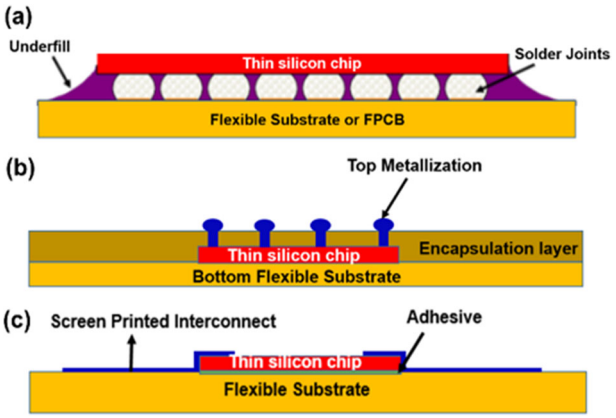

Fig. 7 Major schemes of packaging UTC: **a** Flip-Chip packaging of UTC, **b** UTC lamination between two flexible layers and **c** UTC on flexible substrate with screen-printed connection

The most challenging task in the packaging of UTCs comes when the contact pads on the chip are to be connected to the extended pads on the substrates. Wire bonding technique, which is widely used for traditional packaging is not suitable for UTCs, which are fragile and can crack due to the impact of bonding head-tool.[87,88] Further, the bond wires protruding out of plane of UTCs add to the thickness and affect the form factor. These challenges are driving the search for suitable materials and techniques for UTC packaging. The integration of UTCs on flexible substrate have been achieved mainly by the following three techniques.

Flip chip assembly on flexible substrate

In this style of packaging, UTCs in face down configuration are assembled on polyimide or liquid crystal polymer (LCP) substrate through flip chip bonder,[89] as shown in Fig. 7a. In the case of polyimide substrate, the solder bumped die are reflow soldered to the patterned flex. In the case of LCP, vias are etched through to expose the underside of contact pads. However, these solder bumps become coarse due to ageing and the growth of intermetallic compound, which eventually results in a changing shear mode and increase of resistance.[90] A right combination of temperature and pressure at the curing step is needed during flip

chip technique to get reliable electrical joints from bumps.[91] The major limitation of flip chip techniques is seen in the case of packaging of sensors requiring their sensing area to be exposed, as in the case of POSFET (Piezoelectric oxide semiconductor field effect transistor), ISFET (ion sensitive field effect transistor) etc.[92,93] This could be addressed by selectively removing the substrate from sensing area.

Laminating UTCs between two flexible layers

This type of packaging generally aims to put UTCs in the neutral plane by embedding it between the substrate and encapsulation layer, as shown in Fig. 7b. The advantage of this approach is that it leads to a reduced stress on UTCs and as a result the electrical response of UTC is minimally affected by bending. The integration of UTCs between two polyimide layers has been demonstrated for conformable and wearable wireless ECG monitoring system.[94,95] A challenge with this type of packaging is that the heat produced during device operation cannot escape to ambient. This could lead to high local temperature and can damage or degrade the device performance, as also discussed in the section "Ultra-thin chip properties". Moreover, the adhesion between the polyimide and the Si may vary due to localized area of high temperatures and this could lead to uneven adhesion of package or air bubbles formation within the package.[96] In this direction, the on-chip cooling mechanism could be explored. For example, the nanostructured super lattice-based thin-film thermoelectric material (e.g., Be_2Te_3) integrated with Si based electronics results in reduction of temperature by ~14.9 °C at target site.[97] Similar advances could be explored for UTCs to improve the reliability of package. Recently, embedding of micro-air vertical channels in UTCs have been reported for faster cooling and lower constant load saturation temperature.[98,99] Use of flexible materials with high thermal conductivity (e.g., copper, graphene, etc.) and structuring them as fins to act as a heat sink or using commercial thermal conductive tape outside the package are other potential solution.[100,101]

UTCs on foil with printed connections

In this approach, UTC are placed in the face-up configuration on the flexible substrate using epoxy based adhesive. Conductive wires are printed-on top of flexible substrate to realize electrical connections between the chip and the substrate, as illustrated in Fig. 7c. Screen printing or ink-jet printing is used to connect the contact pads on chip to the external connections on the flexible substrate. Silver based conductive ink and polymer based conductive material like Poly (3,4-ethylenedioxythiophene): polystyrene sulfonate (PEDOT:PSS) have been used for this purpose.[102,103] The silver ink provides much higher conductivity than PEDOT:PSS but it is susceptible to cracking during bending.[16] On other hand, PEDOT:PSS provides more flexibility than silver ink but shows low conductivity. A durable connection by combining screen printed silver grid with PEDOT:PSS could be a potential solution.[28,104] Although printing is simple and can be extended to large area, due to poor resolution of printers the contact pads and wires realized through printing are usually big in comparison to contact pads on the chip. This issue will be overcome with advances in printing technologies.

For fully flexible electronics system other materials may also be used in conjunction with UTCs.[105] For example a:Si/Poly-Si, inkjet or transfer printed nanowires,[106,107] 3,3‴-didodecylquarterthiophene (PQT), solution processed organic/inorganic materials such as peri-xanthenoxanthene (PXX),[108] Lithium Super Ionic CONductor (LISICON),[109] pentacene,[110] dinaphthothienothiophene (DNTT),[111] copper hexadecafluorophthalocyanine (F16CuPc),[112] PEDOT,[113] and thixotropy materials,[114] etc. could be used to obtain advanced multifunctional flexible electronics systems.

APPLICATIONS OF UTCS

A wide range of applications require UTCs as through underpinning high-performance electronics they enable advances in several areas, as illustrated in Fig. 1. The UTCs form the key components of various smart systems as sensing units, data processing or storage unit, driving or output unit and power or energy management units etc. Depending on the application requirements, the specification of electronics/sensing components on UTCs may vary. Some of the applications where UTCs are used as sensing units, data processing or storage unit, driving or output unit, and power or energy management units are described below.

Sensing/input

UTCs smart sensing units offer interesting solution for several existing applications such as implantable systems, neurotechnology, wearables, robotics and prosthetics etc. Futuristic applications such as body area network, body-dust, neural interfaces, bidirectional prosthesis, internet of everything and smart homes etc. will also benefit from UTCs based sensing units. As tactile interface chip for flexible touch panel, the UTCs will bring transformation in flexible portable devices (Fig. 1)[115] and e-skin for prosthesis or robotics (a flexible and transparent electronic skin as illustration for sensing/input in Fig. 1).[116–119] Portable devices such as smartphones are expected to be flexible in the future, and for this to happen various components including touch panel should be flexible. In such cases, the active tactile layer could comprise of large area flexible material such as graphene,[116,120] but the sensory data from array of taxels will be processed locally by a tactile interface IC or neuromorphic ICs before the data is transferred to complex computing hardware. UTCs will strengthen the capability of such systems by enabling features that require high-performance such as multitouch sensing, 2D/3D gestures, handwriting recognition, pen/stylus input, pressure sensitivity, fingerprint recognition, and security operations.

In order to achieve biomimetic tactile sensing, about 250 MRs/cm^2 are required in the fingertip of prosthetic limb,[121] which could be achieved by high density tactile sensors such as flexible POSFET that can conform to fingertips.[122] Further, UTCs could be useful for large area tactile skin based on planar off-the-shelf electronics integrated on FPCBs.[123] Lack of bendability of electronics has often limited the use of large area skin to body parts with large curvature. UTCs are ideal to address such applications as besides high-performance sensing they could also conform to the curved surface of prosthesis.

Implantable systems have brought a distinctive transformation in the field of medical diagnosis and treatments.[124] Flexible microchips with integrated sensors or microelectrodes are advantageous for applications such as brain interfaces as they can conform to soft tissues and hence allow recording of reliable data. Flexible UTCs with RFIDs encapsulated with biocompatible liquid crystal polymers has been successfully implanted and tested.[80] UTCs also find application in video endoscopy, smart catheters, diagnostic pills, sub-retinal implants, neural interfaces,[125] swallowable smart pill[126] and tactile functional prosthetics etc.[127,128] In the field of medical diagnosis, UTCs find application as conformal retinal implant for blind vision, electromyographic and/or neural prosthetic implant, and blast sensor patch in sports/military helmets to detect trauma injury. Neurotechnology is another area which will greatly benefit from electronics that bends, stretches and conforms to curved surfaces. For example, complementing current in vivo studies, the flexible and conformal microelectrode arrays will offer powerful new tool in traumatic brain injury research. UTCs are attractive for such applications as in addition to the active microelectrodes they could also offer functionalities such as wireless communication.

Thanks to the flexibility and conformability, the UTCs will be far more comfortable for people using them.

In applications for health monitoring[129] where the devices are worn or wrapped around the body the high-performance and compact electronics on UTCs could provide solutions such as measuring human pulses on wrist, and orthodontic forces of invisible aligners for dental treatment.[130] The convergence of soft and deformable textiles technologies with high-speed computational capacity of UTCs is another application.[131] The rough and uneven surface of fabric makes it difficult to have seamless integration of UTC, which could be solved by using smoother intermediate layer between textile and UTC. The UTCs can have sensors, interconnects and processor for on-chip processing of the data. This type of arrangement will greatly influence the applications such as military garment devices, antibacterial textiles, and personal electronics like MP3 jacket and smart carpet.[132]

Data processing/storage

The consumer electronic devices such as smart phones, mobile gaming systems, and ultrabook computers etc. have fueled the growth of semiconductor industry in recent years. Consumer prefer smaller, thinner, and lighter systems with additional features such as wearable to meet their mobile lifestyles. Thanks to Moore's law and ITRS roadmaps,[133,134] CMOS technology has come a long way breaking many challenges with many material and technology innovation leading to the current state-of-the-art. Commercially, 14 nm technology FinFET based microprocessors are available which operates at >4 GHz and now gearing to 10 nm.[135] Considering the huge number of objects, with different size, shape and rigidity, which will be connected in IoT environment, high performance, and mechanical flexibility of devices employed in these objects is inevitable. As discussed in the section "Introduction", the wireless communication in IoT will require data handling ultra-high frequency range. UTCs will be useful here as they could support faster communication, high bandwidth, and efficient distributed computation with very high switching speed. With interconnect schemes such as through-silicon-vias, low power consumption and excellent high performance, the UTCs have potential for 3D integrated circuits (3D ICs) to handle large amount of data and processing in IoT concept.[136,137]

Flexible portable devices, smart contact lenses or augmented reality systems are some other areas where UTCs could trigger advances as they could enable high-speed computation at lower power and high-density storage. The Ferroelectric Random Access Memory (FeRAM) based on flexible silicon shows superior performance and can be good choice for flexible memory applications for IoT.[138] Emerging memory devices such as RRAM (Resistive random-access memory), memristors, and other high density nanoelectronic non-volatile memories could also be integrated with UTC technology.

In applications such as bidirectional prosthesis at par with human hand, the electronics on e-skin should process data from 18k mechanoreceptors (MRs) to mimic the glabrous palm area of a hand. As number of sensory components increase, there is demand to handle large data.[139] The on-site processing and signal conditioning of the raw data can be fulfilled by UTCs integrated on the e-skin. While the active tactile layer could comprise of large area flexible material such as graphene, the sensory data from array of taxels should be processed locally by a tactile interface IC before it is fed into the computing chip. The high-performance UTC serve are ideal for such task. They could also reduce the load on the computing block or could enable new features such as multitouch input, 2D and 3D gestures, handwriting recognition, pen/stylus input, pressure sensitivity, fingerprint recognition, and security operations. In areas such as wearable systems, where different modules need to communicate within and outside the system, the UTCs could be used to develop components for body area networks, and RF communication such as Bluetooth 4.0 low energy communication etc.

Driving/output

The UTCs could also offer solution for efficient driving or output unit for many applications such as optogenetics, flexible portable devices, antenna, actuators. The drive units should provide precise control on current and/or power and/or voltage and/or timing. As an example, in optogenetics pulses of light with spatiotemporal precision are needed to stimulate the neurons and UTCs could be used to achieve this. Typically, optogenetic stimulation is carried out by external light source with fiber-optics to deliver the light to the targeted location. Typical driving requirements is such application are precise temporal requirement i.e., rise time and fall time (10–90% and vice-versa) of current pulses <100 µs and in some specific applications <1 µs and current level up to 1.5 A. Such an arrangement is cumbersome and involves tether. Tether-free implantable miniaturized optogenetic systems are preferred in such cases and UTCs based drivers could provide the required temporal and spatial resolution. Further, with UTCs it will be possible to achieve multi-wavelength and multi-array microLEDs (µLED) targeting various optogenetic channels (corresponding to various opsins) such as channelrhodopsin,[140] halorhodopsin,[141] archaerhodopsin,[142] bacteriorhodopsin.[143] The typical current requirement for such µLED driving is 2–5 mA.[144] Depending on the requirements, the compound semiconductor layers for µLEDs could also be grown or transfer printed on Si, from which UTC is fabricated. Such implantable optogenetic chips can communicate with external transceivers through RF communication in which case UTCs could drive the antennas. Similarly the UTCs could provide the drive/output unit in bidirectional prosthesis, treatments for epilepsy, cardio-arrhythmias, drug addiction, and brain/neural circuit mapping.[145,146] UTC could also find application in driving flexible pacemakers and defibrillators. For example, the UTC chips integrated with EMG sensing electrodes could process the signal in real-time to identify potential arrhythmia. Wherever needed, they could drive the electrodes to provide stimulus for pacing, cardioversion or defibrillation. UTCs could also drive various components in wearable systems such as LED drivers for pulse oximetry, electro-tactile stimulation, haptic communication gloves for deaf-blind,[147] bendable oral systems (for example to control prosthesis[148] or wheelchair,[149]) smart insole for health monitoring and prosthesis control.

In applications such as smart portable display, there is a growing interest in manufacturing portable devices with flexible display that can undergo bending, flexing and rolling. While flexible AMOLED display are commercially available,[115] for flexible smartphone various components such as battery, driving unit, communication chip etc. are not bendable yet. Some of these form the areas of active research, for example, flexible batteries.[150] With high performance flexible circuits, UTC could remove the current bottlenecks for flexible displays.

Power management and energy harvesting

Optimizing battery life for portable systems presents a significant engineering challenge for system designers. While low power high efficiency FETs help in achieving this goal to some extent, alternative approaches are being explored by researchers to harvest energy to develop energy autonomy.[116] Current solutions such as batteries require charging at regular intervals. However, for applications such as health monitoring devices it is advantageous to power the device with energy harvested from the ambient, such as light, heat or motion.[55,56,151,152] UTSi and UTC technology could help in addressing the need for power management and energy harvesting using high efficient flexible

solar cells, buck or boost DC-to-DC convertors, power electronics drivers. Photovoltaic technology is one area where thin Si was initially used as explained in the section "Historical perspective". Due to continuous growth rate over the last decade, the cumulative installed capacity of photovoltaics have exceeded 303 GW-peak by the end of 2016.[153] Monocrystalline silicon based PV with their long life span (up to 40 years) and high conversion efficiency (15–26%) is a better choice.[154] However, the higher cost of monocrystalline silicon (compared to amorphous or micro-crystalline silicon) makes it expensive. In this scenario, UTCs present an interesting avenue.[155,156] The solar grade large wafers (>8" diameter) are best choice for manufacturing solar panels with ultra-thin Si as active material. However, with lesser thickness the special optical trapping techniques are required to harvest maximum light energy as explained in the section "Ultra-thin chip properties". The energy harvesting component in Fig. 1 shows array of micro photovoltaic cells made of monocrystalline Si.[157] Further, a graphene based transparent coplanar capacitive touch sensor combined with solar cells forming a smart energy autonomous electronic skin system is also shown in Fig. 1.[116] Thermal energy harvesting is another possibility, where a flexible harvester realized on the top of thin Si has been reported to produce around 30% more output power than that of realized on bulk Si.[56]

Thus, with several applications, the UTCs could bridge the gap between CMOS technology and several of the above mentioned emerging applications of flexible electronics.

CONCLUSION

The international roadmap for semiconductors (ITRS) highlighted the need for thin chips almost 15 years ago in context with 3D IC staking for system-in-package. In fact, the 2005 ITRS report laid emphasis on UTCs thinner than 20 µm as well as wafer thinning and handling, small and thin die assembly and packaging of thin chips. Until few years ago the demand for UTCs was primarily for 3D system integration, where multiple active dies having active and lateral interconnects are vertically connected through silicon vias. However, this is changing with emerging applications such as mHealth, wearable systems, smart cities, and IoT. The high-performance and flexibility of electronics needed in these applications are primarily pushing the interest in UTCs. In fact, these requirements have fuelled the research for high-mobility materials such as graphene, which owing to excellent electrical, mechanical and optical properties holds the promise for high-performance flexible electronics. However, the technology for these new high-mobility materials is not mature yet for large-scale integration. The limited success of electronics from these high-mobility materials and well-established Si based high-performance electronics respectively act as the push and pull factors of UTC research. A range of silicon based non-bendable devices are already being used in ad hoc arrangements in a wide ranging applications. With this background, this review article has presented and compared the ways to make bendable Si and variations in the response of devices on UTCs because of changes in electrical, optical and mechanical behaviour. Tremendous progress has been made for obtaining UTCs and a range of thinning methods used for this purpose have been compared in this paper.

Going forward, the major hurdles for UTCs will be in the areas related to packaging, modelling and dealing with the effect of stress and strain on electrical response of UTCs. The handling of thin fragile wafers and packaging of UTCs needs more attention. Unlike conventional chips, UTCs cannot be bonded easily with wire-bonder because of high chances of cracks when the bonder tip hits the bonding pad. Reliable and durable connection from chip to the substrate is a challenging task because of the bumps coarsening (in the case of flip-chip bonding) and chances of electrical discontinuity (in the case of screen-printing). With suitable thermal management and embedding the chip between two layers of pre-patterned electrical connection it is possible to overcome the bonding related issues. While much has been done to realize UTCs, the stress induced effects and related models are scarcely researched. A major reason behind the success of Si technology was the availability of accurate models to predict device response. However, this is challenging in the case of UTCs as they experience stress because of external bending. The modelling and simulation of devices on UTCs has not received sufficient attention and this will pose major challenge to the circuit designers. The cost of fabrication of UTCs is also argued as an area that requires attention, especially when they are realized from SOI wafer. However, with mass manufacturing of UTCs the costs will come down and this is likely to be a non-issue. In conclusion, despite many challenges the UTCs hold great promise for advances in many areas where high-performance flexible or conformable electronics are needed.

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AUTHORS CONTRIBUTIONS

S.G. and W.T.N. contributed equally to this work. L.L. and R.D. oversaw all research phases. In addition, R.D. led the preparation of the manuscript and contributed to modifications of the overall text.

ADDITIONAL INFORMATION

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