Study of Radiation-Tolerant Integrated Circuits for Space Applications

A Thesis Presented to the
College of Graduate Studies and Research
In Fulfillment of the Requirement
For the Degree of Master of Science
In the Department of
Electrical and Computer Engineering
University of Saskatchewan
Saskatoon, Saskatchewan
Canada

By

Yan Ding

PERMISSION TO USE

In presenting this thesis in partial fulfilment of the requirements for a Postgraduate degree from the University of Saskatchewan, I agree that the Libraries of this University may make it freely available for inspection. I further agree that permission for copying of this thesis in any manner, in whole or in part, for scholarly purposes may be granted by the professor or professors who supervised my thesis work or, in their absence, by the Head of the Department or the Dean of the College in which my thesis work was done. It is understood that any copying or publication or use of this thesis or parts thereof for financial gain shall not be allowed without my written permission. It is also understood that due recognition shall be given to me and to the University of Saskatchewan in any scholarly use which may be made of any material in my thesis.

Requests for permission to copy or to make other use of material in this thesis in whole or part should be addressed to:

Head of the Department of Electrical and Computer Engineering
57 Campus Drive
University of Saskatchewan
Saskatoon, Saskatchewan, Canada
S7N 5A9

ACKNOWLEDGEMENTS

Wherever I am and whatever I become, I shall never forget my parents. Their love is the greatest thing to me. Their love accompanied me growing up.

I would like to thank my thesis supervisor Professor Li Chen for his guidance and support. I also wish to thank Professor Saadat Mehr, Aryan S. for his financial support during my study here. My thanks are also due to Robert L. Shuler for his guidance, generosity and patience. I could not have completed this work without an excellent working environment and the support of several helpful faculty members and students at the Department of Electrical and Computer Engineering. I am grateful to the fabrication support provided by CMC and the helpful suggestions from the design community (https://forums.cmc.ca/index.jspa).

ABSTRACT

Integrated Circuits in space suffer from reliability problems due to the radiative surroundings. High energy particles can ionize the semiconductor and lead to single event effects. For digital systems, the transients can upset the logic values in the storage cells which are called single event upsets, or in the combinational logic circuits which are called single event transients. While for analog systems, the transient will introduce noises and change the operating point. The influence becomes more notable in advanced technologies, where devices are more susceptive to the perturbations due to the compact layout. Recently radiation-hardened-by-design has become an effective approach compared to that of modifying semiconductor processes. Hence it is used in this thesis project. Firstly, three elaborately designed radiation-tolerant registers are implemented. Then, two built-in testing circuits are introduced. They are used to detect and count the single event upsets in the registers during high-energy particle tests. The third part is the pulse width measurement circuit, which is designed for measuring the single event transient pulse width in combinational logic circuits. According to the simulations, transient pulse width ranging from 90.6ps to 2.53ns can be effectively measured. Finally, two frequently used cross-coupled LC tank voltage-controlled oscillators are studied to compare their radiation tolerances. Simulation results show that the direct power connection and transistors working in the deep saturation mode have positive influence toward the radiation tolerance. All of the circuit designs, simulations and analyses are based on STMicroelectronics CMOS 90 nm 7M2T General Process.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
C^2MOS	Clocked CMOS
CREST	Circuit for Radiation Effects Self Test
CS	Cross Section
DICE	Dual Interlocked Storage Cell
EMI	Electro Magnetic Interference
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
LET	Liner Energy Transfer function
MBU	Multiple-Bit Upset
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PGS	Patterned Ground Shield
PRN	Pseudo-Random Numeric block
RHBD	Radiation-Hardened By Design
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupts
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SERT	Single Event Resistant Topology
SET	Single Event Transient
SEU	Single Event Upset
SHE	Single Event Hard Errors
SOI	Silicon on Insulator
SOS	Silicon on Sapphire
TG	Transmission Gate
TID	Total Ionizing Dose
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Space Environment

In the Solar system, the Sun is a giant radiation source. It constantly ejects various energetic particles and rays, which act like a wind blowing toward every direction. The interaction between the Solar wind and Earth's magnetic field generates a radiation belt. It was firstly predicted by James Van Allen, an American astrophysicist, in 1958 and named as Van Allen belt. His prediction was confirmed from the information secured by launching the first U.S. earth satellite, Explorer I during the International Geophysical Year [1].

The Van Allen belt extends above the Earth at an altitude from about 400 km to 60,000 km, and this region has been termed as magnetosphere to distinguish from the atmosphere. This region is not uniformly distributed. On the side facing to the Sun, it is compressed, while on the other side it is elongated [2].

The Van Allen belt can be split into two distinct belts. The inner belt extends from about 400 km to 12,000 km above the Earth. It contains energetic protons with energies up to 400 MeV and electrons with energy range of hundreds of keV. The outer belt extends from about 12,000 km to 60,000 km above the Earth. It is dominated by a population of energetic electrons up to 10Mev [1][2][3].

Commercial Integrated Circuits (ICs) are susceptible to the radiations. Or even worse, they could be damaged. For instance, satellite shielded by 3 mm of aluminum in an elliptic orbit will receive almost all types of radiations when passing through the inner radiation belt [4].

1.2 Single Event Effects on Microelectronics

Single Event Effects (SEEs) are the perturbation behavior of the semiconductor circuits induced by a single, high energy ionizing particle [5]. SEE can result in data corruption and transient disturbance. If not handled properly, it could cause unexpected functional interrupts or even catastrophic failures.

SEE can be classified into non-destructive and destructive effects [6]. The one that changes the state of a circuit belongs to the former, which is also called a soft error. Representative phenomenon includes single event upset (SEU, corruption of the information stored in a storage element), single event functional interrupt (SEFI, corruption of a data path leading to loss of normal operation) and single event transient (SET, impulse response of certain amplitude and duration). On the contrary, the destructive effects interrupt device function and permanently damage the device. Representative phenomenon includes single event latch-up (SEL), single event burnout (SEB, destructive burnout due to the high current conditions), single event gate rupture (SEGR, rupture of gate dielectric due to high electrical field conditions), and single event hard errors (SHE, unalterable change of state in a memory element).

SEUs are the radiation-induced errors in digital systems, which are caused by energetic particles (usually from the radiation belts or from cosmic rays) [7]. Normally, they appear as the bit flips in memory cells or registers. If the particle travels through multiple nodes and upsets many of them, it leads to the Multiple-Bit Upset (MBU).

SETs are the transient responses due to the energetic particle strike. They refer to the voltage pulses propagating through the circuit. Different from SEUs, SETs may not cause the error unless they are latched in a storage cell.

1.3 Brief History

The occurrence of SEU was firstly forecasted by Wallmark and Marcus in 1962 [8] and the first confirmed report was presented at the NSREC (Nuclear and Space Radiation Effects Conference) in 1975 by Binder et al. [9]. The term "single-event upset" was firstly appeared in the paper of Guenzer et al. [10]. SEL was firstly reported in the year of 1979 [11].

Soft errors in terrestrial microelectronics manifested shortly after the first observations of SEU in space [12]. In their work, the primary cause of soft errors at the ground level was diagnosed not from space but rather from concentrations of uranium and thorium presented in IC packaging materials.

The flourishing development in fabrication technologies toward smaller feature sizes and higher speed brings significant challenges in maintaining system reliability. In the 21st century, radiation-hardened-by-design (RHBD) becomes a useful method when facing the challenges. "In RHBD, electronic components are manufactured to meet

specified radiation performance criteria, but the techniques employed to meet these criteria are implemented either in layout or in the application architecture and not in the fabrication process. RHBD is typically considered distinct from radiation-hardening-by-process (RHBP)" [13]. RHBD provides a cost-effective solution compared to RHBP.

Registers are important components in digital circuits, and they are susceptible to SEUs. Some researchers have conducted related works to improve their reliabilities. Calin et al. proposed a popular dual-redundancy storage cell – DICE, to settle SEU problem in sequential logics and memory array [14]. Following their work, more reliable structures were developed. Casey et al. used Cascode-Voltage Switch Logic (CVSL) gates to substitute the inverters in DICE [15]. The designs were implemented with IBM CMRF8SF 130nm technology. According to the simulations, their design is immune to multiple node hits. Heavy ions with LETs from 10 to 100MeV-cm^2/mg could not lead to upset. In 2005, Balasubramanian et al. presented another solution [16]. In their work, the DICE was further enhanced by replacing the inverters with guard gates. They implemented the designs and ran simulations to evaluate the electrical performances. Shuler et al. proposed their own dual cross-coupled storage cell and realized dual-rail registers [17].

1.4 Motivations and Thesis Outline

Some of the storage cells exhibited excellent radiation tolerance in previous technologies. So we would like to see if their performances are still acceptable (or how they perform) in a more advance technology (it is also more sensitive to the radiation effects). In this work, these storage cells will be adopted to build registers. Circuits will

be implemented in the CMOS 90 nm general process. We will investigate their radiation tolerances under various radiation intensities. To count the SEU rates of these registers, two built-in test structures will be implemented. After fabrication, energetic particle test will be performed to evaluate their radiation tolerances and find an optimal solution for the space applications. We would also like to establish a relation between the radiation intensity and the SET pulse width in this technology. So we will implement a SET pulse width measurement circuit to capture and measure the voltage pulses in combinational logic circuits.

Voltage-controlled oscillator (VCO) is an important component in many systems like frequency synthesizer, clock and data recovery circuit and clock generator. It is sensitive to the SET introduced noise. Through this study, we are trying to find a solution for the space applications. In this work, two frequently used structures will be studied. The circuits will be working in the different operating points so as to find the key parameters determining the radiation tolerance.

This thesis is arranged as follow: In chapter 2, radiation effects in microelectronics will be introduced. Charge collection, SET effects in a CMOS inverter and the SEU effect in a conventional storage cell will be introduced. The radiation tolerant registers, built-in test structures and SET pulse width measurement circuit will be discussed in Chapter 3. In this Chapter, the mechanisms of the radiation tolerant storage cells and the clock realization approaches will be discussed in detail. Chapter 4 is a specification of the test bench, PCB design and the test methodologies. Two types of cross-coupled LC VCOs will be studied in Chapter 5. In this chapter, the SET will be imitated by Cadence

Spectre, and the frequency responses of the circuits will be analyzed. Chapter 6 will make a conclusion to this thesis and present several suggestions on the future works.

Chapter 2

Radiation Effects on MOS Devices

This is a transition chapter which particularly expatiates on the radiation effects and provides a theoretical basis for the following chapters. The energetic particles bring undesired effects to semiconductor devices like SEEs, total ionizing dose (TID) effects and displacement damage. In this chapter, a useful concept, linear energy transfer, is firstly introduced. Then the charge collection, SET effects in a CMOS inverter and SEU effects in a conventional storage cell are discussed in detail. Finally, we briefly introduce SEL and TID effects.

2.1 Linear Energy Transfer

Linear energy transfer (LET) is the energy deposited per unit path length as an energetic particle travels through a material. LET for SEE studies is the mass stopping power defined by:

$$\left(dE / dX\right) / \rho \tag{2.1}$$

The dE/dX is the energy loss per unit path length, whereas ρ is the material density. Equation 2.1 results in an LET unit of MeV/(mg/cm^2) of material, which is the energy loss per density thickness. The density thickness describes the areal density of electrons

(electrons/cm^2). LET varies enormously with the particle involved, energy, and the material traversed [7].

A single high LET particle can generate net charges in the semiconductor substrate. Under an external electric field, some of the charges recombine while the others drift. Eventually, the latter can be collected at sensitive nodes. If the charge amount exceeds a threshold (LET_{th}), an SEE may occur in the circuit, affecting the electrical performance of the circuit. As a matter of fact, solar event protons and protons trapped in the Earth's radiation belt are the primary LET sources for commercial products [5].

The cross section (CS or σ) for a SEE measures the probability for a SEE to occur. It is a function of the LET. Below the LET_{th}, the collected charge in the sensitive node is too low to induce a SEE. Saturation cross section (CS_{sat} or σ_{sat}) defines the upper limit for a SEE. LET_{th} and σ_{sat} are the key measures of a SEE [5][18]. The CS-LET relationship is useful when evaluating the circuits' radiation tolerances.

2.2 Charge Collection and Single Event Transient

In conventional semiconductor processes, metal and polysilicon layers are insusceptible to SEEs due to the low resistivity [19]. Whereas, the energetic particles can generate electron and hole pairs when penetrating the substrate and losing its kinetic energy. Some of the generated charges cannot recombine immediately. Figure 2.1 illustrates the cross section of a CMOS inverter, which is the elementary component in digital circuits. An energetic particle is traveling through a NMOS transistor. Once charges are generated in the epitaxial, the electrons will be swept into the reverse-biased

PN junctions, consumed by the power rail or neutralized by the positive charges. And the holes will drift along the electrical field, and be consumed by the ground through the bulk contact. The charge collection could happen at multiple nodes simultaneously depending on the dimension and integration density. If a PN junction is on the path of the strike particle, the equilibrium in their depletion region will be temporarily disturbed. A high conductance path will be formed and extended to the substrate. This phenomenon is termed as funneling effect, which can enhance the charge collection effect [20][21].

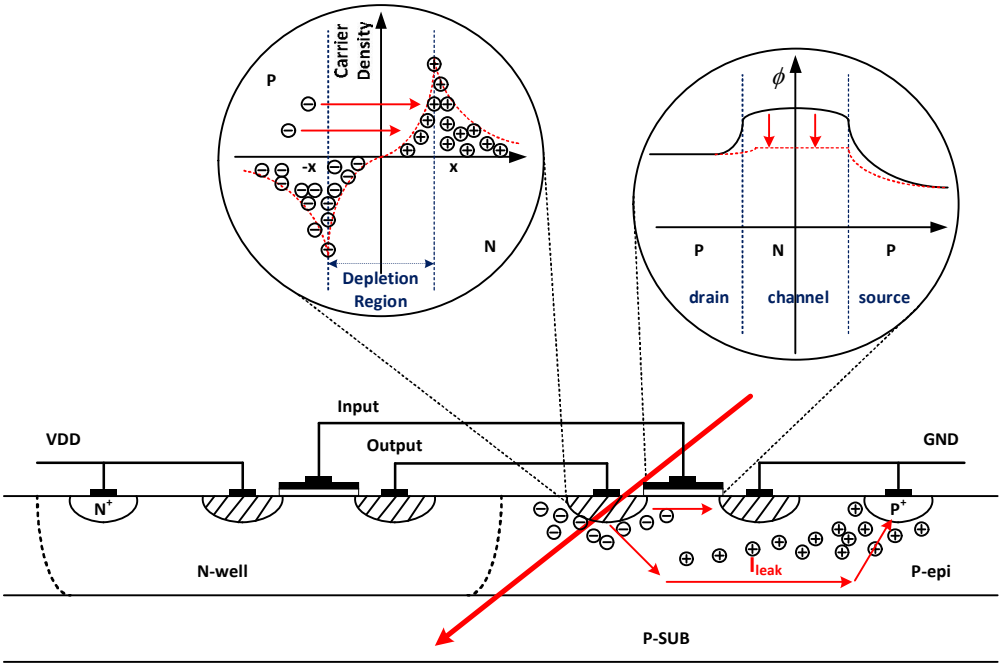

Figure 2. 1: Charge collection and SET in a CMOS inverter

Besides, a new mechanism from the funneling effect has been verified. A particle travels horizontally may pass through both the source and the drain of a MOSFET, disturb the PN junctions, and produce a low conductance path. For digital circuits, it will

make a momentary pseudo “on” state to the transistor; while for the analog applications, it will shift the I_{DS} and transconductance. This channel conduction mechanism is also closely linked to the size of active device and layout density. In advance technologies, particles can even lead to this phenomenon from non-zero incident angles [20].

If the particle is strong enough and the charge amount exceeds the threshold (LET_{th}), it will cause a transient current flowing from the drain to the source or from the drain to the P^+ contact of the substrate. The potential at the output node will be temporarily pulled down. Thus, lead to a SET in the CMOS inverter. The amplitude and duration of the transient pulse is determined by the total collected charge. Although the analyses are based on a NMOS transistor, they are also suitable for PMOS transistors.

In a semiconductor device, some nodes (Like the NMOS transistor’s drain region in the CMOS inverter, just analyzed above.) are highly related to the SEE. The particles traveling through these nodes or the charge collections in these nodes can directly lead into SEEs and hence cause soft errors. These locations are termed as sensitive nodes. They should be carefully treated in the study of radiation tolerant designs.

2.3 Single-Event Upset (SEU) in Storage Cell

The conventional storage cell is made up of two interconnected inverters. Besides the radiation intensity and particle strike location, whether a SEU will occur depends on the fabrication processes, layout styles and transistor dimensions. These factors determine the RC values in the storage loop. Smaller RC delay means less time required for writing operation, but it also makes the circuit more vulnerable to SETs.

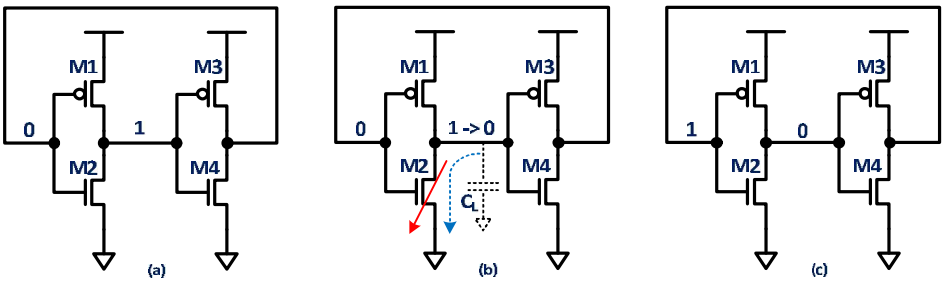

Figure 2. 2: SEU at conventional storage cell

Figure 2.2 depicts the conventional storage cell when encountering an energetic particle strike. From (a), two inverters are connected back to back. There are two internal storage nodes, with opposite logic values. When the particle strikes at a sensitive node, the drain region of M2, as shown in (b), the net electrons will be collected and neutralized by the excessive positive charges in the storage node. Or an instantaneous conductive channel might be formed and the internal load capacitor C_L begins to discharge. As analyzed in Section 2.2, these effects can pull down potential of the storage node. If the collected charge exceeds the threshold, the bit information will be changed, as shown in (c), and a SEU happens. The new bit information remains even after the transient fades away.

2.4 Single-Event Latch-up (SEL)

SEL is the latch-up phenomena induced by energetic particles. It happens when the particle strikes the parasitic thyristor inherent in bulk CMOS technologies and causes a short circuit current from the power to ground. SEL is strongly temperature dependent. As the temperature increasing, the cross section increases and the threshold for SEL decreases [6][7]. It is a critical effect with potential hazard for space borne

microelectronics. Epitaxial substrates, silicon on insulator (SOI) or silicon on sapphire (SOS) are often used to mitigate the susceptibility [22]. The SEL can also be effectively suppressed by applying layout techniques like guard rings and guard drains. SEL is a destructive radiation effect. It is mitigated through fabrication processes and layout techniques, which are out of our interest. It is not included in this research.

The miniaturization of semiconductor devices, increment of the integration density and the operation frequencies have negative influences on radiation tolerance. In general, the SEE can be mitigated from different approaches, including fabrication process, gate/circuit level and system level. From fabrication point of view, the SEE problems are settled through special processes like SOI and SOS. In the circuit level, devices/circuits are hardened by sacrificing the electrical performances and layout area. While in the system level, redundancy techniques are applied to improve the reliability. Our research focuses on non-destructive SEE in bulk CMOS processes, and we are working on the approaches to mitigate SETs and SEUs at gate/circuit level.

2.5 Total Ionizing Dose (TID) Effects in MOSFET

The total ionizing dose (TID), mostly due to electrons and protons, is the cumulative ionizing radiation that a semiconductor device receives over a specified period of time. It can be measured in terms of the absorbed dose, which is a measure of the energy absorbed by matter. The unit is rad (radiation absorbed dose) [23][24][25]. In Si the unit is gray (Gy), 1Gy=100rad=1J/kg.

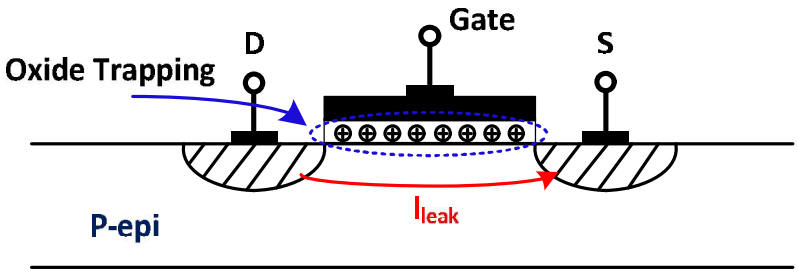

Figure 2. 3: Charge trapping at Si/SiO_2 interface

As depicted in Figure 2.3, ionization can excite carriers from the conduction band to the valence band and the charge trapped at interface of Si/SiO_2 will change the characteristics of the channel. Electrons have higher mobility so they are quickly consumed, whereas the holes are trapped at the interface. One of the typical influences is the threshold shift in MOSFETs. The TID strongly depends on the bias condition and fabrication process [25].

TID and SEE are both resulted from the ionizing radiation. The former is a long time effect, which changes the electrical properties of the device, while the latter is an instantaneous perturbation due to the energetic particle strike. The TID effect is insignificant in advanced technologies since the gate dielectric is too thin to trap the charges. This work focuses on the SEEs and ignores the TID.

Chapter 3

Radiation-Tolerant Registers and Built-in Test Structures

In this chapter, radiation-tolerant registers are introduced in detail. Radiation-tolerant storage cells and SET mitigation technologies are presented in Section 3.1; then the clock control and register implementation are discussed in Section 3.2; in Section 3.3, another register designed by the research group from Avionic Systems Division, NASA Johnson Space Center is introduced. Subsequently, two test structures are built for the energetic particle testing. Finally, a pulse width measurement circuit is introduced to estimate the SET pulse widths in combinational logic circuits.

3.1 Radiation-Tolerant Storage Cells

Storage cells are the basic component in sequential logic circuits. In this section, several radiation tolerant cells are introduced to overcome the SEU problem.

3.1.1 Dual Interlocked storage Cell (DICE)

DICE is a commonly used radiation tolerant approach for latches. As shown in Figure 3.1, the cell is made up of four interlocked inverters instead of two [14]. It has four internal storage nodes. This structure is more reliable when exposed to the radiation

environments. Normally it has two inputs connecting to the interleaved nodes separately, for example, node 1 and 3, or node 2 and 4. For elaborately designed DICE, the bit information can be overwritten only when the logic values in the interleaved nodes change simultaneously.

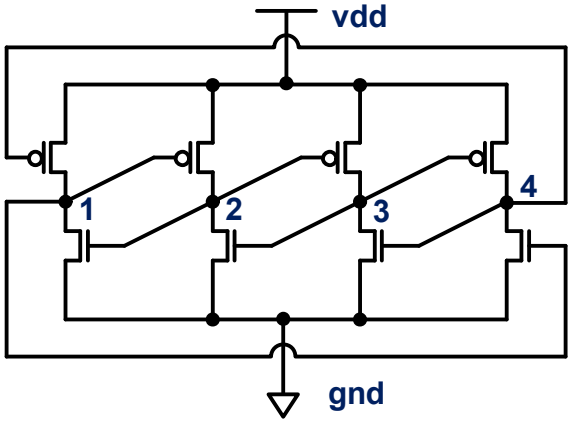

Figure 3. 1: Schematic view of a DICE

Initially, as shown in Figure 3.2, the logic value at node 1 and 3 is 0, while node 2 and node 4 is 1. Transistors A, D, E, H are in the "on" state, while B, C, F, G are in the "off" state. If an energetic particle strikes at the neighboring area of transistor D, and the total generated charge exceeds the threshold, the voltage potential at node 2 will be pulled down. Similar to the conventional storage cell, this can be caused by the collection of electrons at the drain of transistor D, or instantaneous conduction at the channel. Consequently, the state of transistors B and E, which are directly controlled by node 2, could be changed. Voltage level at node 3 will increase and the attainable value is determined by the dimension of PMOS and NMOS transistors together, while node 1 will be floated. The attainable value at node 3 and the threshold voltages V_{TN} and V_{TP}

determine whether transistor D and G will change their states. When transistor G turns to the "off" state, node 4 will be floated. At this time, the discharge may invalidate the entire DICE. For this case, the time constant is related to the fabrication process and layout style. If the transistor G does not change its state, the bit information could be recovered after the transient fades away.

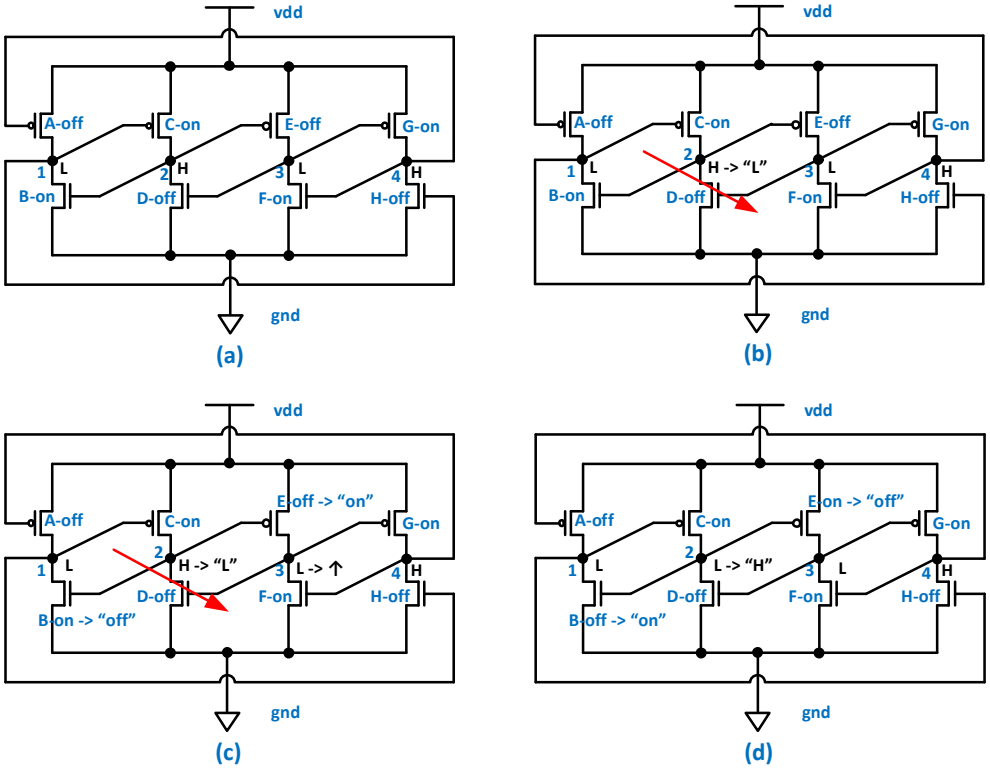

Figure 3. 2: SEU and data recovery in DICE

The potential at node 3 is determined by the pull-up and pull-down transistors together. Normally, either of them should be in the "off" state. However, if they conduct simultaneously, the current will flows through both of them, from Vdd to Gnd. The achievable potential is related to the dimensions (transistor's dimension determines the

equivalent resistance and the drive capability). We term this phenomenon as “conflict” for the convenience of the following analyses.

3.1.2 Guard Gate and SET Mitigation

Guard gate is introduced by Balasubramanian et al. for radiation tolerant designs [16]. As shown in Figure 3.3, it has two inputs and one output. Normally, the logic value of the two inputs should be identical. If they are different from each other, the output node will be floating, and the logic value will sustain its previous one.

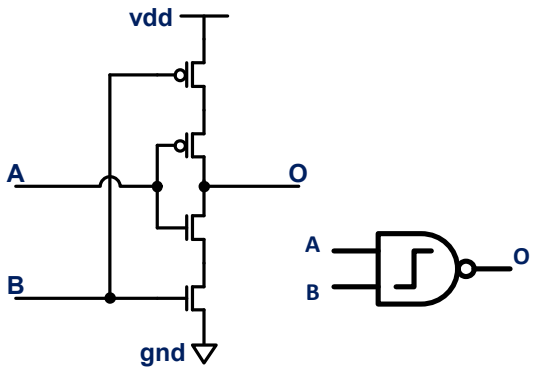

Figure 3. 3: The schematic view and symbol of the guard gate

The gate structure is more tolerant to SETs. Assume both input values are logic “0”, the two PMOS transistors are in the “on” state and the NMOS transistors are in the “off” state. If a SET happens during such a static state, the momentary conductive channel will not lead to the short circuit between the output and ground due to the existence of another NMOS. From this point of view, the guard gate is immune to single node particle strike.

Table 3. 1: The truth table of the guard gate

A	B	O
0	0	1
0	1	hold
1	0	hold
1	1	0

Table 3.1 is the truth table of guard gate. The output value is determined by the input values, not the dimension of transistors.

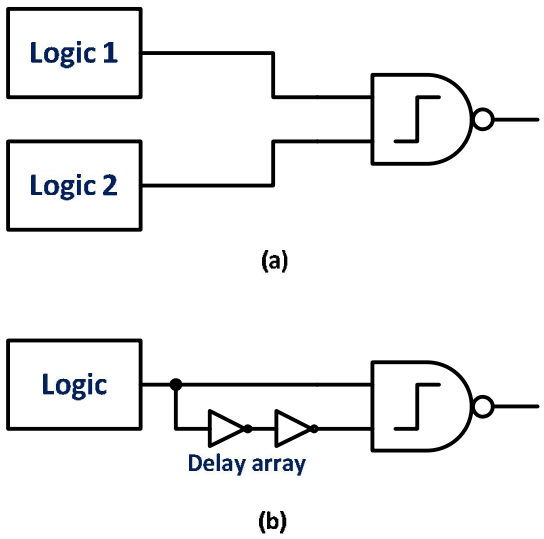

Figure 3. 4: SET mitigation technologies: (a) Dual redundancy (b) delay array

In a dual-redundancy design, the two inputs of the guard gate are driven by two identical circuits, as shown in Figure 3.4(a). The SET in one path can be eliminated. Alternatively, as shown in Figure 3.4(b), a delay unit can be arranged to either input path. A SET with pulse width smaller than the delay will be shielded [16]. For some extreme cases like SETs from the two paths arrive at the same time in circuit (a), or the

pulse wide exceeds the delay array in circuit (b), the guard gate will become invalid. These problems can be settled from using the triple redundancy logic or a greater delay unit.

3.1.3 Guard Gate Based DICE

Taking the advantage of guard gates, the radiation tolerance of the DICE can be further improved. As shown in Figure 3.5, the four inverter-like gates in pre-mentioned DICE are substituted by the guard gates [16]. The newly constructed cell also has four internal storage nodes, and the logic value at each node is determined simultaneously by the neighboring two. Compared to the conventional DICE, there are two transistors between the storage node and the power rail. This property can reduce the upset probability as interpreted in the guard gate. Unlike the original DICE, this structure is totally immune to a single node upset. Take the second branch (the second guard gate from left) for instance. If a SEU happens to its output, which is one input to the first and the third branch, the first and third guard gate will sustain the previous state because their inputs are different. Therefore the other three storage nodes sustain their values for a single node upset. After the energetic particle induced effect fading away, the upset node can be recovered. There is no “conflict” risk for this case. So the function is independent of the dimension and technology used.

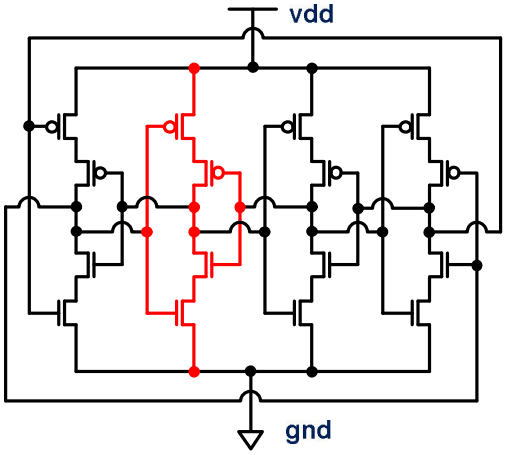

Figure 3. 5: DICE based on guard gate

3.2 Realization of Clock Control

Registers are developed based on the storage cells introduced in the last section. This section will present several clock control solutions and discuss their advantages and disadvantages.

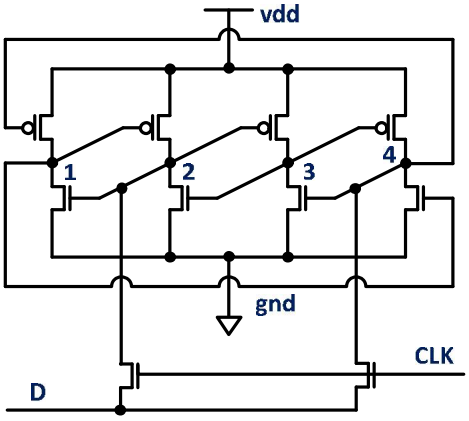

Figure 3. 6: DICE based latch with NMOS access transistor

One pair of NMOS transistor can be used as the access transistors, as shown in Figure 3.6. It is a simple way to realize a DICE based latch [14]. However, the sizes of transistors should be carefully selected. Take node 2 for example, assume its bit information is “0” and the NMOS pull-down transistor is in the “on” state. If logic “1” is going to be written into this node, the access transistor must have stronger drive capability to pull up the voltage potential. Moreover, in a master-slave register, the master latch should have a stronger drive capability than that of the slave one to guarantee the data flow to the correct direction.

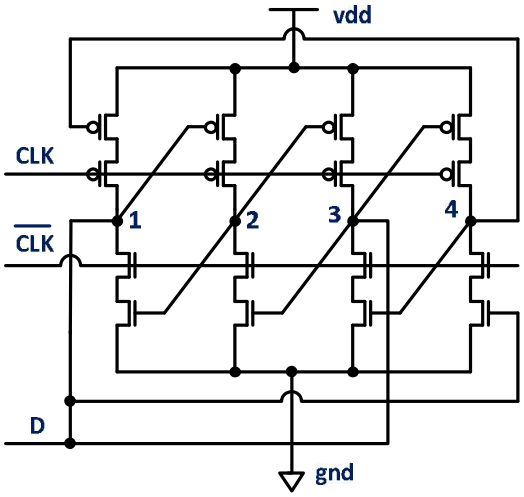

Figure 3. 7: DICE with clock embedded inside

Another solution is to implant the clock control transistors inside the cell. Similar to the C^2MOS (clocked-CMOS), one NMOS transistor and one PMOS transistor are embedded next to each storage node, as depicted in Figure 3.7. In writing cycle, the transistors controlled by clock signals are in the “off” state, and the output nodes are floating. While in the reading cycle, clock controlled transistors are in the “on” state,

and the circuit works simply as a DICE. In this solution, the writing of data is efficient because the outputs are insulated from power rails. On the other hand, the floating nodes make the circuit susceptible to the direct charge deposition and charge collection. This approach conflicts with the original intention of the DICE. Moreover, simulation results showed that a severe cross-talking exists between the outputs and the clock signals, especially at high frequencies.

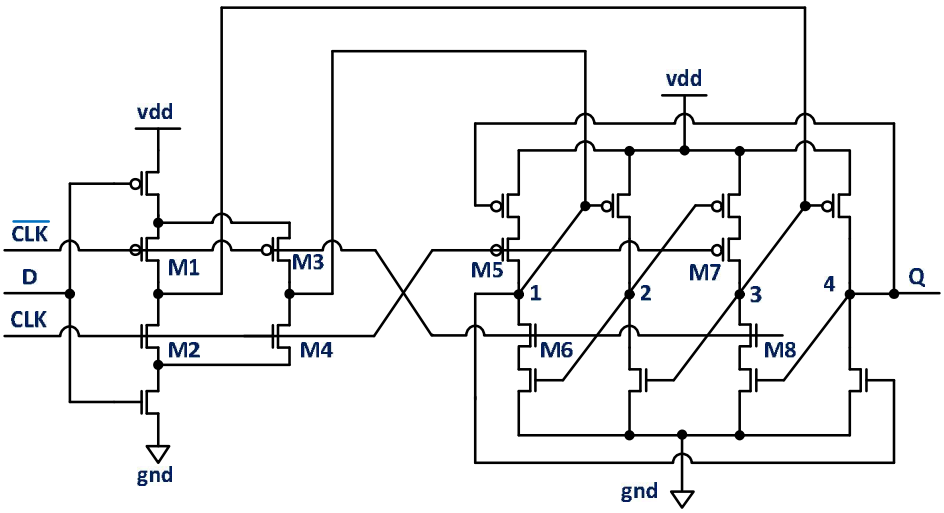

Figure 3. 8: DICE based latch

To overcome the aforementioned problems, the clock control transistors near the output nodes are moved out of the cell, as depicted in Figure 3.8. This circuit works as a latch. When the clock signal is high, transistors M1 ~ M4 are in the “on” state, while M5 ~ M8 are in the “off” state. The data is written into the storage cell through node 1 and 3. During this cycle, any logic value transition from the input can be directly reflected at the output. Node 1 and 3 are connected to the power either through M1, M3 or M2, M4. The writing is highly efficient and no conflict exists. When the clock signal is low,

transistors M1 ~ M4 are in the “off” state, while M5 ~ M6 are in the “on” state. The left part of the latch works as a traditional DICE and the logic value transition from the input does not affect the output. All storage nodes are connected to the power rails either through M5, M7 or M6, M8. The input gate (the left part) can also be substituted by a guard gate so that the latch is capable of eliminating the SETs from the input.

To sum up, no floating node exists for the whole clock cycle, and no conflict phenomenon exists. The load to the preceding gate and the propagation delay are minimized, the power consumption is optimized. This type of latch provides a good and flexible solution to the radiation-tolerant register, which can be implemented from cascading latches, with a reversed clock signal, as shown in Figure 3.9.

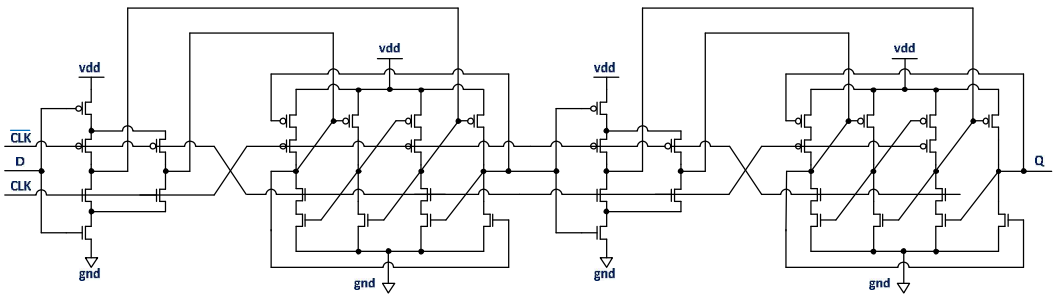

Figure 3. 9: DICE based master-slave register

3.3 Single Event Resistant Topology (SERT) Based Register

As shown in Figure 3.10, a half transition NAND gate can be realized from removing one PMOS transistor from the guard gate. It has a similar logic function to the guard gate, except that the output responds to a “high to low” transition at the input A. The half transition NAND gate is also free of conflict.

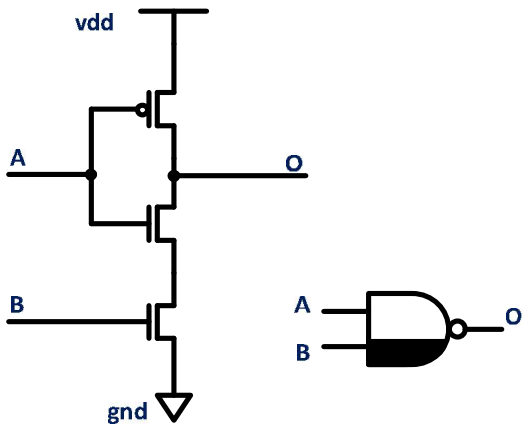

Figure 3. 10: The half transition NAND gate

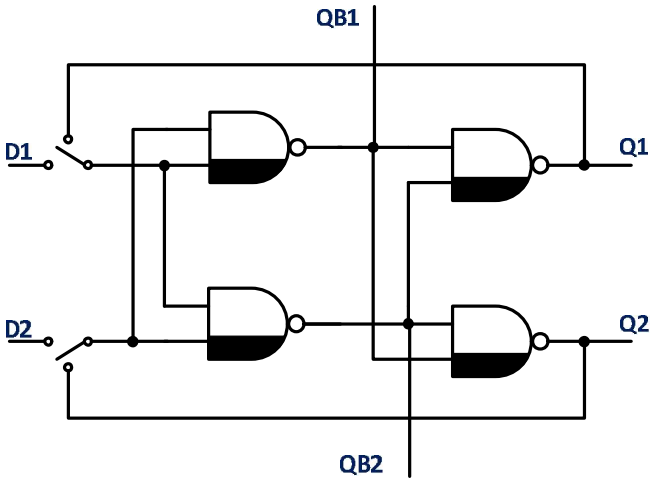

Figure 3. 11: The schematic view of SERT Latch

The SERT latch shown in Figure 3.11 was developed by Gambles in Avionic Systems Division, NASA Johnson Space Center [17]. Similar to the guard gate based DICE, the storage cell is realized from four half transition NAND gates. The clock control is implemented by transmission gates instead of the C^2MOS logic. The outputs will not be updated unless two inputs agree. This latch is capable of eliminating SETs from the input. One approach is to apply it in dual redundancy circuits. Another approach is to

leave a delay array at one of the inputs. The latch is also free of conflict. A register can be built from the SERT latch, as shown in Figure 3.12 [17].

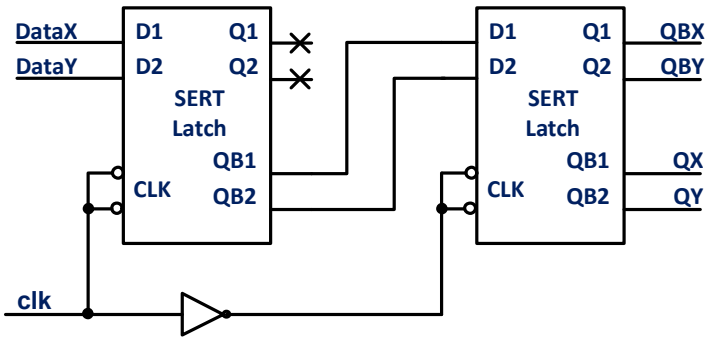

Figure 3. 12: SERT based register

3.4 A Standard Cell and Comparison of Electrical Performances

The register (FD1QSVTX1) shown in Figure 3.13 is designed for general usages, not for space applications. It has been adopted in our experiment as a reference so that we can make general comparisons in both electrical performances and radiation tolerances.

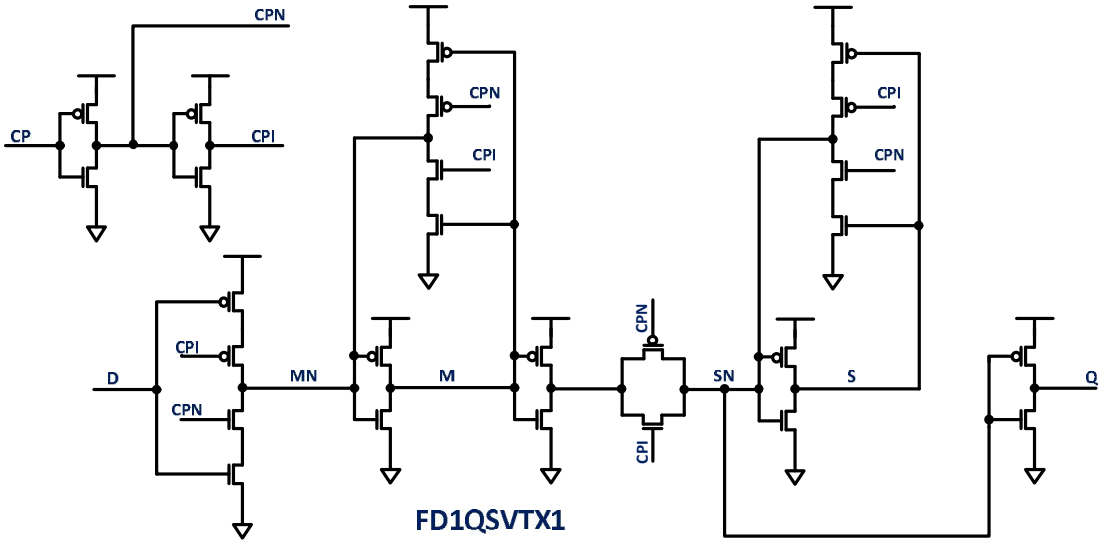

Figure 3. 13: The schematic view of a register from STM CMOS 90 nm digital library

Table 3. 2: Comparison of electrical performances

Register Type	Transistor amount	Area (um^2)	Propagation Delay (s)	Power @ 500MHz (W)
FD1QSVTX1	26	14.9	4.77E-11	4.73E-6
DICE	40	49.9	6.08E-11	4.35E-6
Guard gate DICE	56	55.5	7.99E-11	5.26E-6
SERT	44	45.9	6.46E-11	4.73E-6

Table 3.2 lists the simulation results of propagation delays and power consumption in room temperature (300K). The Simulations are done with Cadence Spectre. FD1QSVTX1 is the one from STM's digital library. For the radiation tolerant registers, their speed is degraded because the signal needs to propagate more gates and the internal load is relatively large. However, the power consumption differences are not significant.

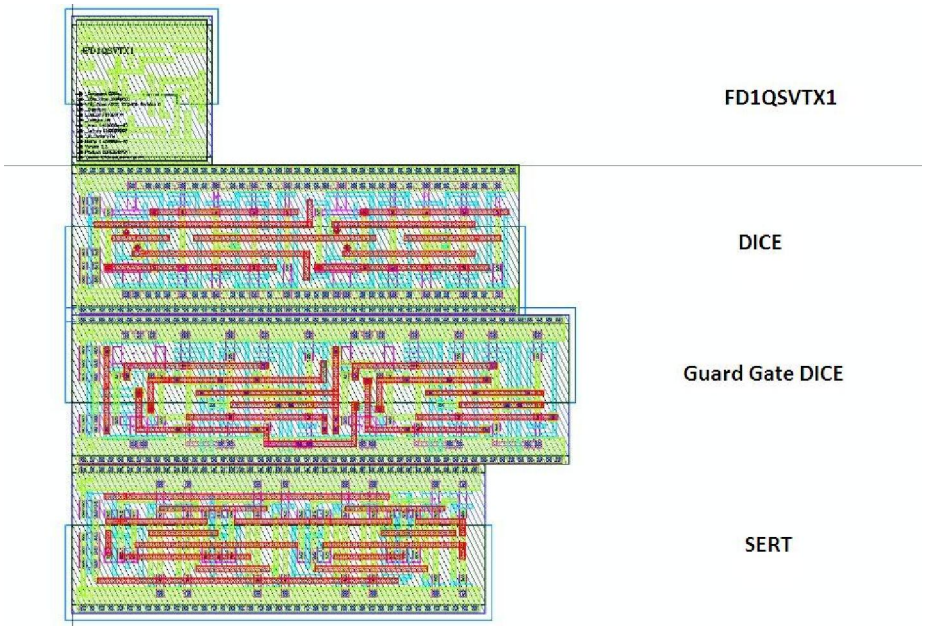

Figure 3. 14: The layout view of registers

Figure 3.14 compares the registers' layout sizes. The standard register occupies the smallest area, whereas the radiation-tolerant designs consume 3~4 times larger areas. Compared with the DICE, area increment for the guard gate DICE register is not as significant as the transistor amount. The comparison gives a general idea on the area tradeoff for our solutions. The radiation tolerance is also related to the layout style and integration density. Increasing the area can weaken the multiple node charge collection and single event latch up effects, and hence, improve the reliability.

3.5 Built-in Test Structures

The built-in test circuits are designed for counting upset rates of the target registers, thus, to evaluate their radiation performances. They are expected to work under various radiation intensities and clock rates (from few tens of MHz to 100MHz), and should

reliably report the SEUs in target registers. In this section, two built-in test structures are discussed.

3.5.1 Circuit for Radiation Effects Self Test (CREST)

The idea of CREST originates from Paul Marshall's work [26]. As depicted in Figure 3.15, the pseudo-random numeric (PRN) block generates periodic random signals to the register chains. The output vector repeats every 2^n-1 clock cycles. In our case, n equals to 7. There are seven registers in the PRN block, as depicted in Figure 3.16. We applied 127 registers for each chain. In the CREST, the outputs of PRN block and register chains are connected to the upset detection circuits. Normally, their patterns should be identical. Once exposed to the radiation, the bit information might be changed. This kind of error will be shifted out of the chain and be detected.

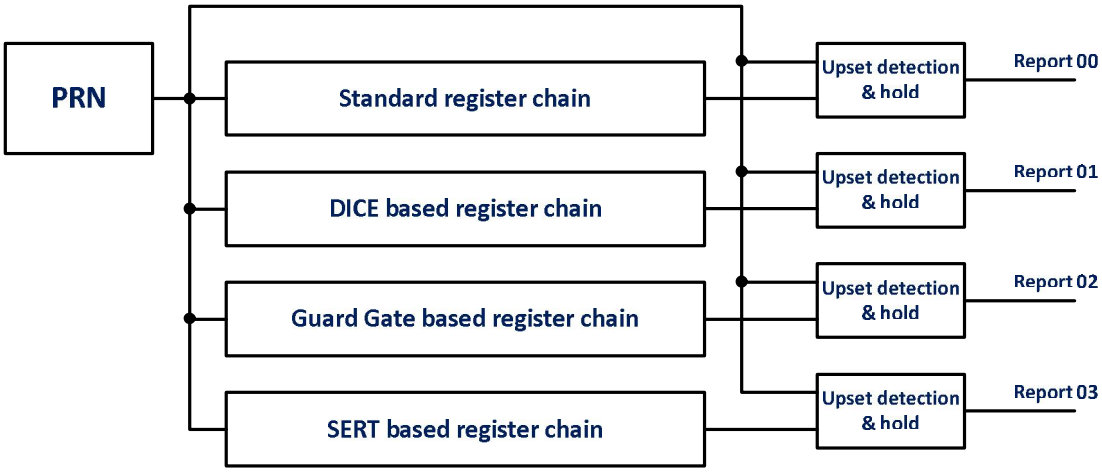

Figure 3. 15: The block diagram of CREST

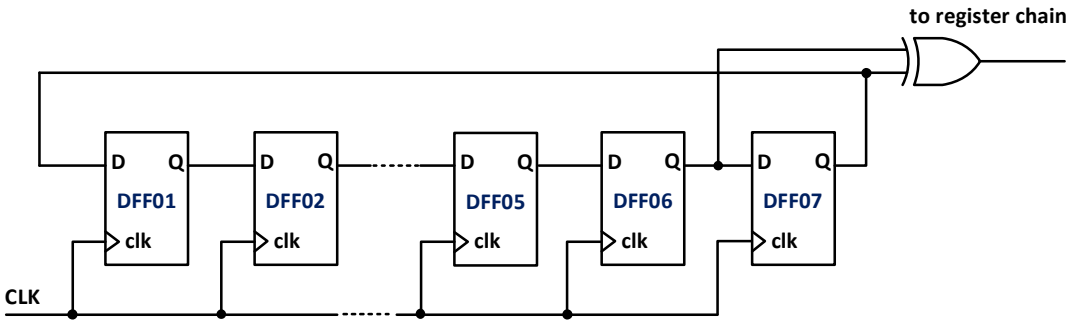

Figure 3. 16: The schematic view of the pseudo-random numeric (PRN) block

CREST is a flat structure, and the detection circuit executes the comparison 1-bit per clock cycle. Even if the particle strikes at near-zero grazing angle and SEUs happen at multiple nodes simultaneously (MBU), CREST can reliably report the upset bit information.

However, some of the SEUs probably come from the PRN block and upset detection circuits. Take the PRN block for example, the output is logic “1” at a certain clock cycle. After one period (127 cycles), the value should also be “1”. If a SEU happens at this time, the bit information changes to “0”. The detection circuit compares the “1” from the register chain to the “0” from the PRN block. Because these two values are not identical, one error will be reported. However, the PRN block and upset detection circuits consume very small area in the overall layout, as shown in Figure 3.17. Therefore, the pre-mentioned probability is not significant.

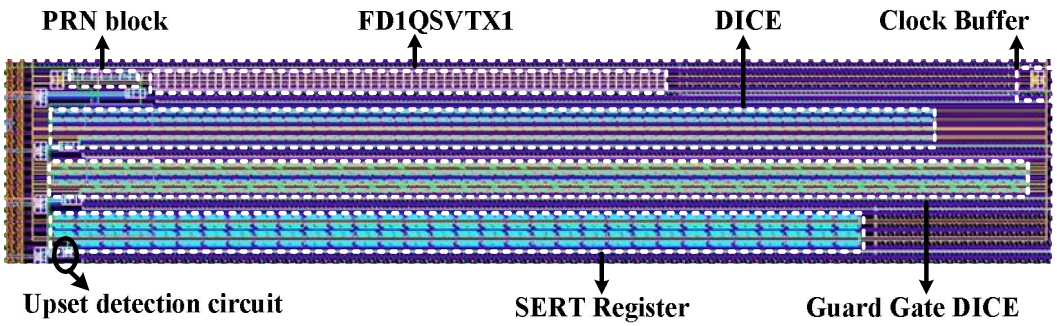

Figure 3. 17: The layout view of the CREST

3.5.2 SEU Detection Circuits (SEUDC)

The SEUDC is developed by Shuler with Avionic Systems Division, NASA Johnson Space Center [26]. As depicted in Figure 3.18, groups of comparators work independently. Their outputs are connected to the upset detection circuit through OR gates. Different from the CREST, this is a hierarchical structure. The SEU in each comparator propagates hierarchically to the top. For the particle traveling at a grazing incidence angle, a single event MBU could happen. These upsets pass through the OR gates simultaneously, however, only one upset will be detected. Therefore, the results can not accurately report single event MBUs.

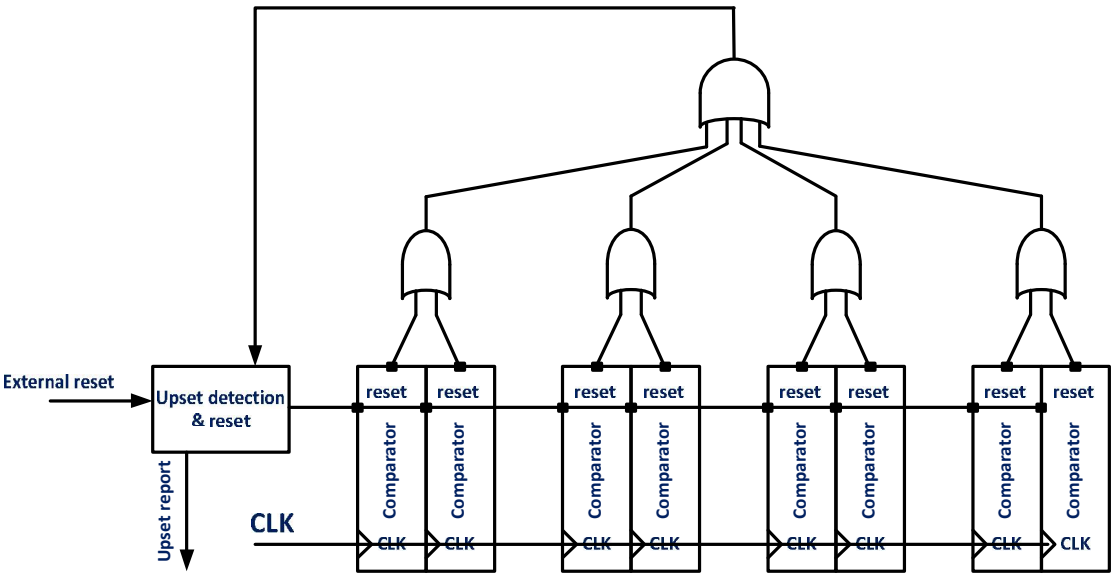

Figure 3. 18: The block diagram of a SEU detection circuit

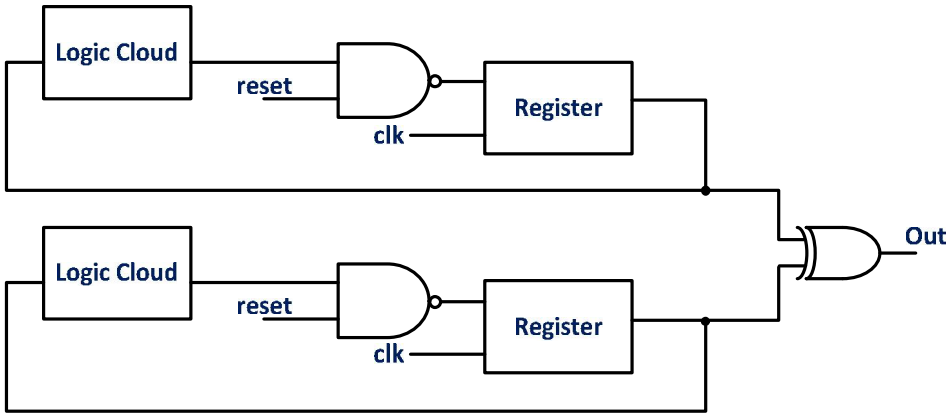

Figure 3. 19: The block diagram of the comparator in SEU detection circuit

As shown in Figure 3.19, the comparator contains two identical sub-circuits. In a sub-circuit, the Logic Cloud (as depicted in Figure 3.20) is a unit function combinational logic circuit, which provides a fixed value to the register unless the input changes. Normally registers in the two sub-circuits have the same bit information. Their outputs

are connected to a XOR gate. The energetic particle can lead to a SEU to either of them and make the outputs different. For this case, the output of comparator changes from logic “0” to logic “1”. SEUs can also happen to the two registers at the same clock cycle, but the probability is very low. Nevertheless, it has difficulty in detecting single event MBU as mentioned in the last paragraph.

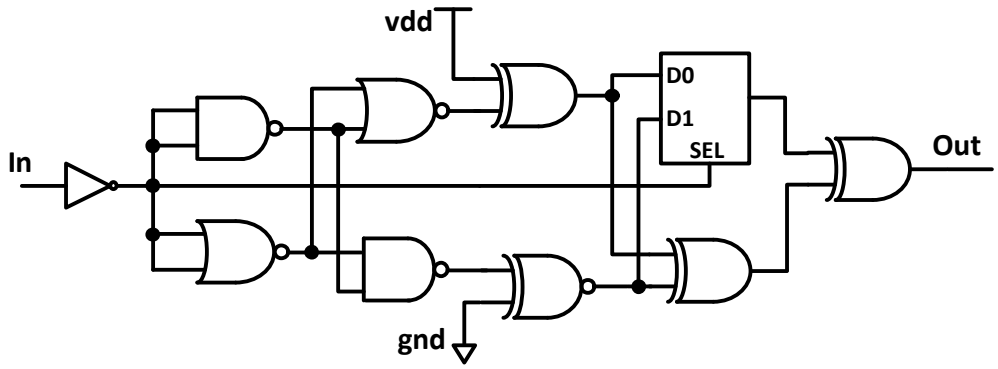

Figure 3. 20: The schematic view of the Logic Cloud

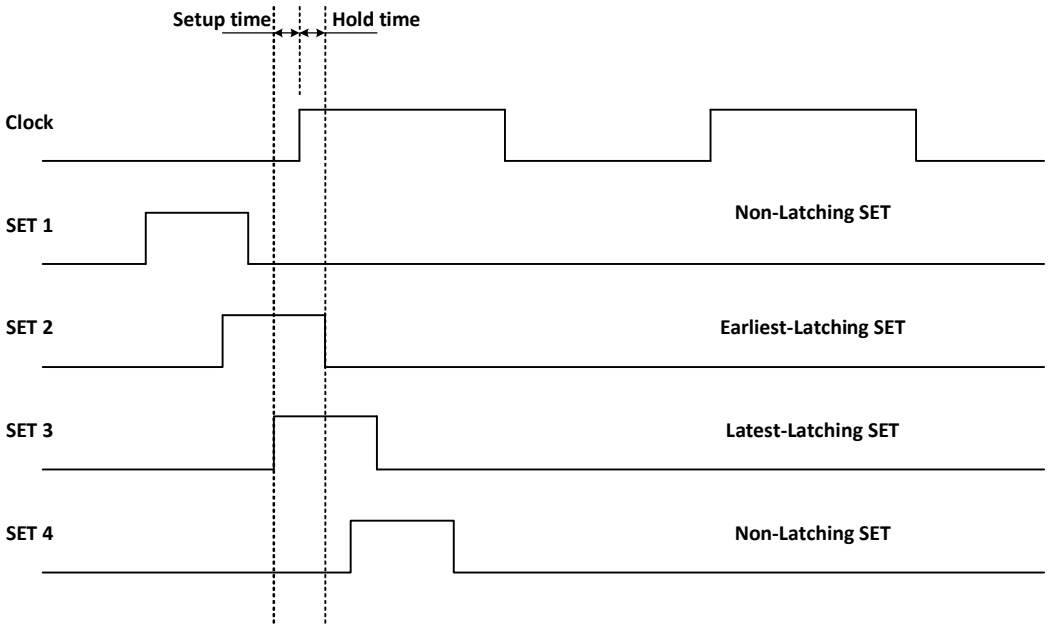

Figure 3. 21: SETs from register’s inputs and setup/hold time

SEUs are not the only potential hazard to registers. SETs from the inputs could be captured if the transient pulse satisfies the setup time and hold time, as shown in Figure 3.21. For the SET with a certain pulse width, the higher working frequency leads to the higher probability of being captured. The Logic Cloud can generate SETs when exposed to the radiation. So the SEU detection circuit is capable of evaluating the error rate induced by input SETs. This function is useful for dual-rail designs (like the SERT register). It also helps to establish relationships between the working frequencies and the SEU rates at different radiation intensities.

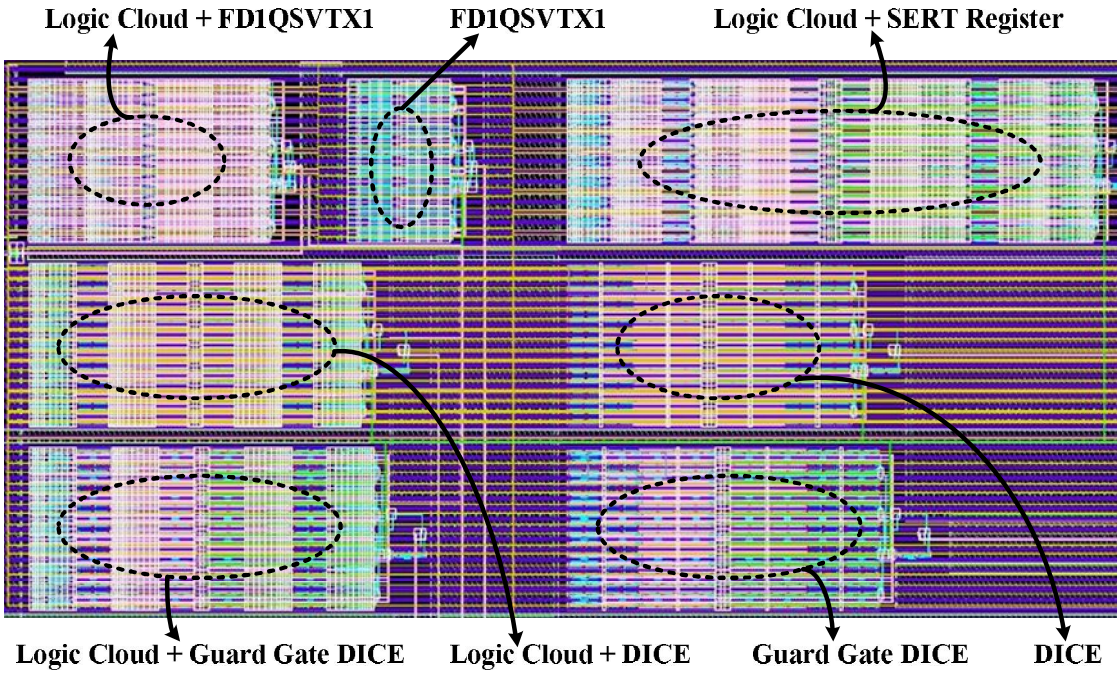

Figure 3. 22: The layout view of SEU detection circuits

The four types of registers are embedded into the SEU detection circuits. In addition, we would like to evaluate only the SEU rates and neglect the SET factor, so as to compare the results with CREST. Three more groups are realized for this purpose. In

these circuits, the Logic Clouds are removed. In this way, the comparators only detect the SEUs in the registers. The SERT register is not reused in the SEU evaluation because its storage cell also belongs to the dual interlocked design, similarly to the DICE. As shown in Figure 3.22, seven groups of SEU detection circuit have been implemented.

3.6 Pulse Width Measurement Circuit

The shrinking transistor size makes the digital circuits more and more susceptible to SETs. Besides the clock frequency, the error rate has a strong relationship with the SET pulse width. Wider pulses have a greater probability of being captured by the registers at the edge of the clock [28] [29]. Therefore, it is important to characterize the width of transient pulses for advanced CMOS technologies.

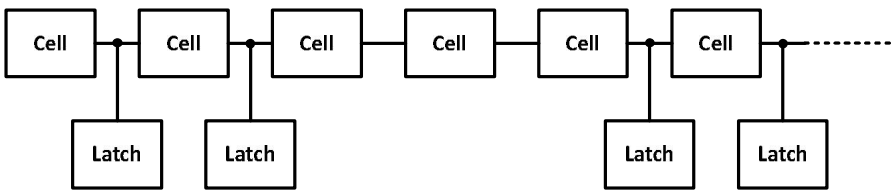

Figure 3. 23: Periodic distribution of the pulse capturing latches

Researchers have investigated the SET pulse width measurement approaches. In one solution, the transient pulses are directly measured with high speed oscilloscopes [30]. The stray capacitances of the measurement system are the main problems, which can distort SET pulses. Another solution is to use a chain of identical cells monitored by latches to characterize the pulse width [31], as depicted in Figure 3.23. In this method,

the latches are clocked continuously to monitor the state of the cells. However, due to the limitation of clock frequency, the circuit cannot reliably capture a SET pulse.

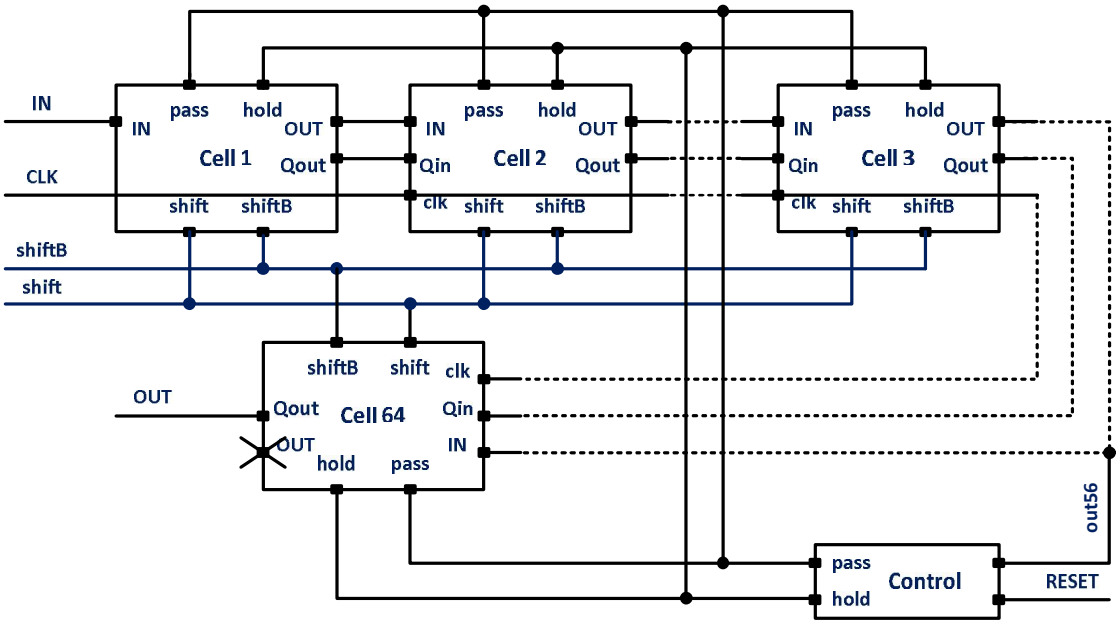

Figure 3. 24: Block diagram of pulse width measurement circuit

Our work is based on the solution presented by Narasimham et al. [32]. The circuit contains 64 measurement cells, which are connected in series. As depicted in Figure 3.24, the entire circuit works as a ruler and the cells compose the scale. When the SET voltage pulses are propagating through the circuit, their widths can be measured. As shown in Figure 3.25, each measurement cell contains two parts. The part in dashed line is used to measure the pulse width, and the rest is a register designed for reading out the results. The propagation delay between “IN” and “OUT” in each cell determines the minimum resolution. Figure 3.25 (a) and (b) depict the first and the following stages, respectively.

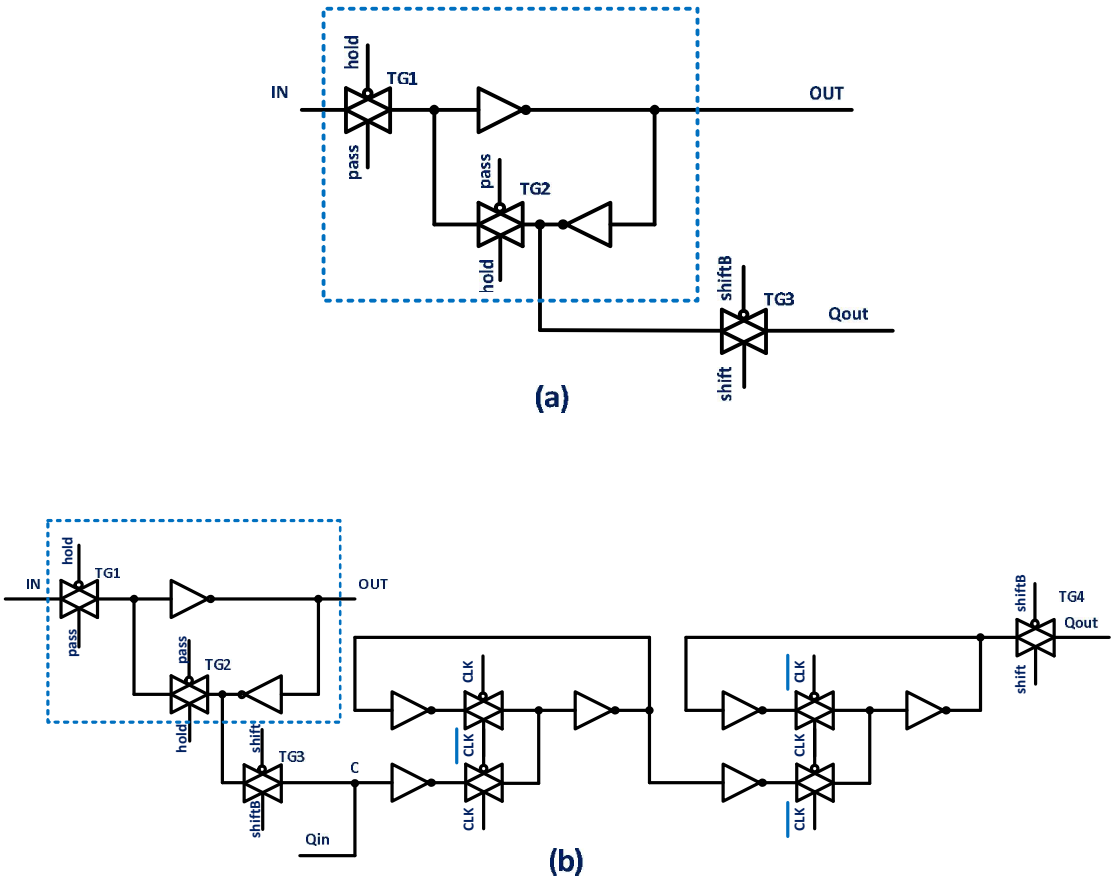

Figure 3. 25: The schematic view of the measurement cells.

When the circuit is in the "pass" state, the transmission gates TG1 and TG 3 are open, TG2 and TG4 are blocked. In this case, the SET pulse can propagate through the measurement chain. At this moment, the transient value goes through TG3, reaches node C, and be stored in the register. Once a SET pulse propagates into the circuit and reaches the output of the 56th cell, its falling edge will trigger the control circuit, as depicted in Figure 3.26. Consequently, the "pass" and "hold" signals will change, and the measurement circuit enters the hold state. In words, the transient pulse will stop propagating, and be captured by the circuit. In this case, TG1 and TG3 are blocked, TG2

and TG4 are open. The last moment value is stored in the register before TG3 is turned off. Once the “hold” signal is activated, the “shift” signal can be applied to read out the result. Because the propagation delay of the control circuit should also be taken into consideration, eight more cells are placed after the 56th. Moreover, the control circuit drives sixty-four measurement cells. Two groups of buffers are applied to improve the drive capability.

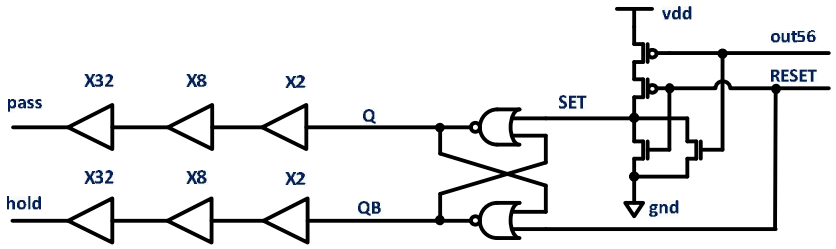

Figure 3. 26: The schematic view of the control circuit

Table 3.3 lists the four states of the circuit. The output value of the 56th cell should be logic “1” in normal condition. To initialize the circuit, a short reset pulse is applied. In the “pass” state, the reset signal is deactivated, and the SR-latch keeps its previous state. Once, the output of the 56th cell turns to 0, the “hold” signal changes to logic “1” and the pulse width measurement circuit enters the “hold” state. At this time, the bit information of each cell is stored in the register and the result is ready for reading out. Sufficient reading period must be provided (at least 64 clock cycles) to guarantee the integrality of the result. When the reading operation is finished, a positive pulse could be applied to reset the circuit, preparing for another round of measurement.

Table 3. 3: The truth table for the SET pulse width measurement circuit

Signal	Out56	Reset	Set	Pass	Hold
Initialization	1	1	0	1	0
Pass State	1	0	0	1	0
Hold State	0	0	1	0	1
Reset	0	1	0	1	0

The circuit is implemented with STM CMOS90nm process. Dimension of the devices are optimized to minimize the delay and hence improve the resolution. Simulations showed the propagation delay of each cell is about 45.3 ps which is 3.4 times of a single inverter (13.3 ps) due to the extra delay introduced by the transmission gate. A SET pulse ranging from 90.6 ps to 2.53 ns can be efficiently measured. The resolution of the result is one cell's delay.

Figure 3.27 shows the simulation result from Cadence Spectre. The waveform on the top indicates that a 936 ps pulse is injected at 20 ns transient. After 56 cells' delay, the pulse reaches the 56^{th} cell and the output begins to change. The waveform at the bottom depicts the data from the register chain. The labels mark the first and the last abnormal cells whose outputs are affected by the injected pulse. For this case, twenty cells change their outputs. This means the duration of transient pulse equals to 20 cells' delay. The SET pulse width can be calculated from multiplying the unit cell delay by the cell amount. That is 45.3*20=906ps $\pm$45.3ps. The manually injected pulse (936ps) falls into this range.

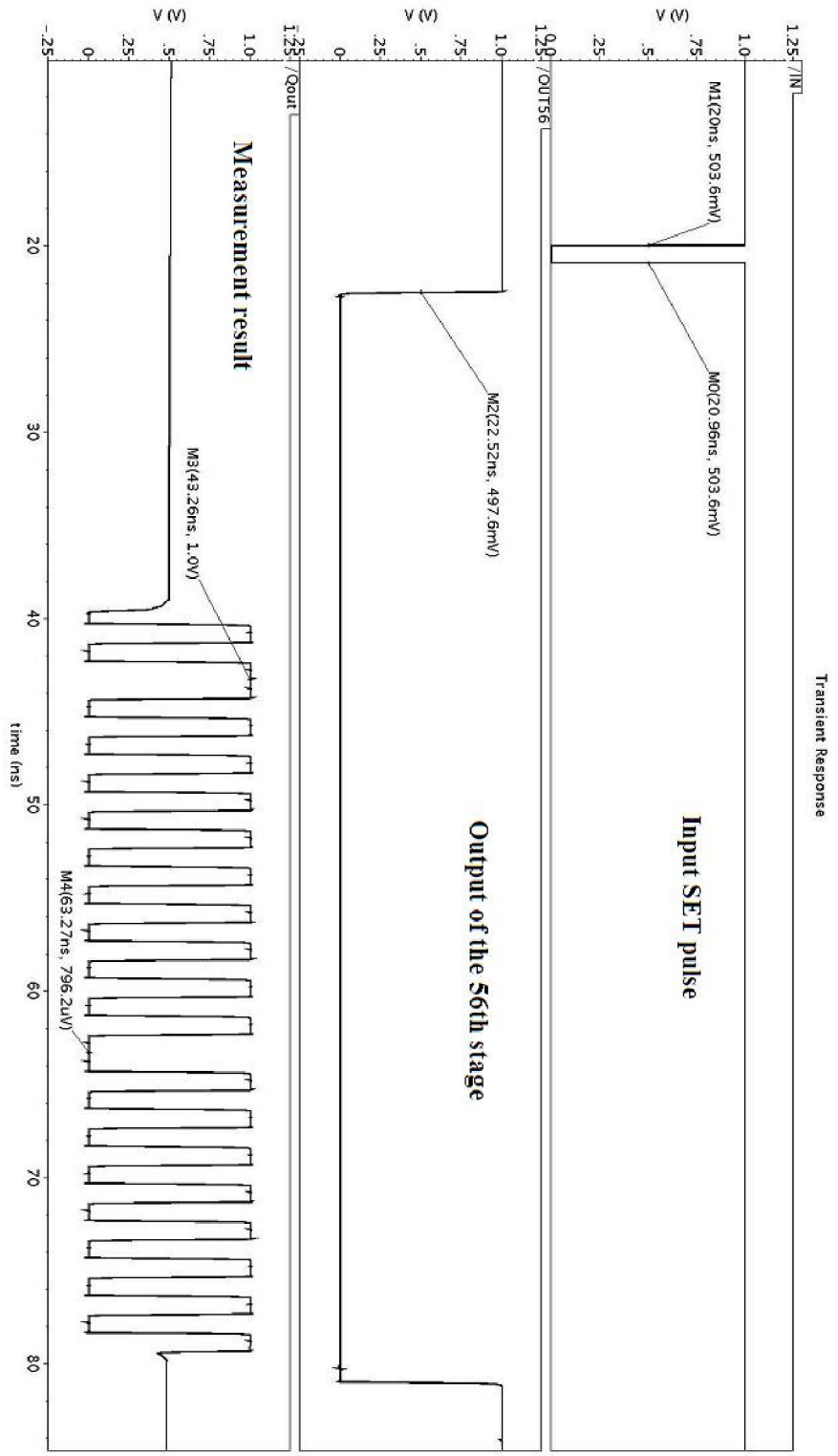

Figure 3. 27: The simulation result from the pulse width measurement circuit

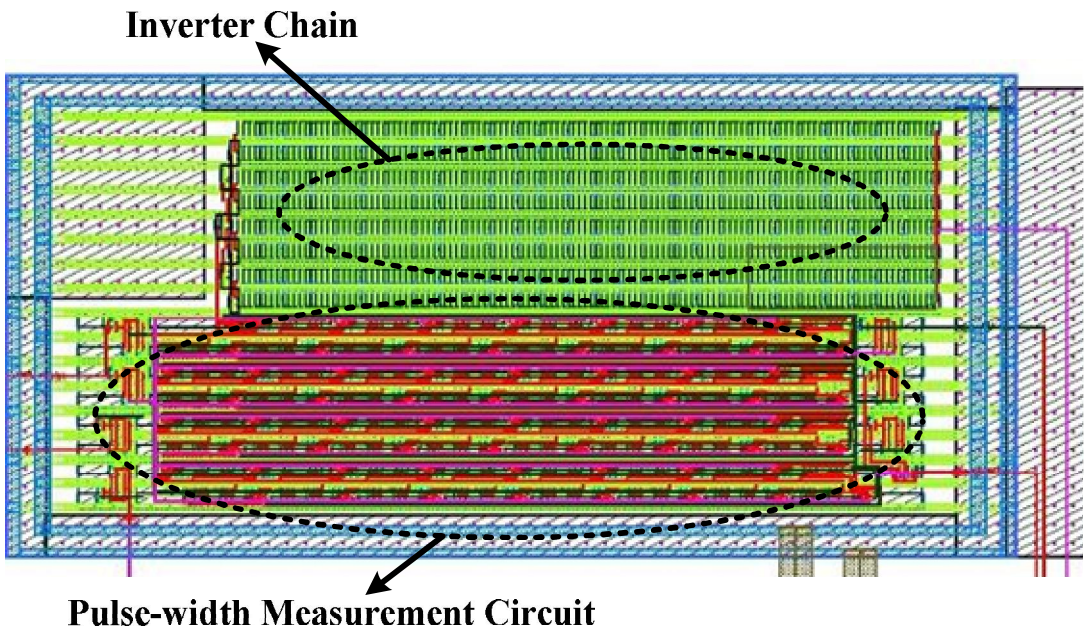

Figure 3. 28: Layout view of the pulse width measurement circuit and inverter chain

Figure 3.28 is the layout view of the pulse width measurement circuit. The input is connected to an inverter chain, which is designed for generating SETs during the laser or energetic particle test.

3.7 Summary

In this chapter, we have introduced radiation-tolerant storage cells in Section 3.1. The DICE technology is introduced first. According to the analyses, an elaborately designed DICE can recover from a single node upset. Then the guard gate technology and the DICE built from guard gates are introduced. This cell is more tolerant than the original DICE, and there is no conflict phenomenon. At the same time, two SETs mitigation technologies are also discussed. In Section 3.2, we investigate the clock issues. An

optimal solution has been applied to realize the DICE and the guard gate DICE based registers. In this approach, there is no floating node during the whole clock cycle and the writing operation is efficient. In Section 3.3, the SERT technology and SERT based register are introduced. This register is built from half transition NAND gates, which are simplified from the guard gates. The clock control is implemented by transmission gates. In Section 3.4, we compare the transistor amounts, areas, propagation delays and power consumptions of the radiation-tolerant registers to the unhardened one, which is from STM CMOS90nm digital library. Our designs consume 3~4 times larger areas. The propagation delays are also larger compared to the standard cell.

To evaluate the SEU rates of the four types of registers. Two built-in testing structures are implemented. We have discussed them in Section 3.5. The flat structure (the CREST) can detect only one bit information per clock cycle, whereas it is useful for the single event MBU detection. The hierarchical structure (the SEUDC) executes groups of comparison simultaneously. Besides the SEUs occurring inside of the registers, it can also be used to evaluate SET-tolerant performance of combinational logic circuits. However, the hierarchical structure is not capable of detecting single event MBU.

The pulse width measurement circuit is implemented to measure the SET pulse widths. In Section 3.6, we have implemented a 64-cell measurement circuit. According to the simulation results from Cadence Spectre, SET pulses ranging from 90.6 ps to 2 ns can be captured and measured. The resolution is one cell's delay. That is 45.3 ps for our case.

Figure 3.29 depicts the overall layout of the test chip. The chip's dimensions are 1 mm × 1 mm including the I/O ring. It contains the radiation-tolerant registers, two types of the built-in test structures and the pulse width measurement circuit. The translator ring inside the I/O ring translates voltages between 1V (the core) and 2.5V (I/O).

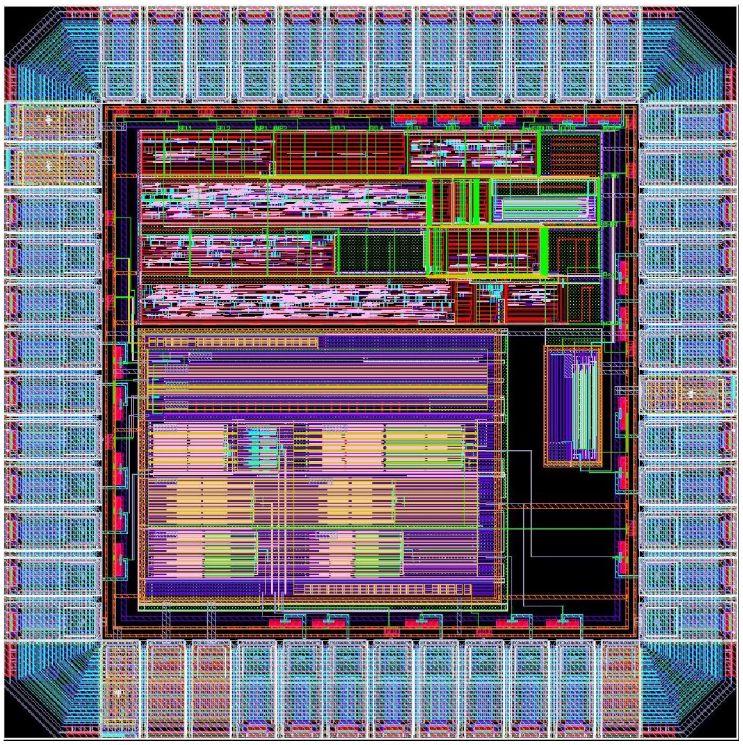

Figure 3. 29: The overall layout of the test chip

Chapter 4

Test Bench Design

This chapter introduces the details of printed circuit board (PCB) design and test methodology. XILINX Spartan-3 Starter Kit Board is used to carry out the test.

4.1 I/O Distribution and function specification

Figure 4.1 shows chip's I/O. For global signals, VDDIOCOs are 2.5V power supplies to both I/O ring and voltage translators. VSSIOCOs are ground connections to both I/O ring and the core. In this design, PPLs are shorted with VSSIOCOs. PPXs are 1.0V power supplies to the core.

As mentioned in chapter 3, four register chains are developed in CREST. N7 is a reserved I/O for providing test vectors to the FD1QSVTX1 register chain. In the energetic particle test, this I/O should be grounded. Considering the SEU rate from standard cell register chain might be very high, the corresponding upset detection and hold circuit is controlled by an individual reset signal, which is C_RESET_00. While, C_REST_01 is the reset signal to the radiation-tolerant register chains. They are both active-low signals. REPORT_00, REPORT_01, REPORT_02 and REPORT_03 are the outputs of FD1QSVTX1 chain, DICE chain, guard gate DICE chain, and SERT chain, respectively. Initially, their logic value is 1.

During the energetic particle test, a reset signal should be applied to each upset detection and hold circuit to initialize them. XILINX Spartan-3 assists to count the error rate from each register chain. Every time a SEU is generated in the chain, the corresponding output is locked to sustain logic 1 until FPGA senses the error report and feeds back a reset signal.

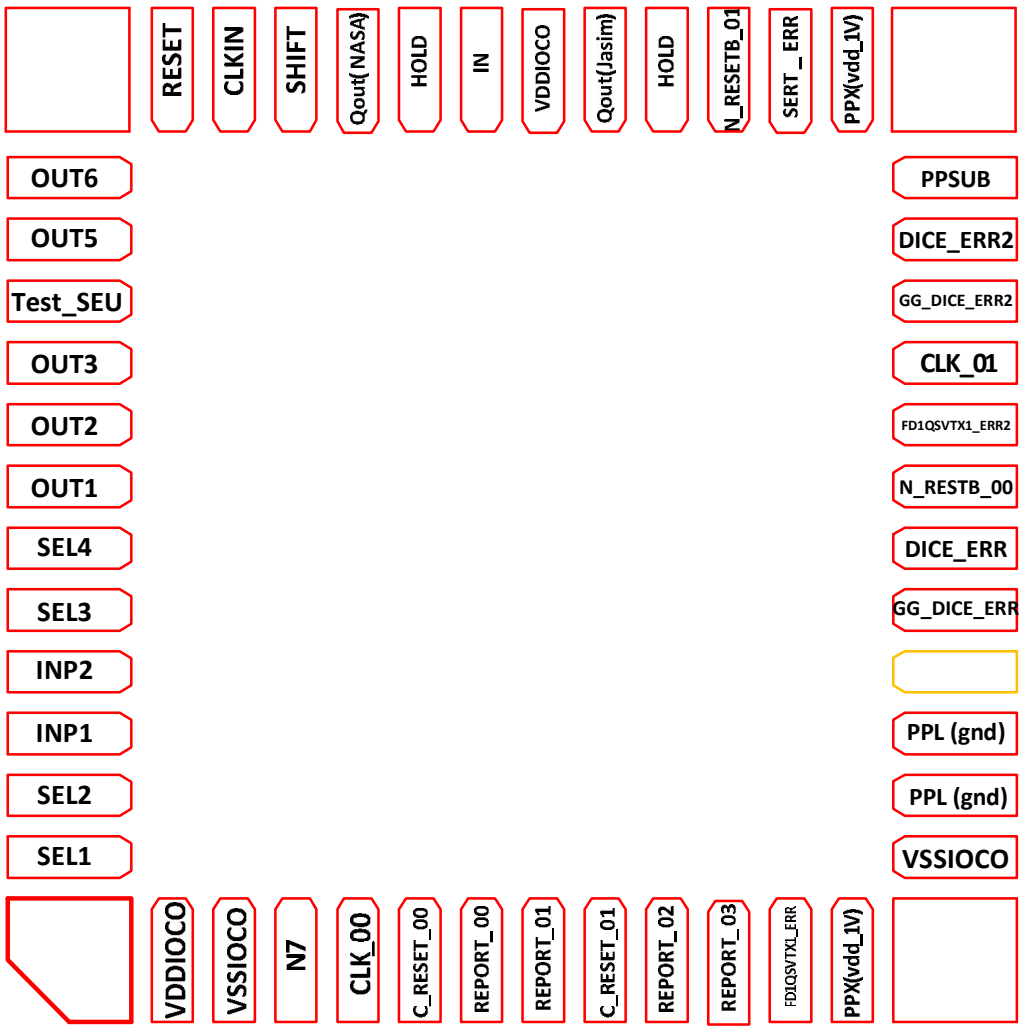

Figure 4. 1: I/O distribution

For the SEUDCs, FD1QSVTX1_ERR, DICE_ERR, GG_DICE_ERR and SERT_ERR are output signals from the regular designs. Their comparators are built with registers and Logic Clouds. FD1QSVTX1_ERR2, DICE_ERR2 and GG_DICE_ERR2 are output signals from the modified ones. The Logic Clouds in their comparators are substituted by corresponding registers. N_RESETB_00 is the reset signal to the standard register. N_RESETB_01 is reset signal to the radiation-tolerant ones. They are both active-low signals.

For the pulse width measurement circuit, the inverter chain requires a fixed input. In our case, IN is connected to Vdd to make the input of pulse width measurement circuit logic "1". Therefore, the output of the 56^{th} cell is also logic "1". RESET and SHIFT are active-low signals. The HOLD signal is used for observing the internal state. Normally, its value should be logic "0". Once it changes to logic "1", the SHIFT signal can be applied to read out the result through Qout. It's an active-high signal. CLKIN provides clock for the reading operation.

4.2 Test Board specification

To evaluate the radiation tolerances under different supply voltages, the test board supplies tunable voltages to the chip. The power generation circuits contain adjustable regulators and 100 position digital potentiometers [33][34][35], as depicted in Figure 4.2 and Figure 4.3. LM385 zener diodes limit the maximum voltage so as to protect the chip from burning out [36][37].

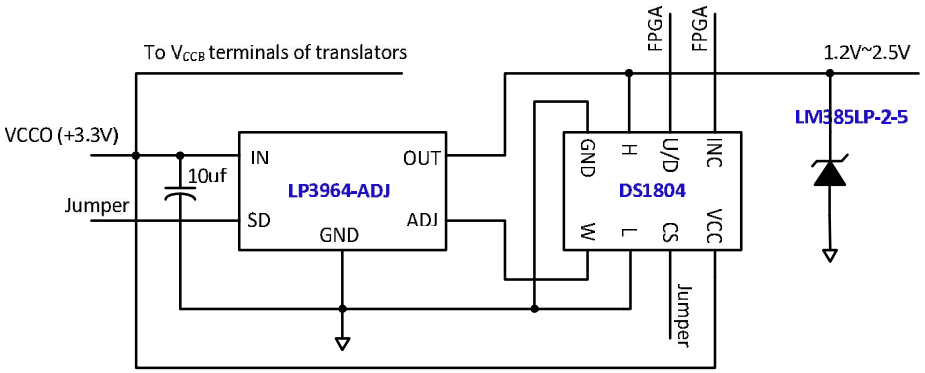

Figure 4. 2: 1.2V~2.5V power generation circuit

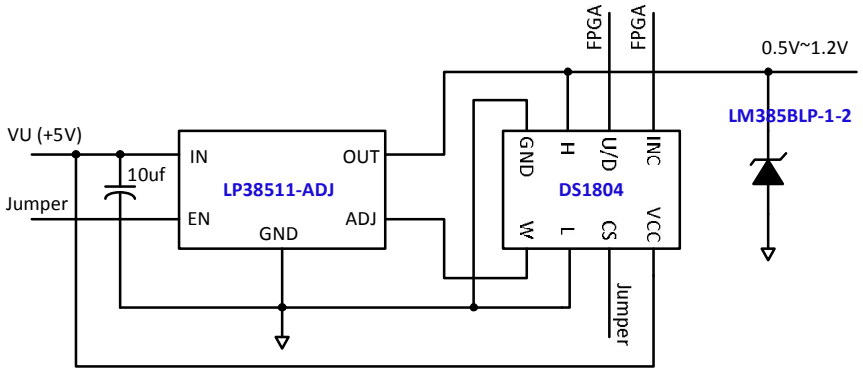

Figure 4. 3: 0.5V~1.2V power generation circuit

Figure 4.4 shows the test board. There are eight jumpers on the top. From left to right, they are connected to N7, SEL1, SEL2, INP1, INP2, SEL3, SEL4 and IN of the chip. Four jumpers lie on the left. From top to down, they control CS1V2 (CS signal in 0.5V~1.2V power generation circuit), EN (enable signal for LP3851-ADJ), CS2V5 (CS signal in 1.2V~2.5V power generation circuit) and SD (enable signal for LP3964-ADJ). Because these signals are fixed during energetic particle test, they are controlled by the jumpers instead of the FPGA. The 40-pin interface on the bottom is connected to the A2

connector of FPGA board. Decoupling capacitors are applied between power supplies. The ground plane on both sides helps to improve signal integrity.

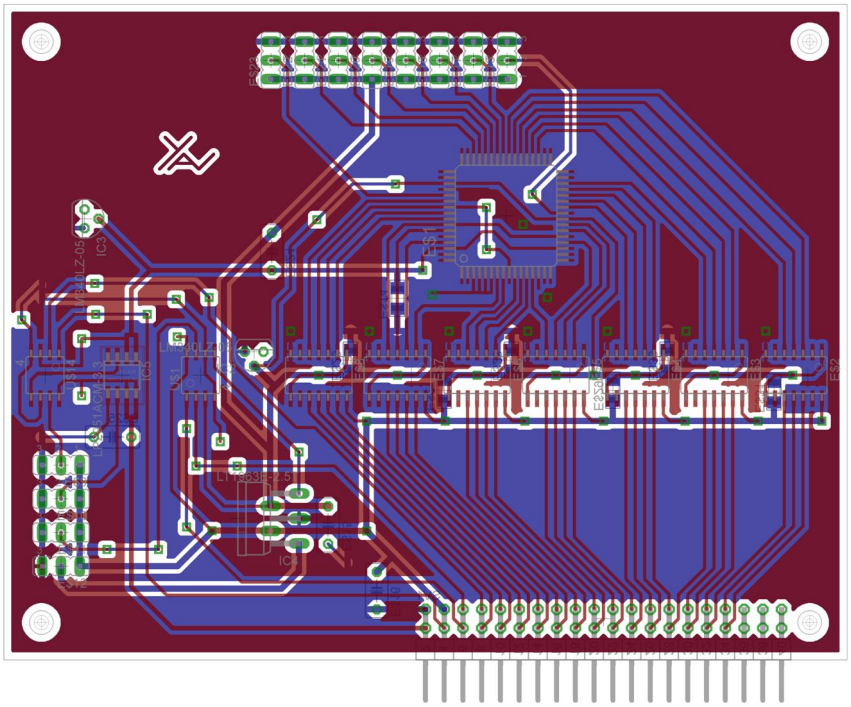

Figure 4. 4: Layout of the test board

Table 4.1 lists the ports distribution [38]. GND is a shared port among VSSIOCOs, PPLs, floating, PPSUB and also for the chipset from the power generation circuits. VU (+5) is connected to the input of one power generation circuit. It supplies 0.5V~1.2V power to the chip's core. VCCO (+3.3V) is connected to the input of the other power generation circuit. It supplies 1.0V~2.5V power to V_{ccb} terminal of the voltage translators [39]. (E6) and (C5) controls the INC signals in potentiometers from 0.5V~1.2V and 1.2V~2.5V power rail respectively. (D5) and (D6) controls the U/D signals in potentiometers from 1.2V~2.5V and 0.5V~1.2V power rail respectively.

N_RESETB_00 and N_RESETB_01 are combined with C_RESET_00 and C_RESET_01 respectively to save port number.

Table 4. 1: Interface connector

ICLSKYAN	FPGA Pin	Connector		FPGA Pin	ICLSKYAN
*	GND	1	2	VU (+5)	**
***	VCCO (+3.3V)	3	4	(E6)	#1
#2	(D5)	5	6	(C5)	#3
#4	(D6)	7	8	(C6)	CLK_00
C_RESET_00	(E7)	9	10	(C7)	REPORT_00
REPORT_01	(D7)	11	12	(C8)	C_RESET_01
REPORT_02	(D8)	13	14	(C9)	FD1QSVTX1_ERR
GG_DICE_ERR	(D10)	15	16	(A3)	DICE_ERR
FD1QSVTX1_ERR2	(B4)	17	18	(A4)	CLK_01
GG_DICE_ERR2	(B5)	19	20	(A5)	DICE_ERR2
SERT_ERR	(B6)	21	22	(B7)	HOLD
Qout(Jasim)	(A7)	23	24	(B8)	HOLD
Qout(NASA)	(A8)	25	26	(A9)	SHIFT
CLKIN	(B10)	27	28	(A10)	RESET
OUT6	(B11)	29	30	(B12)	OUT5
testSEU	(A12)	31	32	(B13)	OUT3
OUT2	(A13)	33	34	(B14)	OUT1

Chapter 5

Radiation-Tolerant Cross-Coupled LC VCO

A voltage-controlled oscillator (VCO) is a frequency varying circuit. Its output frequency varies according to the voltage input. It is widely used in many systems, for instance frequency synthesizer, clock and data recovery circuit and clock generator. Cross-coupled LC VCO is frequently used due to the simple structure and outstanding phase noise performance. In space applications, the radiation effects appear as extra noise sources, which can degrade the phase noise level. Previous researchers have investigated the impact of SETs on cross-coupled LC VCOs from laser beam tests and simulations. Similar circuit topologies were fabricated in different technologies. Results indicated that SETs can distort the output spectrum. The recovery time from the perturbation is determined by the recovery time of the affected transistor and the start-up time of the oscillator, whereas, is not related to the resonance frequency [40].

In this work, the behavior of cross-coupled LC VCOs encountering SETs is imitated by Cadence Spectre. Circuits are implemented with STM CMOS 90 nm general silicon-based process. Different operating points are analyzed to find the key parameters affecting the radiation tolerance. The remainder of this chapter is arranged as follow: Section 5.1 reviews the principles of cross-coupled LC VCOs; since the monolithic inductor is a critical component, Section 5.2 briefly discusses the layout techniques;

Section 5.3 introduces the simulation methodologies and analyzes the results; Section 5.4 makes a conclusion and gives design suggestions for space applications.

5.1 Cross-Coupled LC VCOs

A Cross-coupled LC VCO can be implemented with the complementary MOS structure or the NMOS/PMOS only structure. The former exhibits outstanding phase noise level and power efficiency under high voltage supply, while the latter is frequently adopted in low voltage designs [41]. Normally, circuits implemented in advanced processes are working under low voltages.

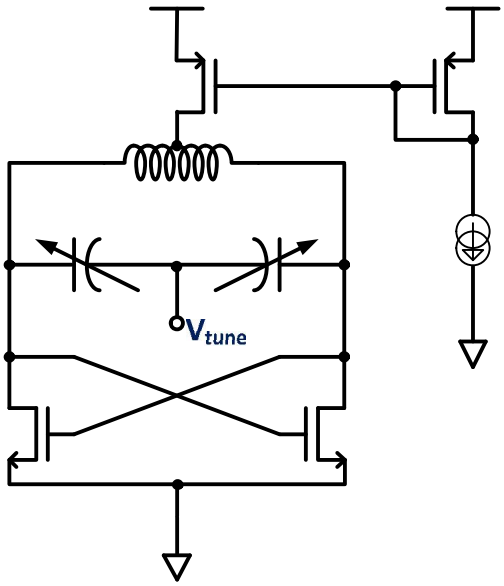

Figure 5. 1: Cross-coupled LC VCO with PMOS current source

Figure 5.1 is the LC VCO based on NMOS transistor pair. Two common source amplifiers form a close loop system. Each one provides a 180 degree phase shift. The loop gain must be greater than unity gain to sustain the oscillation:

$$G_M \times R_P \geq 1 \tag{5.1}$$

Where, G_M is the small signal gain; R_P is the equivalent parallel resistance of the resonator due to the non-ideality of the inductor and varactor. In order to guarantee a reliable start-up of the oscillation, the excess loop gain $G_M R_P$ is normally designed greater than 2.

The self resonance frequency is determined by the inductance of the inductor and the capacitance of the varactor:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{5.2}$$

The quality factor - Q is a critical parameter. It is determined by the quality factors of the inductor - Q_L and varactor - Q_C:

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{5.3}$$

Q_L and Q_C can be further expressed as [42]:

$$Q_L = \frac{\omega_0 L}{R_L} \tag{5.4}$$

$$Q_C = \frac{1}{\omega_0 R_C C} \tag{5.5}$$

Where, R_L and R_C are the equivalent series resistances of the inductor and varactor, respectively.

For monolithic devices, Q_C is much larger (greater than 20) than Q_L (around 10). So Q_L plays an important role in the overall quality factor. The equivalent shunt resistance R_{pL} of the inductor is determined by [42]:

$$R_{pL} = R_L(Q_L^2 + 1) = \frac{\omega_0 L(Q_L^2 + 1)}{Q_L} \tag{5.6}$$

For a reasonable large Q_L:

$$Q_L = \frac{R_{pL}}{\omega_0 L} \tag{5.7}$$

R_{pL} dominates the equivalent tank resistance R_P. It is proportional to Q_L. To satisfy Equation 5.1, increasing R_P can reduce the requirement for small signal gain.

Phase noise is a metric of the spectrum purity, which is an important parameter for a VCO. It is estimated by [41]:

$$L\{\Delta\omega\} = 4KTR_P \cdot (1 + \gamma n G_m R_P) \cdot \frac{G_m R_P}{2} \cdot \left(\frac{1}{2Q}\right)^2 \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \frac{2}{V_A^2} \tag{5.8}$$

where, K is Boltzmann constant, T is temperature in Kelvin; γ is the excess noise of active devices, 2/3 for long channel MOS transistor; n takes into account the bulk transconductance modulation by channel thermal noise, n=1.5; V_A is the sinusoidal voltage over the resonator. According to Equation 5.1 and 5.8, the excess loop gain must be large enough to meet the oscillation start-up requirement. On the other hand, it is expected to be as small as possible to improve the phase noise level.

Varactor is a tunable capacitor and the tuning range is determined by the ratio of C_{max} /C_{min}. The capacitance is controlled by the bias voltage. When building the resonator, the gate terminals of varactors should be connected to the oscillation nodes to reduce the parasitic capacitances [43]. In this work, PMOS varactors are used to build the LC tank. The bulk is used as the voltage tuning terminal without the source and drain connection.

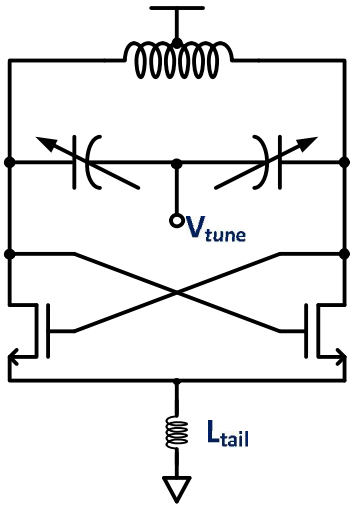

Figure 5. 2: Cross-coupled LC VCO without current source

LC VCOs can also be implemented without the current source transistor. As shown in Figure 5.2, the absence of the current source transistor reduces the necessary supply voltage. Hence, it is a good solution for low power and low voltage designs. A tail inductor with appropriate value can be added between the NMOS transistor pair and ground. This inductor can eliminate the noise from power rail and attenuate the effect of harmonics at the output node [44]. As a matter of fact, the tail inductor does not have quality factor issue as the ones in the resonator. So the layout becomes more flexible.

5.2 Monolithic Inductor

According to the previous analyses, the most effective way to improve the phase noise level is to use large Q_L inductors. This section briefly introduces the monolithic inductor and the methods to increase its quality factor.

Q_L is a parameter strongly related to fabrication processes and layout styles. Figure 5.3 is the inductor model with parasitical parameters [45]. There are two main mechanisms contribute to the energy loss. One is the series resistance due to the nature of inductor's material. The other one is the eddy current caused by the magnetic field due to the low resistive dielectrics and substrates.

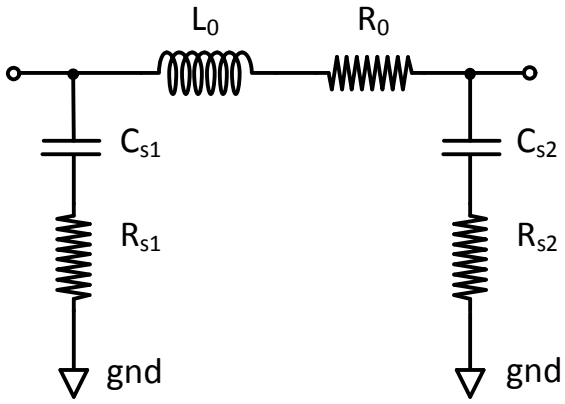

Figure 5. 3: π model of monolithic inductor

From Equation 5.6, increasing the shunt resistance or reducing the series resistance is the key to achieve a high quality factor. Series resistance can be reduced from using low resistivity and large cross section area metal. Multi layers of metal can also be connected in parallel to realize it. To achieve a high Q value, the inner diameter of the

inductor should be kept large, while maintaining relatively small outer radius. The space between the coils should be carefully chosen to minimize the parasitic capacitance [46].

The eddy current in the substrate can generate a magnetic field in the reversed direction to counteract the original one. Research showed that for a few nano henries' monolithic inductor, the series resistance dominates the loss of the device at low frequencies (under 1GHz), while the substrate effect dominates at high frequencies (greater than 1GHz) [43][44]. Placing a patterned ground shields (PGS) underneath the inductor is an effective way to isolate the inductor from the lossy substrate. Grounded metal and polysilicon strips are interlaced under the coils. The PGS can prevent the magnetic field from penetrating into the substrate, and equalize the potential to minimize the eddy current. Figure 5.4 is the layout view of PGS.

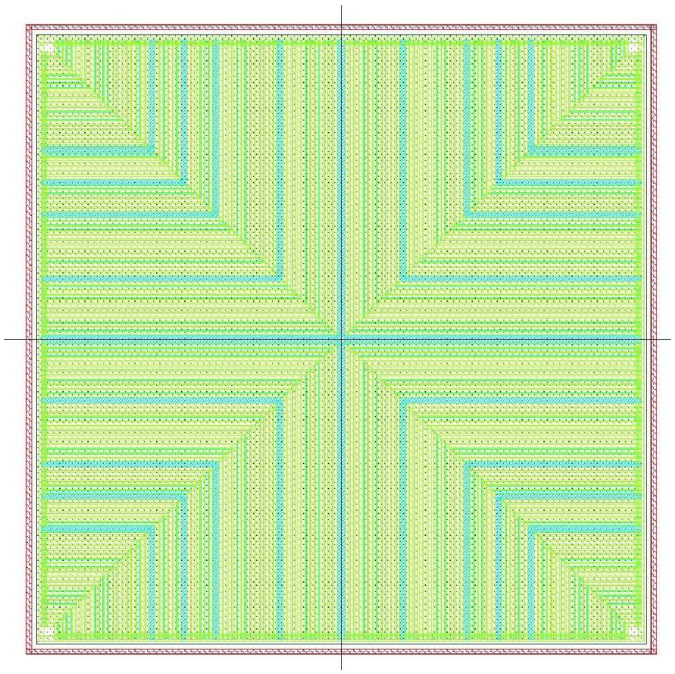

Figure 5. 4: Patterned ground shield (PGS)

Figure 5.5 shows an example of a cross-coupled LC tank VCO's layout. The metal wall around the inductor works as a Faraday cage, which isolates the electromagnetic field and protects the active devices from the electromagnetic interference (EMI). The cross coupled MOSFETs are also isolated by deep N-wells for the same reason. The PGS is provided by the foundry, and the layout style is invisible. The whole structure is highly symmetrical to improve the spectrum purity.

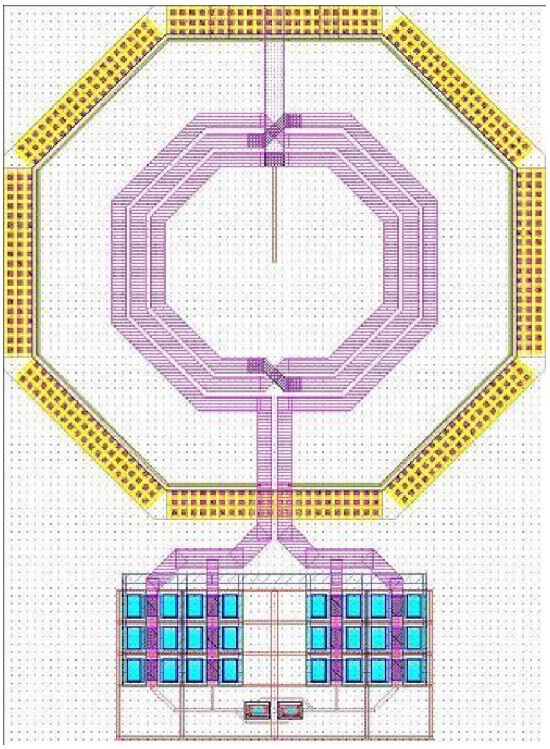

Figure 5. 5: The layout view of the LC VCO

5.3 SET Simulation Methodologies and Result Analyses

According to the analyses in chapter 2, the cross-couple transistor pair is sensitive to the radiation. To quantitatively analyze the spectrum distortion for each type of LC

VCO, Cadence Spectre/SpectreRF is applied for the circuits' analyses and SETs simulation. The SET pulses are imitated by double-exponential current sources. The circuits are divided into two groups: the LC VCO without current source (the circuit topology shown in Figure 5.2) and the one with current source (the circuit topology shown in Figure 5.1). In the first group, circuits with and without the tail inductor, supplied by high voltage and low voltage are analyzed. In the second group, circuits are working under different bias currents.

In reality, the duration of SET ranges from few tens of pico seconds to few nano seconds. These components are close to the working frequencies of typical LC VCOs. The closer the perturbation is to the oscillation frequency, the greater the amplification of the noise (Alternatively, the SETs can be traded as a special noise source). To make the results comparable without losing generality, the single ion strike is imitated by a 2ns double exponential pulse. The amplitudes of transient voltages and currents are proportional to V_{DS} and the current flowing into the drain, respectively. The small signal transconductances of NMOS transistor under different circuits and supply voltages are set identical for each case to make the results comparable. The center frequencies are 5 GHz.

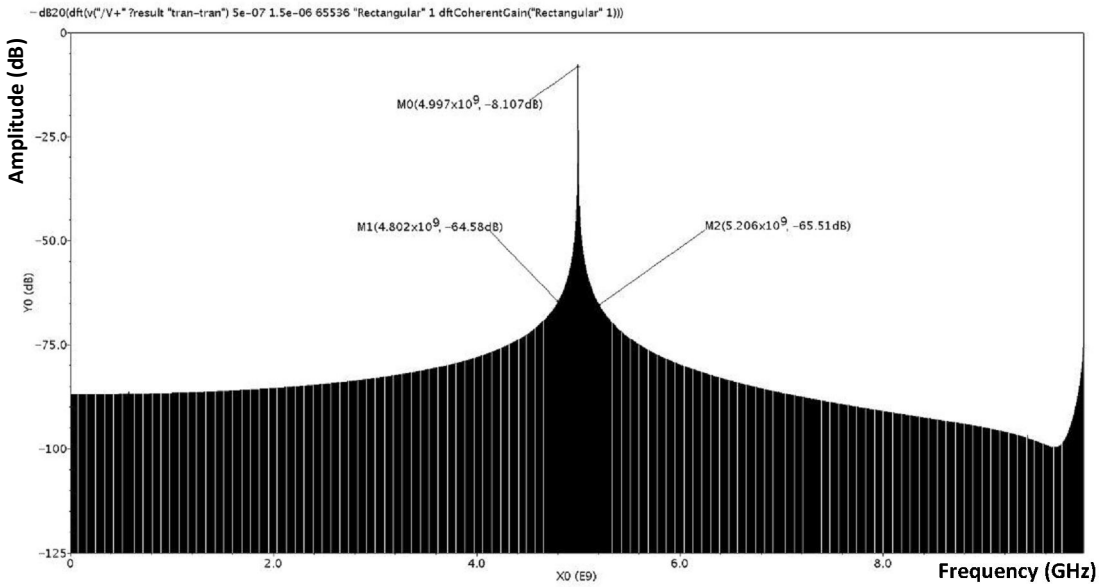

Figure 5. 6: Diagram of the output spectrum from the circuit working under 1V supply and 2.8 mA bias current.

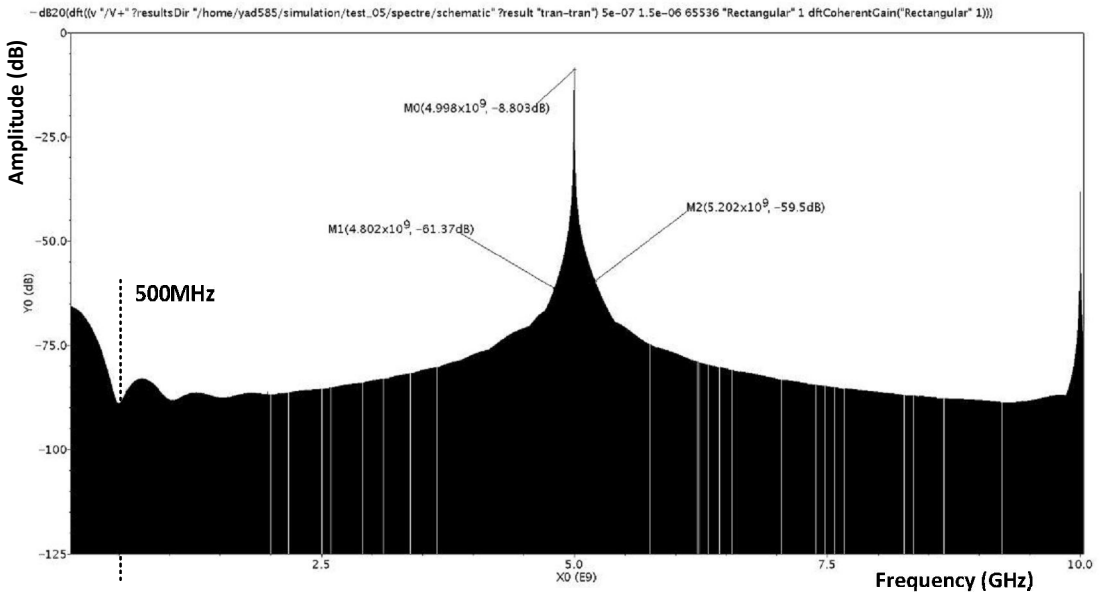

Figure 5. 7: Diagram of the output spectrum after introducing SET.

Comparing Figure 5.7 with 5.6, serious distortion can be observed around 500MHz due to the 2 ns transient. The "skirt" becomes “fat” after the ion strike. Because the noise component is close to the center frequency, it is impossible to filter it out completely. The cross-coupled LC VCO is a regenerative feedback system. It can accumulate and amplify the perturbation until the transient fades away and the circuit recovers. In order to find out an optimal solution for space applications, it is reasonable to focus on the circuit topologies and the key parameters.

When considering the supply voltage, there is a tradeoff between the phase noise level, tuning range and power consumption. Lowering the voltage can directly reduce the power. However, the output swing will also be reduced, which will degrade the phase noise level. On the other hand, the size of cross-coupled transistors must be increased to meet the small signal transconductance requirement. In our case, 800mV and 500mV supplies are chosen for the first group.

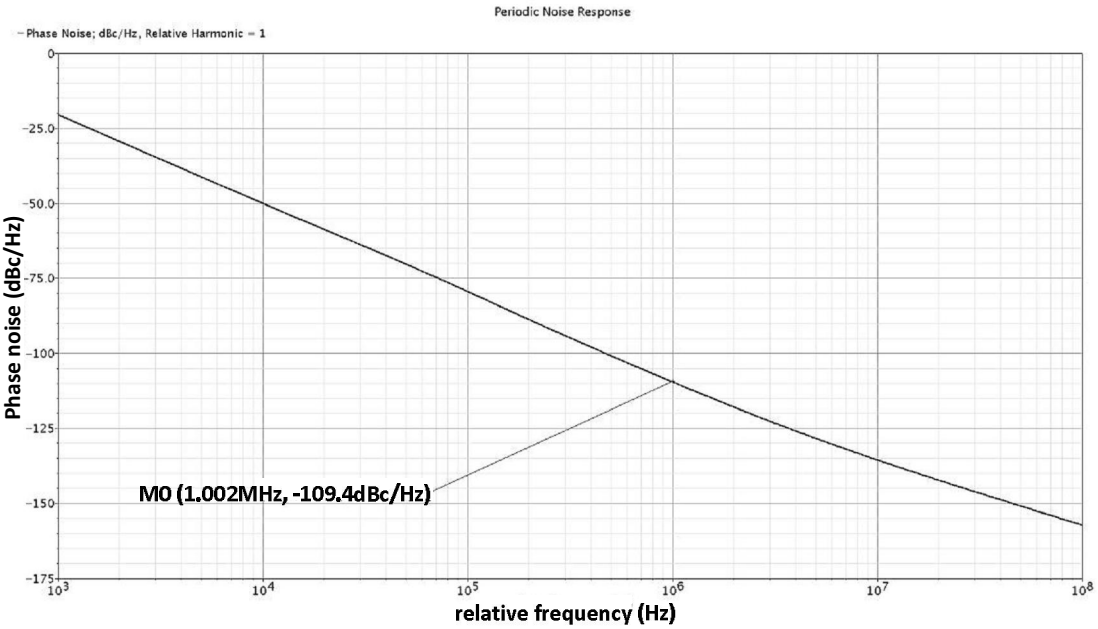

Figure 5. 8: The plot of phase noise to the circuit without tail inductor.

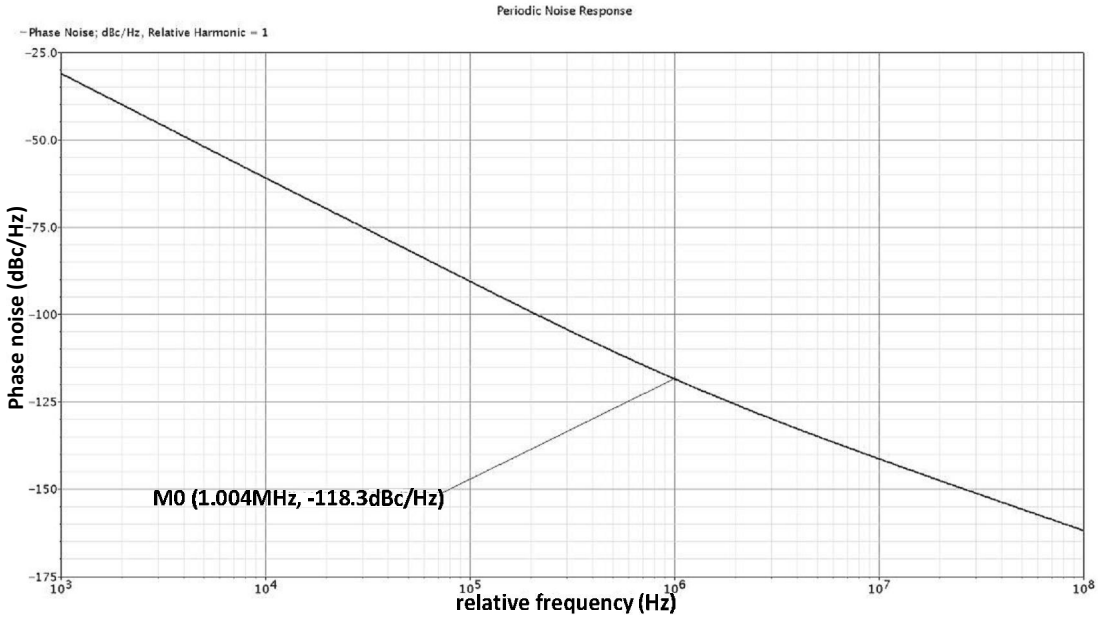

Figure 5. 9: The plot of phase noise of the circuit with tail inductor.

As shown in Figure 5.9 and 5.8, circuit with 800 mV supply and tail inductor exhibits better phase noise performance due to the current restriction effect. However, this effect also makes the tail current difficult to be changed instantaneously, which means the transient current in one transistor has an influence on the current in the other one. Moreover, the tail inductor is a barrier between the transistors and ground. It has a negative influence on the net charge (the holes generated by energetic particle) absorption. Similar phenomena is also observed in the circuit with 500mV supply and tail inductor.

In the second group, the center voltage is set to 500 mV so as to compare with the corresponding configuration in the first group. The bias current is set large enough to make the circuits working in the voltage limited regime. Similar to the tail inductor, the current source also restricts the total current. However, the good thing is that due to the absence of tail inductor, the charge can be absorbed by the power rail faster.

Table 5.1 lists several representative data. DC and Average Current are measured before and after oscillation, respectively. The tail inductor can reduce the transconductance by restricting the average current, and hence improves the phase noise level in ordinary designs. The restriction effect becomes remarkable for large swing and large current applications. However, it is not a good choice for radiation tolerant designs. The amplitude values are measured from 200 MHz offset frequency. From the results, circuits with tail inductor have 10 dB and 20 dB degradation during SET simulations. While for the ones with current source, the degradations are around 5dB. The circuit without tail inductor and current source, working under 800mV supply

exhibits the best radiation tolerance (the lightest spectrum distortion). The direct ground connection makes the net charge absorption fast. Transistor working in the deep saturation region is not sensitive to the SET introduced perturbations.

Table 5. 1: Comparison of cross-coupled LC VCOs

LC VCO Type	W/L	DC (mA)	Average Current (mA)	Spectrum Distortion Under Normal / SET Simulation (dB)
800mV supply	75	6.54	5.70	(-63.71, -57.62) / (-64.79, -57.66)
800mV supply and tail inductor	75	6.54	4.98	(-81.83, -80.99) / (-57.18, -56.64)
500mV supply	135	2.62	2.96	(-70.53, -73.94) / (-64.59, -69.52)
500mV supply and tail inductor	135	2.62	2.72	(-71.49, -69.51) / (-61.85, -60.4)
1V supply and 4mA bias current	100	3.52	2.96	(-67.98, -69.33) / (-61.43, -55.6)
1V supply and 2.8mA bias current	135	2.66	2.28	(-64.58, -65.51) / (-61.37, -59.5)

5.4 Conclusions

In this chapter, we analyzed the influence of SETs toward the frequency responses of the cross-coupled LC VCOs. The behavior of the SET is modeled; two frequently adopted structures are simulated by Cadence Spectre/SpectreRF. From quantitative analyses, the optimum solution for radiation tolerant design is the one with simplest structure. The direct power connection and transistors working in the deep saturation mode have positive influences on the radiation tolerance. The SET influence on PMOS

transistors is not discussed due to the lack of data showing the exact response under the same radiation intensity as for the NMOS transistor. However, from radiation-tolerant point of view, the less and smaller of active devices, the lower probability the circuit will be affected. The presence of PMOS transistor will enlarge the area of active devices, and degrade the reliability.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

This work investigated the influence of the SEEs towards CMOS 90nm technology. In the first part, three types of radiation tolerant registers were implemented. The clock control plans were carefully chosen so that there is no floating storage node during the whole clock cycle. The register based on DICE suffered the "conflict" phenomenon when encountered a SEU, while the other radiation tolerant designs were free from this phenomenon. Compared to the standard cell from the digital library, they had more transistors because the dual interlocked storage cells were more complicated. So the layouts consumed 3~4 times larger areas. They also have greater propagation delays due to the relatively larger internal loads.

Two built-in test structures were designed to count the SEU rates of the registers so as to evaluate their radiation tolerances. On the one hand, the CREST was capable of detecting the single event MBU, whereas the SEUDC could not. This property made the CREST very useful for the situation that the particles travel in grazing incident angles. On the other hand, the SEUDC could detect the SEUs not only from the internal of the registers but also caused by the SETs from inputs.

A SET pulse width measurement circuit with 64 measurement cells was also implemented. According to the simulations, the circuit could reliably capture and measure the voltage pulses ranging from 90 ps to 2 ns. The error tolerance was one cell's delay (that is 45.3 ps).

The test bench was made up of the test PCB and the XILINX Spartan-3 FPGA board. The test PCB provided tunable powers to the translators, I/O pad and the core. It communicated with the FPGA board through the 40-pin interface. The FPGA board assisted to count the SEU rates from the registers and calculate the SET pulse widths from the combinational logic circuits.

In the second part of this work, two frequently used cross-coupled LC VCOs with different operating points were studied. The SET was imitated and the frequency responses were simulated with Cadence Spectre. The current restriction effect of the tail inductor could improve the phase noise performances for the regular applications. However, the corresponding output spectra were seriously distorted after introducing SETs, because the inductor could slow down the charge absorption speed. The direct power connection had a positive influence on the charge absorption. Moreover, transistors working in the deep saturation region become insensitive to the perturbations introduced by SETs.

6.2 Future Works

In the future, the test bench will be sent out for energetic particle test. The radiation tolerances of the registers will be evaluated under different supply voltages and clock

frequencies. The circuit will be exposed to various radiation intensities to establish the relation between the particle energy and the SET pulse width.

During the study of cross-coupled LC VCOs, the parameters related to the SET simulations were arbitrary. It is necessary to establish a relation between the radiation intensity and the frequency response. Therefore the behavior of the circuit can be predicted.

As mentioned in the beginning of this thesis, SEEs are becoming a serious problem as the shrinking of the feature size, increasing of the integration density and working frequency. It is significant to carry out researches on the SEE detection and mitigation technologies in a more advance technology.

Appendix
Inductor Synthesization

ASITIC is used to synthesize the monolithic inductor [45]. The rule file and mapping table come from the CMC discussion forums [47]. This appendix shows our inductor synthesization process.

ASITIC> optpoly

Desired Inductance, Accuracy (+/-)? (nH) 1.1 1

Name? ind

Length (2*Radius)? 200

How many sides? 8

Spacing? 4

Min/Step/Max Width? 8 0.005 12

Metal layer? 6

Frequency? (GHz) 5

Simulation started at:

Simulation ended at:

Pi Model at f=5 GHz: Q = 14.53 , 14.68 , 15.49

L = 1.089 nH R = 2.077

Cs1 = 20.35 fF Rs1 = 541.9

Cs2 = 20.34 fF Rs2 = 472.9 Est. Resonance = 33.8 GHz

Found: n =2.2500, w =11.5100, s =4.0000, L =1.0893 (nH), Q = 14.5272

ASITIC> cp ind ind00 7

ASITIC> joinshunt ind ind00

ASITIC> set timing=true

ASITIC> pix ind 5

maxL = 1500.00, maxT = 0.97, maxW = 0.97 (lambda = 30000.00, delta = 1.21)

Performing Analysis at 5 GHz

Generating capacitance matrix (72x72).Could not open data file at frequency = 5.00. Tried using . as path.

Generating data at 5.00 GHz...

Calculating Green Function...

Computing FFTs...

Writing data.....

Generating inductance matrix (432x432).....

Ind Timing: tot = 6368, setup = 25, fill = 2350

invert = 3979, reduce = 14, eddy = 00

Calc Times (ms): total = 29222, cap = 22853, ind = 6368, node = 00

Pi Model at f=5 GHz: Q = 15.14 , 15.21 , 18.18

L = 993.3 pH R = 1.385

Cs1 = 44.61 fF Rs1 = 438.3

Cs2 = 42.36 fF Rs2 = 522.2 Est. Resonance = 23.91 GHz

References

[1] Van Allen radiation belt. http://en.wikipedia.org/wiki/Van_Allen_radiation_belt

[2] http://www.windows.ucar.edu/tour/link=/glossary/radiation_belts.html&edu=high

[3] Marc Poizat, "Space Environment and Effects" http://space.epfl.ch/webdav/site/space/shared/industry_media/02%20EPFL_space_environment.pdf

[4] Ptak, Andy (1997). "Ask an Astrophysicist". NASA GSFC. Retrieved 2006-06-11. http://imagine.gsfc.nasa.gov/docs/ask_astro/answers/970228a.html

[5] Alessandro Paccagnella, "Single Event Effects: Introduction" http://sirad.pd.infn.it/scuola_legnaro_2007/Presentazioni_pdf/12_Paccagnella_PartA.pdf

[6] F. Sturesson, "Single Event Effects (SEE) Mechanism and Effects," http://space.epfl.ch/webdav/site/space/shared/industry_media/07%20SEE%20Effect%20F.Sturesson.pdf

[7] Single Event Effects. http://holbert.faculty.asu.edu/eee560/see.html

[8] J.T. Wallmark, S.M. Marcus, "Minimum size and maximum packaging density of non-redundant semiconductor devices," *Proc. IRE*, vol. 50, pp. 286-298, March 1962.

[9] D. Binder, E.C. Smith, and A.B. Holman, "Satellite anomalies from galactic cosmic rays, " *IEEE Trans. Nucl. Sci.*, vol. 22, pp. 2675–2680, Dec. 1975.

[10] C.S. Guenzer, E.A. Wolicki, and R.G. Allas, "Single event upset of dynamic RAM's by neutrons and protons, " *IEEE Trans. Nucl. Sci.*, vol. 26, pp. 5048–5053, Dec. 1979.

[11] W.A. Kolasinski, J.B. Blake, J.K. Anthony, W.E. Price, and E.C. Smith, "Simulation of cosmic-ray induced soft errors and latchup in integrated-circuit computer memories, " *IEEE Trans. Nucl. Sci.*, vol. 26, pp. 5087–5091, Dec. 1979.

[12] T.C. May and M.H. Woods, "Alpha-particle-induced soft errors in dynamic memories, " *IEEE Trans. Electron Devices*, vol. 26, pp. 2–9, Feb. 1979.

[13] Hugh J. Barnaby, "Will Radiation-Hardening-by-Design (RHBD) Work?" http://www.ieee.org/organizations/pubs/newsletters/npss/0305/rhbd.html

[14] Calin T., Nicolaidis M., and Velazco R., "Upset hardened memory design for submicron CMOS technology," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 6, pp. 2874-2878, Dec. 1996.

[15] Casey M.C., Bhuva B.L., Black J.D., Massengill L.W., Amusan O.A., and Witulski A.F., "Single-Event Tolerant Latch Using Cascode-Voltage Switch Logic Gates," *Nuclear Science, IEEE Transactions on*, vol. 53, no. 6, pp. 3386-3391, Dec. 2006.

[16] Balasubramanian A., Bhuva B.L., Black J.D., and Massengill L.W., "RHBD techniques for mitigating effects of single-event hits using guard-gates," *Nuclear Science, IEEE Transactions on*, vol. 52, no. 6, pp. 2531- 2535, Dec. 2005.

[17] Shuler R.L., Bhuva B.L., O'Neill P.M., Gambles, J.W., and Rezgui, S., "Comparison of Dual-Rail and TMR Logic Cost Effectiveness and Suitability for FPGAs With Reconfigurable SEU Tolerance," *Nuclear Science, IEEE Transactions on*, vol. 56, no. 1, pp. 214-219, Feb. 2009.

[18] "Single Event Effects Testing" http://www.aero.org/capabilities/seet/primer.html

[19] Dong Pan, H.W. Li, and B.M. Wilamowski, "A radiation hard phase-locked loop," *in Industrial Electronics, 2003. ISIE '03. 2003 IEEE International Symposium on*, vol. 2, pp. 901–906 vol. 2, June 2003.

[20] P.E. Dodd and L.W. Massengill, "Basic mechanisms and modeling of single event upset in digital microelectronics," *Nuclear Science, IEEE Transactions on*, vol. 50, no. 3, pp. 583–602, June 2003.

[21] Massengill L.W., Amusan O.A., Dasgupta S., Sternberg A.L., Black J.D., Witulski A.F., Bhuva B.L., and Alles M.L., "Soft-Error Charge-Sharing Mechanisms at Sub-100nm Technologies," *Integrated Circuit Design and Technology, 2007. ICICDT '07. IEEE International Conference on*, pp.1-4, May 30, 2007-June 1, 2007.

[22] "Single event upset," http://en.wikipedia.org/wiki/Single_event_upset

[23] Aashish Agrawal, "Radiation Effects in Microelectronics" http://www.nd.edu/~gsnider/EE698A/Agrawal_radiation_effects.ppt

[24] "Total Ionizing Dose," http://holbert.faculty.asu.edu/eee560/tiondose.html

[25] Marc Poizat, "Total Ionizing Dose Mechanisms and Effects," http://space.epfl.ch/webdav/site/space/shared/industry_media/03%20EPFL_TID_Basic-Mech.pdf

[26] Marshall P., Carts M., Currie S., Reed R., Randall B., Fritz K., Kennedy K., Berg M., Krithivasan R., Siedleck C., Ladbury R., Marshall C., Cressler J., Guofu Niu, LaBel K., and Gilbert B. "Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5AM SiGe circuit for radiation effects self test (CREST)," *Nuclear Science, IEEE Transactions on*, vol. 52, no. 6, pp. 2446- 2454, Dec. 2005.

[27] Shuler R.L., Kouba C., and O'Neill P.M. "SEU performance of TAG based flip-flops," *Nuclear Science, IEEE Transactions on*, vol. 52, no. 6, pp. 2550- 2553, Dec. 2005.

[28] B. Narasimham, V. Ramachandran, B. L. Bhuva, R. D. Schrimpf, A. F. Witulski, W. T. Holman, L. W. Massengill, J. D. Black, W. H. Robinson, and D. McMorrow, "On-chip characterization of single event transient pulse widths, " *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 4, pp. 542–549, Dec. 2006.

[29] P. Eaton, J. Benedetto, D. Mavis, K. Avery, M. Sibley, M. Gadlage, and T. Turflinger, "Single event transient pulse width measurements using a variable temporal latch technique," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 3365–3368, Dec. 2004.

[30] Ferlet-Cavrois V., Paillet P., McMorrow D., Torres A., Gaillardin M., Melinger J.S., Knudson A.R., Campbell A.B., Schwank J.R., Vizkelethy G., Shaneyfelt M.R., Hirose K., Faynot O., Jahan C., and Tosti L., "Direct measurement of transient pulses induced by laser and heavy ion irradiation in deca-nanometer devices," *Nuclear Science, IEEE Transactions on*, vol. 52, no. 6, pp. 2104- 2113, Dec. 2005.

[31] Nicolaidis M., and Perez R., "Measuring the width of transient pulses induced by ionising radiation," *Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International* , pp. 56- 59, 30 March-4 April 2003.

[32] Narasimham B., Bhuva B.L., Schrimpf R.D., Massengill L.W., Gadlage M.J., Amusan O.A., Holman W.T., Witulski A.F., Robinson W.H., Black J.D., Benedetto J.M., and Eaton P.H., "Characterization of Digital Single Event Transient Pulse-Widths in 130-nm and 90-nm CMOS Technologies," *Nuclear Science, IEEE Transactions on*, vol. 54, no. 6, pp. 2506-2511, Dec. 2007.

[33] DS1804Z-100. http://datasheets.maxim-ic.com/en/ds/DS1804.pdf

[34] LP38511MR-ADJ/NOPB. http://www.national.com/ds/LP/LP38511-ADJ.pdf

[35] LP3964ET-ADJ/NOPB. http://www.national.com/ds/LP/LP3961.pdf

[36] LM385LP-1-2. http://focus.ti.com/lit/ds/symlink/lm285-1.2.pdf

[37] LM385LP-2-5. http://focus.ti.com/lit/ds/symlink/lm285-2.5.pdf

[38] Spartan-3 FPGA Starter Kit Board User Guide. http://www.xilinx.com/support/documentation/boards_and_kits/ug130.pdf

[39] TXB0104PWR. http://focus.ti.com/lit/ds/symlink/txb0104.pdf

[40] Wenjian Chen, V.Pouget, H.J. Barnaby, J.D. Cressler, Guofu Niu, P. Fouillat, Y. Deval, and D. Lewis, "Investigation of single-event transients in voltage-controlled oscillators," *Nuclear Science, IEEE Transactions on*, vol. 50, no. 6, pp. 2081–2087, Dec. 2003.

[41] B. D. Muer and M. Steyaert, "CMOS Fractional-N Synthesizers Design for High Spectral Purity and Monolithic Integration," *Kluwer Academic Publishers*, 2003.

[42] Ryan Norris, "LC Tank Voltage Controlled Oscillator Tutorial" http://www.asic.uwaterloo.ca/files/vcotut.pdf

[43] Han-il Lee, Tae-young Choi, Mohammadi S., and Katehi L.P.B., "An extremely low power 2 GHz CMOS LC VCO for wireless communication applications," *Wireless Technology, 2005. The European Conference on*, pp. 31-34, 3-4 Oct. 2005

[44] Hanil Lee and S. Mohammadi, "A subthreshold low phase noise CMOS LC VCO for ultra low power applications," *Microwave and Wireless Components Letters, IEEE*, vol.17, no.11, pp.796–798, Nov.2007.

[45] http://rfic.eecs.berkeley.edu/~niknejad//asitic.html

[46] Upadhyaya P., Rajashekharaiah M., Heo D., Rector D.M., and Yi-Jan Emery Chen, "Low power and low phase noise 5.7 GHz LC VCO in OOK transmitter for neurosensory application," *Microwave Symposium Digest, 2005 IEEE MTT-S International*, pp. 1539-1542, 12-17 June 2005

[47] https://forums.cmc.ca/forum.jspa?forumID=41